

Design, Fabrication, and Calibration of a MEMS based Sensing Rosette for Quantifying the Influence of Strain Engineering on the Piezoresistive Coefficients

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Abstract— Strain has been used extensively in enhancing the electron mobility for high speed and low power transistors. As stretching the silicon atoms away beyond their normal atomic space has a significant influence on the carrier mobility. In this paper, to study the effect of strained silicon on piezoresistivity, the strained silicon will be integrated into a ten element sensing rosette, that utilizes the unique properties of crystalline silicon over the (111) plane to fully extract the six stress components in fully temperature compensated manner. Two chips were designed and fabricated, where the pre-strain state was induced onto the silicon substrate during microfabrication. In the first design, a highly compressive film (stressor layer) was utilized to globally produce a tensile strain at the front side of the substrate where the sensing elements were fabricated. While in the second design, the stressor layer was patterned in a way allowing for inducing both local tensile and compressive transverse uniaxial pre-strain onto the substrate. In another word, stressor strip with intrinsic compressive stress will cause a tensile pre-strain underneath it and compressive stress on both sides. This allows for applying different local strain using the same stressor rather than using nitride capping for tensile or silicon germanium for compressive as used on strained based transistors. To evaluate the effect of the pre-strain on the piezoresistive coefficients, uniaxial, thermal, and hydrostatic loading will be utilized to calibrate both designs.

Keywords-component; Strain Engineering; MEMS; Piezoresistivity, local stressor, biaxial pre-strain, uniaxial pre-strain, intrinsic stress.

I. INTRODUCTION

STRAIN ENGINEERING is a cutting edge technology that is being employed mainly to enhance the performance of many CMOS devices [1] as shown in Figure 1. To continue Moore's

law without scaling, strain technology has been utilized in many high volume production, such as Intel [2], [3], IBM [4], Freescale [5], and Texas Instruments [6]. For decades, thermal mismatches [7], lattice mismatches [8], and non-equilibrium deposition [9] have been utilized extensively in producing pre-strain state globally and locally. For instance, stress accompanying with silicide and nitride layers were used on integrating strain with the CMOS devices as pictured in Figure 1. Since 1992, biaxial [10] [11] [12], uniaxial [13] [14], and three dimensional stress [15] were induced onto different transistors to allow for higher performance and speed without going smaller. Many techniques have been employed to apply different controlled strain, such as silicide [16], nitride capping [17], dual stress linear [18], shallow trenches isolation [15], stress memorization technique [13], and selective epitaxial Si-Ge/Si-C layer [3] [19] [20].

As mobility is directly related to the piezoresistive coefficients, these coefficients were utilized to evaluate the influence of strained silicon on the electron and hole mobility. Accordingly, strain engineering has high influence on the piezoresistive coefficients. Hence, strain would have a tremendous impact on the piezoresistive based sensing rosette. For instance, strain engineering could improve the sensitivity of piezoresistive based stress sensors by 30 percent [21]. In this work, a biaxial and transverse strain will be produced and integrated with a piezoresistive sensing rosette, which will allow for quantifying the effect of strain on the piezoresistive coefficients. Tensile and compressive transverse local strains are applied using the same stressing layer rather than using nitride capping for tensile or silicon germanium for compressive strain [2], [3]. Unlike other type of stress, transverse uniaxial stress has the same effect on both electron and hole mobility [16].

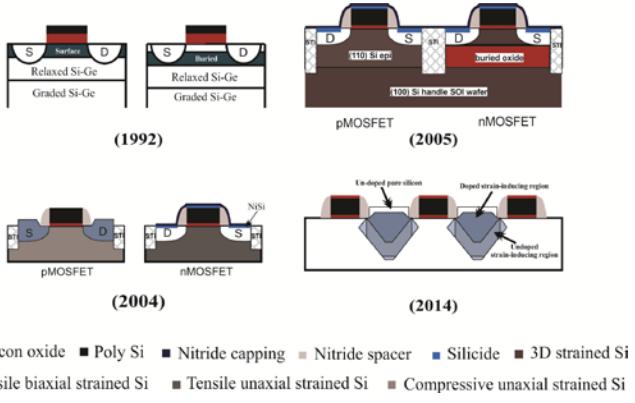


Figure 1. MOSFET structure changes in the past 30 years [2]

II. STRESSOR DESIGN

A ten-elements sensing rosette, which was developed by the author's group, was utilized to study both global biaxial and local uniaxial strain. This chip was fabricated on (111) silicon to develop a set of independent linear equations that yield the six stress components with full-temperature compensation [22], [23]. The strained silicon technology has been integrated during microfabrication via deposition of highly compressive plasma enhanced chemical vapor deposition (PECVD) nitride film that bends the substrate as plotted in Figure 2. This will produce a tensile biaxial strain at the top side of the substrate, where the sensing rosette is located. Considering that the in-plane stresses are equal on all directions and the (111) plane has isotropic elastic properties [24], the biaxial elastic modulus can be utilized to calculate the pre-stain. A compressive nitride film stress of 600 MPa was measured via the wafer curvature, however the finite element analysis for the stress distribution shows large stress losses up to 70% between the film and substrate.

The same stressing layer was patterned in a way allowing for producing uniaxial local strain onto the silicon substrate as shown in Figure 3. Both tensile and compressive strains were applied using the same layer. Also the shallow trenches technique was used to maximize the strain produced at the piezoresistors' area. The shallow trenches were etched on both sides of the piezoresistors using reactive ion etching. The effect of the stressors and the trenches was numerically studied extensively via ANSYS finite element software package. The result shows that nitride stressor would generate uniaxial tensile and compressive transverse stress around 50 MPa. The simulation indicates a dominant influence of film thickness on the stress transmitted to the silicon, which can reach up to 150 and -200 for tensile and compressive stress respectively, as presented in Figure 4. While the shallow trenches introduce more strain up to 200 and -250 MPa for tensile and compressive stress respectively.

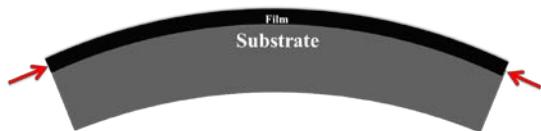


Figure 2. Curvature caused by highly compressive film

Canadian Microsystems Corporation (CMC).

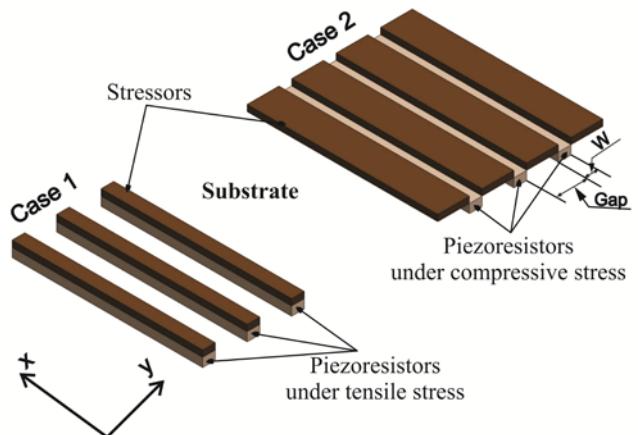


Figure 3. The mechanism of producing tensile and compressive pre-strain

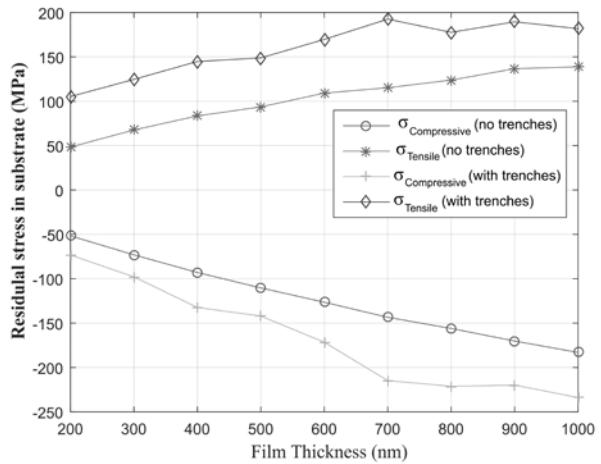
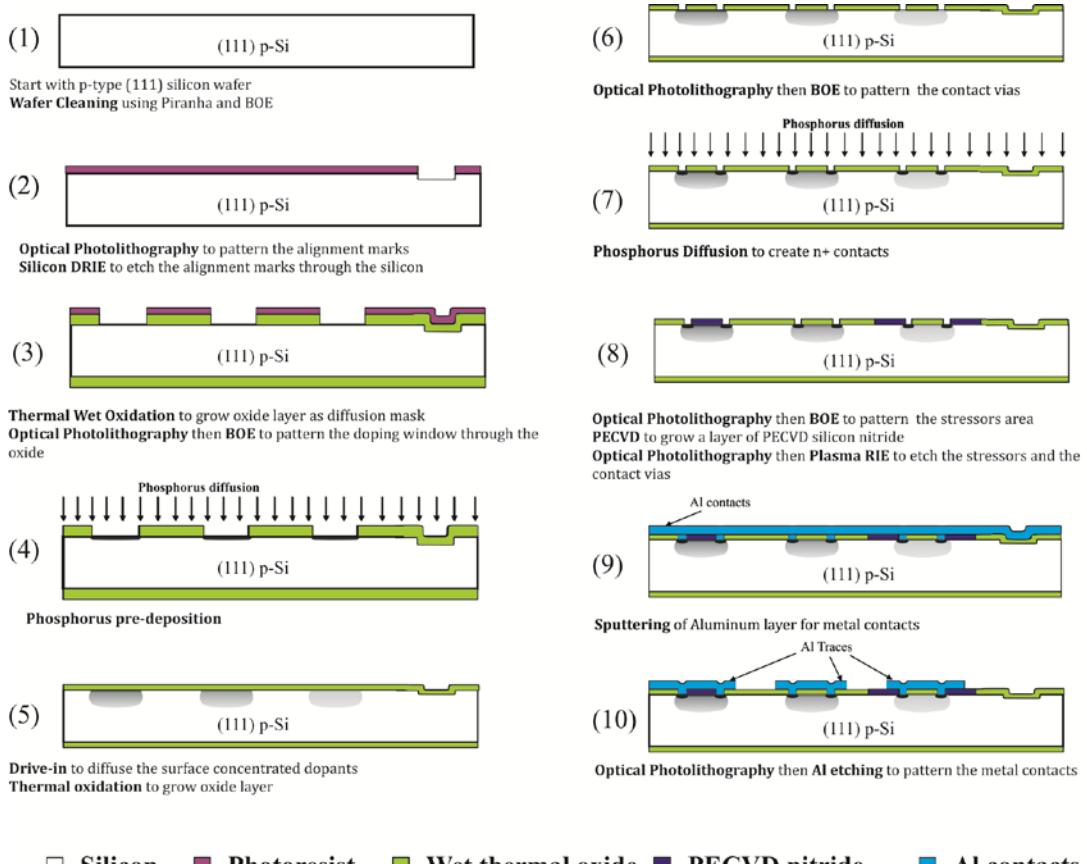


Figure 4. Stress transferred to the silicon versus the film thickness

III. MICROFABRICATION

Two different designs have been fabricated in the nanoFAB and the MEMS/NEMS Advanced Design Laboratory (ADL) at the University of Alberta. In the first design, a biaxial tensile pre-strain was induced at the front side of the substrate. While both tensile and compressive uniaxial stresses were integrated in the second chip. Both recipes were fabricated on a p-type (111) prime silicon wafers which were initially cleaned using piranha and buffered-oxide etches (BOE). The main fabrication steps are creating the piezoresistive sensing elements and applying the pre-stress state as represented in Figure 5. A highly compressive layer of PECVD silicon nitride was locally deposited to induce tensile and compressive strain onto the sensing elements rather than straining the whole wafer. Finally, prior to the metallization, an additional predeposition diffusion step was carried out to create n+ region at the contact vias to obtain ohmic contact behavior between Al and Si. The fabricated chips were experimentally characterized to assess the piezoresistors functionality. The concentration profile was measured using a time-of-flight secondary ion mass spectrometry (ToF-SIMS). Photomicrographs of both designs are shown in Figure 6 and Figure 7.



□ Silicon ■ Photoresist ■ Wet thermal oxide ■ PECVD nitride ■ Al contacts

Figure 5. Microfabrication process flow of strained ten-element sensing rosette

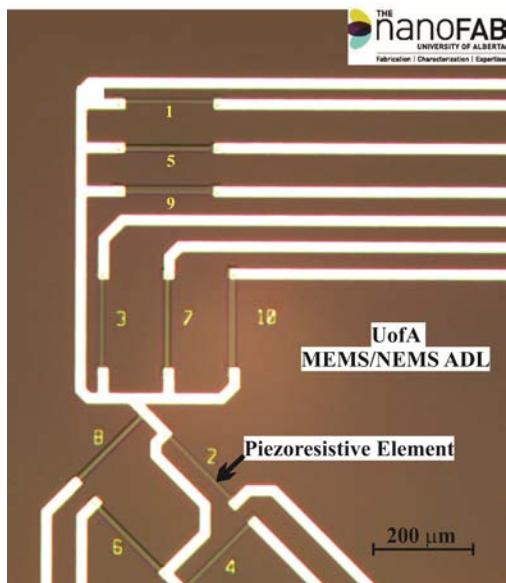


Figure 6. Photomicrograph of the microfabrication biaxial strained based sensing rosette

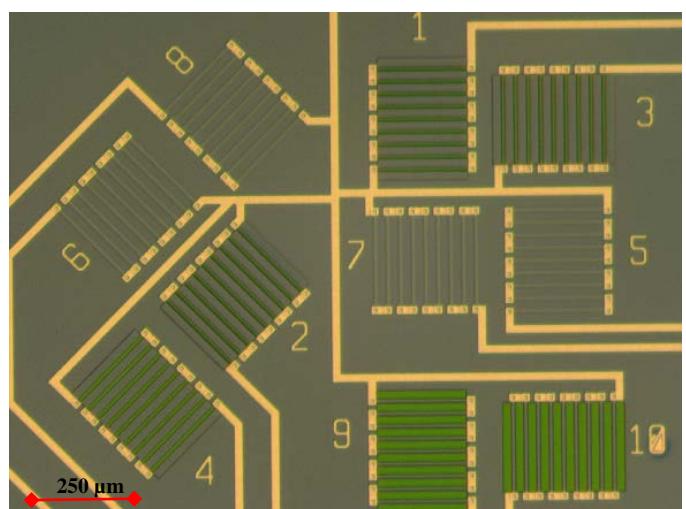


Figure 7. Photomicrograph of the microfabrication uniaxial strained based sensing rosette

IV. CALIBRATION

A full calibration of the piezoresistive coefficients over (111) (B_1 , B_2 , B_3) were carried out to quantify the influence of strained silicon on piezoresistive coefficients. The typical calibration results would be used to calculate the piezoresistive coefficients. This test was carried out using a four-point bending (4PB) setup, environmental chamber, and hydrostatic test [21]. Applying known uniaxial stress on the current fabricated sensing chip will give B_1 and B_2 directly, while hydrostatic load will measure B_3 . This calibration setup does not require packaging of the sensing die, where the calibration die is a part of a rectangular beam cut from the wafer, and is connected to a zero-insertion force (ZIF) connector using aluminum traces as shown in Figure 8. These aluminum traces are connected to voltmeter to provide six bias voltages which are enough for fully calibrating the piezoresistive coefficients. The resistance changes from the 0° sensing elements (R_1 , R_5 , and R_9) are used to determine the B_1 parameters, while B_2 was calibrated via the sensing elements oriented at 90° (R_3 , R_7 , and R_{10}) as shown in (1). Unlike the B_1 and B_2 , B_3 can be calculated from 0° or 90° sensing elements using the hydrostatic test.

$$B_1 = \frac{\partial}{\partial \sigma} \left(\frac{\Delta R_\phi}{R_0} \right) \quad \text{and} \quad B_2 = \frac{\partial}{\partial \sigma} \left(\frac{\Delta R_{90}}{R_0} \right) \quad (1)$$

The test procedure started with measuring the nominal resistance of the six piezoresistors at no load. Then the load was increased incrementally and measured. At each load increment, the resistances were measured again to calculate the change in resistance. Figures 9-11 show the typical results came from the calibration, where the slopes represent the B_1 , B_2 and B_3 .

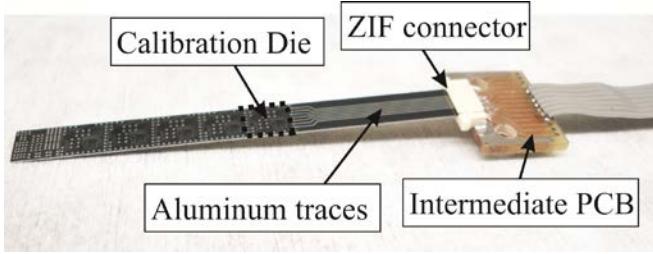


Figure 8. The silicon beam that used in calibration

V. CONCLUSION

In the frame of employing strain engineering on enhancing the performance of a MEMS 3D stress sensor, a strained based piezoresistive sensing rosette was developed for studying the effect of strain on the piezoresistive coefficients. The intrinsic stress accompanied with PECVD silicon nitride was utilized to induce a pre-strain into the silicon substrate during microfabrication. Both biaxial global and uniaxial transverse local strain was produced using the same stressing layer. A full study including design, fabrication, and calibration was

carried out to build a chip that can be used to quantify the strain effect.

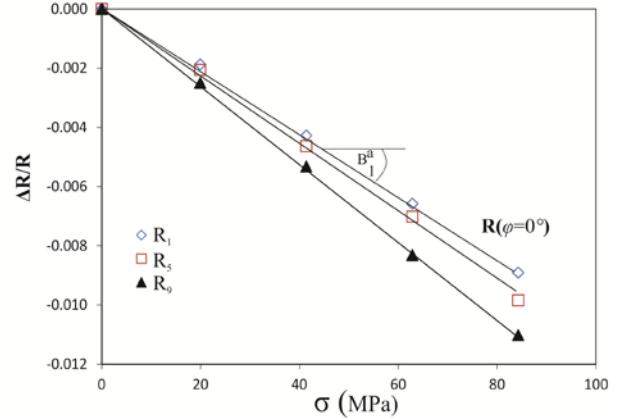


Figure 9. Typical 4PB results for R1, R5, and R9

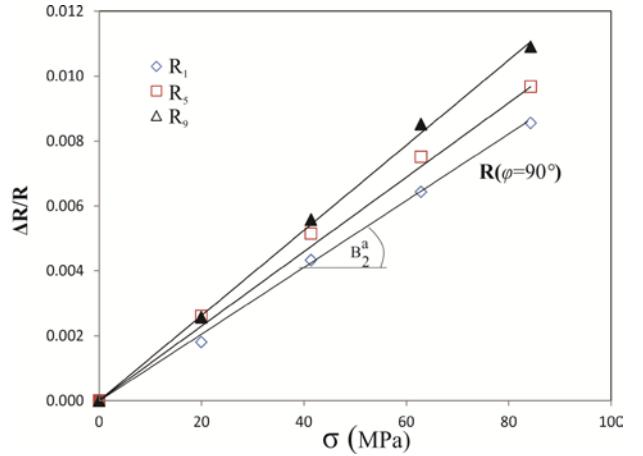


Figure 10. Typical 4PB results for R3, R7, and R10

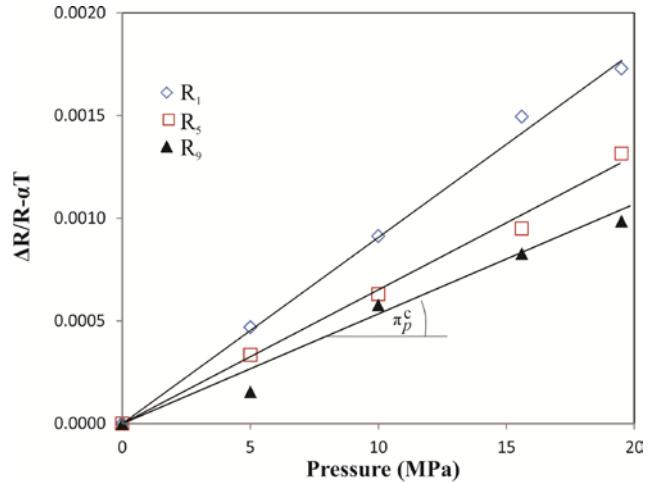


Figure 11. Adjusted hydrostatic calibration data

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