Modular Photovoltaic (PV) Step-up Converter With A Coupled Power Balancing Scheme for DC-Distributed Systems

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Abstract

The total global energy capacity for renewable energy systems has been increasing exponentially, with photovoltaic (PV) energy having a 25% growth rate in the past year along with a continual decrease in cost. A high-power PV energy conversion system typically consists of a medium voltage (MV) grid that collects power from individual PV arrays. In a MV Direct Current (DC) distributed grid architecture, since the output voltage of the PV array is significantly lower than the voltage level of medium voltage grid (such as tens of kV), a power electronic interface with sufficiently high voltage gain is required. To safely and effectively connect multiple PV energy sources to the MVDC grid, modular structure of PV power converter is used to convert and maximize the capture of PV energy. The converter also consists of external power balancing units to ensure equal power distribution and safe operation amongst all the converter modules. Developing highly power-efficient and cost-efficient power converter topologies and controllers with minimal number of components is the key to achieve a truly optimized PV energy power conversion system.

In this dissertation, a highly power-efficient modular PV power converter with high voltage gain and coupled power balancing stages is developed. To be specific, the first part of this dissertation focuses on the development of a novel current-sensor-less maximum power point tracking (MPPT) technique that functions with the use of a single voltage sensor for the devised high voltage gain PV converter module. In the second part of this dissertation, a new embedded PV power balancing scheme that utilizes high frequency (HF) interlinking active voltage quadruplers (AVQ) is proposed for the developed modular PV power architecture. The proposed design allows the devised MPPT stage in the PV converter to ensure optimal PV power extraction under all conditions while the interlinking AVQs distribute power equally across all modules to ensure safe operation. In the final part of this dissertation, a power efficiency optimization control scheme is proposed to allow the devised modular PV converter system to achieve high efficiency over a wide range of PV irradiation level. The operating principles and characteristics of the proposed topology and control principles are explained in detail in this dissertation. The feasibility and performance of the devised modular PV converter and control concepts are validated through simulation verification and hardware experimental verification on proof-of-concept prototypes.

Acknowledgement

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PWM Pulse Width Modulation	100
RMS Root Mean Squared	147
SAS Solar Array Simulator	80
SEPIC Single-ended Primary-inductance Converter	29
SiC Silicon Carbide	142
SMD Surface Mount Device	143
TMS Texas Instruments	81
VQ Voltage Quadrupler	42
ZE Zero	21
ZVS Zero Voltage Switching	7, 143

Chapter 1. Introduction

Due to the anticipation of fossil fuel shortages by the end of the century[1], there has been a trend towards the integration of renewable energy sources. This include technologies such as photovoltaic (PV), wind, hydro-power, bio-power, and geothermal [2]. Currently 30% of the world's energy is generated through renewable resources and it is predicted to reach 40% by 2040[3].

PV energy is one of the more promising renewable energy sources due to its simplicity and the advancement in its field. The growth rate of installed PV energy has been increasing year by year and in the past year had a 25% growth rate from 760GW to 942GW [4]. Figure 1-1 shows the growth rate of installed PV energy for the past ten years where yellow represent the total capacity at the start of the year and orange represents the additional capacity added during that year. It can be seen that the installed capacity increases year on year. PV energy provides several advantages such as quiet energy conversion, easy transportation due to light weight, simple installation, and a continuously decreasing cost. The cost of PV systems has also decreased by more than 50% in the past five years and is predicted to continue to decrease. This cost reduction has made PV systems an economically competitive investment in the long run [3].

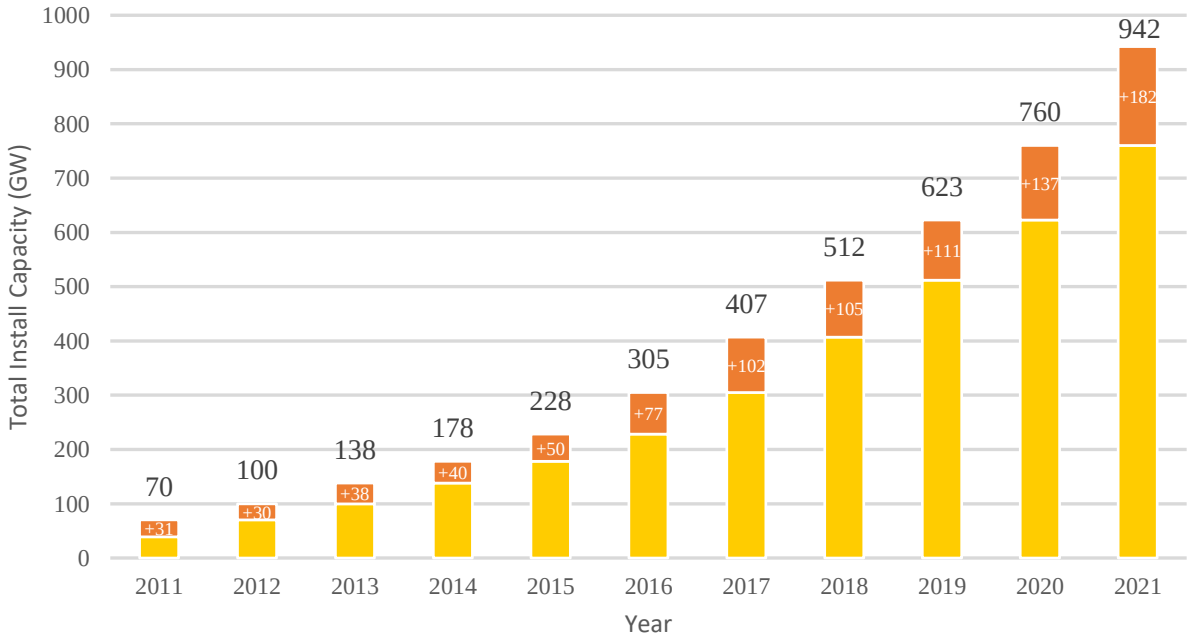


Figure 1-1: Global Growth rate of installed capacity of PV energy from 2011 to 2021 [4]

Canada is ranked 7th in production of renewable energy and 9th in production of PV energy in the world. In Canada, 18.9% of the energy generated in 2017 was from renewable resources, most of which was generated through hydro-power; however, the generated PV energy capacity has been on the rise. The installed capacity of PV power in Canada has increased from 16.7MW in 2005 to 3040MW in 2018. This value reached 3651MW in 2020 [5] and the total capacity is predicted to reach 4398MW by the end of 2023 [6], [7]. A similar trend is seen in Ontario, with PV install capacity increasing from 281MW in 2010 to 2670 in 2019 [8]. There are several PV farms scattered across Canada. As of 2022, the top three PV farms are the Travers Solar Farm [9] which utilizes 1.3 million PV panels and generates 465MW in Alberta, the Sol-Luce Kingston Solar PV Park and the Grand Renewable Energy Park in Ontario which both generates approximately 140MW[10].

1.1 PV Energy

PV panels can be manufactured from various components such as monocrystalline, polycrystalline, and thin-film PV cells. A PV module consists of a number of individual PV cells connected in series. Connecting PV modules in series forms a PV string and connecting a group of PV strings in parallel forms PV arrays as can be seen in Figure 1-2. These configurations as well as the type of PV cell used results in different Power-Voltage (P-V) and Current-Voltage (I-V) characteristics. These characteristics are non-linear and vary with the solar irradiation and temperature. Figure 1-3 shows an example of a 250W PV panel's P-V (blue) and I-V (red) curves.

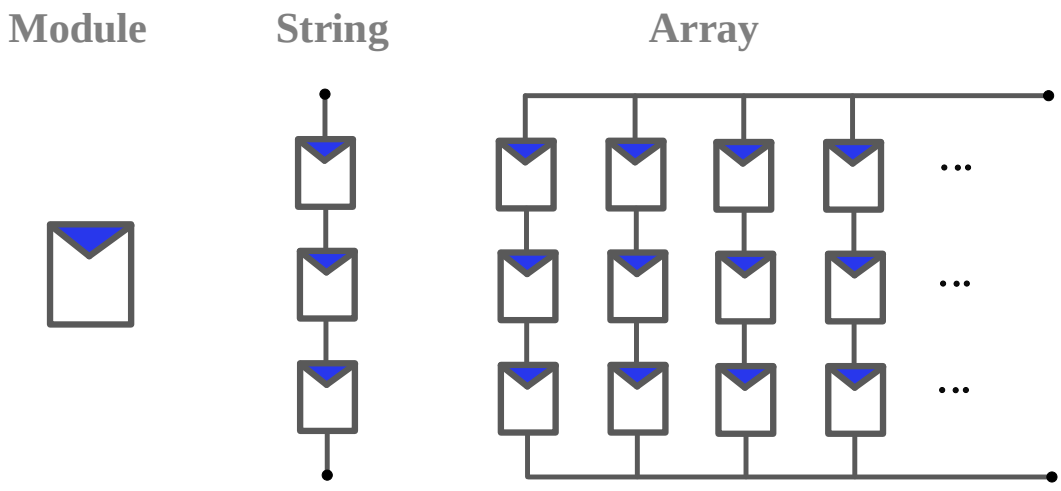


Figure 1-2: Example of a PV module, strings, and arrays

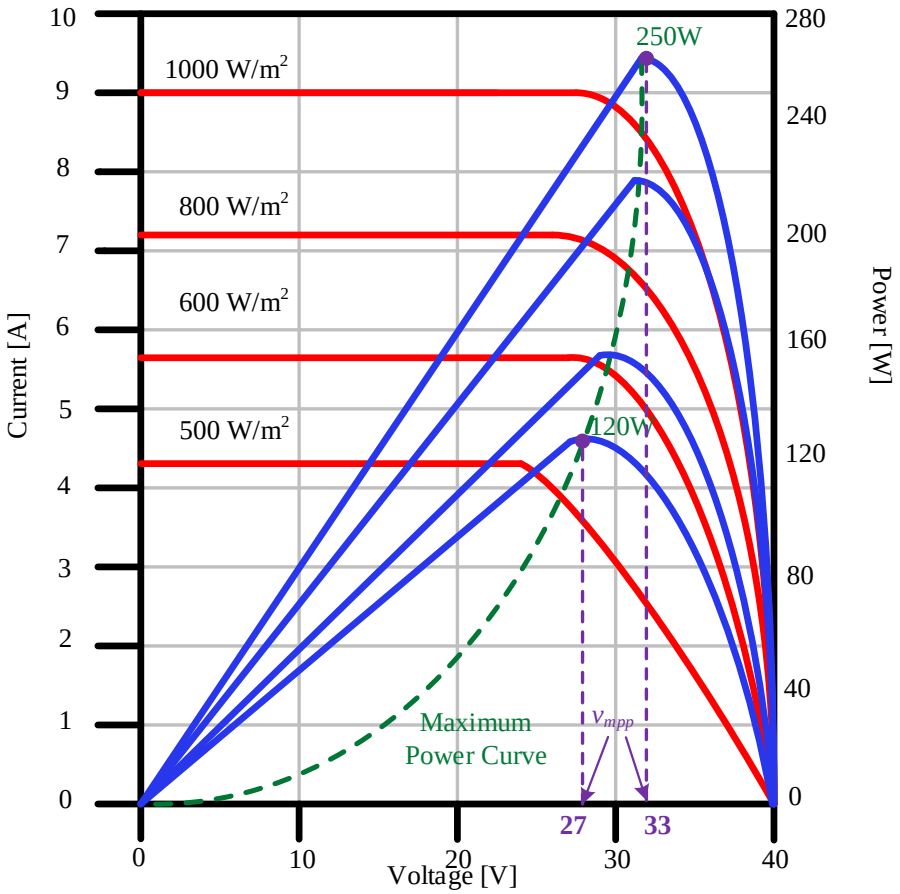


Figure 1-3: Example of a P-V and I-V curve for a 250W PV panel.

By multiplying the y-axis of the I-V curve with the x-axis, which is the operating voltage, the P-V curve is obtained. The peak of each P-V curve is known as the Maximum Power Point (MPP) and it can be seen that the operating voltage required to be at the peak of each curve is different. PV panels do not naturally operate at the peak of their P-V curve which implies that there is a need for controllers to adjust the system parameters such that the PV panel moves towards its maximum. These are known as maximum power extraction (MPE) or maximum power point tracking (MPPT) controllers.

Unfortunately, the extracted PV energy cannot be immediately used by the load or connected to a DC-grid and needs to be converted into useable electrical energy. This is due to the mismatch between PV panels and the load. The output voltage of a PV panel is low (30-40V) compared to what a load or MVDC-grid would require (from a few kV to hundreds of kV [11], [12], [13]). Further, maximum power extraction techniques cannot be directly applied to a PV panel or array

by itself. This implies the need for an additional stage, such as power electronic converters, to be placed between the PV panel and the output to step-up the panel voltage and to perform maximum power extraction.

1.2 Power Electronic Converters for MVDC Systems

Power electronic converters are a key component for integrating PV energy systems with DC grids or loads. These units typically consist of active components such as MOSFET switches and diodes as well as passive components such as capacitors, inductors, and transformers. Different configurations of these components allow for the assembly of circuits that carry out the required performance. An example of PV arrays connected to a power electronic converter is shown in Figure 1-4 along with a simple MPPT controller. The DC/DC power electronic converter converts captured PV energy into useable electrical energy as well as provides a step-up gain. The operating parameters of the PV array such as the voltage and current are sensed in order to allow the PV system to operate at their MPP.

Many power electronic converters have been designed to allow for high step-up voltage operation for MVDC applications. MPPT is typically implemented at the front-end of these converters. Different types of step-up DC-DC converters are discussed in this section as well as their merits, drawbacks, and types of power loss.

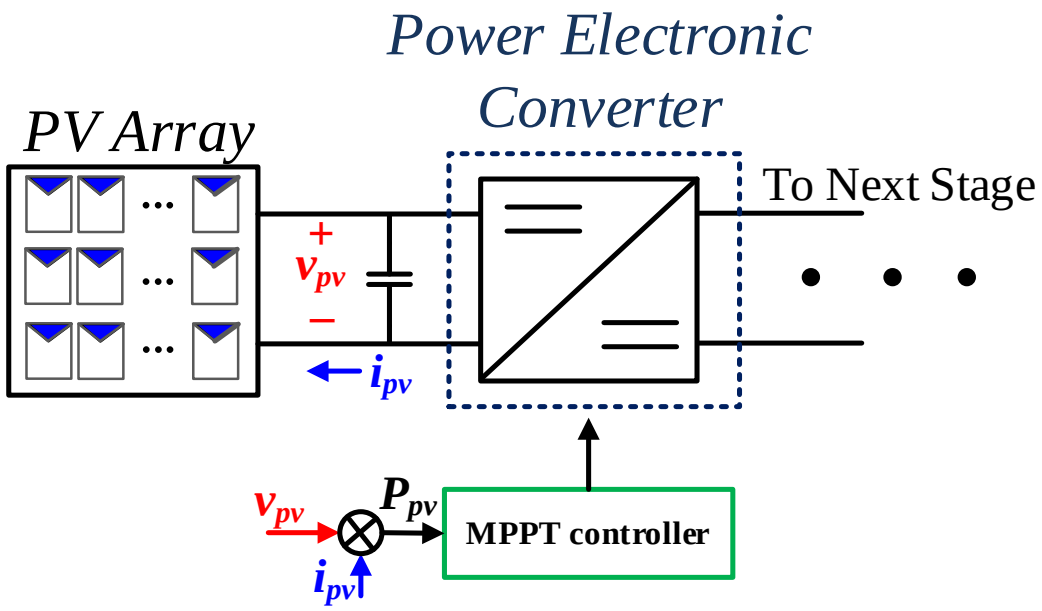


Figure 1-4: Example of a PV panel connected to a step-up DC-DC power electronic converter with a MPPT controller

1.2.1 Power Loss

Power electronic converters are required for their step-up capability, power conversion, for regulating the generated PV energy. Active and passive components used in these converters are not ideal and therefore are a source of power loss. The main power loss associated with power electronic converters are switching loss and conduction loss [14], [15].

1.2.1.1 Switching Loss

Converters typically utilize components such as MOSFET switches and diodes whose state varies between active (on) and inactive (off). Switching losses in these devices occur when there is an overlap in the voltage and current waveform during transition between switching states. This switching mechanism is also known as hard-switching which generates heat and can have negative impacts on both the component and the overall converter operation. Figure 1-5 shows a case of hard-switching where v_s is the switch voltage, i_s is the switch current, t_{fv} and t_{rv} are the fall and rise time of the switch voltage, and t_{ri} and t_{fi} are the rise and fall time of the switch current. The power loss equation for a single switch is provided in (1.1). It can be understood that the power loss is a function of the voltage and current during the overlap, the overlap time, and the switching frequency. One method to minimize hard-switching power loss is to decrease the switching frequency. However, the size of passive components such as inductors and capacitors are inversely

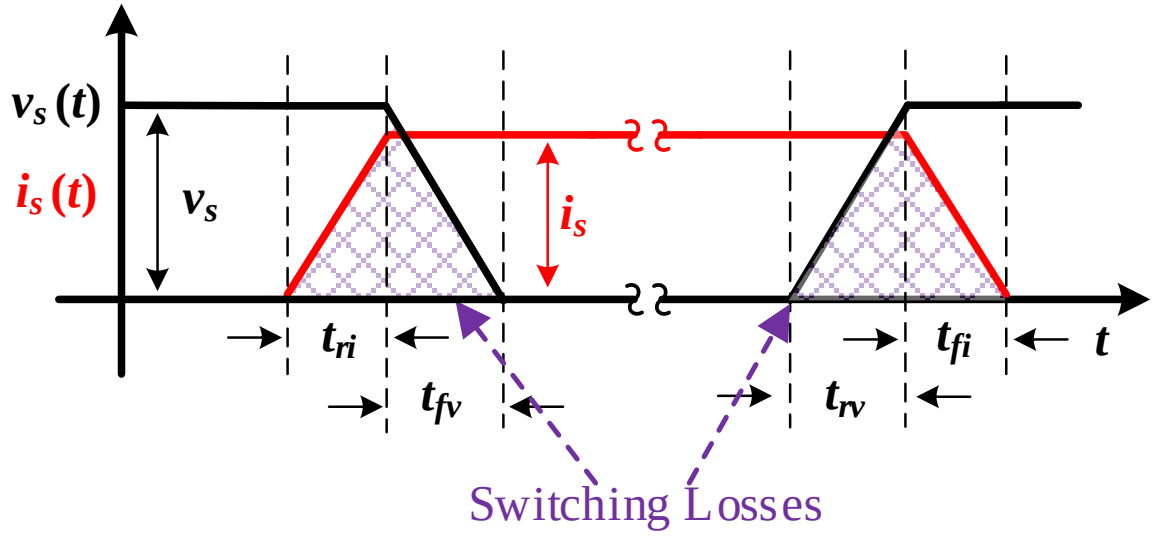


Figure 1-5: Example of a MOSFET's voltage and current waveforms during hard-switching

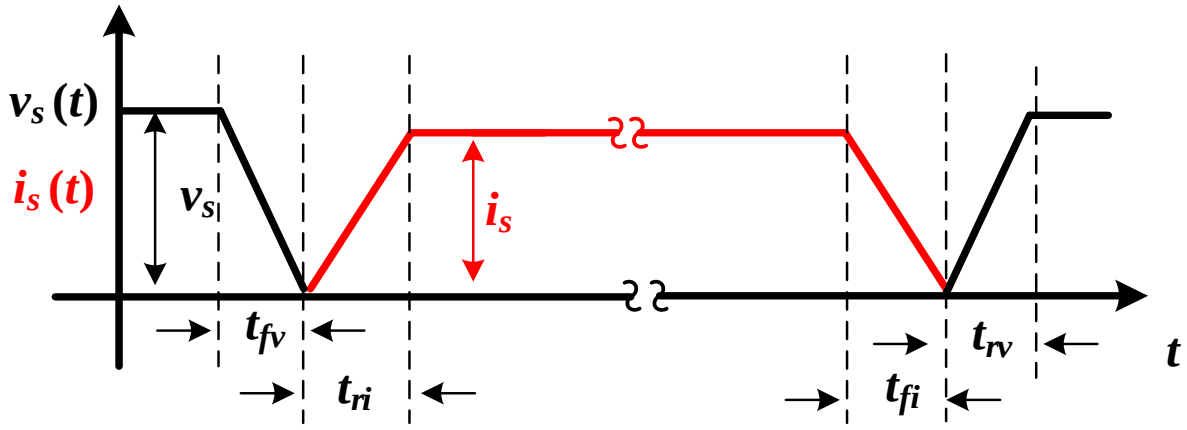


Figure 1-6: Example of a MOSFET's voltage and current waveforms during soft-switching

proportional to the switching frequency. This implies that lowering the switching frequency will increase the system size and decrease the power density, which is undesirable.

$$P_{sw\_loss} = 0.5 v_s(t) \times i_s(t) \times f_s \times \left(t_{fv} + t_{ri} + t_{fi} + t_{rv} \right) \tag{1.1}$$

To overcome the issues with hard-switching, converters are designed to operate under soft-switching condition as seen in Figure 1-6. This technique prevents overlap of the switch voltage and current waveform during transition periods result in what is known as zero voltage switching (ZVS) This can be achieved with additional external auxiliary circuits [30], or through the use of resonant circuits. Soft-switching not only improves the system efficiency, the operating frequency is restriction is removed. This allows for smaller passive components to be used and ensures the system achieves a smaller power density.

1.2.1.2 Conduction Loss

Conduction loss occurs in both active and passive components while they are conducting current. In practical implementations, passive components have parasitic resistive elements such as a capacitors equivalent series resistance (ESR) or the DC resistance (DCR) of an inductor. When current flows through these components, conduction loss occurs. For active components such as MOSFET switches, the conduction loss is a function of the RMS current and the on-resistance (1.2), while for diodes the conduction loss is a function of their average current and forward voltage drop (1.3).

$$P_{cond\_sw} = I_{s\_\mathrm{RMS}}{}^{2} \times R_{ds\_\mathrm{on}} \tag{1.2}$$

$$P_{cond\_d} = I_{D\_\mathrm{avg}} \times V_f \tag{1.3}$$

1.2.2 Resonant Converters

Due to their low losses and soft-switching capability, resonant converters are an attractive topology for use in MVDC systems. An example of a resonant converter configuration is provided in Figure 1-7. PV arrays connect to the input switch network which inverts the DC PV voltage into a square-wave or a rectangle-wave voltage whose frequency matches the switch network's frequency. From here, the newly generated AC voltage waveform is connected to the input terminals of the resonant tank. Resonant tanks consist of passive components such as capacitors, inductors, and in some cases transformers or coupled inductors to provided isolation. The tank is capable of increasing or decreasing the voltage level as well as provided additional benefits such as soft-switching to the switch network. The AC waveform generated at the output terminals of the resonant tank is then rectified back to DC through the use of a rectifier circuit and a low pass filter (LPF).

Several different types of resonant circuits [16] have be developed, which include two, three, and four-element based configurations. The *LCC*, *LLC*, and *CLL* are three of the most well-known three-element based topologies [16], [17], [18], [19].

An example of the *LCC* topology is shown in Figure 1-8(a). An inductor is placed at the input and in series with a capacitor and there is a second capacitor in parallel with the output. *LCC* can be considered a series-parallel circuit as it utilizes the benefits of both an *LC* series and *LC*

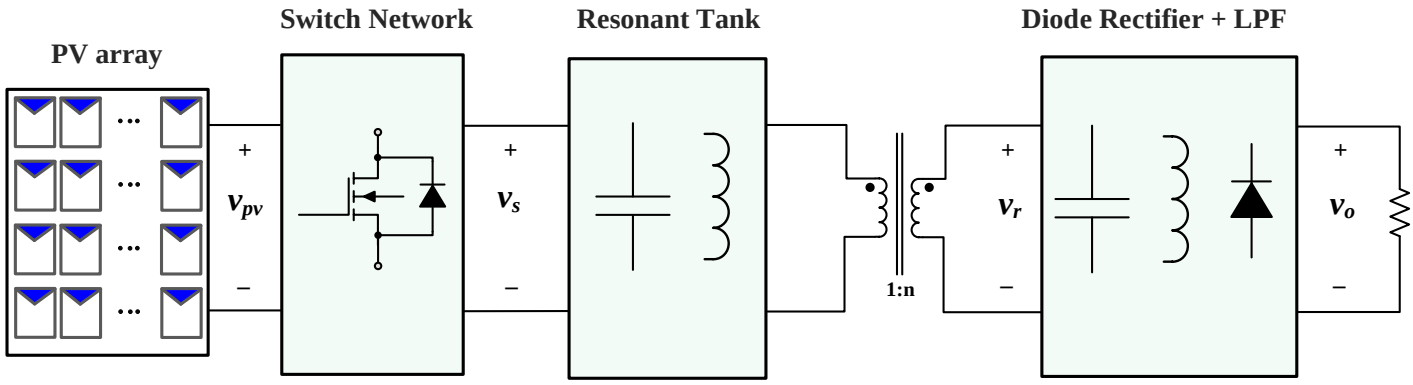


Figure 1-7: Resonant Converter Configuration

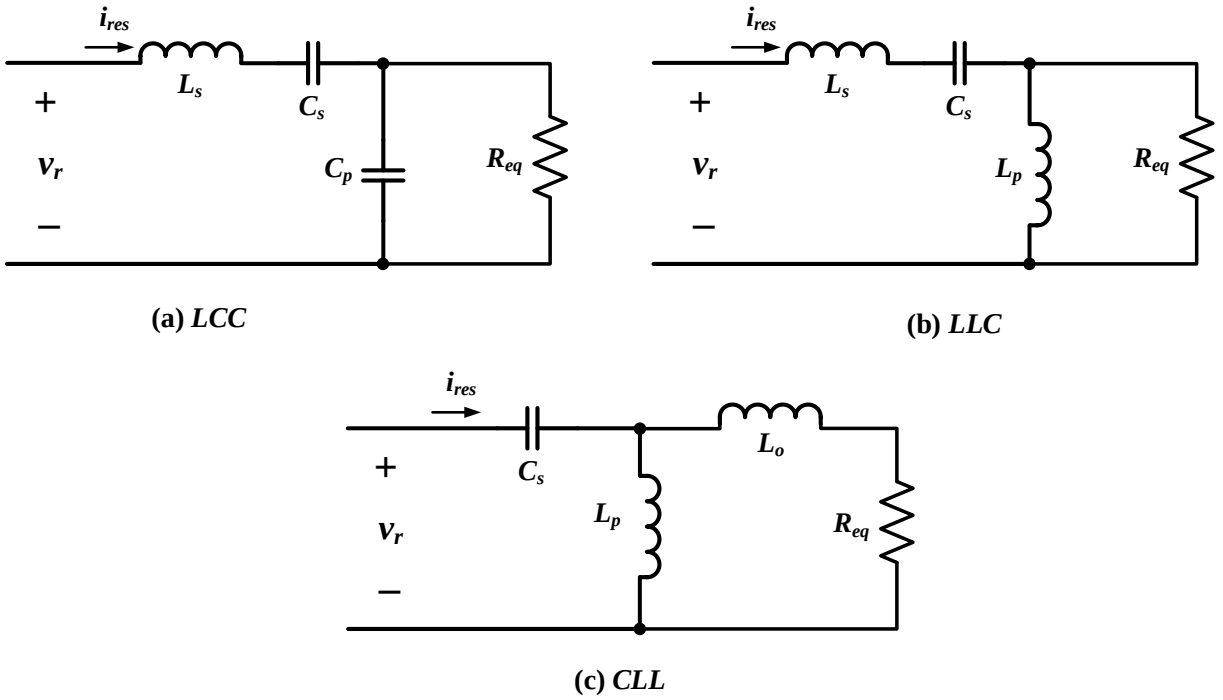


Figure 1-8: (a) equivalent circuit of *LCC*, (b) *LLC*, and (c) *CLL* resonant topologies

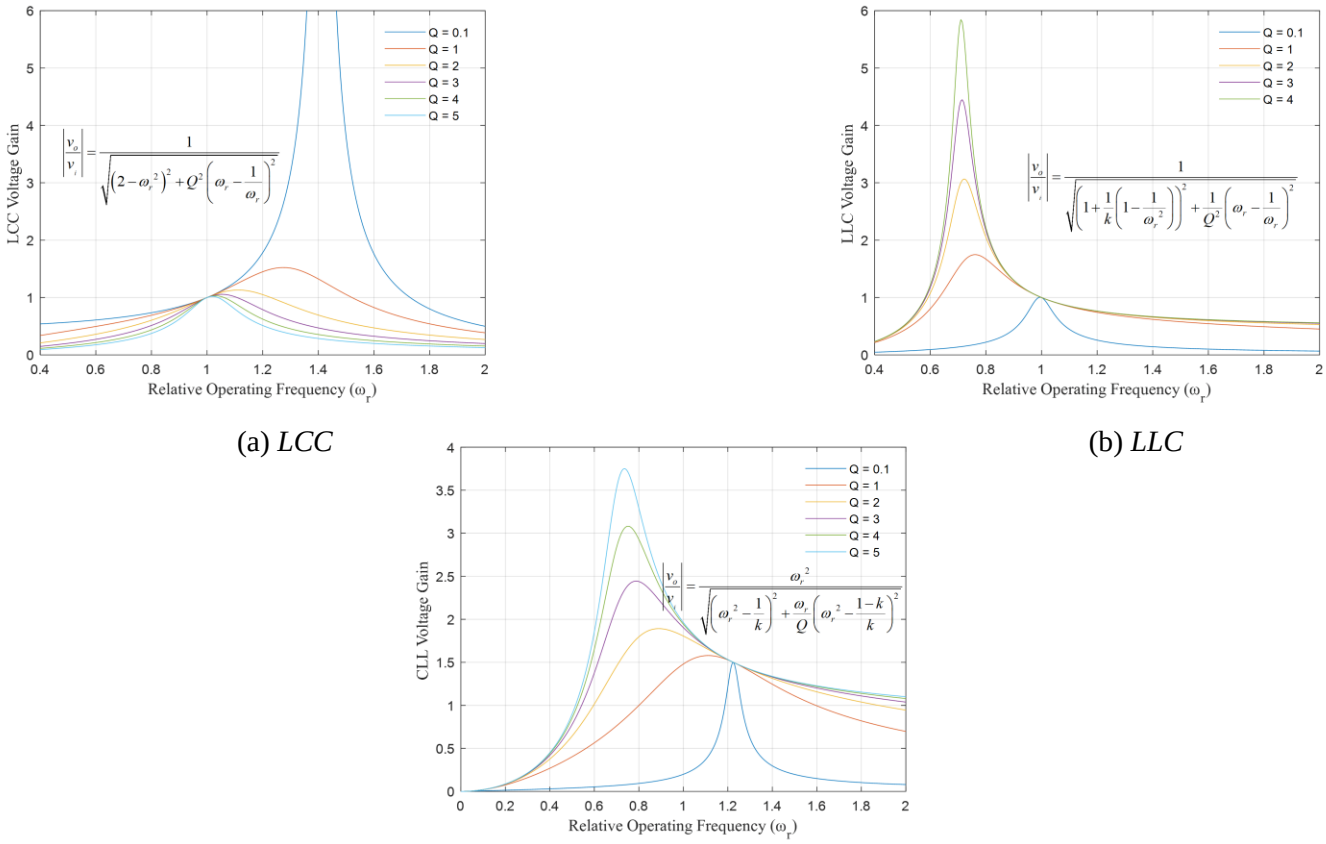
parallel resonant converter. The *LCC* topology has two resonant frequencies which are given in (1.4) and (1.5) respectively and where (1.6) is the equivalent resonant capacitance. The ratio between the resonant capacitors, (1.7), affect whether the topology operates as a series resonant or parallel resonant. *LCC* converters suffer from high circulating current which has a negative impact the circuit efficiency. These topologies also struggle to achieve soft-switching operation as well as have difficulty operating close to open circuit and short circuit conditions. The *LCC* gain equation is provided in (1.8) and shown in Figure 1-9(a) where *Q* is the quality factor as provided in (1.9).

$$\omega_{rs} = \frac{1}{\sqrt{L_s C_s}} \tag{1.4}$$

$$\omega_{rp} = \frac{1}{\sqrt{C_{eq} L_s}} \tag{1.5}$$

$$C_{eq} = \frac{C_s \times C_p}{C_s + C_p} \tag{1.6}$$

$$k_c = \frac{C_p}{C_s} \tag{1.7}$$



(a) *LCC* (b) *LLC*

(c) *CLL*

Figure 1-9 Voltage gain characteristics of three resonant converters: (a) *LCC*, (b) *LLC*, (C) *CLL*

$$\left|\frac{v_o}{v_i}\right| = \frac{1}{\sqrt{\left(2-\omega_r^{\,2}\right)^2 + Q^2\left(\omega_r - \frac{1}{\omega_r}\right)^2}} \tag{1.8}$$

$$Q = \frac{R_{eq}}{L\omega_o} \tag{1.9}$$

Recently, both *LLC* and *CLL* configurations having been gaining attention for high frequency applications as they are capable of maintaining desired operations such as soft-switching or high gain over a wide range [19]. An example of the *LLC* topology is shown in Figure 1-8(b). As in the case of the *LCC* configuration, an inductor is placed at the input and in series with a capacitor, however an inductor is used for the *LLC* parallel branch. This inductor can be replaced with a transformer to allow for isolation between the input and output. *LLC* configurations allow

for low circulating current and component stress and can build a current-driven rectifier network and achieve soft-switching. The gain of a *LLC* converter is provided in (1.10) and shown in Figure 1-9(b) where *Q* is the quality factor provided in (1.11) and *k* is the ratio between the parallel and series inductance provided in. (1.12)

$$\left|\frac{v_o}{v_i}\right| = \frac{1}{\sqrt{\left(1+\frac{1}{k}\left(1-\frac{1}{\omega_r{}^2}\right)\right)^2 + \frac{1}{Q^2}\left(\omega_r - \frac{1}{\omega_r}\right)^2}} \tag{1.10}$$

$$Q = \frac{R_{eq}}{L\omega_o} \tag{1.11}$$

$$k = \frac{L_p}{L_s} \tag{1.12}$$

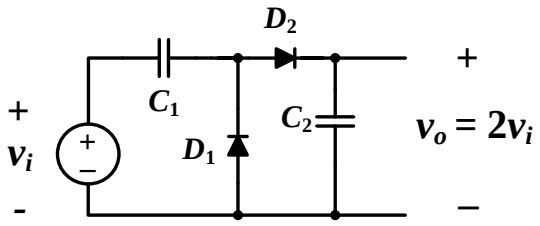
An example of the *LLC* topology is shown in Figure 1-8(c). The *CLL* topology utilizes a series capacitance which matches the *LCC* and *LLC* topologies. The main difference between *CLL* and *LLC* is that the series inductance is placed after the parallel inductor. If a transformer or coupled-inductor is utilized for the parallel branch, the series inductor would be on the secondary side. This allows *CLL* configurations to reducing the system size, volume, and cost by utilizing an isolating coupled inductor and placing the second inductor on the secondary side. However, the *CLL* configuration leads to an increased voltage and current stress across the resonant components. The gain of a *CLL* converter is provided in is provided in (1.13) and shown in Figure 1-9(c).

$$\left|\frac{v_o}{v_i}\right| = \frac{\omega_r{}^2}{\sqrt{\left(\omega_r{}^2 - \frac{1}{k}\right)^2 + \frac{\omega_r}{Q}\left(\omega_r{}^2 - \frac{1-k}{k}\right)^2}} \tag{1.13}$$

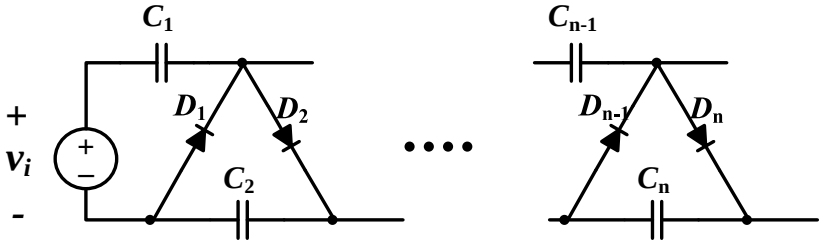
1.2.3 Voltage Multiplier

The output of the resonant tank is fed into a rectifier circuit to convert the AC output back to DC. Some works in literature utilize voltage multiplies for the resonant converter's rectifier stage [20]. Different component configurations result in different voltage multiplier topologies[21], [22], [23]. A few examples of voltage multipliers are provided in Figure 1-10. Figure 1-10(a) shows a Greinacher Voltage Doubler which is a well-known half-wave rectifier typically used at the output of transformer-based DC-DC converters. This topology rectifies the AC voltage and provides an additional step-up voltage gain of 2. The Cockcroft–Walton shown in Figure 1-10(b) is minor modification of the Greinacher Voltage Doubler topology. By cascading n topologies in series, the total voltage gain reaches 2n. The output voltage is directly across the capacitor C_2 in both topologies, which means for high voltage applications a high rated capacitor is required.

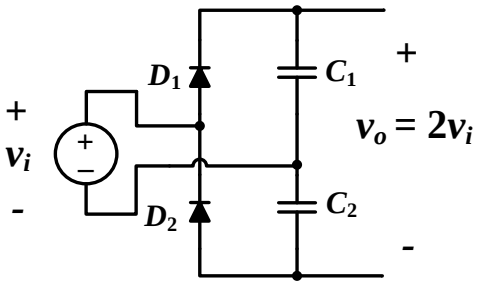
Figure 1-10(c) and (d) show two voltage multiplier topologies which utilize two capacitors at the output. Figure 1-10(c) is a voltage doubler, similar to that of Figure 1-10(a). In the case of Figure 1-10(c), when the input voltage is positive, diode D_1 is on and capacitor C_1 is charged to the positive of the input voltage and when the input voltage is negative, diode D_2 is on and capacitor C_2 is charged to the trough of the input. Consequently, the output voltage is double that of the input. Figure 1-10(d) is a voltage quadrupler whose output is four times the input voltage. An additional four components are needed to achieve this. The operation of this multiplier is similar to that of the voltage double as the switching of D_1 and D_2 charge C_1 and C_2 to the input. Diodes D_3 and D_4 then allow the capacitors C_3 and C_4 to be double that of C_1 and C_2, results in the total output voltage being four times the input. Figure 1-10(e) is a voltage multiplier consisting of the two capacitors and three diodes per stage [20]. By cascading additional stages, the voltage gain of this topology can be expanded, similar to that of Figure 1-10(b).



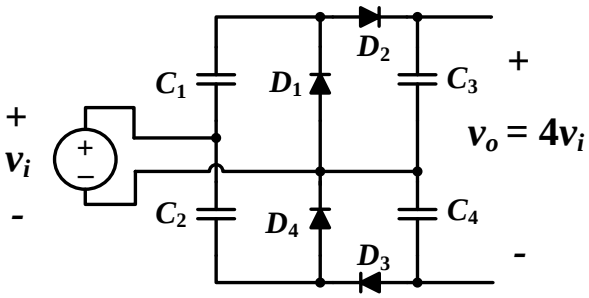
(a) Greinacher Voltage Doubler Rectifier



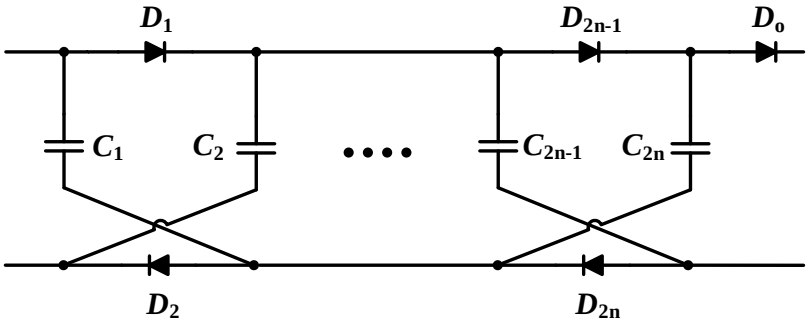
(b) Cockcroft_Wolton Voltage Doubler Rectifier



(c) Full-Wave Voltage Doubler Rectifier



(d) Full-Wave Voltage Quadrupler Rectifier



(e) Voltage Multiplier discussed in [19]

Figure 1-10: Example of voltage multipliers (a) Greinacher voltage doubler, (b) Crockcroft_Wolton voltage double, (c) full-wave voltage doubler, (d) voltage quadrupler, (e) scalable multiplier discussed in [19]

Table 1-1 Comparison of different voltage multipliers

Multiplier Rectifier Type	**# of Diodes**	**# of Capacitors**	**Voltage Gain**	**Diode Voltage Stress**	**Output Capacitor Voltage Stress**
Greinacher Voltage Doubler	2	2	2	v_o	v_o
Cockcroft_Wolton Voltage Doubler	$2n$	$2n$	$2n$	v_o	v_o
[19]	$2n$+1	$2n$+1	$2n$+1	v_o	v_o
Voltage Doubler	2	2	2	v_o	$v_o/2$
Voltage Quadrupler	4	4	4	$v_o/2$	$v_o/2$

Table 1-1 summarizes the component count and voltage stress for the rectifiers presented in Figure 1-10. The Greinacher and Cockcroft-Wolton rectifier both achieve the same step-up gain as the voltage doubler but operates with a higher output capacitor voltage stress. The rectifier discussed in [19] achievers a higher voltage gain but suffers from the same voltage stress issue. Out of the five rectifier types discussed in Table 1-1, the voltage quadrupler has the highest voltage gain however it requires additional diodes and capacitors.

1.3 Maximum Power Extraction

As discussed in section 1.1, PV panels do not naturally operate at their MPP and system operating conditions must be changed such that the PV panels operate at their MPP. This is achieved by regulating an operating parameter of a power electronic converter, such as their duty-ratio or frequency, which in turn adjusts the equivalent resistance of the system seen by the panel and changes the panel's operating voltage. Therefore, by tuning the operating parameter, one would be able to move the operating voltage to the MPP. However, as the light intensity from the sun or the atmospheric temperature varies, the operating condition of the PV panel and the location of the MPP is constantly changing.

Figure 1-11 shows a scenario with varying light intensity at a fixed temperature. In Figure 1-11(a), the system is operating at 25V which matches the required voltage necessary to operate at the MPP. As the light intensity increases, the short-circuit current (I_{sc}) increases which shifts the MPP to the right. This is seen in Figure 1-11(b) as Isc increases from approximately 4.5A to 9A and the new MPP occurs at 33V which is to the right of the previous point relative to the x-axis. Although there is a new MPP location (33V), the system continues to operate at the old MPP location (25V). In order for the system to operate at the new MPP, the equivalent resistance of the system must be changed through duty-ratio or frequency control. By doing so, the operating conation will slowly move towards the new MPP as shown in Figure 1-11(c).

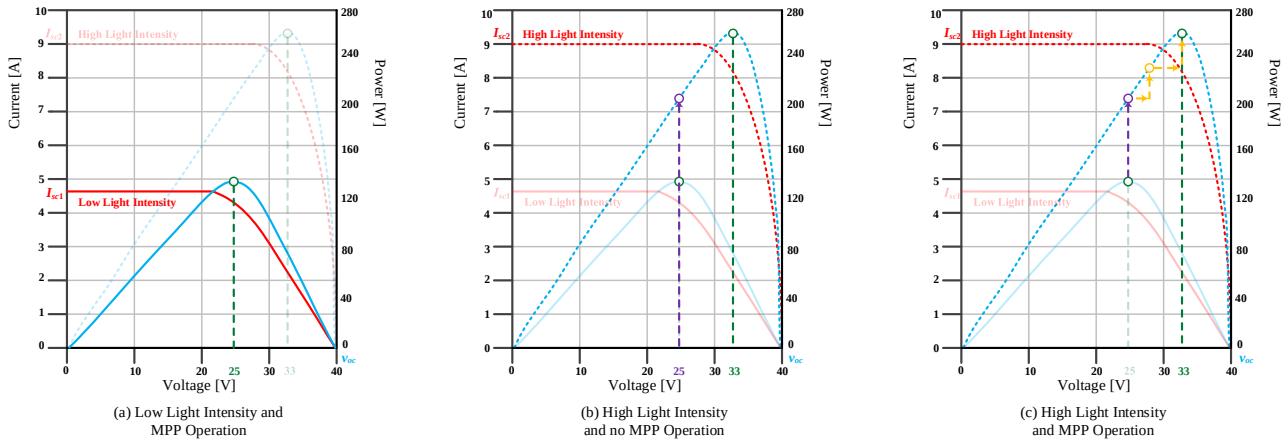


Figure 1-11: Panel P-V and I-V curves during (a) low light intensity and MPP operation (b) high light intensity and no MPP operation, (c) high light intensity and MPP operation

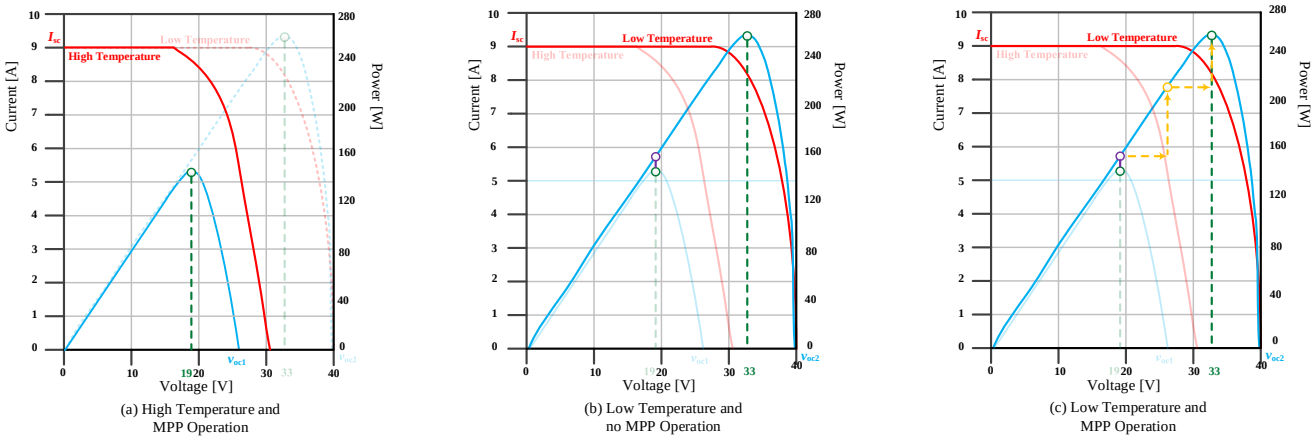


Figure 1-12: Panel P-V and I-V curves during (a) high temperature and MPP operation (b) low temperature and no MPP operation, (c) low temperature and MPP operation

Figure 1-12 shows a scenario with varying temperature at a fixed light intensity. Unlike varying light intensity, I_{sc} does not change. Instead, the open circuit voltage (v_{oc}) varies with the temperature. As the temperature increases the new MPP moves to the left. To keep consistency with Figure 1-11, the scenarios shown in Figure 1-12 are from high to low temperature. Figure 1-12(a) shows the system operating at a high temperature while at the MPP. From here the temperature decreases demonstrated in Figure 1-12(b). This results in an increase in the system's v_{oc} while the I_{sc} stays constant. The operating voltage of the PV array stays at the previous value until the system changes the operating converter parameters such that the can move towards the new MPP as seen in Figure 1-12(c).

In practical scenarios, the rate at which the operating atmospheric conditions changes is far greater than the speed at which one can manually change converters control parameter. To overcome this issue, controllers known as maximum power point trackers have been developed to automatically regulate the converter's operating parameter such that the maximal amount of PV power is extracted at all times. This section will discuss several different implementation of maximum power point trackers in literature including classic techniques, intelligent trackers and current-sensorless based trackers.

1.3.1 Classic MPPT Algorithms

The classic method to perform MPPT is to directly obtain the operating parameters of the PV panel which are the voltage and current. These parameters can be multiplied together to obtain the operating power of the panel which can be used to estimate the systems location of the I-V and P-V curve.

1.3.1.1 Perturb and Observe (P&O)

One of the two basic MPPT algorithm is Perturb and Observe (P&O) which is also known as hill-climbing. The P&O algorithm implements a small fixed perturbation in the control variable which causes an increase or decrease in the PV voltage. Based on Figure 1-13, it can be understood that this will change the x-axis location on the P-V curve which in turn will result in an increase or decrease in the operating power. Table 1-2 displays four possible scenarios that can occur as a result of this perturbation. Consequently, the controller can determine how the control variable should be varied in order to move the system state towards the MPP.

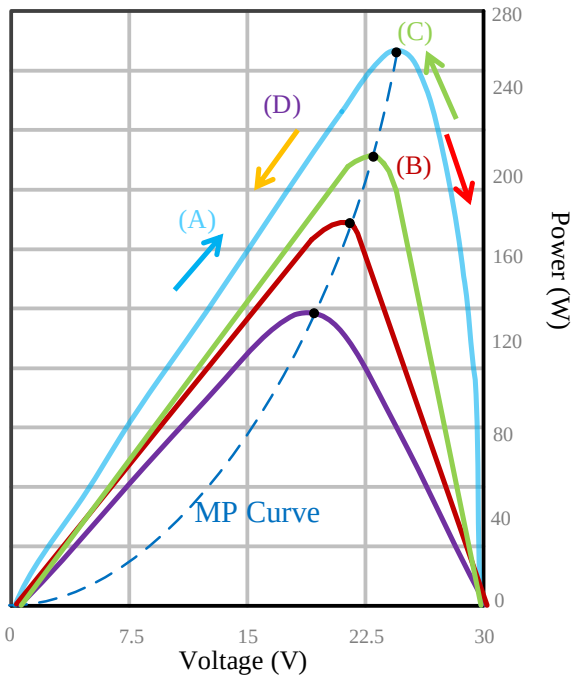


Figure 1-13: An example of four possible scenarios for P&O during operation for a 250W PV panel

Table 1-2 Four possible P&O scenarios

Initial Perturbation	Change in Power	Scenario	Next Perturbation
Positive	Positive	(A)	Positive
Positive	Negative	(B)	Negative
Negative	Positive	(C)	Negative
Negative	Negative	(D)	Positive

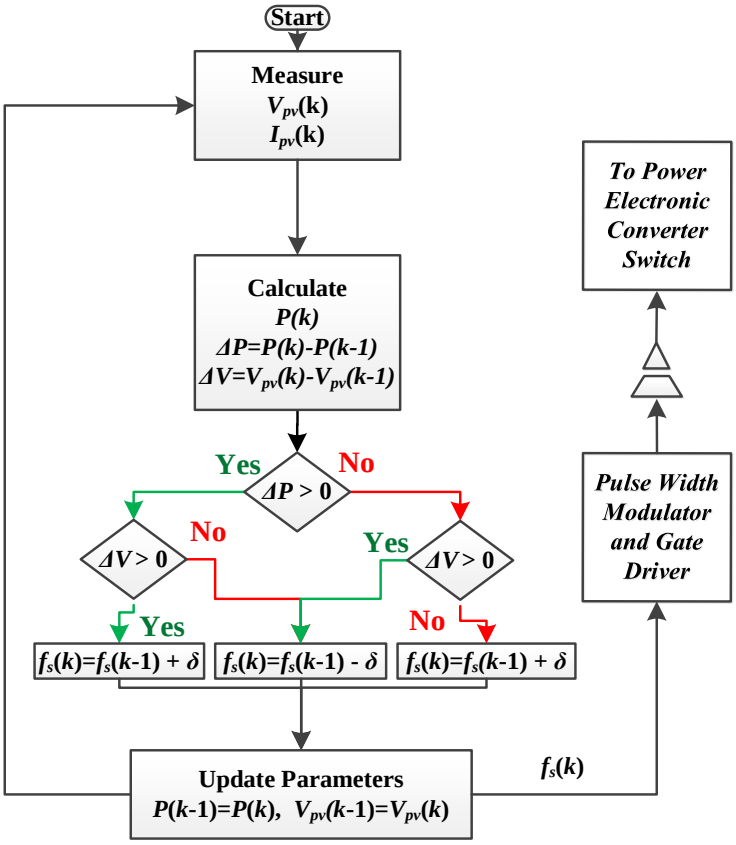


Figure 1-14: Example of a simple frequency-based P&O algorithm.

If the previous perturbation resulted in an increase in the operating power, the system will continue to move in that direction to further increase the operation power. This situation is shown in scenario (A) and (C) in Table 1-2. If the previous perturbation resulted in a decrease in the operating power, it implies the system overshot the MPP and that the direction of perturbation must be reversed. This situation is shown in scenario (B) and (D) in Table 1-2. The main advantage of P&O is in its simplicity as this method does not require complex mathematical functions to determine whether the system is at the MPP. A P&O algorithm can be developed with simple if-

else comparison statements such as the flowchart shown in Figure 1-14. However, this simplicity also results in the system oscillating around the MPP. By utilizing P&O, the system will never operate at the MPP. This technique still results in a high (>90%) extraction efficiency [24], [25], [26], [27], [28], [29], [30], [31], [32].

1.3.1.2 Incremental Conductance (INC)

Another commonly used MPPT technique is known as incremental conductance (INC) [24], [25], [26], [27], [28], [29], [30], [31], [32]. Unlike P&O, this method relies on the panel's rate of change of current as a function of the rate of change of the input voltage (1.14). If the system is at the MPP, it implies that the rate of change of the power as a function of PV voltage is zero meaning the left-hand-side of (1.14) is zero. Based on this condition, there are three possible scenarios for which the system could be operating at. These scenarios are provided in equations (1.15), (1.16), and (1.17) respectively.

$$\frac{dP}{dv} = \frac{d(iv)}{dv} = i + v\frac{di}{dv} \tag{1.14}$$

$$\frac{di}{dv} > -\frac{i}{v} \text{ to the left of the MPP} \tag{1.15}$$

$$\frac{di}{dv} < -\frac{i}{v} \text{ to the right of the MPP} \tag{1.16}$$

$$\frac{di}{dv} = -\frac{i}{v} \text{ At the MPP} \tag{1.17}$$

If the rate of change of the input current as a function of the rate of change of the input voltage is greater than the negative of the input current divided by the input voltage then the system is operating to the left of the MPP. The controller then changes the control variable such that the system operates closer to the MPP. If instead the value is less than the negative of the input current divided by the input voltage then the system is operating to the right of the MPP. If the values are equal then the system is operating at the MPP.

Based on (1.17), it can be understood that incremental conductance is able to determine if the system is at the MPP which is an advantage when compared to P&O. However, INC requires more complex mathematical equations compared to P&O which slows down its tracking speed

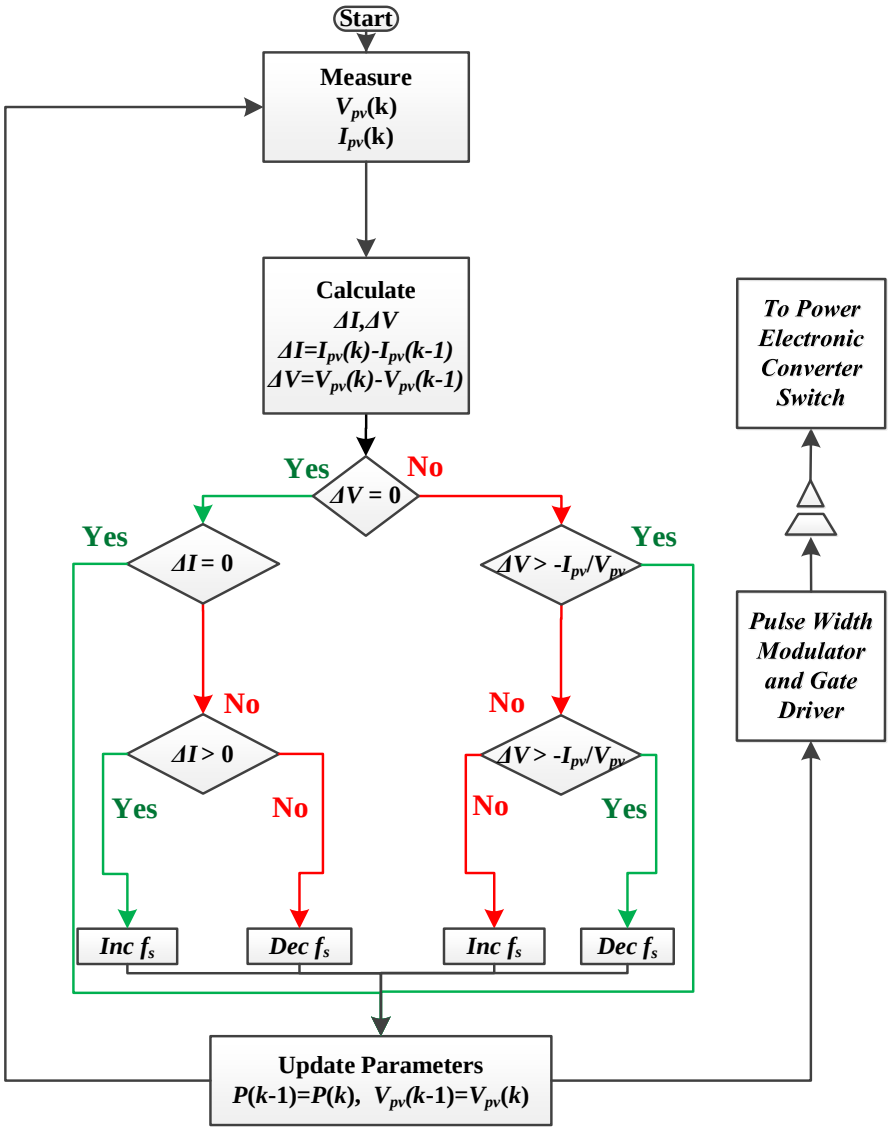


Figure 1-15: Example of a simple frequency-based INC algorithm.

and in turn faces difficulties operating under rapidly changing atmospheric conditions. An example of a simple INC implementation is given in Figure 1-15.

1.3.1.3 Curve Fitting

The P-V curve shown in Figure 1-3 can be approximated as a third-order polynomial function as given by (1.18) which allows for the required voltage needed to operate at the MPP to be calculated. The coefficients a_0, a_1, a_2 and a_3 are unique to each PV panel and need to be obtained by sampling the input voltage and power. However it should be noted that this technique does not

require the parameter a_3 as it goes unused in the first derivative as shown in (1.19). Once parameters a_0, a_1, and a_2 are obtained the voltage required to operate at the MPP can be determined by(1.20). As this method approximates the P-V curve, the obtained v_{mpp} is also an approximation which implies the system will usually operate close to but not at the MPP. The sampling requirement also affects the operation speed, which can lead to issues under rapidly changing MPP conditions [33].

$$P = a_0 v^3 + a_1 v^2 + a_2 v + a_3 \tag{1.18}$$

$$\frac{dP}{dv} = 3a_0 v^2 + 2a_1 v + a_2 \tag{1.19}$$

$$v_{mpp} = \frac{-a_1 \pm \sqrt{a_1^{\,2} - 4a_0 a_2}}{2a_0} \tag{1.20}$$

1.3.2 Intelligent MPPT Algorithms

Classic MPPT algorithms are capable of achieving high extraction efficiency however they suffer from drawbacks including inability to track under fast changing atmospheric conditions and costly control circuits [32]. There are several advanced tracking algorithms in literature to overcome the drawbacks of classic MPPT algorithms [38]–[59] and they will be discussed in this section.

1.3.2.1 Fuzzy Logic

In the case of P&O and incremental conductance, the controller regulates the control variable based on simple comparisons. Fuzzy logic control (FLC) [34], [35], [36], [37] is a control-based approach that has been gaining popularity in the last decade due to its ability to handle imprecise inputs without a mathematical model. FLC operates using degrees of truth, such as partially true or partially false. The algorithm consists of three stages: fuzzification, inference, and defuzzification. In the fuzzification stage the controller converts the input parameters to fuzzy linguistic variables that are used by the controller. From here the variables are mapped to a lookup table such as the one shown in Table 1-3 [36]. There are five different fuzzy levels which are negative big (NB), negative small (NS), zero (ZE), positive small (PS), and positive big (PB). The more levels a fuzzy logic controller uses the more accurate its performance is, however additional levels increase the difficulty of implementation. One such example is [46] which utilizes a 49

Table 1-3 Example of a twenty-five fuzzy rule table

Linguistic Variable	***NB***	***NS***	***ZE***	***PS***	***PB***
NB	PB	PB	PS	PB	PB
NS	PB	PS	PS	PS	PB
ZE	NS	NS	ZE	PS	PS
PS	NB	NS	NS	NS	NB
PB	NB	NB	NS	NB	NB

fuzzy rule table. Once the variables have been mapped using the lookup table the controller then converts the results from a linguistic variable back to an output variable and uses this result to vary the control variable. The inputs to a FLC-based controller are typically the error and the change in error while the output is the control variable such as the duty-ratio or frequency. FLC's are capable of having quick convergence to the MPP with little oscillations compared to P&O, however knowledge of the PV array parameters is typically used to determine the fuzzy rule table and levels.

1.3.2.2 Artificial Neural Network (ANN)

In order to improve the response time and efficiency of conventional MPP algorithms artificial neural network (ANN) based techniques have been implemented in literature. ANN MPP algorithms treat the PV system as a black box which means they do not require information about the specific converter or load conditions to function. These algorithms typically require the panel's operating current and voltage however more complex versions also require the atmospheric irradiance and temperature. The output of these algorithm is the operating duty-ratio or frequency required for the system to operate at the MPP. ANN algorithms are trained beforehand such that during operation they can easily and efficiently calculate the required operating condition [34]. An example of an ANN system is shown in Figure 1-16. For MPP based algorithms the inputs are typically atmospheric conditions such as temperature or irradiance along with the PV panel operating conditions including the voltage and current. These measurements are sent into the hidden layers to be multiplied by weights and then summed up to obtain the required output.

[38] presented an ANN based algorithm to help reduce the oscillations around the MPP that arise from using P&O. A feed-forward algorithm utilizing 2400 samples, 5 hidden layers, and

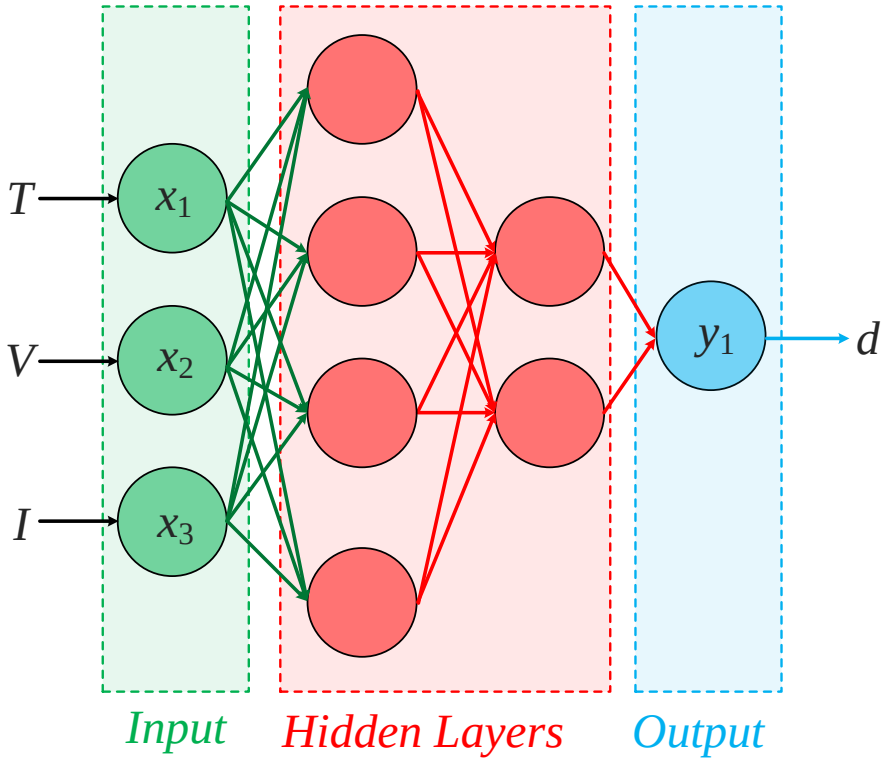


Figure 1-16 Example of an ANN with two hidden layers utilizing temperature (*T*), voltage (*V*), and current (*I*) to determine the required duty-ratio (*d*)

100 epochs were utilized to obtain the required duty-ratio to operate at the MPP. The weights were trained using the Levenberg-Marquardt algorithm which is a least squares method that utilizes a damping factor [39]. The authors compared their ANN based algorithm to the basic P&O and INC algorithms when applied to a boost converter operating at 130W in simulation. It was found that their proposed algorithm took 30ms to reach the MPP and operated with minimal oscillations during steady state whereas both P&O and INC took double the time (60ms) as well as exhibited oscillations around the MPP.

[40] utilized a hill-climbing adaptive neuro-fuzzy inference system (ANFIS) technique. This method used temperature and irradiance sensors to obtain the atmospheric conditions which was sent through their ANFIS to estimate the required operating duty-ratio. From here this estimate is utilized along with the panels operating voltage and current with a hill-climbing algorithm to refine the estimated duty-ratio. This method resulted in a high tracking efficiency of over 99% and the two stage (hill-climbing and neuro-fuzzy) allowed the system to correctly operate under partial shading condition. However, it was noted in [34] that although the final implementing was not

complex, this method required a complex membership function design which contributed to a high cost.

One benefit of ANN based MPP tracker is that they do not require detailed information of the converter system or mathematical models. However, to design more accurate models, multiple hidden layers are required, which increases the implementation cost [28]. Also, it is difficult to implement ANN based MPP techniques in low-cost hardware processors due to the large amount of data storage and extensive real-time computations.

1.3.2.3 Steepest-Descent/Gradient Ascent

Steepest descent, also known as gradient descent, is a first-order algorithm for locating a local minimum whereas gradient ascent is used to locating a local maximum. The term gradient refers to the rate of change of a function. They are both iterative optimization algorithm and proceeds by successive improvements to the control variable. In the case of MPPT, the variable for which we are trying to optimize is the input power while the control variable is the PV panel voltage, and based on the P-V curve provided in Figure 1-11, the optimum location is the maximum, hence gradient ascent is a viable option. The P&O MPP algorithm utilizes a fixed incremental step-size to vary the control parameter. By integrating gradient ascent with P&O, it is possible to track the MPP with a variable step-size that changes based on the gradient [25], [30], [41], [42], [43], [44], [45]. For a PV energy system, to change the input voltage, a parameter of the power electronic converter such as the duty-ratio or frequency is used. (1.21) shows an example of gradient ascent iterative duty-ratio step-size change. As a rule, in a gradient ascent algorithm, the controller output (d_{n+1}) is updated based on the previous iteration's output (d_n) and the gradient of the control variable ($\nabla P(d)$) multiplied by a constant parameter (α). The term $\alpha \nabla P(d)$ is added to the duty-ratio as we are attempting to maximize the operating power.

$$d_{n+1} = d_n + \alpha \nabla P(d) \tag{1.21}$$

1.3.3 Current-Sensorless Based Algorithms

The MPP tracking techniques discussed in section 1.3.1 and 1.3.2 utilize voltage, current, or other sensors to determine the operating characteristics of the PV panel. For example, P&O uses voltage and current measurements to calculate the operating PV power while INC uses the same parameters to determine the rate of change. The implementation of a voltage sensor is fairly simple

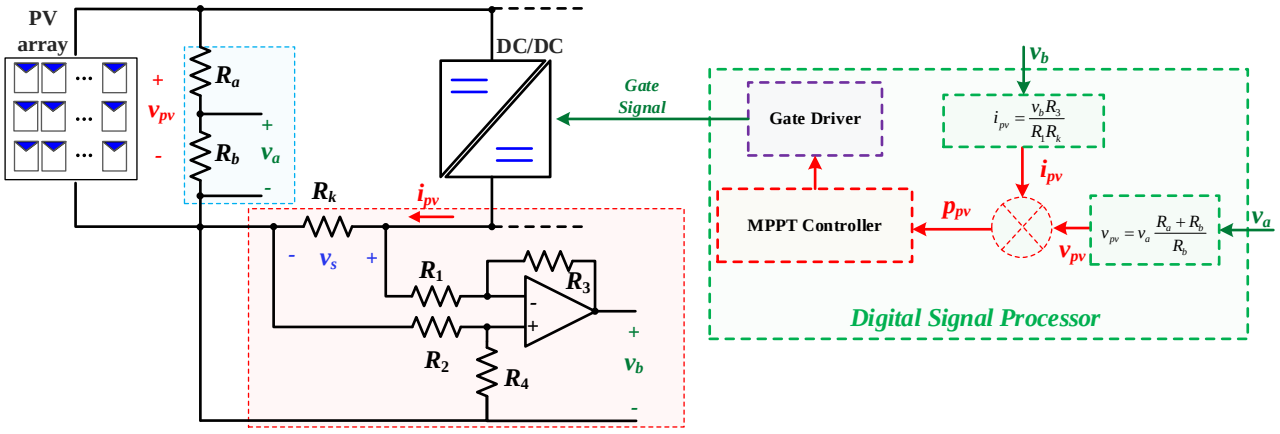


Figure 1-17 Example of a voltage (blue box) and current (red box) sensor implementation as well as a controller (green box)

compared to a current sensor. A resistive bridge can be placed in parallel with the point of measurement such that the voltage can be safely scaled down and sent to a controller. An example of a voltage sensor implementation is shown in Figure 1-17 where two resistors R_a and R_b are used to scale down the PV voltage, v_{pv}, to a lower value, v_a (1.22), which is then safely sent to a controller. From here, the controller can use the sensed voltage and resistor values to obtain v_{pv} (1.23).

$$v_a = v_{pv} \frac{R_b}{R_a + R_b} \tag{1.22}$$

$$v_{pv} = v_a \frac{R_a + R_b}{R_b} \tag{1.23}$$

There a multiple way to perform sense current such as with a Kelvin resistor or a hall-effect sensor, however all methods are more complex compared to voltage sensing. An example of current sensing using a Kelvin resistor is shown in Figure 1-17 where a sense resistor, R_k, is placed in the path of the output current of the PV array, i_{pv}, which generates a voltage drop, v_s. A small R_k is used to minimize the sensors impact on the system efficiency however this leads to a small v_s and as a result an amplification stage is required in order for the signal to be utilized by the controller. The addition of these components reduces the systems robustness, decreases the overall accuracy, and drives up the cost of the overall system [46]. Hall effect sensors have less of an impact on the system efficiency however their cost is much greater than a Kelvin resistor while still requiring an additional amplification stage.

PV based MVDC system typically use multiple modules with individual MPPT controllers. This implies that for an ‘M’ module system, ‘M’ voltage and ‘M’ current sensors are required, which can drive up the system cost. To overcome the challenges associated with current sensing, there have been numerous current-sensorless MPPT algorithms discussed in literature which this section will cover.

1.3.3.1 Alternative Sensor

One method tested in literature to remove the need of current sensors is through the use of alternative sensors. The operating power of a PV panel varies with the light intensity and the operating temperature, which is why [38] utilizes irradiance and temperature sensors to track the MPP. The algorithm utilizes these measurements with a feed-forward neural network to train weights. These weights along with the panel voltage measurement will return the exact operating location on the P-V curve. From here the neural network algorithm calculates the exact duty-ratio required to operate at the MPP. [47] utilized a two-stage adaptive neuro-fuzzy inference system (ANFIS) based on temperature, irradiance and voltage sensors. The first stage would employ temperature and irradiance measurements to derive the required panel voltage to operate at the MPP, similar to [38]. From here, the second stage would use the actual operating voltage of the panel along with the first stage output to determine the duty ratio, (d), required to push the operating voltage to the MPP voltage. To train this network, 200 sets of temperature and solar irradiance data were utilized along with 30,000 epochs with a target error of 1.1%. Both these methods calculate the required MPP instead of arriving at it through perturbation or comparisons, which imply they work well under rapidly changing intensity conditions. Although they provide fast MPP tracking without the need of a current sensor, the PV panel characteristics are required in the first stage, which implies these method’s application are limited as the algorithm would also need to be updated for different PV panels. As temperature and solar intensity sensors are required, the resulting overall cost could end up higher than using a current sensor.

1.3.3.2 Converter Parameter Based

Other MPPT methods attempt to estimate the PV panel’s operating current by using known converter parameters. In [48], [49] two voltage sensors, known converter parameter values, and the load resistance are used to estimate the average input current of a flyback converter with a PV panel connected to the input as shown in Figure 1-18. Once the average input current is known,

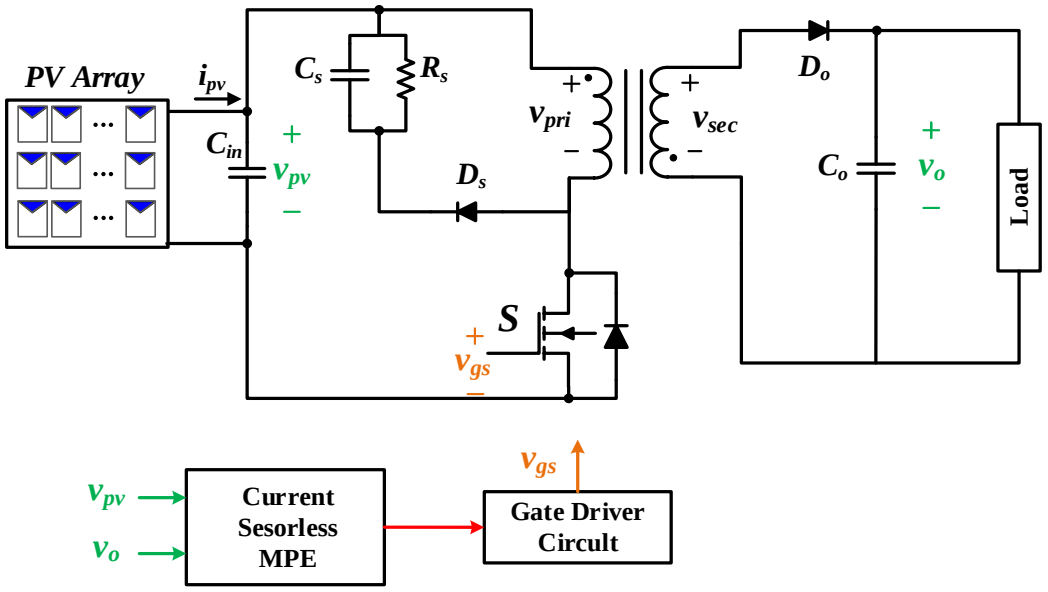


Figure 1-18 Current-sensorless MPPT with a Flyback converter and two voltage sensors [54]

this value is used together with the measured PV voltage to implement a P&O based MPE algorithm. (1.24) shows the estimated PV current equation used in [48] where C_{in} is the input capacitance, v_{pv} is the input voltage, C_o is the output capacitance, v_o is the output voltage, R is the load resistance, and n is the flyback converter turns-ratio. This technique does remove the need for a current sensor however the controller is specifically for this circuit which limits the range of applications. This circuit also requires the use of an additional snubber circuit in order to achieve soft-switching operation on the converter's switch which increases the component count.

$$i_{pv}(t) = n\left(C_o \frac{dv_o(t)}{dt} + \frac{v_o(t)}{R}\right) + C_{in}\frac{dv_{pv}(t)}{dt} \tag{1.24}$$

1.3.3.3 Single-Sensor

Reference [50] utilizes a similar technique to [51] but with a single voltage sensor. Their proposed algorithm aims to maximize the tracking efficiency equation derived from a specially designed quasi double-boost converter as given by (1.25). The operating panel current is estimated by utilizing the duty-ratio (d) and operating period (T_s) of the converters two switches as well as the input capacitance (C_{in}) and the PV panel voltage ripple (Δv_{in}).

$$i_{pv}(t) = \frac{(1+d)\times C_{in}\times \Delta v_{in}}{d(1-d)\times T_s} \tag{1.25}$$

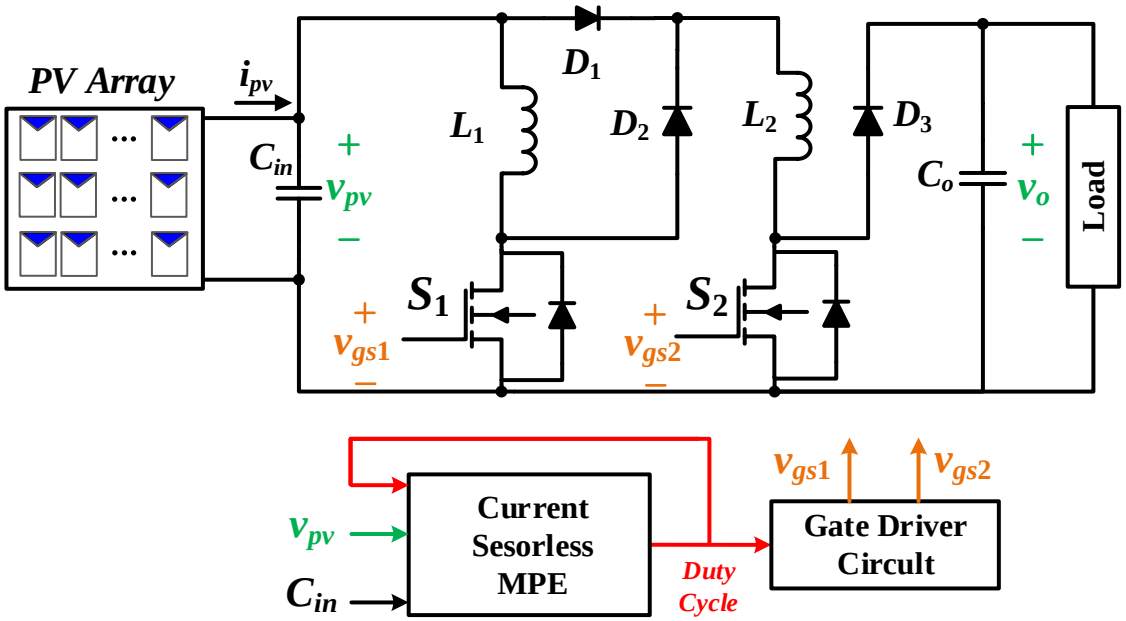


Figure 1-19 Current-sensorless MPPT with a double-boost converter [56]

Although this approach removes the need for a current sensor, it is specifically designed for a double-boost converter as shown in Figure 1-19, which limits its application. To apply this method to another converter, (1.25) would need to be recalculated implying the controller needs to be redesigned. This approach also requires knowledge of the converter's passive components value such as the input and output capacitance which are values that change over time due to use. As a result, either the controller would need to be periodically updated or the converter would need to go through maintenance which could be costlier compared to using a current sensor.

Reference [52], [53] discuss a current-sensorless method utilizing a single voltage sensor that does not require knowledge of passive component values. Based on the operating duty-ratio, voltage, and the rate of change of both, an objective function equation is derived. When the objective function is equal to zero the system is at the MPP. An example of the implemented controller is shown Figure 1-20 utilizing (1.26) where d is the duty-ratio of the converter, v_{pv} is the operating voltage of the panel and dv_{pv} and dd are the rate of change of the panel voltage and duty-ratio respectively.

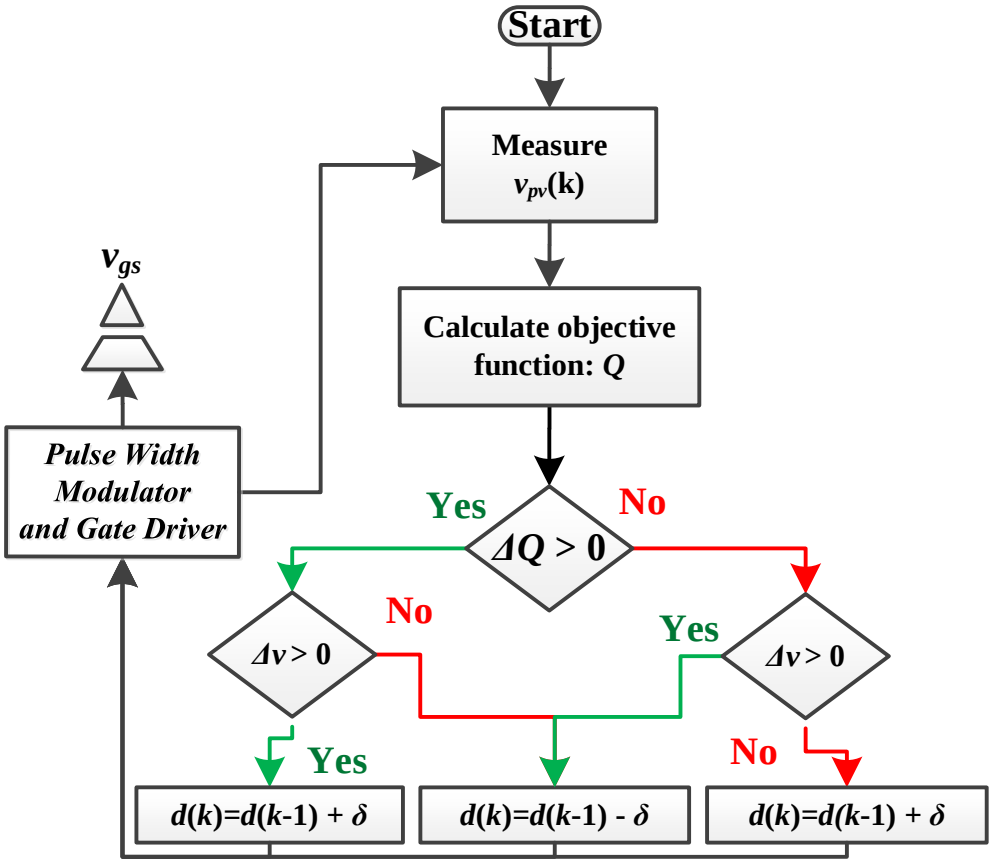


Figure 1-20 Single sensor current-sensorless algorithm discussed in [59]

$$Q = d\left(1-d\right)\times dv_{pv} + v_{pv}\times dd \tag{1.26}$$

$$\begin{aligned} &Q > 0 \text{ on the left of the MPP} \\ &Q < 0 \text{ on the right of the MPP} \\ &Q = 0 \text{ at the MPP} \end{aligned} \tag{1.27}$$

This method is a modified incremental conductance method as it utilizes rate of change of measurements and can determine the operating area of the converter on the MPP curve. Based on the calculated value of the objective function Q the controller can determine whether the system is operating to the left, the right or at the MPP (1.27) similar to how the incremental conductance algorithm functions. This method successfully removes the need for a current sensor and only utilizes a single voltage sensor which means compared to other discussed current-sensorless techniques it has a lower impact on the overall cost, power density, and complexity. However, it is specifically designed for a single-ended primary-inductance converter (SEPIC) which means as

with the other discussed methods, the algorithm's application is limited. In a MVDC scenario where different converters are utilized, this algorithm would not be sufficient. For example, if one converter were to be flyback while the other is SEPIC, the MPP controller would need to be different for each converter.

1.4 Modular Power Flow and Voltage Balancing

Multi-module converters can allow for the overall system to achieve a large output voltage while minimizing the voltage and current stress on each individual sub-module. This is especially useful in PV based MVDC topologies due to the large voltage mismatch between the PV arrays and the grid. There are four examples modular configurations that can be used which are highlighted in Table 1-4.

Table 1-4 Different types of modular configurations [54]

Configuration	**Applications**	**Issues and Drawbacks**
Input-Series Output-Parallel (ISOP)	High output voltage with low input voltage	Input voltage balance, additional stages required.
Input-Series Output-Series (ISOS)	High input and output voltage	Input and output voltage and power balance
Input-Parallel Output-Series (IPOS)	High output voltage with low input voltage	Voltage and Power balance
Input-Independent Output-Series (IIOS)	High output voltage with low input voltage	Voltage and Power balance

Of the aforementioned four configurations, input-parallel output-series (IPOS) and input-independent output-series (IIOS) topologies are able to achieve a high step-up gain with a low input voltage [54], [55], [56], however in the case of IPOS an additional conversion stage is required. Typically for IPOS systems, the input is connected to a low-voltage DC (LVDC) bus. This implies to utilize an IPOS system for PV energy applications, a converter is needed between the panel and the LVDC bus in addition to the step-up converter between the LVDC bus and the output. For an "N" module system, this implies the requirement of "N" additional converters. The IIOS connected modular configuration are seen as a feasible way to achieve high output voltage with high energy conversion. Connecting the output of each module in series allows for a higher output voltage as the modular output voltages are summed. Having input of each converter connected to different sets of independent PV panels allows for modules to operate at different locations. The light intensity of each PV array will vary due to atmospheric conditions such as

cloud cover and the angle of incident [57]. Therefore, each submodule will operate at a different power level. Due to the output series connection, each sub-module shares the same output current. As the current is the same while the operating power is different, it implies that the output voltages of each sub-module are unbalanced which can have an impact on the voltage-limitation requirements. To overcome these drawbacks, researchers have designed different topologies to help extend the safe operating range of the converters.

1.4.1 Multi-stage

Two-stage topologies, also known as cascaded converters, are composed of two back to back converters connected in series as discussed in section 1.2.2 An example of this for MVDC applications is shown in Figure 1-21. Each module's front end consists of a PV array connected to a DC/DC converter. This converter is typically used for MPPT and providing a minor step-up gain. From here the output is fed into a second DC-DC converter. The output of each module's second converter is connected in series with the other sub-module outputs to sums up the output voltage so that it can be connected to a MVDC bus as given by (1.28).

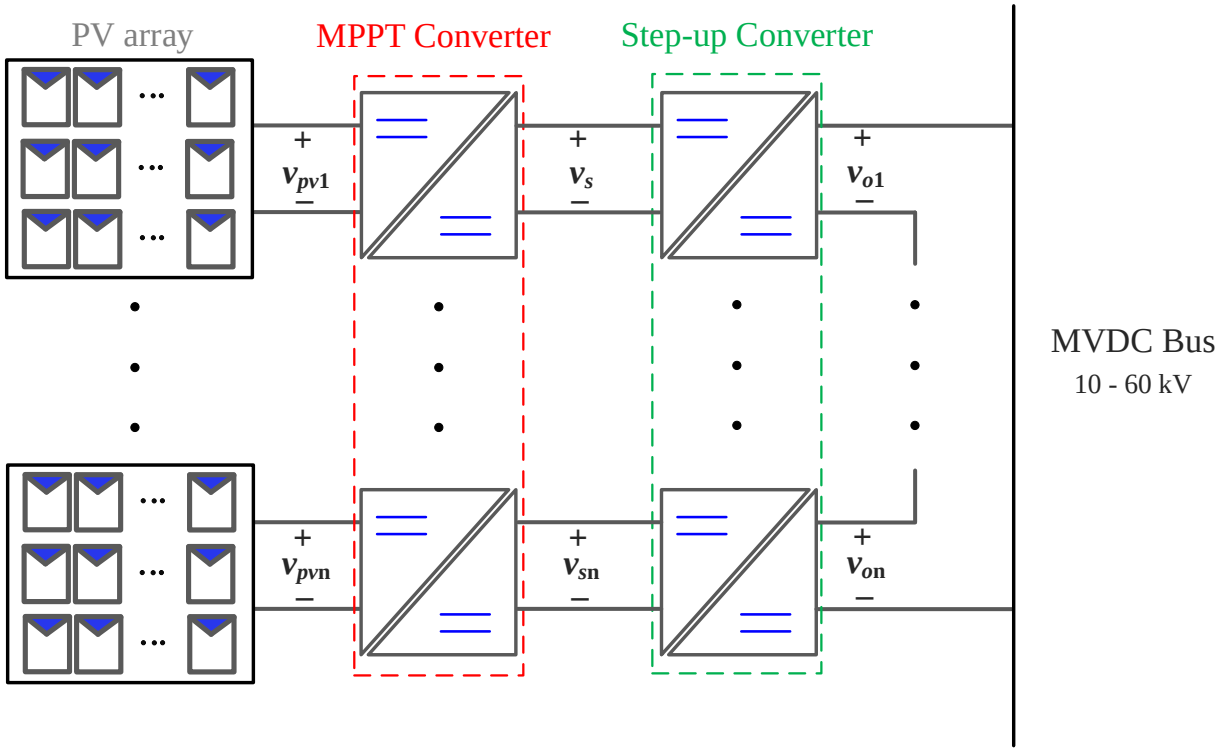


Figure 1-21 Example of a two stage MVDC system consisting of N series connected modules.

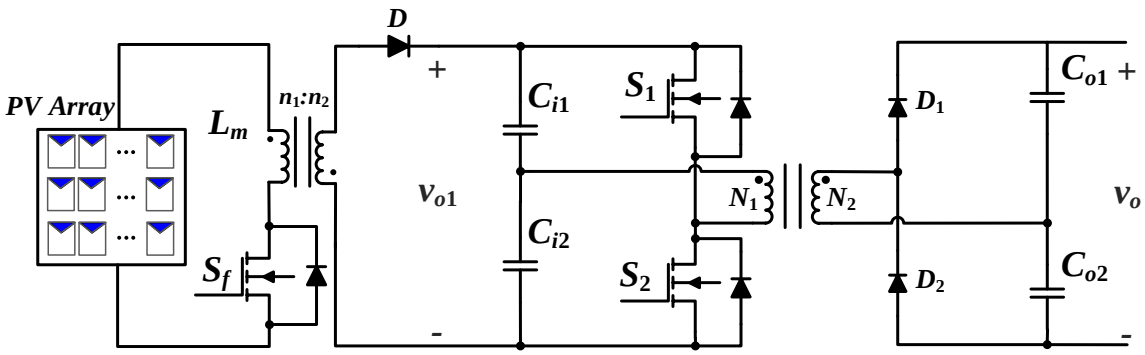


Figure 1-22 Cascaded Flyback Half-Bridge two-stage approach [59]

$$v_o = \sum_{i=1}^{n} v_{oi} \tag{1.28}$$

As the inputs are each connected to a different panel while the outputs are all connected together, the IIOS configuration is used. The two or more utilized DC-DC converters per module are typically different so that each can be designed for their specific task of MPP tracking and high voltage gain [58].

Reference [59] takes the multi-stage approach by using a flyback for the first stage and a half-bridge for the second stage as demonstrated in Figure 1-22. The flyback stage enables MPPT as well as a step-up gain through duty-ratio control on the switch S_f. This stage also provide isolation between the PV array and the grid due to the transformer L_m. The second stage regulates the total output voltage, v_o, while providing an additional step-up gain with a transformer and voltage doubler. The output of each module would be connected in series and the individual module output is regulated using the half-bridge switches. In total three switches are utilized and due to the half-bridge configuration, the stress across the two back-end switches are equal to the first-stage output voltage given by (1.29) where d is the duty ratio and n is the turns-ratio.

$$v_{s1} = v_{s2} = v_{dc} = \frac{nd}{1-d} \tag{1.29}$$

The controller employed to balance the output voltages calculates the power deviation between modules and then calculates the required duty-ratio of each second stage such that the

power deviation is zero or minimized. Equation (1.30) shows the transfer function relating the DC-link voltage and the total output power where N is the number of cells in the PV panel and C_1 is the DC-link capacitance and $\overline{v_{dc}{}^2}(s)$ is the average DC-link voltage provided in (1.31). For a more accurate transfer function the authors also included the parallel loss resistor of the DC-link capacitor as shown in (1.32).

$$\overline{v_{dc}{}^2}(s) = \frac{P(s)}{sNC_1} \tag{1.30}$$

$$\overline{v_{dc}{}^2}(s) = \frac{1}{N}\sum_{k=1}^{N} v_{dck}{}^2 \tag{1.31}$$

$$\overline{v_{dc}{}^2}(s) = \frac{P(s)\times R_{dc}}{sNR_{dc}C_1 + 1} \tag{1.32}$$

This implies that their proposed control algorithm requires the value of each DC-link capacitance, a value that can change over time. Also, the algorithm is reliant on the number of cells in the PV panel, suggesting that this method is only applicable to specific setups. The converter also utilizes a large turns-ratio in the front-end isolating flyback stage to allow for an increased step-up gain, to help with the previously discussed voltage regulation issue. However, each sub-module would require this ratio which increases the cost of the system. In their scaled down prototype, the authors utilized a turns-ratio of 1:3 for all eight modules with a primary side magnetizing inductance of 1mH. To achieve this large inductance several windings would be required for the primary side which is then tripled on the secondary side. This topology addresses the power mismatch issue to a certain degree however the capacity for voltage regulation is restricted based on the converter chosen for the second stage.

1.4.2 Multi-port

An alternative power and voltage regulation method adopted in literature is the use of an additional voltage bus for power collection. Instead of connecting two back-to-back converters in series, the output of the first converter is connected to a Low-voltage (LV) DC bus. From here the input of the second converter is also connected to the LVDC bus. The front-end converter of each submodule is connected in parallel while the output of each second converter are still connected

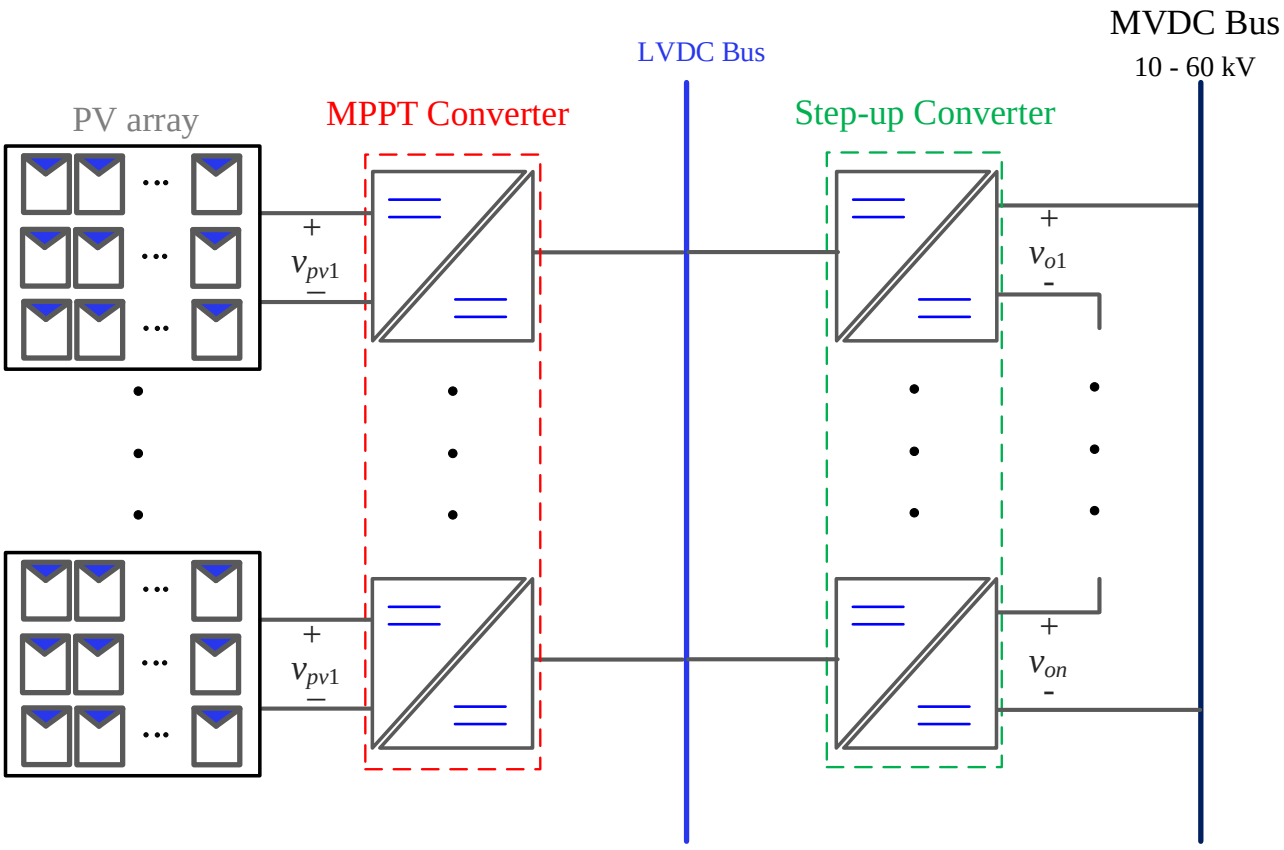


Figure 1-23 Example of a low voltage bus based MVDC system

in series to form a large step-up gain to connect to the MDVC grid. This configuration is the IPOS that was discussed at the start of section 1.4. An example of this configuration is provided in Figure 1-23. In PV energy applications, the front-end converters perform maximum power extraction while the back-end converters can independently balance their output voltage.

By utilizing an IPOS topology, the converter design is simplified. For the back-end converter, the input and output voltage are constant, therefore the peak voltage and current stress of components are known. The same applies to the front-end converter as knowing the peak operating power would allow the designer to select ideal components. However, utilizing multiple converters increases the size and cost of the system as well as impacts the system efficiency, which is an issue also present in multi-stage IIOS topologies.

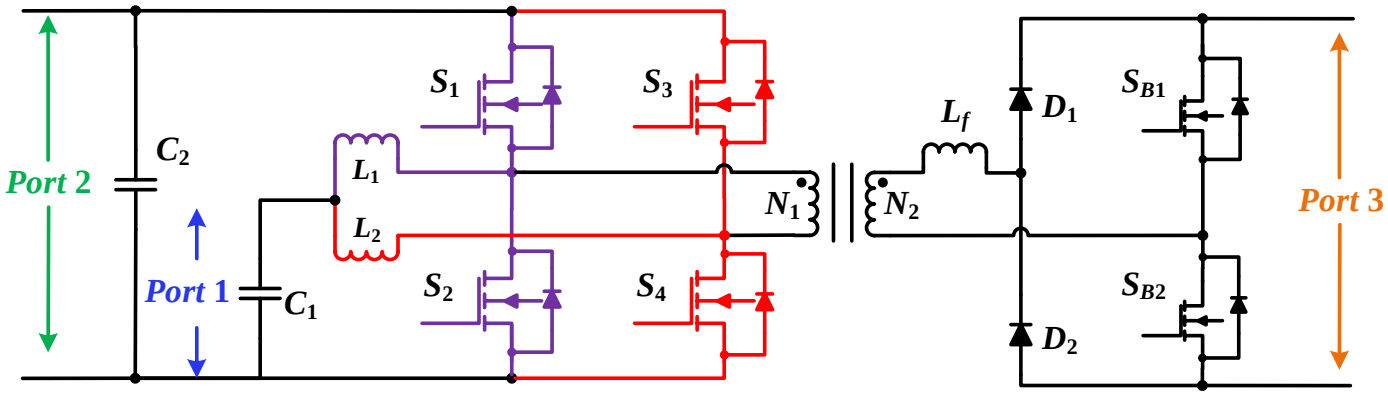


Figure 1-24 Example of the three-port converter discussed in [61]

Instead of utilizing two converters to connect to a LV and MV bus, an alternative option is the use of a three-port converters (TPC). [60] utilizes a full-bridge based converter connected to both a LV and HVDC bus. The first two ports of each module are connected in series with other modules which are then connected across the HVDC bus. The third port of each module is connected in parallel which the LV-DC bus to allow for power flow between each module. Integrated TPC are claimed to have increased efficiency with higher power density and lower weight and size compared to conventional solutions. However, the discussed solution still results in the panel power being processed twice. In [61], an interleaved bi-directional converter is utilized for the front-end converter to allow power to flow from either the input panel to the HVDC bus or the LVDC bus based on the controller setting while a bridge-less boost rectifier is used to connect the output of the front-end converter to the HVDC grid. An example of this system is shown in Figure 1-25. Although this system does allow for balanced output voltages of each sub-module, the semiconductor component count is high which leads to increased conduction loss and a lower overall system efficiency.

1.4.3 Power Balance Units (PBU)

Another method of ensuring a balanced output voltage across each module is by introducing additional components to form a power balance unit (PBU). These devices are typically placed between two modules, removing the series connection. From here the PBU regulates the power flow between modules such that the output voltages are balanced. A general diagram of a MVDC system consisting of PBU's between modules is shown in Figure 1-25. As a PBU is required between each module, for an "N" module system the total number of required PBU's is "N-1". There are several different PBU topologies which utilize either active or passive components.

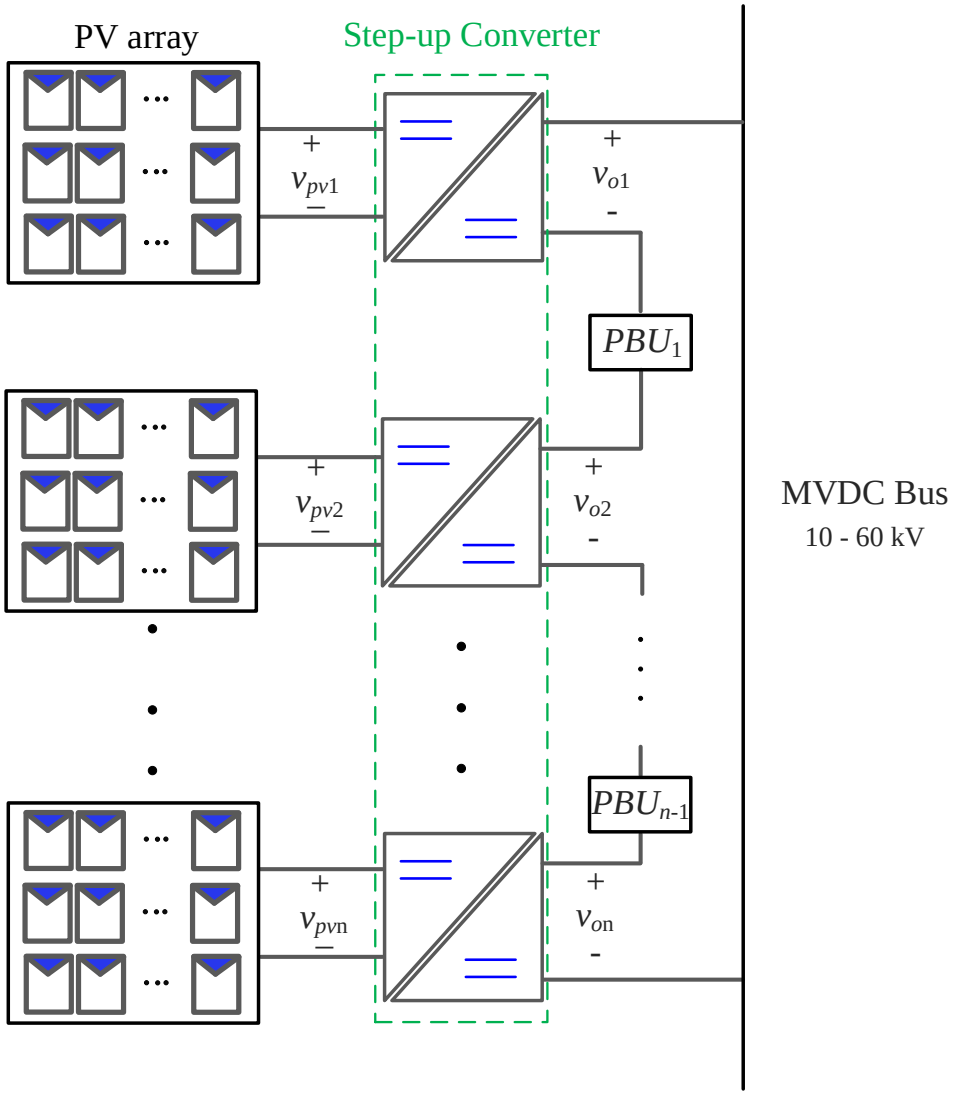


Figure 1-25 Modular system consisting of power balance units to regulate the per-module output voltage

1.4.3.1 Active Component Based PBU

[61] utilizes a PBU consisting of two switches and an inductor which operates similar to a bidirectional buck-boost converter was designed. This configuration allows for power transfer between modules based on the chosen duty ratio. The designed PBU is shown in Figure 1-26. and due to this configuration, the voltage balancing capabilities of the system is unlimited. Even if one module input power is zero, the output voltage of each sub-module can still be balanced. The main downside is this setup requires two active switches for each PBU which implies "2(N-1)" switches needed in total for an "N" module system. This drawback significantly increases the system cost and can lead to lower efficiency.

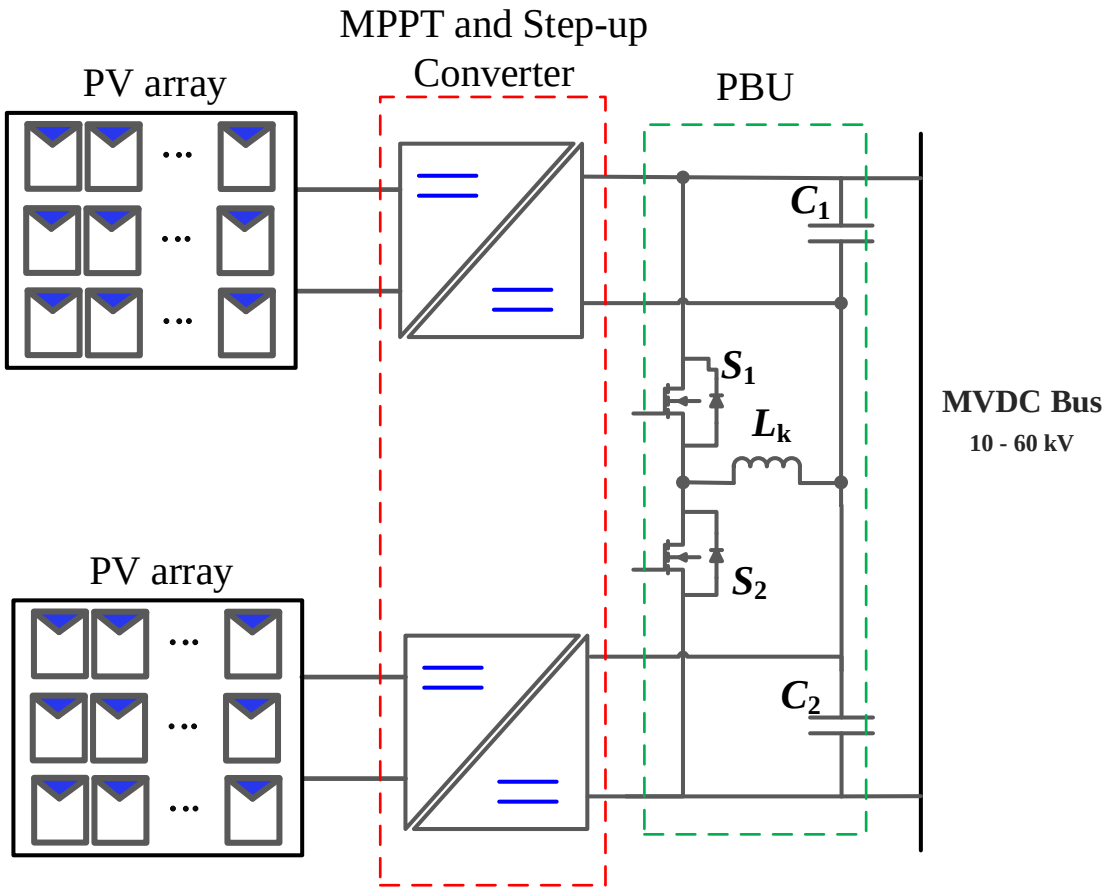


Figure 1-26 Modular MVDC system with power balance units [61]

[62] also utilizes two switches and an inductor to form a PBU however the control strategy is different from [61]. An example of the author's setup is shown in Figure 1-27. This PBU has one switch node connected to a DC link capacitor and another connected to an inductor. Only one switch is active at a time and its duty-ratio is controlled to regulate power flow. The unit operates under two modes. Mode A is shown in Figure 1-27 (a) and (b), which is when the system wants to transfer power from the module k to the module k+1. During this mode switch S_2 is off while switch S_1's duty-ratio is controlled to specify the amount of power transferred to module k+1. When the gate signal is applied to S_1, power from module k is stored in the inductor L_k. Once the gate signal is removed from the S_1, the inductor discharges through the anti-parallel diode of S_2 which allows the stored energy to transfer to module k+1. Mode B is shown in Figure 1-27 (c) and (d) and works exactly as mode A but transfers energy from module k+1 to k.

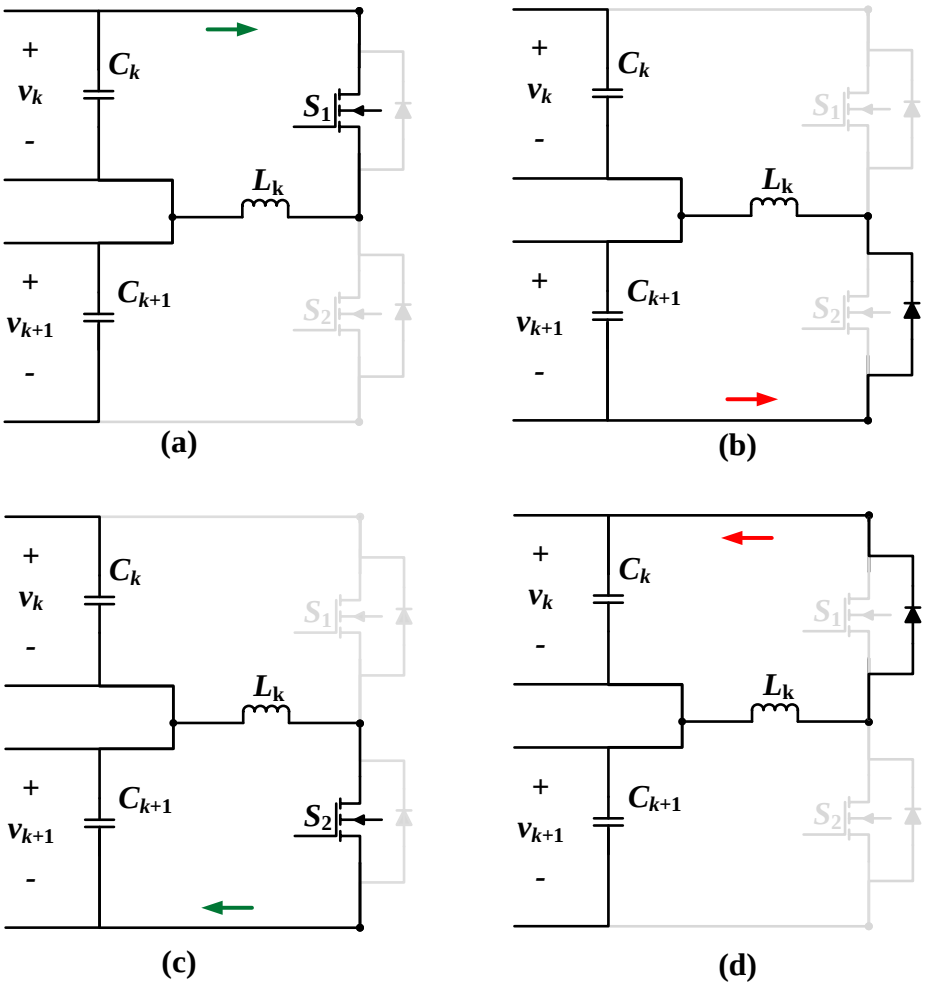


Figure 1-27 Operation of the power balance unit discussed in [62]: (a) and (b) Power transfer from module K to K+1, (c) and (d) Power transfer from module K+1 to K

1.4.3.2 Passive Component Based PBU

[63] utilizes an alternative configuration using only an inductor and a capacitor as shown in Figure 1-28. The converter consists of a full-bridge circuit on the PV side and a half-bridge circuit on the grid side. This topology is able to achieve individual MPPT and voltage balancing through the use of six switches. The phase shift of the four full-bridge switches (S_1-S_4) can be controlled to track the MPP through phase-shift modulation. The output voltage of each module is balanced using the additional capacitor C_{Bk} and inductor L_{Bk} while gating the secondary side switches. This implies the system discussed in [63] achieves MPPT and voltage balancing individually.

The capacitor C_{Bk} is the power transfer point between modules. While the secondary switch is gated the current through the inductor L_{Bk} is positive and power is transferred from the other module capacitors to C_{Bk}. Once the gate signal is removed from the switch the current through the inductor begins to decrease and power is transferred to the other modules. This implies that the

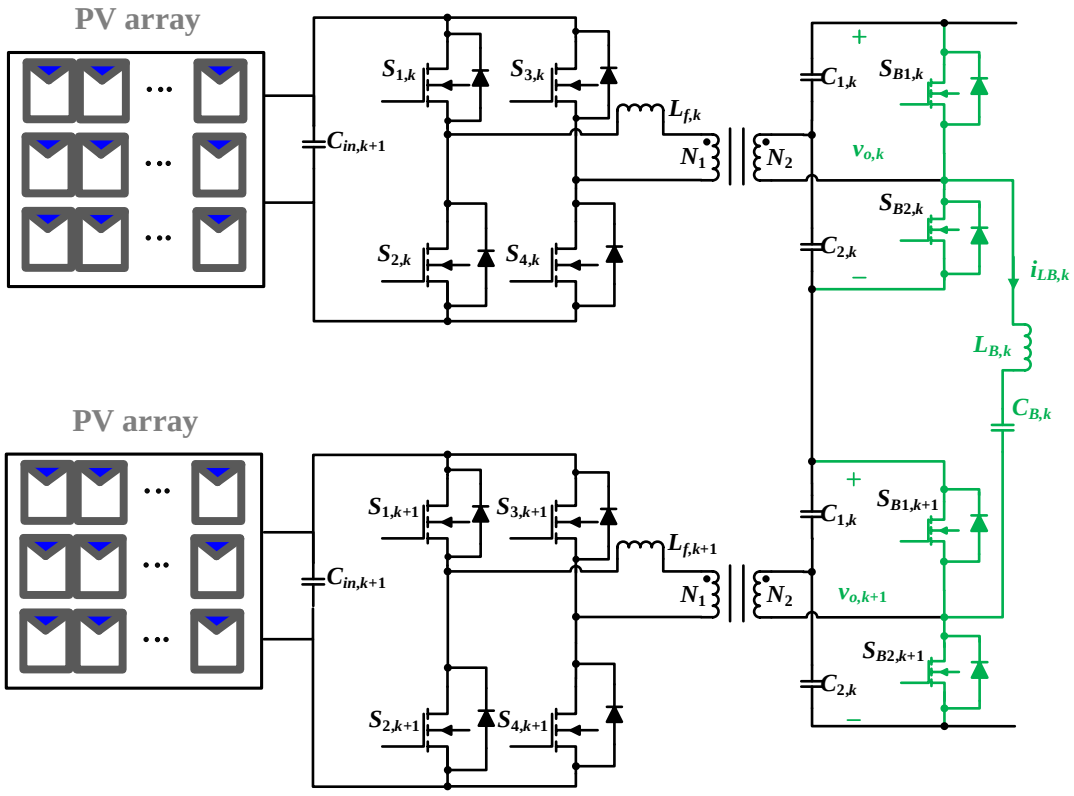


Figure 1-28 Modular converter consisting of a power balance unit to regulate the output voltage [63]

power transferred to a module is a function of the module voltage and the current flowing through

the PBU inductor as shown in (1.33). Further, the current flowing through the PBU inductor is related to the length of time in one switching period that the switch is gated, as given by (1.34).

$$P_{B,k} = V_{SM,k} I_{LB,k} \frac{\left(1-2d_{B,k}\right)}{2} \tag{1.33}$$

$$I_{LB,k} = V_{SM,k} \frac{d_{B,k}}{4 f_s L_{B,K}} \tag{1.34}$$

By utilizing a switch-less PBU, the power efficiency of the system is improved compared to [62]. The topology also allows for the system to operate with a low voltage stress over each of the six switches. The authors claim the switches operate under ZVS at all scenarios and takes less than 200ms to balance the module voltages.

1.5 Research Objectives

Various types of power electronic converters designed for MVDC applications as well as MPPT controllers have been introduced and discussed for PV energy applications. However, these topologies and techniques suffer from one or more of the follow challenges.

- Current sensor based maximum power point tracking

- Single sensor based maximum power point tracking designed for limited topologies;

- Modular converter design approach with low step-up voltage conversion ratio

- Lack of efficient power and voltage balance techniques or additional components;

- Limited soft-switching condition or additional circuitry required.

The proposed research is aimed at developing a novel modular MVDC system for PV energy system by overcoming the aforementioned drawbacks. The objectives of this research are as follows:

(1) Develop a new high-gain step-up converter that can be extended to modular structure while provided soft-switching condition over a wide range.

(2) Develop a new robust single-sensor based maximum power extraction algorithm that can be applied to several topologies including the topology developed in (1) that operate with a single voltage sensor.

(3) Develop an integrated power balance unit and controller capable of achieving balanced output voltage for modules that are arranged in either linear and circular based configurations, where each module utilizes the converter from (1).

(4) Develop control techniques to optimize the power flow of the modular system in (3) to improve the system efficiency and circuit operation while minimizing component voltage and/or current stress.

Each of the outlined research goals should be achieved while ensuring the functionality of the entire system. For example, the developed power balance unit technique (3) should not interfere with the single-sensor maximum power extraction algorithm (2) and the efficiency optimizing algorithm (4) must not affect both the (2) and (3).

1.6 Dissertation Outline

In Chapter 1, the concept of modular PV MVDC system was introduced. A review of different step-up power electronic converter for PV MVDC applications was presented. To ensure effective power extraction for the system, various types of classic and intelligent maximum power extraction techniques along with their strengths, drawbacks, and implementation challenges have been addressed. Then, topologies and control techniques to resolve issues regarding modular power and voltage imbalance have been discussed. Towards the end, the research motivations of this dissertation, as well as its organization were highlighted in this chapter.

In Chapter 2, a novel single-sensor current-sensorless maximum power extraction controller is proposed together with a new high step-up converter with complete soft-switching operation suitable for PV energy systems. The designed converter utilizes an integrated boost and *CLL* resonant converter to take advantages of both topologies while minimizing the component count. The *CLL* resonant converter utilizes an isolating coupled inductor which connects to a high gain voltage quadrupler (VQ) rectifier to ensure a high voltage gain in all scenarios.

The proposed controller utilizes an alternative voltage signal and aims to maximize this parameter such that the operating power of the input PV array is indirectly maximized. To allow for fast and accurate tracking compared to classic algorithm, the proposed controller employs a modified gradient ascent algorithm. Analysis and design of the controller and converter are provided in this chapter. Operation of the overall system is examined in simulation and the feasibility of the design in the real world is evaluated with a scaled down proof-of-concept hardware prototype.

In Chapter 3, a power balancing technique utilizing high frequency coupled inductors and active voltage quadruples is proposed for modular MVDC based PV energy systems. In the proposed approach, the converter designed in Chapter 2 is extended by modifying the series output inductor of the *CLL* resonant circuit such that an additional power flow path is created between modules. From here the voltage quadrupler updated to include an active switch whose duty-ratio can be controlled to regulate the power flow. As the power is shared between modules before the voltage quadrupler, the proposed technique can achieve balanced output voltage and a high step-up gain across a wide operating range. The proposed topology is capable of achieving soft-switching operation on all switches. To highlight the benefits of the proposed system, the operation

of the converter topology and power balance unit are first verified by the means of simulation and then through experimental work on a scaled down proof-of-concept hardware prototype.

In Chapter 4, the performance of the active voltage quadrupler and the proposed system's efficiency is examined and an optimized controller to enhance the overall system efficiency for a wide operating range is devised. The proposed approach optimizes the power transfer of each modules PBU such that the per-module conduction loss is reduced under all scenarios. In addition, the approach optimizes the voltage ratio between the output capacitors and in turn minimizes, the voltage stress across the active voltage quadrupler (AVQ) switch. The performance of the proposed controller is verified through simulation and experimental work on a scaled down proof-of-concept hardware prototype.

In Chapter 5, the contributions of this dissertation are highlighted. Possible future work related to improving the topologies and controllers discussed this dissertation as well enhancing the area of application are proposed.

Chapter 2. Proposed Single-Sensor Current-Sensorless Based Maximum Power Extraction Algorithm for PV Energy Systems

To reduce the reliance of current sensors which are known to introduce uncertainties in system operation through noise while also driving up the system cost, the current research trend is to utilize current-sensorless MPPT algorithms. This chapter focuses on the development of a current-sensorless based maximum power extraction algorithm for use with PV energy systems.

The first part of this chapter will discuss a novel high step-up DC-DC converter with complete soft-switching operation for PV energy systems. The proposed topology will employ a step-up resonant converter to achieve a large output gain compared to other topologies developed in literature. By operating under soft-switching condition, the converter can utilize a high switching frequency allowing for smaller sized components and a higher power density while also improving the system efficiency. The duty-ratio of each switch can be regulated to achieve MPP operation. Both design equations and the operation stages of the proposed converter will be provided and discussed.

The second part of this chapter will discuss a new single-sensor, current-sensorless maximum power extraction algorithm for PV energy systems that is compatible with various step-up DC-DC converter including the topology proposed at the start of this chapter. Operating principles and analysis of the controller will be provided. Finally, to confirm the operation of the proposed maximum power extraction algorithm, the performance of both the converter and the controller are verified through simulation and experimental work on proof-of-concept prototypes.

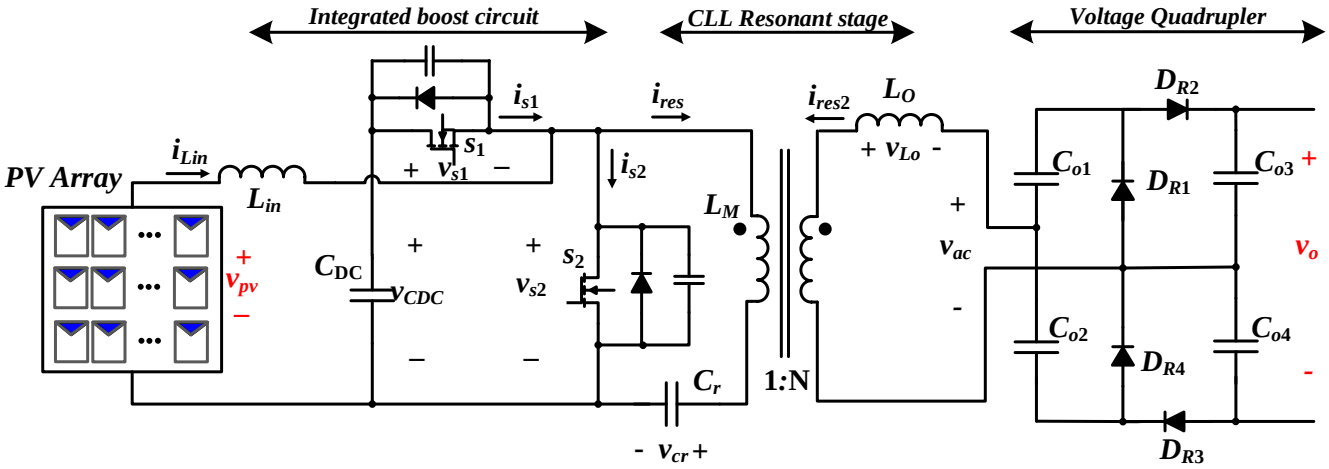


Figure 2-1 Proposed high step-up gain DC-DC converter with complete soft-switching operation for PV energy systems

2.1 DC/DC Converter Topology

Resonant topologies are a popular configuration in PV applications due to their step-up gain, isolation, and soft-switching capabilities, which makes a suitable choice for MVDC systems. As discussed in Chapter 1, a switch network, resonant tank, and a rectifier are typically used in these topologies. The switch network can then be controlled to achieve maximum power operation. Figure 2-1 shows the proposed high step-up gain DC-DC converter. The input stage of the proposed converter consists of PV arrays connected to an integrated boost-*CLL* resonant circuit. In this converter, the boost diode is replaced with a switch and the output capacitor is removed such that the output is an AC waveform. As a result, two switches, S_1 and S_2, are used to boost the PV voltage as well as to provide maximum power extraction with duty-ratio control. The switches operate with complimentary duty-ratio which means when S_1 is on S_2 is off and vice-versa. This technique generates a rectangular AC voltage waveform across S_2 which form the input to the *CLL* resonant stage. This stage consists of a series capacitor C_r, a magnetizing coupled inductor L_M, and a series output inductor L_o. The coupled inductor provides isolation between the primary and secondary side while its 1:N turns-ratio provides an additional step-up voltage gain. The output of the *CLL* resonant stage connects to a voltage quadrupler which rectifies the *CLL* output voltage to DC and provides a further step-up gain.

2.1.1 Proposed Converter Operating Principles

This section will provide an in-depth look at the operating principles and stages of the proposed converter step-up converter. To simplify the discussion, the converter will be discussed in two parts which are the input to the resonant stage and the voltage quadrupler rectifier. In order to discuss the converter operating principles, the following assumptions are made.

1) All components, such as semiconductor switches and diodes, inductors, and capacitors are ideal unless stated otherwise.

2) The coupled inductor leakage inductance is neglected.

3) The duty-ratio of switch S_2 is greater than S_1.

2.1.1.1 Input and Resonant stage

The theoretical operating waveforms of the proposed converter are provided in Figure 2-2 for a duty-ratio, *d*, greater than 50% while the various operating modes are provided in Figure 2-3. A dead-time is utilized between the gate signals to ensure soft-switching turn-off condition.

[$t_0 < t < t_1$]: At time t_0, the gate signal, v_{gs1}, is applied to the switch S_1 and removed from the switch S_2. The current that was once flowing through S_2 begins to flow in the direction of S_1. From Figure 2-3 (a), it can be understood that this current is the difference between the resonant current and the input current. As the input current is larger than the resonant current, this value is negative and thus flows through the anti-parallel diode of S_1. During this time period, the voltage across the input inductor, L_{in}, is the difference between the input PV and DC-link voltage. As this is a step-up converter it is evident that this value is negative and hence, the inductor current is decreasing while the resonant stage current is increasing. Therefore, the current through the anti-parallel diode is increasing. S_1 will achieve ZVS turn-on operation when this current transitions from negative to positive at time t_1.

[$t_1 < t < t_2$]: At time t_1, switch S_1 turns on under ZVS condition. As the resonant current is sinusoidal, it will eventually reach its maximum point and then begin to decrease which occurs at time t_2.

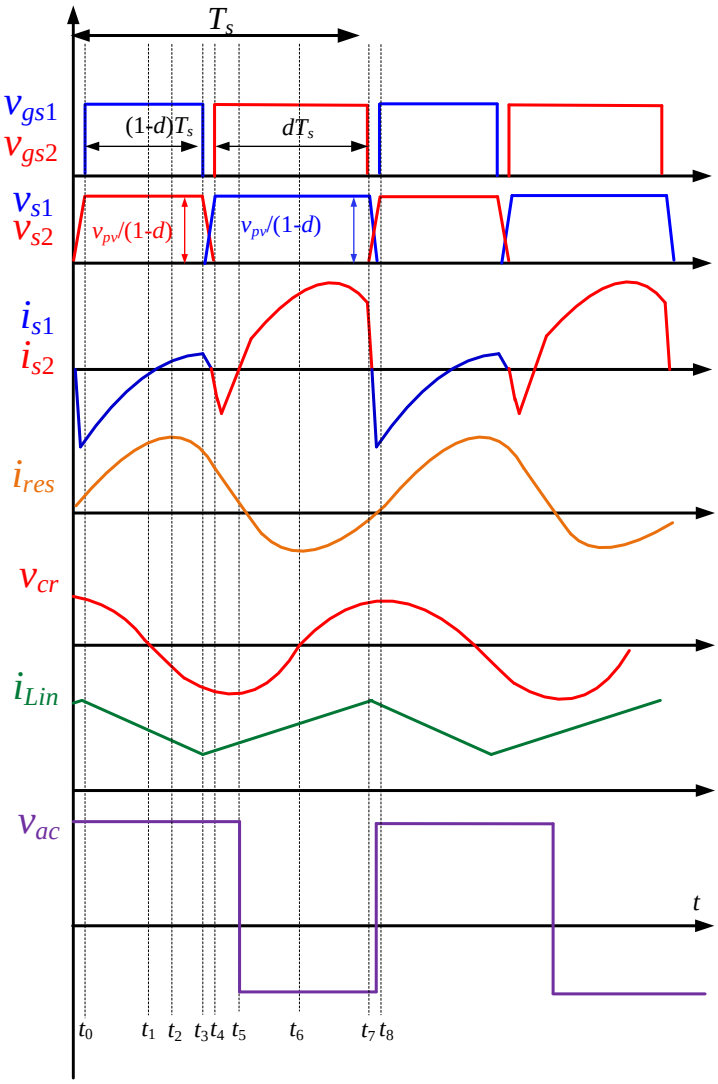


Figure 2-2 Theoretical operating waveforms of the proposed converter

[$t_2 < t < t_3$]: At time t_2, the resonant current has reached its peak value and begins to decrease. The rate of decrease is less than the rate at which the input current is decreasing and as a result, the current through S_1 continues to increase. This persists until the gate signal is removed from S_1.

[$t_3 < t < t_4$]: At time t_3, gate signal is removed from S_1 and the voltage across the snubber capacitor begins to decrease. There is a small deadtime from when the gate signal is removed from S_1 and applied to S_2 which lasts from t_3 to t_4. During this transition period, the voltage across S_1's snubber capacitor increases while the voltage across S_2's snubber capacitor decreases. The deadtime is chosen such that the system achieves near zero turn off losses.

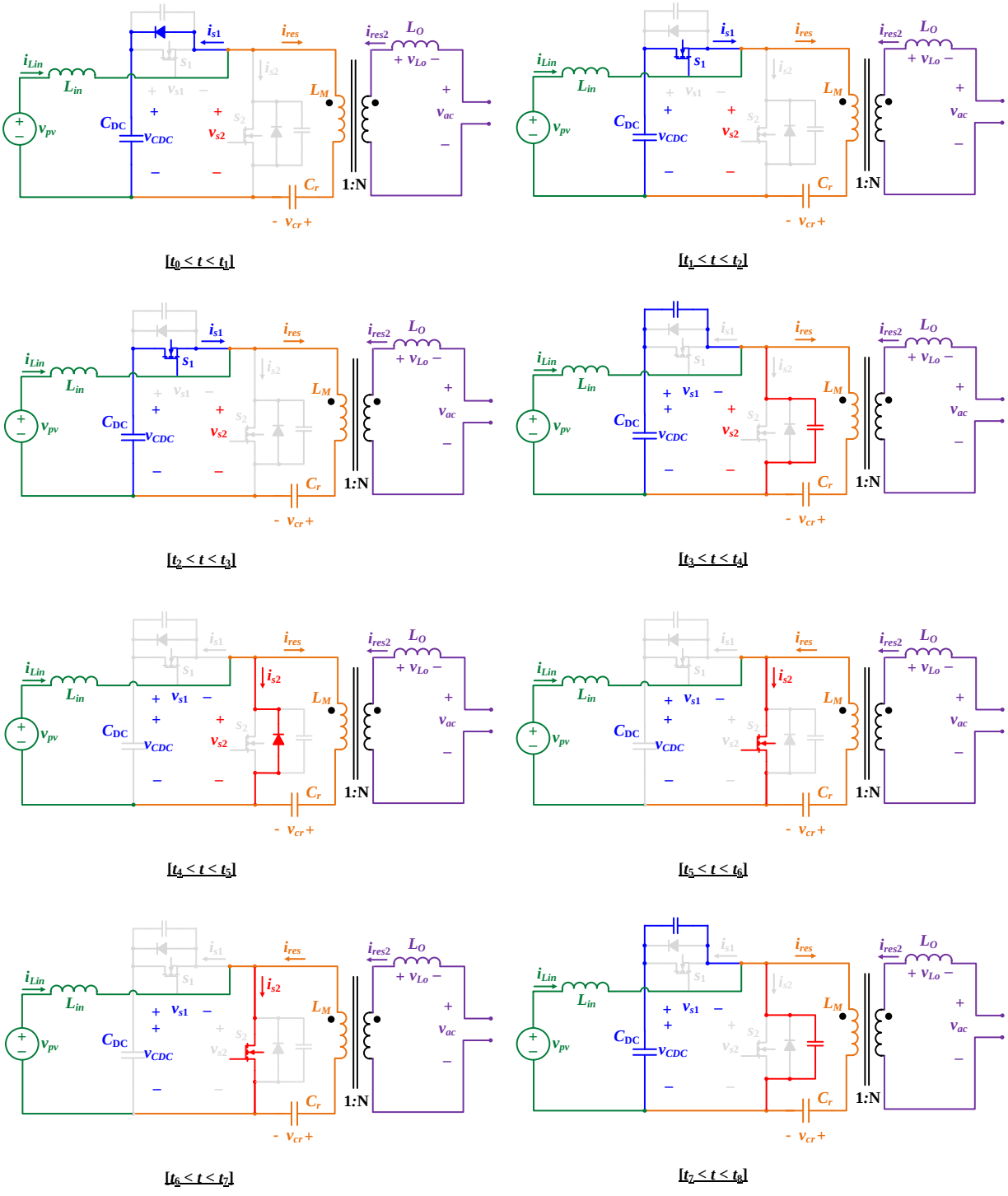


Figure 2-3 Theoretical operating waveforms of the proposed converter

[$t_4 < t < t_5$]: At time t_4, the gate signal, v_{gs2}, is applied to switch S_2. The current flowing through S_2 is the difference between the input inductor current and the resonant current. As the resonant current is still greater than the input inductor current, it implies that the current through S_2 is negative and flows through its anti-parallel diode. During this time period, the negative terminal of the input inductor is connected to ground through S_2, which implies it is connected in parallel with the PV panel and that the voltage across the inductor is positive. This results in an increase in the current through the inductor and in turn an increase in the switch current. This continues until the current through S_2 reaches zero.

[$t_5 < t < t_6$]: At time t_5, S_2 turns on under ZVS condition. This time period is close to when the resonant current reaches zero and continues to decrease. From the basic capacitor current equation, it is understood that the capacitor current crosses zero when the rate of change of the capacitor voltage is zero. Therefore, the resonant capacitor reaches its minimum value at this point and begins to increase. As the switch current is the difference between the input and resonant current, the rate at which the switch current is increasing rises. Due to the resonant current's change in polarity, the output voltage of the resonant circuit becomes negative. This stage ends once the resonant capacitor voltage is zero.

[$t_6 < t < t_7$]: At time t_6, the resonant capacitor voltage reached zero and begins to increase. From the basic capacitor current equation, it is understood that as the capacitor voltage is positive, the capacitor current begins to increase. This results in a decrease in the switch current. This continues until the gate signal is removed from S_2.

[$t_7 < t < t_8$]: At time t_7, gate signal is removed from S_2 and the voltage across the snubber capacitor begins to decrease. There is a small deadtime from when the gate signal is removed from S_2 and applied to S_1 which lasts from t_7 to t_4. During this transition period, the voltage across S_2's snubber capacitor increases while the voltage across S_1's snubber capacitor decreases. The deadtime is chosen such that the system achieves near zero turn off losses. This stage ends once the gate signal is applied to S_1 and the system transitions back to the first state.

2.1.1.2 Voltage Quadrupler Stage

The proposed converter utilizes a VQ to rectify the *CLL* resonant output. VQs were previously mentioned in section 1.2.3 however the circuit operation was not discussed. Figure 2-4 shows the operating waveforms of the VQ assuming the output voltage of the *CLL* resonant circuit is the same as shown in Figure 2-2.

[$t_0 < t < t_1$]: At time t_0, the input voltage to the VQ, v_{ac}, is positive and as a result, diodes D_{R2} and D_{R4} are active while D_{R1} and D_{R3} are inactive as shown in Figure 2-5(a). The input is directly connected across Co_2 as illustrated with the green loop in Figure 2-5(b), leading to (2.1).

$$v_{c2} = v_{ac} \tag{2.1}$$

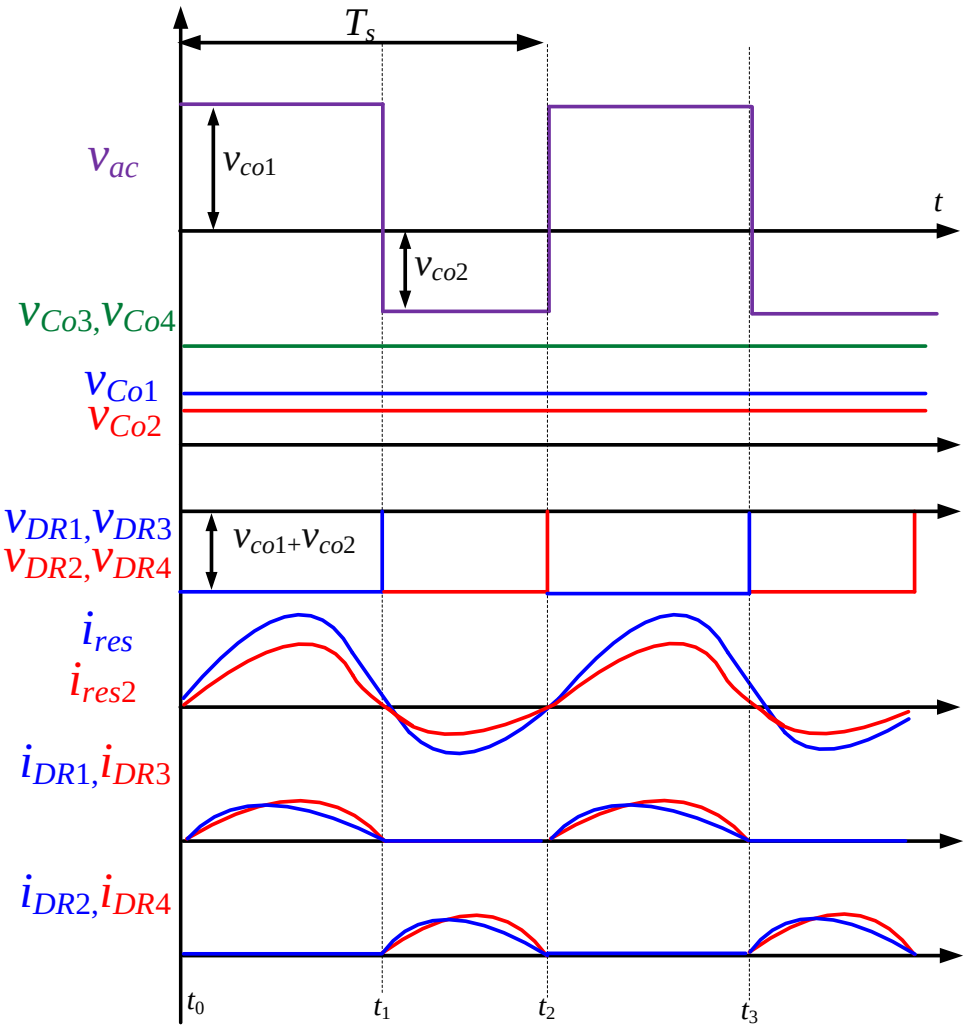


Figure 2-4 Theoretical operating waveforms of the voltage quadrupler

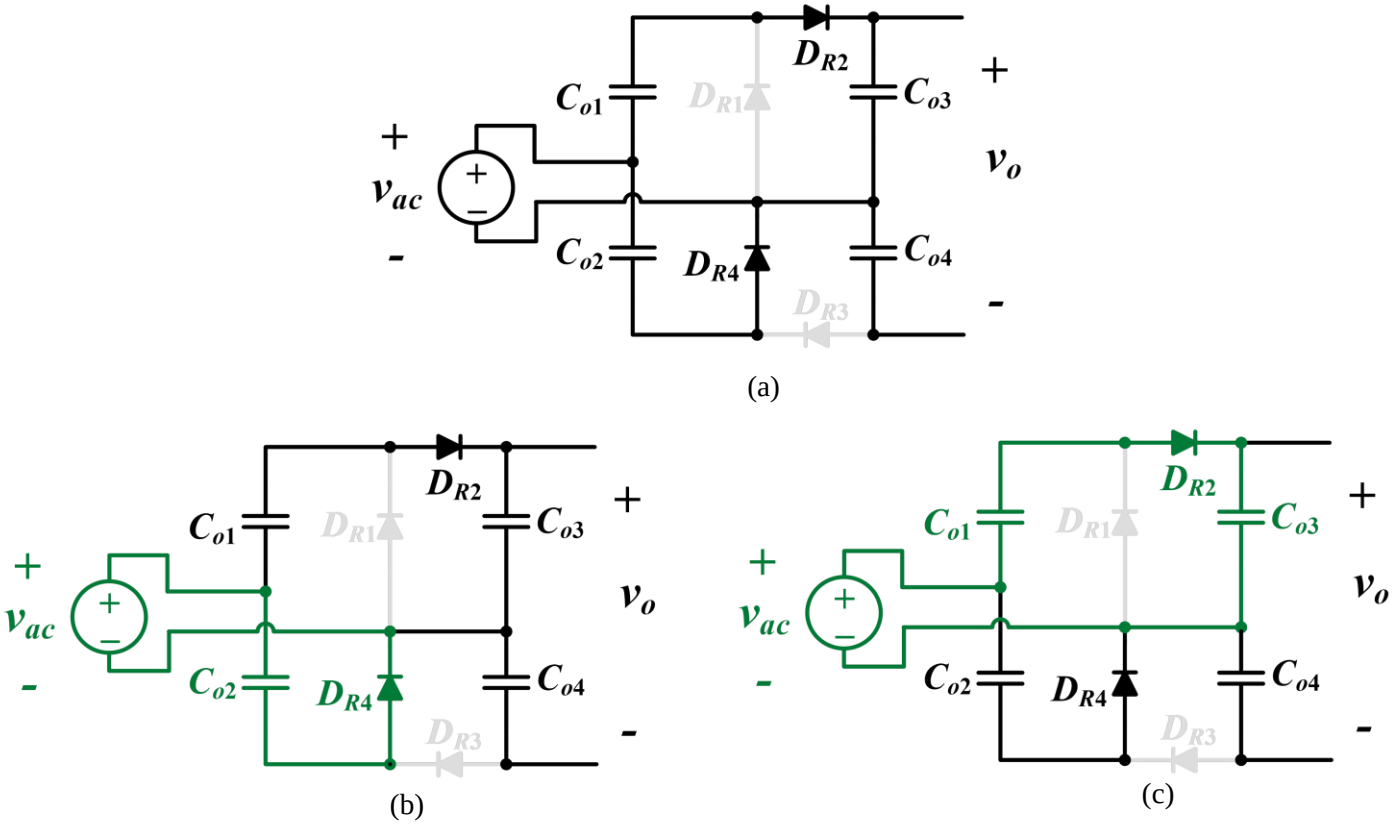


Figure 2-5 (a) Active components of the voltage quadrupler during **[$t_0 < t < t_1$]**, (b) KVL loop for Co_2, (c) KVL loop for Co_1.

As D_{R1} is inactive, the input voltage is also connected across both Co_1 and Co_3 as seen in Figure 2-5(c) which leads to (2.2) and finally (2.3).

$$v_{ac} = -v_{c1} + v_{c3} \tag{2.2}$$

$$v_{c3} = v_{c1} + v_{c2} \tag{2.3}$$

This stage ends once the input voltage to the VQ transitions from positive to negative. From the theoretical operating waveforms shown in Figure 2-2, it is understood that this occurs when the resonant current transitions from negative to positive.

[$t_1 < t < t_2$]: At time t_1, the input voltage to the VQ is positive and as a result, diodes D_{R2} and D_{R4} are active while DR$_1$ and D_{R3} are inactive as shown in Figure 2-6(a). The input is directly connected across Co_2 as seen in Figure 2-6(b) which leads to (2.4).

$$v_{c1} = v_{ac} \tag{2.4}$$

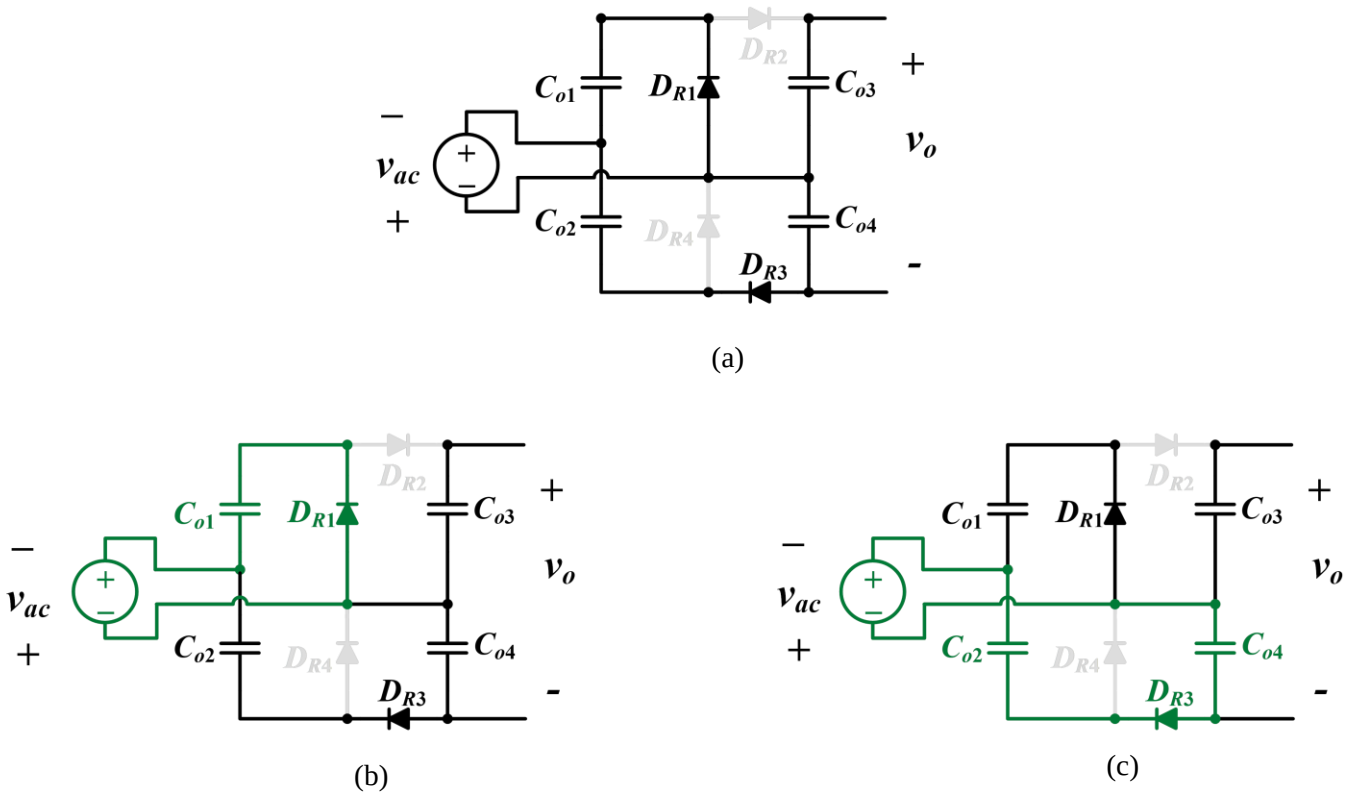


Figure 2-6 (a) Active components of the voltage quadrupler during **[$t_1 < t < t_2$]**, (b) KVL loop for C_1, (c) KVL loop for C_2.

Due to D_{R2} being inactive, the input voltage is also connected across both Co_2 and Co_4 as seen in Figure 2-6(c) which leads to (2.5) and finally (2.6).

$$v_{ac} = -v_{c2} + v_{c4} \tag{2.5}$$

$$v_{c4} = v_{c1} + v_{c2} \tag{2.6}$$

From the above discussion, it can be understood that the voltage across the output capacitors Co_3 and Co_4 are equal in all scenarios, however the voltage across the input capacitors Co_1 and Co_2 can be different. In the case the maximum and minimum are equal in magnitude and opposite in polarity, the input capacitor voltages would be balanced however in all other cases they are unbalanced.

2.1.2 Proposed Converter Theoretical Analysis

This section will provide an in-depth steady state analysis on the characteristic of the proposed converter. In order to perform steady state analysis, the assumptions provided in section 2.1.1 are once again used.

2.1.2.1 DC-Link Capacitor and Input Switch Voltage

The input stage of the proposed converter is shown in Figure 2-7 up to the magnetizing inductance. The peak voltage across both switches are seen to be the same as a standard boost converter. Switches S_1 and S_2 operate with complementary duty ratios, that is to say when S_1 is on, S_2 is off, and vice versa. The output of the boost stage is the voltage across the DC-link capacitor C_{DC}. Figure 2-7 shows the operating condition of the input boost stage when S_1 is on and S_2 is off (a) and when S_2 is on and S_1 is off (b) respectively. When S_1 is on, the nodes of S_2 are connected across C_{DC} through S_1, and when S_2 is on, the nodes of S_1 is connected across C_{DC} through S_2. Based on this, the peak voltage across each switch and the DC-link capacitor can be obtained (2.7)

.

$$v_{s1} = v_{s2} = v_{CDC} = \frac{v_{pv}}{1-d} \tag{2.7}$$

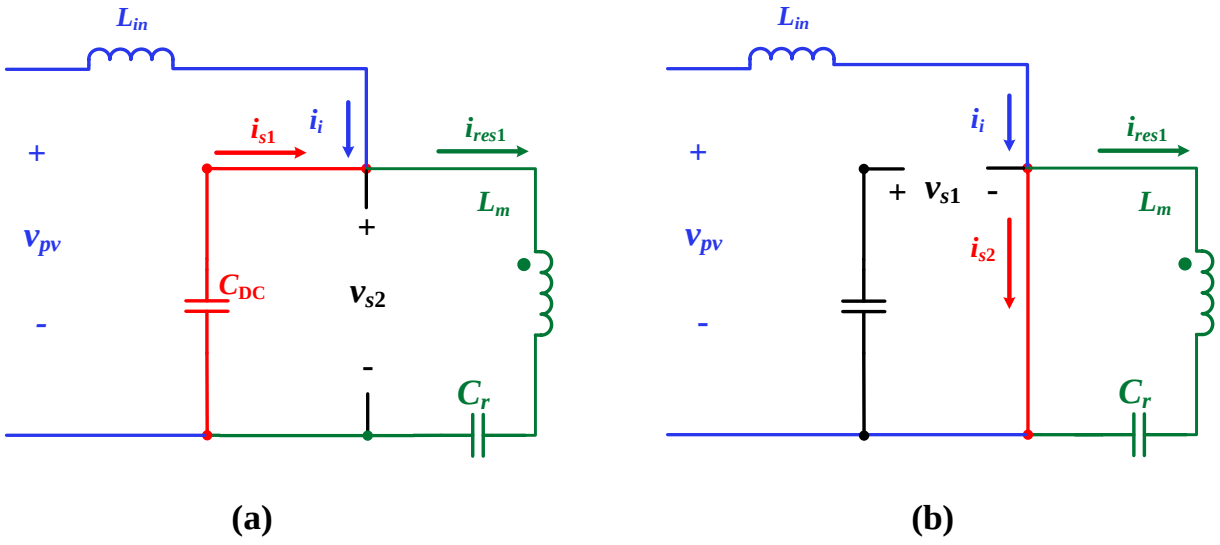


Figure 2-7 Input stage during (a) S_1 on (b) S_2 on.

2.1.2.2 *CLL* Resonant Input Voltage

The switching of S_2 generates a rectangular voltage waveform which is applied to the input of the *CLL* resonant circuit. The peak of this waveform is v_{s2} which was provided in (2.7) while the minimum of the waveform is zero. The duty-ratio of S_2 dictates the shape of this waveform, for example if the duty-ratio is 50% then the resulting voltage waveform will be square. The Fourier series representation of this waveform is provided in (2.8). It can be seen that this waveform consists of both a DC and an AC component, however due to the DC blocking capability of the resonant capacitor (C_r), only the AC component is applied to the resonant circuit. This AC component is provided in (2.9) where f_s is the operating switching frequency and θ is the phase angle (2.10).

$$v_{res} = \frac{v_{pv}}{1-d} + v_{s(ac)} \tag{2.8}$$

$$v_{res} = v_{s(ac)} = \frac{\sqrt{2}v_{pv}}{\pi(1-d)}\sqrt{1-\cos(2\pi d)}\sin(2\pi f_s t + \theta) \tag{2.9}$$

$$\theta = \tan^{-1}\left(\frac{\sin(2\pi d)}{1-\cos(2\pi d)}\right) \tag{2.10}$$

2.1.2.3 Magnetizing Inductance Voltage

The resonant stage is isolated through the use of a coupled inductor. Typically, the voltage across an inductor is a function of only the inductor current (2.11), however, for a coupled inductor, the voltage across a winding is a function of the current through each winding and the turns-ratio [64]. The relationship between the primary and secondary winding voltage is provided in (2.12) where n_1 is the amount of turns for the primary winding, n_2 is the amount of turns for the secondary winding, N is the ratio between the two side's windings, v_{LM1} is the primary side voltage and v_{LM2} is the secondary side voltage. The ratio between each side's inductance, which is known as the magnetizing inductance, L_m, can also be expressed as function of the turns-ratio (2.13). For example, if the turns-ratio is 1:2, it implies that the secondary side voltage and inductance will be two times and four times the primary side respectively. The voltage across each winding can be expressed as the rate of change of the current through each winding. This is provided in (2.14) and

(2.15) respectively where i_{res1} and i_{res2} is the current through the primary and secondary winding of the magnetizing inductor respectively.

$$v = L\frac{di}{dt} \tag{2.11}$$

$$v_{Lm2} = v_{Lm1}\frac{n_2}{n_1} = N \times v_{Lm1} \tag{2.12}$$

$$L_{m2} = L_{m1}\left(\frac{n_2}{n_1}\right)^2 = N^2 \times L_{m1} \tag{2.13}$$

$$v_{Lm1} = L_m\frac{di_{res}}{dt} + L_m N\frac{di_{res2}}{dt} \tag{2.14}$$

$$v_{Lm2} = L_m N\frac{di_{res}}{dt} + L_m N^2\frac{di_{res2}}{dt} \tag{2.15}$$

2.1.2.4 Resonant Capacitor Voltage

Equations (2.14) and (2.15) are expressed in terms of the rate of change of the resonant current, which is an issue as this parameter is unknown. In order to obtain an equation for the resonant current, the resonant capacitor voltage needs to be examined. Figure 2-8 displays the input and resonant stage of the proposed converter. By applying Kirchhoff's voltage law (KVL) to the green loop which consists of the switch S_2, L_m and the resonant capacitor, C_r, the equation for the resonant capacitor voltage is obtained (2.16) and the primary winding voltage, V_{Lm1}, from (2.14) can be substituted which results in (2.17).

$$v_{Cr} = v_{s2} - v_{Lm1} \tag{2.16}$$

$$v_{Cr} = v_{s2} - \left(L_m\frac{di_{res1}}{dt} + L_m N\frac{di_{res2}}{dt}\right) \tag{2.17}$$

The resonant capacitor voltage is now represented in terms of the rate of change for both the primary and secondary winding current. In order to represent the voltage in terms of only the primary winding current, an equation representing the secondary winding current is required. KVL can be applied to the red loop in Figure 2-8 which consists of the secondary winding of L_m, the output inductor L_o, and the resonant stage's output voltage v_{o1} (2.18). From here (2.15) is

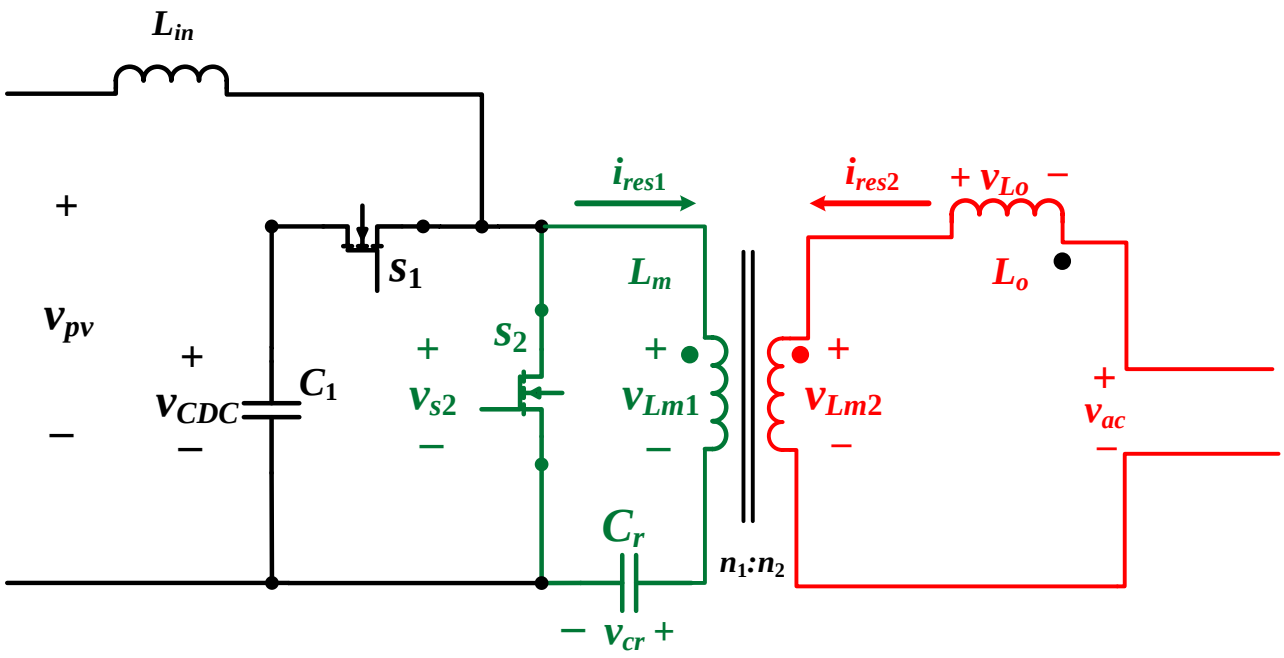


Figure 2-8 Input and Resonant Stage of the Proposed Converter

substituted into the left-handside of (2.18) and v_{Lo} is written in terms of its inductance and current to obtain (2.19).

$$v_{Lm2} = v_{Lo} - v_{ac} \tag{2.18}$$

$$L_m N \frac{di_{res1}}{dt} + L_m (N)^2 \frac{di_{res2}}{dt} = L_o \frac{di_{res2}}{dt} + v_{ac} \tag{2.19}$$

In order to remove the secondary side current from (2.17), it is clear that (2.19) must be rearranged such that the secondary side current is isolated on one side and all other parameters are separate as seen in (2.20) and (2.21). From here, (2.21) can be substituted back into (2.17) which allows the resonant capacitor voltage in terms of only the primary side current (2.22) to be obtained. This equation can be simplified further into (2.23) by taking the common denominator which allows two terms of the numerator to be cancelled (2.24).

$$\frac{di_{res2}}{dt}\left[L_m (N)^2 - L_o\right] = v_{ac} - L_m N \frac{di_{res1}}{dt} \tag{2.20}$$

$$\frac{di_{res2}}{dt} = \frac{v_{ac} - L_m N \dfrac{di_{res1}}{dt}}{L_m (N)^2 - L_o} \tag{2.21}$$

$$v_{Cr} = v_{s2} - \left(L_m \frac{di_{res1}}{dt} + L_m N \frac{v_{o1} - L_m N \dfrac{di_{res1}}{dt}}{L_m \left(N\right)^2 - L_o} \right) \tag{2.22}$$

$$v_{Cr} = v_{s2} - \left(\frac{{L_m}^2 \left(N\right)^2 \dfrac{di_{res1}}{dt} - L_o L_m \dfrac{di_{res1}}{dt} + L_m N v_{o1} - {L_m}^2 \left(N\right)^2 \dfrac{di_{res1}}{dt}}{L_m \left(N\right)^2 - L_o} \right) \tag{2.23}$$

$$v_{Cr} = v_{s2} - \left(\frac{-L_o L_m \dfrac{di_{res1}}{dt} + L_m N v_{o1}}{L_m \left(N\right)^2 - L_o} \right) \tag{2.24}$$

As the proposed converter utilizes a *CLL* resonant circuit, we can express the equivalent inductance seen by the system in terms of the magnetizing and output inductance, (2.25). This allows (2.24) to be further simplified to (2.26). It can be understood that the resonant capacitor voltage is a function of the switch voltage, the equivalent inductance, the chosen turns-ratio, the rate of change of the resonant current and the resonant output voltage. For simplicity the equation can be rewritten as (2.27) where *V* is provided in (2.28).

$$L_{eq} = \frac{L_o L_m}{L_m \left(\dfrac{n_2}{n_1} \right)^2 + L_o} \tag{2.25}$$

$$v_{Cr} = v_{s2} - \left(-L_{eq} \frac{di_{res1}}{dt} + \frac{L_{eq}}{L_o} \frac{n_2}{n_1} v_{ac} \right) \tag{2.26}$$

$$v_{Cr} = -L_{eq} \frac{di_{res1}}{dt} + V \tag{2.27}$$

$$V = v_{s2} - \frac{L_{eq}}{L_o} \frac{n_2}{n_1} v_{ac} \tag{2.28}$$

Unfortunately, (2.27) is still written in terms of the change in current as a function of time. This parameter is typically not known and will need to be expressed in a different form. One common technique to overcome this issue is Laplace transform. Laplace transform is an integral-based transform that converts a differential equation into algebraic equations. This transform is particularly useful for solving linear ordinary differential equations such as the one presented in (2.27). In this case, we can convert the equation from the time domain (t) to the frequency domain (s).

Two equations will be used for this technique, the first being the resonant capacitor voltage (2.27) and the second will be the resonant current (2.29). Applying Laplace transform to (2.29) results in (2.30), while applying Laplace transform to (2.27) results in (2.31). We can now substitute i_{res}(s) from (2.30) into (2.31) to remove the current component and obtain (2.32). In order to solve for the resonant capacitor voltage we need to isolate the voltage component, v_{cr}(s), on the left-hand side (2.33).

$$i_{res} = C_r \frac{dv_{cr}}{dt} \tag{2.29}$$

$$i_{res}(s) = C_r \left[s v_{cr}(s) - v_{cr}(t_0) \right] \tag{2.30}$$

$$v_{cr}(s) = -L_{eq} \left[s i_{res}(s) - i_{res}(t_0) \right] + \frac{V}{s} \tag{2.31}$$

$$v_{cr}(s) = -L_{eq} \left[s\left(C_r \left[s v_{cr}(s) - v_{cr}(t_0) \right] \right) - i_{res}(t_0) \right] + \frac{V}{s} \tag{2.32}$$

$$v_{cr}(s)\left(1 + s^2 C_r L_{eq}\right) = s C_r L_{eq} v_{cr}(t_0) + L_{eq} i_{res}(t_0) + \frac{V}{s} \tag{2.33}$$

Now inverse Laplace transform can be applied to move from the frequency domain back to the time domain. Before this, it is best to simplify the equation by replacing the equivalent inductance and resonant capacitance with the resonant frequency ω_o (2.34).

$$L_{eq} C_r = \frac{1}{\omega_o^{\,2}} \tag{2.34}$$

Substituting (2.34) into (2.33) results in (2.35) which can then be rearranged such that the resonant capacitor voltage is on one side of the equation (2.36).

$$v_{cr}(s)\left(\frac{\omega_o^{\,2}+s^2}{\omega_o^{\,2}}\right)=\left(\frac{s}{\omega_o^{\,2}}\right)v_{cr}(t_0)+\frac{1}{c_r\omega_o^{\,2}}i_{res}(t_0)+\frac{V}{s} \tag{2.35}$$

$$v_{cr}(s)=\left(\frac{s}{\omega_o^{\,2}+s^2}\right)v_{cr}(t_0)+\left(\frac{1}{\omega_o^{\,2}+s^2}\right)\frac{i_{res}(t_0)}{c_r}+\frac{V}{s}\left(\frac{\omega_o^{\,2}}{\omega_o^{\,2}+s^2}\right) \tag{2.36}$$

From here, inverse Laplace transform can be applied to obtain the resonant capacitor voltage equation (2.37) where $v_{cr}(t_0)$ is the initial capacitor voltage, $i_{res}(t_0)$ is the initial capacitor current, and Z is the characteristic impedance given in (2.38).

$$v_{cr}=v_{cr}(t_0)\cos(\omega_o t)+i_{res}(t_0)Z\sin(\omega_o t)+V\left(1-\cos(\omega_o t)\right) \tag{2.37}$$

$$Z=\sqrt{\frac{L_{eq}}{C_r}}=\frac{1}{\omega_o C_r} \tag{2.38}$$

2.1.2.5 Resonant Capacitor Current

In 2.1.2.4, Laplace transform was used to solve for the resonant capacitor voltage. This technique can also be applied to solve for the resonant capacitor current. Instead of substituting (2.30) into (2.31), the reverse can be done to obtain (2.39).

$$i_{res}(s)=C_r\left[s\left(-L_{eq}\left[si_{res}(s)-i_{res}(t_0)\right]+\frac{V}{s}\right)-v_{cr}(t_0)\right] \tag{2.39}$$

From here the same method to simplify the equation (2.40) and to convert back to time domain can be applied (2.41).

$$i_{res}(s)=\frac{s}{\omega_o^{\,2}+s^2}i_{res}(t_0)+C_r\left(V-v_{cr}(t_0)\right)\left(\frac{\omega_o^{\,2}}{\omega_o^{\,2}+s^2}\right) \tag{2.40}$$

$$i_{res}=i_{res}(t_0)\cos(\omega_o t)+\frac{V-v_{cr}(t_0)}{Z}\sin(\omega_o t) \tag{2.41}$$

2.1.2.6 Voltage Quadrupler

The output voltage of the resonant stage forms the input to the voltage quadupler. This stage rectifies the AC input waveform and as a result the output voltage is DC as shown in Figure 2-4. From the operating principles discussed in section 2.1.1.2, it is understood that the voltage across the Co_1 is equal to the peak of the AC input waveform, (2.42), while the voltage across the Co_2 is equal to the trough of the AC input waveform, (2.43).

$$v_{Co1} = v_{ac\_\max} \tag{2.42}$$

$$v_{Co2} = v_{ac\_\min} \tag{2.43}$$

Figure 2-5 and Figure 2-6 make it evident that the output capacitor voltages are half that of the total output voltage and equal to the summation of the two input capacitors (2.44).

$$v_{Co3} = v_{Co4} = v_{Co1} + v_{Co2} = \frac{v_o}{2} \tag{2.44}$$

The voltage stress across the VQ diodes can also be obtained through a similar circuit analysis. In the positive half-cycle shown in Figure 2-5 it can be seen that when diode D_{R1} is inactive, D_{R2} is active and results in D_{R1} being in parallel with the output capacitor Co_3 (2.45). The same occurs with D_{R3} and Co_4 due to D_{R4} being active (2.46)

$$v_{DR1} = v_{co3} \tag{2.45}$$

$$v_{DR3} = v_{co4} \tag{2.46}$$

In the negative half-cycle shown in Figure 2-6 it can be seen that when diode D_{R2} is inactive, D_{R1} is active and results in D_{R2} being in parallel with the output capacitor Co_3. The same occurs with D_{R4} and Co_4 due to D_{R3} being active. It should be noted that since the voltage across Co_3 and Co_4 are balanced, the voltage stress across all four of the VQ diodes are equal.

2.1.2.7 Voltage Gain

The total voltage gain of proposed converter is a combination of the integrated boost stage, the APWM resonant circuit stage, and the voltage quadrupler. This relationship can be obtained by as follows. First of all, the output voltage of the boost stage which was provided in (2.7) forms the input to the *CLL* resonant stage which alternates between its maximum value and zero based on whether switch S_2 is on or off. This voltage waveform can be obtained by applying the fundamental harmonic approximation (FHA) which can then be simplified as shown in (2.9). Figure 2-9(a) provides an example of the converter from the resonant stage to the output. To analyze this converter, by assuming the converter is connected to an infinite voltage source at the output, it is recommended to replace the VQ with an equivalent resistance (2.47) which simplifies the converter to the version shown in Figure 2-9(b). From here, the secondary side components are reflected onto the primary side as shown in Figure 2-9(c).

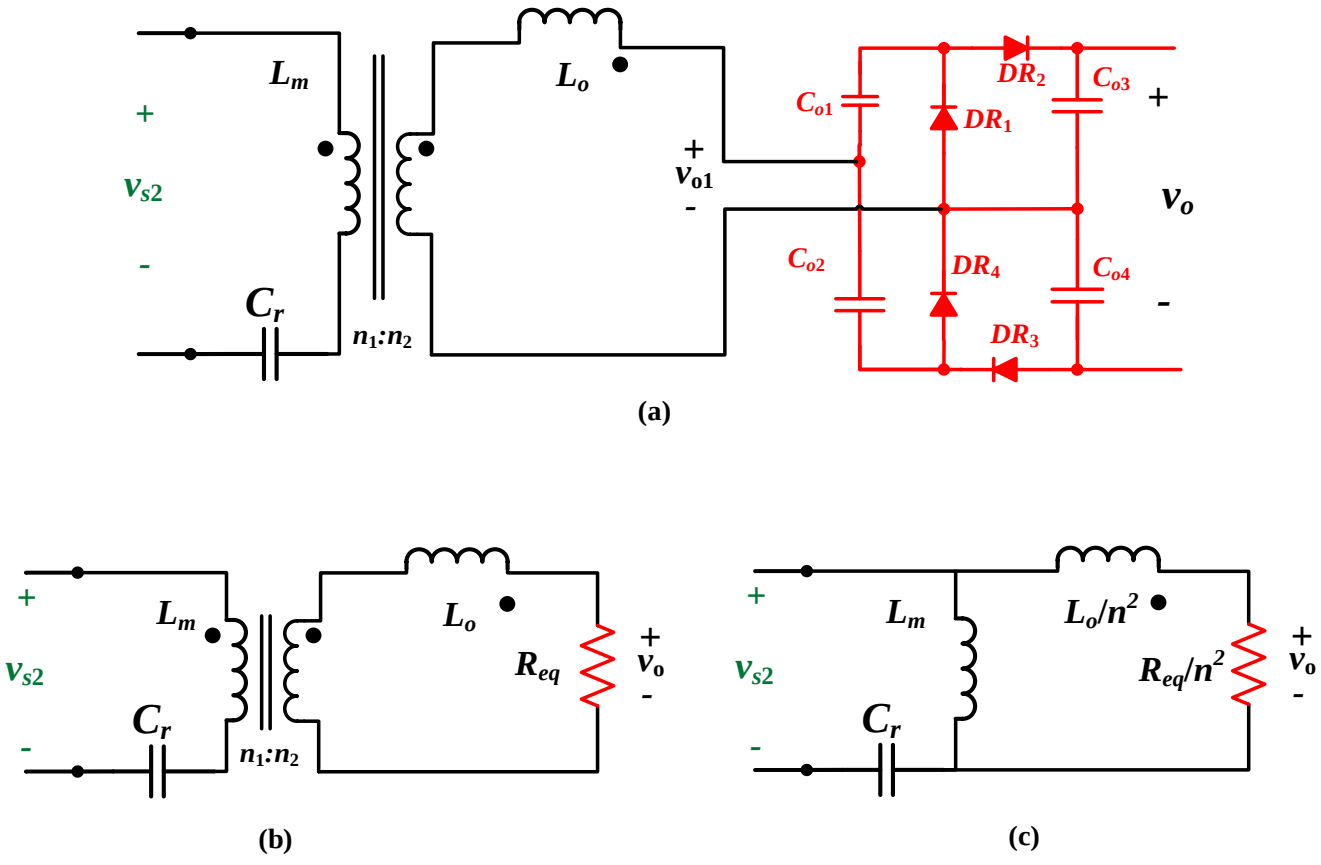


Figure 2-9 Topology of the (a) *CLL* resonant circuit with VQ (b) *CLL* resonant circuit with VQ represented as an equivalent resistance, (c) *CLL* resonant circuit referred to the primary side

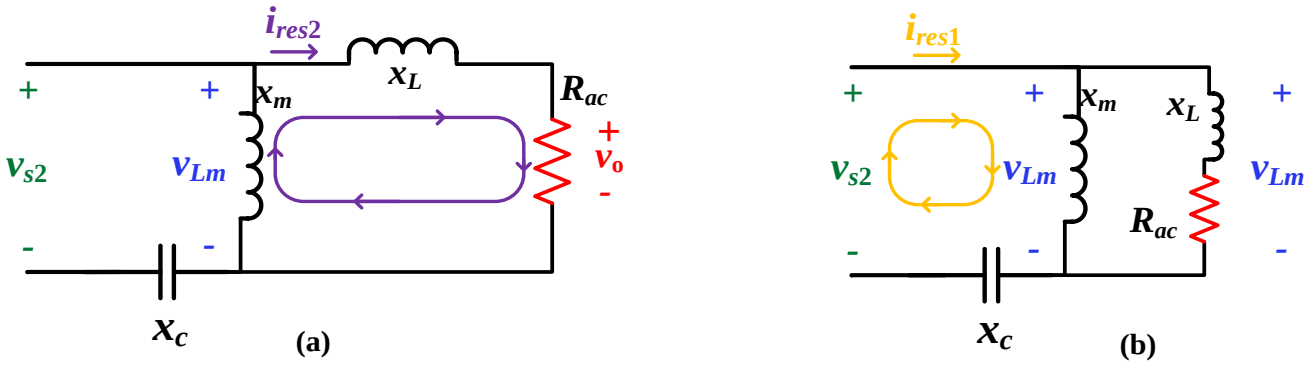


Figure 2-10 Loops for (a) secondary side resonant current i_{res2} (b) primary side resonant current i_{res1}

$$R_{eq} = \frac{2}{\pi^2} R \tag{2.47}$$

$$R_{ac} = \frac{R_{eq}}{n^2} = \frac{2}{(n\pi)^2} R \tag{2.48}$$

From here, basic circuit theory can be applied to derive the ratio between the output and input voltage of the resonant stage. This is done by analyzing two loops seen in Figure 2-10 to obtain voltage equations (2.49) and (2.50) where x_m, x_o, and x_c, are provided in equations (2.51) to (2.53) respectively.

$$\frac{v_{o1}}{v_{Lm}} = \frac{R_{ac}}{R_{ac} + x_o} \tag{2.49}$$

$$\frac{v_{Lm}}{v_{s2}} = \frac{x_m \| (R_{ac} + x_o)}{x_m \| (R_{ac} + x_o) + x_c} = \frac{1}{1 + \frac{x_c}{x_m \| (R_{ac} + x_o)}} = \frac{x_m (R_{ac} + x_o)}{x_m (R_{ac} + x_o) + x_m x_c + x_o x_c + R_{ac} x_c} \tag{2.50}$$

$$x_m = sL_m = j\omega L_m \tag{2.51}$$

$$x_o = \frac{sL_o}{n^2} = j\omega \frac{L_o}{n^2} \tag{2.52}$$

$$x_c = \frac{1}{sC_r} = \frac{1}{j\omega C_r} \tag{2.53}$$

The end goal is to obtain the ratio between the input and output voltage, therefore equations (2.49) and (2.50) are multiplied together to obtain (2.54) which can be simplified to (2.55). From here the equation is reconfigured to set the numerator equal to 1 (2.56).

$$\frac{v_{o1}}{v_{s2}} = \frac{v_{Lm}}{v_{s2}}\frac{v_{o1}}{v_{Lm}} = \frac{x_m\left(R_{ac}+x_o\right)}{x_m\left(R_{ac}+x_o\right)+x_m x_c + x_o x_c + R_{ac}x_c} \times \frac{R_{ac}}{\left(R_{ac}+x_o\right)} \tag{2.54}$$

$$\frac{v_{o1}}{v_{s2}} = \frac{x_m R_{ac}}{x_m\left(R_{ac}+x_o\right)+x_m x_c + x_o x_c + R_{ac}x_c} \tag{2.55}$$

$$\frac{v_{o1}}{v_{s2}} = \frac{1}{1+\frac{x_c}{x_m}+\frac{x_c}{R_{ac}}+\frac{x_o}{x_m}\left(\frac{x_m+x_c}{R_{ac}}\right)} \tag{2.56}$$

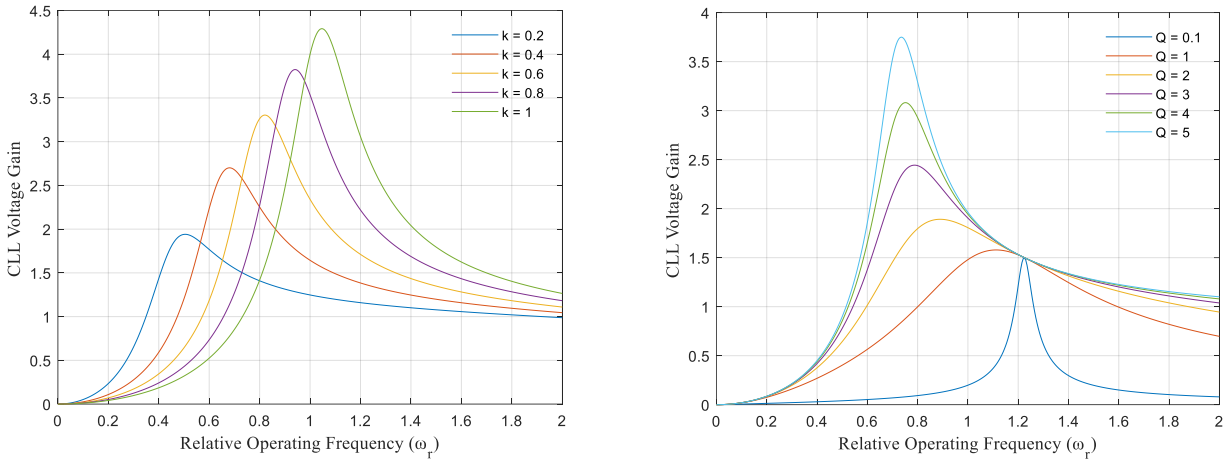
This equation does not provide useful information it is current form, so equations (2.51) to (2.53) are substituted to obtain (2.57). From here, the denominator is rearranged to isolate the real and imaginary components (2.58) and then simplified (2.59).

$$\frac{v_{o1}}{v_{s2}} = \frac{1}{1-\frac{1}{\omega^2 L_m C_r}+\frac{1}{j\omega C_r R_{ac}}+\frac{L_o}{L_m n^2}\left(\frac{j\omega L_m+\frac{1}{j\omega C_r}}{R_{ac}}\right)} \tag{2.57}$$

$$\frac{v_{o1}}{v_{s2}} = \frac{1}{\left(1-\frac{1}{\omega^2 L_m C_r}\right)-j\left(\frac{L_s}{L_m n^2}\left(\frac{\frac{1}{\omega C_r}-\omega L_m}{R_{ac}}\right)+\frac{1}{\omega C_r R_{ac}}\right)} \tag{2.58}$$

$$\frac{v_{o1}}{v_{s2}} = \frac{1}{\left(1-\frac{1}{\omega^2 L_m C_r}\right)-j\left(\frac{L_s}{L_m n^2}\left(\frac{1-\omega^2 L_m C_r}{\omega C_r R_{ac}}\right)+\frac{1}{\omega C_r R_{ac}}\right)} \tag{2.59}$$

In order to further simplify the equation to achieve (2.60), the denominator parameters are substituted with additional variables which are both the operating and relative operating frequency



(a) (b)

Figure 2-11: CLL voltage gain of proposed converter as a function of relative operating frequency for (a) varying quality factor (Q), (b) varying inductance ratio (k).

ω_o and ω_n (2.61), the quality factor Q (2.62), and the inductance ratio k (2.63). From here we can obtain the gain of the resonant stage (2.64).

$$\frac{v_{o1}}{v_{s2}} = \frac{1}{\left(1-\frac{k}{\omega_n^{\,2}\left(k+1\right)}\right) - j\left(\frac{Q}{\omega_n}\left(1+k-\omega_n^{\,2}\left(k+1\right)\right)\right)} \tag{2.60}$$

$$\omega = \omega_o \times \omega_n \tag{2.61}$$

$$Q = \frac{\omega_o \times L_{eq}}{R_{ac}} \tag{2.62}$$

$$k = \frac{L_o \times n^2}{L_m} \tag{2.63}$$

$$\left|\frac{v_{o1}}{v_{s2}}\right| = \frac{1}{\sqrt{\left(1-\frac{k}{\omega_n^{\,2}\left(k+1\right)}\right)^2 + \left(\frac{Q}{\omega_n}\left(1+k-\omega_n^{\,2}\left(k+1\right)\right)\right)^2}} \tag{2.64}$$

A plot of the voltage gain as a function of the relative operating frequency and the quality factor is provided in Figure 2-11(a). The voltage gain plot as a function of the relative operating frequency and the ratio between the magnetizing and output inductor is provided in Figure 2-11(b).

2.2 Single-sensor Maximum Power Extraction

The previous section of this chapter discussed a high step-up DC-DC converter for PV energy applications. In order for the system to achieve maximum power operation, a voltage and current sensor could be used to obtain the operating characteristics of the panel. However, as stated before, multiple sensors including current sensors increases the size and cost of the system while adding additional uncertainties and noise which can have a negative impact on the overall system operation. To overcome this issue, a single-sensor, current-sensorless maximum power extraction technique is presented in this section. The proposed extraction technique operates by tracking the condition of a separate voltage parameter whose characteristics follows that of the input power and aims to maximize this parameter. Through maximizing this parameter, the input PV power is indirectly maximized.

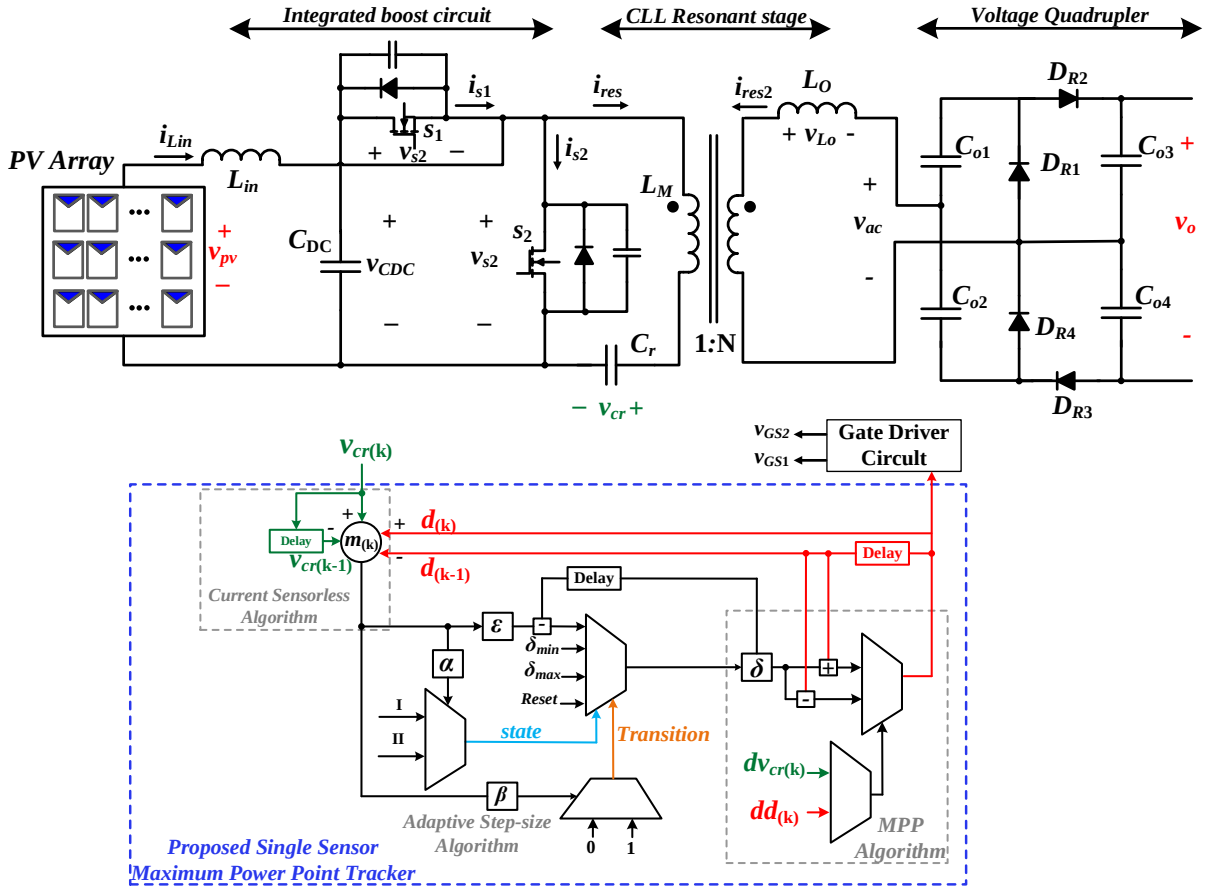


Figure 2-12: Proposed single-sensor current-sensorless MPPT control scheme together with the developed converter

2.2.1 Measured Parameter

Voltage sensing can easily be performed with a voltage divider, which results in minimal cost and losses compared with other sensors such as current, temperature, or light intensity, which makes it a good choice for single sensor implementations. However, it is not possible to perform MPP tracking only by measuring the panel's output voltage unless the algorithm is designed for a specific power converter. As a result, to perform MPP tracking with only a voltage sensor, an alternate voltage parameter must be measured. In some converters, such as the discussed APWM *CLL* resonant converter, there are voltage parameters that meet this criterion.

The resonant capacitor voltage for the proposed converter was previously given in (2.37). By modifying this equation, it can be seen that the resonant capacitor voltage is a function of the input power (2.65). The scenario at which the peak resonant capacitor voltage occurs varies based on the chosen resonant parameters and the coupled inductor turns-ratio, however in all scenarios the peak resonant capacitor value can be simplified to (2.66) where α is a constant parameter consisting of the peak switch voltage, resonant components, and initial condition values (2.67). For v_{cr} to be maximized at any condition the cosine parameter must be at its max which is 1. Therefore, if the resonant capacitor voltage is sensed, it would be essentially the same as measuring a scaled and shifted version of the input power. When a PV panel is connected to the input of the proposed converter, varying the duty-ratio varies panel voltage and in turn the operating power. From this it is understood that if the duty-ratio of the proposed converter is varied to maximize v_{cr}, the input power will be indirectly maximized.

$$v_{Cr} = v_{s2} + \frac{v_{s2} - v_{Cr(0)} + \dfrac{P \times R \times \dfrac{n_2}{n_1}}{2L_o}}{\omega_0 Z}\cos(\omega_0 t) - \frac{i_{res(0)}}{\omega_0}\sin(\omega_0 t) + \frac{P \times R \times \dfrac{n_2}{n_1} \times L_{eq}}{L_o} \tag{2.65}$$

$$v_{Cr_{\max}} = P\left(\frac{R\dfrac{n_2}{n_1}\left(1 + 2L_{eq}\omega_0 Z\right)}{2L_o\omega_0 Z}\right) + \alpha \tag{2.66}$$

$$\alpha = v_{s2} + \frac{v_{s2} - v_{Cr(0)}}{\omega_0 Z} \tag{2.67}$$

At the same time, the voltage across the resonant inductor is related to the resonant capacitor and switch voltage. This relation is provided in (2.68) for when the switch is off and on respectively.

$$v_{Lm} = \begin{cases} -v_{cr}, & S_2 \text{ is on} \\ v_{s2} - v_{cr}, & S_2 \text{ is off} \end{cases} \tag{2.68}$$

The peak resonant capacitor voltage occurs when the resonant current transitions from positive to negative which based on Figure 2-2 occurs during the period when switch S_2 transitions from on to off. Therefore, the minimum inductor voltage is equal to the peak resonant capacitor voltage and can be used as a substitute signal for the input power. Although both duty ratio or frequency control can be applied to the proposed converter for maximum power extraction, in this dissertation, duty ratio control is employed as it has a lower impact on the *CLL* converter gain (2.64) and soft-switching operation compared to frequency control. As a result, with duty ratio control, the proposed converter is able to achieve both maximum power extraction and a high step-up gain while maintaining soft-switching at all conditions.

2.2.2 Voltage Sensing

To implement the voltage sensor, a resistive bridge is required. The proposed current-sensorless algorithm would be implemented on a hardware controller such as a digital signal processing (DSP) controller. To correctly sense the voltage, it is expected that the ground of the sensor is connected to the ground of the DSP board, however to control the gate signals the DSP controller must be connected to the converter ground. As a result, the optimal configuration is to place have one node of the resonant capacitor connected to ground. In Figure 1-8(c), it can be seen that the *CLL* resonant capacitor is not connected to ground, however due to the series connection, this capacitor can easily be moved to the bottom of the circuit as shown in Figure 2-12.This allows for only a simple voltage divider to be used to safely sense the voltage and send it to DSP controller

The proposed controller requires the peak value of the resonant capacitor voltage, however the above discussion would sense the entire voltage waveform. The peak voltage can be easily obtained by sampling the measured voltage. Most commercially available controllers operate in the range of megahertz (MHz) such as the TMSF28335 DSP controllers that operates at 150MHz The controller's analog-to-digital converter (ADC) can be set to sample at 25MHz, which allows for 250 samples per cycle if the converter operates at 100 kilohertz (kHz). From here it is understood that the peak resonant capacitor voltage can reasonably be obtained by sampling the required measurement and storing the maximum value per cycle.

2.2.3 Adaptive Tracking and Ripple Minimization

The previously discussed single-sensor algorithm can function with a P&O based algorithm. However, it would be more efficient to implement an intelligent adaptive step-size algorithm as they can provide faster tracking speed and lower oscillations near the MPP. Gradient based methods can be employed for adaptive step-size as they utilize the change in the measured parameter and the operating state. The benefit of this implementation for the developed single-sensor MPPT is that additional sensors are not required. The proposed algorithm senses the peak resonant capacitor voltage and compares it to the previous iteration. From here the algorithm takes the previous duty-ratio and perturbs it towards the MPP. Therefore, the proposed algorithm already has the required information necessary to calculate the resonant capacitor voltage rate of change as a function of the duty-ratio change. This technique would help to increase the tracking speed during periods when the operating conditions change, which leads to a more stable system and higher overall extraction efficiency.

A flowchart of the proposed algorithm is shown in Figure 2-13. There are two states in which the algorithm operates in. State I is the tracking state and occurs when the system is not operating near the MPP while in the process of approaching it. State II is known as ripple minimization state and occurs when the system is operating close to or at the MPP. The controller transitions between states based on the gradient value.

2.2.3.1 State I: MPP Tracking

During each iteration (k), the controller senses the peak operating voltage of the desired component and along with the previous operating state determines the rate of change. When operating away from the MPP, the rate of change is large. The controller utilizes this large value to tune the step-size as shown in (2.69)

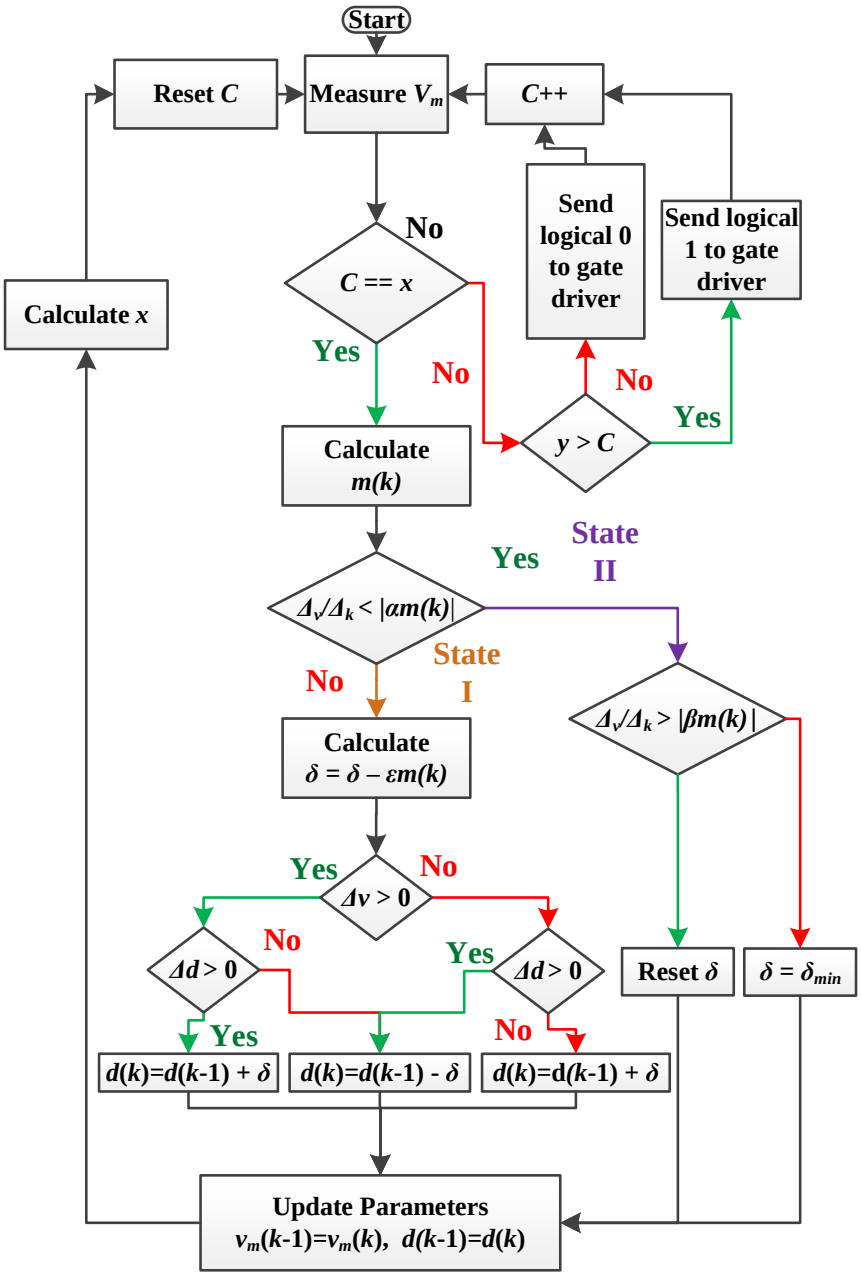


Figure 2-13: Flowchart of the proposed single-sensor current-sensorless MPPT controller

$$y_{(k)} = y_{(k-1)} - \frac{v_{(k)} - v_{(k-1)}}{d_{(k)} - d_{(k-1)}} \varepsilon_v \tag{2.69}$$

where $y_{(k\text{-}1)}$ and $y_{(k)}$ are the previous iteration and the new step-size, $d_{(k\text{-}1)}$ and $d_{(k)}$ are the previous iteration and current iteration duty-ratio, ε_v is the scaling factor chosen by the designer and $v_{(k\text{-}1)}$ and $v_{(k)}$ are the previous iteration and current iteration sensed voltage. This allow for faster tracking compared to the standard P&O algorithm. As the operating parameter is perturbed, the rate of change decreases, and in turn the step-size decreases. If the rate of change is much smaller than the measured peak as indicated in (2.70), the controller transitions to the second state which is oscillation minimization.

$$\frac{v_{(k)} - v_{(k-1)}}{d_{(k)} - d_{(k-1)}} \leq \beta \times v_{(k)} \tag{2.70}$$

2.2.3.2 State II: Ripple minimization

During State II the step-size is significantly reduced to allow for minimal oscillation around the MPP. This is determined based on the gradient as shown in (2.70). If this condition is satisfied, it implies the system is operating very close to the MPP and the step-size can be decreased to reduce the chance of overshoot. While operating in this state, if there is a change in the light intensity the calculated rate of change would be large according to (2.71), which alerts the controller to transition back to State I.

$$\frac{v_{cr_{max}(k)} - v_{cr_{max}(k-1)}}{d_{(k)} - d_{(k-1)}} \geq \gamma \times v_{cr_{max}(k)} \tag{2.71}$$

2.2.4 Single-Sensor Tracking Stability

The proposed algorithm operates with simple comparisons and updates the step-size based on the rate of change. Therefore, the controller can be shown to be stable as it will always converge at the MPP. Figure 2-14 shows four tracking scenarios while the system is not operating at the MPP. The x-axis of each graph represents the operating duty ratio where $d_{\min}$ and $d_{\max}$ are the implemented duty ratio limits which are chosen such the system maintains soft-switching condition. The y-axis represents the measured voltage labelled as v_m.

Figure 2-14(a) shows the ideal situation, in which the system arrives at the MPP without an overshoot. Figure 2-14(b) shows the second scenario which is when the system overshot the MPP and arrived at a location where the calculated rate of change is close to zero. However, the system does not transition into State II as the change in the perturbed variable, which in Figure 2-14 is the duty ratio, is high. This alerts the controller that the MPP was overshot and that the operating side has changed. The third scenario is shown in Figure 2-14(c) which is when the perturbation

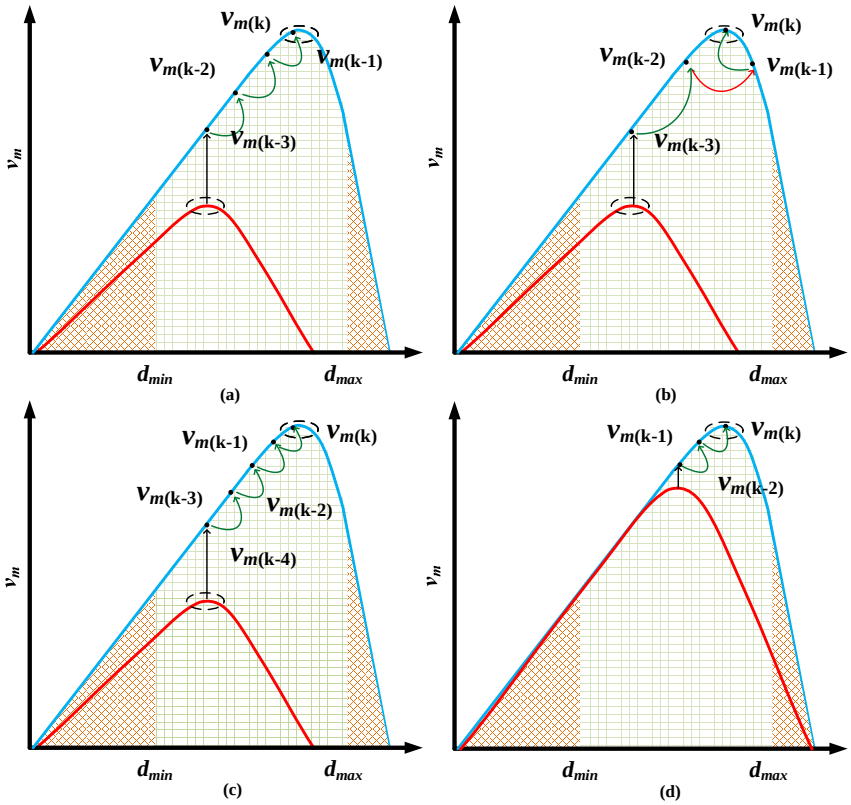


Figure 2-14 Four possible tracking scenarios during operation of the proposed controller

parameter approaches zero. As with the previous scenario, the measured rate of change would be close to zero, however the change in the perturbed variable would also be zero. For the proposed algorithm, this scenario will always be avoided by ensuring that the controller operates with a minimum step-size, such that the rate of change will only be close to zero when operating very close to the MPP. Based on the change of slope, the controller can determine the operating side of the system. In Figure 2-14(a) when the intensity changed from low to high the controller would measure a positive slope, implying the system is operating to the left of the MPP. If the controller measured a negative slope it would imply that the intensity changed from high to low and the system is operating to the right of the MPP. Therefore, the controller knows the initial perturbation direction to approach the new MPP location.

2.3 Simulation Results

In order to verify the operation of the developed high-gain DC/DC converter, simulation was preformed using the circuit simulation software PowerSim (PSIM). The developed converter was tested with PV arrays connected to its input. It was assumed that three 45V, 5.3A panels were utilized in series to obtain an open circuit voltage of 150V and a short circuit current of 5A. The duty-ratio of the converter was controlled in an open-loop fashion as the goal is to first confirm the converters operation. Figure 2-15(a) shows the converter's input switch voltage waveforms while the switch current waveforms are shown in Figure 2-15(b). The peak voltage across both switches are seen to be equal, which is expected as when the switches are off their positive node (drain) is connected to the DC-link capacitor and their negative node (source) is connected to ground as mentioned in (2.7). With an input voltage of 133V and an operating duty-ratio of 63%, the peak switch voltage should be approximately 359V which closely matches the simulation results of 357V. The switches are confirmed to operate with soft-switching as the during the period where the switch currents in Figure 2-15(b) transition from negative to positive, the respective switch voltage is zero. Figure 2-15(c) shows the input current waveform which can be seen to operate in continuous conduction mode (CCM) as the minimum input current value is greater than zero. The current through switch S_2 is also included to confirm the operating condition is the same as in Figure 2-15 (b).

The input and output voltage of the resonant circuit is shown in Figure 2-16. The input to the resonant circuit is the same as the voltage across switch S_2 as previous shown in Figure 2-8(a). The resonant capacitor voltage is shown in Figure 2-16 (b) and it can be seen that location of the maximum and minimum voltage occurs at the same location where the resonant output voltage transitions from negative to positive.

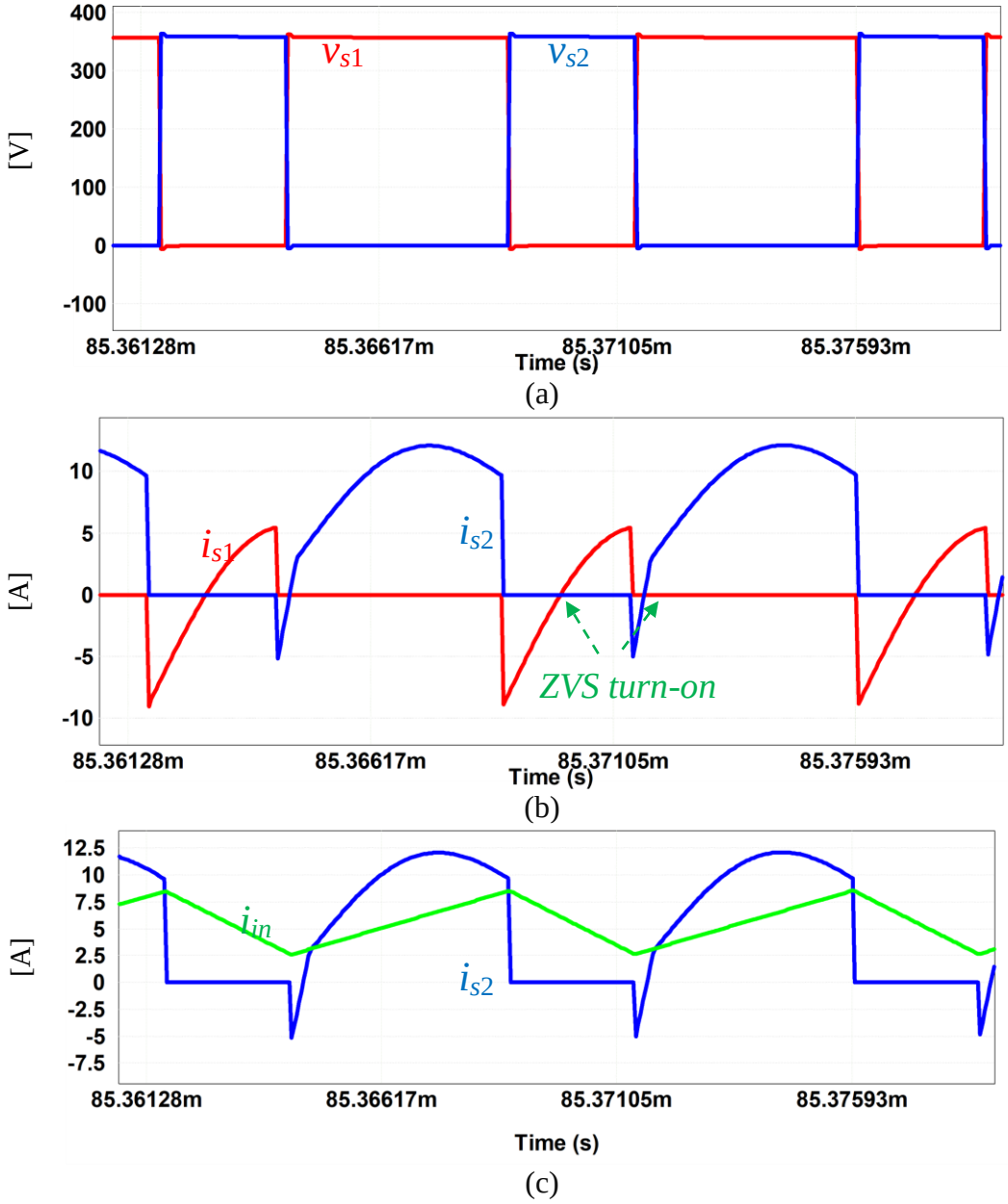
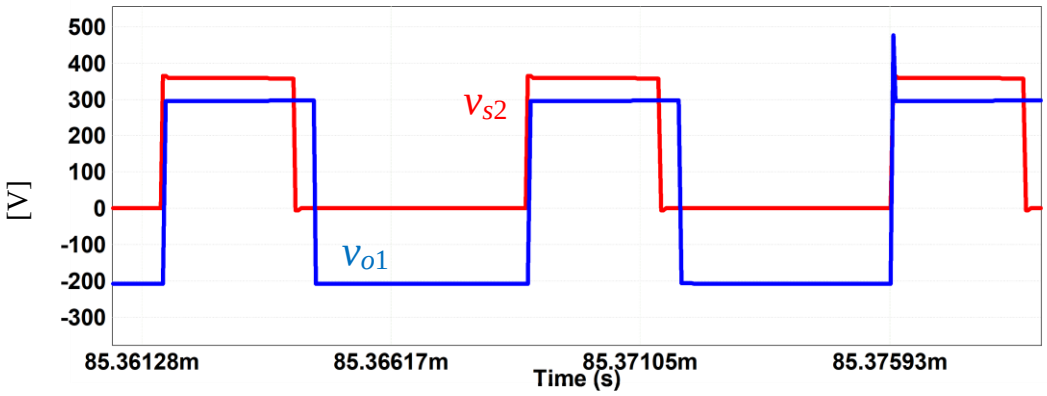
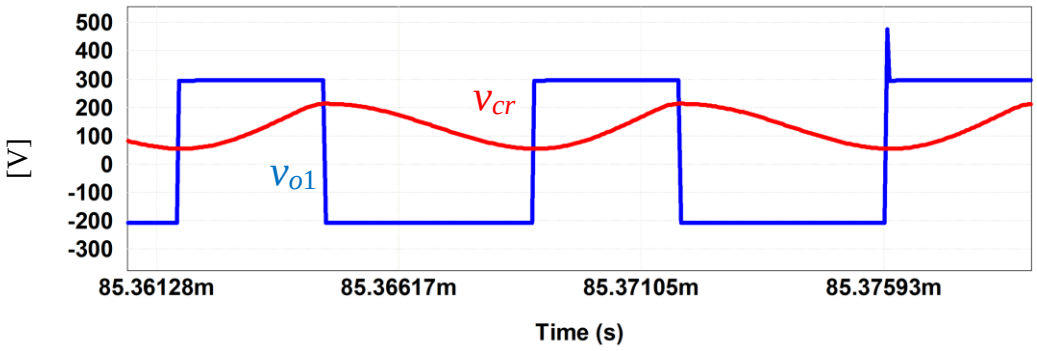


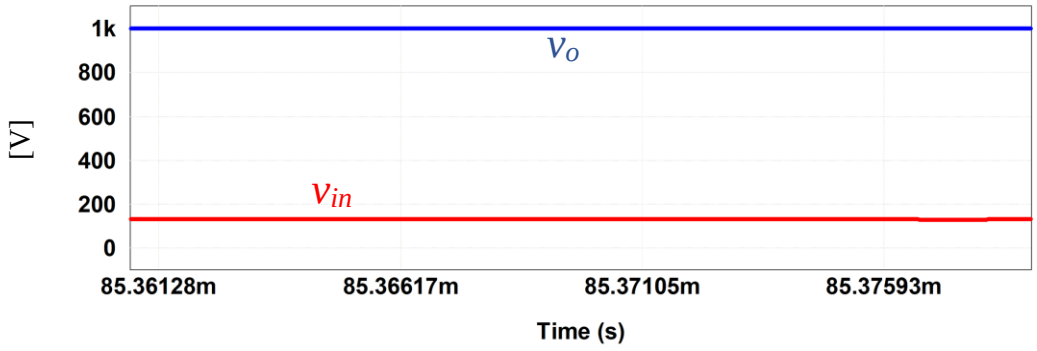
Figure 2-15 Converter Operating Waveforms (a) Input switch voltage (b) Input switch currents, (c) Input switch and inductor current



(a)



(b)



(c)

Figure 2-16: Converter operating waveforms (a) input switch voltage S_2 and resonant output voltage, (b) resonant output voltage and resonant capacitor voltage, (c) input and output voltage

Table 2-1 Simulation and Prototype Parameters

	Simulation Parameters	**Hardware Parameters**
Input Inductance	100µH	43µH
Magnetizing Inductance	490µH	490µH
Output Inductance	47µH	47µH
Input Capacitance	10µF	5µF
Resonant Capacitance	100nF	100nF
Output Capacitance	10µF x4	5µF x4
MOSFET Switch	SCT3030AW7TL	SCT3030AW7TL
Power Diode	MURS360BT3G	MURS360BT3G
Output Voltage	400V	400V
Converter Gain Range	4-5	4-5
	PV Panel Parameters	PV Emulator Parameters
Maximum Power Level	240W	200W
Voltage at Maximum Power	44V	85V
Current at Maximum Power	5.5A	2.4A
Open Circuit Voltage	50V	90V
Short Circuit Current	5.7A	2.5A
	PSIM Controller Parameters	Prototype DSP Parameters
Digital Signal Processing Board	-	TMSF28335
System Operating Frequency	120kHz	120kHz
System Duty-Ratio Range	30% - 80%	30% - 80%
Sampling Frequency	-	25MHz

In order to verify the accuracy of the proposed single-sensor MPP tracking algorithm, the designed controller was implemented in the circuit simulation software PSIM together with the DC-DC converter discussed in Figure 2-1. Table 2-1 shows the components used in the simulation. A maximum operating power of 200W was set for the PV array with an MPP voltage and current of 43V and 5.5A respectively. The open circuit voltage and short circuit current were 50V and 5.7A respectively. The converter was operated at 120kHz with a duty-ratio range between 30% and 80%.

To confirm that the proposed converter's resonant capacitor voltage followed the characteristics of the input PV panel, the duty-ratio of the converter's switches was manually varied from 30% to 80%. Figure 2-17 shows a plot of both the panels operating power (a) and the peak resonant capacitor voltage (b) when the operating intensity of the panel ranged from 700W/m^2 to 1000W/m^2. It can be seen that the peak resonant capacitor voltage occurs at approximately the same duty-ratio that results in the peak operating power at all conditions. This confirms that by

varying the duty-ratio to maximize the resonant capacitor voltage the input power is maximized indirectly. The small x-axis offset can be reasonably accounted for due to the delay in the simulation wattmeter measurement signal.

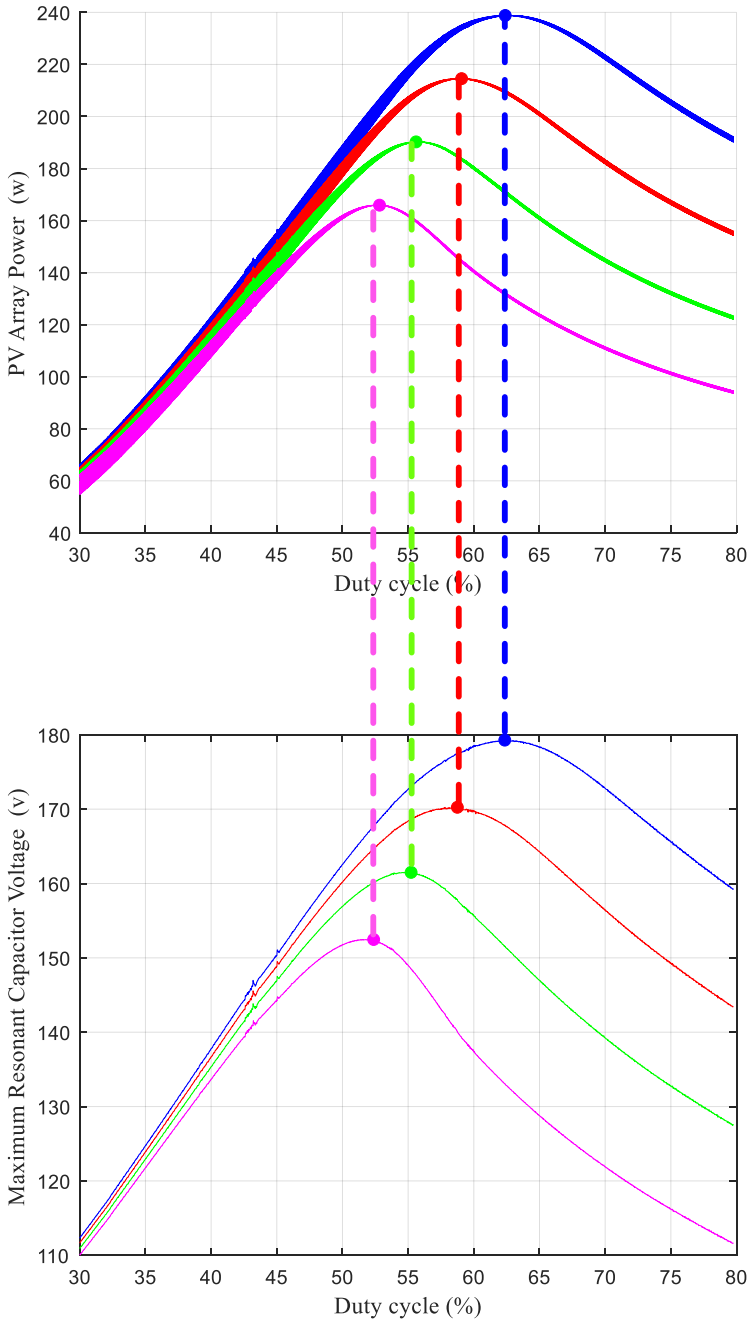


Figure 2-17: (a) PV Array Operating power (b) Maximum resonant capacitor voltage as a function of the converters operating duty-ratio

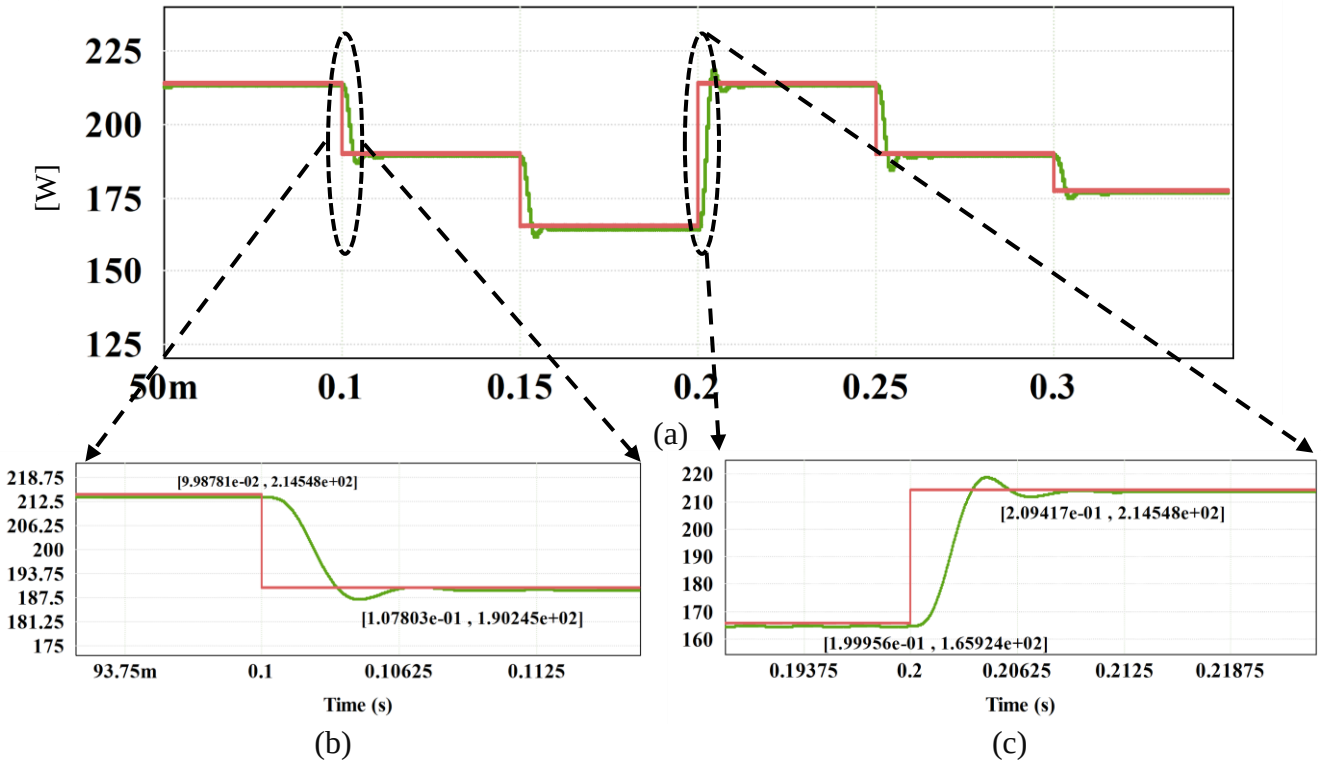


Figure 2-18: (a) Theoretical and operating PV array power, power level transition from (b) high to low, (c) low to high

Figure 2-18 shows the converter waveforms when the light intensity of the input panel varied between 600W/m^2 and 900W/m^2 every 50ms. The discussed single-sensor maximum power extraction algorithm was employed to automatically vary the duty-ratio of both switches to ensure maximum power operation while staying within the duty-ratio limit. Figure 2-18(a) shows that the controller was successful in bringing the operating state to the maximum power at all operating conditions. Further, Figure 2-18(b) and (c) show that the oscillations around the MPP were minimized leading to an extraction efficiency of 99.4% implying the adaptive step-size and ripple mitigation portion of the proposed algorithm was functional. This confirms that by using a surrogate signal to indirectly track the MPP, the accuracy and power extraction has been enhanced. The output voltage, switch voltage and current are given in Figure 2-18(d) and (e) along with a zoom-in. The proposed converter maintained soft-switching at all operation conditions while the MPP algorithm was varying the converters duty-ratio. It can also be seen that the peak voltage of the switches were approximately four times less than the output voltage, showing that the converter can achieve a large step-up gain without the need of high rated components.

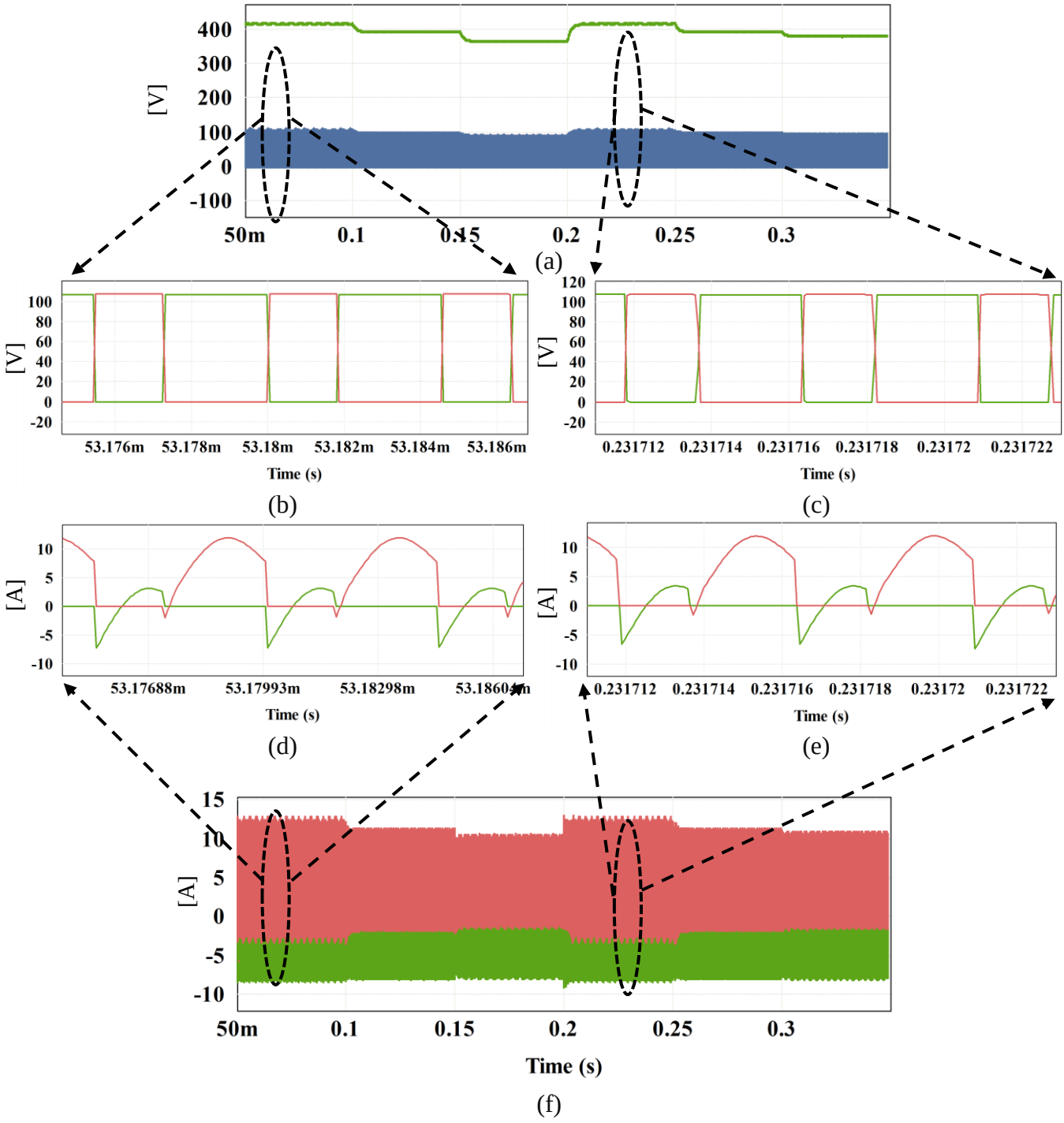
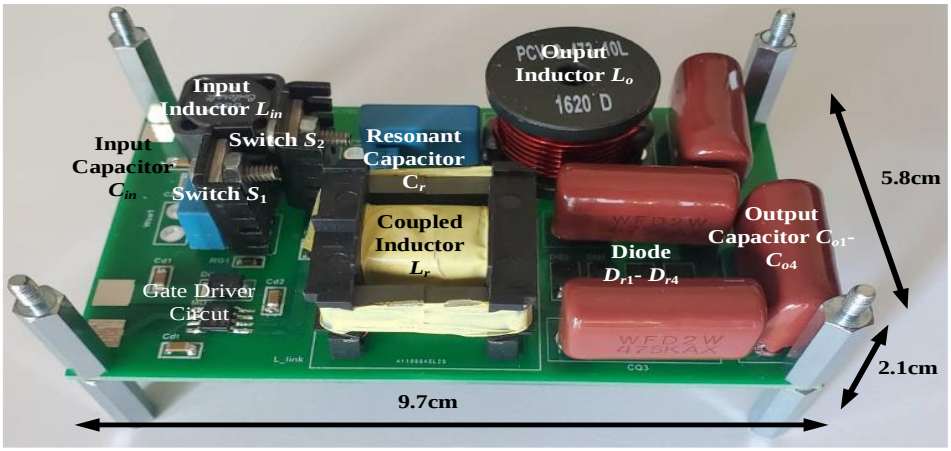


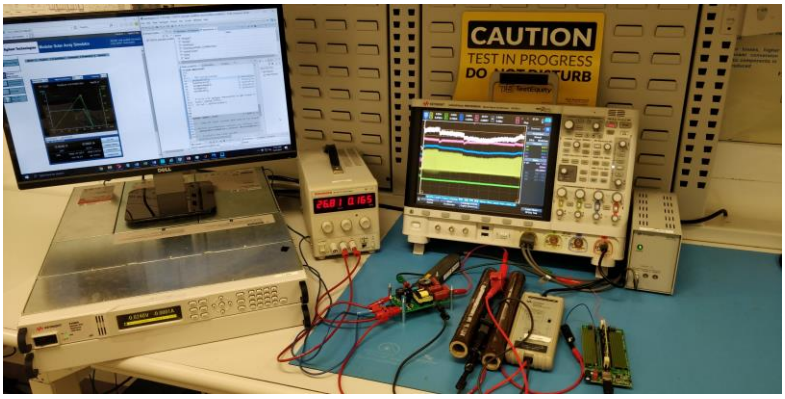
Figure 2-19: (a) switch voltage and output voltage, (b) zoom-in of switch voltage (c) zoom-in of switch voltage (d) zoom-in of switch current (e) zoom-in of switch current (f) switch current

2.4 Experimental Results

To further verify the operation of the proposed single-sensor current-sensorless MPPT controller, a scaled-down proof-of-concept hardware prototype of the converter discussed in section 2.1 was designed. This prototype is shown in Figure 2-20(a) with the input switches located at the top left while the AVQ diodes and capacitors are located at the bottom right. The dimensions of the prototype were 9.7cm x 2.1cm x 5.8cm. An E4360A Modular Solar Array Simulator (SAS)



(a)



(b)

Figure 2-20: (a) picture of hardware prototype (b) experimental setup

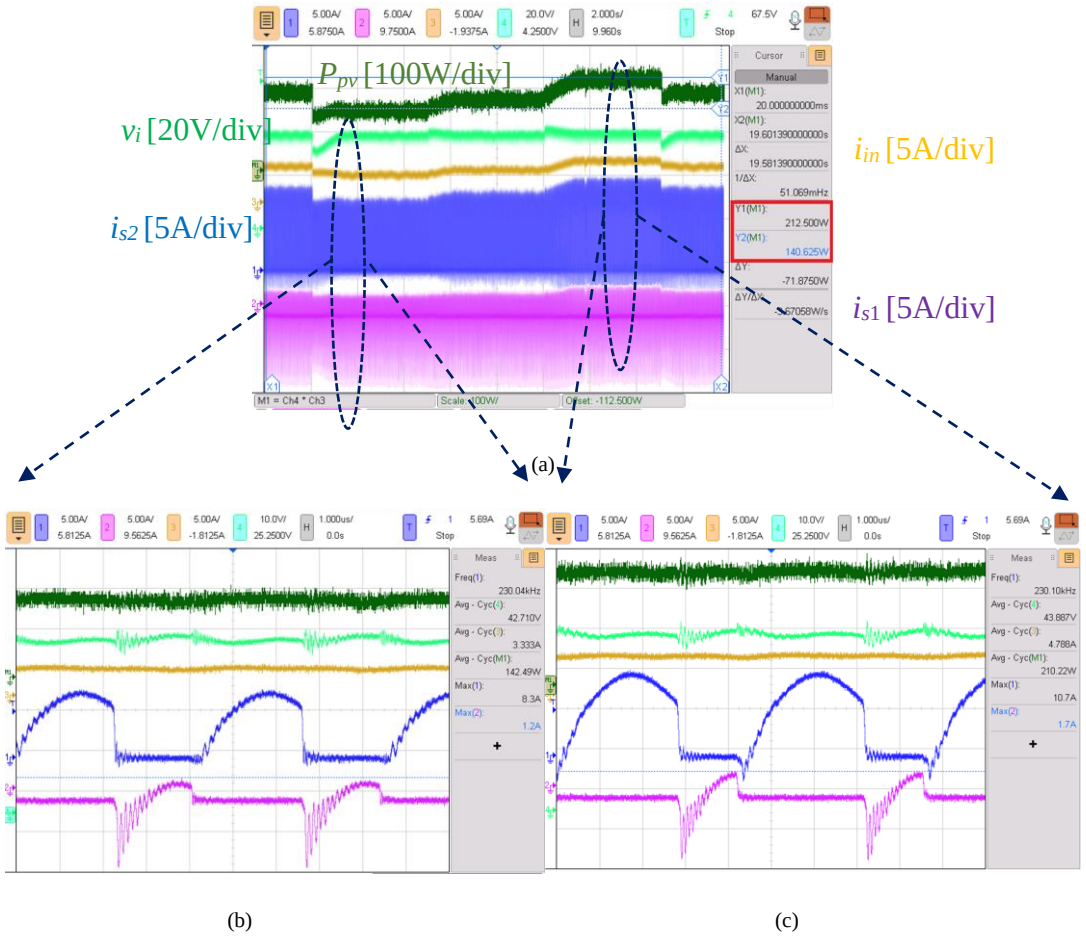


Figure 2-21: experimental waveforms with the light intensity varying every five secs: (a) v_i, i_{in}, P_{pv}, i_{s1}, i_{s2}, zoom-in at (b) 210W, (c) 215W

was used simulate the operating conditions of two PV array. The PV parameters were based on a 220W Sanyo HIT-N220A01 PV panel. An InfiniiVision MSOX6004A oscilloscope from Keysight Technologies was used to obtain the experimental waveforms and measure the efficiencies. The proposed single-sensor MPPT algorithm was implemented on a Texas Instruments (TMS)320F28335 DSP board and a single voltage divider consisting of two resistors were used to ensure the peak resonant capacitor voltage could be measured safely. The Texas Instruments Code Complier Studio (CCS) software was used to code the DSP board. The components used on the scaled-down prototype are provided in Table 2-1. Figure 2-20(b) shows the experimental setup along with the hardware prototype.

Figure 2-21(a) shows the input voltage, input current, both switch currents, and the panel operating power for 20 seconds of operation with the light intensity changing every 5 seconds. It can be seen that when the light intensity changed the operating power either dropped or increased

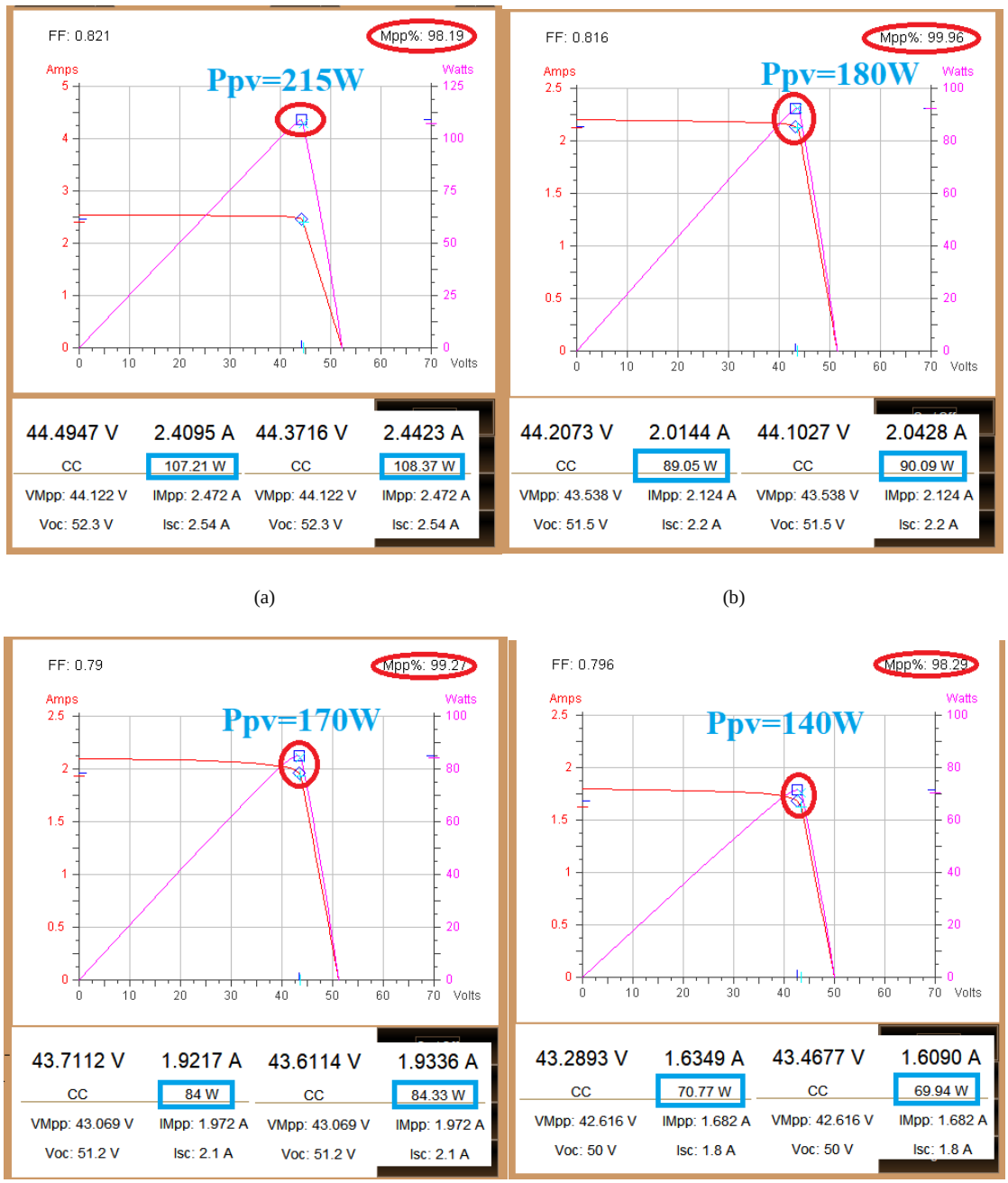


Figure 2-22: PV emulator Maximum Power Operating at (a) 215W, (b) 180W (c) 170W (d) 140W

but then eventually moved towards steady state. Figure 2-21(b) shows a zoom-in of the operating waveforms at 140W and 215W respectively. It can be seen that the system maintained soft-switching operation at all conditions regardless of the operating state.

As stated in Table 2-1, two emulator channels were connected in parallel to increase the PV current and power level. Figure 2-22 shows the operating power of both channels for the two

scenarios discussed in Figure 2-21. The MPP% located at the top right of each figure confirms that the extraction efficiency was above 99% in all scenarios. The measured input power in Figure 2-21(c) is seen to be approximately 215W. Figure 2-22(a) lists the operating PV power of the first channel to be approximately 107W which is confirmed in the shown P-V curve. The second channel is seen to operate at approximately 108W which leads to a total power of 215W. This confirms that the system was operating at the MPP. The operating condition in Figure 2-21(c) can also be seen to match the MPP shown in Figure 2-22(d). This confirms that the single-sensor MPP algorithm was successfully able to track the MPP operation condition with only the resonant capacitor voltage.

Figure 2-23 shows the converter's input inductor current and the resonant capacitor voltage and current at the rated condition. With a minimum value of 3.28A, it is confirmed that the proposed converter operates well into continuous conduction mode (CCM). The resonant capacitor voltage and current waveforms match the expected waveforms shown in Figure 2-2. Figure 2-24 (a) shows the converter output voltage when operating at 215W. The converter operated with an output voltage of 392V which confirms it is able to achieve a large step-up gain. Figure 2-24 (b) shows the switch voltage and current waveforms while a zoom-in of the turn-off transition point is shown in (c) and (d). Here it can be seen that the converter operated with near zero turn-off losses.

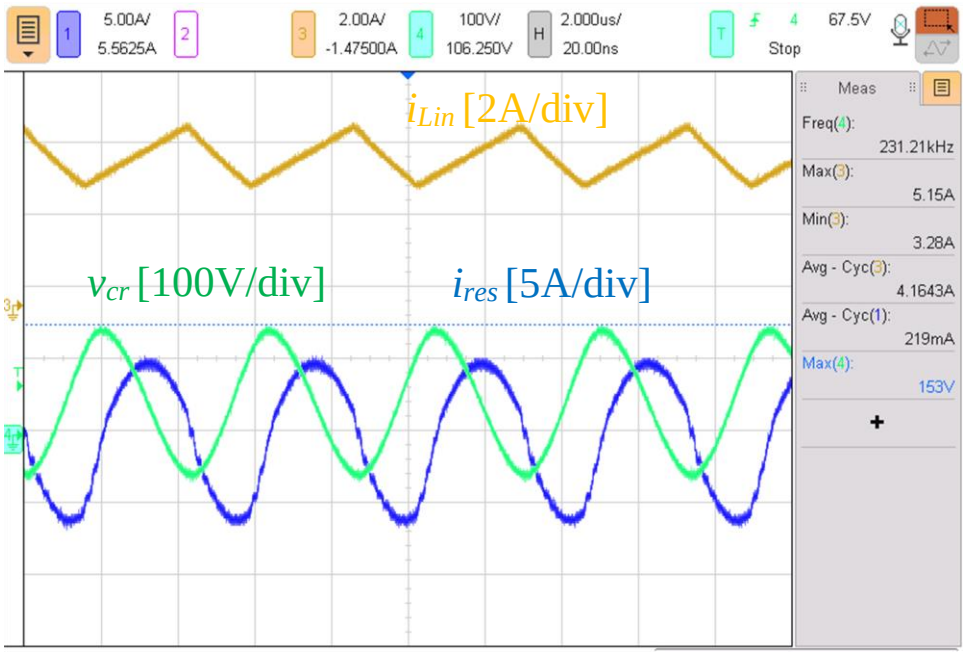
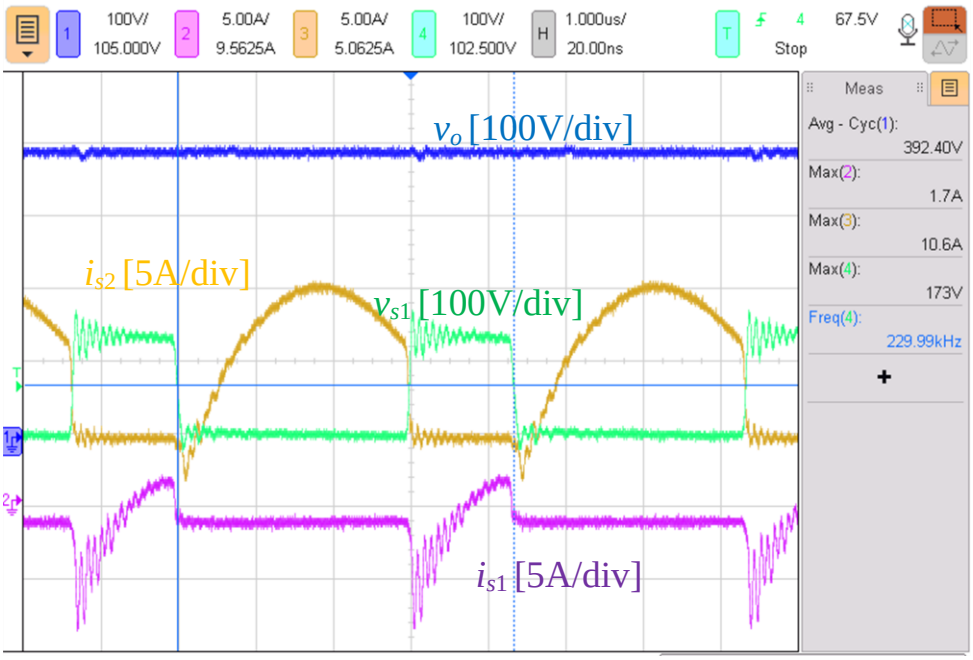
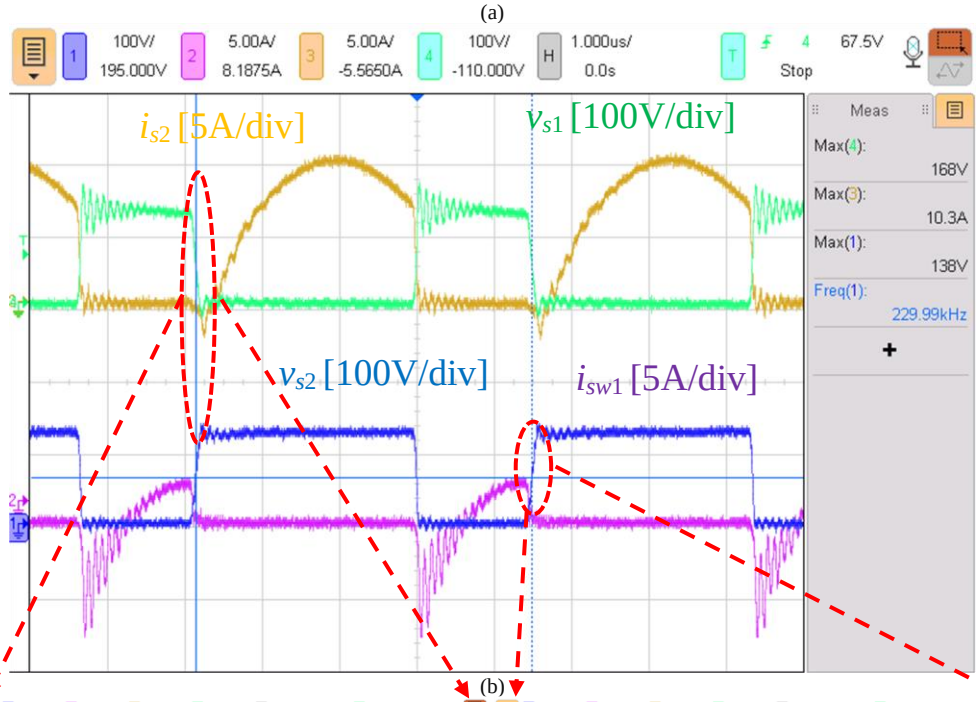


Figure 2-23: experimental waveforms: v_{cr}, i_{res}, i_{Lin}



(a)



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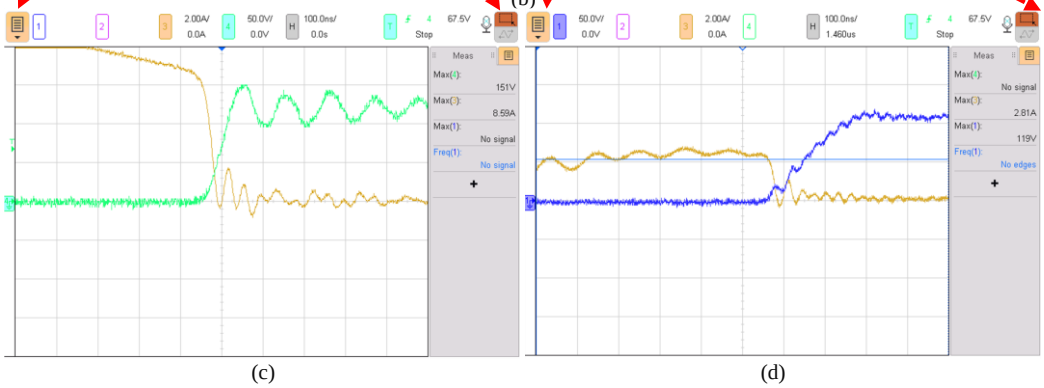


(c) (d)

Figure 2-24: (a) v_o, v_{s1}, i_{s1}, i_{s2} (b) v_{s1}, v_{s2}, i_{s1}, i_{s2}, zoom-in at (c) s_1 turn off, (d) s_2 turn off

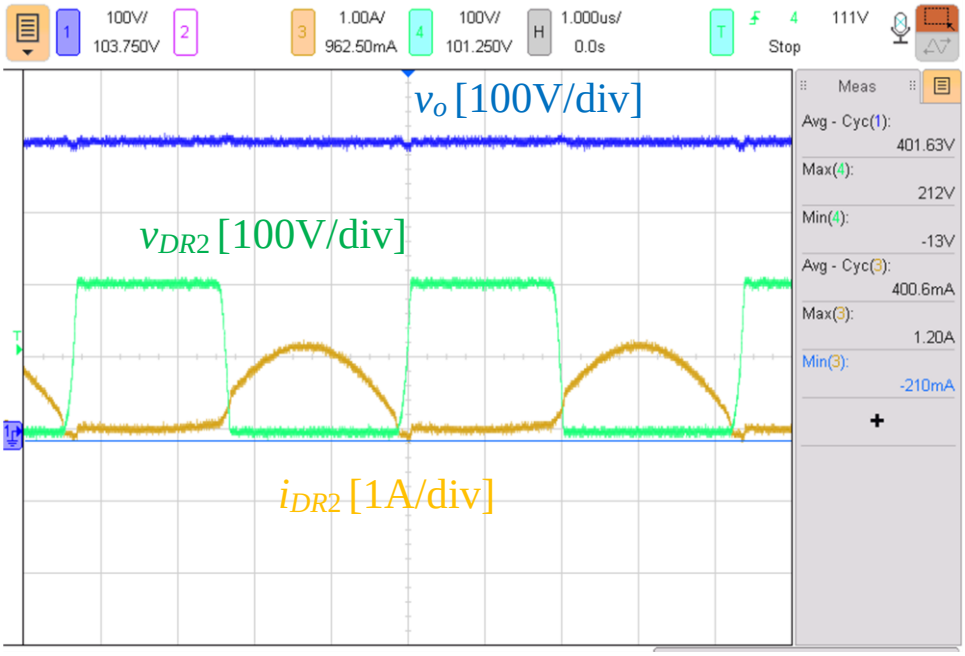
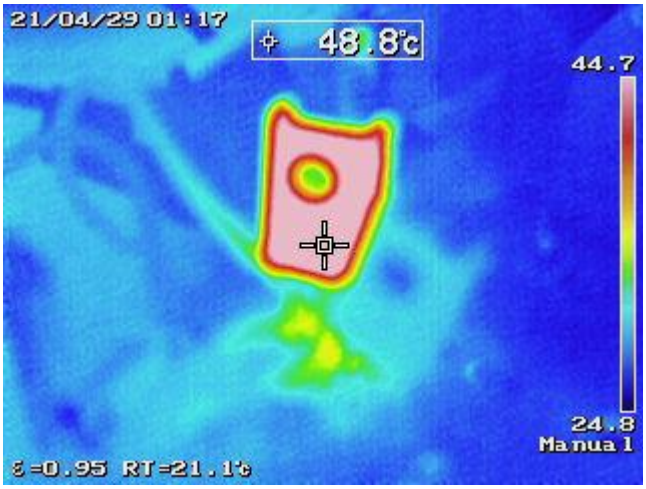
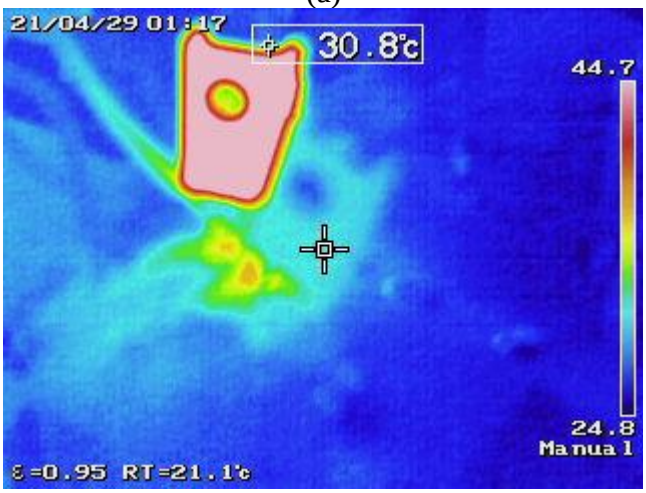


Figure 2-25: experimental waveforms: v_o, v_{DR2}, i_{DR2}

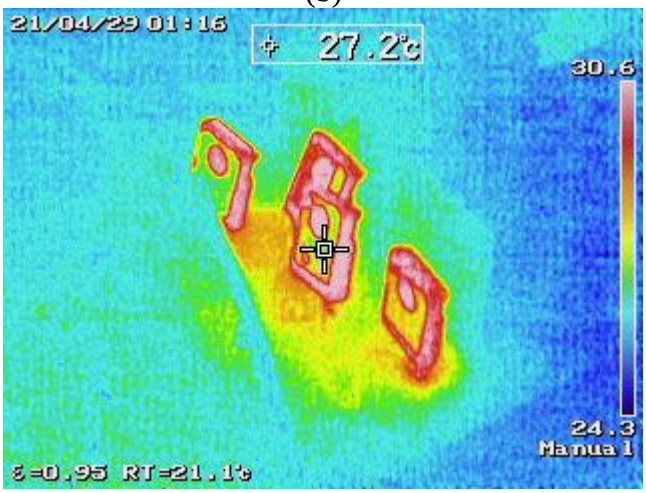
The operating condition of one of the VQ diode is shown in Figure 2-25. It can be seen that the peak diode voltage is half of the output voltage which is expected from (2.45). It can also be seen that the VQ diodes turn on and off with ZVS. Figure 2-26 shows thermal images of the hardware prototypes switches and the four VQ diodes when operating at 220W. Figure 2-26 (a) and (b) show S_1 and S_2 respectively and from this it can be seen that the temperature of S_2 is 10°C higher than S_1. As the RMS current of S_2 is larger than S_1, it is expected that S_2 will have increased conduction losses. A peak temperature of 48.8°C for S_2 was measured. The four VQ diodes shown in Figure 2-26 (c) are all operating below 30°C. The scaled-down hardware prototype's efficiency is shown as a function of the rated power in Figure 2-27. The peak operating efficiency was 97.1%, and the California Energy Commission (CEC) efficiency was 95.7%.



(a)



(b)



(c)

Figure 2-26 Thermal measurements: (a) S_2, (b), S_1 (c) Dr_1, Dr_2, Dr_3, Dr_4

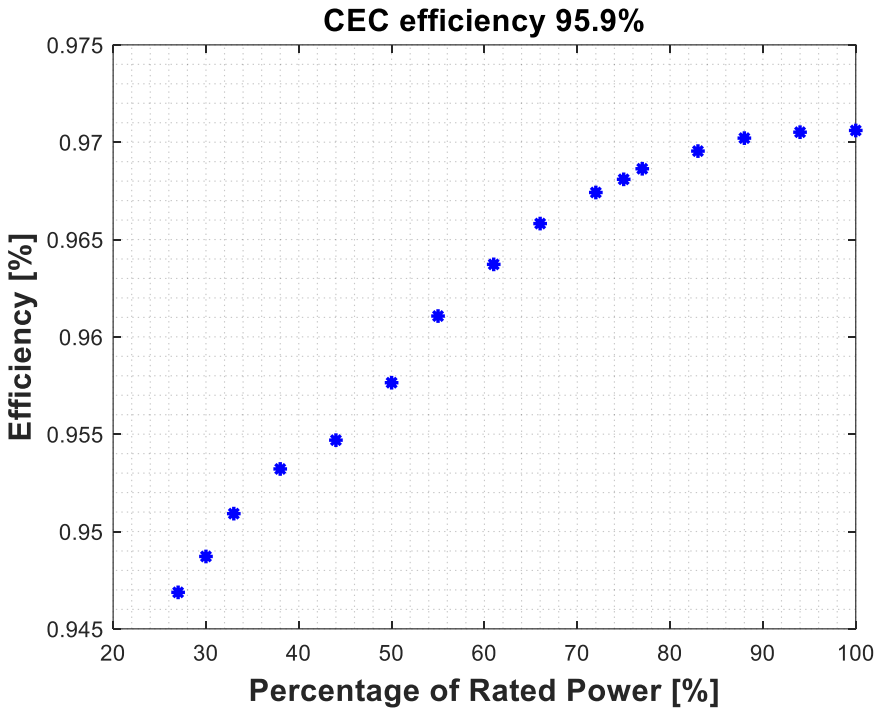


Figure 2-27 Converter efficiency at different operating power conditions

To highlight the benefits of the proposed converter, it is compared with other high-gain converters in Table 2-2. Of the six converters provided, it can be seen that [65] operated with the least number of switches, however eight diodes and nine capacitors are required which leads to a higher total component count. This converter also operates under hard-switching condition, along with [66] which limits their switching frequency and increases the size of passive components. [23] and [67] both function without a transformer but hard-switching, no isolation, and low switching frequencies are major drawbacks. [68] and [69] achieve a high step-up gain while also operating under soft-switching condition however an electrolytic capacitor is used at the input which are known for reducing the overall lifetime expectancy of the system. [68] also requires a large turns-ratio of 1:5.4. Compared to this, the proposed converter achieved a gain of ten, operates with soft switching and at a higher switching frequency, and provides isolation with a low turns-ratio.

Table 2-2 Comparison of High Gain topologies for PV energy systems

Converter	**Components**					***Isolated?***	***MPPT Sensor***	F_s	**Soft/hard switching**	**Rated Power**	**Gain**	**Rated V_o**
	Switch	Diode	Inductor	Capacitor	Transformer							
[23]	2	6	2	7	0	No	-	100kHz	Hard	200W	20	
[66]	2	4	1	4	1 (1:1)	No	I, I, V, V	50kHz	Hard	100W	10	
[68]	2	2	3	6	1 (1:5.4)	Yes	I, V	50kHz	Soft	300W	10	400
[69]	2	4	1	8	1 (1:2.2)	No	-	60kHz	Soft	250W	9.5	380
[65]	1	8	1	9	1 (12:26)	No	-	40kHz	Hard	200W	13	400
[67]	2	3	2	2	0	No	I, V	50kHz	Hard	10W	5	100
Proposed Converter	2	4	2	6	1 (1:2)	Yes	V	230kHz	Soft	220W	10	400

Table 2-3 Comparison Current-sensorless MPPT algorithms for PV energy systems

Controller	***MPPT Sensor***	***Implementation Cost***	**Converter Dependent**	**Extraction Efficiency**	**Settling Time**
[38]	*Irr*, *T*	High	No	99.2%	30ms
[47]	*Irr*, *T*	High	Yes	>99%	-
[49]	*V*, *V*	Medium	Yes	99.0%	50ms
[50]	*V*	Low	Yes	-	-
[53]	*V*	Low	Yes	99.81%	250ms
Proposed Controller	*V*	Low	Buck, Boost, Flyback,	99.4%	20ms

To highlight the advantages of the proposed single voltage MPP tracker, its operation was compared to other single-sensor algorithms as shown in Table 2-3. [38] and [47] both opted to use temperature and irradiance sensors as well as neural network-based algorithms to determine the MPP. Although they are capable of high extraction efficiency and fast settling time, the required sensors and algorithm type implies the implementation cost is high. Further, [47] was designed for a quazi Z-source inverter and will not function with other topologies, which limits its application. This issue is also present with [49], [50], and [53]. Although they operate with a single voltage sensor, their algorithms are designed for specific topologies, implying they must be updated or modified to function in other scenarios. In particular, [49] requires knowledge of the converters passive components which is not always available and can change over time. Compared to these controllers, the proposed algorithm is not limited to a single topology and achieves both a high extraction efficiency and fast settling time with only a single voltage sensor.

2.5 Chapter Summary

In this chapter, a new single sensor current-sensorless maximum power extraction technique for PV energy systems was proposed. A new high gain boost-*CLL* integrated resonant converter with complete soft-switching operation was first designed and discussed. By integrating a boost and *CLL* resonant circuit, the system was capable of achieving a high voltage gain while simultaneously being capable of MPPT operation through duty ratio control. A voltage quadrupler was employed as the rectifier to achieve both a DC output voltage and an additional step-up gain. The *CLL* resonant circuit also allowed for complete soft-switching operation for both the boost switches and the voltage quadrupler diodes. From here the proposed current-sensorless MPPT algorithm was applied to the system. This algorithm sensed and maximized a simple voltage parameter of the converter such that the generated PV array power was indirectly maximized at all operating conditions. An additional adaptive tracking and ripple minimization stage utilizing gradient ascent was included to further enhance the algorithm's operation.

The converter is first tested in simulation with a 150V input, 1kV output system to confirm the high-gain and soft-switching capabilities. To verify the performance of the proposed single-sensor MPPT algorithm as well as the developed converter, simulation results on a 220W, 120kHz, 400V output system have been provided. Initial results established that the resonant capacitor voltage can be used to indirectly maximize the PV array power. This was further validated as the controller was able to maximize the input power in various scenarios. The steady-state waveforms confirmed that complete soft-switching operation was achieved. To further verify the accuracy and feasibility of the converter and controller, a scaled down proof-of-concept hardware prototype was constructed with an operating power, frequency, and output voltage that matched the simulation. The experimental results demonstrate the accuracy of the proposed controller, which achieves a tracking efficiency of over 99% while employing only a single voltage sensing loop. The dynamic performance of the converter confirmed a high step-up gain and soft-switching operation were achieved. The final results also confirmed a maximum CEC efficiency of 95.9% for the hardware prototype. Comparison between the proposed converter and controller to existing works in literature have been provided to further highlight its benefits.

Chapter 3. Proposed Modular High Step-up DC-DC Converter with Integrated Power Balance Units for PV Based MVDC System

In Chapter 2, a single-sensor current-sensorless maximum power extraction technique for PV energy systems was presented and tested on a newly developed high-gain converter. The proposed approach was able to maximize the PV array's operating power without the use of a current sensor, complex mathematical functions, or multiple sensors while being compatible with a wide range of converters. The developed converter achieved a high-gain through the use of a resonant circuit and a voltage multiplier rectifier. This makes the designed algorithm and converter a good choice for modular based MVDC topologies.

As discussed earlier, modular topologies such as IIOS suffer from unbalanced modular output voltage due to power mismatch, leading to overvoltage scenarios which makes the design

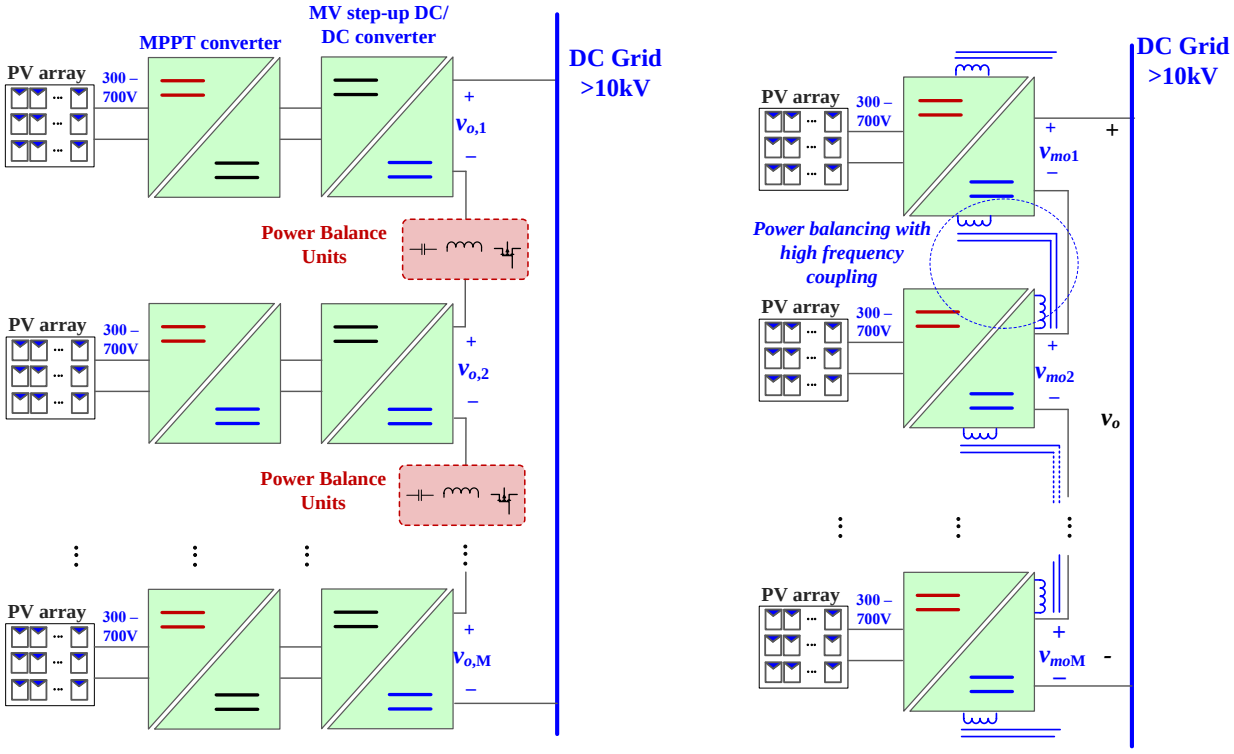


Figure 3-1: (a) typical power architecture in PV MVDC systems utilizing external PBU (b) proposed modular power architecture utilizing integrated PBU for PV MVDC systems

of each module challenging. Figure 3-1(a) shows a typical power architecture in PV MVDC systems to address the power balance issue. As discussed in section 1.4.3, additional power balance units (PBU) are added to the system to remove the output series connection and regulate power flow such that the output voltage across all modules are equal. Although this can resolve the issues with IIOS topologies, it is evident from Figure 3-1(a) that additional components are required per-module which can have a negative impact on the operating efficiency and system cost.

In an effort to alleviate the power balance issue without the use of additional stages, this chapter focuses on the development of an integrated power balance controller for modular IIOS topologies in MVDC applications as shown in Figure 3-1(b). In the first part, potential topologies and their control techniques are discussed. From here, the operating principles and analysis of the chosen topology and the power balance controller will be provided. In the final section, the performance of both the modular based MVDC system and the power balance controller are verified through simulation and experimental work on proof-of-concept prototypes.

3.1 Potential PBU Topologies

Figure 3-1(b) shows the concept behind the proposed work. Instead of attempting to share module power and balance the output voltage at the final stage, the converters would be coupled to their neighboring modules such that the module power is shared earlier. This can provide additional benefits in scenarios of severe light intensity variations.

3.1.1 Standard Power Balance Unit

Figure 3-2(a) shows an example of the conventional topologies with two modules during a situation where the second module's PV array is not generating power. The PBU would distribute the power evenly to prevent voltage imbalance, however, this implies the first module must be capable of providing a large step-up gain such that it can reach the MVDC grid level. This indicates that in an 'M' module system each module would need to be designed for the worst-case scenario, which is when all other modules are inactive, in order to ensure the system can withstand all cases. This would require high rated components that would increase the size and cost of the system. Further, there is no guarantee that such high rated components exist.

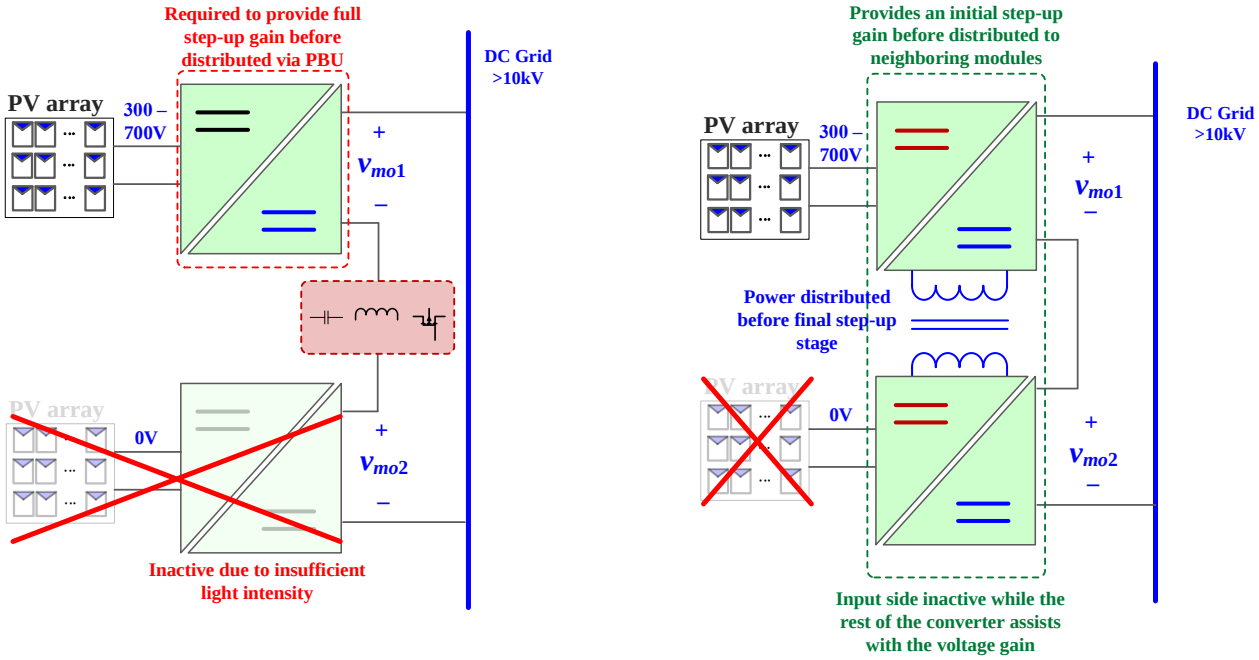


Figure 3-2: Example of power balancing units in (a) literature (b) proposed work

3.1.2 Integrated Power Balance Unit

Figure 3-2(b) shows an example of the proposed concept under the same condition mentioned above. Although the second module's PV array is inactive, as the power is shared before the final step-up stage, the second module's converter can partially contribute to the voltage gain. The proposed topology from Chapter 2 utilizes a *CLL* resonant circuit with an output inductor on the secondary side located before the voltage quadrupler. By coupling this inductor together with a nonboring module's output inductor, a power flow path between modules is created. Therefore, each modules VQ would be contributing to the step-up gain regardless of whether their PV array is functioning.

Although coupling the output inductors allows for power flow between modules, this flow cannot be regulated as is. In order to regulate the power flow, a parameter of each module has to be controlled. For the topology discussed in Chapter 2, the input switches duty ratio is regulated for MPPT purposes. If the module's output inductor is now coupled to another module, the operating frequency of these switches must be kept consistent between all modules and thus variable frequency control cannot be used. To overcome this issue, the VQ can be modified to

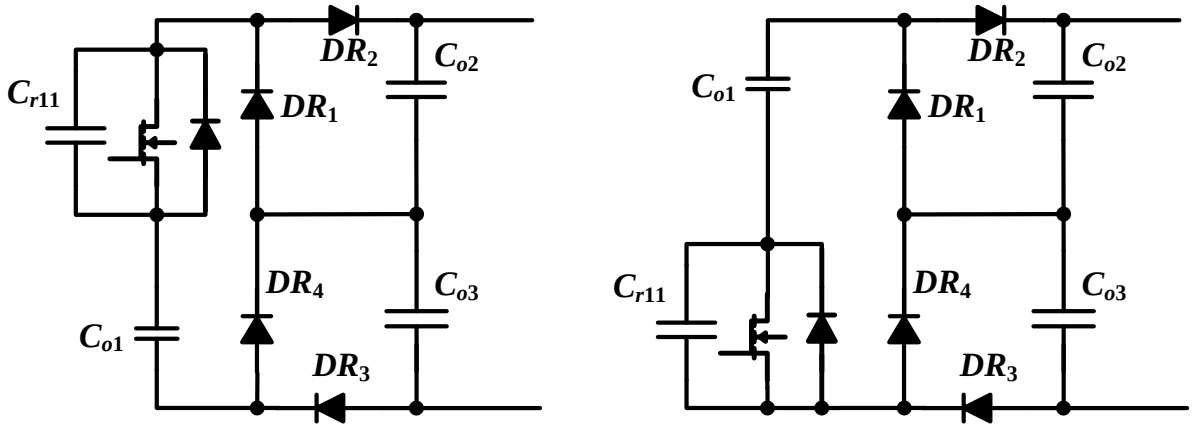


Figure 3-3: Possible AVQ configurations

include an active switch. Two possible configurations are shown in Figure 3-3 (a) and (b) where the upper and lower input capacitors have been replaced with an active switch respectively. Although both topologies are capable of regulating power flow between modules through variable duty ratio, the direction of current flow into the AVQ can impact soft-switching operation. For this work, the version shown in Figure 3-3(b) was chosen.

3.1.3 Topology Configuration

In 3.1.2 it was discussed that the VQ used in Chapter 2 can be modified to include an active switch whose duty ratio can be regulated to control power flow and in turn the output voltage of each module. This power flows from one module to another through the output inductor of the *CLL* resonant circuit which is now coupled to a neighboring module. Out of the various possibilities for coupling modules together, there are two possible configurations for the proposed topology. The linear configuration is shown in Figure 3-4(a) for a four-module system where the output inductor of each module is coupled to their neighboring module below itself. Modules M_2 and M_3 have both their output inductor and the neighboring module's inductor present whereas M_4 has only the secondary side of the third module's inductor. As a result, for an 'M' module system, 'M-1' coupled inductors are required. The circular configuration is shown in Figure 3-4(b) where the fourth modules output inductor is coupled to the first module. This means that for an 'M'

module system, ‘M’ coupled inductors are required. Although the circular topology requires an extra coupled inductor compared to the linear topology all modules would be designed the same. For the linear topology, the first and last module’s coupled inductor must be designed differently to accommodate the lack of another modules output inductor. This can be done by changing the turns-ratio of the inductor. For the circular topology, as all modules have the same design, it is easier to implement a plug-and play approach for increasing or decreasing the number of modules in the system. As a result, for this work the circular approach has been chosen.

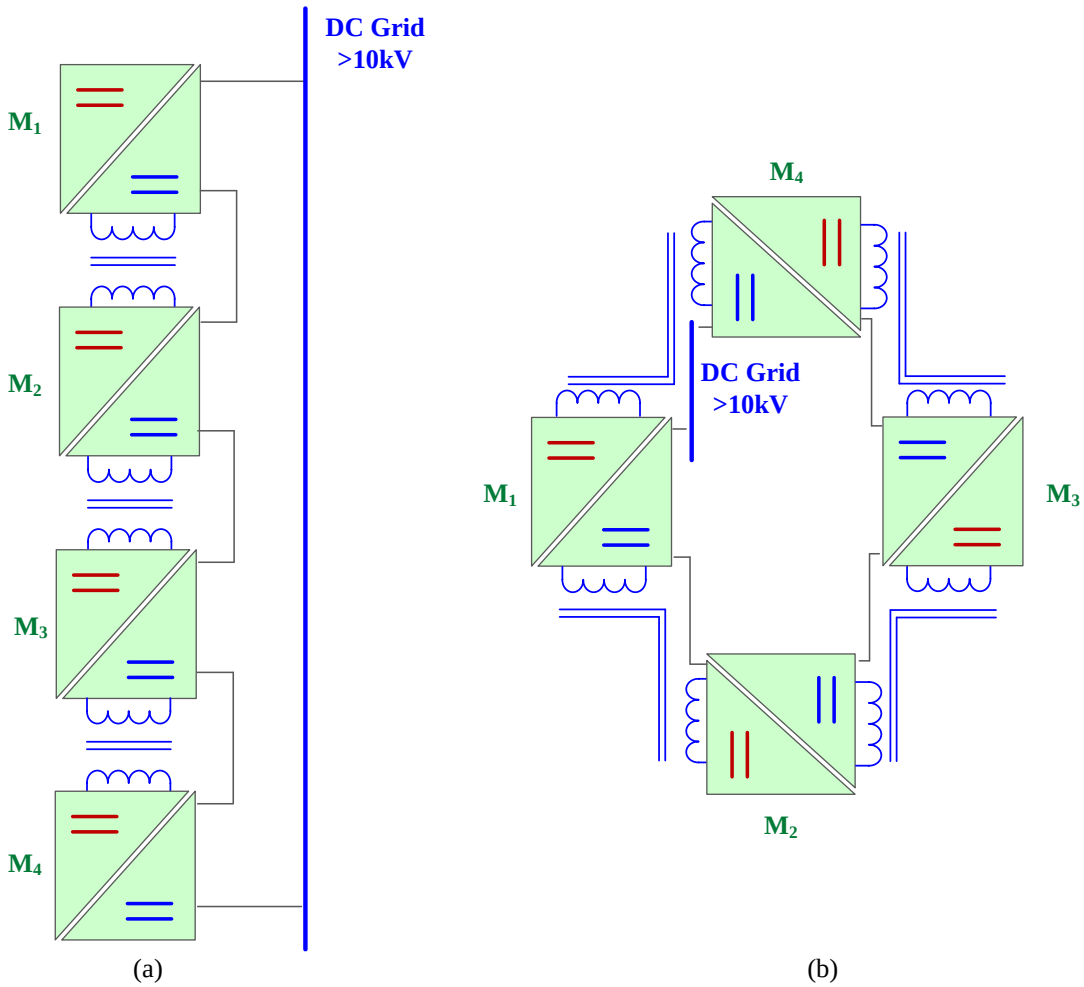


Figure 3-4: Proposed topology configurations (a) Linear, (b) Circular

3.2 Proposed Integrated Modular Power Balance Topology and Operation

Figure 3-5 displays topology of an M-module configuration. A single module consists of an integrated boost and an isolated *CLL* resonant circuit together with an active voltage quadrupler. The input switches S_{M1} and S_{M2} are gated with a duty-ratio of d_M and 1-d_M respectively to achieve both a step-up voltage gain and maximum power extraction. This is similar to the topology discussed in Figure 2-1 of Chapter 2. The voltage waveform generated across the switch S_{M2} forms the input to the *CLL* resonant stage which consists of a resonant capacitor (C_{rM}), a 1:n coupled inductor with a magnetizing inductance (L_{mM}) which isolates the primary and secondary side, and output coupled inductor (L_{oM}). The neighboring module's output inductor is also present on the

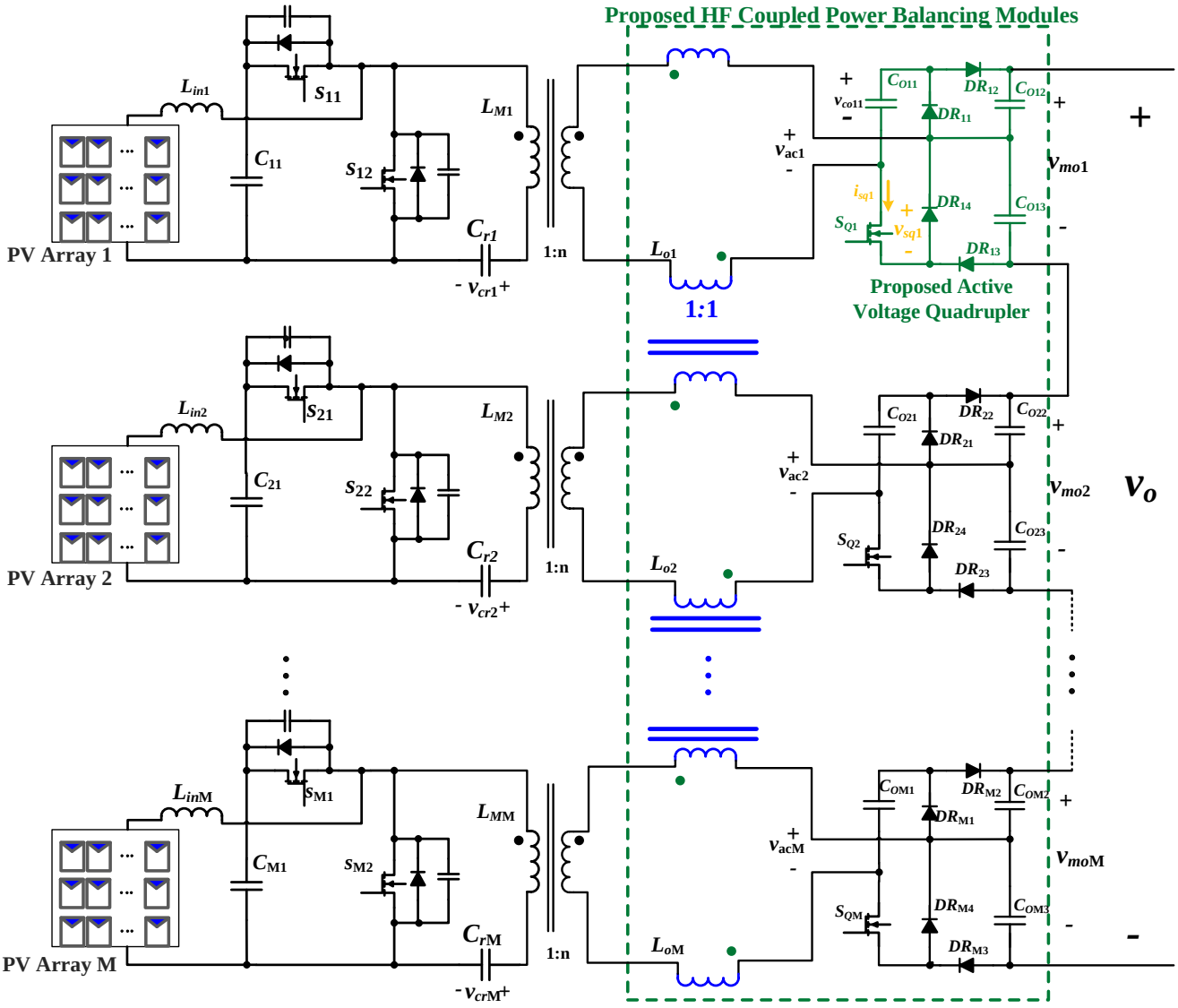


Figure 3-5 Topology of the proposed M-module system

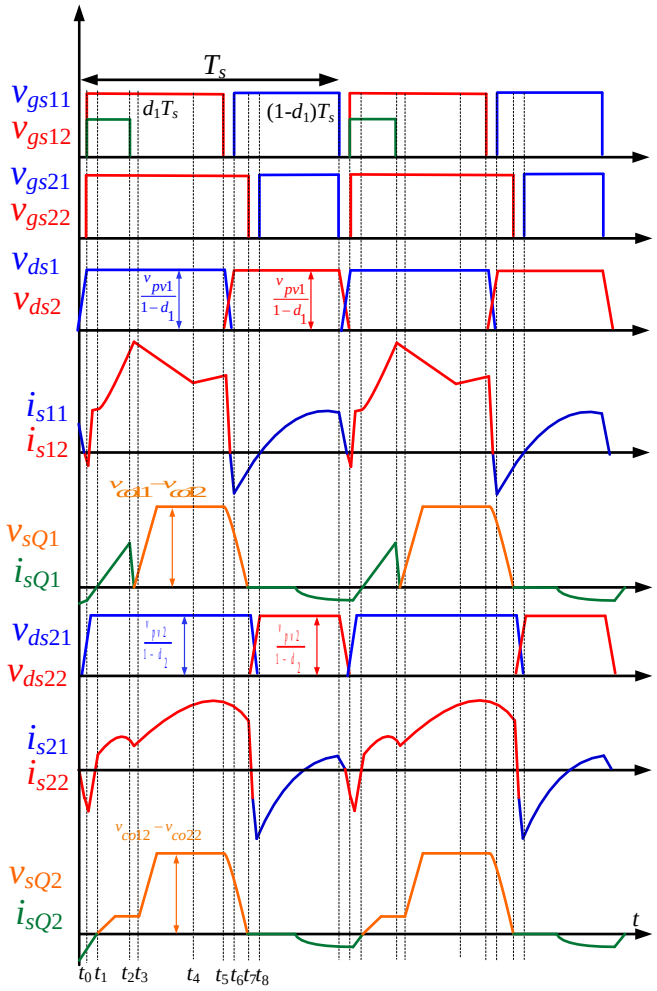


Figure 3-6 : Input and AVQ operating waveforms during power sharing condition with two modules

secondary side in a series connection. The output of the resonant stage connects to an active voltage quadrupler (AVQ) that rectifies the resonant stage's AC voltage back to DC. The AVQ consists of an active switch S_{QM} whose duty-ratio can be controlled to regulate the power flow from the module to its neighboring modules. This switch operates at the same frequency as the input switches. Although the primary side of the proposed converter matches that of the topology discussed in section II, due to the output inductor being coupled to the neighboring modules and the AVQ switch, the shape of the resonant circuit output voltage and current waveforms have changed. This section will discuss the theoretical operation of the converters input stage.

[$t_0 < t < t_2$]: At time t_0, the gate signal is removed from S_{11} and S_{21} and applied to S_{12}, S_{22}, and S_{Q1}. As the summation of the input and resonant current is negative and as the secondary side resonant

current is negative, the anti-parallel diodes of all switches are active which allows for ZVS turn-on performance to be achieved. During the time period between t_0 and t_1, S_{12}, S_{22} and S_{Q1} turn on with ZVS condition. At this point the input to the AVQ is short, and power is transferred from module M_1 to M_2. At the same time, the resonant current of both modules continues to increase. The voltage across the switch S_{Q2} begins to rise and maximizes at the point that is equal to the difference between the voltage across the secondary side of the magnetizing inductance of each module. The duty-ratio of S_{12} and S_{22} are chosen to achieve maximum power extraction while the duty-ratio of S_{Q1} is chosen to regulate the module power flow. As the duty-ratio of S_{Q1} is always less than S_{12}, this stage ends once the gate signal is removed from S_{Q1}.

[$t_2 < t < t_4$]: At t_2, the gate signal is removed from S_{Q1} and the secondary side resonant current of each module can now flow through their respective AVQ. The voltage across S_{Q1} begins to charge slowly due to the snubber cap, resulting in ZVS turn off operation at time t_3. The change in the secondary side resonant current is reflected on the primary side resulting in a decrease in the current through S_{12}. This continues until the resonant current reaches zero at time t_4.

[$t_4 < t < t_6$]: Once the resonant current reaches zero at time t_4, only the input inductor current contributes to the current flowing through S_{12}. This continues until the gate signal is removed from S_{12} at t_5. As both modules are operating at different power levels and have individual MPPT controllers, it is expected that each module operates at a different duty-ratio and thus S_{22} is still active. During time period t_5 to t_6, current begins to flow through the anti-parallel diode of S_{11} while the voltage across the AVQ switches begin to decrease to zero.

[$t_6 < t < t_8$]: The gate signal is applied to S_{11} at t_6 and as the current is negative, the S_{11} will eventually achieve ZVS operation. At t_7, the gate signal is removed from S_{22} and applied to S_{21} at t_8, allowing for eventual ZVS operation. The voltage across the AVQ switches reaches zero and once the secondary side resonant current is negative, the current will begin to flow though the switches anti-parallel diode and allow for ZVS operation to be achieved. At the end of this stage, the circuit reverts back to the first stage.

3.3 Proposed Power Balance Controller and AVQ Description and Operation

The proposed converter is capable of simultaneous and individual maximum power extraction and voltage balancing which are handled by different parameters as shown in Figure 3-7. In modular IIOS configuration, each module operates with a different set of PV arrays which can have different locations and are subjugated to different atmospheric conditions. Therefore, individual MPPT controllers are required per module. Typically for modular IIOS configurations, conventional MPPT controllers that function with voltage and current sensors to calculate the operating power are employed. This implies that for an 'M' module system, 'M' voltage and 'M' current sensors are required, which can drive up the system cost. Due to the simplicity of voltage sensors, in this work a single-voltage sensor MPPT controller is employed to maximize the operating power of each individual module. As seen in Figure 3-7, the converter's resonant capacitor voltage is utilized by the controller to maximize the operating PV power. Specific details regarding this controller have been discussed in Chapter 2 and will not be repeated here. The AVQ switch, S_{QM}, can allow for power transfer between modules through the use of duty-ratio control. By operating the module at a larger duty-ratio compared to neighboring modules, power can be transferred through the HF coupled output inductor. An example of this controller implemented on a two-module system is shown in Figure 3-8. The system senses the per-module output voltage which is sent to a proportional integral (PI) controller. The error between the output and reference voltage is utilized to regulate S_{QM}'s duty-ratio with pulse width modulation (PWM) control. If the duty-ratio of Module M_2's AVQ is larger than Module M_1, then power can be transferred from M_2 to M_1 during the on state of the switch. At the same time, the AVQ provides a further step-up voltage gain, allowing all modules to achieve a high gain.

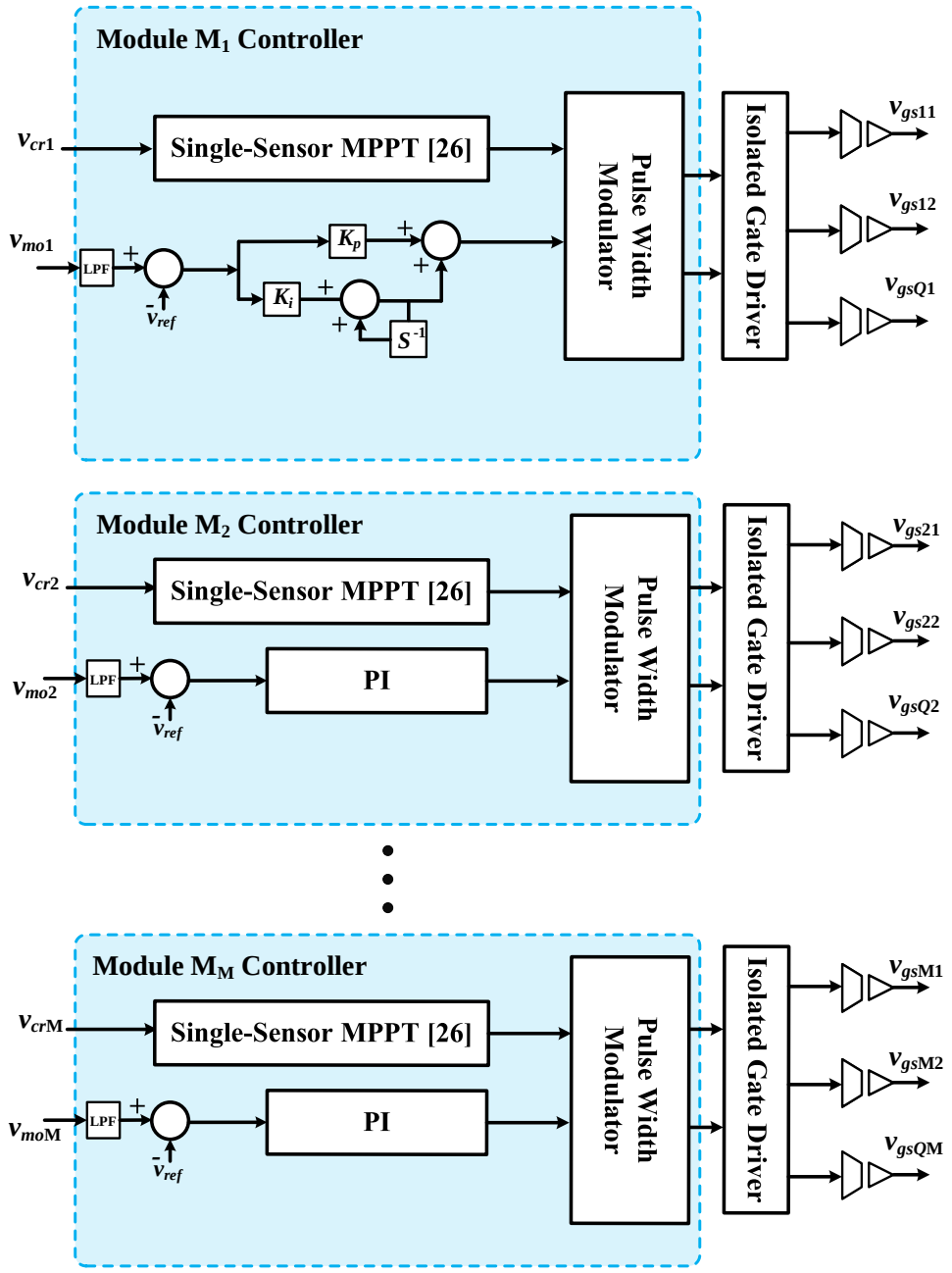


Figure 3-7: Single-voltage sensing MPPT and the power balancer controller for the proposed topology

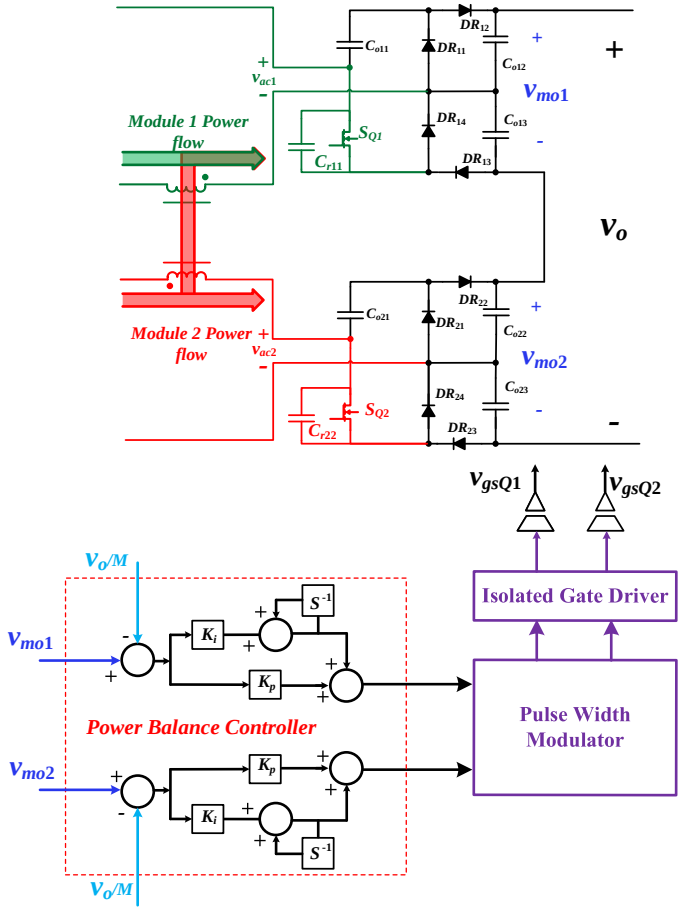


Figure 3-8: Operation of the power balancer controller (for two modules case)

The key operating AVQ waveforms for two modules are shown in Figure 3-9 under the assumption that the power level of module M_1 is greater than that of module M_2.

[$t_0 < t < t_3$]: At time t_0, the gate signal is applied to switch S_{Q1} and S_{Q2}. As the gate signals are applied to the AVQ switches while the currents are negative and increasing, the AVQ switches will eventually turn on under ZVS condition during this stage which is shown at time t_1. Module M_2 operates at a lower power level, therefore the gate signal is removed from S_{Q2} at time t_2. The resonant current i_{res22} flow through diode D_{R24} which connects the input of to the AVQ across the snubber capacitor. This allows for a path for the capacitor C_{r22} to charge to the voltage difference across the output inductance. As C_{r22} is in parallel with the AVQ switch, this voltage is listed as v_{sQ2} in Figure 3-9. During this same time period, the current through module M_1's AVQ switch,

S_{Q1}, has become positive and S_{Q1} has turned on under ZVS condition. As S_{Q1} is active, the input to the AVQ is short circuit which locks v_{ac1} at zero. The resonant current of M_1, i_{res12}, flows from the input of the resonant stage, through the S_{Q1} and the diode D_{R14}, and through the coupled inductor. This allows for power transfer from M_1 to M_2. Once the snubber capacitor is fully charged, i_{res22} reaches zero and the system proceeds to the next stage.

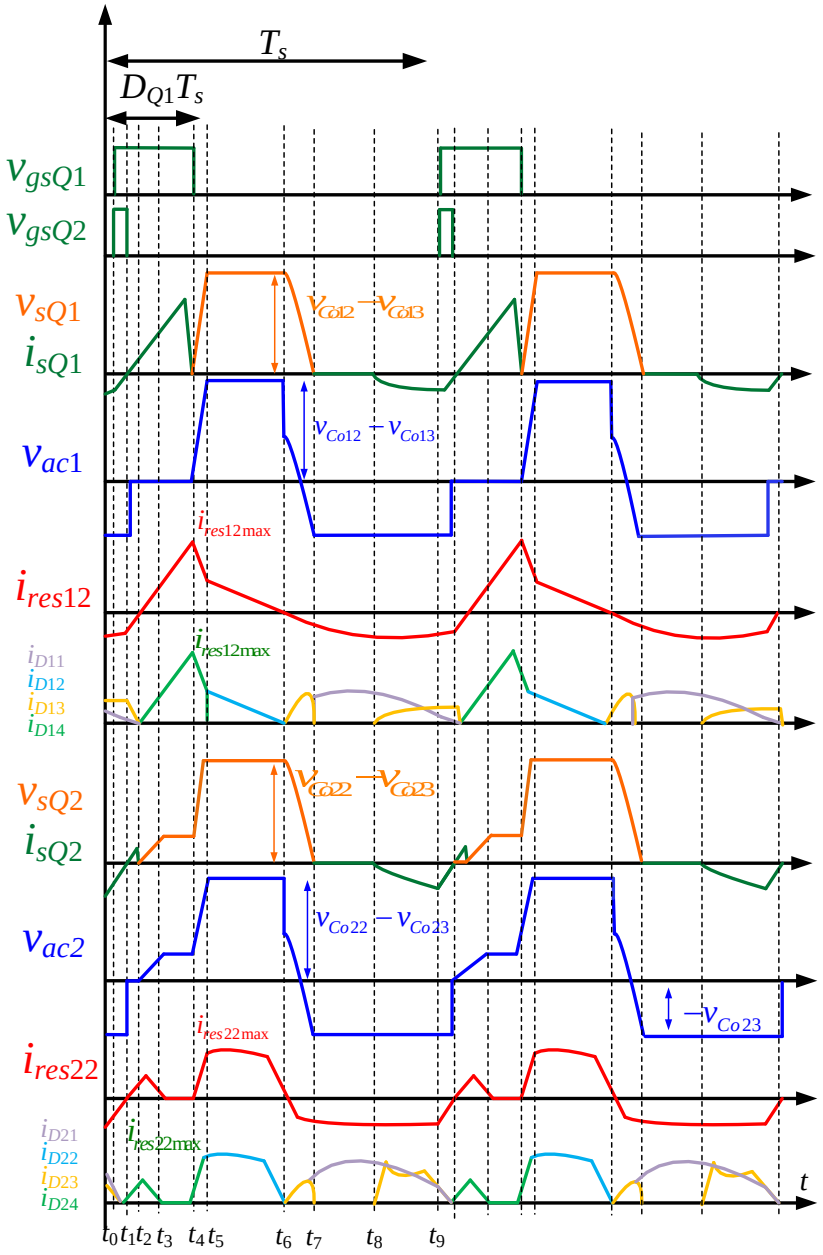


Figure 3-9 : AVQ operating waveforms during power sharing condition

[$t_3 < t < t_4$]: At time t_3, i_{res22} has reached zero, however i_{res12} is still positive and flows through S_{Q1}. Therefore, power is still being transferred from M_1 to M_2. At time t_4, the gate signal is removed from S_{Q1}. The current i_{res12} continues to flow through D_{R14} and now continues through the snubber capacitor, C_{r12}, allowing it to charge similar to how C_{r22} was charging in the previous stage. In M_2, the resonant current begins to flow again through D_{R24}, allowing for its snubber capacitor to continue to charge which is represented as an increase in the voltage v_{sQ2} in Figure 3-9. Once the

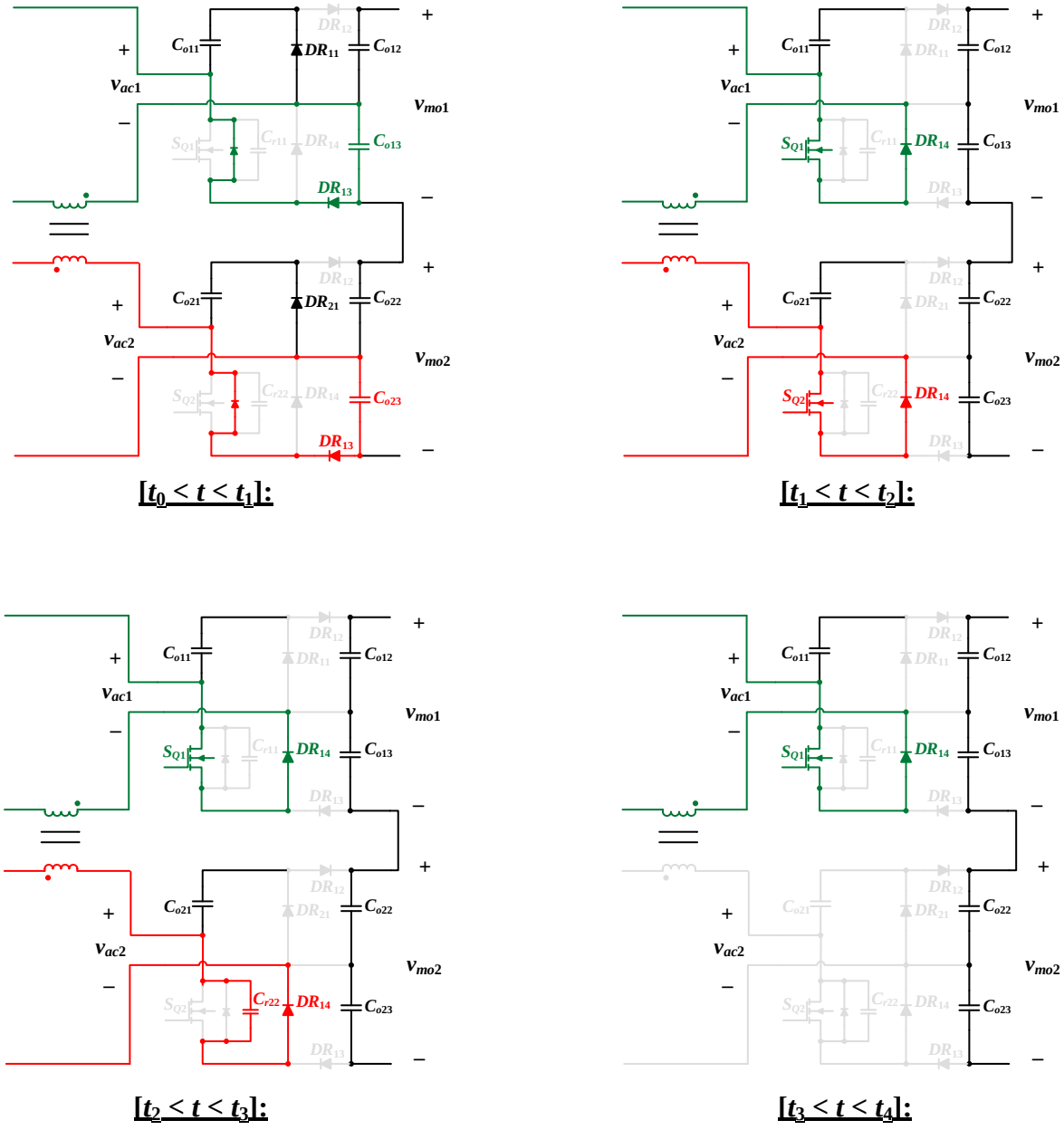


Figure 3-10: AVQ operating states for a two-module topology: [$t_0 < t < t_4$]

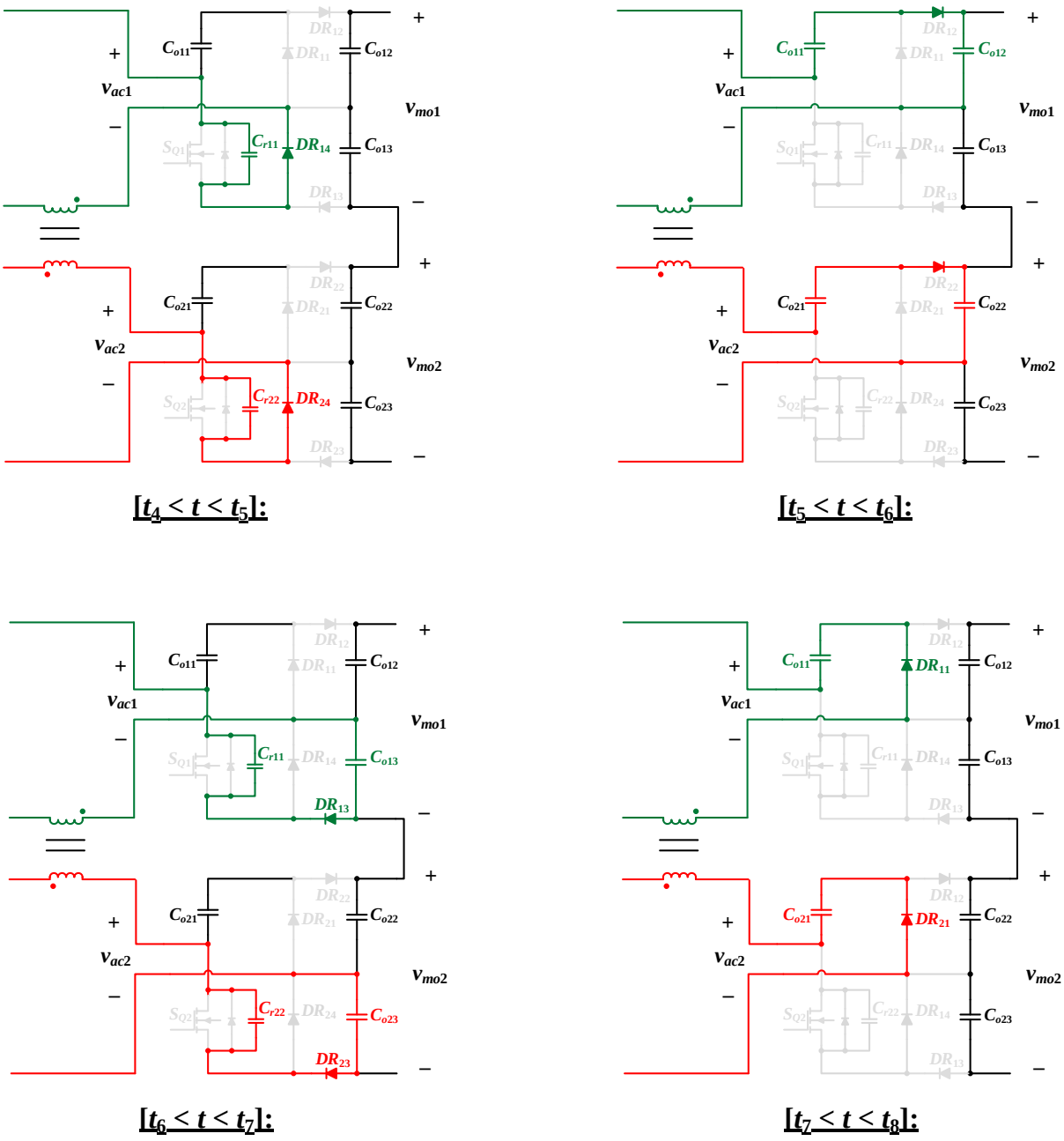


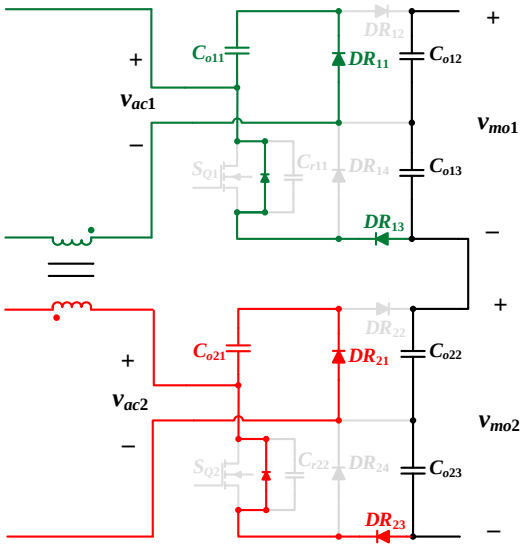
Figure 3-11: AVQ operating states for a two-module topology: [$t_4 < t < t_8$]

capacitor of both modules have fully charged, the respective resonant currents of each module begin to decrease towards zero. This stage ends once the resonant currents have reached zero.

[$t_5 < t < t_7$]: Once the snubber capacitors are fully changed and the voltage across the AVQ switches have reached their peak, the resonant current of each module begins to flow through the diodes D_{12} and D_{22} respectively and continues to decrease towards zero. At t_6, the resonant current is

negative and begins to flow through the diodes D_{13} and D_{23}. This allows for a path such that the snubber capacitors can discharge and allow the AVQ switch voltage to decrease to zero. As diode D_{14} and D_{24} are off, the capacitor pairs C_{o11} and C_{o12} along with C_{o21} and C_{o22} are no longer connected across their respective AVQ inputs, which results in an immediate decrease in the AVQ input voltage as shown in Figure 3-9. This stage ends once the voltage across the AVQ switch has reached zero.

[$t_7 < t < t_9$]: The voltage across the AVQ switch has reached zero and the resonant current begins to flow through the diodes D_{11} and D_{21}. During this time, as the resonant current is negative and continues to decrease, the input voltage to the AVQ is negative. At t_8, the resonant current begins to flow through the diodes D_{13} and D_{23} and in turn the anti-parallel diode of the AVQ's switch. Due to the negative resonant current, it is understood that the AVQ switches will turn on under ZVS operation. This stage ends once the gate signals are applied to the switch and the system reverts back to the first stage.



[$t_8 < t < t_9$]

Figure 3-12: AVQ operating states for a two-module topology: [$t_8 < t < t_9$]

3.4 Converter Analysis

This section will provide an in-depth analysis on the characteristic of the developed interlinking converter with the AVQ. In order to perform steady state analysis on the developed topology, the following assumptions are made.

1) All components, such as semiconductor switches and diodes are ideal unless stated otherwise.

2) The gating signal delay between switches are neglected.

3) The snubber capacitance effect across the semiconductor switches are neglected.

4) The coupled-inductor turns-ratio is 1:1 for the output inductor and 1-n for the magnetizing inductance.

5) Each module consists of the exact same component parameters.

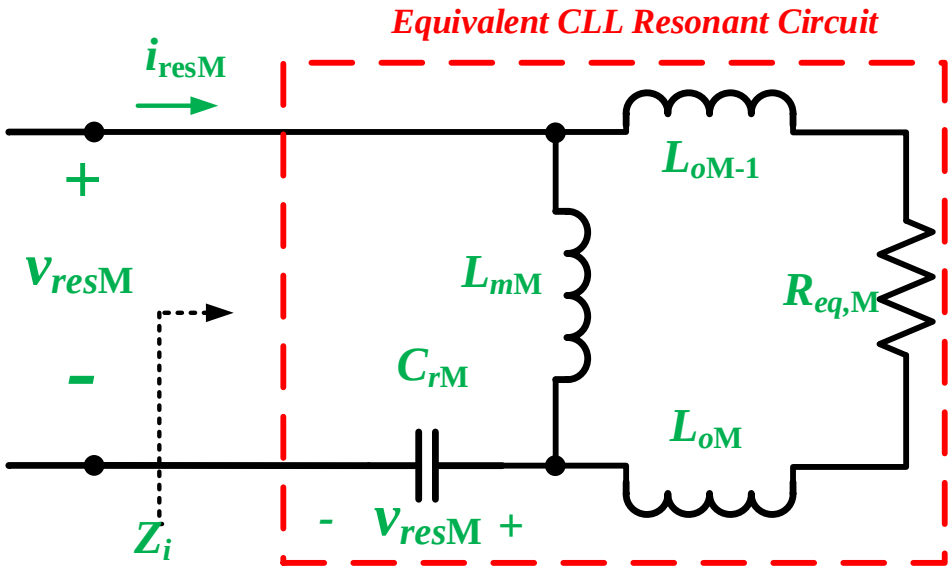


Figure 3-13 Equivalent circuit of the *CLL* resonant circuit

3.4.1 DC-Link Capacitor and Input Switch Voltage

The input stage of each module is the same as the topology discussed in Chapter 2 section 2.1.2.1 and as a result the voltage stress across the input switches and the DC link capacitor are (3.1) where $v_{pv\mathrm{M}}$ is the PV array voltage of the M$^{\mathrm{th}}$ module and d_{M} is the operating duty-ratio of the second input switch of the M$^{\mathrm{th}}$ module.

$$v_{\mathrm{sM1}} = v_{\mathrm{sM2}} = v_{\mathrm{CDCM}} = \frac{v_{pv\mathrm{M}}}{1-d_{\mathrm{M}}} \tag{3.1}$$

3.4.2 *CLL* Resonant Input Voltage

The equivalent circuit of the *CLL* resonant circuit is provided in Figure 3-13. The AVQ is replaced with an equivalent resistance and the *CLL* resonant output inductor of both the module and its neighboring module are present. The input voltage to the *CLL* resonant circuit, v_{resM}, is once again formed by the voltage waveform across the second input switch. As with before the *CLL* resonant capacitor blocks the DC component of this waveform, resulting in (3.2) where f_{s} is the system's operating frequency and θ is the phase angle provided in (3.3).

$$v_{res\mathrm{M}} = v_{s(ac)} = \frac{\sqrt{2}v_{pv\mathrm{M}}}{\pi\left(1-d_{\mathrm{M}}\right)}\sqrt{1-\cos\left(2\pi d_{\mathrm{M}}\right)}\sin\left(2\pi f_s t+\theta\right) \tag{3.2}$$

$$\theta = \tan^{-1}\left(\frac{\sin\left(2\pi d_{\mathrm{M}}\right)}{1-\cos\left(2\pi d_{\mathrm{M}}\right)}\right) \tag{3.3}$$

3.4.3 Resonant Capacitor Voltage

The resonant capacitor of each module is located on the primary side of the *CLL* resonant circuit as seen in Figure 3-14. Thus, the voltage across the resonant capacitor can be obtained by applying *KVL* to the green loop (3.4). As with Chapter 2, this equation is a function of the rate of change of the resonant current as a function of time for both the primary and secondary. What differs from Chapter 2 is the presence of the neighboring module's output inductor $L_{o\text{M-1}}$. As mentioned in 2.1.2.3, the voltage across a coupled inductor is a function of the current through all of its windings. Therefore, when applying KVL to the red loop in Figure 3-14 the secondary side current of the neighboring module is present (3.5) and contributes to the rate of change of the secondary side current (3.6).

$$v_{Cr\text{M}} = v_{s\text{M2}} - \left(L_{m\text{M}} \frac{di_{res\text{M1}}}{dt} + L_{m\text{M}} N \frac{di_{res\text{M2}}}{dt} \right) \tag{3.4}$$

$$L_{m\text{M}} N \frac{di_{res\text{M1}}}{dt} + L_{m\text{M}} \left(N\right)^2 \frac{di_{res\text{M2}}}{dt} = L_{o\text{M}} \frac{di_{res\text{M2}}}{dt} + L_{o\text{M}} \frac{di_{res(\text{M-1})2}}{dt} + v_{ac} \tag{3.5}$$

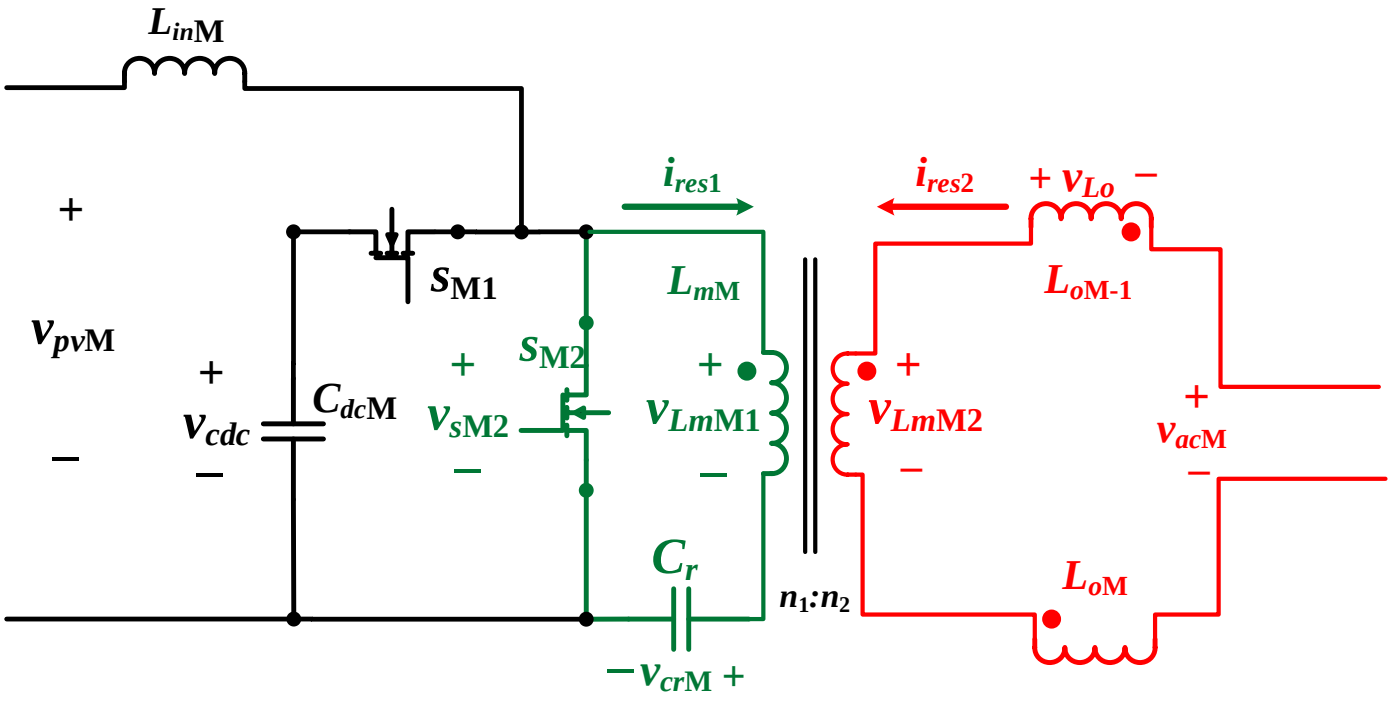


Figure 3-14 Input boost and *CLL* resonant stage of the proposed converter

$$\frac{di_{res2}}{dt} = \frac{v_{ac} - L_m N \frac{di_{res1}}{dt} + L_{oM} \frac{di_{res(M-1)2}}{dt}}{L_m \left(N\right)^2 - L_o} \tag{3.6}$$

As each module is coupled to their neighboring module, the secondary side of the neighboring modules output inductor is present. However, it can be understood that the neighboring modules output inductor is essentially in series with output inductor of the module under question. Assuming all modules are designed to be the same, if the output inductance is set to be half that of the converter discussed in Chapter 2, the same equation is obtained (3.7) where the relative operating frequency is provided in (3.8) and the characteristic impedance is provided in (3.9).

$$v_{cr} = v_{cr}(t_0)\cos(\omega_o t) + i_{res}(t_0) Z \sin(\omega_o t) + V\left(1 - \cos(\omega_o t)\right) \tag{3.7}$$

$$\omega_o = \frac{1}{\sqrt{L_{eq} C_{rM}}} \tag{3.8}$$

$$Z = \sqrt{\frac{L_{eq}}{C_{rM}}} = \frac{1}{\omega_o C_{rM}} \tag{3.9}$$

3.4.4 AVQ Voltage Stress

The peak voltage across the AVQ diodes are directly related to the voltage across the AVQ capacitors. Figure 3-15(a) shows the AVQ of a single module during the scenario when the switch is active. The switch current flows through the diode D_{RM4} which results in the other three diodes being inactive. The positive node and negative node of diode D_{RM1} is connected to the positive and negative node of the capacitor C_{oM1} resulting in (3.10) The same is seen for D_{RM3} whose positive and negative nodes are connected to the positive and negative nodes of capacitor C_{oM1} resulting in (3.11).

$$v_{DrM1} = v_{CoM1} \tag{3.10}$$

$$v_{DrM3} = v_{CoM3} \tag{3.11}$$

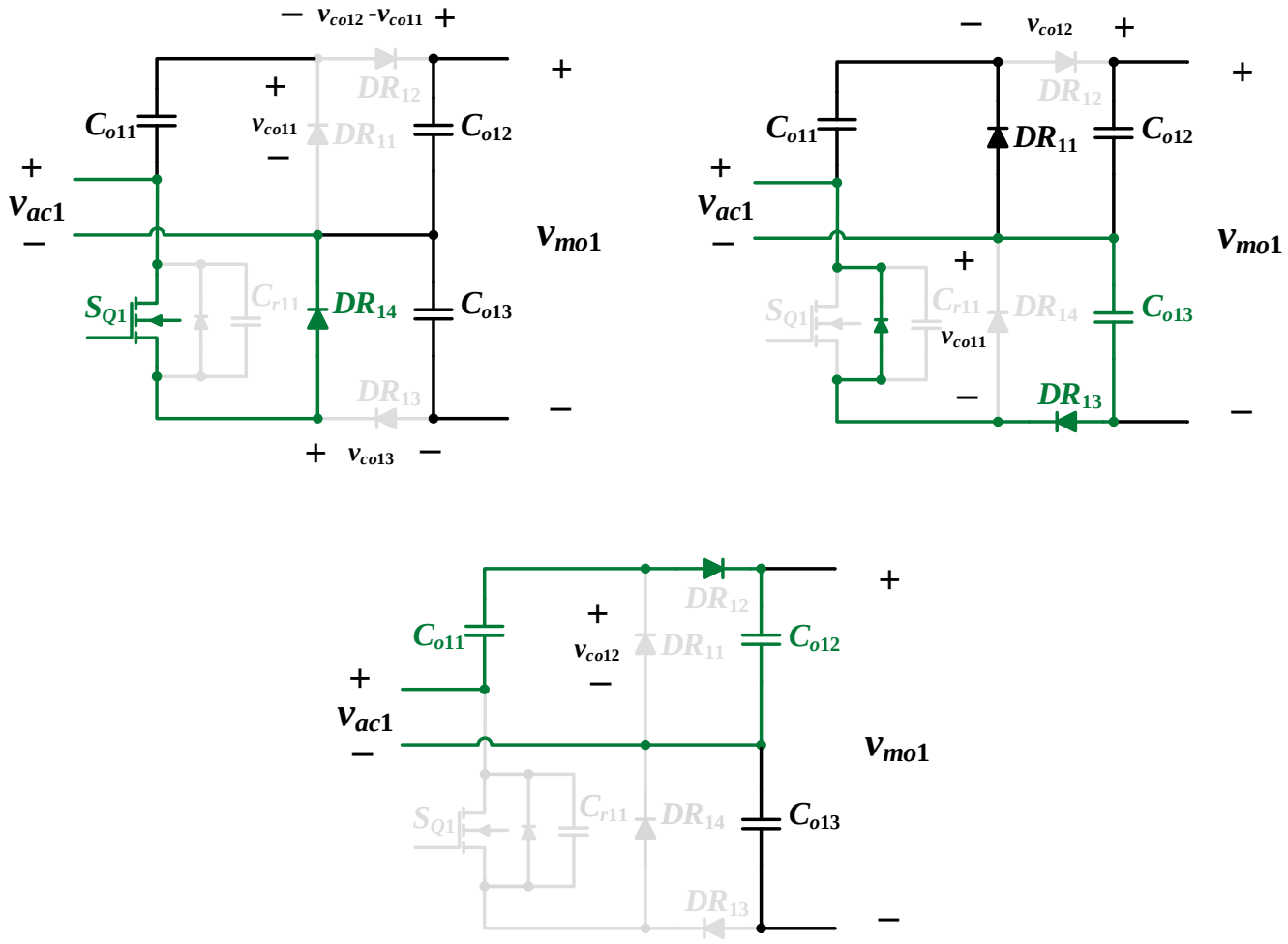


Figure 3-15: AVQ operation when (a) switch is active, (b) anti-parallel diode is active, (c) switch is off

In the case of D_{RM2}, the voltage across it is the difference between the voltage across the capacitors C_{oM2} and C_{oM1} which results in (3.12). These values are not necessarily the peak voltage across the switch as there are two other operating conditions for the AVQ.

$$v_{DrM2} = v_{CoM2} - v_{CoM1} \tag{3.12}$$

Figure 3-15(b) shows the AVQ of a single module during the scenario when the switch in active and the current is flowing through the anti-parallel diode of the switch. This scenario is also the same as when the current is charging the AVQ switch capacitor. The diode D_{RM4} is connected across C_{oM1} through D_{RM1} which results in (3.13). During this condition, due to D_{RM1} being active the voltage across D_{RM2} is now (3.14).

$$v_{DrM4} = v_{CoM1} \tag{3.13}$$

$$v_{DrM2} = v_{CoM2} \tag{3.14}$$

Figure 3-15(c) shows the AVQ of a single module during the scenario when the switch in active and the current is flowing through the anti-parallel diode of the switch. In this scenario, the output capacitor C_{oM2} is directly connected across the diode D_{RM1} which results in (3.15)

$$v_{DrM1} = v_{CoM2} \tag{3.15}$$

From here the peak voltage across the AVQ diodes are summarized in (3.16) and (3.17).

$$v_{DrM1max} = v_{DrM2max} = v_{CoM2} \tag{3.16}$$

$$v_{DrM3max} = v_{DrM4max} = v_{CoM1} \tag{3.17}$$

The average voltage across the AVQ diodes are also a function of the output capacitors and are listed in (3.18) and (3.19).

$$v_{DRM1avg} + v_{DRM2avg} = v_{CoM2} \tag{3.18}$$

$$v_{DRM3avg} + v_{DRM4avg} = v_{CoM3} \tag{3.19}$$

The two output capacitors of the AVQ sum up to the output voltage, however this voltage is not distributed equally across the capacitors. In the scenario that the AVQ switch and diodes

D_{RM1} and D_{RM3} are active, the capacitors C_{oM1} and C_{oM3} are in parallel which leads to the following relationship (22).

$$v_{coM1} = v_{coM3} \tag{3.20}$$

The total active time for the diodes is a function of the secondary side resonant current. The AVQ switch's gate signal is removed during the scenario where the secondary side resonant current is positive, which results in the current charging the resonant capacitor and increasing SQM's voltage to its maximum. During this condition, which is shown in Figure 3-15(b), the diodes D_{RM1} and D_{RM3} are active, which results in the SQM being in parallel with the capacitors C_{oM1} and C_{oM2} and leads to the following relationships.

$$v_{sQM\max} = v_{CoM2} - v_{CoM1} \tag{3.21}$$

$$v_{moM} = v_{CoM2} + v_{CoM3} \tag{3.22}$$

$$v_{coM2} > \frac{v_{moM}}{2} > v_{coM1} \tag{3.23}$$

The relationship between the output capacitors C_{oM2} and C_{oM3} are provided below where 'a' is the time period in which the resonant capacitor is charged and 'b' is the time period in which the secondary side resonant current is greater than zero.

$$v_{coM2} = v_{coM3}\frac{a+b}{a} \tag{3.24}$$

3.4.5 Voltage Gain

The voltage gain of a single module can be obtained by analyzing the converter in three sections which are the integrated boost, the *CLL* resonant circuit, and the active voltage quadrupler. The integrated boost stage is the same as the topology discussed in Chapter 2 and was provided in (2.7). The resonant stage of a single module is different from the topology discussed in Chapter 2 due to the presence of the neighboring modules output inductor on the secondary side of the modules resonant circuit as seen in Figure 3-16(a). The rectifier has been modified from a VQ to an AVQ as also seen in Figure 3-16(a). The gain of the AVQ varies based on duty-ratio of the

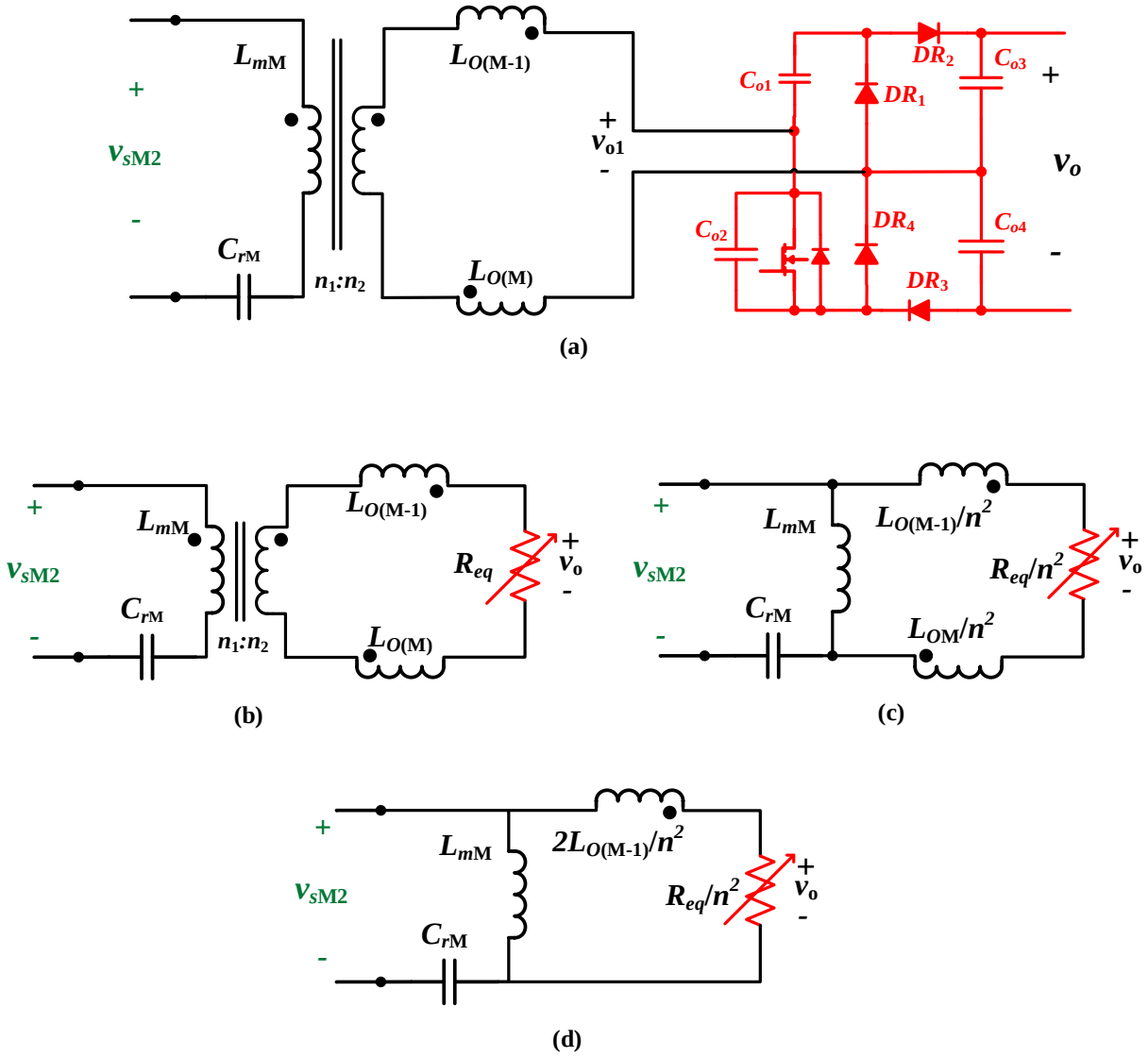


Figure 3-16 Topology of the (a) Modular *CLL* resonant circuit with AVQ (b) *CLL* resonant circuit with VQ represented as an equivalent resistance, (c) *CLL* resonant circuit referred to the primary side

AVQ's switch. Therefore, the AVQ can be replaced with an equivalent variable resistor R_{eq} as seen in Figure 3-16(b). From here the secondary side can be referred through the primary side as seen in Figure 3-16(c). As the current through both output inductors are the same, they can be combined together into one equivalent inductor as seen in Figure 3-16(d). The final equivalent circuit shown in Figure 3-16 (d) is in the same configuration as the equivalent circuit shown in Figure 2-9(c). Therefore, solving for the resonant circuit voltage gain of one module would result in the same equation (3.25) where Q is the quality factor (3.26), k is the ratio between the magnetizing inductance and the sum of the output inductance (3.27), and ω_n is the relative operating frequency provided in (3.8). The equivalent resistance in (3.26) is once again a function of the magnetizing inductance and the sum of the output inductance (3.28).

$$\left|\frac{v_{o1}}{v_{s2}}\right| = \frac{1}{\sqrt{\left(1-\frac{k}{\omega_n^{\,2}\left(k+1\right)}\right)^2+\left(\frac{Q}{\omega_n}\left(1+k-\omega_n^{\,2}\left(k+1\right)\right)\right)^2}} \tag{3.25}$$

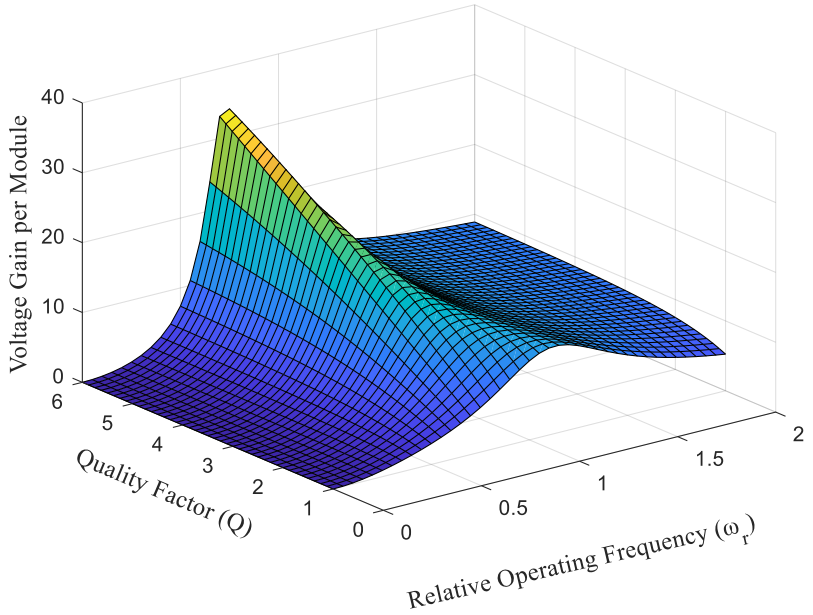
$$Q = \frac{\omega_o \times L_{eq}}{R_{eq}} \tag{3.26}$$

$$k = \frac{L_{o\mathrm{M}} \times n^2}{L_{m\mathrm{M}}} \tag{3.27}$$

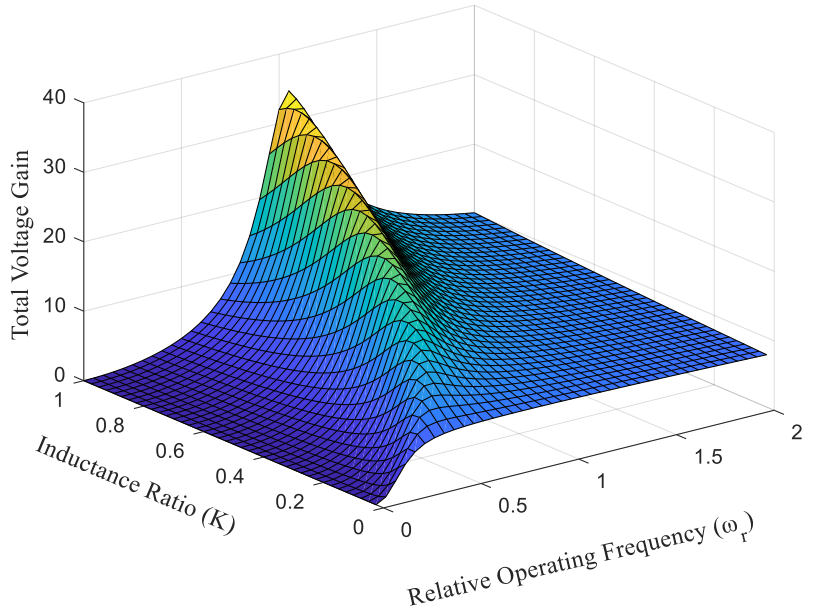
$$L_{eq} = \frac{L_{o\mathrm{M}} L_{m\mathrm{M}}}{L_{m\mathrm{M}} n^2 + L_{o\mathrm{M}}} \tag{3.28}$$

It should be noted that the equivalent resistance provided in (3.26) varies based on the duty-ratio of the AVQ switch. We can then solve for the gain of a single module by factoring in the gain from the boost stage (3.29). A 3D plot of this gain as a function of the relative operating frequency and quality factor is provided in Figure 3-17(a) for a fixed "k" and duty-ratio while the gain as a function of relative operating frequency and inductance ratio is provided in Figure 3-17(b) for a fixed "Q" and duty-ratio.

$$\left|\frac{v_{o1}}{v_{pv}}\right| = \left|\frac{v_{s2}}{v_{pv}}\right| \times \left|\frac{v_{o1}}{v_{s2}}\right| = \frac{\sqrt{2}}{\pi\left(1-d_{\mathrm{M}}\right)} \frac{\sqrt{1-\cos\left(2\pi d_{\mathrm{M}}\right)}}{\sqrt{\left(1-\frac{k}{\omega_n^{\,2}\left(k+1\right)}\right)^2+\left(\frac{Q}{\omega_n}\left(1+k-\omega_n^{\,2}\left(k+1\right)\right)\right)^2}} \tag{3.29}$$



(a)



(b)

Figure 3-17: Gain of a single module of the proposed system as a function of (a) ω_r and Q for $k = 0.5$, ω_r and k for $Q = 3$

3.5 Simulation Results

To confirm the performance of the proposed modular HF interlinking system, a 10kW, three module DC-DC converter system was developed in the circuit simulation software Powersim (PSIM). Each module consisted of the components shown in Figure 3-5 with their output inductors coupled to their neighboring module. At the input of each module were PV arrays connected in series and parallel to achieve 3.3kW at maximum light intensity. The single-sensor based MPPT algorithm discussed in Chapter 2 was employed such that each module would operate at their maximum power under all conditions. Table 3-1 shows detailed information in regards to the operating conditions and components utilized per module.

Table 3-1 Simulation and Prototype Parameters

General Parameters		
	Full Scale Simulation	**Prototype**
Generated Power	13kW	500W
DC-Grid/Output Voltage	10kV	850V
Number of Modules	3	2
Number of Panels per String	8-14	2-4
Number of Strings	2	1
PV Voltage Range (per module)	300 - 700V	55 - 110V
Gain Range (per module)	5 - 10	7 - 10
System Operating Frequency	140kHz	170kHz
System MPP Duty Range	30% - 70%	30% - 70%

Converter Specifications		
	Full Scale Simulation	**Prototype**
Input Inductance	100µH	100µH
Magnetizing Inductance	900µH	490µH
Turns-Ratio	2:3	2:3
Output Inductance	75µH	47µH
Input Capacitance	10µF	5µF
Resonant Capacitance	150nF	150nF
Output Capacitance	10µF x4	5µF x4
MOSFET Switch	G3R160MT17D	SCT3030AW7TL
Power Diode	GD05MPS17H	MURS360BT3G
DSP Controller	-	TMSF28335

The output of each module was connected in series to reach the chosen DC-grid voltage level of 10kV and the designed power balance controller was employed to ensure balanced output voltage in all scenarios. The total operating power was 10kW while the number of modules was three. Seven PV panels were connected together in series to form a string and from here two strings were connected in parallel to form the PV array. Three sets of these PV arrays were used, one per module. Due to the higher voltage and power level compared to the simulation performed in Chapter 2, several of the converter parameters had to be modified to ensure the desired operation was maintained. An operating frequency of 140kHz was chosen for all module switches. The ratio between the magnetizing inductance and output inductance, *k*, impacts resonant current and in turn the system efficiency. A larger *k* allows for a higher efficiency while a small output inductance increases the voltage balancing range. The resonant components were modified to be 900µH and 150nF for the magnetizing inductance and capacitance respectively. The turns ratio of the coupled inductor was set to 2:3. The output inductance was set to 75µH and a turns-ratio of 1:1 was chosen.

To confirm the accuracy of the proposed power balancing topology as well as the previously discussed single-sensor maximum power extraction technique, the system was tested with and without the power balancer. The light intensity seen by the PV arrays of each module were varied between 500W/m^2 and 1000W/m^2 while the power balance controller was inactive. Figure 3-18(a)-(c) shows the theoretical maximum and operating PV power of each module respectively. At 0.1s the light intensity of M_1 was increased from 700W/m^2 to 900W/m^2 while at

Figure 3-18: Simulation waveforms with inactive power balance controller: Maximum and Operating power of (a) M_1, (b) M_2, (c) M_3, (d) output voltage per module.

0.15s the light intensity of M_2 was decreased from 900W/m^2 to 500W/m^2. Finally, at 0.2s the light intensity of M_3 was increased from 500W/m^2 to 1000W/m^2. It can be observed that each module operated at their maximum value at all conditions. It should be noted that M_1 and M_2 can be seen to diverge from the MPP during scenarios where other modules power levels changed. This is expected as the equivalent resistance seen by each module's input panel changes, and hence the required duty-ratio to operate at the MPP is different. As the module eventually reach back to their respective MPP, it can be understood that the single-sensor MPPT controller from Chapter 2 is

Figure 3-19 Simulation waveforms with the power balance controller: Maximum and Operating power of (a) M1, (b) M2, (c) M3, (d) output voltage per module.

functional with the proposed system. Each module's output voltage is shown in Figure 3-18(d) which are seen to be unbalanced in all conditions with the higher power modules operating with a larger output voltage. It should be noted that during 0.1s < t < 0.15s M_1 and M_2's output voltage is the same, which makes sense as they operate at the same power level during this time period. The same can be seen for M_2 and M_3's output voltage during the time period 0.15s < t < 0.2s. Unbalanced output voltage is expected as the system's power balance controller is inactive for this test.

The same test was then performed with the power balance controller active. The operating PV power is provided in Figure 3-19(a-c) during this condition, and it is evident that all modules

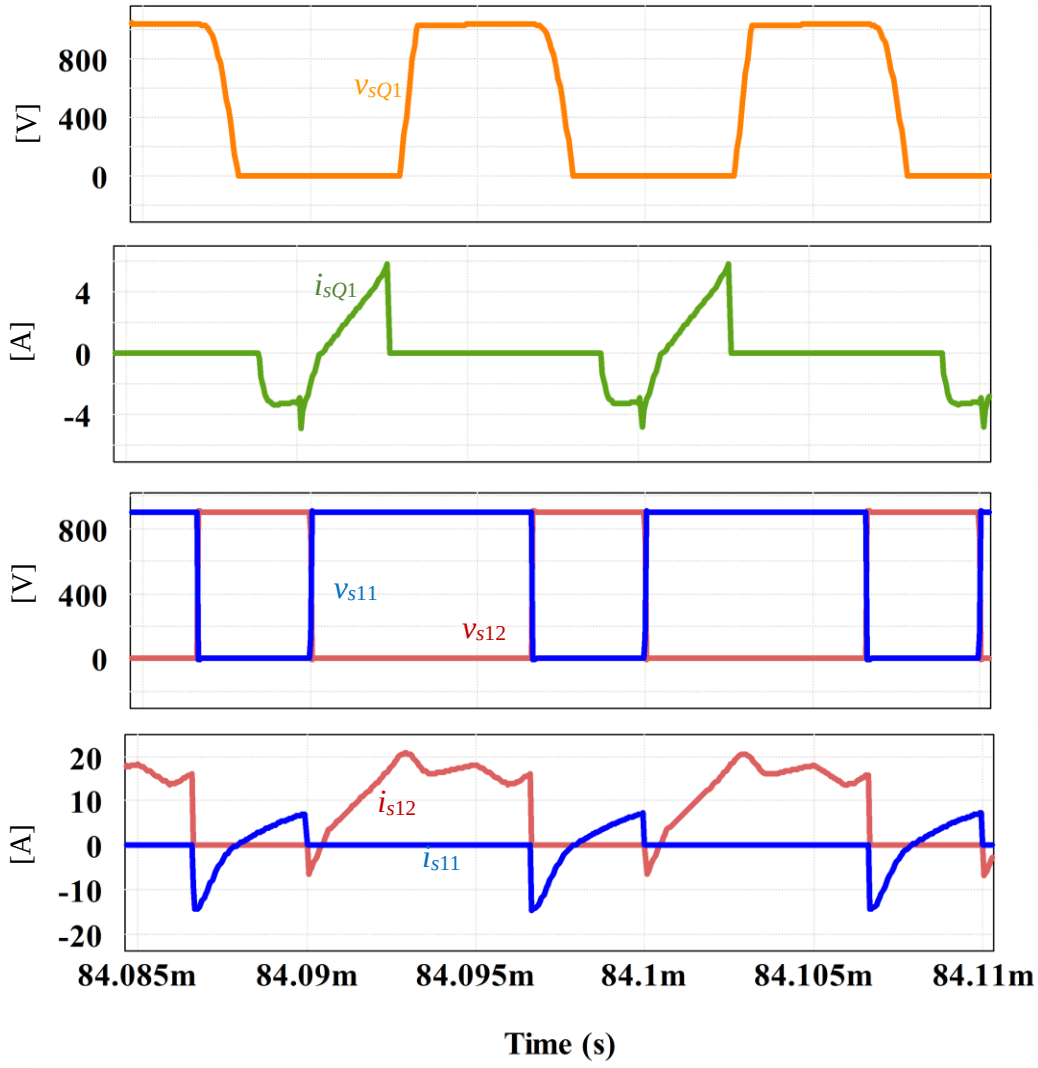


Figure 3-20 M_1 operating waveforms (a) AVQ switch voltage, (b) AVQ switch current, (c) input switch voltage, (d) input switch current

operated at their respective MPP. Figure 3-19(d) shows the individual module output voltages in this condition which are seen to be approximately equal to each other. This confirms that the proposed modular structure allowed for power balancing during power mismatch scenarios without impacting the maximum power operation of each individual module's PV array.

Figure 3-20(a)-(d) to Figure 3-22(a)-(d) shows the operating switch voltage and current waveforms for each module during the first scenario where M_2 operated at the highest power level while M_3 operated at the lowest power level. It can be observed that soft-switching was achieved for all switches in all scenarios as when the switch current transitioned from negative to positive, the voltage across the switch was zero. Further, the higher power module is seen to operate at a

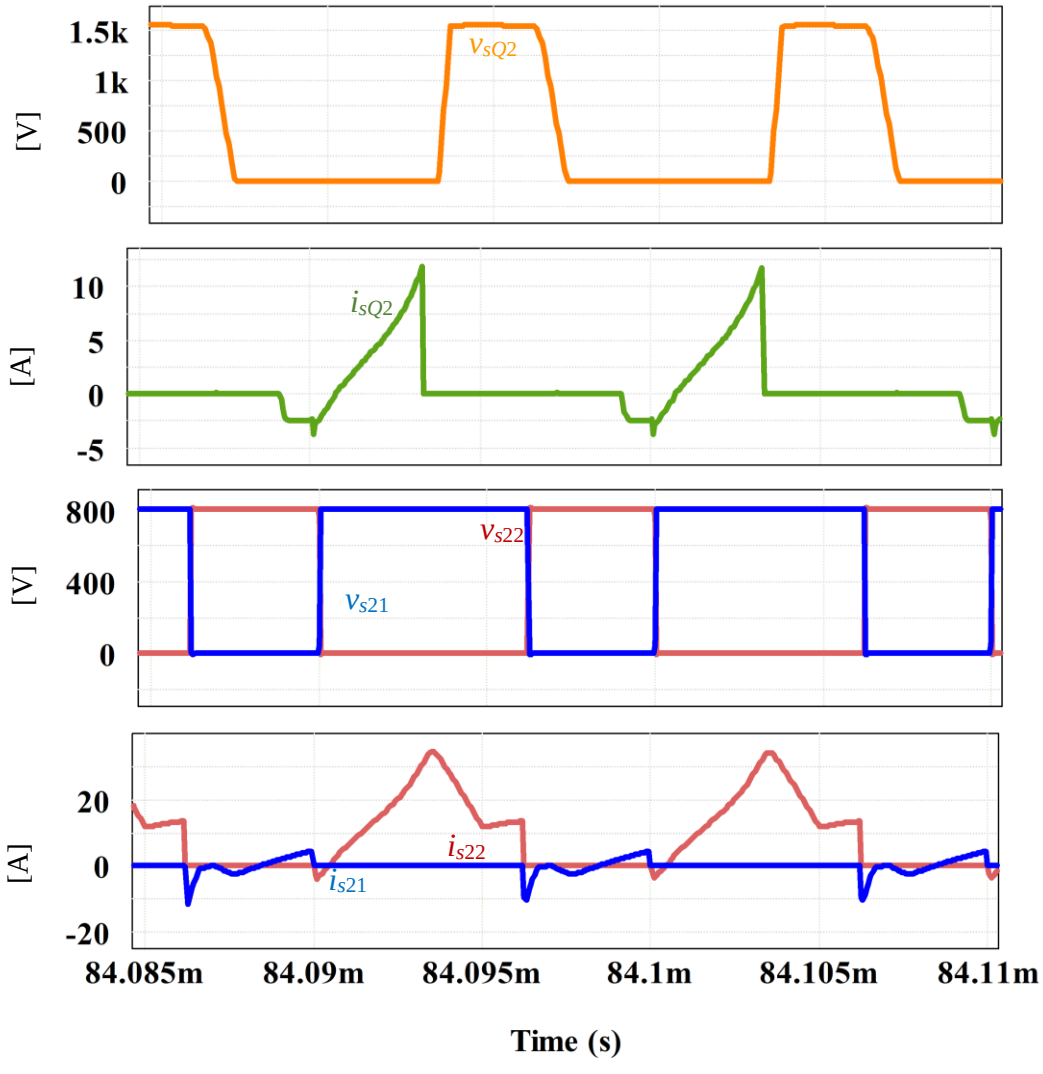


Figure 3-21 M_2 operating waveforms (a) AVQ switch voltage, (b) AVQ switch current, (c) input switch voltage, (d) input switch current.

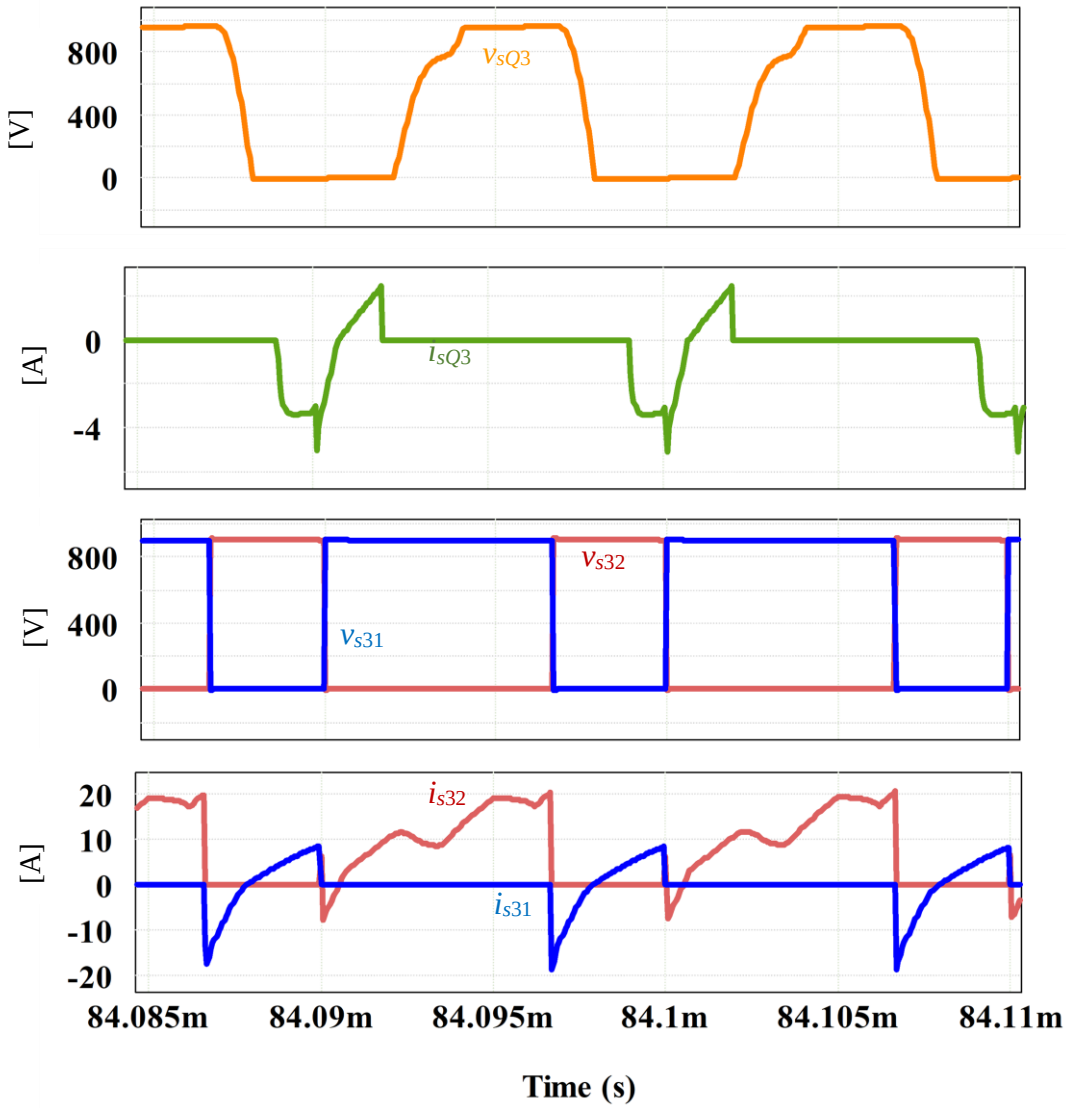


Figure 3-22: M_3 operating waveforms (a) AVQ switch voltage, (b) AVQ switch current, (c) input switch voltage, (d) input switch current.

lower duty-ratio than the lower power modules, which is expected due to the MPPT duty-ratio controller. From the AVQ switch voltage and current waveforms of each module it is observed that the higher power module operated with a higher duty-ratio compared to lower power modules to allow for power transfer between modules.

In the simulation results shown in Figure 3-18 to Figure 3-22, all PV arrays were set to receive solar intensity and generate power. In Figure 3-2 it was mentioned that by coupling the modules before the final step-up stage, the system can achieve a balanced output voltage and regulate power flow in scenarios of severe power mismatch or cases where PV arrays are not functioning. To confirm this an additional simulation was performed shown in Figure 3-23 using different operating conditions compared to Figure 3-18. Figure 3-23(a)-(c) contain the operating power and the ideal maximum power of each PV array which once again confirms the functionally of the single-sensor MPP algorithm. Figure 3-23(d) shows the output voltage of each module when the voltage balance controller is inactive. At [t = 2s] M_1's PV array became inactive which resulted in an input power drop from 1.5kW to 0W. This was followed by a significant voltage imbalance across all modules. The voltage across M_2 and M_3 are almost 150% over their rated value which could lead to damaged converter components. Figure 3-23(e) shows the modular output voltage when the voltage balancer is active. Under all conditions the system is able to achieve balanced output voltage, including the case where M_1's PV array was inactive. It can be seen that the time taken to balance the output voltage was a few milliseconds longer than the unbalanced conditions shown at [t = 0.1s] and [t = 0.15s]. This is expected as the power level drop was larger than these conditions.

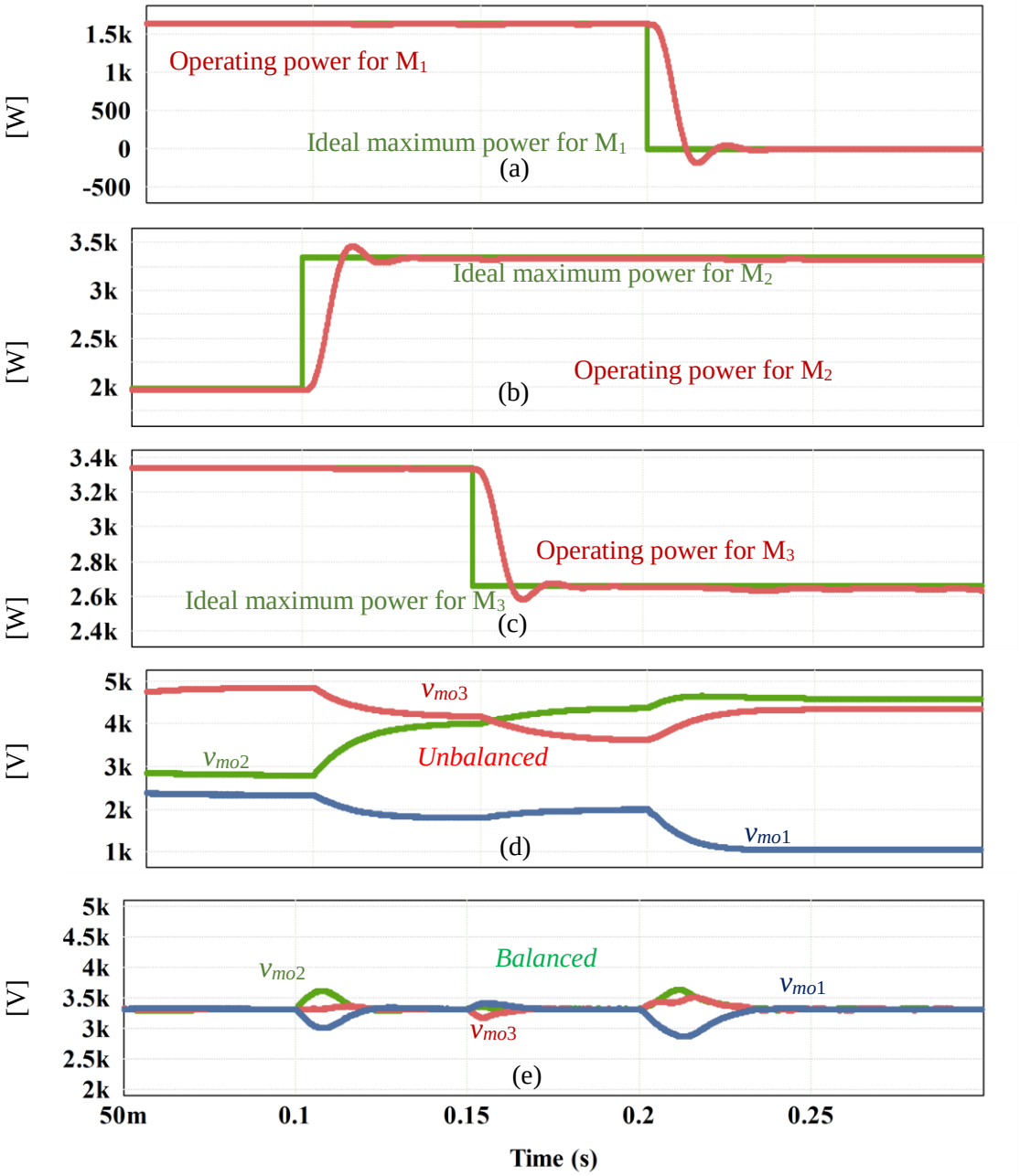
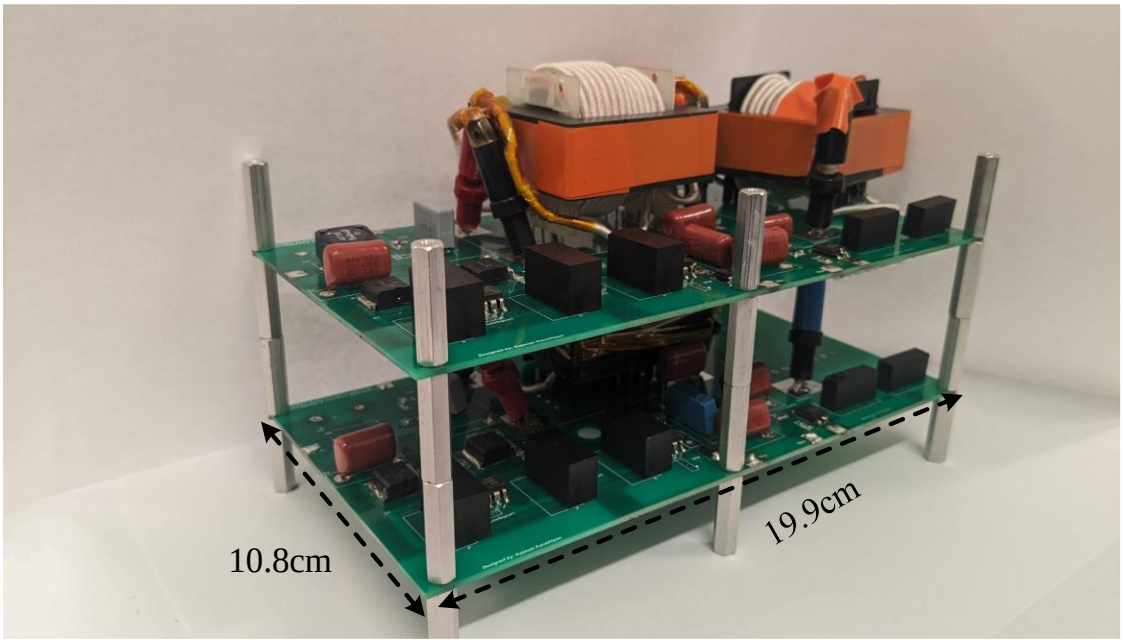


Figure 3-23 Simulation waveforms with the power balance controller: Maximum and Operating power of (a) M1, (b) M2, (c) M3, (d) output voltage per module under unbalanced condition, (e) output voltage per module under balanced condition.

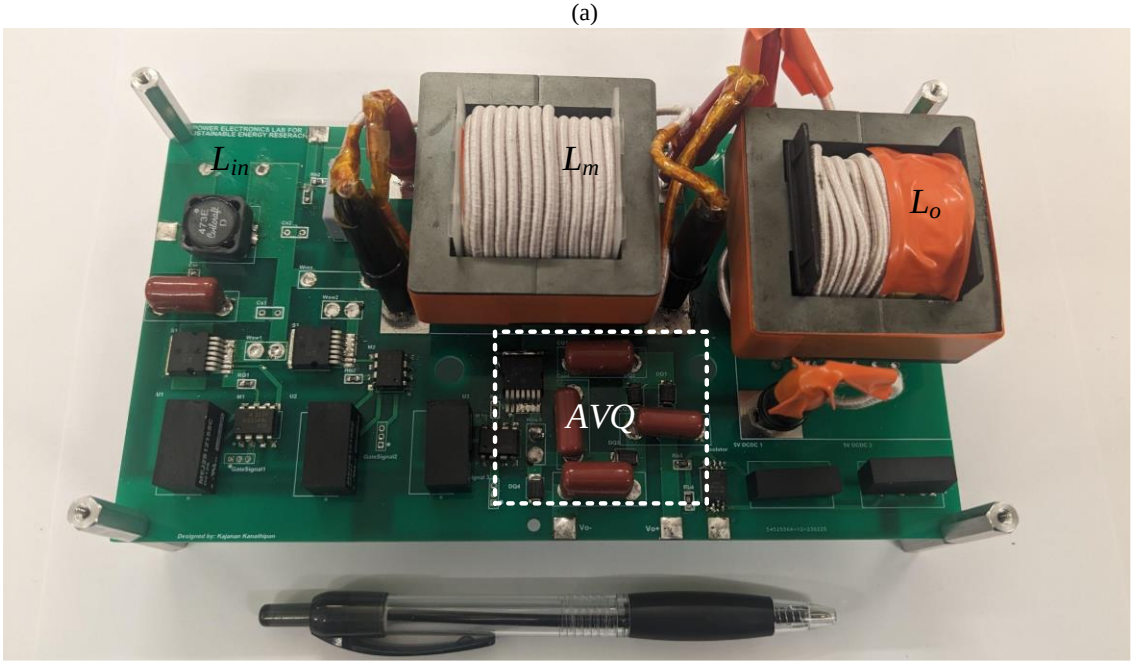
3.6 Experimental Results

In order to confirm the feasibility of the proposed system, a scaled-down proof-of-concept hardware prototype consisting of two modules was constructed. Figure 3-24(a) shows the hardware prototypes and dimensions while Figure 3-24 (b) shows the top view of a single module. Each module was approximately 19.9 x 10.8 x 2.7 cm^3 which lead to a power density of 8.51W/cm^3. Details of the parameters and utilized components are provided in Table 3-1.

In order to operate with a high voltage gain, a quality factor and inductance ratio of 3 and 0.2 were chosen respectively. An operating frequency of 170kHz was also chosen. By substituting (3.26) into the left-hand-side of (3.27) and (3.28) into the right-hand side, the magnetizing and output inductance was obtained. From here, (3.8) was used to obtain the resonant capacitance. The chosen values of the magnetizing inductance and output inductance were 490μH and 47μH respectively while the resonant capacitance was determined to be 150nF. A ferrite core with N87 material from TDK was selected for both the coupled inductors along with 1000 strands of AWG44 Litz wire. For the magnetizing inductance, approximately nine turns and fourteen turns were used for the primary and secondary side respectively to obtain a ratio of 2:3. For the output inductance, approximately seven turns were used for both the primary and secondary winding. The SCT3030AW7TL SiC power MOSFET and the MURS360BT3G power rectifier were chosen for the modules switches and diodes respectively.



(a)



(b)

Figure 3-24(a) Designed two module proof-of-concept prototype (b) single module components and dimension.

To confirm the operation of the voltage balancer and its independence from the single-sensor MPP controller, two modules with different operating power were employed. Two channels of the Keysight E4360A Solar Emulator were independently connected to the input of each module and were set to have a maximum power of 250W and 130W respectively. The output voltage of each module (v_{mo1} and v_{mo2}), the total output voltage (v_o), as well the current through switch S_{12} (i_{s12}) are shown in Figure 3-25 during unbalanced and balanced condition. The power mismatch resulted in an output voltage unbalance between the two modules as shown on the left-hand side of Figure 3-25 where the module output voltage was 535V and 320V respectively. From here, the voltage balancer was activated and it can be seen that the output voltage M_1 decreased to 427.5V while the output voltage of module M2 increased to 427.5V. A zoom-in of the waveforms during balanced condition is shown on the right side of Figure 3-25 which shows that M_2's input switch operated under soft-switching condition and had a peak current of 9.1A.

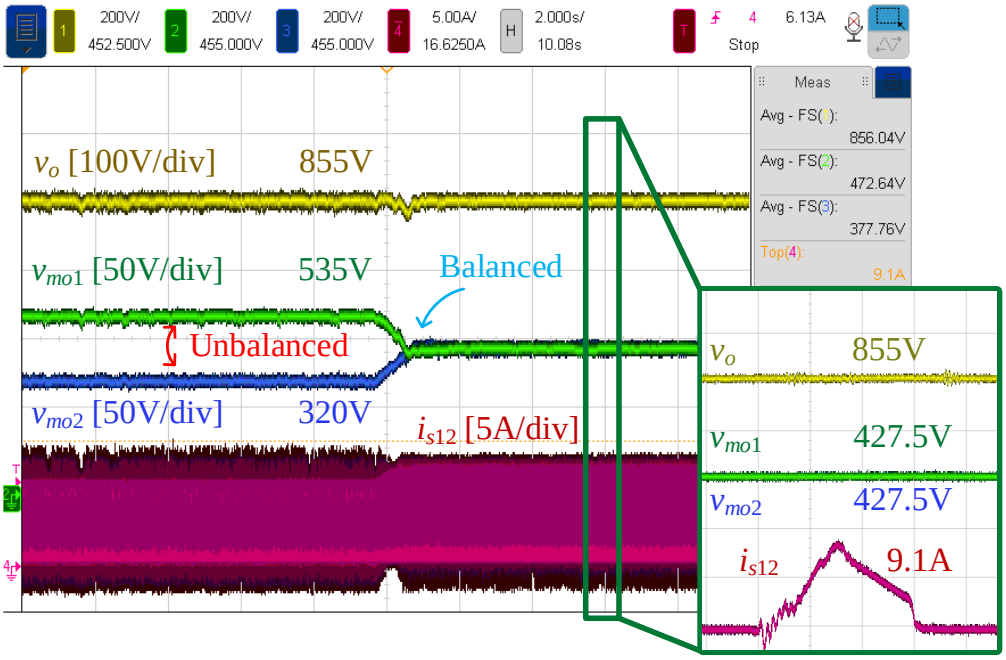
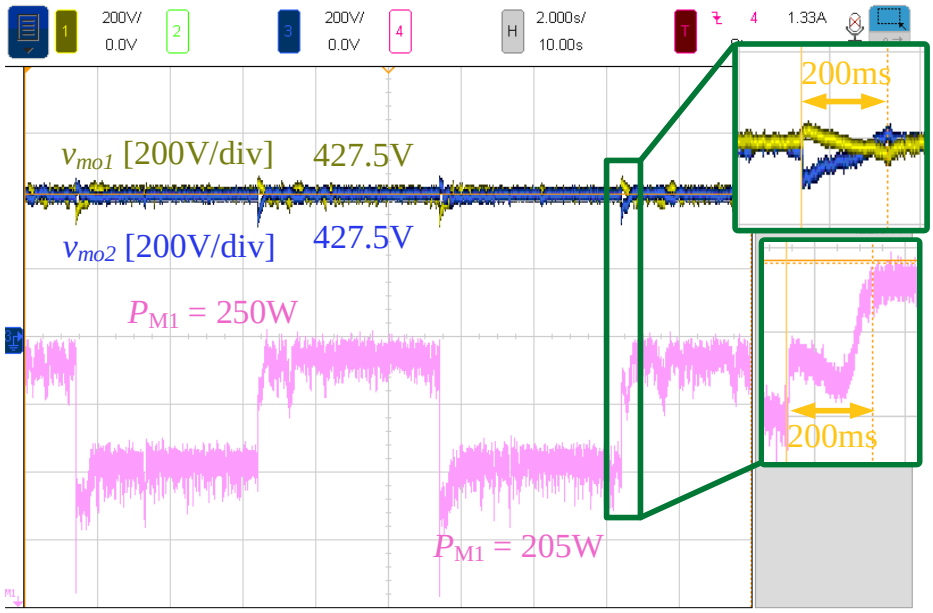
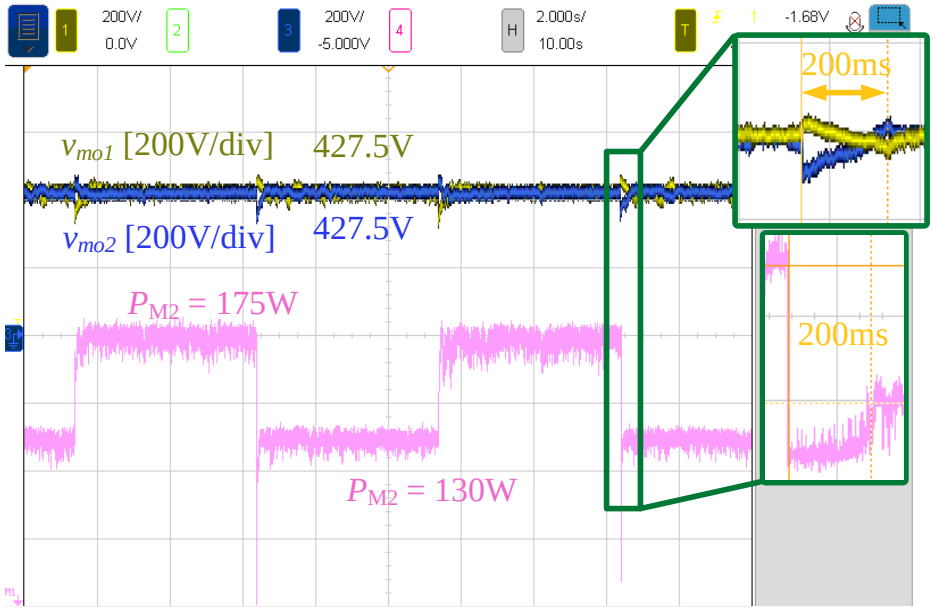


Figure 3-25 Experimental waveforms: unbalanced to balanced condition as well as a zoom-in of the balanced condition



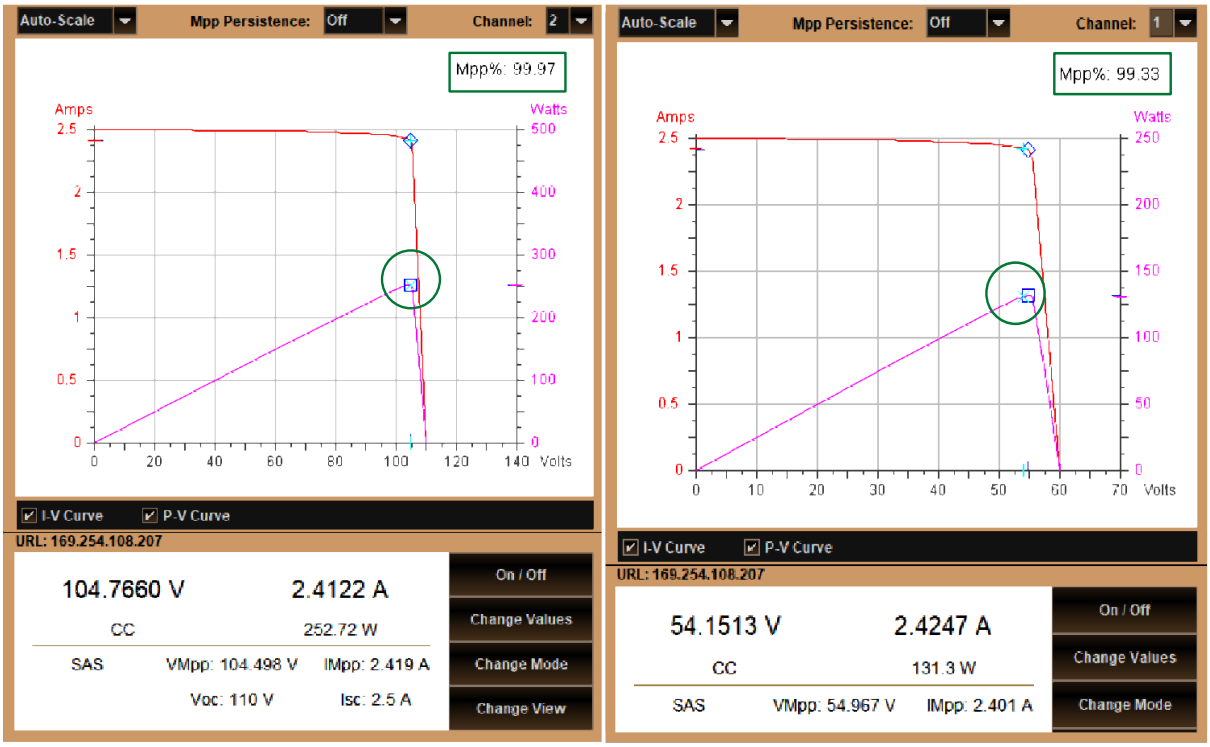
(a)



(b)

Figure 3-26: Experimental waveforms: Modular output voltage and input power of (a) M_1 (b) M_2

The modular output voltage as well as the input power of M_1 and M_2 are provided in Figure 3-26(a) and (b) respectively. In this condition, the proposed power balance controller and the designed single-sensor MPP controller were active. The operating power of M_1 would vary between 130W and 175W every 5 seconds while M_2 would vary between 250W and 205W within the same time frame. It is clear that the voltage balancer and single-sensor based MPPT controller operated simultaneously and independently to maintain balanced output voltage and the MPP for

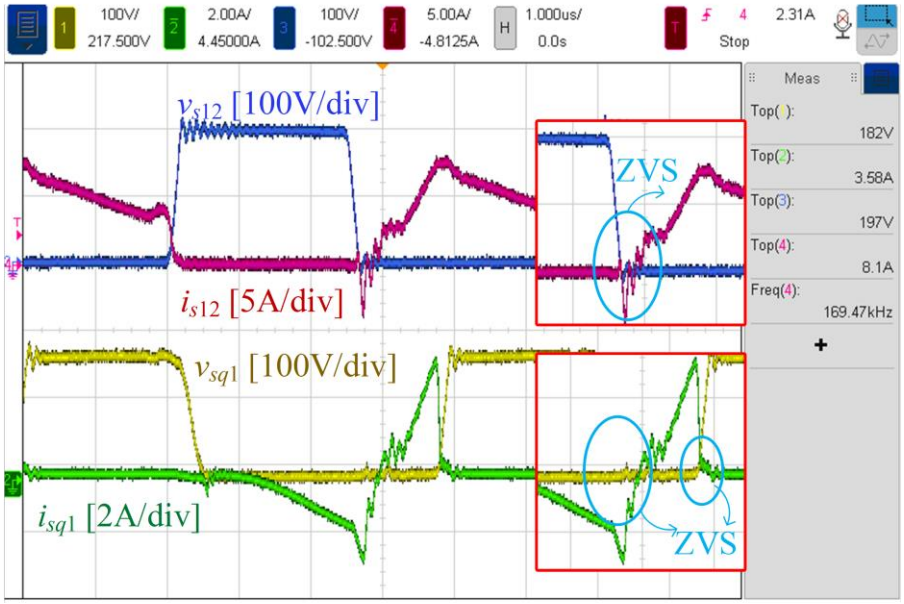


(a) (b)

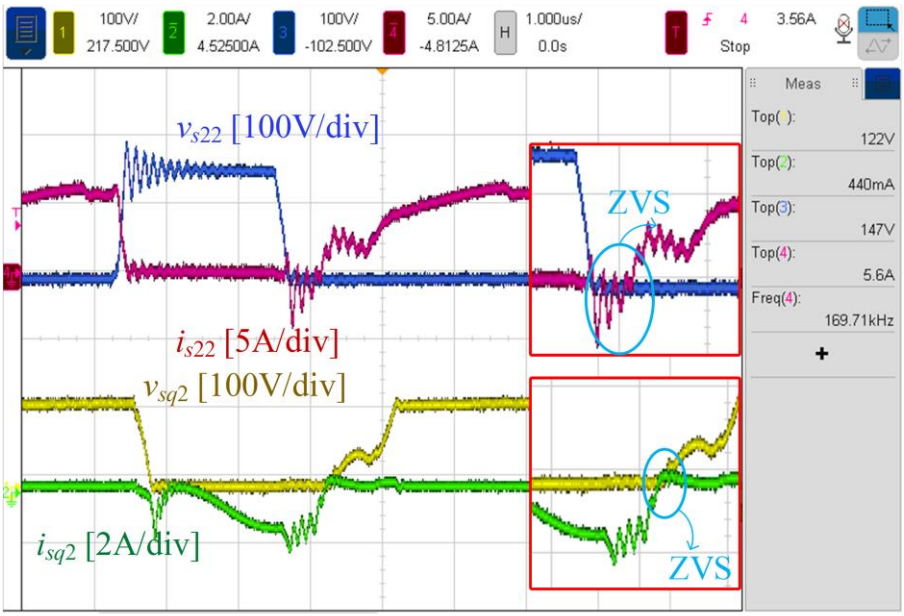
Figure 3-27 Experimental waveforms: MPP operation for (a) M_1 (b) M_2

each module while ensuring the voltage imbalanced did not exceed 10% of the rated value. In all scenarios the single-sensor MPPT controller brought the system to the new MPP within 200ms. The short spike in the power waveforms during the time-period where the power level changed is due to the Keysight probes connected to the oscilloscope and is not a concern.

Figure 3-27 shows the operating power-voltage curve and current-voltage curve as well as the percentage of maximum power extraction of both modules during the scenario shown in Figure 3-26 when M_1 operates at approximately 130W (a) while M_2 operates at approximately 250W (b). To emulate the power drop from 250W to 130W, the panel operating voltage decreased from 105V to 54V while the open-circuit voltage decreased from 110V to 60V. As the short-circuit current was kept constant in both cases, this represents a temperature increase similar to the example shown in Figure 1-12. Each module is seen to operate at over 99.9% of their respective MPP, further confirming the accuracy of the developed single-sensor based MPPT controller designed in Chapter 2.



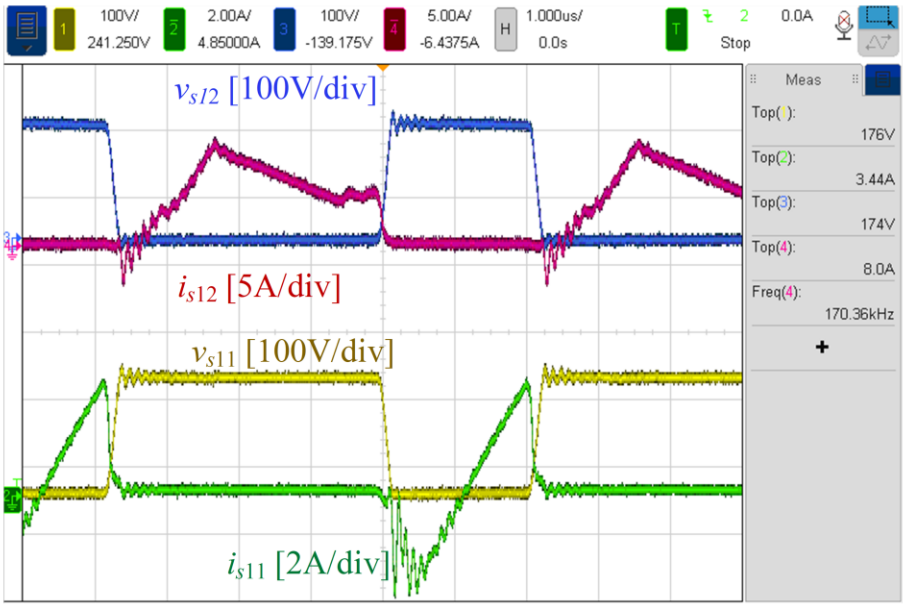
(a)



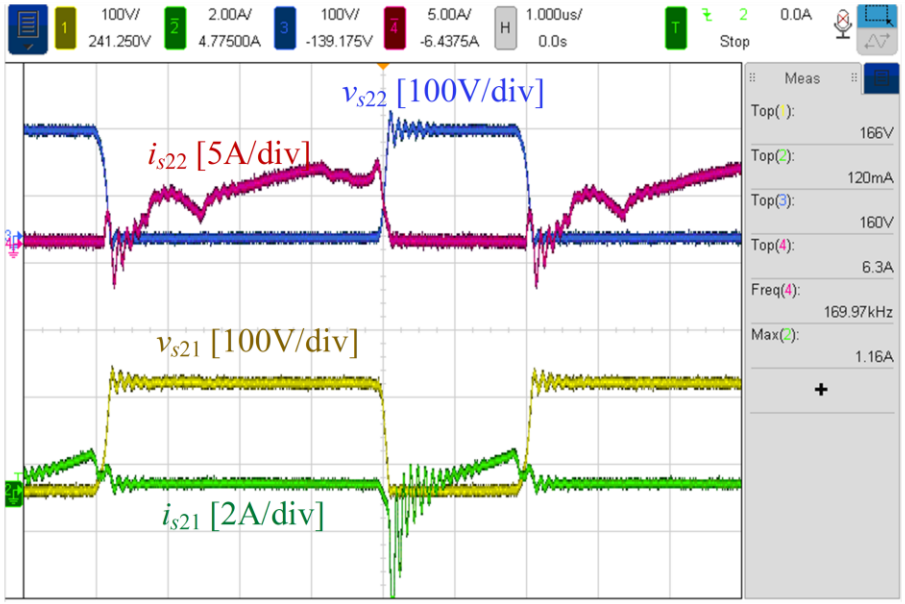
(b)

Figure 3-28 Experimental waveforms: Input switch SM2 and AVQ switch SQM voltage and current waveforms for (a) M1 (b) M2

Figure 3-28 shows the voltage and current across the switches S_{M2} and S_{QM} per module during the power mismatch scenario on the left-hand side of Figure 3-25. Figure 3-28(a) shows the waveforms of module M_1 which operated at 250W and it can be seen that both the input switch



(a)



(b)

Figure 3-29 Experimental waveforms: Input switch voltage and current waveforms for (a) M_2 (b) M_1

and the AVQ switch achieved ZVS turn-on operation. A zoom-in of these conditions are provided on the right-hand side Figure 3-28. Similarly, module M_2 is seen to have achieved ZVS turn-on for the displayed switches on the right-hand side of Figure 3-28(b). Figure 3-29 shows the voltage and current across both input switches for both modules during the same scenario. The results confirm ZVS turn-on operation for both modules input switches. A plot of the total system

efficiency as a function of each module's operating power is provided in Figure 3-30. It can be seen that the total system efficiency is the highest when the modules operate close to the same power level whereas the more unbalanced the PV power is the lower the system efficiency. This makes sense as the AVQ switch must be active for a longer period of time to transfer power during unbalanced scenarios which results in increased switch conduction loss.

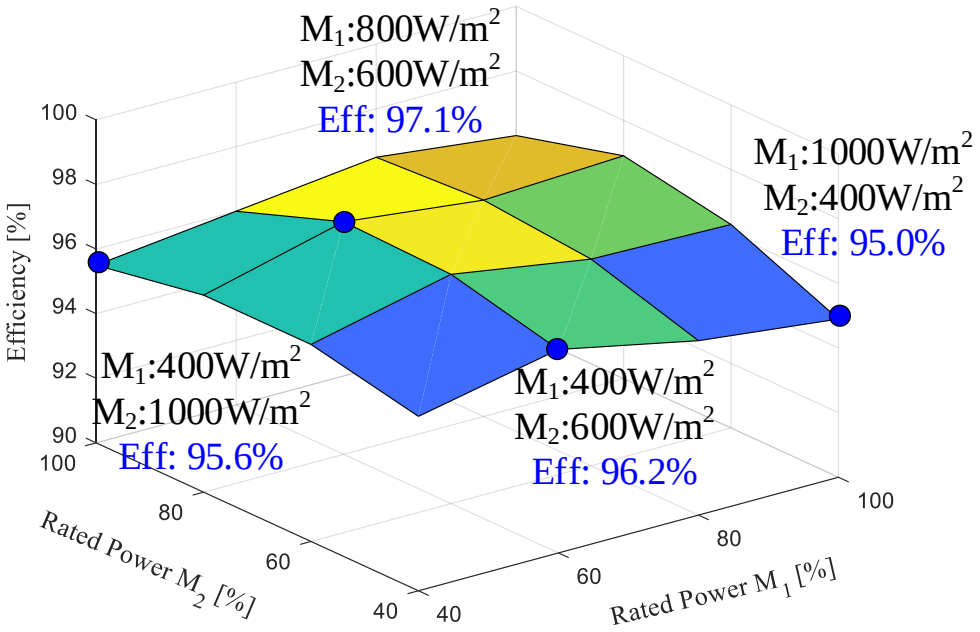


Figure 3-30 System efficiency at different operating power

Table 3-2 Three Module Prototype Parameters

General Parameters	Value
Total Generated Power	330W
DC-Grid/Output Voltage	750V
Number of Modules	3
Number of Panels per String	3
Number of Strings	1
Input Power Range (per module)	60-150W
Input Voltage Range (per module)	35-55V
System Operating Frequency	170kHz
System MPP Duty Range	30% - 70%

The previously discussed experimental tests were conducted with a two-module configuration. To further confirm the operation of the proposed system, a three-module configuration was tested. Modules M_1 and M_2 were connected to PV emulators while M_3 was connected to a DC-voltage source. Table 3-2 contains the experimental parameters while the component values of each module were the same as shown in Table 3-1. The total output voltage was to be 750V which implies the per-module output voltage was to be 250V. Figure 3-31 contains the per-module output voltage and the total output voltage during unbalanced and balanced condition. M_3's output voltage is seen to be only 100V, which implies M_1 and M_2 are over the expected value. It can be seen that the output voltage of M_2 was 370V which is almost 50% over the expected value. From here the balancer was activated and the voltage across all modules moved towards 250V. A zoom-in of the waveforms during balanced condition is shown on the right side of which confirms the operation of the integrated power balancer with three modules.

Figure 3-32 shows the voltage and current across the switches S_{M2} and S_{QM} per module during the balanced scenario on the right-hand side of Figure 3-31. It can be seen that all modules achieved soft-switching operation.

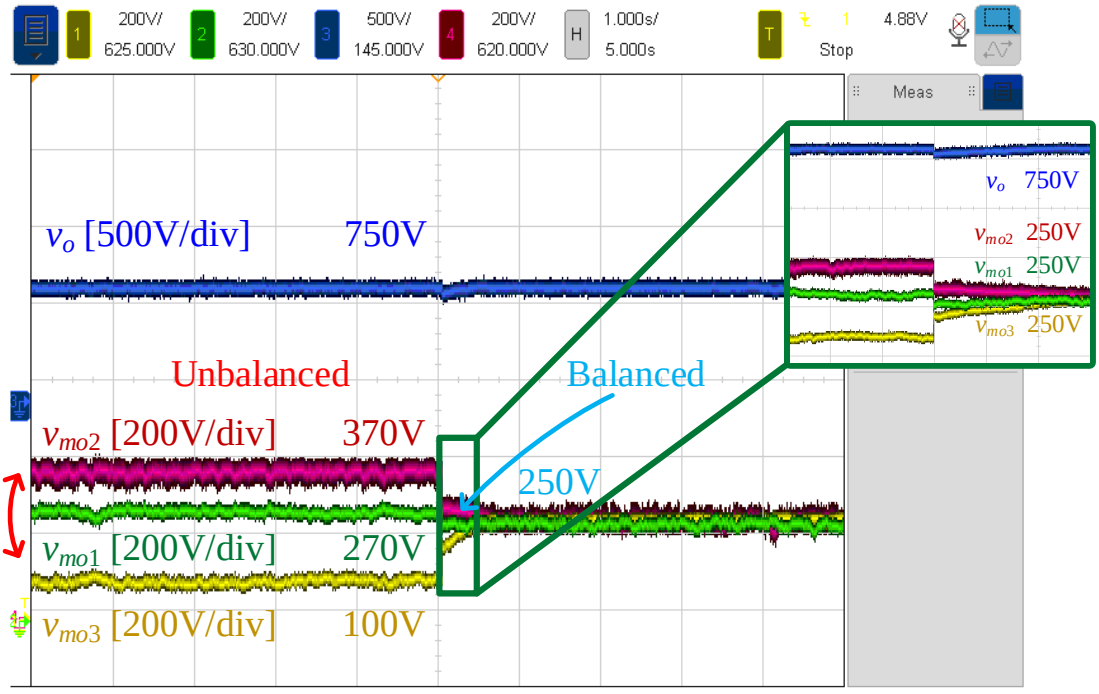
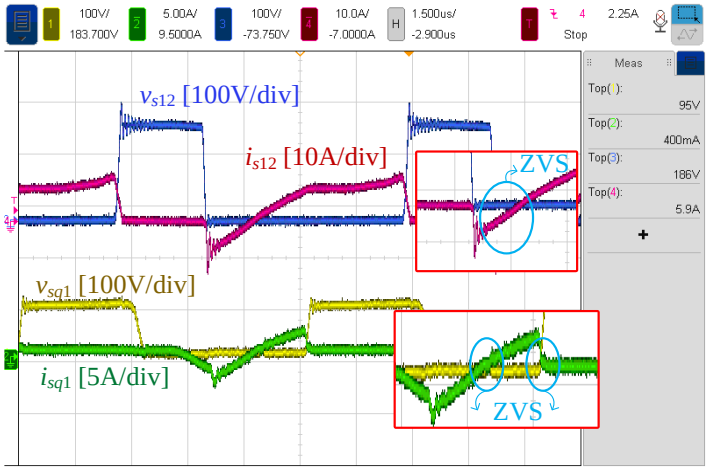


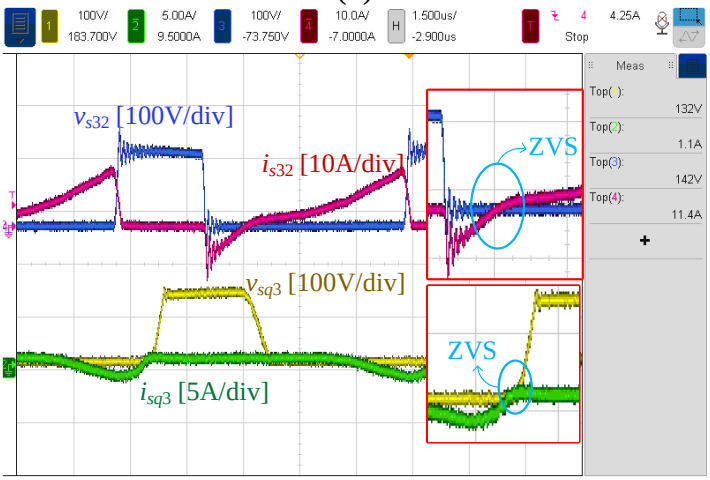
Figure 3-31: Experimental waveforms: unbalanced to balanced condition as well as a zoom-in of the balanced condition for a three-module system



(a)

ccc

(b)



(c)

Figure 3-32 Experimental waveforms: unbalanced to balanced condition as well as a zoom-in of the balanced condition for a three-module system

In order to confirm the systems functionality under conditions where one PV array is not functioning, the power level of module M3 was set to zero. Figure 3-33 contains the modular output voltage and the total output voltage during unbalanced and balanced scenarios. It can be seen that at the start of the experiment, the module voltages were unbalanced with M_2 having an output voltage of 330V whereas under a balanced condition it would be 250V. Halfway through the test the power balance controller was activated and it can be seen that the output voltage of each module was balanced at 250V even with the inactive M_3. This further confirms the system is able to safely function in the case of a failed PV module.

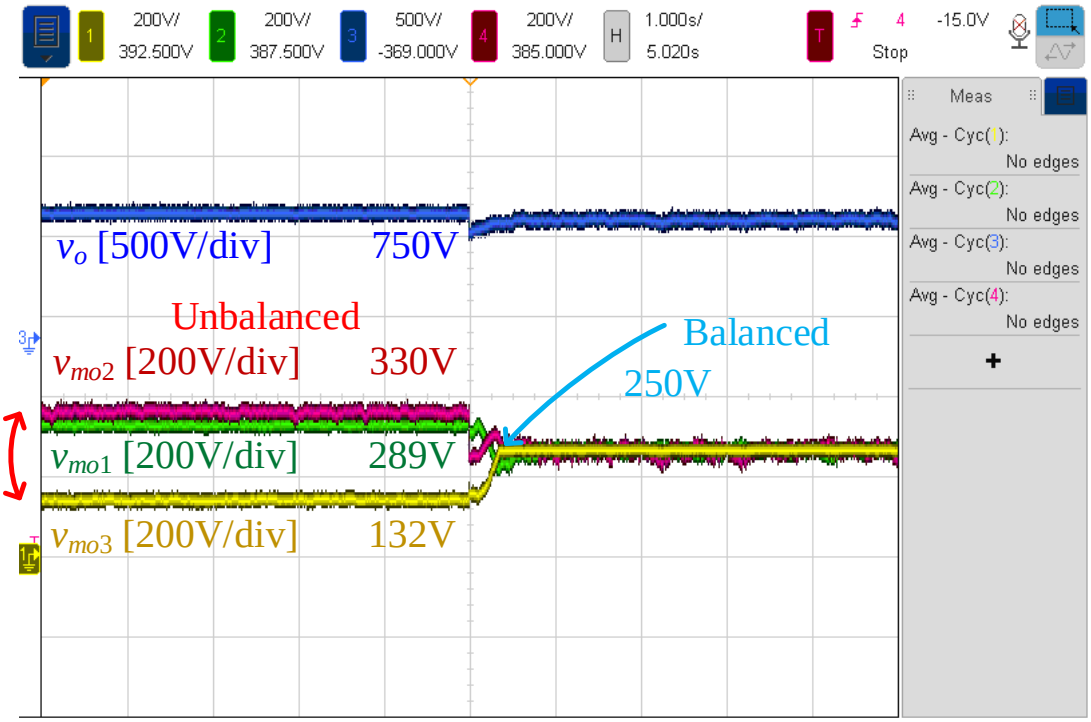


Figure 3-33 Experimental waveforms: unbalanced to balanced condition for a three-module system under a scenario with an inactive M_3

A comparison of the proposed modular topology to existing topologies is provided in Table 3-3. Topologies [60], [61], [63], [70], [71], and [72] utilize six switches per module, with two specifically for modular power transfer, and operate at a lower switching frequency compared to the proposed system which operates with half as many switches. These topologies achieve a gain between 1 and 4 per module whereas the proposed system can achieve a gain of close to 10 per module. Although topologies [61], [60] operates with a similar switching frequency and a high gain, they utilize several components which increases the size and cost of the system. Topology [73] utilizes a similar number of switches and magnetic components per module however this topology achieves a lower efficiency, lower gain, and operates at a lower switching frequency implying larger components values are required. From this table, it can be understood that the proposed topology achieved a higher peak efficiency and overall gain per module while operating at a higher switching frequency and utilizing fewer active switches.

Table 3-3 Comparison of Power and Voltage Sharing Topologies

Reference	**Rated System Power**		**Output Voltage**		**Operating Frequency**	**Gain**		**Voltage Stress (Max)**	**Module Component Count**			**Soft-Switching**	**Prototype Peak Efficiency**
	Simulation	Prototype	Simulation	Prototype		Simulation	Prototype		Switch	Diode	Magnetics		
[60]	20kW	900W	10.4kV	600V	100kHz	4-6.6	1.3-2.2	v_o	6	2	4	Yes	-
[61]	-	500W	-	300V	100kHz	-	3-4.3	v_o	6	2	3	Yes	96.0%
[63]	288kW	1.3kW	6kV	240V	20kHz	1.98	1.9	v_o	6	0	3	Yes	96.4%
[70]	24kW	336W	1.2kV	150V	50kHz	-	1	v_o	6	2	3	Yes	94%
[80]	120kW	900W	6kV	300V	50kHz	2	1.92	v_o	4	0	3	Yes	95.4%
[73]	200W	150W	200V	200V	10kHz	1.6	1.6	-	3	1	3	No	94.05%
[71]	50kW	400W	4kV	160V	50kHz	0.83	4	v_o	6	2	2	Yes	-
[72]	158kW	1kW	6kV	240V	20kHz	2	2	v_o	6	0	3	Yes	96.3%
Proposed	13kW	500W	10kV	850V	170kHz	5-10	7-10	$v_o/2$	3	4	3	Yes	97.2%

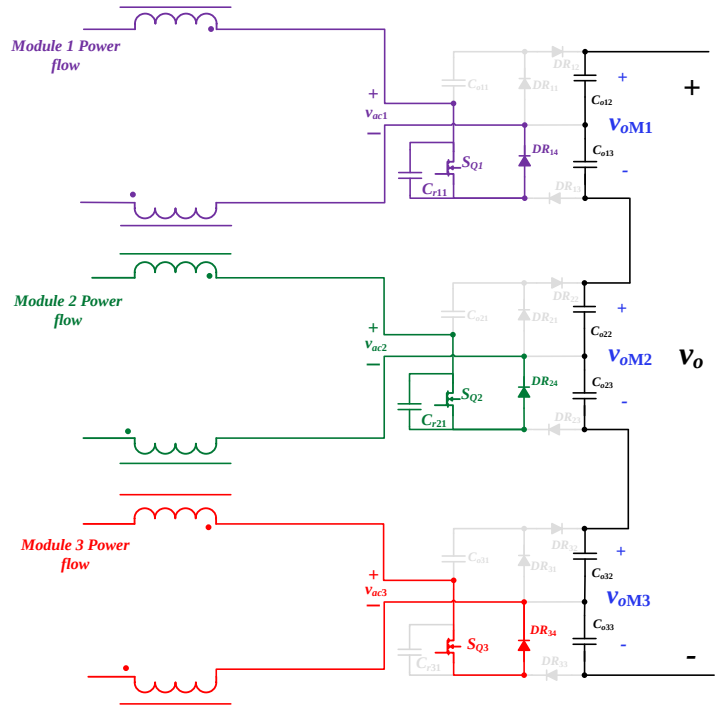
3.7 Chapter Summary

In this chapter, a modular based input independent output series PV energy system utilizing interlinking high frequency active voltage quadruplers capable of achieving balanced output voltage across all modules through power flow regulation was proposed. Instead of utilizing additional power balance units cascaded at the output, the output inductor of the *CLL* resonant converter was coupled to its neighboring module to allow for a power flow path to be created between modules. This flow was then regulated through variable duty-ratio control on the AVQ switch. Thus, balanced voltage across the output of each module could be easily realized without the need of complex controllers. Further, as power flow is regulated before the final step-up stage the system is able to achieve a high-step up gain even in scenarios of inactive PV arrays. The operating principles and steady-state analysis of each module as well as the power balance controller have been discussed in details throughout the chapter. In the final section of this chapter, the performance of the proposed system was verified through simulation results on a three module 13kW/10kV-output MVDC grid system and experimental results with a laboratory-scale two and three module 500W/850V-output system. The provided simulation results confirm the operating of the integrated power balance controller as each module achieved balanced output voltage under various power mismatch scenarios. The provided hardware results verified the feasibility of the proposed system by achieving balanced output voltage under unbalanced input power conditions including conditions with inactive PV arrays.

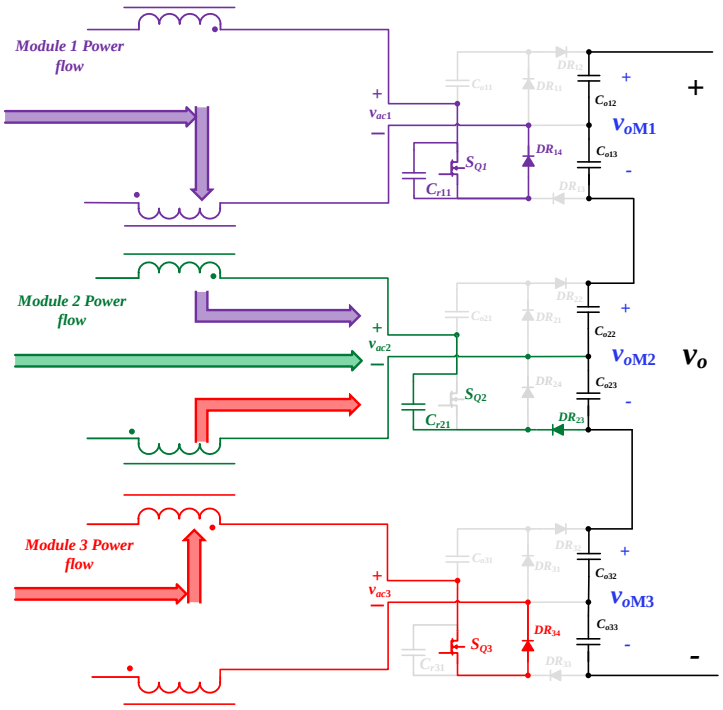
Chapter 4. Proposed Efficiency Optimization Scheme

In Chapter 3, a modular based input independent output series PV energy system capable of achieving balanced output voltage and power through the use of an integrated power balance unit was proposed. The controller used to regulate the power flow between each module is based on a simple PI controller. As discussed in Figure 3-7 this controller would regulate the duty-ratio of each AVQ such that their output voltage matched a provided reference signal. Due to rapidly changing atmospheric conditions such as light intensity and temperature, the AVQ duty-ratio will be constantly changing. Although a simple PI controller is capable of achieving balanced output voltage, as there are several possible operating conditions which results in balanced output voltage and there is no guarantee this simple controller will chose the optimal operating condition which minimizes the duty ratio of all module's AVQ switches.

This chapter focuses on the development of a novel control-based scheme to minimize the redundancy of the converter's operating state in order to maximize the overall system efficiency. The proposed efficiency optimization scheme identifies the module whose operating power is the lowest relative to its neighboring modules. From here the controller limits the duty-ratio of the AVQ switch to prevent excess power sharing which in turn reduces the required duty-ratio of each module. This is performed by sensing a change in the polarity of the AVQ input voltage. The proposed optimization scheme is integrated with the interlinking power balance units of the system designed in Chapter 3. The power loss associated with various components of the converter module are provided along with a power loss breakdown. The operating principles and analysis of the proposed controller are provided. In the final section of this chapter, both simulation and experimental results on a scaled down proof-of-concept prototype will be provided to highlight the performance of the proposed system.



(a)



(b)

Figure 4-1: System power flow for a three-module configuration (a) All AVQ switches active, (b) M_2 AVQ switch inactive

4.1 Power Loss Analysis

The AVQ switch duty-ratio of the system designed in Chapter 3 is regulated to achieve balanced modular power flow. Due to this, the AVQ switch duty-ratio is not independent from neighboring modules. Figure 4-1 shows an example of the power flow process between modules where it is assumed that modules M_1 and M_3 operate at a power level greater than M_2. The corresponding gate signals and AVQ switch current waveforms are shown in Figure 4-2. Figure 4-1(a) shows the scenario when all three switches are active. This corresponds to the red scenario in Figure 4-2. In this case the input to all module's AVQ is short circuit and the coupled inductors store energy. As there is no path from a module to the output, power is not shared between modules during this stage. The gate signal from the M_2's AVQ switch is removed first which is shown in Figure 4-1(b) and in the green scenario in Figure 4-2. The power from modules M_1 and M_3 begin to flow to the AVQ of M_2. Due to the output series connection, this results in an increase in M_2's output voltage. The time duration of the scenario shown in Figure 4-1(a) would dictate the required duty-ratio of each AVQ switch as the gate signals are removed in order from the module with the lowest power to the highest power. This implies that the scenario discussed in Figure 4-1(a) is unnecessary and contributes to an increased duty-ratio and in turn increased conduction loss in all

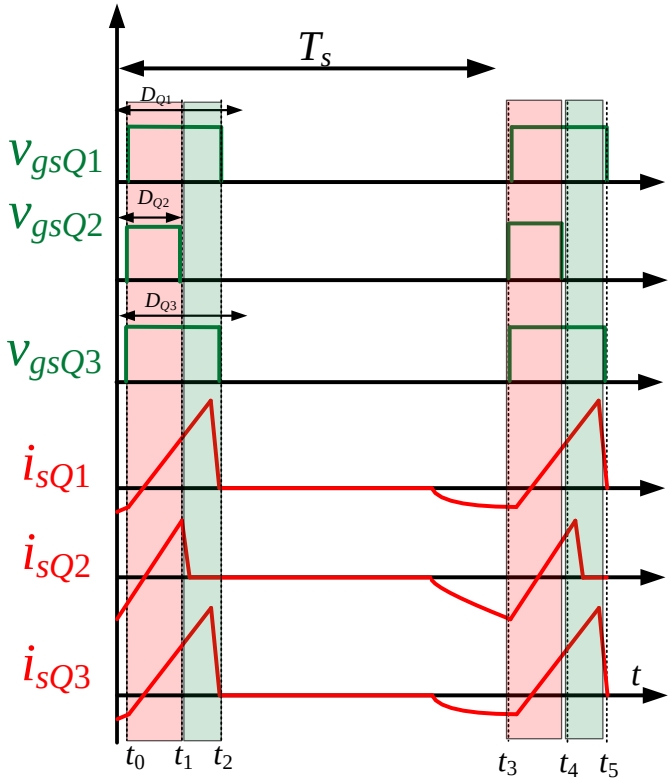


Figure 4-2: AVQ switch gate signal and current for the conditions shown in Figure 4-1

modules. By removing this operating stage from the system, the overall efficiency could be improved. However, it is possible that other components in the system have a larger impact on the system efficiency.

In order to optimize the operating state of the system and maximize the system efficiency, first the converter power loss breakdown must be understood. Different components of the proposed converter contribute to the overall power loss. These losses can be categorized into MOSFET power losses, diode power losses, capacitor power losses, and inductor power losses.

4.1.1 MOSFET Power Loss

The proposed converter utilizes three switches per module which are the two input switches S_{M1}, S_{M2} and the AVQ power balancing switch S_{QM}. As the converter is targeting MVDC applications, a Silicon Carbide (SiC) MOSFET was utilized for both the simulation and hardware tests conducted in Chapter 3. According to application note from ROHM Semiconductor [74], the power losses of SiC MOSFETs mainly contain: conduction loss, switching loss, MOSFET gate charge loss, and integrated circuit (IC) operation loss. Each of these will be discussed in the following section.

4.1.1.1 MOSFET Conduction Loss

Conduction loss was briefly touched upon in section 1.2.1.2 of Chapter 1. It was stated that the MOSFET conduction loss is (4.1). where I_{S_RMS} is the root mean square (RMS) of the current through the switch and R_{DS_on} is the ON-resistance of the switch between the drain and source.

$$P_{cond\_sw} = I_{s\_\mathrm{RMS}}{}^{2} \times R_{DS\_\mathrm{on}} \tag{4.1}$$

In the case that the current through the MOSFET is constant, the conduction loss can be determined from the switch current, the on-resistance of the switch, and the time duration for which the switch is active. This is typically the duty-ratio. In the case of the APWM boost converter used in this work, the power loss is represented in (4.2) and (4.3) for the high-side and low-side switch respectively. Due to the *CLL* resonant stage, the current flowing through the two MOSFET's are not constant. Based on Table 3-1 it is understood that the same switches are used for the input and AVQ stage and this the total conduction loss can be expressed as (4.4) where "*i*" is the *i*th switch, '*N*' is the total number of switches which is three. The ON-resistance can be obtained from the

manufacturer datasheet. In this work the "G3R160MT17D" SiC Power MOSFET was used for simulation which has an ON-resistance of 160mΩ and both the "SCT3030AW7TL" SiC surface mount device (SMD) and "SCT3030AL" through-hole Power MOSFET were used for the scaled down prototype which have an ON-resistance of 30mΩ.

$$P_{ON-H} = i_{sM2}{}^2 \times R_{ON-H} \times \left[1 - \frac{v_{pv}}{v_{Cdc}}\right] \tag{4.2}$$

$$P_{ON-L} = i_{sM1}{}^2 \times R_{ON-L} \times \frac{v_{pv}}{v_{Cdc}} \tag{4.3}$$

$$P_{cond\_sw} = \sum_{i}^{N} i_{s\_Mi\_RMS}{}^2 \times R_{ds\_on} \tag{4.4}$$

4.1.1.2 MOSFET Switching Loss

A brief overview of MOSFET switching losses was provided in section 1.2.1.1. As MOSFETs do not transition between states instantly and take a finite amount of time, the switching loss comes from the voltage and current during this time period. It was stated in section 1.2.1.1 that the switching loss is a function of the switch voltage, current, and the operating frequency (4.5).

$$P_{sw\_loss} = 0.5 v_{Cdc} \times i_s(t) \times f_s \times \left(t_{fv} + t_{ri} + t_{fi} + t_{rv}\right) \tag{4.5}$$

In this work, all MOSFETs operate with ZVS turn-on operation, and thus the power loss associated with the converter's MOSFETS are mainly conduction loss and turn-off operation.

4.1.1.3 MOSFET Dead Time Loss

In topologies that make use of a high-side and low-side MOSFET, there is a period of time during the transition state where a short-circuit occurs. In the proposed topology, switch S_1 is the high-side switch while S_2 is the low-switch. To prevent this overlap, a deadtime is programmed into the controller. The power loss due to this deadtime is provided in (4.6) where V_D is the forward voltage of S_2's body diode, I_D is the current through the body diode, t_{Dr} and t_{Df} are the rise and fall deadtime, and f_s is the switching frequency. These deadtimes are normally set by the designer.

$$P_D = V_D \times I_D \left(t_{Dr} + t_{Df}\right) \times f_s \tag{4.6}$$

4.1.1.4 MOSFET Gate Charge Loss

Gate charge loss is a type of loss associated with MOSFET gate charging and varies based on the gate charge capacity, also known as electric charge capacity. The gate charge loss can be obtained from (4.7) where Q_g is the gate electric charge, V_g is the required gate drive voltage, f_s is the switching frequency, and C_g is the gate capacitance.

$$P_{G\_loss} = Q_g \times V_g \times f_s = C_g \times V_g^{\,2} \times f_s \tag{4.7}$$

MOSFETS with a low on-resistance have a higher gate capacitance which in turn increases the gate charge loss. Typically, this loss is considered when the input to the converter is also used to power the gate driver and the MOSFETs. In this work an external source is used and thus the MOSFET gate charge loss is not considered.

4.1.2 Diode Power Loss

Each module of the proposed system utilizes four diodes per module which are used to form the AVQ. Several application notes from diode manufacturers [75], [76], [77] states that power loss associated with diodes can be categorized into two main sections which are forward and reverse losses. Forward losses occur when the diode is forward biased and conducting current. Reverse loss, also known as reverse recovery loss, occurs when the diode is transitioning from on-state to off-state and therefore can be characterized as a type of switching loss.

4.1.2.1 Forward Conduction Loss

The conduction loss of single diode is similar to that of a MOSFET switch in the sense that it is the product of the current flowing through the diode, i_f, the forward voltage of the diode, v_f, and the time duration for which this occurs (4.8).

$$P_{cond\_D} = \frac{1}{T_s}\int_0^{T_s} \left(i_f \times v_f\right) dt \tag{4.8}$$

The forward voltage is typically provided in the component datasheet, however the forward voltage is also a function of both the operating temperature and the diode current i_f. In this work four “MURS360BT3G” ultrafast power rectifier were chosen for the AVQ which have a typical forward voltage of 0.83V and a maximum value of 1.25V.

4.1.2.2 Reverse Recovery Loss

The calculation of the reverse recovery loss is more complicated than the forward conduction loss. An example of this loss is shown in Figure 4-3 where i_f is the forward current, v_f is the diode voltage and Q_{rr} is the estimated power loss. When a diode switches from forward conduction to reverse conduction, the current flowing through the diode, i_f, decreases towards zero while the diode voltage is still equal to the forward voltage v_f. Once the current reaches zero, it continues to decrease until it reaches a negative value known as the maximum reverse recovery current, i_{rr}. The time period from when the diode current passes the zero-axis until the current reaches the value of i_{rr} is shows as t_{rr1}. At the point the diode voltage starts to decrease towards the expected voltage across the diode v_d. The time required to reach this value is shown as t_{rr2} and the total time period of this condition is shown as t_{rr} in Figure 4-3. The diode can be considered off after this time period. The overlap between the voltage and current waveform during t_{rr} results in the reverse recovery loss (4.9).

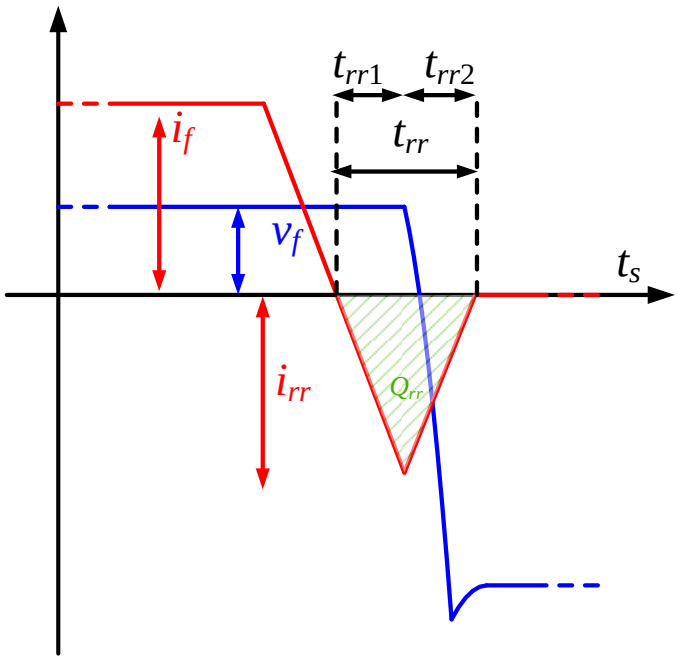


Figure 4-3: Example of a reverse recovery loss situation

This loss is typically approximated by taking the forward voltage to be constant (4.10). This equation can be further simplified by substituting the reverse recovery charge, Q_{rr}, which is provided in (4.11) into (4.10) to obtain (4.12)

$$P_{loss} = \frac{1}{t_s}\int_0^{t_s}\left(i_f \times v_f\right)dt \tag{4.9}$$

$$P_{RR\_loss} = \frac{1}{2} i_{rr} t_{rr} v_r f_s \tag{4.10}$$

$$Q_{rr} = \frac{1}{t_s}\int_0^{t_s}\left(i_f\right)dt = \frac{1}{2} i_{rr} t_s \tag{4.11}$$

$$P_{RR\_loss} = Q_{rr} v_r f_s \tag{4.12}$$

4.1.3 Capacitor Power Loss

Each module of the proposed system utilizes five capacitors per module which are the input capacitor between the PV arrays and the converter, the resonant capacitor which is part of the CLL stage, and the three AVQ capacitors. The conduction loss associated with a capacitor (4.13) is the product of the square of the capacitor's RMS current and their equivalent series resistance (ESR). The ESR of a capacitor is provided in (4.14) where f is the switching frequency of the converter, C is the capacitance, and δ is the loss angle. Typically, tan(δ) is referred to as the dissipation factor[78]. Figure 4-4 provides an example of how (4.14) is obtained. The ESR is located on the positive x-axis of the real complex plane while the capacitive reactance is located on the negative y-axis. The loss angle, δ, can then be obtained as shown.

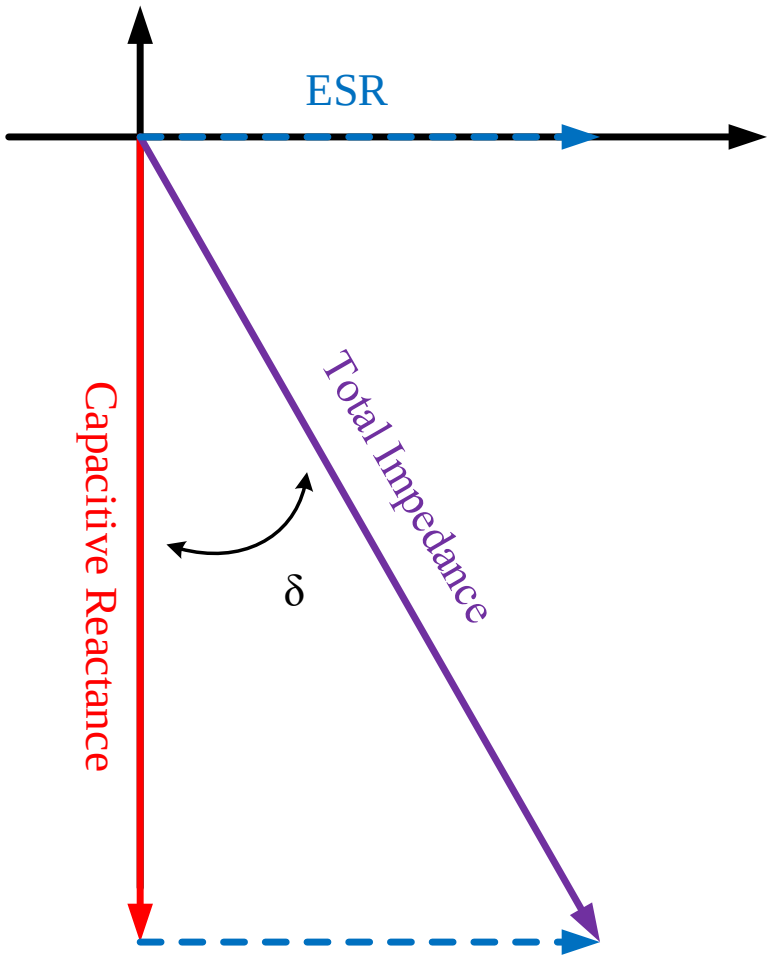


Figure 4-4: Capacitor ESR calculation

$$P_C = ESR \times i_{c,rms}^2 \tag{4.13}$$

$$ESR = |Z_C| \tan\delta = \frac{\tan\delta}{2\pi fC} \tag{4.14}$$

In the proposed work, the chosen *CLL* resonant capacitor is a "BFC233820224" 220nF film capacitor. When operating at approximately 130kHz, the total impedance is found to be approximately 7.23Ω which matches the impedance graph provided in the manufacturer datasheet. From here, the dissipation factor is listed as $70*10^{-4}$. Substituting these values into (4.14) results in an ESR of approximately 46mΩ. By using a Keysight E4980AL precision LCR meter, the ESR of the chosen capacitor was measured to be 37mΩ which is close to the calculated value.

4.1.4 Inductor Power Loss

The proposed system utilizes a single inductor and two coupled inductors per module which are the input inductor, the magnetizing inductance used for the *CLL* resonant stage and the output inductor used for both the *CLL* resonant stage and the power flow transfer between modules. Power loss occurs the in the inductor windings due to the DC resistance which can be estimated as shown in (4.15).

$$P_{cond} = R_{L\_DCR} \times i_{L,rms}^2 \tag{4.15}$$

Magnetic components such as coupled inductors typically utilize a core such as a steel core, solid ferrite core, or an air core. Power loss due to the core of magnetic components can be calculated by basic Steinmetz equation [79], where k, α and β are constant parameters that are unique to the material used, f_{sw} is the system frequency, and B is the peak flux density.

$$P_{core} = k \times f_{sw}^{\alpha} \times B^{\beta} \tag{4.16}$$

As mentioned in section 3.6, in this work, a ferrite core with N87 material from TDK was selected for the coupled inductors along with 1000 strands of AWG44 Litz wire.

4.1.5 Power Loss breakdown

Based on the power loss analysis provided throughout section 4.1, a power loss breakdown for the system designed in Chapter 3 has been conducted. Figure 4-5 contains the power loss breakdown of the system from PSIM. It can be seen that MOSFET conduction loss contributes to the majority of the system power loss, totaling approximately 55%. The AVQ diode conduction loss totaled approximately 22% of the system conduction loss, however as diodes are uncontrolled components of a circuit, their losses cannot be directly controlled. However, by optimizing the MOSFET conduction time, the diode power loss could in turn be reduced. This implies that by attempting to minimize the MOSFET conduction loss per module, the overall system efficiency would increase.

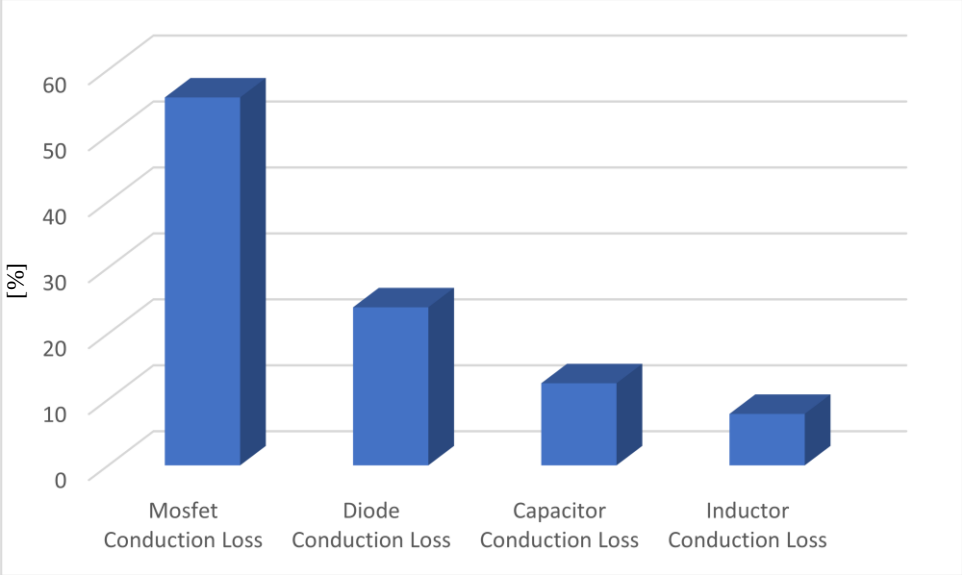


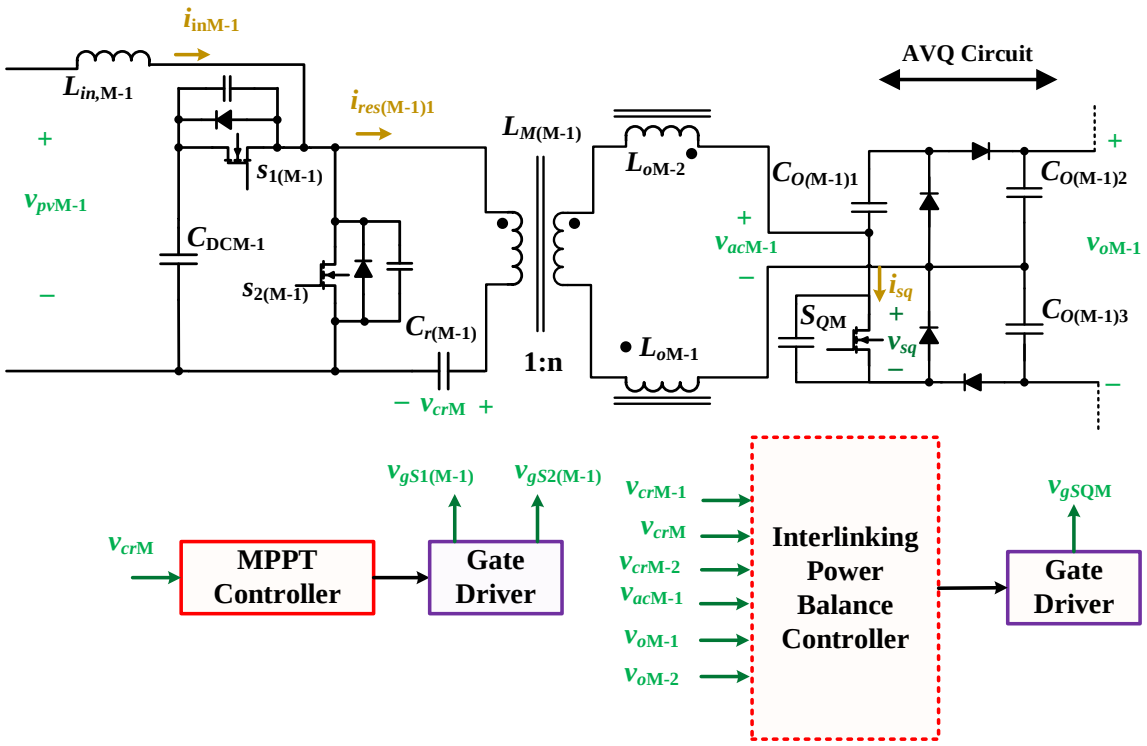
Figure 4-5: Power Loss Breakdown of the designed system from Chapter 3

4.2 Proposed AVQ efficiency optimization algorithm and converter topology

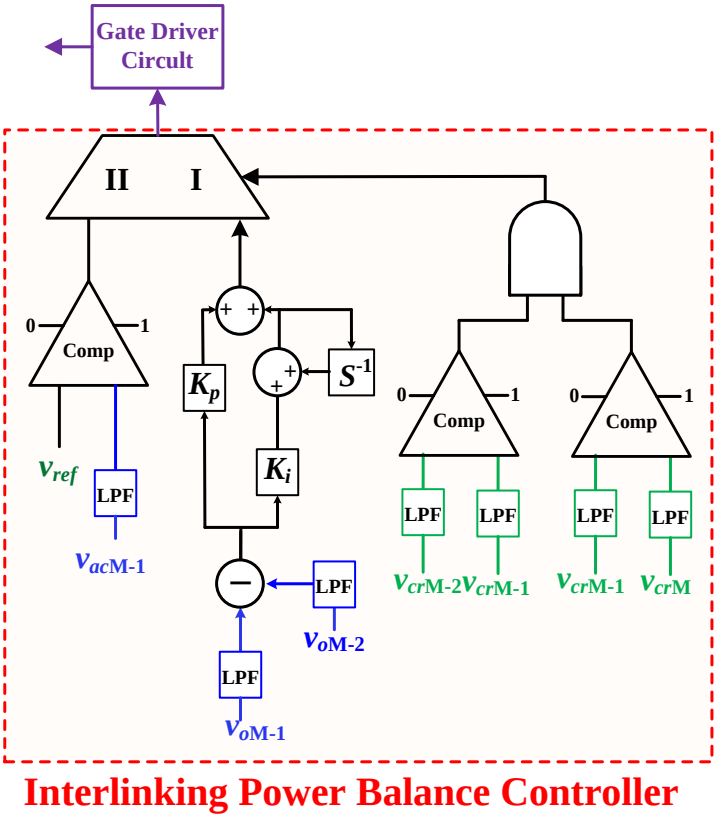
Figure 4-6(a) contains an example of a single module topology for the proposed system. The module consists of an integrated boost-*CLL* whose output inductor is coupled to its neighboring modules as well as an AVQ. This matches the topology discussed in Chapter 3. The utilized MPPT controller is once again the single-sensor current-sensorless algorithm that was designed in Chapter 2. The interlinking power balance controller has changed compared to the version shown in Chapter 3. It now takes in six voltage signals which are the module and its two neighboring modules resonant capacitor voltage, v_{cr}, and the input voltage to the AVQ, v_{ac}. These parameters are utilized in order to generate the AVQ gate signal of each module. The controller operating states, analysis, as well as the design and stability of this controller will be discussed in this section.

4.2.1 Proposed Controller Operating States

The details of the proposed efficiency optimizing interlinking power balance controller is provided in Figure 4-6(b). The controller operates in two states which depend on the operating power of the module relative to its neighboring two modules. If the controller determines that the module's operating power is higher than one of its neighboring modules, the controller will operate in the State I which utilizes a PI controller similar to that from Chapter 3. If the module's operating power is lower than both of the neighboring modules, the controller will switch to State II. In this state, the controller attempts to minimize the AVQ switch duty-ratio. To determine which state to function in, the operating power of three modules is required. This can be done with the use a voltage and current sensor which would measure the input parameters of the converter and multiply them together to obtain the power level.



(a)



(b)

Figure 4-6: (a) Topology of a converter module used in the proposed system, (b) The designed interlinking power balance controller

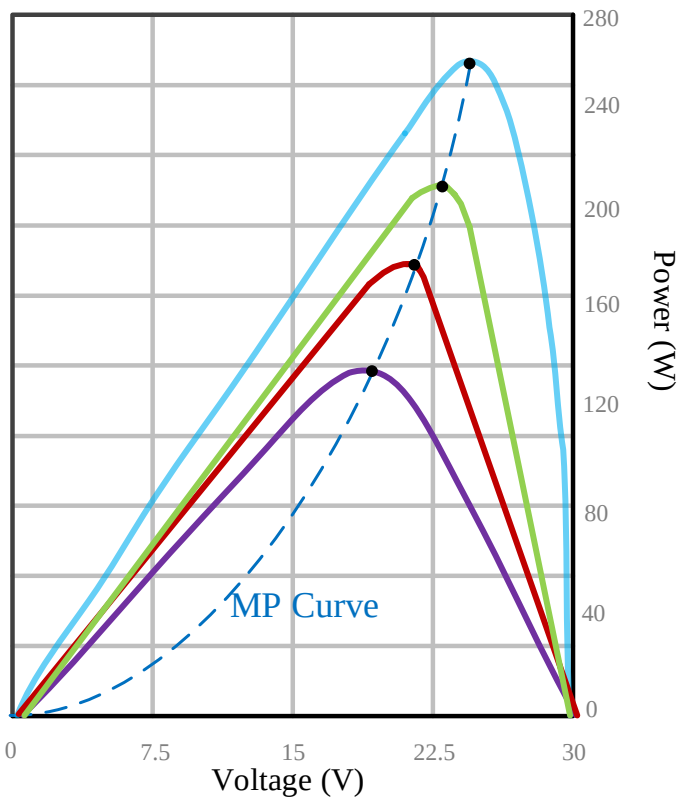


Figure 4-7: An example of a PV panels power characteristics,

However, this goes against the goal of Chapter 2 as a current sensor would be required. Figure 4-7 contains a plot of a generic PV array with the operating PV voltage on the x-axis and the operating PV power on the y-axis. Each plot represents a different light intensity. It can be seen that as the light intensity decreases, the required PV voltage to operate on the MPP curve decreases. Therefore, if it is assumed that all modules operate with the same type of PV array, then it would be possible to determine the lower power module based on the operating PV voltage. Although we could include a voltage sensor to perform this function, due to the chosen boost-CLL resonant circuit another parameter can be used.

Figure 4-8 contains the proposed module from the input stage to the isolating coupled inductor. A KVL loop containing the input PV voltage, the average input inductor voltage, the average isolating coupled inductor's primary side voltage, and the average resonant capacitor voltage is highlighted in green and results in (4.18). The inductor voltages can be represented in terms of their inductance and current as illustrated in (4.19). The voltage-second balance principle states that the average voltage across an inductor is always zero, therefore both the average input

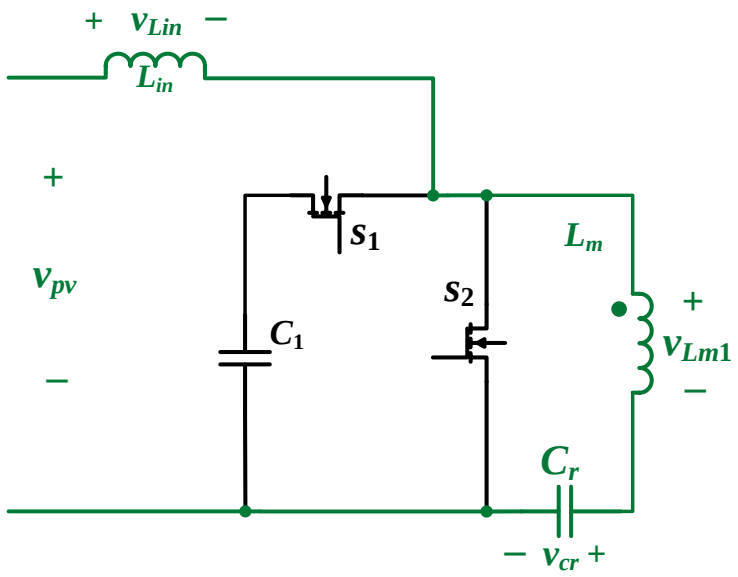


Figure 4-8: KVL loop on the input stage of each module

inductor and primary side voltage can be removed which results in (4.20). This implies that instead of sensing the input PV voltage, the resonant capacitor voltage can be sensed and averaged instead.

$$v_{pv} = v_{Lin\_avg} + v_{Lm\_avg} + v_{cr\_avg} \tag{4.18}$$

$$v_{pv} = L_{in}\frac{di_{Lin}}{dt} + L_m\frac{di_{Lm}}{dt} + v_{cr\_avg} \tag{4.19}$$

$$v_{pv} = v_{cr\_avg} \tag{4.20}$$

As shown in Figure 4-6(a), the resonant capacitor voltage is already used by the MPPT. This means that the resonant capacitor voltage is already available to the controller and additional sensor components would not be needed to identify the lower power module. When the proposed controller functions in state II, the operating duty-ratio of the lower power module is minimized to remove the redundant operating stage discussed in Figure 4-1 where all three AVQ switches are active. It would be simple to set the duty-ratio of the lower power module's AVQ switch to zero, however this may result in an increased settling time for power balancing when switching states. As seen in Figure 3-9, all AVQ switches operate under ZVS condition. This implies that when the gate signal is applied to the switch the secondary side resonant current is negative and flows through the anti-parallel diode of the switch prior to activation. Power is transferred between modules while the resonant current is positive. Therefore, the optimal duty-ratio that which the

lower power module should operate as is a value such that the gate signal is removed from the switch when the secondary side resonant current transitions from negative to positive. To determine this, one could use a current sensor to measure the polarity change, however as previously mentioned, current sensors are not ideal for this application. (4.21) contains the secondary side resonant current equation which is a function of the primary side magnetizing inductance, primary side resonant current rate of change, the magnetizing inductance turns-ratio, the equivalent output inductance, L_o, and the input voltage to the AVQ, v_{ac}. From this equation it can be understood that by sensing the input voltage to the AVQ the ideal duty-ratio can be obtained.

$$\frac{di_{res2}}{dt} = \frac{v_{ac} - L_m N \frac{di_{res1}}{dt}}{L_m (N)^2 - L_o} \tag{4.21}$$

4.2.2 Proposed Controller Design

The proposed controller utilizes the duty-ratio each modules AVQ switch to regulate power flow from the higher operating power modules to the lower operating power modules. As seen in Figure 4-6(b), a PI based closed loop controller attempts to drive the error between the measured module output voltage and the reference signal to zero. In order to design this controller, the proportional and integral gains of the controller, which are k_i and k_p, are required. These gains were

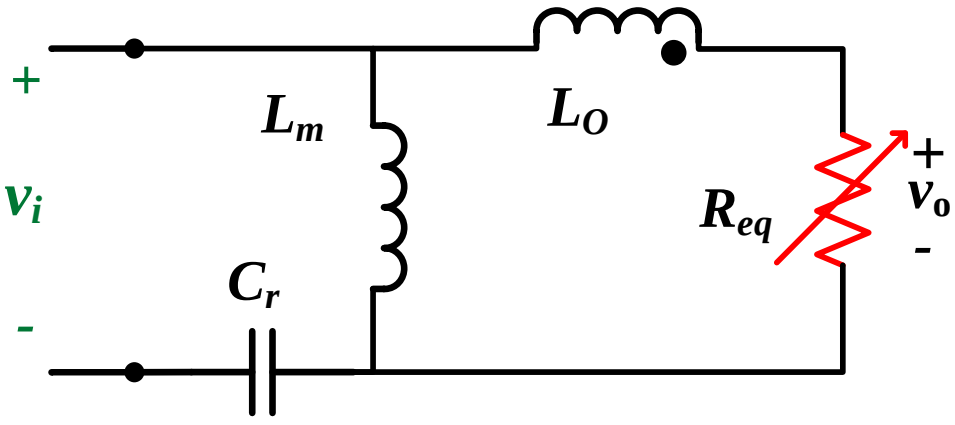


Figure 4-9: Equivalent circuit of a single module's CLL resonant stage

calculated through the use of the fundamental harmonic approximation as well as the Control System Analysis Toolbox from MATLAB. The proposed system utilizes two separate controllers, one for duty-ratio control on the input switches for MPP operation and one for duty cycle control on the AVQ switch for voltage balancing and power flow regulation. Utilizing the complete converter model will result in a complicated design process, thus the equivalent circuit of the CLL resonant circuit is used. This equivalent circuit is shown in Figure 4-9. The input voltage is generated from the duty-ratio of the input switches. By applying KVL to the circuit shown in Figure 4-9 three non-linear state equations are obtained:

$$\frac{di_{Lo}}{dt} = -\frac{sign(i_{Lo})v_o}{L_o} \tag{4.22}$$

$$\frac{di_{Lm}}{dt} = \frac{v_{res}}{L_m} - \frac{v_{cr}}{L_m} \tag{4.23}$$

$$\frac{dv_{cr}}{dt} = \frac{i_{res}}{C_r} \tag{4.24}$$

In the proposed efficiency optimization algorithm, duty-ratio control on the AVQ switch, $D_{q\mathrm{m}}$, is utilized for output voltage regulation. However, this parameter does not exist in the above equations as an independent parameter and instead is implicitly present in R_{eq}. Therefore, the system will be described in a non-linear form (4.25).

$$\frac{dx}{dt} = f(x) + g(x,u) \tag{4.25}$$

To design a PI controller to provide voltage regulation through duty-ratio control on the AVQ switch, the non-linear system has been linearized through the use of the Control System Analysis Toolbox in MATLAB. The system was set up in SIMULINK and a small AC perturbation was applied to the control input such that an estimated transfer function can be obtained. Once the estimation was obtained, the PID Tuner function in the Control System Analysis Toolbox was used to provide stability. To this end, the following transfer function was considered (4.26).

$$H(s) = K_p + \frac{K_I}{s} = \frac{K_p s + K_I}{s} = \frac{K_p\left(s + \frac{K_I}{K_p}\right)}{s} \tag{4.26}$$

The controller type shown in (4.26) was specified in the program and the response time as well as the transient behavior were modified in order to achieve a stable closed-loop system as seen in Figure 4-10. The gain and phase plots of this system are provided in Figure 4-11.

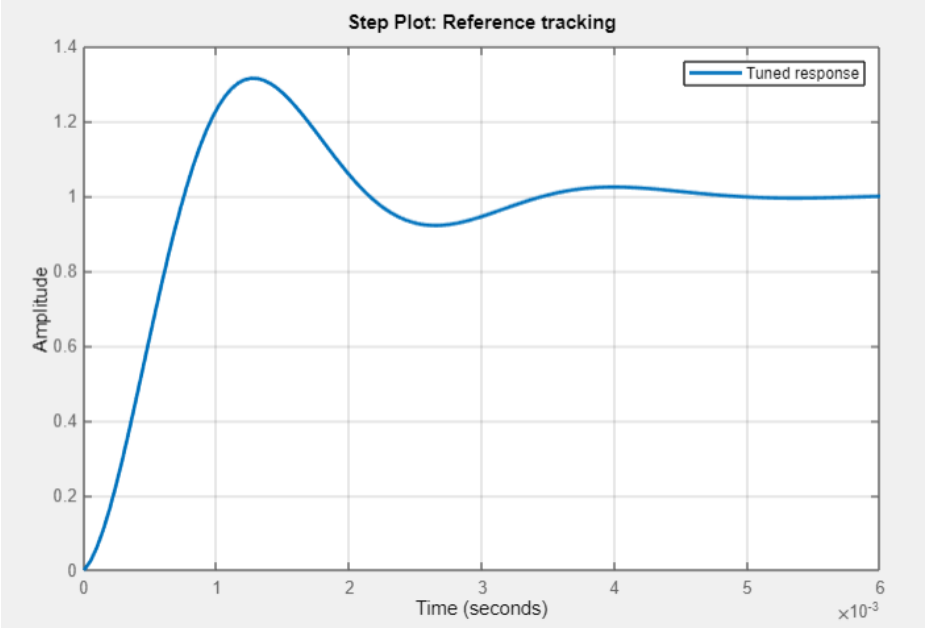


Figure 4-10: Tuned step-response from MATLAB

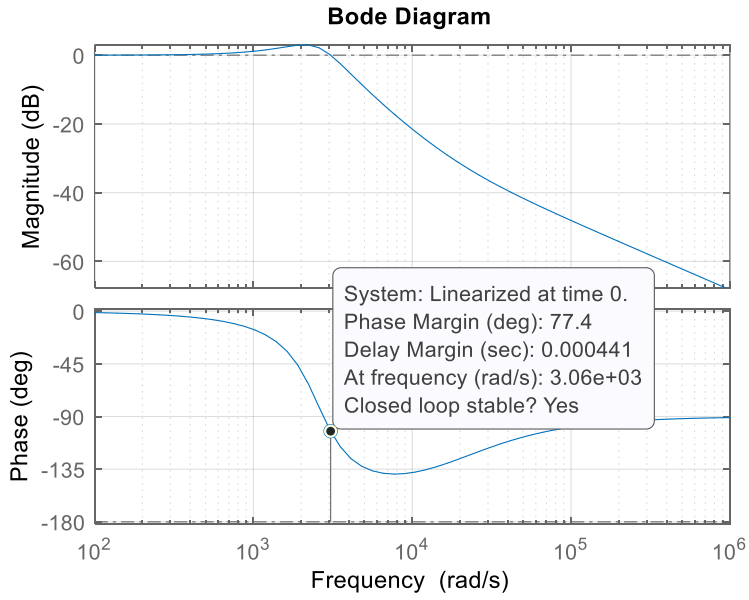


Figure 4-11: Closed-loop estimated bode plot of the developed AVQ controller

4.3 Converter Theoretical Operation

The key operating AVQ waveforms for two modules are shown in Figure 4-12 under the assumption that the power level of module M_1 is greater than that of module M_2.

[$t_0 < t < t_2$]: At time t_0, the gate signal is applied to switch S_{Q1} and S_{Q2}. As the gate signals are applied to the AVQ switches while the currents are negative and increasing, this facilitates ZVS turn-on operation for the higher-power module at t_1. At this point, the input voltage to the lower operating power AVQ, v_{ac2}, transitions from negative to positive. This polarity change acts as a trigger for the proposed controller remove the gate signal from the AVQ switch which prevents unnecessary delay in power transfer as well as additional conduction loss. The resonant current i_{res22} flows through diode D_{R24} which connects the input of to the AVQ across the snubber capacitor. This allows for a path for the capacitor C_{r22} to charge to the voltage difference across the output inductance. As C_{r22} is in parallel with the AVQ switch, this voltage is listed as v_{sQ2} in Figure 4-12. During this same time period, the current through module M_1's AVQ switch, S_{Q1}, has become positive and S_{Q1} has turned on under ZVS condition. As S_{Q1} is active, the input to the AVQ is short circuit which locks v_{ac1} at zero. The resonant current of M_1, i_{res12}, flows from the input of the resonant stage, through the S_{Q1} and the diode D_{R14}, and through the coupled inductor. This allows for power transfer from M_1 to M_2. Once the snubber capacitor is fully charged, i_{res22} reaches zero and the system proceeds to the next stage.

The following stages follow the same procedure as discussed in Section 3.3 of Chapter 3, but are repeated here for convenience.

[$t_3 < t < t_4$]: At time t_3, i_{res22} has reached zero, however i_{res12} is still positive and flows through S_{Q1}. Therefore, power is still being transferred from M_1 to M_2. At time t_4, the gate signal is removed from S_{Q1}. The current i_{res12} continues to flow through D_{R14} and now continues through the snubber capacitor, C_{r12}, allowing it to charge similar to how C_{r22} was charging in the previous stage. In M_2, the resonant current begins to flow again through D_{R24}, allowing for its snubber capacitor to continue to charge which is represented as an increase in the voltage v_{sQ2} in Figure 3-9. Once the capacitor of both modules has fully charged, the respective resonant currents of each module begin to decrease towards zero. This stage ends once the resonant currents have reached zero.

[$t_5 < t < t_7$]: Once the snubber capacitors are fully changed and the voltage across the AVQ switches have reached their peak, the resonant current of each module begins to flow through the diodes

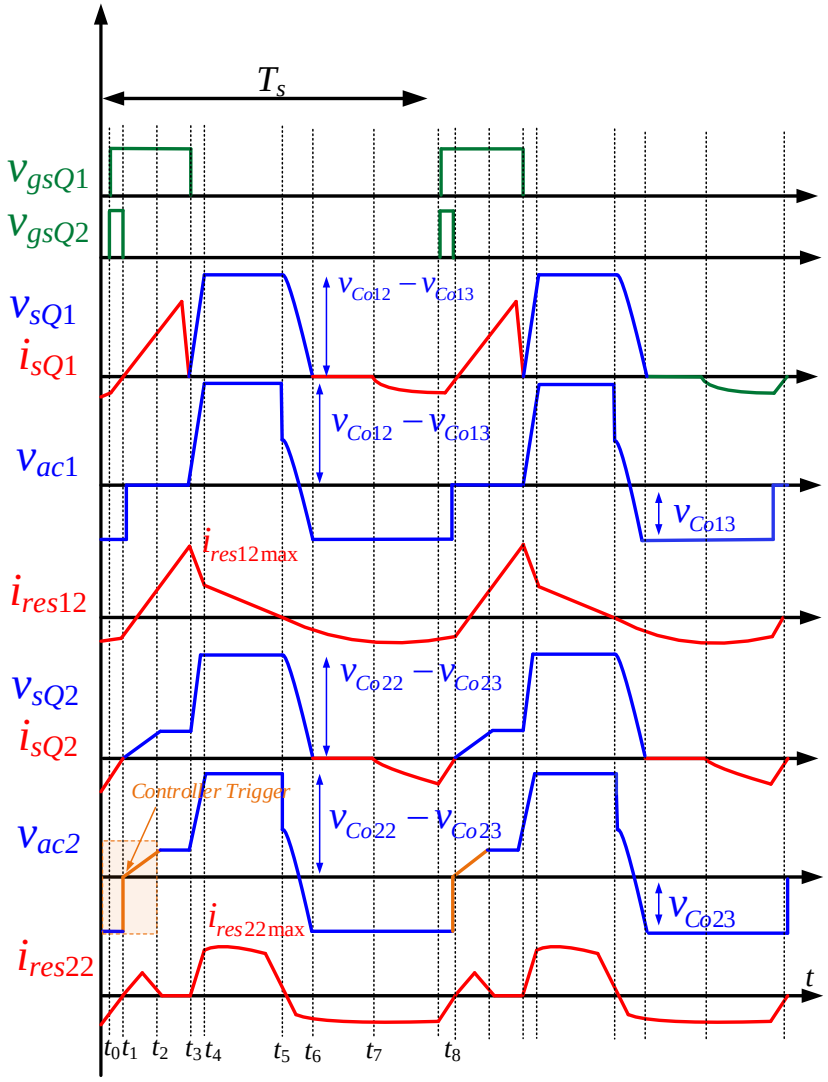


Figure 4-12: Operating waveforms of the AVQ for two modules operating at different power levels

D_{12} and D_{22} respectively and continues to decrease towards zero. At t_6, the resonant current is negative and the voltage across the snubber capacitors begins to decrease. The diode D_{14} and D_{24} are off, which results in an immediate decrease in the AVQ input voltage. This stage ends once the voltage across the AVQ switch has reached zero.

[$t_7 < t < t_9$]: The voltage across the AVQ switch has reached zero and the resonant current begins to flow through the diodes D_{11} and D_{21}. During this time, as the resonant current is negative and continues to decrease, the input voltage to the AVQ is negative. At t_7, the resonant current begins to flow through the diodes D_{13} and D_{23} and in turn the anti-parallel diode of the AVQ's switch. Due to the negative resonant current, it is understood that the AVQ switches will turn on under ZVS operation. This stage ends once the gate signals are applied to the switch and the system reverts back to the first stage.

4.4 Simulation Results

To confirm the performance of the proposed modular HF interlinking system, a 10kW, three module DC-DC converter system was developed in the circuit simulation software Powersim (PSIM). Similar to that of Chapter 3, each module consisted of the components shown in Figure 4-6(a) with their output inductors coupled to their neighboring module. PV arrays joined in series and parallel were connected at the input of each module to achieve 3.3kW at maximum light intensity. The single-sensor based MPPT algorithm discussed in Chapter 2 was employed such that each module would operate at their maximum power under all conditions. The proposed power efficiency optimizer algorithm was implemented such that the duty-ratio of all AVQ's would be regulated to perform both power flow regulation and minimize system losses. Table 4-1 shows detailed information in regards to the operating conditions and components utilized per module.

Table 4-1: Simulation and Prototype Parameters

General Parameters		
	Full Scale Simulation	**Prototype**
Generated Power	10kW	500W
DC-Grid/Output Voltage	10kV	850V
Number of Modules	3	2
Number of Panels per String	7	3
Number of Strings	2	1
PV Voltage Range (per module)	200-700V	55-110V
Gain Range (per module)	5 - 10	7 – 10
System Operating Frequency	140kHz	170kHz
System MPP Duty Range	30% - 70%	30% - 70%
Converter Specifications		
	Full Scale Simulation	**Prototype**
Input Inductance	100µH	100µH
Magnetizing Inductance	900µH	490µH
Turns-Ratio	2:3	2:3
Output Inductance	75µH	47µH
Input Capacitance	10µF	5µF
Resonant Capacitance	150nF	150nF
Output Capacitance	10µF x4	5µF x4
MOSFET Switch	G3R450MT17D	SCT3030AW7TL
Power Diode	GD05MPS17H	MURS360BT3G
DSP Controller	-	TMSF28335

To evaluate the benefits of the proposed converter, the system was first tested with the basic PI controller used in Chapter 3. The light intensity of each module was varied between 1000W/m^2 and 400W/m^2 which results in a power variation between 1.7W and 4.4kW. The light intensity was changed every 60ms. Figure 4-13(a), (b) and (c) contain the operation power of M_1, M_2 and M_3 respectively while the output voltage of each module is shown in Figure 4-13(d). As expected, the proposed power sharing configuration with a standard PI controller from Chapter 3 was once again able to balance the output voltage in all scenarios while simultaneously achieving MPP operation.

Figure 4-14 contains the AVQ switch voltage and current during two of the four scenarios tested in Figure 4-13. Specifically, the time periods between 0.06s to 0.12s and 0.12s to 0.18s. In both scenarios, there is a period of time where all AVQ switches are active and the switch current is greater than zero. This implies that there is a redundant time period during which power could be transferred between modules but is unable to. The peak switch current is seen to be approximately 12A Figure 4-14(a) and 15A in Figure 4-14(c).

The peak switch voltage is seen to be 1.5kV in Figure 4-14(b) and 1.7 kV in Figure 4-14(d) while the peak switch voltage for the other two AVQ modules are around 1kV during these conditions. As mentioned in Section 3.4.4 of Chapter 3, the peak AVQ switch voltage is equal to the difference in voltage between the output capacitors which itself is related to the turn-off duration of the switch and hence the duty-ratio. Due to the redundant time period in which all AVQ switches are active, the required duty-ratio to balance the output voltages is larger than required.

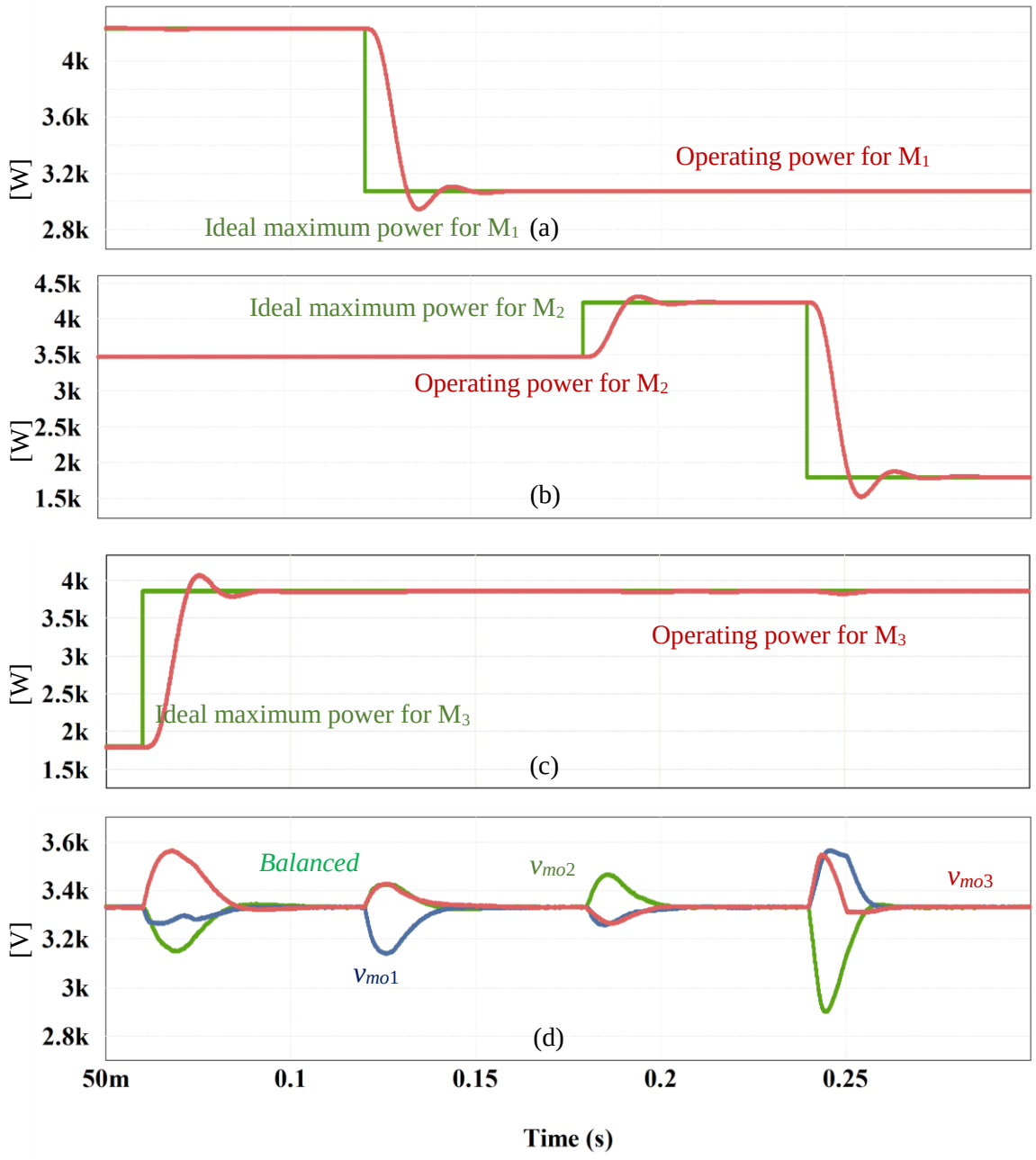


Figure 4-13: Simulation waveforms with standard power balance controller: Maximum and Operating power of (a) M_1, (b) M_2, (c) M_3, (d) output voltage per module.

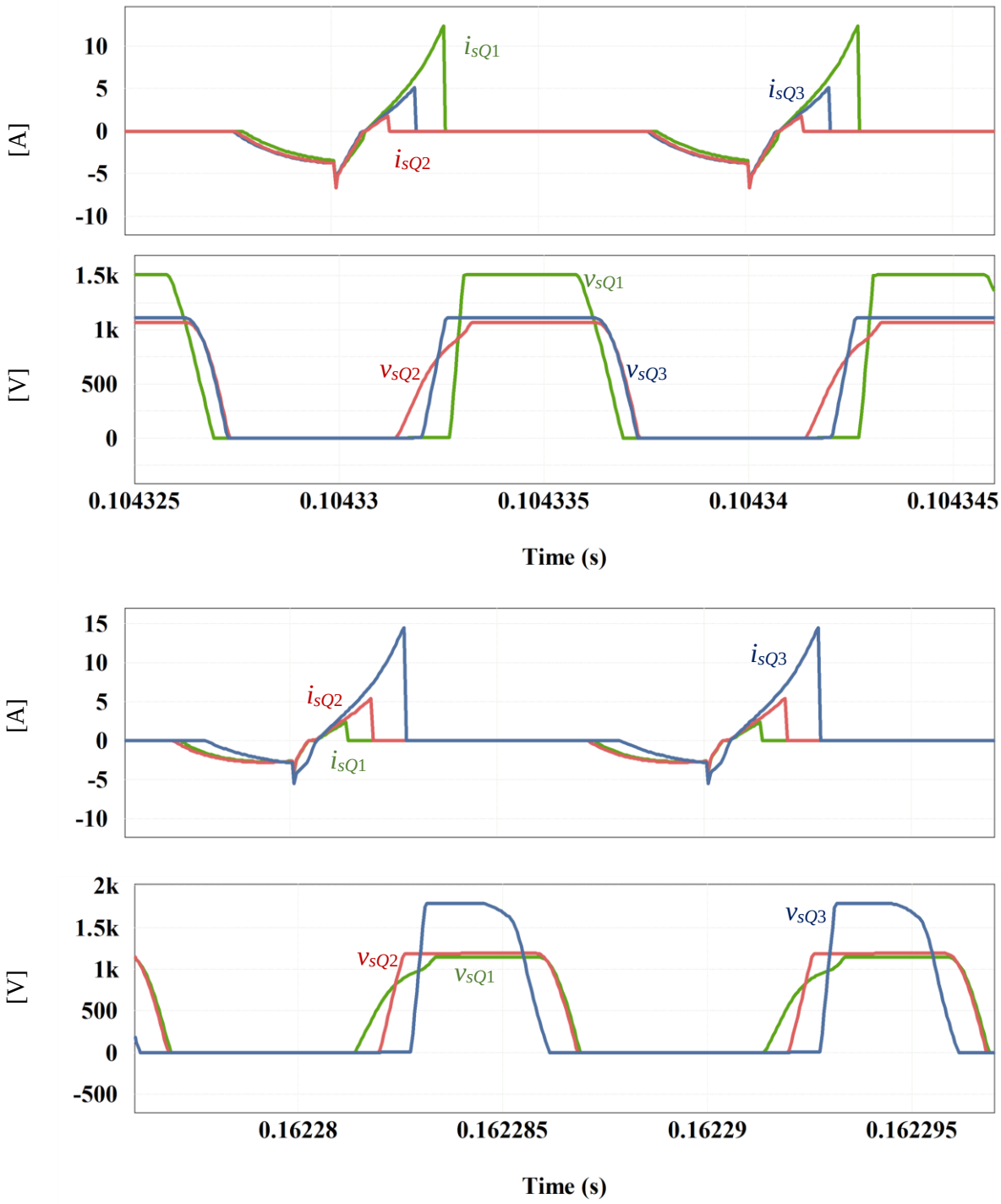


Figure 4-14: Conventional Controller: 0.06s<t<0.12s (a) Modular AVQ switch current, (b) Modular AVQ switch voltage, 0.12s<t<0.18s (c) Modular AVQ switch current, (d) Modular AVQ switch voltage

Figure 4-15 provides the simulation results with the newly proposed controller under the same operating conditions as the system discussed in Chapter 3. The light intensity of each module was once again varied between 1000W/m^2 and 400W/m^2 every 60ms. It can be seen that the newly proposed controller was able to achieve balanced output voltage for each module while simultaneously achieving MPP operation similar to that of the results with the basic PI controller seen in Figure 4-13. The time taken for the system to balance the output voltage is relatively the same as the results in Figure 4-13.

Figure 4-16 contains the AVQ switch voltage and current during two of the four scenarios tested in Figure 4-15. The first point of note is that in both cases, there is one AVQ switch whose current does not transition from negative to positive. In Figure 4-16(a) this corresponds to M_2, and as seen in Figure 4-15, M_2 is the module operating at the lowest input power during the time period 0.06s and 0.12s. In Figure 4-16(c), M_1 is the module whose AVQ switch does not conduct and once again from Figure 4-15 it can be seen that M_1 is the module operating at the lowest input power during the time period between 0.12s and 0.18s. From Figure 4-16 (a) and (c) it can be seen that the peak switch current is approximately 10A and 11A respectively which are both lower than the results seen in Figure 4-14(a) and (c). The peak switch voltage seen in Figure 4-16 (b) and (d) are both lower than their corresponding values in Figure 4-14(b) and (d). From this it can be understood that the proposed system was able to achieve maximum power extraction and balanced output voltage while simultaneously operating with a lower peak switch voltage and current.

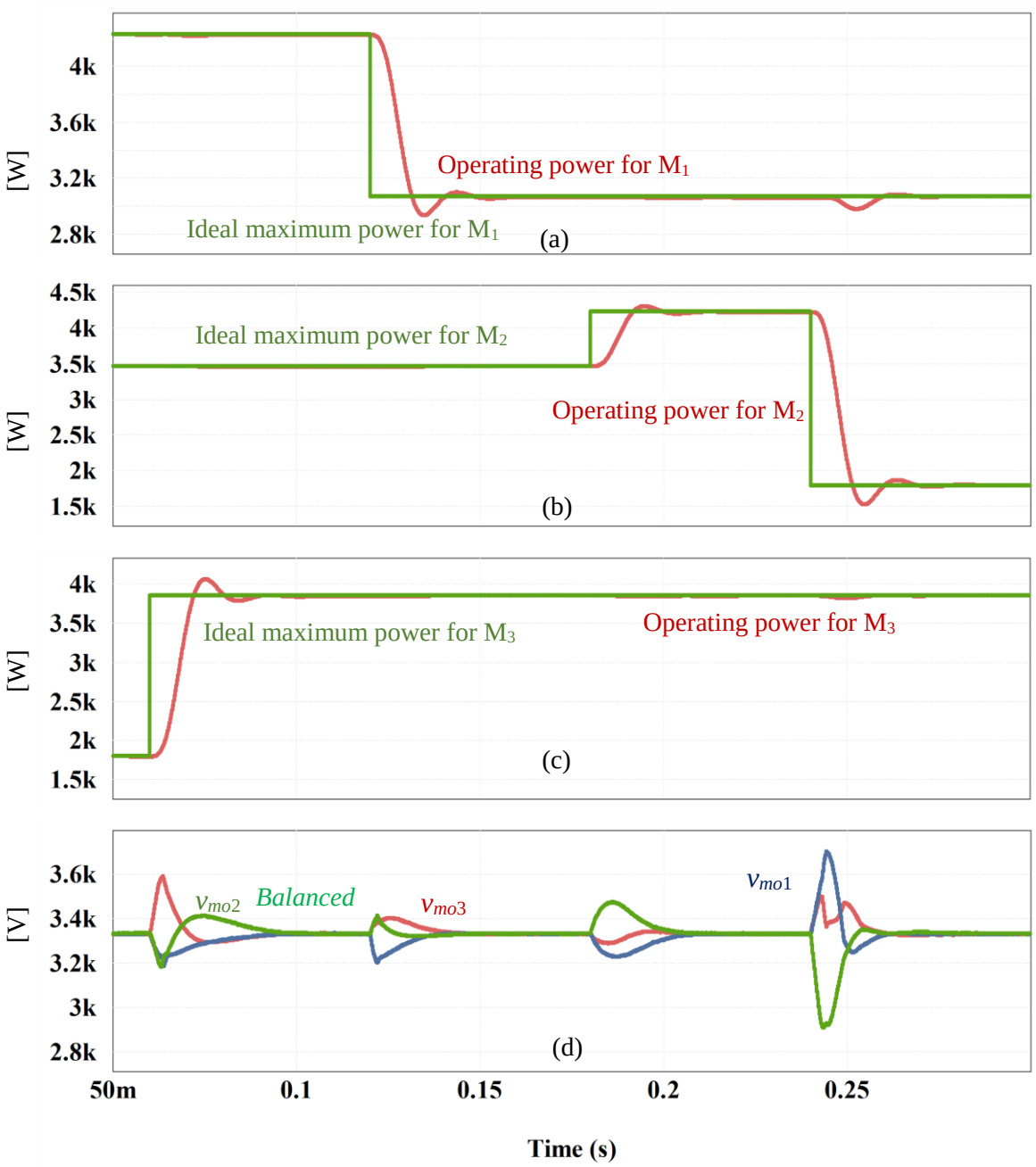


Figure 4-15 Simulation waveforms with proposed power balance controller: Maximum and Operating power of (a) M_1, (b) M_2, (c) M_3, (d) output voltage per module.

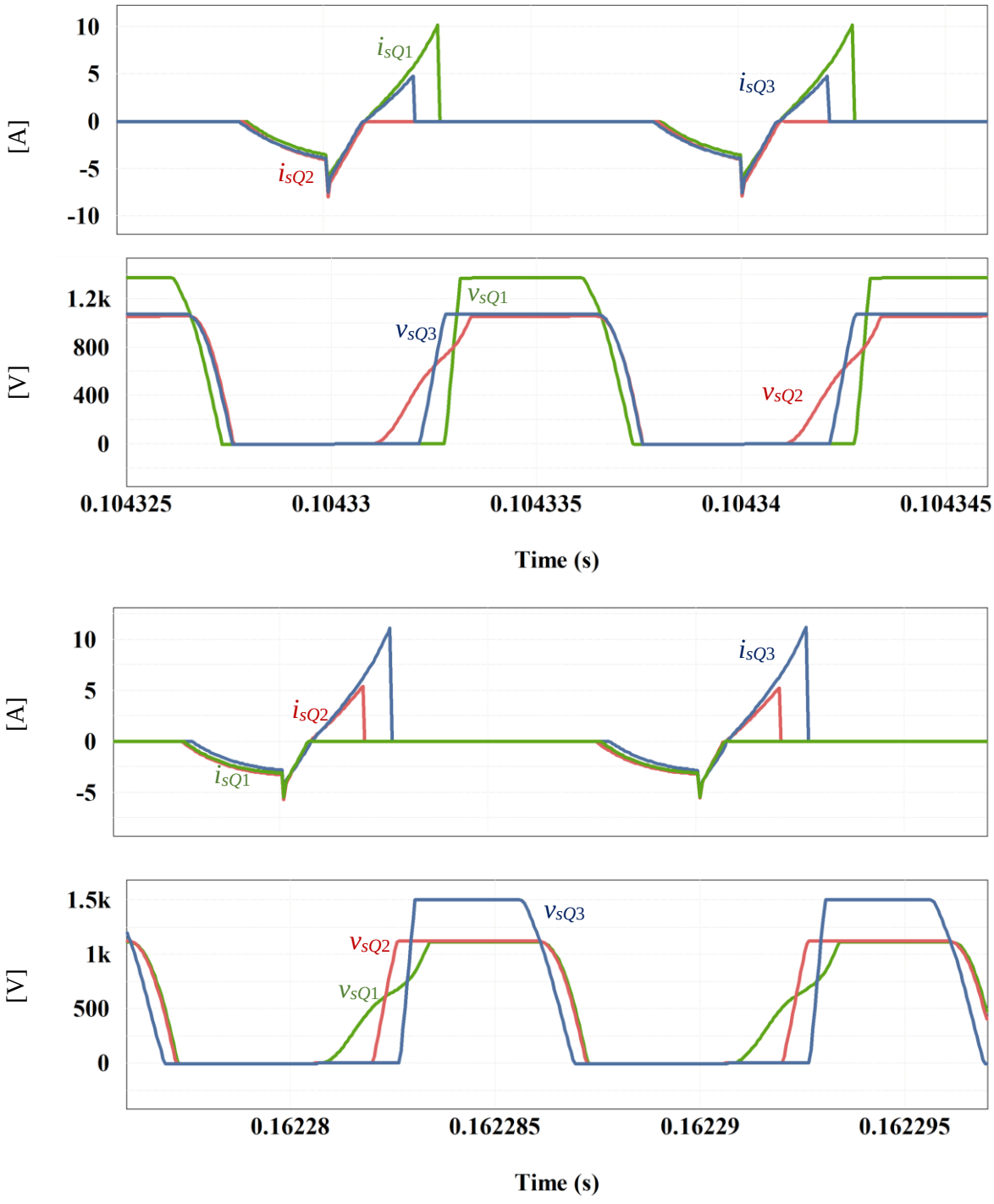


Figure 4-16: Proposed Controller: 0.06s<t<0.12s (a) Modular AVQ switch current, (b) Modular AVQ switch voltage, 0.12s<t<0.18s (c) Modular AVQ switch current, (d) Modular AVQ switch voltage

The efficiency of the designed system with the proposed controller is compared to the same system with a basic PI controller. Figure 4-17 and Figure 4-18 shows the total system efficiency while the operating power of each module varied between 400W/m^2 and 1000W/m^2 in steps of 200W/m^2. As there are three modules, to efficiently display the data, a 3D plot was used with the operating power of M_2 on the x-axis, the operating power of M_3 on the y-axis and the total system efficiency on the z-axis. From here, each graph in Figure 4-17 and Figure 4-18 represent M_1's operating power from 1000W/m^2 to 400W/m^2 respectively. The solid plot represents the efficiency of the system using the controller setup from Chapter 3 while the transparent plot represents the efficiency of the system using the proposed controller. It can be seen that in the case of unbalanced power levels, the proposed controller achieved a higher operating efficiency compared to the basic PI controller in almost every scenario. In all four cases highlighted in Figure 4-17 (a) the proposed converter allowed the system to achieve an increased efficiency of 1% compared to the conventional controller. This is again seen in Figure 4-18 which confirms that the proposed controller is capable of achieving a higher system efficiency compared to the standard PI controller.

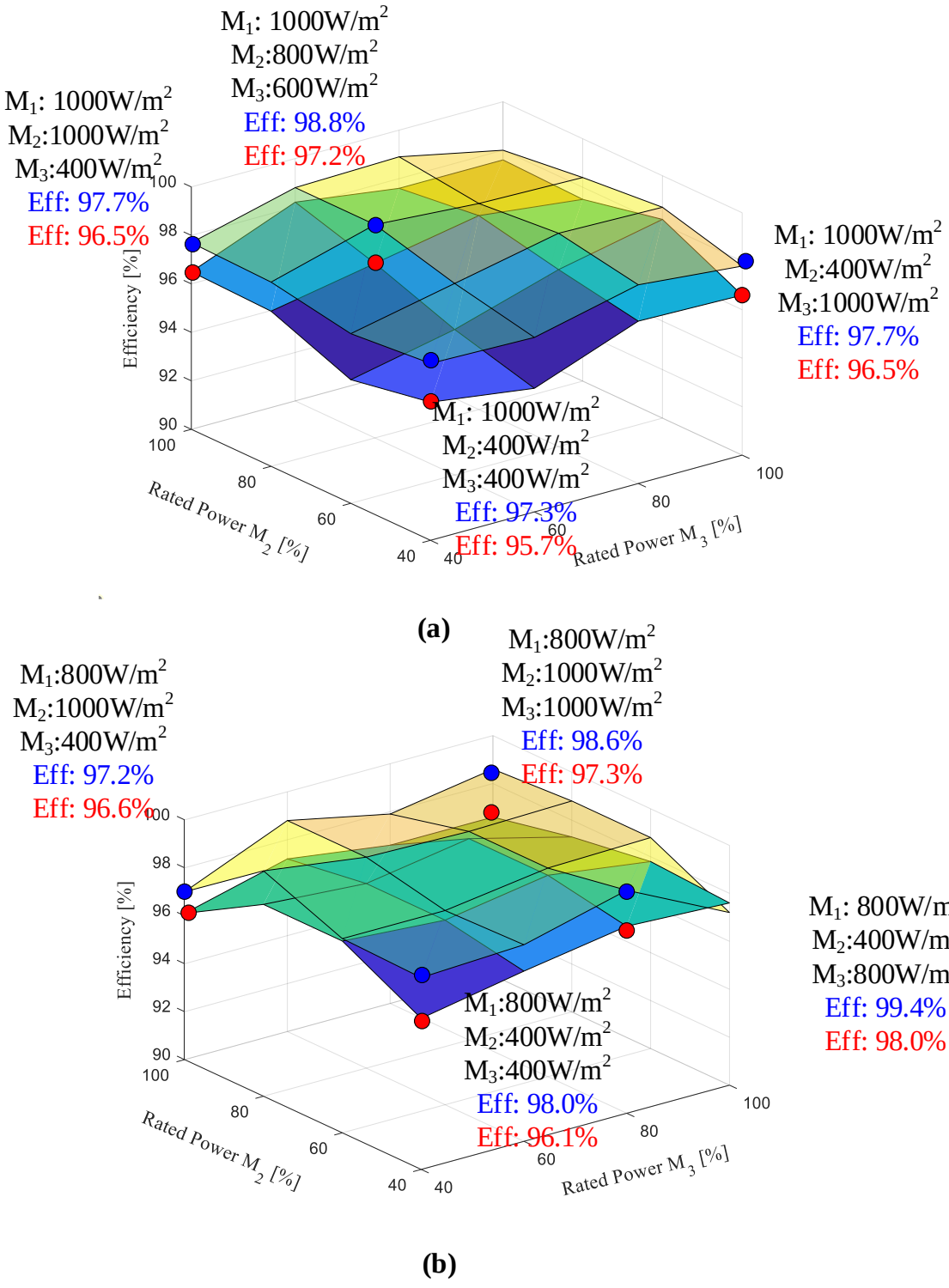
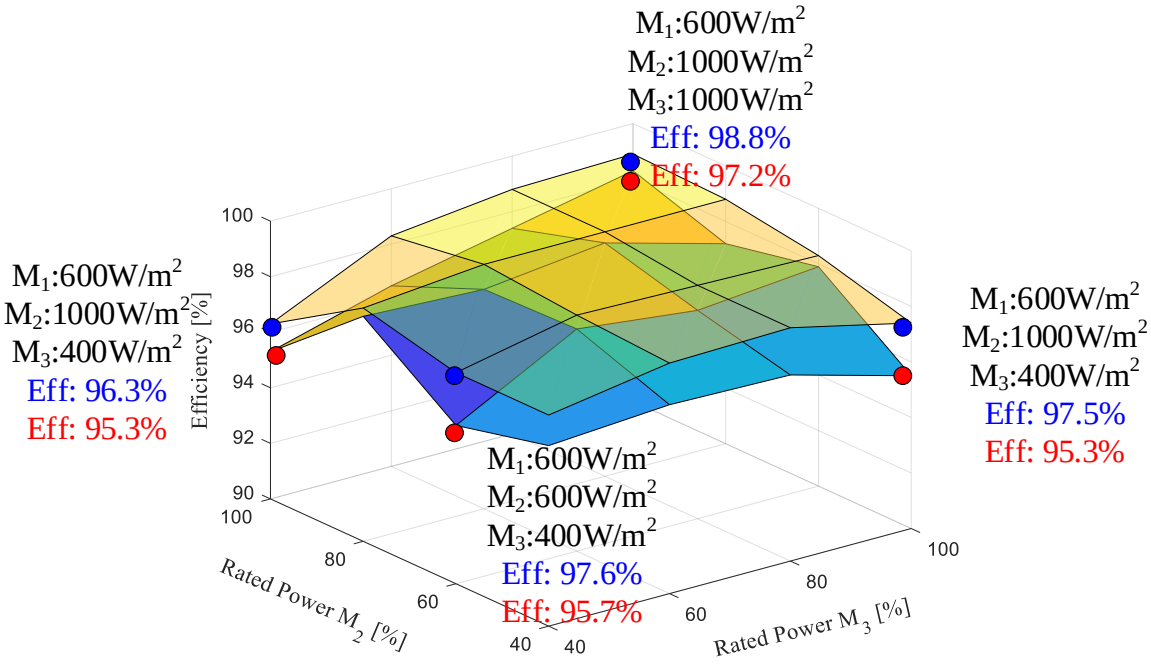
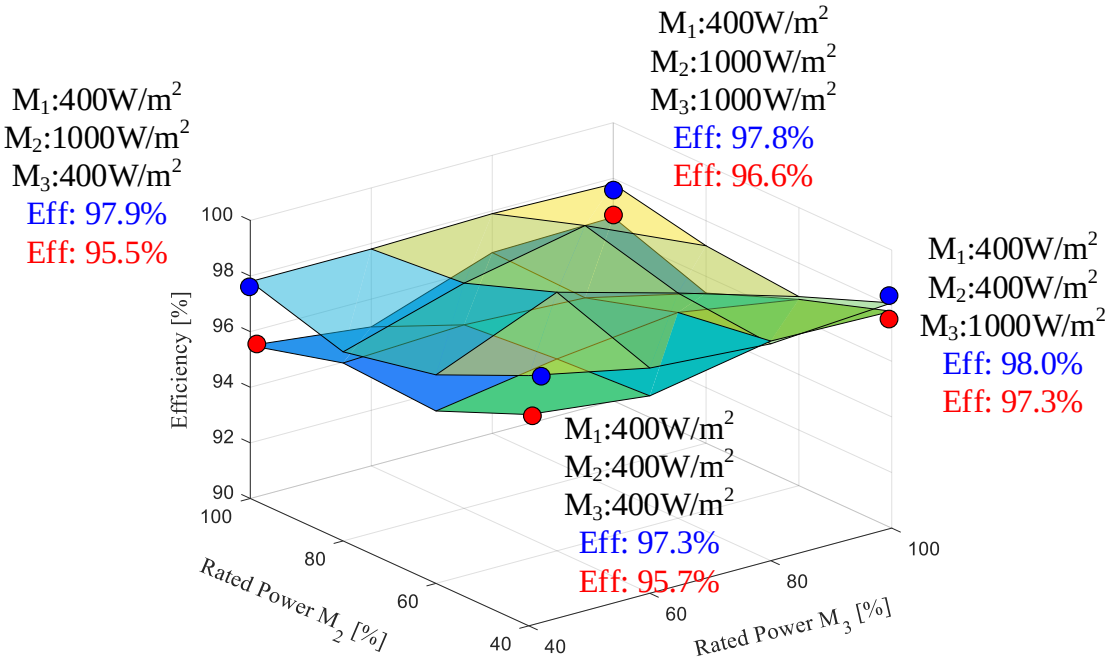


Figure 4-17: Three module system efficiency comparison between the basic controller and proposed efficiency optimization controller at varying light intensity (a) M_1: 1000W/m^2 (b) M_1 800W/m^2



(a)



(b)

Figure 4-18: Three module system efficiency comparison between the basic controller and proposed efficiency optimization controller at varying light intensity (a) M_1: 600W/m^2 (b) M_1 400W/m^2

4.5 Experimental Results

In order to confirm the functionality of the proposed system, scaled-down proof-of-concept hardware prototypes were constructed. The prototype consisted of the same layout used for the previous converter but was slightly modified such that additional sensing components could be added. The input voltage to the AVQ is located on the secondary side of the converter while the controller would be common grounded with the primary side of the converter. Therefore, once the AVQ input voltage was scaled down using a resistive bridge, an isolating op-amp was used to refer the scaled down voltage to the primary side such that the signal could be safely sent to the controller. The TMSF28335 digital signal processing (DSP) board was used to implement the proposed controller. In order to remove the gate signal based on the sensed parameter, the trip-zone interrupt module was used. This module can immediately trip the enhanced pulse width modulator (ePWM) which is useful in scenarios such as fault detection. In this work, the gate signal is to be removed from the switch when the input voltage to the AVQ transitions from negative to positive and therefore the trip-zone interrupt module can be applied.

To confirm the operation of the voltage balancer and its independence from the single-sensor MPP controller, two modules with different operating power were employed similar to that of the setup in Chapter 3 Section 3.6. Two channels of the Keysight E4360A SAS were independently connected to the input of each module and were set to have a maximum power of 250W and 130W respectively. The output voltage of each module (v_{mo1} and v_{mo2}), the total output voltage (v_o), as well the current through the AVQ switch S_{q1} (i_{sq1}) are shown in Figure 4-19 during unbalanced and balanced condition. The total output voltage was approximately 855V which meant that each module should have an output voltage of approximately 427.5V. However. the power mismatch resulted in an output voltage unbalance as the modules had approximately 535V and 320V respectively. Halfway through this test, the voltage balancer was activated which decreased the output voltage of M_1 to 427.5V and simultaneously increased output voltage of module M_2 to 427.5V. This confirms the proposed controller is also able to achieve balanced output voltage. A zoom-in of the waveforms during balanced condition is shown on the right side of Figure 4-19 which shows that M_2's AVQ switch operated under soft-switching condition and had a peak current of 7.2A in this condition.

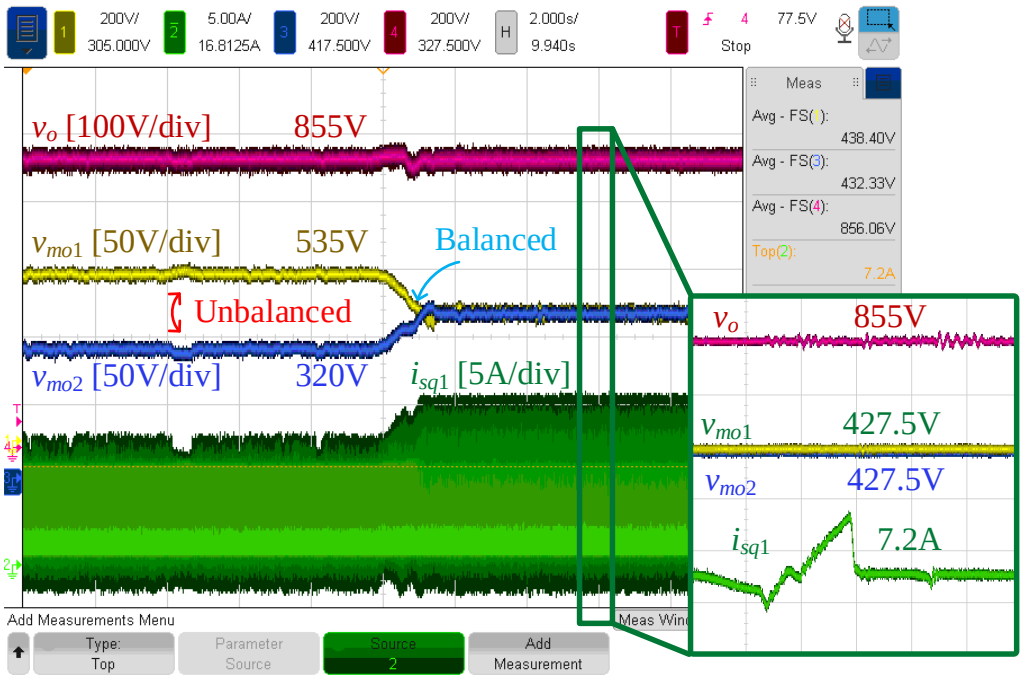
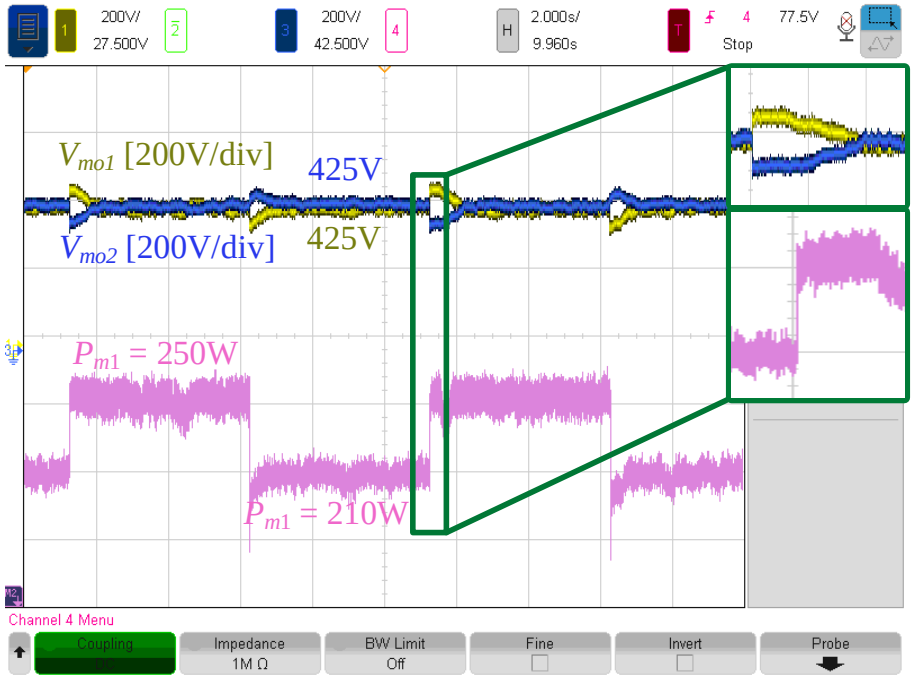
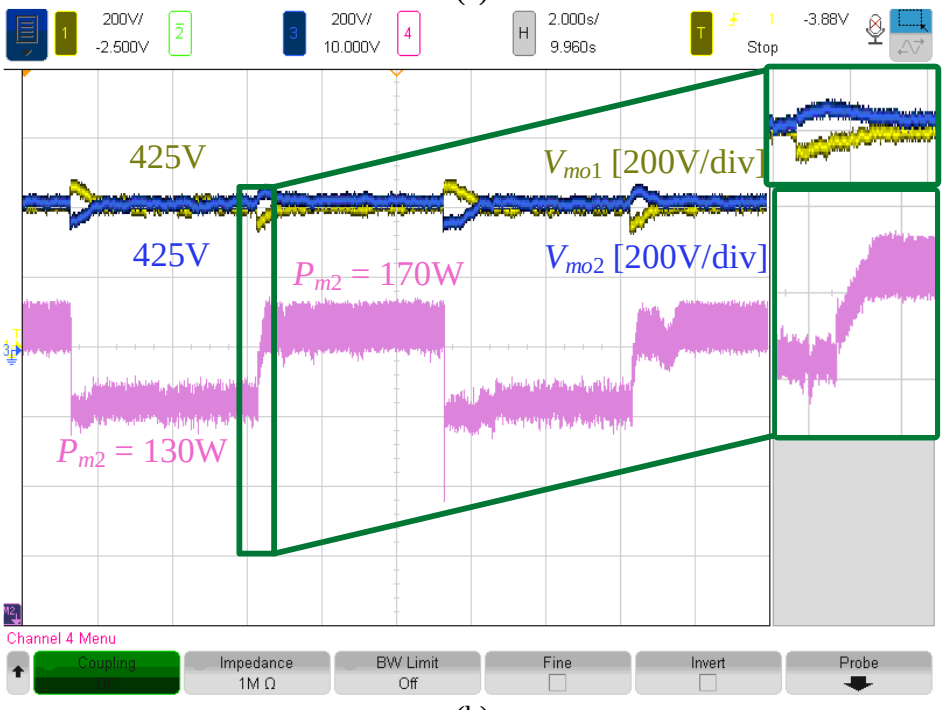


Figure 4-19: Experimental waveforms: unbalanced to balanced condition as well as a zoom-in of the balanced condition

To further confirm the balancing operation of the controller, a test similar to Figure 3-26 was performed. The modular output voltage as well as the input power of M_1 and M_2 are provided in Figure 4-20(a) and (b) respectively. The proposed efficiency optimization power balance controller and the designed single-sensor MPP controller were both active to ensure simultaneous MPPT and power transfer operation. As with the scenario in Figure 3-26, the operating power of M_1 would vary between 130W and 175W every 5 seconds while M_2 would vary between 250W and 205W within the same time frame. The operating power seen from the PV emulator is provided in Figure 4-21. From both of these figures, it is clear that the voltage balancer and single-sensor based MPPT controller operated simultaneously and independently to maintain balanced output voltage and the MPP for each module while ensuring the voltage imbalanced did not exceed 10% of the rated value. By comparing these results with Figure 3-26 it can be inferred that the proposed controller does not impact the MPPT and voltage balancing operation compared the conventional converter from Chapter 3.

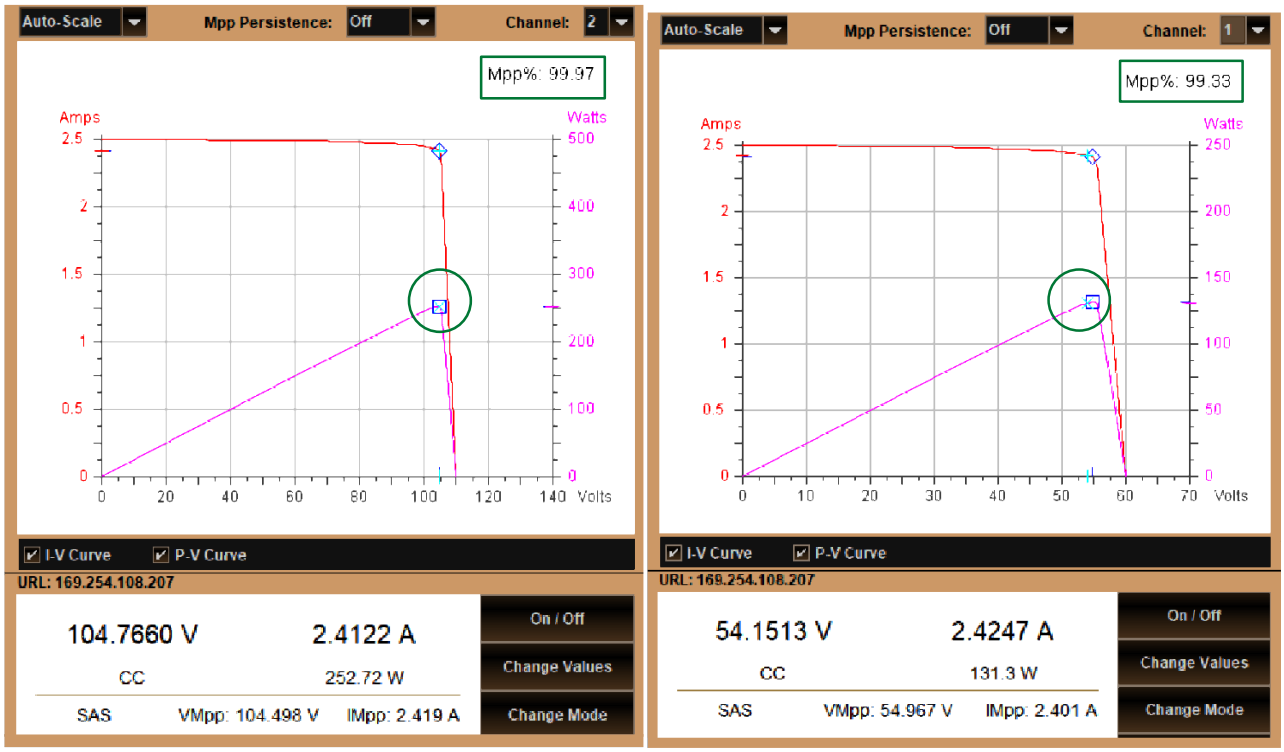


(a)



(b)

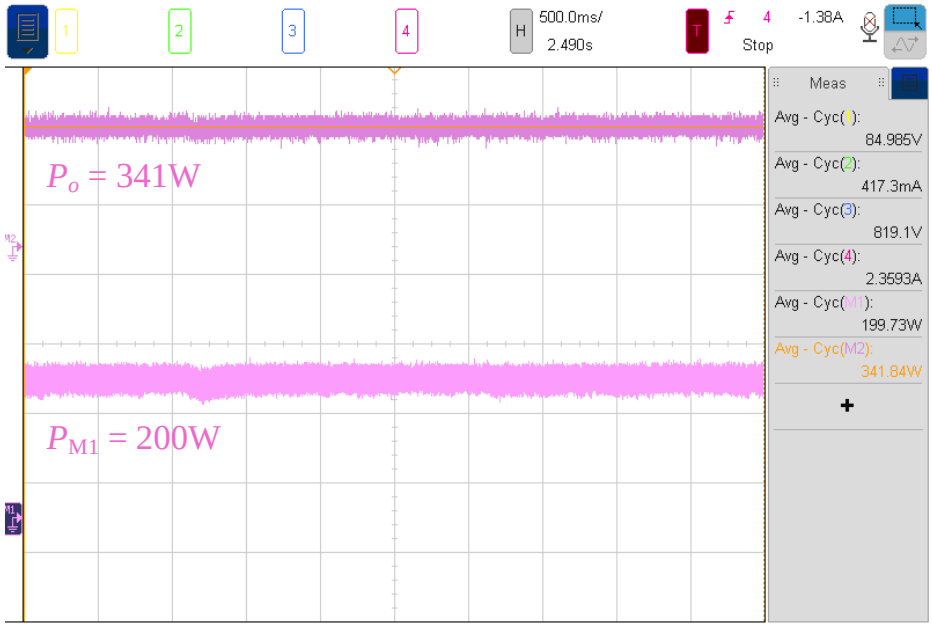
Figure 4-20: Experimental waveforms: Output voltage of both modules and input power of (a) M_1 (b) M_2



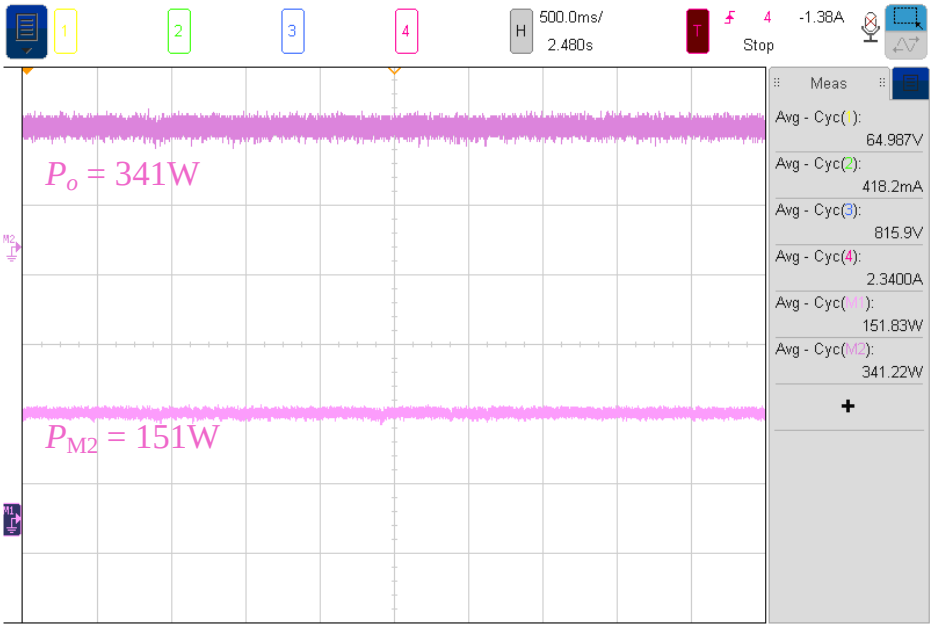
(a) (b)

Figure 4-21 Experimental waveforms: MPP operation for (a) M_1 (b) M_2

To confirm the efficiency of the proposed system the input power of each module and the total system output power were measured on an oscilloscope. The Keysight Infiniivision MSOX6004A Mixed Signal Oscilloscope with a sample rate of 20 GSa/s was used in this test. The operating voltage and current of each PV emulator channel were connected to each of the four analog channels. The MSOX6004A has a built in MATH function that can be used to obtain the operating power by multiplying the channel measurements. Using this method, the input and the system total output power were obtained and are provided in Figure 4-22(a) and (b). By dividing the total output power by the summation of the input power the converter efficiency is obtained which was 97.7%.



(a)



(b)

Figure 4-22: (a) Total output power and operating power of M_1, (b) Total output power and operating power of M_2.

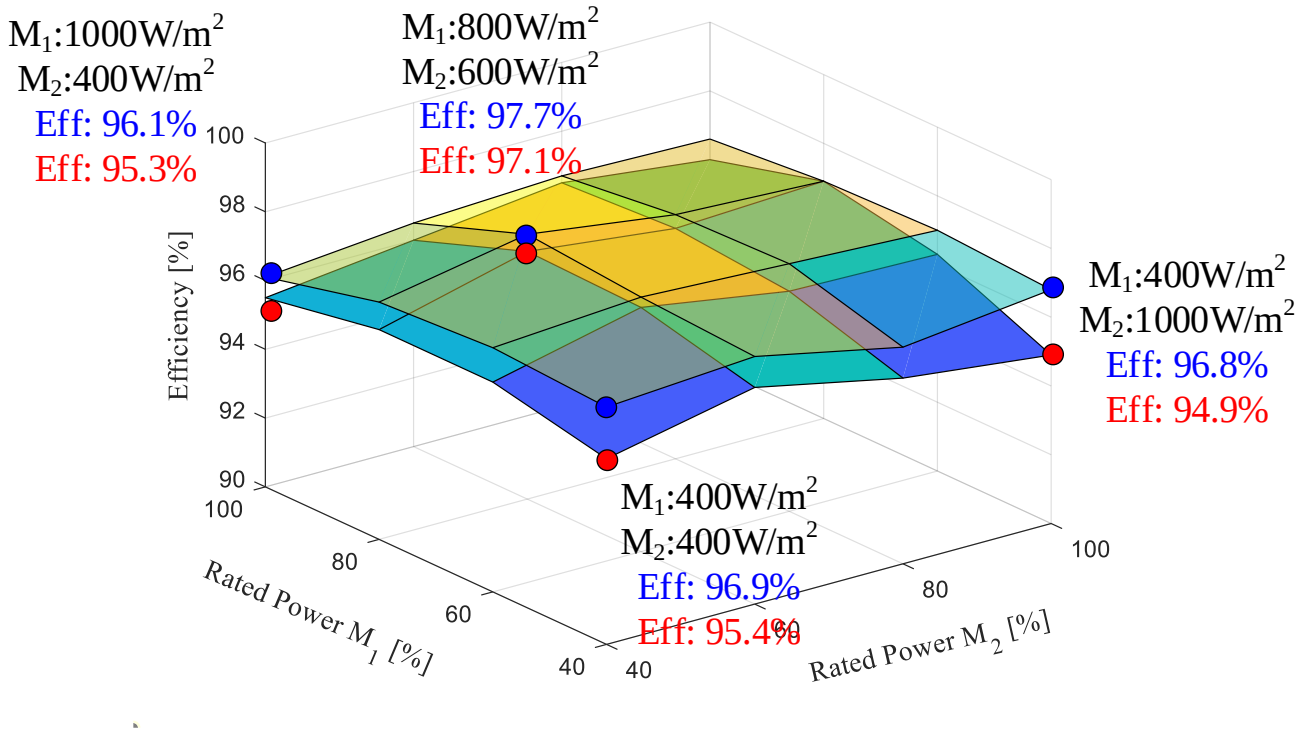


Figure 4-23: System efficiency at different operating power

The efficiency of the two-module system when utilizing the proposed controller is compared with that of the same system utilizing the basic controller from Chapter 3. Figure 4-23 contain a plot of both controller efficiencies where the see-through plot represents the system efficiency with the proposed controller. It can be seen in all scenarios the system achieved a higher efficiency compared to the version with the basic controller. The peak efficiency was 97.7% which is a 0.6% increase compared with the basic controller which achieved an efficiency of 97.1%. When M_2 operated at 1000W/m^2 and M_1 operated at 400W/m^2 an increased efficiency of 1.9% was observed. Throughout the entire operation range, the minimum system efficiency was found to be 96.1%. These results confirm the effectiveness of the proposed efficiency optimization scheme in achieving a high efficiency over a wide range.

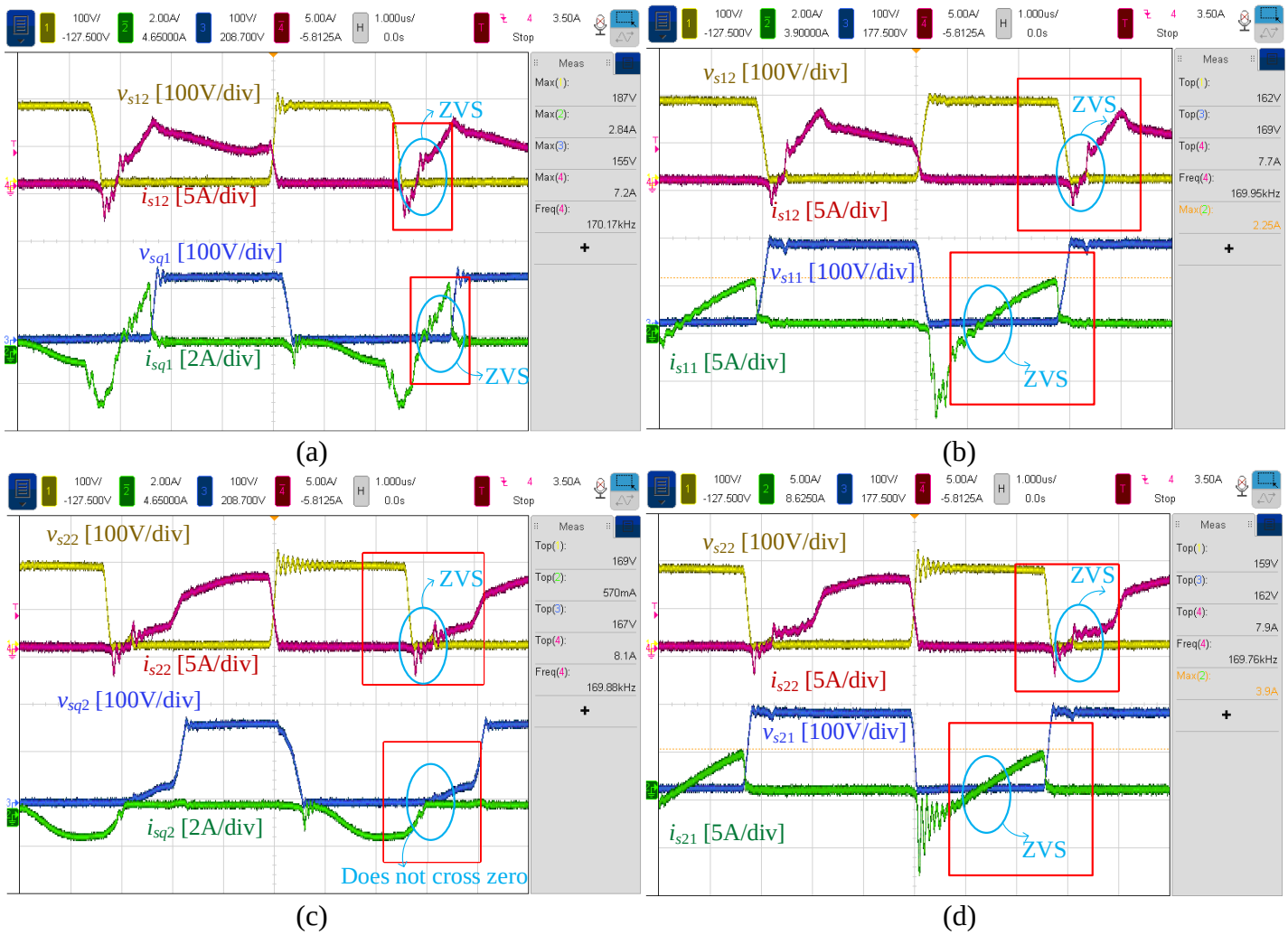


Figure 4-24 Experimental voltage and current waveforms for M_1: (a) S_{12} and S_{1q}, (b) S_{12} and S_{11}, M_2: (c) S_{12} and S_{1q}, (d) S_{22} and S_{21}

Each module's AVQ and input switch waveforms are shown in Figure 4-24. Figure 4-24(a) contains M_1's AVQ switch voltage and current waveform along with the input switch S_{12} while Figure 4-24(b) contains the voltage and current waveform of both input switches. The same waveforms are shown for M_1 in Figure 4-24(c) and (d) respectively. In all cases, ZVS operation is visible, implying the newly designed controller does not interfere with the systems operation. The peak AVQ switch voltage and current for M_1 are seen to be 155V and 2.8A respectively in Figure 4-24(a) which are lower than their respective versions from Chapter 3. For M_2, it can be seen that the AVQ switch current does not cross zero, implying the proposed controller was able to remove the gate signal from the switch. This matches the expected result as a proposed efficiency optimizer reduces the AVQ switch duty-ratio which results in a lower peak switch voltage and current and increased system efficiency.

4.6 Chapter Summary

In this chapter, an efficiency optimization scheme for modular soft-switched PV converters that utilize high frequency linking power balance units was proposed. The proposed efficiency optimization scheme minimizes the power loss due to the linking power balance units such that the system can achieve a high efficiency over a wide range. It achieves this by determining the module with the lowest operating power in terms of its neighboring modules and minimizes it's AVQ duty-ratio by identifying a polarity change in the AVQ input voltage. As a result, this technique can be integrated within the interlinking power balance controller discussed in the previous chapter. The power loss associated with various components of the converter module are provided along with a power loss breakdown. The operating principles and justification of the proposed optimization scheme and its integration with the power balance controller have been discussed in details throughout the chapter. The provided simulation results confirm the operating of the integrated power balance and efficiency optimization controller as the overall system achieved a higher efficiency when compared with the same system using a standard controller. Further, balanced output voltage under various power mismatch scenarios, single-sensor MPP tracking and soft-switching operation were achieved which indicates the proposed optimization scheme does not negatively impact the system operation. The provided hardware results verified the feasibility of the proposed system.

Chapter 5. Conclusions and Future Work

Power generated from renewable resources has been on the rise in the past decade. The total install capacity of photovoltaic (PV) energy has increased from 70MW to 942MW in the last ten years while its cost has decreased by over 50% in the same time frame. This has made PV energy systems an economically competitive investment. Power electronic converters play a key role in the integration of PV energy with MVDC grids. These converters are responsible for providing maximum power point tracking operation, converting the captured PV energy into usable electrical energy, and to step-up the PV voltage to reach the desired voltage range.

Conventional modular PV energy systems for MVDC applications utilize input independent output series connections to allow for both maximum power extraction for each module and the summation of all module voltages such that the system can reach the MVDC level. As the input to each module is independent and the outputs are connected in series, situations involving mismatched power levels will result in overvoltage situations which can damage converter components and ultimately result in the failure of the system. To overcome this issue, existing topologies reported in literature for PV based MVDC applications rely of power balance units to regulate power flow between modules to ensure balanced output voltage and in turn system stability. However, these topologies suffer from at least one of the following challenges: (1) the need for external power balance units to ensure system safety; (2) maximum power extraction is performed with multiple sensors or designed for specific topologies; (3) relatively low step-up voltage gain; (4) lack of or limited soft-switching operation as well as low efficiency over a wide operating range. The motivation of this research and this dissertation are inspired from these challenges and drawbacks. The contributions of this dissertation are summarized and highlighted in the next section.

5.1 Contributions

The contributions of this dissertation are summarized below:

1. A new step-up DC-DC converter for PV energy applications has been proposed and analyzed. The presented topology is capable of achieving a high step-up gain through the combined use of an integrated boost-*CLL* resonant circuit as well as a voltage quadrupler. Duty-ratio control can be applied to the input MOSFETs to achieve maximum power operation. ZVS turn-on and close to ZVS turn-off is achieved for all semiconductor devices including the input MOSFETs and the voltage quadrupler diodes.

2. A novel maximum power extraction technique utilizing only a single voltage sensor has been designed for PV energy applications. An alternative voltage parameter is tracked and maximized such that the maximum PV array power is extracted under all conditions. By utilizing a modified gradient ascent algorithm, the proposed controller is capable of adapting the perturbation step size to accelerate tracking while minimizing oscillations. The designed controller is compatible with a wide range of topologies and functions under both varying irradiance and temperature. Detailed descriptions of the designed controller have been provided.

3. A new power flow regulation and voltage balancing technique using interlinking coupled inductor for modular based MVDC systems has been proposed. The *CLL* resonant output inductor of each module has been coupled to their neighboring module and the previously utilized voltage quadrupler has been updated to replace a capacitor with a switch. By coupling the output inductor of each module, an alternative power flow path is created and by regulating the duty-ratio of the active voltage quadrupler switches the system power flow between modules can be regulated. This allows the system to achieve balanced output voltage across each module under power mismatch scenarios without the need of additional power balance units or conversion stages. Further, as power sharing occurs before the final step-up stage, each modules AVQ contributes to the total system gain regardless of the input PV array operating state.

4. A novel efficiency control system designed to optimize the system's power efficiency over a wide range is proposed for the modular PV based MVDC system discussed in Chapter 3. The developed control algorithm optimizes the AVQ duty-ratio operation by identifying the lower power module with respect to its neighboring modules. This minimizes both the conduction loss and redundant power transfer of each module and in turn allows for a higher operating efficiency over a wide range of PV power levels. A relatively flattened efficiency curve compared to conventional controllers is obtained without affecting achievements from previous sections.

5. Operating principles and steady-state analysis of all controller and converters have been discussed in details. The performance of all developed controllers and DC-DC converter modules have been validated by simulation results based on actual PV system parameters in a 10-13kW 10kV-output system and 200W per module laboratory-scale proof-of-concept hardware prototypes utilizing PV emulators. The design procedure of the discussed converters has been presented in details in this dissertation.

5.2 Future Work

A number of future works relating to this dissertation are summarized below:

1. The experimental work was performed in a laboratory environment not equipped with windows or artificial light sources which lead to the use of PV emulators. Testing the proposed system and controller with PV arrays in an environment similar to what an end user would have could enhance the results and provide further validation to this concept. The roof of York University's engineering building (Bergeron) could be used to provide light intensity to the PV arrays. From here the proposed converters could mounted to the back of each array or placed separately.
2. In the proposed power balancing topology discussed in Chapter 3, balanced output voltage is achieved through variable duty-ratio control. This voltage is distributed across the two the output capacitor voltage of the AVQ based on the turn-off time of the AVQ switch. It could be possible to modify the AVQ in such a way that both output voltage regulation and balanced output capacitor voltage can be achieved.

3. Many conventional energy systems make use of bi-directional converters such that energy storage systems such as batteries can stock up on additional power not required by the load or the grid. Others make use of different types of renewable energy sources such as wind energy to form hybrid energy systems. It would be interesting to test and see if the proposed work is compatible with different forms of generating or storage sources at the input of each module.

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Appendix A. List of Publications

A.1 Referred Journal Papers

J1. **K. Kanathipan** and J. Lam, “Coupled PV Step-up Resonant Converter Modules With An Enhanced Efficiency Optimization Scheme For the Power Balancing Stage” Submitted to IEEE Transactions on Power Electronics

J2. **K. Kanathipan** and J. Lam, “High Frequency Interlinking High Voltage Gain PV Converter Modules with Embedded Power Balancing Technique for DC-Distributed System” IEEE Journal of Emerging and Selected Topics in Power Electronics. Accepted Feb 2024

J3. **K. Kanathipan** and J. Lam, "A High Voltage Gain Isolated PV Micro-Converter With a Single-Voltage Maximum Power Point Tracking Control Loop for DC Micro-Grid Systems," IEEE Journal of Emerging and Selected Topics in Industrial Electronics, vol. 3, no. 3, pp. 755-765, July 2022

J4. **K. Kanathipan** and J. Lam, "An Electrolytic Capacitor-Less PV Micro-Inverter Based on CLL Resonant Conversion With a Power Control Scheme Using Resonant Circuit Voltage Control Loops," IEEE CPSS Transactions on Power Electronics and Applications, vol. 7, no. 2, pp. 139-149, June 2022

A.2 Referred Conference Papers

C1. **K. Kanathipan** and J. Lam, “Modular Soft-switched PV Converter with An Efficiency Optimization Scheme for High Frequency Linking Power Balancers” in Proc. of the 2024 IEEE Applied Power Electronics Conference and Exposition (APEC) Long Beach, CA, USA, 2024 pp. 1403-1408

C2. **K. Kanathipan** and J. Lam, “New Interlinking PV Converter Modules with Individual MPPT and Integrated Power Balance Units (AVQ)” in Proc. of the 2023 IEEE Energy Conversion Congress & Expo (ECCE) Nashville, TN, USA, 2023, pp. 6574-6576

C3. **K. Kanathipan** and J. Lam, “A Modular Step-up PV Converter With Coupled Output Power Balancers Utilizing A New Fully Soft-switched Active Voltage Quadrupler (AVQ)” in Proc. of the 2022 IEEE Energy Conversion Congress & Expo (ECCE) Detroit, MI, USA, 2022, pp. 1-6

C4. **K. Kanathipan** and J. Lam, "A Modular Single-Stage PV Step-up Converter With Integrated Power Balancing Feature Using Inter-Coupled Active Voltage Quadruplers," in Proc. of the 2022 IEEE Applied Power Electronics Conference and Exposition (APEC) Houston, TX, USA, 2022, pp. 2086-2091

A.3 Patent Applications

K. Kanathipan & J. Lam*, “Modular single-stage step-up PV converter with integrated power balancing feature*,” International Patent Application No. PCT/CA2022/050755, filed on May 12, 2022.

K. Kanathipan & J. Lam, *“Modular single-stage step-up PV converter with integrated power balancing feature,”* US Patent Application No. 63/194836, filed on May 28, 2021.

Appendix B. Printed Circuit Board (PCB) Layouts

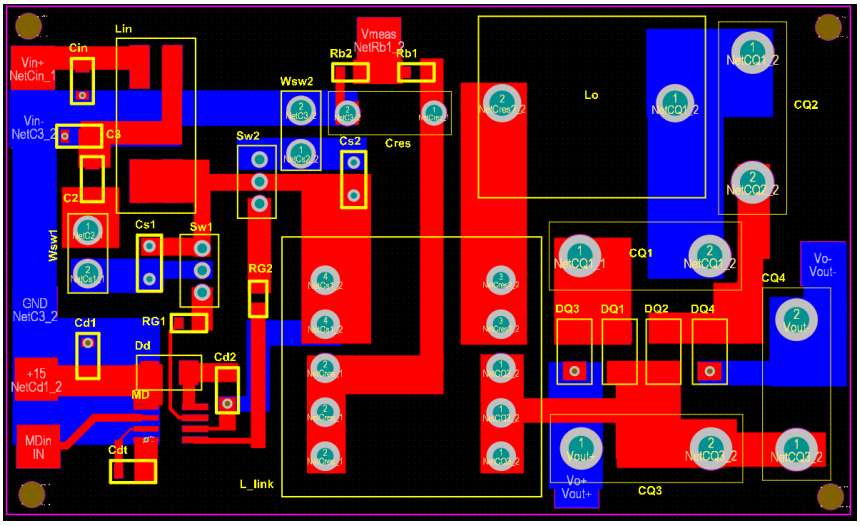

Figure B - 1: PCB Layout of the converter topology from Chapter 2

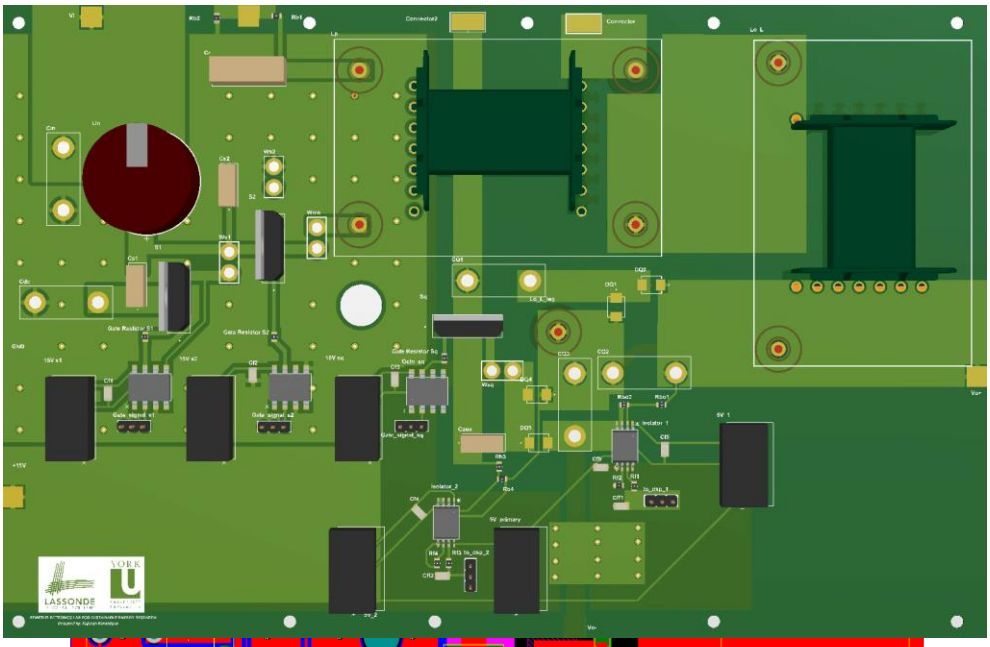

Figure B - 3: 3D view of the PCB Layout of a single module of the proposed modular converter topology

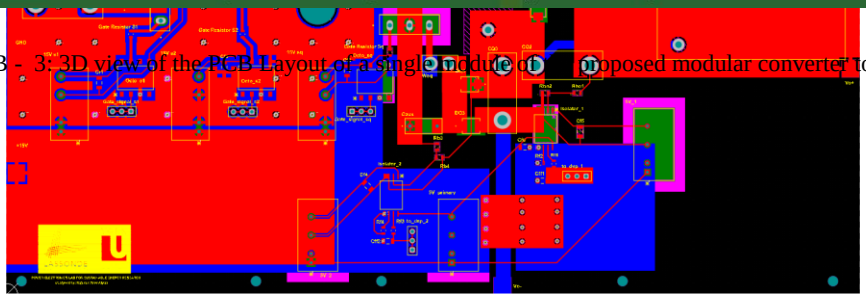

Figure B - 2: PCB Layout of a single module of the proposed modular converter topology utilized in Chapter 3

Appendix C. PSIM Schematics

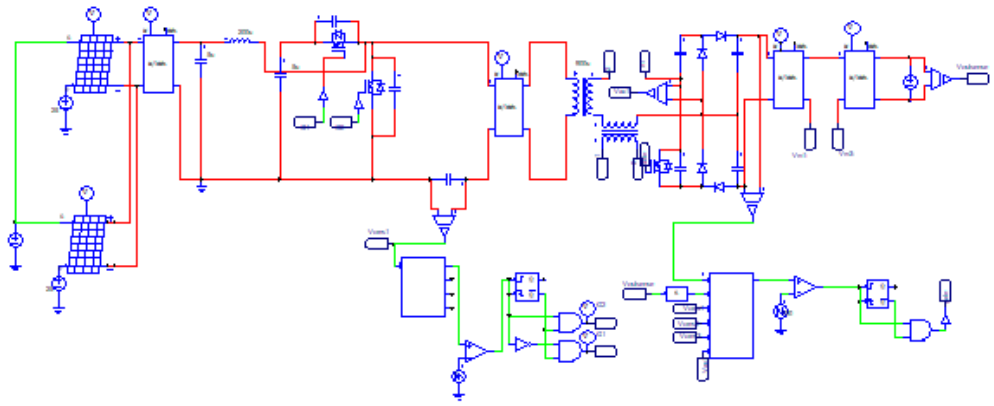

Figure C - 1: Diagram of a single module of the proposed modular converter topology from PSIM

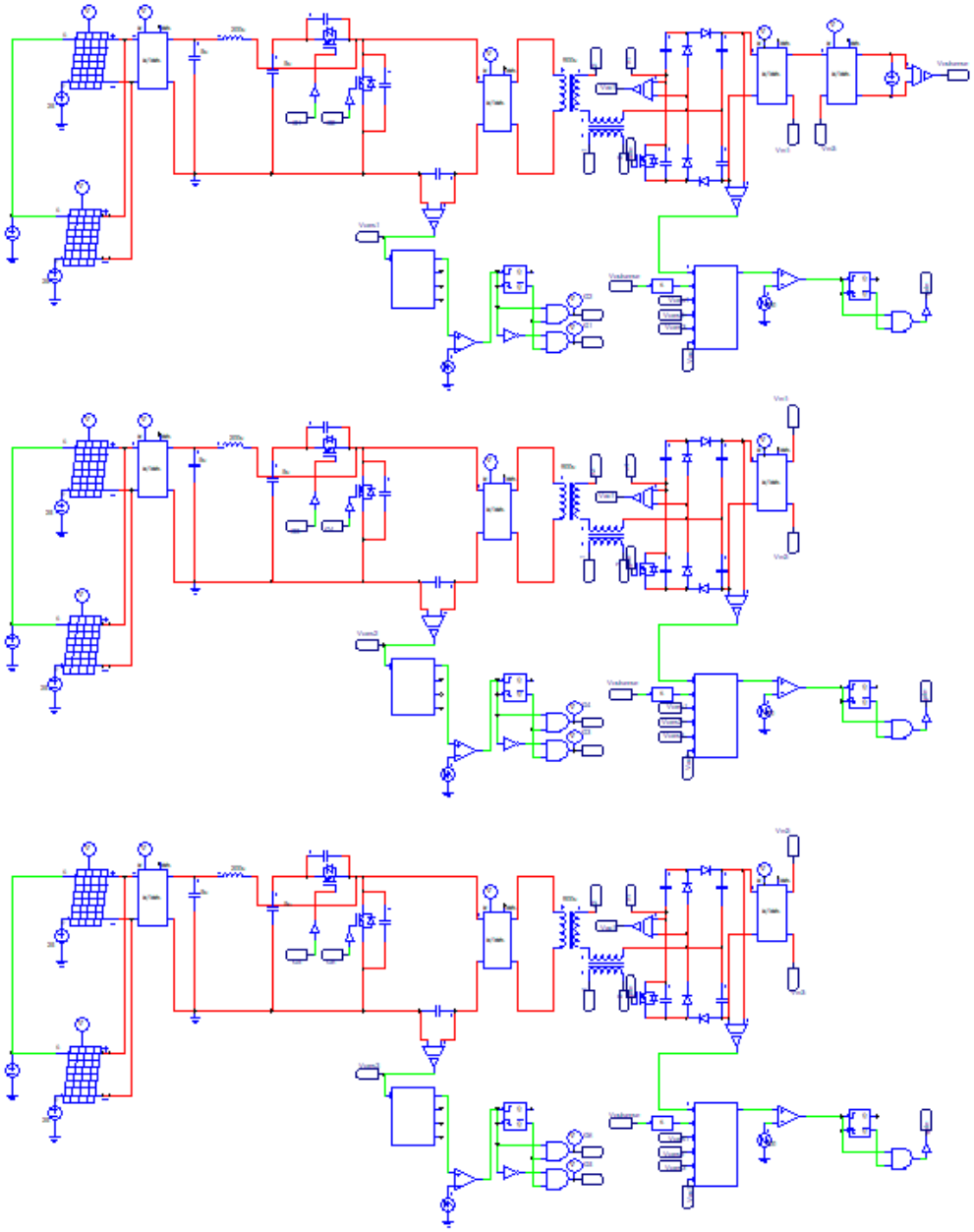

Figure C - 2: Diagram of a three-module configuration in PSIM