

**INTEGRATED ANALOG READOUT ARRAY AND DIGITAL
BACKEND FOR MOBILE DNA SEQUENCING**

YUNUS IBRAHIM DAWJI

A DISSERTATION SUBMITTED TO THE FACULTY OF GRADUATE STUDIES
IN PARTIAL FULFILMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

GRADUATE PROGRAM IN
ELECTRICAL ENGINEERING AND COMPUTER SCIENCE
YORK UNIVERSITY
TORONTO, ONTARIO

DECEMBER 2024

© Yunus Ibrahim Dawji, 2024

Abstract

DNA, a fundamental biomolecule, contains the genetic code that governs the development, functioning, and reproduction of all living organisms. It is composed of smaller molecular units called nucleotides. The process of determining the specific sequence of these nucleotides is known as DNA sequencing. An innovative approach to this is nanopore-based DNA sequencing. Unlike many other methods, nanopore sequencing detects DNA molecules directly, rather than relying on secondary phenomena, and can do so in real-time as the molecules pass through the device. This technology holds the potential to significantly democratize DNA sequencing, which could revolutionize medical diagnostics and personalized medicine, ultimately improving the lives of billions. This report focuses on optimizing the performance and cost-efficiency of nanopore-based sequencing, particularly by exploring the opportunities for implementing low-cost, integrated analog front-end arrays and application-specific accelerated digital back-end systems.

This thesis presents three iterative versions of a digital readout integrated circuit (DROIC), each enhancing *throughput density* through architectural and circuit-level advancements. The first version (DROICv1) employs a discrete-time (DT) amplifier with in-pixel successive approximation ADCs. The second version (DROICv2) increases *throughput density* using column-based ADCs. The third version incorporates an asynchronous reset amplifier, further enhancing *throughput density* by reducing amplifier noise.

To validate the system's functionality, the thesis demonstrates biological ion-channel

and solid-state nanopore measurements. It also introduces methods for post-processing the chip to enable on-chip sensors. Finally, a RISC-V-based digital basecaller is presented, optimizing the speed and energy efficiency of the digital backend.

Table of Contents

Abstract	ii
Table of Contents	iv
List of Tables	viii
List of Figures	ix
1 Introduction	1
1.1 First-generation Sequencing	2
1.2 Second-generation Sequencing	2
1.3 Third-generation Sequencing	4
1.3.1 Nanopore-based Sequencing	4
1.4 Thesis Outline	7
1.5 Chapter Summary	9
2 Review Of Nanopore-based Sequencing Frontends	10
2.1 Chapter Summary	10
2.2 Sensors	11
2.2.1 Nanopore Sensing Methods	11
2.2.2 Resistive Pulse Shaping	11
2.2.3 Transverse Currents	13
2.2.4 Optics and Plasmonics	14

2.3	Nanopore Sensor Structures	16
2.3.1	Biological Nanopores	16
2.3.2	Solid-State Nanopores	18
2.4	Signals	20
2.5	CMOS	23
2.5.1	Amplifiers	23
2.5.2	Continuous-Time CMOS Readout	25
2.5.3	Discrete-Time CMOS Readout	27
2.5.4	Arrays	29
2.6	Microfluidics	34
3	Digital Readout Integrated Circuit (DROIC)	38
3.1	Chapter Summary	38
3.2	Introduction	39
3.3	System Overview	39
3.4	Analog Front-End (AFE) Design	45
3.4.1	AFE Timing	51
3.4.2	AFE Signal and Noise Analysis	52
3.4.3	AFE Simulation Results	58
3.5	ADC	60
3.5.1	Simulation Results	69
3.6	System	71
3.7	Measurement Setup & Results	72
3.7.1	AFE Measurement Results	77
3.7.2	ADC Measurement Results	79
3.7.3	Complete Chain Digitized Result	81
3.7.4	Channel Interference	83
4	Digital Readout Integrated Circuit (DROIC) with Column ADCs	87

4.1	Chapter Summary	87
4.2	Introduction	88
4.3	System	88
4.4	Amplifier	91
4.5	ADC	92
4.5.1	LMS-Based Digital Calibration	95
4.6	Measurement Setup & Results	98
4.6.1	PCB Testboard	98
4.6.2	FPGA Readout System	101
4.6.3	System Measurement Results	103
4.6.4	Digital Calibration of the ADC	105
4.6.5	Coarse Offset Correction Using a Lookup Table	107
4.6.6	Amplifier and ADC Gain and Offset Calibration Combined	109
5	Asynchronous Reset Amplifier	111
5.1	Chapter Summary	111
5.2	Introduction	112
5.3	Amplifier Analysis	113
5.3.1	Noise Analysis	115
5.4	Simulation Results	115
5.5	Measurement	117
5.5.1	Measurement Setup	117
5.5.2	Asynchronous System Transient	117
5.5.3	Asynchronous System Noise	118
6	Ion-channel and Solid-state Measurements	122
6.1	Chapter Summary	122
6.2	Introduction	123
6.3	Biological ion-channel experiments	124

6.3.1	Gramicidin Ion-channel Activity	127
6.4	Solid state measurement	128
6.5	On-Chip Post-processing	132
7	Digital Back-end - Basecaller	135
7.1	Chapter Summary	135
7.2	Introduction	136
7.3	Background	138
7.3.1	Rocket Core	138
7.3.2	Rocket Custom Co-processor Interface	139
7.4	Design and Architecture	140
7.4.1	Specifications	140
7.4.2	System Organization	142
7.4.3	Accelerator (ACC) Design	143
7.5	Implementation and Measurements	146
8	Conclusion	150
8.1	Contributions	150
8.1.1	DROIC	150
8.1.2	Digital Backend Basecaller	152
8.2	Publications	154
8.3	Future Work	155

List of Tables

2.1	Nanopore-Relevant DT and CT AFE Performance Comparison	30
2.2	A summary of CMOS array approaches and performance levels for nanopore based sequencing.	34
3.1	Gain and bandwidth options for components in each channel	48
3.2	Simulated dynamic performance of ADC with BW-DAC & AC-DAC .	70
3.3	Performance summary for the nanopore detector array	72
3.4	SNR & SINAD for various amplitude input voltage.	80
3.5	Gain and open-input input referred noise for various gain and filter settings	83
4.1	Opcode for controlling the functions on board via the GUI using UART	100
7.1	Custom command functions implemented by the accelerator	146
7.2	State descriptions for state machine shown in Fig. 7.10	147
8.1	Performance comparison with state-of-art nanopore arrays and amplifiers	151

List of Figures

1.1	Double helix structure of the DNA. [1]	2
1.2	Illustration of SGS process [1].	3
1.3	Illustration of nanopore-based sequencing process [1].	5
1.4	Block diagram of a miniature DNA sequencer's main components.	5
2.1	Examples of biological nanopore designs.	18
2.2	A rough illustration of what the nanopore current from a single DNA measurement looks like. The region between 55 and 116 pA is indicative of the signal when DNA is translocating through the pore.	20
2.3	Transimpedance amplifier (TIA) main topology arrangements for current-based sensor readout. a) Resistive feedback TIA b) CT capacitive feedback TIA c) DT capacitive feedback TIA	25
2.4	Illustration of the readout noise on amplifier output [2]	32
2.5	Distortion free readout techniques for a nanopore readout array (recreated from [3])	33
2.6	Painting bi-layer on a teflon microaperture [4]	34
2.7	Illustration of monolayer droplets forming a DIB [5]	35
2.8	Pore formation method using amphiphilic molecules used by oxford nanopore [6]	35
2.9	Pore formation method using synthetic lipids used by oxford nanopore [6]	36

2.10	Example setup of microfluidic nanopore system [6]	37
3.1	Simplified overview of system for nanopore readout (Only three rows and three columns have been shown to keep the image simple)	43
3.2	The DT analog front-end (AFE). This analog signal processing system consists of three main components: the TIA, the LPF, and the CDS.	46
3.3	The TIA in more detail. Input, reset and capacitor gain bank and programming switches are indicated.	48
3.4	Transistor-level schematic of the folded cascode OTA used in the TIA.	49
3.5	G_m -C filter transistor-level schematic.	50
3.6	CDS component for each channel of the AFE with gain options determined by the C_1 capacitor bank settings.	51
3.7	Illustration of the TIA output (related to the voltage across C_F) (left) and the timing of the clocks driving the TIA's reset switch (right). A high clock signal implies the switch is closed, while a low clock signal implies the switch is open.	52
3.8	Equivalent circuit of the AFE's first-stage integrator opamp with input-referred opamp noise.	53
3.9	Integrator opamp noise model	54
3.10	CDS equivalent circuit	54
3.11	Signal transfer function of the DT-TIA.	56
3.12	a) Input referred noise of DT-TIA. b) SNR with respect to signal bandwidth for DT TIA model.	56
3.13	(a) Integrated input-referred noise with respect to opamp thermal noise floor at 10 kHz sampling rate, 5 pF input capacitor and 20 fF integrator feedback capacitance (b) major noise contributors [in percentage] with respect to the opamp thermal noise floor.	57

3.14 (a) Simulated gain of the TIA and (b) simulated input referred noise of the TIA.	58
3.15 Eye-diagram of AFE transients with noise from form the integrator, filter, and CDS included.	59
3.16 SAR ADC block diagram.	61
3.17 Illustration of a 5-bit analog-to-digital conversion by a SAR ADC. . .	61
3.18 Initial DAC configuration during sampling phase	63
3.19 DAC in second bit conversion when $MSB = 0$	65
3.20 DAC in second bit conversion when $MSB = 1$	65
3.21 Split Attenuated DAC	66
3.22 DAC layout for SAR ADC with routing consideration [7].	67
3.23 Class AB latched comparator schematic.	68
3.24 a) Transient Output of $(251/512) * 100\text{-kHz}$ input sine wave with 1V pk-pk b) Spectrum of $(251/512)*100\text{-kHz}$ input sine wave with 1V pk-pk.	70
3.25 Histogram of ENOB for matched capacitive BW-DAC only generated using MC simulation.	70
3.26 a) Gain of the latched comparator b) Output noise of the latched comparator	71
3.27 Latch comparator noise cumulative distribution simulated to measure integrated noise	72
3.28 Layout of the complete chip.	73
3.29 Chip micrograph and detailed floorplan of a channel.	74
3.30 Custom two wire interface protocol for readout.	75
3.31 DROIC readout system implemented on Zynq FPGA.	75
3.32 Block diagram for <i>sampler</i> IP	76
3.33 TIA test setup block diagram.	77
3.34 PCB testbench for DROICv1	77

3.35	Transient output of integrator, LPF and CDS for a 10 pA DC input current.	78
3.36	Transient output of the integrator at different gain settings for a 10 pA DC input current to the AFE.	78
3.37	Transient output of CDS at different gain settings for a 10 pA DC input current to the AFE.	79
3.38	a) Transient output for constant input voltage (550 mV). b) Spectrum of ADC output for constant input voltage (550 mV).	80
3.39	ADC output voltage for (1999/4096)·125 kHz sine input sampled synchronously.	81
3.40	SNR for ADC at 550 mV pk-pk (1999/4096)·125 kHz sine input near the Nyquist frequency.	81
3.41	SINAD for ADC at 550 mV pk-pk (1999/4096)·125 kHz sine input near the Nyquist frequency.	82
3.42	Transient output for multiple channels operating in parallel.	84
3.43	Spectrum of multiple channels operating in parallel.	84
3.44	Timing diagram for serial ADC operation scheme.	85
3.45	Timing diagram for parallel ADC operation scheme.	85
3.46	Temporal responses to sine wave input (100 pA) for parallel and serial operation modes.	86
3.47	Spectra responses to sine wave input (100 pA) for parallel and serial operation modes.	86
4.1	A simplified overview of a nanopore readout system based on column-ADC arrangements. Only four rows and three columns have been shown to keep the image simple.	89
4.2	DROICv3 chip layout	90
4.3	Timing diagram for the DROICv2 array readout.	91

4.4	Miller-compensated two-stage opamp schematic.	92
4.5	Metal-on-metal (MOM) unit capacitor physical arrangement.	93
4.6	DAC capacitor bank layout.	94
4.7	SAR ADC block diagram with added pre-amplifier	94
4.8	Block diagram with LMS based ADC calibration.	97
4.9	PCB testboard for DROICv2	98
4.10	PCB ground plane cutout as a RF choke to minimize noise from oscillator	99
4.11	PCB ground plane cutout under amplifier inputs to reduce effect of ground fluctuations	101
4.12	Block diagram of DROICv2 FPGA readout system	102
4.13	Input referred noise at various front-end settings.	105
4.14	Input referred noise, integrated noise and transient output for solid state nanopores	106
4.15	SNDR plot before calibration.	106
4.16	SNDR plot after calibration (calibration with a 10-Hz signal).	107
4.17	LMS calibration error vs iteration.	107
4.18	Coarse offset correction showing before and after offset cancellation for three channels	108
4.19	Block diagram for LMS based correction with AFE & ADC	110
4.20	Digitized output corrected for amplifier & ADC gain and offset error across 3 channels.	110
5.1	Asynchronous DT capacitive feedback AFE.	113
5.2	Illustration of the amplifier output (left) and phase timing (right) for the amplifier	113
5.3	Timing diagram for asynchronous reset amplifier.	114
5.4	Asynchronous reset amplifier vs. synchronous rest amplifier gain com- parison.	116

5.5	Asynchronous Reset amplifier vs Sync Reset Amplifier noise spectral density	117
5.6	Async amplifier noise density wrt. input capacitance	118
5.7	Raw output for 100-pA square wave input sampled at $F_s = 148.8$ kHz.	119
5.8	Process transient output for a 400-pA square wave input sampled at $F_s = 148.8$ kHz.	119
5.9	Asynchronous noise with respect to the reset frequency. Input capacitance = 100 pF and $F_s = 100$ kHz.	120
5.10	Asynchronous noise with respect to the sampling frequency. Input capacitance = 100 pF and $F_s = 10$ kHz.	120
5.11	Open input noise for $F_s = 30$ kHz and 148.8 kHz.	121
6.1	Test apparatus and fluidic chamber used in lipid bilayer experiments .	124
6.2	Noise spectrum for a lipid bilayer at 14 kSps and 3.5 kSps sampling frequencies.	126
6.3	Ion-channel integrated noise vs. bandwidth for an input capacitance of 40 pF and $F_s = 3.5$ kHz.	126
6.4	Gramicidin ion-channel activity illustration.	127
6.5	Gramicidin ion-channel activity in KCl buffer filtered at 1000 Hz. . .	128
6.6	Three different substrates used in solid state experiments.	129
6.7	Solid state experiment setup	129
6.8	Transient output for PDMS-covered substrate for a 200-mV triangular input at frequencies of 150 Hz and 300 Hz.	130
6.9	Transient output for a PDMS-exposed substrate. The input was a triangular wave with 20 mV and 40 mV pk-pk amplitude and 100-Hz frequency.	131
6.10	Input referred noise for substrates measured at 36 kSps.	132
6.11	Integrated noise with respect to bandwidth.	132

6.12	Post processing of the chip to remove aluminium and deposit Ag/AgCl	
	a) Micrograph of chip with aluminium electrode before etching b) Micrograph of chip after etching aluminium electrode c) Micrograph of chip after electroplating Silver	133
6.13	Output current injected through Ag/AgCl pad and 1-G Ω resistor. . .	134
6.14	Input referred noise for Ag/AgCl pad and 1G Ω resistor.	134
7.1	Block diagram of a miniature DNA sequencer's main components. . .	137
7.2	The four basic types of RISC-V instructions	138
7.3	The RoCC Interface showing the default Interface (in black) and the extended Interface (in red).	139
7.4	The custom instruction format	140
7.5	Exploratory embedded sequencing SoC organization overview.	142
7.6	a) A bioinformatic analysis for base extraction from ASIC output, b) it implmentation in ACC hardware, c) implementation of the SoC on a test board.	143
7.7	a) Micrograph of test chip with floorplan of accelerators highlighted b) Backside of the chip package showing the BGA [8] c) BGA pinout for the package [8] d)The packaged SoC within its test system.	144
7.8	The interface between RoCC Interface Controller and Basecaller . . .	146
7.9	State machine for processing custom command issued to configure and execute basecaller	147
7.10	State machines for reading and writing on memory RoCC interface .	147
7.11	Measured basecalling speed as a function of clock frequency.	149
7.12	Ratio (red) of SoC efficiency to optimal ARM A53 efficiency and associated (black) minimal SoC supply voltage settings.	149
8.1	Layout of following chips developed with digital design framework . .	153

Chapter 1

Introduction

Sequencing is a measurement and analysis process aimed at identifying the continuous sequence of nucleotide molecules that make up DNA strands. For example, genes can consist of collections of thousands of nucleotides in series. Distinctive molecular sub-parts of nucleotides are called nucleobases, or ‘bases’ for short. The four unique bases that comprise DNA are called/abbreviated: adenine (A), cytosine (C), guanine (G), and thymine (T). In their natural organic state, a single contiguous DNA molecule may span many millions of bases. Current physical limitations and various experimental requirements often result in shredded DNA molecular samples that may span dozens, hundreds, or thousands of bases. The result of a typical DNA sequencing measurement run on such strands will comprise many files filled with text sequences of chemical base name abbreviations as noted above. Naturally, accounting for measurement error, these lines of text should correspond closely to the physical base sequences of the DNA strands that were measured.

Sequencing has become a key tool in basic biological research, medical diagnostics, forensics, drug development and virology. Recently, research in using DNA for data archival has expanded [9], an interest at least partly driven by the technological advances experienced by DNA sequencers, a key element in DNA data archival.

Forty years ago state-of-the-art sequencing technologies could process about 100

bases/day. For reference, the human genome consists of a total of about six billion bases (arranged as three billion complementary ‘base pairs’) [10]. By 2005, after the human genome project, so-called ‘next generation sequencing’ (NGS) machines emerged with throughput capabilities of 10^6 bases/sec. Upcoming sequencing technologies are extending these metrics, including the ability to handle very long uninterrupted DNA samples (i.e. “long reads”) and to operate outside the lab in an extremely miniaturized form. DNA sequencing technology has seen three major generations.

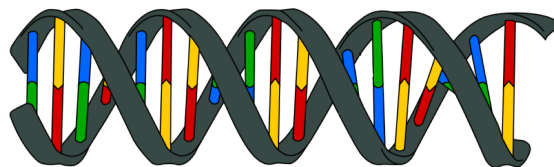


Figure 1.1: Double helix structure of the DNA. [1]

1.1 First-generation Sequencing

In 1977, A.M. Maxam and W. Gilbert described chemical degradation method for determining the sequence of fragmented DNA while Sanger proposed an enzymatic method (the dideoxy chain termination method). First generation technologies could read up to 1000 bases in length with 99.999% accuracy. The cost of the Sanger methodology was about \$1 per kilobase which means \$6 million to sequence a human genome [11].

1.2 Second-generation Sequencing

Second generation sequencing (SGS) used highly parallel short reads to drastically increase throughput. In SGS, two main approaches were used: sequencing by synthesis (SBS) and sequencing by ligation (SBL) [12]. SBS uses a polymerase to synthesize a

fragment of DNA one base at time. The signal is read out in the form of a fluorescence or a charge. In SBL, oligonucleotide attached to a fluorophore is used as a probe sequence. These probe sequence hybridizes with DNA fragment which is readout in form of fluorescence. [1, 13]. SGS does not need host cells to create copies of DNA as FGS technologies. Instead they are attached to beads or solid surfaces to perform library amplification. SGS have very high accuracy but suffers from short reads (100 to 200 base pairs). Short read lengths makes the ensuing assembly process computationally intensive. SGS revolutionised the speed of sequencing by allowing the implementation of a parallel high throughput system. For example, as early as 2005 1.2M strands could be sequenced in parallel [14].

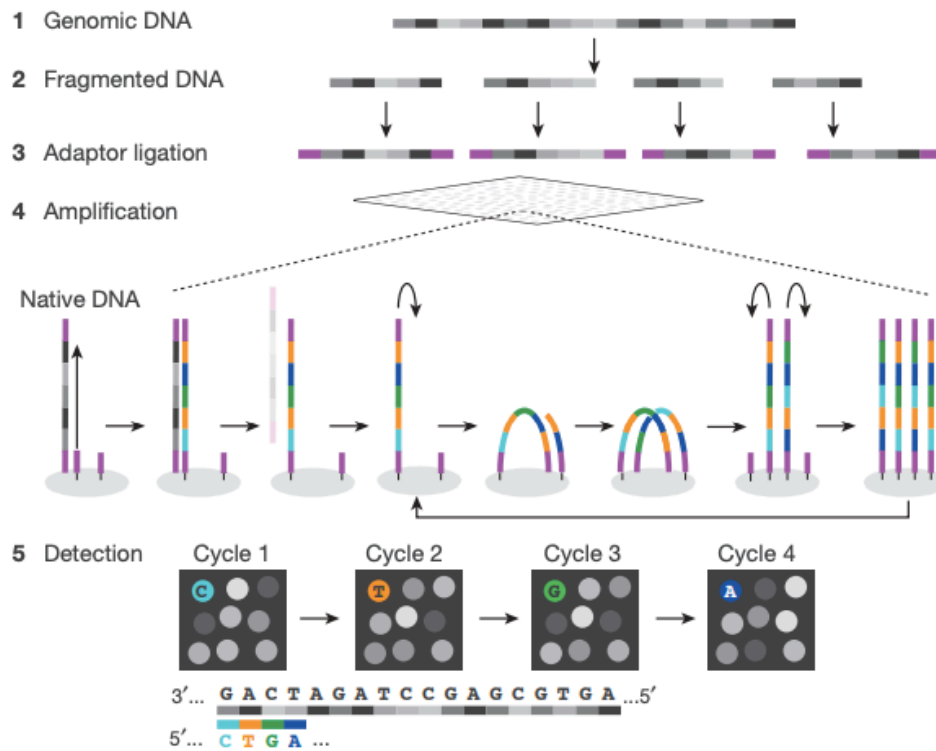


Figure 1.2: Illustration of SGS process [1].

1.3 Third-generation Sequencing

Third-generation sequencing (TGS) technologies focus on single molecule sequencing to reduce cost and chemical processing needed for sequencing. The most successful TGS is nanopore based sequencing from Oxford Nanopore Technologies (ONT). Single-molecule real-time (SMRT) sequencing by Pacific biosciences and Helicos sequencing by the Genetic analysis system are two other key TGS technologies [15].

1.3.1 Nanopore-based Sequencing

Nanopore sequencing uses nanopores (biological and solid-state) to find the order of nucleotide by electrically measuring the motion of a DNA through it. Generally speaking, nanopores are nanometer-sized apertures that, by virtue of their minute physical dimensions, direct molecules to very fine spatial locales. Electrically, nanopores are used as voltage-clamp sensors. A constant voltage is applied across the nanopore to setup a ionic current through the pore. As indicated in Fig. 1.3, such sequencing systems thread (translocate) DNA through the nanopore; in the process the ionic current is modulated in some – usually complicated – relationship to the string of *base* molecules (represented by the ‘A, C, G, T’ text) comprising the DNA. Ensuing signal processors convert the modulated signal to the DNA’s base-equivalent text. Arguably the most prominent success to-date of nanopore-based molecular measurement resides in its central role in commercial DNA strand sequencing machines [16, 17].

Fig. 1.4 presents a block diagram of the essential components in a modern compact DNA sequencing system. The printed circuit board (PCB) contains several key chips: a sensor array that converts DNA molecules into electrical signals; a mixed-signal ASIC that amplifies, filters, and digitizes these signals; an FPGA that manages, buffers, and organizes the processed data; and a USB interface chip that transfers the gathered DNA data off the device.

Limitation and Opportunities

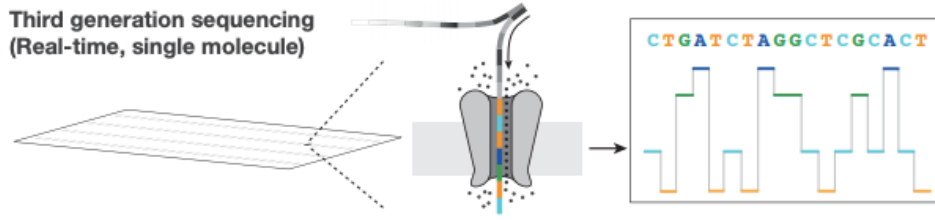


Figure 1.3: Illustration of nanopore-based sequencing process [1].

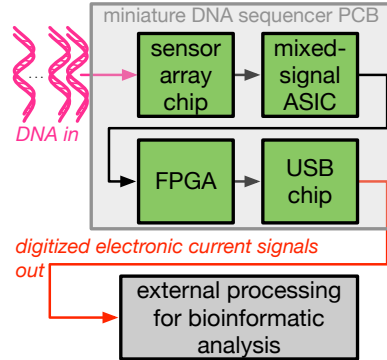


Figure 1.4: Block diagram of a miniature DNA sequencer's main components.

Mixed Signal Readout Array - Since the first published proposals and demonstrations of the nanopore approach to molecular sensing in the mid-90's [18, 19] using α -hemolysin (α HL) proteins, the literature has seen a vast proliferation in structures, methods, and applications of this technique. Although it has been the subject of interesting developments in recent years, relatively muted has been a overview look at the electronic signal-conditioning instrumentation to which such sensors are, or may be, interfaced. But this is a critical component of the nanopore sensing system as the perceived limitations of such circuits (e.g. in throughput, sensitivity, speed, etc.) are often rightly cited as motivation for the introduction of new sensory innovations exploiting ever more exotic combinations of material arrangements and sensing modalities (e.g. tunnelling currents in place of ion blockades). Of particular interest is the state of purely microelectronic readout solutions implemented entirely in complementary metal oxide semiconductor (CMOS) technology for these hold the means by which the most advanced nanopore-based sensing systems, in the form of biochips, may be realized.

The MinION is a portable nanopore-based DNA sequencer produced by ONT. It

weighs 90 grams and is 10 cm in length along its largest dimension. It can currently process DNA at rates of 170 kbp/s (0.25 human genomes/h), a $15\times$ improvement over the technology’s first commercial release in 2014. For context, this throughput is $100\times$ slower than “mainframe” sequencing machines (which themselves are $1000\times$ bigger and costlier) [20].

A MinION incorporates 2048 nanopores arrayed in a small microfluidic chamber about 1 cm on-a-side. These sensors are multiplexed to 512 analog amplifier channels [20, 21]. DNA introduced into this machine translocates at 450 base-pairs/sec (bp/s) (in R10.3) while the analog frontend (AFE) has sample rate of 4 kSps. This means about 10 sample are taken for each k-mer. This nanopore sequencer performance is achieved with the help of a 140 mm^2 CMOS AFE [22] while consuming roughly 2 mW per channel. The area of each channel is about 0.28 mm^2 ($140\text{ mm}^2/512$).

The performance of an amplifier (and analog-to-digital converter (ADC)) can be quantified using “throughput density”. Throughput density is the speed of sequencing (bp/s) per sq. mm of chip area at a particular signal to noise ratio (SNR). A number of capable designs have been proposed in the literature so far [23–27]. All these designs focus on improving the throughput density by increasing the bandwidth of the amplifiers. Moreover, none of the works have attempted a multichannel integrated array with on-chip ADC. The MinION achieves a peak measurement throughput of $1,700\text{ bp/s/mm}^2$ with at least 20 dB SNR. I have developed systems that exceed the current nanopore sequencer throughput density’ record of 1,700 base-pairs-per-second (bp/s) per sq. mm of chip area. Higher translocation frequency would increase throughput density of the system. This can be achieved by improving the SNR of the amplifiers. One can also improve the throughput by increasing the number of parallel channel. This can be achieved by reducing area and power consumption of each channel.

Digital Backend Processor - A mobile DNA sequencing solution requires an

energy-efficient and sophisticated computing device co-located with the DNA sensing and measurement hardware. The existing miniature sequencers do not presently contain any substantial embedded computing, and thus themselves do not carry out any bioinformatic analysis on the measurements they pass through their chassis. Consequently, as Fig. 1.4 shows, for any relevant analysis of DNA equivalent currents, the data must be sent to some external processing resource (e.g., desktop, laptop, cloud, etc.). A standard device has a maximum rated power of 4.5 W with an average draw of about 1 W [28], values on-par with typical smartphone power draw. Clearly, the lower this requirement gets, the more suitable the device becomes for mobile applications. I approximate that if added computing resources use less than a tenth of nominal power, they will serve as practical additions towards future mobile applications. Therefore at present I seek SoCs that can operate below 100 mW. For this purpose, I present a highly energy efficient RISC-V 64-bit application system taped-out in GlobalFoundries 22-nm FDX technology. Among its ability to process generic programs in realtime our system incorporate a specific bioinformatics accelerator. It is worth mentioning that, to the best of my knowledge, my solution was found to be the only embedded basecalling implementation until writing this thesis. Other implementations adopted a standalone hardware accelerator (i.e., based on FPGA or GPU) working in tandem with x86 processor. Our basecalling processor strikes a relatively better balance between performance and energy consumption compared to existing solutions.

1.4 Thesis Outline

Chapter 2 provides a review of nanopore frontend. The chapter provides a comprehensive review of nanopore-based sequencing frontends, focusing on the nanopore types and different sensing methods used in nanopore technology. It also delves into CMOS amplifiers and readout circuits, examining continuous-time and discrete-time designs,

and their role in enhancing signal fidelity and bandwidth. Finally, it addresses the integration of nanopore sensors with microfluidics, exploring techniques for forming lipid bilayers and the scalability issues related to high-throughput sequencing systems.

Chapter 3 describes a ROIC array design (DROICv1) geared for nanopore-based DNA sequencing systems which I refer to as a digital/discrete ROIC (DROIC) to emphasize the design choices made as part of its realization. DROICv1 shows a 30 channel array with in-pixel architecture.

Chapter 4 explore the evolution of the Digital Readout Integrated Circuit (DROIC) architecture, highlighting key advancements from DROICv1 to DROICv2. To address these limitations, DROICv2 introduced a 106 channel column ADC architecture, significantly enhancing throughput density. This design reduced the average area per channel and improved the system performance.

Chapter 5 introduces a novel amplifier design building on the knowledge of discrete time amplifier that employs an asynchronous reset technique to enhance noise performance. Here, I present a digital differentiator based approach which significantly improved power and area efficiency. Reducing area and power are imperative to build a high throughput readout array.

Chapter 6 focuses on the experimental validation of a readout channel design through biological ion-channel and solid-state nanopore measurements. I also present on-chip post-processing, which describes the fabrication of Ag/AgCl electrodes directly on the chip.

Chapter 7 addresses the increasing use of miniature DNA sequencers and the challenges posed by their lack of embedded computing for on-board bioinformatic analysis. To overcome this limitation, I present the design and implementation of a system-on-chip (SoC) that integrates digital computation directly within the sequencing device.

Finally, Chapter 8 provide summary of contribution, publications and directions

for future work.

1.5 Chapter Summary

This chapter introduced the current and emerging sequencing technologies and its application. It also introduced nanopore-based sequencing and its limitations & opportunities for research in this field.

Chapter 2

Review Of Nanopore-based Sequencing Frontends

2.1 Chapter Summary

The chapter provides a comprehensive analysis of the various sensing methods, sensor structures, and readout techniques used in nanopore-based sequencing technologies. I begin by discussing key nanopore sensing approaches, such as resistive pulse shaping (RPS), transverse current detection, optics, and plasmonics, with a detailed focus on the advantages and challenges of the RPS method, which remains dominant due to its simplicity and commercial success. I further examine the structural evolution of nanopore sensors, distinguishing between biological nanopores—like protein-based designs—and solid-state nanopores (SSNs), highlighting their distinct advantages in molecular resolution and scalability. Amplification and signal conditioning methods, critical for translating ionic current into digital signals, are explored through continuous-time and discrete-time designs, emphasizing noise reduction and bandwidth optimization strategies. Finally, the integration of nanopore sensors into CMOS arrays and the role of microfluidic platforms in enhancing stability and performance are addressed, showcasing the technological advancements and practical challenges

shaping the future of nanopore-based sequencing systems.

2.2 Sensors

2.2.1 Nanopore Sensing Methods

Nanopore-based particle sensing is currently being pursued along several main lines of study: resistive pulse shaping (RPS), transverse current detection, optics, and plasmonics. I briefly outline these avenues below, emphasizing the advantages still available to the more mature RPS approach.

2.2.2 Resistive Pulse Shaping

The RPS sensing method is conceptually the simplest means of using nanopores to elucidate molecular structure. Perhaps for this reason it was the first nanopore sensing modality to achieve a relevant commercial impact [29]. Nanopore RPS works by immersing the nanopore sensor in an electrolyte solution across which a DC voltage V_{dc} is applied. This potential prompts the solution’s ions to flow through the sensor, as illustrated above in Figure 1.3, resulting in a small baseline DC current

$$I_{base} = G_p \cdot V_{dc} \quad (2.1)$$

where $G_p = G_{dc}$ is the equivalent conductance of the pore under DC conditions. I_{base} and G_p depend on the nanopore’s construction, V_{dc} , and ionic solution with typical molecular sensors (ranging across biological and solid-state nanopore constructions) operating between about 0.1 and 30 nA [30] and $1/G_p = R_p$ between about 0.1 to 5 G Ω . Detailed models for G_p (as well as the conductance blockade ΔG_t noted below) and the physics motivating them are discussed in [31–33].

When a molecule translocates through the pore it impedes the baseline flow of ions through the sensor, reducing the conductance of the pore by ΔG_t in some relation to

the molecule’s fine structure (again, Figure 1.3 conveys this in an abstract manner), thus resulting in

$$G_p = G_{dc} - \Delta G_t. \quad (2.2)$$

During these periods of occlusion the current through the pore becomes

$$I_p = I_{base} - \Delta I_t = I_{base} - \Delta G_t \cdot V_{dc} \quad (2.3)$$

where ΔI_t is the translocation blockade signal, the perturbation used to infer the blocking molecule’s structure. Relative blockades, $\Delta I_t/I_{base}$, around 0.5 are typically observed in DNA experiments [34].

Ideally, the smaller the nanopore, the more accurately the RPS method can be used to resolve the structure of translocating molecules. Practical pores have facilitated this by achieving diameters as small as 2 nm. However, the reported thickness, t , of these openings has tended to be larger and the prospect of reducing it below the critical feature spacing in complex molecules such as DNA (e.g. ~ 0.34 -nm) is daunting. Typical commercial-grade nanopore thickness may be on the order of 10 nm which means that in an RPS scheme as many as 30 bases may be simultaneously contributing to the blockade current. Having this many simultaneous contributors to the blockade signal is a clear challenge to signal fidelity and downstream signal processing.

A straightforward attempt to address this problem, that of increasing the signal amplitude (and thus the ability of sophisticated detectors to discern complex patterns) via a boost in V_{dc} and hence ΔI_t , is frustrated by the associated increase in DNA translocation rate, f_t , measured in base-pairs per second (bp/s). Although the signal’s amplitude grows its broader spectral profile forces the readout circuitry to accumulate more noise as well.

2.2.3 Transverse Currents

Inspired by the aforementioned issues with nanopore RPS, researchers have proposed and pursued alternate nanopore-based excitation strategies, one being a lateral excitation apparatus. Specifically, by embedding electrodes at opposite sides of a nanopore opening, it was suggested that a fine quantum tunnelling current could be made to flow across the pore [35], perpendicular to its opening. In theory, any ensuing disruption of this transverse current by molecule components moving through the hole could be used to identify the translocating particle in great detail. For instance, electronic transport simulations assuming a 1.5-nm tunnelling gap between graphene electrodes biased at 1 V predicted mean current fluctuations on the order of 10^{-4} , 10^{-5} , 10^{-2} , 10^{-6} pA for bases A, C, G, T, respectively [36]. An excellent recent review of this approach is provided in [37]. This approach also benefits by decoupling the force that drives the molecule through the pore, V_{dc} that is, from the measured signal. Thus may the translocation of the molecule to be slowed without reducing the size of the signal indicative of the molecule’s structure.

Experimental efforts in this direction have resulted in the ability to elicit signals on the order of 100 pA (albeit with noise fluctuations on the same order) from individual (dissolved in a fluid) DNA bases [38, 39] thus strongly demonstrating the capability of this technology for DNA sequencing. Efforts to measure contiguous polymer chains were also successful, although unable to discern the underlying structure of the molecule [40]. Until now, this method has not met with the success achieved by RPS although this may also be a reflection of the great degree to which industry has attempted to solve the myriad of complications associated with practical RPS nanopore systems.

Along similar lines, researchers have been keen to exploit nanowire-like field-effect transistor (FET) measurement methods, these having previously been demonstrated for sensitive real-time chemical detection [41]. Such technologies themselves have

been inspired by the famous ion-sensitive FET (ISFET) approach [42], and, besides improved signal quality, hold the potential for achieving extremely dense sensor arrays. In analogy to the tunnelling modality described above, FET-nanopore devices also rely on the modulation of a transverse current as an indicator of molecular make-up. Structurally, nanopore FETs consist of a semi-conductive material, a nano-channel, in close proximity to (or surrounding) a nanopore. A current is established through this conductor, but instead of molecularly modulating it via the re-arrangement of quantum states (as with conventional tunnelling methods), rather the expectation is that charge on the molecule is screened by charge in the nano-channel. As the molecule translocates the pore, in close proximity to the nano-channel, this screening should theoretically modulate the transverse current in ways unique to the passing molecule’s make-up [43].

However, ensuing experimental investigations implied a different physics at work in these devices [44, 45] than that outlined above. Likely due to the highly conductive ionic solutions, it was estimated that, in place of variations in the local density of states driving modulations in the transverse current, changes in the local potential of the fluid itself (caused by molecule translocation through the pore) were sensed by the nano-channel. Although this approach relies on a signal derived from the contribution of the molecule as a whole (or at least some subset of it), and thus undercuts somewhat an initial motivation for the use of transverse current modalities (i.e. finer resolution of molecular structure), it still holds excellent potential for improved signal and bandwidth performance over RPS methods [46].

2.2.4 Optics and Plasmonics

As applied to DNA sequencing, optical methods based on polymerase-assisted addition of fluorescently labelled nucleotides are presently the dominant means of molecular measurement [47, 48]. In the commercial market, coupled with the *sequencing-by-*

synthesis (SBS) approach, these optical methods appreciably exceed the raw accuracy currently demonstrated by nanopore-based sequencers. This benefit stems from the superior signal-to-noise ratio (SNR) afforded by SBS at the cost of real-time functionality and direct molecular measurements (i.e. PCR-based molecular amplification is required excluding the ability to directly measure unaltered source molecules).

Workers have sought to port this sensing modality to nanopore platforms as well without compromising the single-molecule-detection and real-time processing advantages of deployed RPS nanopore solutions. At the moment the added benefits of this approach seem marginal; unlike purely current-based methods, proposed optical techniques require substantial tampering with the molecular analyte (e.g. expanding each nucleotide into multiple copies) to make room for fluorescent probes intended to work in a nanopore context [49]. However, such structural sequence dilations would effectively address the resolution challenges of RPS approaches as well and without the need to resort to bulky optical hardware (mainly for fluorescent probe excitation by laser). Nonetheless this optical method has been demonstrated [50] and may serve as a useful complementary means of measurement to help deal with the accuracy challenge currently faced by RPS.

The presumed ability of optical methods to simultaneously address multiple sensors has been noted as another of its benefits and has motivated a label-free optical sensing approach (based on Ca^{2+} induced photonic intensity) [51]. Although the opportunity to map a large array of nanopore-molecule reactions onto an imager is interesting, its advantage over pure electronic readout (as in RPS) is not obvious given the present and evolving technological landscape; ultimately all readout methods face the need to separately address individual or small groups of measurement sites (due to limits on the number of available pinouts from a chip). And although established SBS methods require optical pixel areas roughly $100\times$ smaller than those needed for RPS systems, the signals they receive may originate from 1,000 copies of the same nucleotide, real-time nanopore-based sequencing methods, as single-molecule sensors,

do not accommodate such redundancies.

Of qualitative similarity to the tunnelling current method are plasmonic nanoantennas which focus laser light into sub-diffraction limited “hotspots” that may be monitored by an imager. Locating such a hotspot across a nanopore creates the conditions under which a translocating molecule disrupts the highly focused light in ways indicative of its structure. Similar to the tunnelling current approach, the (label-free) plasmonic method has been demonstrated for macromolecule detection (i.e. the presence of a DNA macromolecule is registered, but not down to individual base level) [52]. As with the ideal transverse current approaches, this method decouples the forces driving molecules through the nanopore from the signals indicative of their structure. It also promises higher bandwidth operation (bandwidths around 5-kHz have been demonstrated [53]), but its advantage over nanopore-FET methods (which are more amenable to integration and possess estimated bandwidths around 100-MHz [46]) is not yet certain.

2.3 Nanopore Sensor Structures

In this section I describe performance-leading methods and emerging techniques in nanopore sensors as it pertains to ionic current measurement approaches.

2.3.1 Biological Nanopores

Biological nanopores (biopores) were the first nano-apertures to demonstrate the ability to detect molecular structure. Despite intensive efforts to develop solid-state embodiments, biopores have been the subject of the most concerted industrial attention and, perhaps consequently, have achieved the most compelling successes with regards to DNA sequencing (e.g. the assembly of a contiguous human genome [54]).

Among biopores, protein-based designs are the dominant motif. Using genetically engineered templates biotechnologists tune natural aperture-bearing protein struc-

tures into devices well suited for molecular sensing. Common alterations include changes to the amino acid content of a protein wild-type to affect dimensions, charge, hydrophobicity, obstructions, etc. It is worth noting that alternative biopore construction methods exist including those employing peptide assembly, DNA pores, and synthetic organic channels [55].

Besides now common biopore structures like alpha-hemolysin (α HL) and *Mycobacterium smegmatis* porin A (MspA) [56, 57], leading DNA strand-sequencing technologies have recently adopted variations on the *E. coli* amyloid secretion channel CsgG (Figure 2.1a) [58]. Noted advantages of this structure include a small minimum constriction diameter (0.9 nm adjustable to 1.5 nm) along with a wide channel opening (about 5 nm compared to 3 nm for α HL) capable of better accommodating additional enzymes; a short distance between channel opening and constriction (4 nm compared to MspA's 9.8 nm); and relatively small pore thickness (10.5 nm compared to ClyA's 14.5 nm) [59]. Although longer range influences persist, the relatively small thickness of the CsgG's constriction (about 2 nm) ensures that only about 5 nucleic acid bases make the largest contribution to ionic current modulation. Under standard electrolyte conditions the pore exhibits a R_p around 1 G Ω .

Emerging developments in nanopore-based DNA strand-sequencers include the introduction of pores with multiple recognition sites [60], that is, sensors with more than one appreciable constriction within its lumen. Such sensors achieve a form of time-diversity and thus may be expected to exhibit higher SNR as has traditionally been exploited in communication systems. Accommodating structures for such applications include the protein excreting channels (secretins) common to Gram-negative bacteria such as GspD (a modified example of which is shown Figure 2.1b). In this case, the naturally occurring structure possesses a periplasmic (central) gate (on the *cis* side of an ostensible nanopore sensing apparatus) and an extracellular (cap) gate (on the *trans* side). Although these designs possess relatively large constrictions for efficient protein translocation, mutated structures may be realized for DNA strand se-

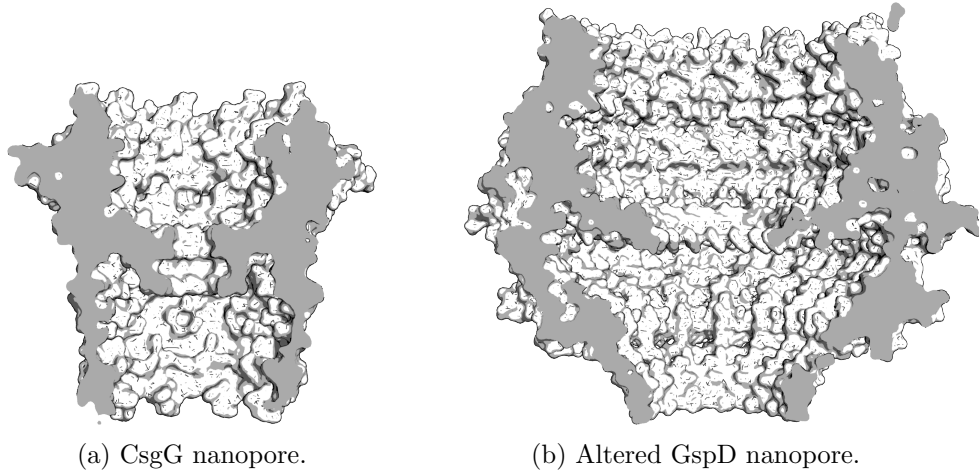


Figure 2.1: Examples of biological nanopore designs.

quencing applications [61]. Along similar lines, composite nanopore sensors comprised of two back-to-back CsgG pores have also been discussed [62].

2.3.2 Solid-State Nanopores

Solid-state nanopores (SSNs) have the potential to demonstrate many advantages over biopore structures, these include not only the ability to operate across a broader range of environments (i.e. chemical and electrical), but also their promise to support a greater number of sensory modalities. Another related benefit often raised in SSNs' favour is the higher baseline current they can accommodate (e.g. I_{base} exceeding 10 nA) compared to their biopore counterparts (which possess $I_{base} \sim 0.1$ nA). This comes as a result of the lower thickness, t , and higher bias, V_{dc} , applicable to SSNs. However, unlike SSNs, biopores have been fit with extra molecular machinery (enzyme ratchets) to regulate their DNA translocation rates. As a result, biopores can offer output signal bandwidths (BW), f_t , below 1 kHz whereas SSNs may easily exceed 1 MHz [63]. Thus, from a spectral density, I_{base}^2/f_t , perspective, SSN and biopore signal integrity remain on a roughly equal footing. Readily accessible means of regulating SSN translocation rates, for example reducing salt concentrations, simultaneously compromise the available signal levels. In response, a number of authors

have sought active means of molecule control through SSNs [64–66] with the ability of slowing translocation rates by two orders-of-magnitude without sacrificing SNR.

Judged by minimum achieved dimensions, among the most successful approaches to SSN formation have employed successive silicon nitride thinning steps (the nitride being supported on a patterned SiO_2/Si substrate) [67]. Starting with a SiN_x layer about 50-nm thick, the nitride is progressively thinned (the process takes approximately 30 minutes) across a small area (roughly $50 \times 50 \text{ nm}^2$) to $\lesssim 2 \text{ nm}$ using repeated exposures to a scanning transmission electron microscope (STEM) probe. A final exposure in one spot achieves cylindrical apertures $\sim 2 \text{ nm}$ in diameter.

Although a highly controlled process, the STEM-mediated nanopore formation approach is challenging to scale to nanopore arrays (e.g. arrays of over 2,000 biopores within thumbnail footprints are now commercially available, achieving the same with one STEM probe would require over a month of fabrication time). Recent successes in replacing focused electron-beam-based fabrication with laser-based thinning are emerging as possibly more practical alternatives [68, 69]. A potentially even more scalable approach to nanopore formation may be available via the dielectric breakdown approach [70] by which randomly distributed nanopores as small as 2-nm have been formed in SiN_x 10–30-nm thick via the application of a large electric field ($\lesssim 1 \text{ V/nm}$). Controlled means of implementing this technique using the tip of an atomic force microscope (AFM) have enabled the controlled formation of 300 pores in only 30 min [71].

Besides achieving nanopore formation via the thinning of bulk substrates, there has been an energetic effort to incorporate 2D materials such as graphene and transition metal dichalcogenides (e.g. WS_2) in the nanopore construction process [72–75]. Given thicknesses as small as 0.3 nm, such constructs are pursued for their potential to directly resolve individual bases [76]. As with the methods above, the current practice of using focused ion/electron beam techniques to perforate these materials presently limits their use in large sensor arrays.

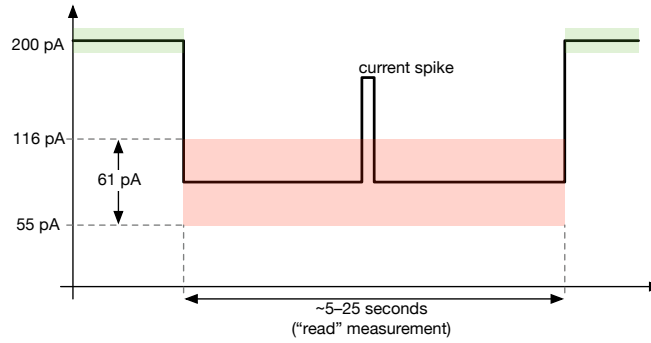


Figure 2.2: A rough illustration of what the nanopore current from a single DNA measurement looks like. The region between 55 and 116 pA is indicative of the signal when DNA is translocating through the pore.

2.4 Signals

In imagining the requirements for the design of a ROIC one could do worse than starting with a consideration of the signals it is meant to process. A high-level and somewhat abstract view of the signals present in nanopore-based DNA-sequencing systems is given in Fig. 2.2. This picture is a very idealized sketch of the “zoomed out” current characteristics associated with an industrially relevant nanopore sensor when a DNA strand goes through it.

The reader may notice that on the left of the picture a “baseline” DC current level is shown which hovers around 200 pA. This is a typical current level through a typical nanopore as used in portable DNA sequencing devices when there is no DNA translocating through it. Such currents are obtained when a bias of about $V_{ct} = -180$ mV from *cis* to *trans* is applied across the nanopore. The green band around the baseline is just a visual reminder that in reality the baseline exhibits random fluctuations, most of which fall within that band.

When a DNA strand actually goes through the pore, I get a sudden drop in the ionic current to an average of about 85 pA as the sensor is partially blocked by the molecule. Thereafter, there are fluctuations around this low current, fluctuations that are denoted by the red band. As with the baseline uncertainty, these fluctuations also include noise, but more importantly, these variations are indicative of the structure

of the DNA molecule translocating through the pore. As indicated in Fig. 2.2, these fluctuations range between about 55 and 116 pA.

The current spike in the middle of the region is just a reminder that some DNA may actually be read twice. That is, as a doubled-stranded DNA – dsDNA – unspools through a pore and translocates as a single-stranded DNA – ssDNA – first one strand, the *template*, would be registered and then, after a current interruption, the second strand, the *complement* would be registered. This behaviour does not happen with all reads, and in some cases current spikes (not shown in Fig. 2.2) may intermittently appear throughout the low-current region simply as some random phenomena or possibly fluctuations imposed on or by the molecular machinery making up the nanopore sensor.

Since DNA strand lengths can vary, the amount of time that the pore’s baseline current is blocked by DNA can vary as well. For example, experimentally prepared strands can be shorter than 100 nucleobases in length. On the other extreme, researchers have shown the ability to prepare and sequence contiguous strands that are 4 million bases long. Typical values range from about 2,000 to 10,000 bases per strand. Thus if the bases move through the pore at an average rate of 450 bases per second than the amount of time that a strand blocks the pore can be about 5 to 25 seconds as indicated in Fig. 2.2. In a typical experiment a pore may read a strand, and thus become blocked as shown in Fig. 2.2 perhaps about every 3 minutes. This estimate is obtained by considering the average amount of DNA bases gathered by a nanopore-based measurement over hours and the total number of DNA bases put into such a device over that time.

As a design guide, the nanopore DNA-handling signal characteristics outlined so far emphasize the need to accommodate an input spanning ~ 200 pA. The precision with which this signal handling must be done is determined by the fluctuations ostensibly present in the “read” measurements segment of Fig. 2.2 (i.e., the red band described above). The translocation-induced fluctuations therein can be modeled as a telegra-

pher's signal with an average pulse arrival rate equal to the *translocation frequency* f_t . In commercially available nanopore-based sequencers $f_t \approx 450$ bases-per-second (bp/s).

With regards to f_t , in practice this term is dependent on many variables, most importantly the voltage, V_{ct} , applied across the nanopore sensor as well as the details of the nanopore's bioengineering (e.g., the speed of the motor protein employed), and the salt concentration of the liquid in which the nanopore is immersed. Recent reports intimate that the arrival of sequencing devices on the market that run at f_t 's in the range of 1000 bp/s are imminent [20].

A spectral analysis of telegrapher signals shows that 90% of the signal power lies in the frequency band from 0 to f_t Hz, and 95% within $2f_t$. In a system based on a Nyquist-rate sampling data acquisition scheme, a sampling frequency of at least $4f_t$ would be needed to capture this energy. In practice, existing systems operate at sampling frequencies about 8 to 10 times that of f_t . This choice is likely influenced by non-ideal filter roll-off and thus the preference to avoid excessive distortion by sampling at higher rates.

Formally, the double-sided current spectral density of a telegrapher's signal can be expressed with

$$S_{ii}(f) = \frac{i_\delta^2}{1 + \left(\frac{2\pi f}{f_t}\right)^2} \quad (2.4)$$

where i_δ^2 is the double-sided mean-square current spectral density of the signal. A rough analysis of nanopore sensor and nanopore sensing apparatus characteristics [77, 78] leads to an estimate of the current spectral density being

$$\sqrt{i_\delta^2} \approx 1 \text{ pA}/\sqrt{\text{Hz}}.$$

Over a frequency range of $2f_t=900$ Hz (our 95% power bandwidth), the above approximation indicates a current signal power of approximately $2.5 \times 10^{-22} \text{ A}_{\text{rms}}^2$. As

a result, to achieve a 20-dB SNR, a ROIC must operate with an equivalent input-referred white noise current spectral density of

$$\sqrt{i_n^2} \approx 50 \text{ fA}/\sqrt{\text{Hz}}.$$

This means that over a 900-Hz band the integrated ROIC noise current value cannot exceed $I_n = 1.5 \text{ pA}_{\text{rms}}$. To operate at 10-dB SNR the $\sqrt{i_n^2}$ and I_n specifications loosen to about $150 \text{ fA}/\sqrt{\text{Hz}}$ and $4.5 \text{ pA}_{\text{rms}}$, respectively.

Of course, the examples of 10 and 20-dB SNR operation are only representative settings, not uncommon in signal processing systems. Their exact needs depend on the quality and sophistication of the following digital signal detection systems that operate on the data provided by a ROIC. Such a system is discussed in Chapter 7 of this thesis.

2.5 CMOS

2.5.1 Amplifiers

The apparatus by which nanopore-sensor electrochemical output signals are readied (i.e. amplified, filtered, digitized) for ensuing digital signal processing (DSP) is the *readout* block. Readout components have been a staple of biophysics and electrophysiology labs for decades where, for example, they support investigations into cellular ion-channel properties. Recent industrial developments have been successful in porting the extensive collections of off-the-shelf equipment traditionally used for readout into a microelectronic instantiation, a readout integrated circuit (ROIC). The creation of such technology has had a profound impact on the applicability of nanopores to molecular sequencing for sophisticated life-science practitioners, not to mention the extreme reduction in size afforded by an IC implementation. A key contribution of these ROIC developments involves their ability to fully leverage the power of

semiconductor implementations by arraying the readout elements across a chip, thus realizing a high-throughput device. I present this multi-channel aspect in § 2.5.4. Presently however I focus on developments associated with the key CMOS circuit building blocks needed within each channel, paying particular attention to the analog front-end (AFE).

Recent advances in CMOS front-ends directly applied to, or directly relevant to, nanopore sensors have addressed current-sensing circuitry appropriate for RPS. All of these systems are an outgrowth of the classic patch-clamp architecture, a circuit by which a stable potential is applied across an ion-channel-infused membrane. In simultaneity with this voltage control, the patch-clamp draws the channel's ion current into one of its biasing nodes and converts it to a voltage (I - V). This is sometimes also classified as a single-electrode voltage-clamp. Ultimately, these designs are fundamentally centred on transimpedance amplifier (TIA) circuit blocks. Standard TIA arrangements to find use in nanopore systems are shown in Figure 2.3.

The resistive-feedback TIA of Figure 2.3a is the most straightforward approach, an input current I_{in} is funnelled through the resistor R_F and thus produces a proportional voltage, V_{out} (the feedback capacitance, C_F may be present as a combination of parasitic and intentionally-designed contributions), but this is impractical for modern nanopore applications. For example, with signal waveforms centred around roughly 100 pA a TIA-feedback resistor, R_F , on the order of 1 G Ω would be needed to provide an output voltage of adequate amplitude. With typical CMOS technologies possessing materials affording about 1 k $\Omega/\mu\text{m}^2$, resistive components of this size would require untenable IC footprints. Also, with parasitic capacitance at roughly 20 fF/M Ω , the bandwidth of such systems would not even reach 100 Hz. Thus a tradeoff immediately presents itself: increase R_F to establish a certain I - V conversion gain, but simultaneously sacrifice the bandwidth over which such gain may be realized.

Nanopore-based signal conditioning imposes a significant circuit design challenge right from the on-set. These have traditionally been handled from the continuous-

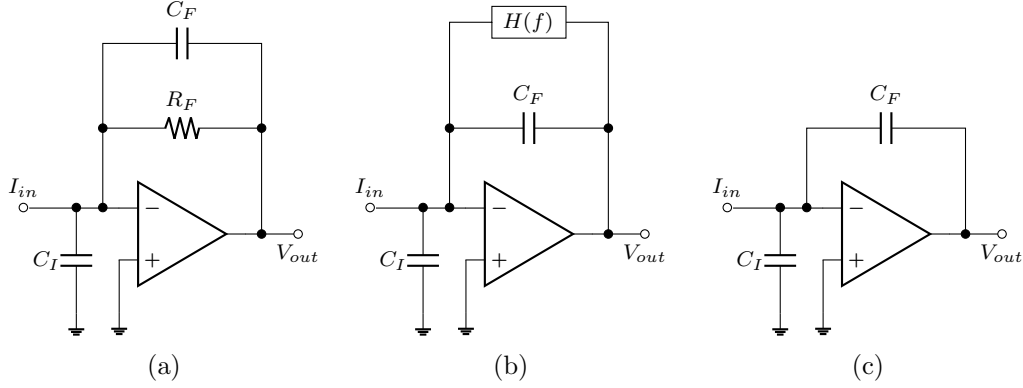


Figure 2.3: Transimpedance amplifier (TIA) main topology arrangements for current-based sensor readout. a) Resistive feedback TIA b) CT capacitive feedback TIA c) DT capacitive feedback TIA

time (CT) perspective, but as the search for CMOS-based solutions has intensified, a growing number of contributions have considered a discrete-time (DT) approach. Both are reviewed in the following.

2.5.2 Continuous-Time CMOS Readout

A critical influence on the choices driving TIA design for nanopore applications is the input capacitance C_I (see Figure 2.3). This component is due to not only the electronic elements of which the TIA is comprised but also depends on the sensory apparatus itself (e.g. the nanopore membrane/support structure, wiring connections, etc.). Even for state-of-the-art microfluidic nanopore-based sequencers C_I can presently approach 5 pF.

An excellent feedforward TIA amplifier can marginalize this contribution, its high gain-bandwidth product (GBP) preventing any significant signal shunting through C_I and thus resulting in a high bandwidth to seemingly affect high-speed nanopore-based DNA sequencing. Of course in this idealistic case, the bandwidth would be set by the $R_F C_F$ time constant, and thus emphasize for the designer the need for means of minimizing C_F . However a realistic TIA's performance is influenced by the mingling of C_I , C_F , and the amplifier's finite GBP; the introduction of a feedforward pole

(at $R_F(C_I + C_F)$) and a feedback zero (at $R_F C_F$) combine to undermine stability at higher bandwidth unless impractically low values are used for C_F [79].

As a result, the speed/stability clash encountered by nanopore-suitable (i.e. patch-clamp applications historically speaking) TIA implementations has traditionally been addressed by targeting a “well-defined frequency response” for the TIA [80]. This approach purposely augments C_F to values that significantly separate the TIA’s two main closed-loop poles despite a potentially high C_I or less aggressive GBP. The most aggressive version of this method replaces the R_F entirely with C_F resulting in a pure integrator whose attenuation at increasing frequencies is corrected by an ensuing differentiator block. Among the advantages of this approach is that it makes the pole/zero compensation of the integrator/differentiator chain easier. However this method clearly presents a problem for CT approaches vis-a-vis the need to periodically discharge the C_F . It is, however, a natural avenue to follow in the DT case as discussed in § 2.5.3.

A re-set free, high-bandwidth (4-MHz), capacitive integrator-differentiator scheme is achieved in 0.35 μm CMOS by implementing a special DC feedback loop [24, 81]. Using a frequency dependent active feedback ($H(s)$ in Figure 2.3b) the DC current is removed from the input to avoid saturating C_F . This active feedback provides low attenuation at low frequencies (below 100 Hz) and high attenuation at high frequencies (so it does not compromise the integrator output). A high resistance is required to implement a low-noise DC feedback. A current-reduction circuit working in tandem with the frequency-dependent feedback essentially scales up a 300 k Ω on-chip reference resistance by six orders of magnitude.

An alternative continuous-time ultra-low-noise pre-amplifier uses a matched double-MOS scheme to multiply the input current [25]. Specifically, in place of R_F the TIA uses a NMOS/PMOS pair (a *double*); at its output, the $N\times$ scaled circuit replica (with matching bias) of the double is present resulting in a translinear current multiplication by a factor of N (ratios of 99 and 10 are tested). This amplifier can reach a noise

floor of $500 \text{ aA}/\sqrt{\text{Hz}}$ under low input current. But as the input current increases the noise increases linearly due to the shot noise of subthreshold feedback transistors. Moreover, this circuit does not implement any flicker noise capture techniques. As a result, one needs to account for the flicker noise from the nanopore itself.

Another integrator-differentiator design built specifically to accommodate the high-frequency requirements of SSNs is discussed in [23, 82]. The integrator follows the general approach described in [24], but employs a much lower feedback resistance, $R_F = 100 \text{ M}\Omega$, and thus achieves its pole/zero cancellation at a much higher frequency (about 25 kHz vs. 100 Hz as noted above). From a signal-amplitude perspective the drop in R_F is acceptable since SSNs accommodate larger currents. Similarly, the possible distortion invoked by the hike in the circuit's lower corner frequency due to the drop in R_F (i.e. below $R_F C_F^{-1}$ the differentiator effectively distorts the signal) is manageable for the higher signal speeds inherent to SSNs (relative to ratcheted biopores). This design also uses a linear current source as an active feedback resistor for low noise. A significant improvement in area was also achieved relative to [24] as a complex DC feedback loop is avoided.

2.5.3 Discrete-Time CMOS Readout

As intimated above, DT ROICs may also follow the integrator-differentiator scheme albeit by embracing a purely capacitive feedback in the integrator stage along the lines shown in Figure 2.3c. An early CMOS example of such an approach for nanopore applications is discussed in [83]. This work presents a DT low-noise amplifier consisting of an integrator, a post amplifier and a low-pass filter. Correlated double sampling (CDS) is performed off-chip. Besides attenuating the offset and flicker noise, the CDS effectively realizes the differentiation function as well, but doubles the thermal noise. To address this latter point, [83] relies on a low thermal noise amplifier in the integrator. A in-depth explanation of working of DT amplifier is shown in § 3.4.

Contemporaneously, [84] described an ultra-low-current measurement technique employing *capacitive matching*. Typically, an AFE for nanopore-based measurement consists of a low noise amplifier, a filter and an analog-to-digital converter (ADC). These blocks introduce signal distortions due to issues such as charge injection in the amplifier and analog imperfections in the ADC. To overcome these problems [84] employs a nested auto-zero scheme and a novel CDS. A threshold comparator, with two threshold levels, is used to measure the slope of the integrator output. After the auto-zero phase, the threshold of the comparator is set to the first threshold level. Once the output the comparator goes high, its threshold is switched to the second threshold level. The time-difference between the two high outputs of the comparator, which is counted using a counter, infers the slope of the integrator. This mechanism acts like a conventional CDS reducing offset and flicker noise. Thus, the input current is measured as a function of pulse width. This eliminates the need for an ADC and marginalizes non-linearities caused by analog mismatch.

A mostly continuous-time circuit that includes re-setting out of concerns that the input amplifier may saturate due to accumulated charge on the input capacitance itself is presented in [85]. A typical instrumentation approach is followed by using a resistive feedback TIA. This causes higher noise and occupies more area.

In the DT amplifiers, the transimpedance gain(R_{EQ}) of the integrator is propositional to the integration period (T_{INT}), $R_{EQ} = T_{INT}/C_F$. All conventional DT circuits have an equal reset rate (f_r) and sampling rate (f_s). To achieve higher bandwidth in conventional DT amplifiers, the integration time needs to be reduced. This in turn reduces the gain of the system and increases the input-referred noise, a major constraint of conventional DT amplifiers. In [26] the authors propose a system where the integrator is re-set at a rate that differs from the ADCs sampling frequency. By sampling at the higher rate, a signal with higher bandwidth can be captured while the reset rate is kept constant. Thus, the gain and the input-referred noise remain the same. The authors proposed a track-and-hold (T&H) after the integrator-differentiator to

avoid sampling the corrupted signal during the reset phase. Alternatively, this can also be done digitally. A low pass filter is also employed to filter out high frequency spurs caused by the T&H.

A completely novel approach using an hourglass ADC, which has similarities to a sigma-delta converter, has been presented in [86]. An hourglass ADC employs a capacitive TIA in feedback. To avoid saturation, a switch flips the polarity of the input signal within a user defined time window. This folds the output of the integrator, converting it from a ramp into a triangular wave and prevents it from saturating. This also converts the output of the integrator from a voltage to a frequency which provides high dynamic range to the hourglass ADC. To improve linearity the input is also connected to a steering DAC which measures the coarse input current and reduces the input to the hourglass ADC.

A summary performance comparison of a number of CT and DT designs discussed above is presented in Table 2.1. Due to the myriad design approaches and even measurement (e.g. the input source capacitance/resistance and the DC level of the input signal) specific conclusions on performance need to be carefully tempered. Generally speaking, DT amplifiers have lower noise while CT amplifiers can amplify signals to a much higher bandwidth and have a higher dynamic range. Also included in Table 2.1 is a comparison of the CMOS proposals to common bench-top instrumentation systems (Axopatch 200B). Clearly, from a noise and bandwidth perspective the CMOS approaches offer highly competitive performance levels (not to mention their intrinsic benefits in cost and size).

2.5.4 Arrays

Although the design and realization of high-performance readout components for biosensors remains a critical objective, their arrangement into high-throughput parallel-channel arrays is arguably even more important in today's rapidly evolving bio-

Table 2.1: Nanopore-Relevant DT and CT AFE Performance Comparison

Ref.	Style	Input Range [nA]	Noise Floor [fA/ $\sqrt{\text{Hz}}$] @kHz	BW [kHz]	Integ. Noise [pArms]	Inp. Cap. [pF]	Input Res. [G Ω]	Power [mW]
[24, 81]	CT	25	4 @100	0.1–1000	–	6	0	–
[23, 82]	CT	10	10 @10	0.1–100 0.1–1000	3.2 24	6	0	5
[25]	CT	40	0.5 @10	0–100	1	5	0	5
[87]	CT	10	8.5 @10	100–10 0.1–100	3.4 13.5	10	1	65
[88]	CT	10	11 @10	0.1–10 0.1–100 0.1–1000	0.4 3.4 52	6	10	30
[89]	CT	11 600	11.6 @1	0–10	1.25	0	0	1.5
[90]	CT	10	8.5 @10	0–10	1.2	5	1	0.6
[83]	DT	0.2	5 @1	0–10	2.44	47	10	1.5
[84]	DT	0.2	0.235@1	–	–	0	–	0.15
[85]	DT	0.05	–	0–10	8.3	50	1	3.8
[26]	DT	0.2	4	0–10	–	3	1	–
[86]	DT	10 000	30 @1	0–1	–	0	0	0.29
200B	Cap.	–	0.7	0–100	–	0	0	–
200B	Res.	–	6	0–100	–	0	0	–

technological landscape. The role of ISFET-based DNA sensing paints a particularly vivid example of this. The introduction of ISFETs in the early '70s as a transistor-based means of chemical analysis [42] effectively launched research into bio-sensing interfaces to active substrates. The realization of these sensors within an untempered commercial CMOS process [91] 25 years later prompted realizations of the first four-element ISFET CMOS sensor arrays after another five years [92, 93]. Within four years of these demonstrations, by 2007, others reported 2D arrays consisting of 260k ISFET pixels [94], by 2011 fully operational DNA sequencers based on 1.5M-pixel chips were announced [14]; a per-pixel area of roughly $20 \mu\text{m}^2$ in a 350-nm CMOS technology.

Judged by element count alone, the scale of integration achieved by ISFET-based CMOS biochips remains unparalleled in the field. This is, at least in part, realized by the extreme degree to which the complexity of ISFET sensing pixels may be reduced, primarily at the cost of dynamic range, to accommodate certain means of sequencing (i.e. broadly speaking, the *sequencing-by-synthesis* SBS method [95]) [96]. For DNA

sequencing, each ISFET pixel may be reduced to two or three transistors producing raw signals on the order of 10 mV and 0.1 Hz (with a final SNR exceeding 20 dB at the detector [14]). Being largely (although not exclusively) intended as single-molecule detectors, nanopore-based readout methods lack the advantages available to SBS systems which benefit from stronger signals due to redundant molecular samples and finely controlled chemical reactions (allowing for lower bandwidth operation).

As a result of their signal characteristics, nanopore-based measurement systems require more intricate readout components (as discussed in § 2.5.1 above) and hence need more sophisticated front-ends within each pixel. Detailed reports on means of effectively arraying such pixels for high performance nanopore-based molecular measurement, specifically DNA sequencing, are practically non-existent in the academic literature; more common, in this sub-specialty, are descriptions of individual component design (again, as discussed in § 2.5.1 above) and the performance stress imposed upon them by nanopore signals.

The only complete functional array for nanopore based sequencing has been proposed in [2]. Nanopore readout system needs ultra-sensitive amplifiers but this makes integration of readout circuitry challenging. The noise from ADCs couples into the sensitive amplifiers through substrate, power supply or voltage references. In this patent, authors have used a DT amplifier with digital CDS to reduce flicker and kT/C noise. The noise caused by the digital readout circuit is uncorrelated, so it cannot be removed by CDS. A DT amplifier consists of reset phase, noise sampling phase and readout phase shown in Fig. 2.4. Noise sampling phase occurs after the amplifier is reset while the sampling phase occurs at the end amplification period. To minimize the noise due to readout circuit, readout needs to be performed outside the these two phases otherwise it corrupts the measured signal. The noise of readout circuit on amplifier output has been illustrated in Fig. 2.4. This noise acts as AC signal and doesn't affect the signal once readout is finished.

To mitigate this issue various scheme have been proposed in [3]. One can perform

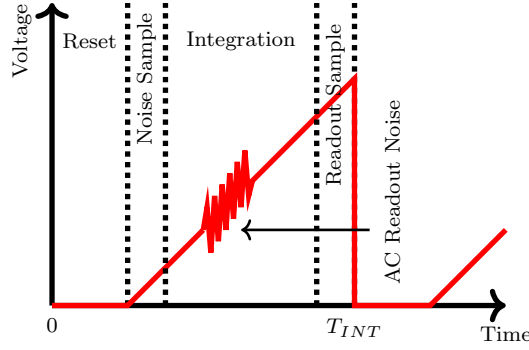


Figure 2.4: Illustration of the readout noise on amplifier output [2]

reading outside the integration period to avoid disturbances but this causes a dead-time for the amplifier. There have been seven schemes proposed in [3] for performing readout. Scheme 1-2 uses a successive approximation register (SAR) ADC while scheme 3-7 could potentially use pipeline ADCs. Scheme 2,4-7 allow for delay in transmission of data. Scheme 1 does the conversion between CDS 1 and CDS 2 and transmits it right away. Scheme 2 perform the conversion between CDS 1 and 2 but transmits it during reset period. This can be useful in reducing noise if data transmission circuits consume high power. Scheme 3 perform both conversion and transmission in the reset period. This would either require a large reset period or high speed ADC. Scheme 4 is opposite of scheme 2 where conversion is performed in reset period while the transmission is done between CDS 1 and 2. Scheme 5-7 perform partial conversion or data transmission in reset period and the rest in between CDS 1 and 2. There needs to be enough time of no activity before the CDS sample for the noise to settle.

In [97] is presented a nanopore sensor array with in-pixel event generation ADCs. The pixels have an integrator and when the integrator output voltage reaches a specific level, an event is generated and the nanopore is reset. Due to the random nature of the events generated throughout the array, the digital activity on the data lines can induce noise on the integrator. To solve this problem appropriate metal shielding techniques were claimed in the work.

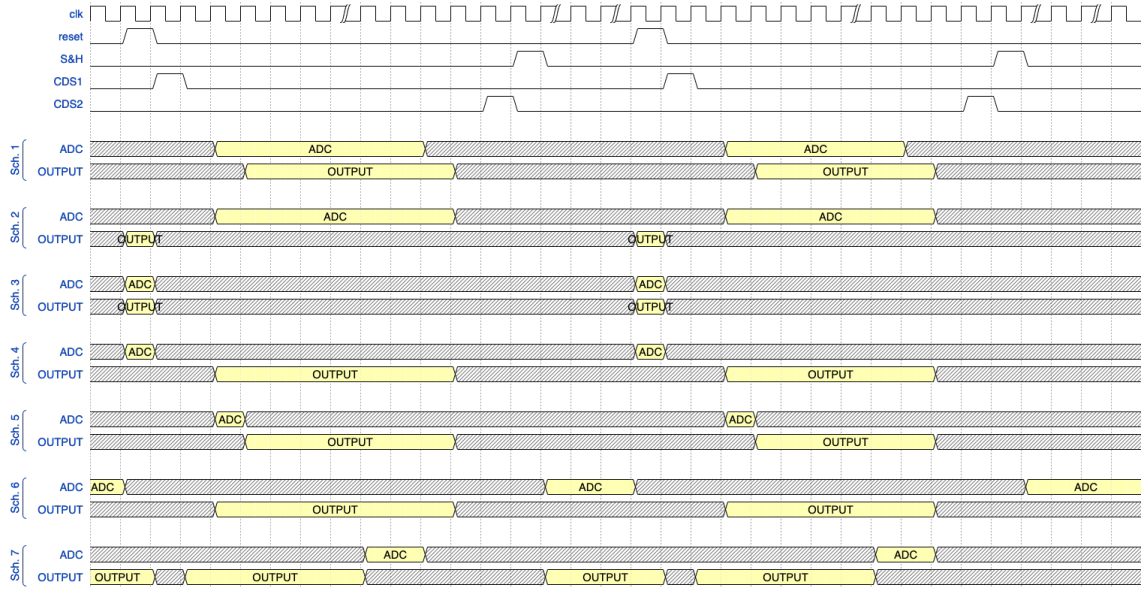


Figure 2.5: Distortion free readout techniques for a nanopore readout array (recreated from [3])

Also in [98] a nanopore array with column based ADCs is presented. Each column ADC is designated to service multiple columns through multiplexing. Each pixel of the sensor is equipped with compact current conveyor integrators. Although the pixel size is relatively small in this claim, higher noise is expected in this method compared to the integration based methods as due to the thermal noise of the current mirror itself [99].

In [100] a four-channel nanopore detector front-end is presented. One half of the differential amplifier, which receives the constant input, is shared among the different cells to reduce the consumed area and power. No ADCs were implemented in this system.

A summary of arrays published in literature have been shown in Table 2.2. Performance metrics of systems published in patents are not available. Hence, they haven't been included in Table 2.2.

Table 2.2: A summary of CMOS array approaches and performance levels for nanopore based sequencing.

Ref.,Yr.	Tech. [nm]	Pixel Count	Chip Area [mm ²]	Pixel Area [μm ²]	BW [Hz]	MDS [pA]	Power [mW]	AFE Type
[23, 82], '12	–	4	–	500 ²	~1M	~155	-	In-pixel CT TIA
[30], '16	–	25	5×5	400 ²	~1M	~129.4	-	In-pixel CT TIA
MinION, '14	–	512	10×13	500 ²	~1k	~0.1	~1000	In-pixel curr. integrator

2.6 Microfluidics

Lipid bilayers are used to suspend biological nanopores in ionic solution. They are nanometer thick but act as a barrier to ions. A tight seal with lipid bilayer has resistance in the range of 10s of GΩ. For DNA sequencing, mostly Black Lipid Membrane (BLM) or Droplet Interface Bilayers (DIBs) are used.

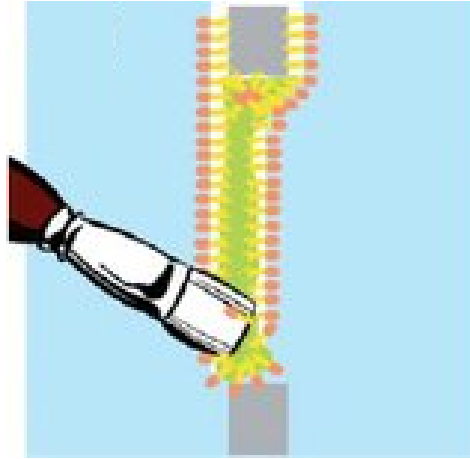


Figure 2.6: Painting bi-layer on a teflon microaperture [4]

The most simple method to form BLM is using the painting method proposed in 1962 [101]. In the painting method, a BLM can be formed by painting lipids dissolved in organic solvent on a micro-aperture. This technique is quite simple but is not a scalable approach for high-throughput sequencing. A semiautomatic BLM formation has been shown in [102] with over 90% success. A ninety-six channel system with microfluidics to form BLM was also shown in [103]. BLMs are formed by alternatively flowing lipid and buffer solution in an integrated microfluidic channel. The system forms a lipid layer in 44 out of 96 wells. Moreover, there is no talk on the mechanical stability

limiting the use to a lab environment.

Another interesting method to form of bilayer is called Droplet Interface Bilayer (DIB). First an aqueous droplet is placed in organic solvent containing lipids. The lipids self assemble to form a monolayer at the interface of solvent and water. The contact interface of two of such droplets forms a DIB [5, 104]. DIB systems allows for measurement with minute amount of analyte.

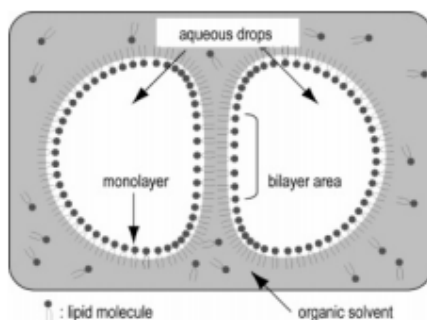


Figure 2.7: Illustration of monolayer droplets forming a DIB [5]

It has been shown that using hydrogel the stability of bilayer can be improved. A BLM with α -hemolysin sandwiched between two layers of agarose gel could be stored for weeks [105]. Membrane can be stored and transported by freezing the nanopore chip to 4°C and bringing the frozen membrane precursor to room temperature to reform the BLM [106].

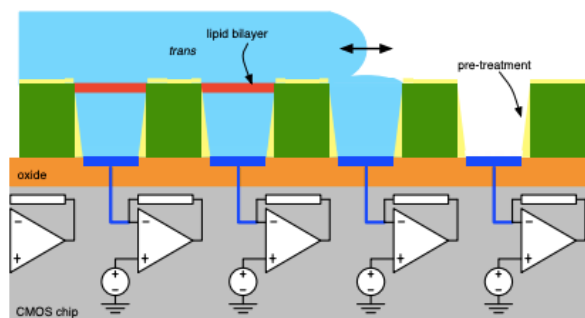


Figure 2.8: Pore formation method using amphiphilic molecules used by oxford nanopore [6]

An early attempt from Oxford Nanopore Technologies involved microwell fabricated on chip using SU-8 shown in Fig.2.8 [107]. These well are pre-treated with hexane

to improve the adhesion of lipids. Then an aqueous solution containing amphiphilic molecules (lipids) is flown to fill the wells and form a lipid bilayer over them. This method has stability issues due to electrical and biological sample stress. To fix this issue, oxford nanopore changed the structure of microwells and used synthetic lipid made using triblock copolymers shown in Fig. 2.9 [108]. These special well structure allows for the formation of droplets which also improves the stability of the bilayer.

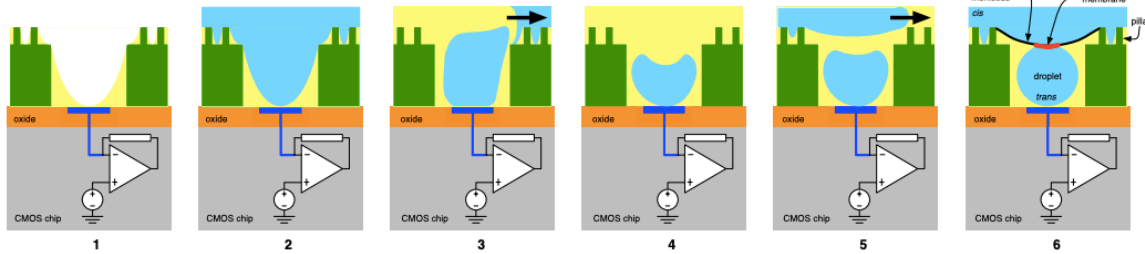


Figure 2.9: Pore formation method using synthetic lipids used by oxford nanopore [6]

To reduce the effect of parasitic input capacitance, the electrode and microwell should be fabricated on the chip using post-fabrication processing. Usually this is done before the chip is wire bonded. An epoxy is applied over the wirebonds using techniques such as dam & fill. An example of such a setup is shown in Fig. 2.10.

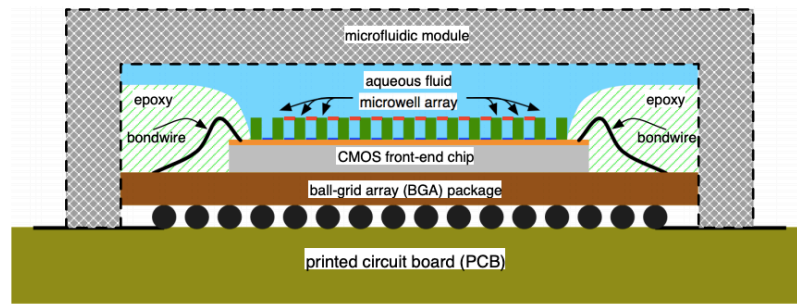


Figure 2.10: Example setup of microfluidic nanopore system [6]

Chapter 3

Digital Readout Integrated Circuit (DROIC)

3.1 Chapter Summary

In this Chapter, I focus on the design and implementation of a Digital Readout Integrated Circuit (DROIC) tailored for nanopore-based DNA sequencing systems. I begin by outlining the critical role of ROICs in bridging the interface between sensors and data processing units, emphasizing the need to amplify, filter, and digitize sensor signals effectively.

Next, I delve into the system design of the DROIC, explaining the decision-making process behind the choice of an arrayed ROIC system with on-chip data conversion. This design approach is crucial for handling the large number of parallel channels needed for modern DNA sequencing technologies, which can involve thousands of sensors.

I then provide a comprehensive overview of the Analog Front-End (AFE) design within each DROIC pixel. The AFE is composed of three main components: the Transimpedance Amplifier (TIA), the Low-Pass Filter (LPF), and the Correlated Double Sampler (CDS). Each of these components is carefully designed to optimize

signal amplification, noise reduction, and signal fidelity. Finally, I cover the design and implementation of a 10-bit SAR ADC (Successive Approximation Register Analog-to-Digital Converter) within each DROIC pixel.

In summary, this chapter provides a detailed account of my design considerations, component selection, and system architecture of a DROIC tailored for nanopore-based DNA sequencing, aiming to achieve high performance and scalability in a compact, low-power format. The throughput density of AFE is 11.1 kbp/s/mm² at 20 dB SNR. Hence, improving throughput density by approx. 6.5x, while consuming 5.8x lower power, compared to ONT’s system.

3.2 Introduction

Readout integrated circuits (ROICs) serve as the interface between sensors and the computers that extract meaning from their measurements. Thus, the main function of ROIC chips is to amplify, filter, and digitize sensor signals. In modern systems and in emerging DNA and bio-molecular measurement systems, ROIC readout is increasingly expected to support large sensor arrays and to do so in a mobile application context as well. In this chapter, I describe such a ROIC array design geared for nanopore-based DNA sequencing systems – which I refer to as a digital/discrete ROIC (DROIC) to emphasize the design choices made as part of its realization.

3.3 System Overview

The signal discussion above specifies a fundamental set of requirements for a ROIC system targeting contemporary nanopore-based DNA measurement applications. The following discussion outlines the structure within which I chose to realize these behaviours and the design logic that motivated it.

Since at least 2005, when the 454 Life Science GS20 machine was released and

ushered in “next-generation DNA sequencing” technology, sequencer designs have emphasized the parallel measurement of vast multitudes of DNA samples. Today’s state-of-the-art, enterprise-class sequencing machines can deal with over a billion DNA sensing reactions in parallel and can scan their detectors across 100 million such activities per second. Even hand-held, nanopore-based, DNA sequencing devices can house thousands of DNA sensors within a thumbnail sized sensing area, all capable of carrying out DNA measurements in parallel.

As the DNA sequencing machine outline above indicates – however it is that a ROIC deals with the signal presented by nanopore sensors – the present and future state of this technology requires that the ROIC does so across many parallel channels, each somehow interfaced to a DNA sensor for some amount of time. Thus, a complete commitment to the realization of an arrayed ROIC was my first major design decision.

This choice narrows other design possibilities. To begin with, including on-chip data conversion becomes paramount. Otherwise, the ROIC would be left having to funnel analog signals off-chip. For very small channel counts (say less than 10) this may be feasible as the space to dedicate individual, high-quality output ports to each channel may be possible. Similarly, the complexity of transporting this many signals to a separate (i.e., off-chip) data conversion and digital-signal-processing (DSP) block may be acceptable. But this approach is clearly impractical when designing for systems with the potential to scale to 100s or 1000s of channels per chip. In such cases, the ability for separate and uncoded analog signals to share a transmission media is extremely limited. Thus, a growth in measurement channels results in growth in the number of separate communication channels that must be accommodated. This is an expensive proposition at the scales that even present-day miniature DNA sequencing technology can achieve. Of course, digitizing input signals on-chip solves the output port problem as it affords a straightforward means of storing and multiplexing digital data through a limited set of standard quality output ports is practical. Thus, com-

mitting to the inclusion of on-chip data converter blocks in my system was the next major design decision in my system implementation journey.

My next concern lay with the need to select the design style for the analog circuitry upon whose output's the data conversion would act. As conveyed by the signal analysis above, the need for such analog circuitry is unavoidable. Nanopore sensors for DNA applications generate only minuscule current signals. No existing on-chip data conversion methods can directly digitize such low power inputs. Thus, some form of analog signal processing embodied in analog integrated circuitry is required to amplify these measurements and to ensure that in the process a minimum of circuit noise is added to the already challenging signal-to-noise ratio (SNR) available from the sensor.

The combination of signal size, SNR, and array plans led me to conclude that, among the analog signal processing (ASP) motifs established by the engineering community, the discrete-time (DT) ASP style (in contrast to the continuous-time style) would be best [109].

In DT-ASPs analog input signals are converted into continuous-level time samples by accumulating input signal energies in capacitive components. By virtue of its sampled nature, this is a convenient prelude to the data conversion blocks already planned for my implementation. From an analog performance perspective, the opportunity to rely on non-resistive components (i.e., capacitors) for signal processing immediately opens the door for low-noise behaviour. In particular, the conversion of small nanopore input currents into large voltage signals by integrating said inputs across a capacitor is particularly suitable for DT implementation. In such cases, the capacitor is made to periodically accumulate and flush signal charge, with suitable interludes for data conversion.

Further, as with large synchronous digital systems, the strictly timed nature of the DT-ASP process affords many opportunities to orchestrate operations. That is, the timing of analog and digital functions (i.e., when the ASP or DSP is allowed

to operate) as well as the analog functions themselves (i.e., the timing of different analog channels in an array) can be finely controlled. This facility is critical for the realization of arrayed systems with ambitions of hosting possibly 100s or 1000s of channels on a single IC. As a result of this feature, I refer to the readout designs in this work as discrete/digital ROIC (DROIC) systems.

The ability to decouple amplification from ADC operation via judicious timing is critical for realizing low-noise analog performance within large DROICs. In particular, during the analog amplification process, the system may benefit from turning off digital circuits. Thus, a cleaner signal, free of digital noise disruptions, may be sampled before digitization (i.e., data conversion). Post digitization, the amplifiers can be reset to suitable initial values and proceed onward to forming the next DT sample.

With the main considerations as discussed above in mind, a high-level design for DROIC was conceptualized as drawn in Fig. 3.1.

This picture shows an overview of the implemented array. Each channel or ‘pixel’ (the terms are used interchangeably in this thesis) consists of two main active blocks: an analog front-end (AFE) and an analog-to-digital converter (ADC). Ideally each pixel would be interfaced to a single nanopore and thus amplify the current emerging from that one sensor. The means of this interface is a challenging problem in its own right, but the most straightforward way of addressing this need at the chip level is by including a metal contact (ostensibly made from the CMOS technology’s “top metal” layer) in each pixel of the array (the “Pad” block in Fig. 3.1). Through this external metal connection, wire or via links to a separate nanopore sensing array can be made. Alternatively, the Pad can be configured to adequately pick up in-solution ionic charges itself. Such configurations are discussed later in this thesis. Below, I describe further the components and connections in Fig. 3.1.

Arguably the most outstanding feature of this arrangement is the choice of in-pixel data conversion (i.e., one ADC per pixel). This extreme implementation, in contrast

way through to physical chip fabrication.

The fabricated DROIC system contains $5 \times 6 = 30$ channels distributed across 5 horizontally-oriented rows and 6 vertically-oriented columns. To keep Fig. 3.1 compact, only 9 channels are shown. To maximize flexibility, the AFE can select from three available inputs: external current input (“In” nodes in Fig. 3.1), a local pad (“Pad”, as discussed above), or a calibration block (“Cal” node).

The In port is connected to the DROIC chip’s peripheral bond pads which may be wire bonded to a package lead frame. Thus it allows for the introduction of nanopore or nanopore-like input signals through standard means, via some connections to a printed-circuit board (PCB) to which the packaged DROIC chip is connected.

As noted above, the Pad port creates the opportunity to feed signal connections directly into each pixel. As such, this input offers the possibility of area-connections (rather than the periphery-connections to which the In ports are limited) to some sensor array apparatus. For systems intended to operate with 100s of sensors in parallel, such input styles are vital.

Finally, the Cal port connects the AFE input to a calibration block which provides a known current to calibrate the gain for channels.

Sensor and control signals flow through horizontal and vertical wire connections running across the DROIC array. As indicated in Fig. 3.1 a set of horizontal input busses (“In. Bus”) ferry sensor signals from the peripheral pads to different pixels. Since there are 6 pixels per row, each bus consists of 6 wires. Adopting this approach to ever larger array configurations is clearly challenging. As the number of inputs increases, the wire run length grows as does the potential impact of signal cross-coupling. This underscores the long-term benefits of making area-connections between sensor signals and pixels through Pad inputs.

The vertical connections (red lines) shown in Fig. 3.1 transport digital signals for DROIC programming and ADC outputs. Each channel contains its own configuration register (“Conf Reg”) implemented using a 10-bit shift register. The contents of these

per-pixel shift registers are used to uniquely establish the settings of each pixel’s AFE (e.g., which input to connect to, gain, bandwidth settings, etc.). As shown, a 1-bit serial input (“Ser. In”) is dedicated to each column of DROIC. These lines daisy chain each of DROIC’s column configuration registers to form a 50-bit shift register. The program for each column can be loaded by shifting five 10-bit words through the Ser. In port.

Similarly, the ADC’s digitized output samples in each column are daisy chained with the 1-bit “Ser. Out” connection. At the end of each conversion period, the results contained in each column are to be clocked out in series. Another 1-bit serial input (“ADC Ser. In”) also allows for the ADC registers to be pre-configured in some starting pattern.

3.4 Analog Front-End (AFE) Design

A schematic of the AFE present within each DROIC pixel is given in Fig. 3.2. In particular, it shows how the AFE consists of three main parts, the transimpedance amplifier (TIA), the low-pass filter (LPF), and the correlated double-sampler (CDS). These components are staples of ASP systems targeted for the bioinstrumentation space, especially applications in the electrophysiological space in need of small current measurement. Given the strong similarity between nanopore-based signal processing needs and such uses, the choice of AFE architecture as shown in Fig. 3.2 is understandable.

In the AFE, the discrete-time TIA (DT-TIA) serves as a current-to-voltage converter. The LPF following the DT-TIA is used to improve the noise performance of the signal processing chain by limiting the contributions of high-frequency noise to the output signal and, from a sampled-system context, fulfills the anti-aliasing function. Finally, the active correlated double sampler (CDS) block is employed to remove flicker noise, charge injection and kT/C noise.

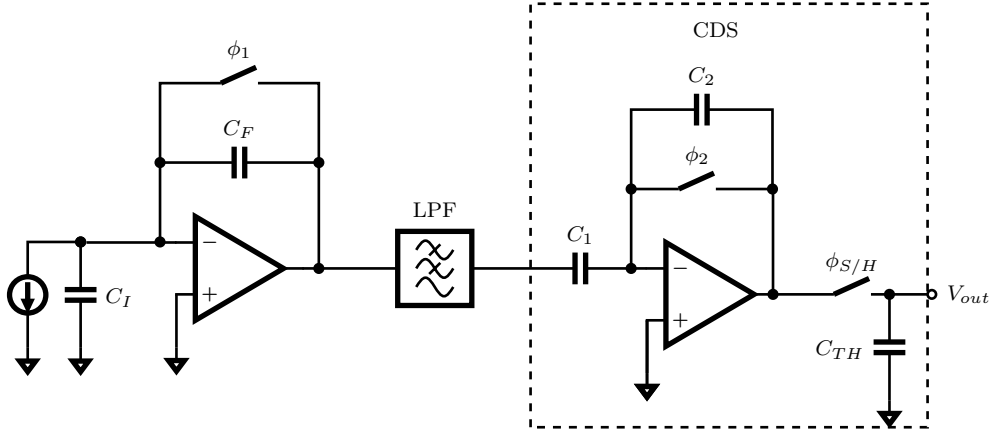


Figure 3.2: The DT analog front-end (AFE). This analog signal processing system consists of three main components: the TIA, the LPF, and the CDS.

TIA

The DT-TIA, ‘simply’ directs the small nanopore current described in § 2.4 onto the feedback capacitor C_F and periodically flushes the charge accumulated upon it. The longer that this current is directed onto C_F between reset flushes the more that C_F is ‘charged up’ and the larger the voltage drop across it. Thus, besides realizing a current-to-voltage conversion, charging of C_F simultaneously realizes an integrating function.

This current-to-voltage change may also be realized with a resistor, but this choice of design is accompanied by a higher noise contribution (due to the lossy nature of the resistive component). Also, relative to a capacitor, using a resistor increases the area and power consumption.

The opamp straddling C_F accommodates the voltage build-up across the capacitor while helping maintain a constant potential across the current’s source of origin: the nanopore sensor; thus a unilateral signal flow is established within the ASP wherein the voltage built-up across the C_F has no first-order impact on the nanopore sensor voltage bias. This, of course, is a classic patch-clamp amplification set-up.

In the DT approach, a short integration time period, T_{INT} , is allotted for voltage build-up across C_F . At the end of this period, the integrated voltage on C_F is sampled

and, immediately thereafter, the potential across C_F is re-set (i.e., flushed as noted above) to zero in preparation for the start of a new sample. A simple sketch of this voltage build-up over time T_{INT} is shown in Fig. 3.7. Not all of T_{INT} is available for purely signal integration purposes as time must be shared across a variety of operations. This compromise and the numbered features of the timing plots in Fig. 3.7 are further discussed in § 3.4.1.

The gain of the integrator stage is dependent on its integration time period T_{INT} and on the value of the feedback capacitor C_F used. Longer integration periods and smaller feedback capacitor values give higher gain. Formally, this gain can be expressed as

$$G_{INT} = \frac{K \cdot T_{INT}}{C_F} [\Omega] \quad (3.1)$$

where K represents the fraction of the integration period, T_{INT} , over which the TIA is actually allowing integration of the input.

What value of C_F is reasonable for a TIA geared towards biological nanopore sequencing applications? Clearly, estimates for required T_{INT} and G_{INT} as well as expected K can provide some guidance. Assuming my system can be arranged so that $K = 0.5$, the remaining terms can be approximated from basic signal considerations. For time, in § 2.4, I have already discussed the translocation frequency, f_t , realistically operating at 1000 bp/s. As also noted above, the preference is to sample this at $10\times$ rates. These estimate then point to a T_{INT} around 100 μ s.

For estimating desired G_{INT} we can consider that we want to be able to capture all the relevant current levels. Thus, as also discussed in § 2.4, we essentially need to digitize the current from about 200 pA to 55 pA, a range of about 150 pA. If we want this swing to be mapped across say 1-V (i.e., the input range of an ADC in a low-voltage technology) then we need an equivalent resistive gain of

$$G_{INT} = \frac{1 \text{ V}}{150 \text{ pA}} = 6.67 \text{ G}\Omega = 196 \text{ dB}\Omega. \quad (3.2)$$

Component	Effect	Settings
Integrator	Feedback Capacitor	26fF, 57fF, 100fF
Gm-C Filter	Current/Gm	3 Capacitor Settings
CDS	Gain	2x, 4x, 8x

Table 3.1: Gain and bandwidth options for components in each channel

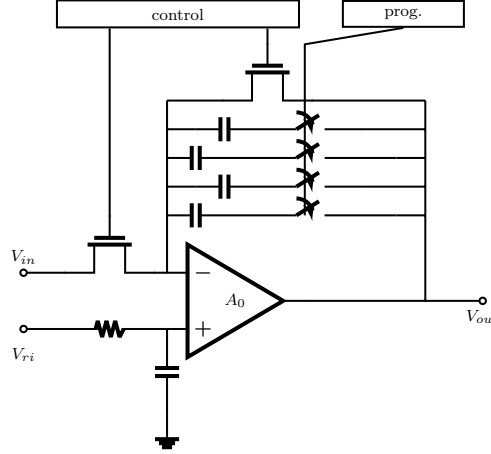


Figure 3.3: The TIA in more detail. Input, reset and capacitor gain bank and programming switches are indicated.

Thus, with the values noted above, (3.1) points to a feedback capacitance value of $C_F \approx 7.5$ fF.

Fig. 3.3 presents a more detailed implementation of the TIA. As shown, my design consists of three feedback capacitors that can be individually switched across the opamp. The control for the feedback capacitors is loaded into the configuration registers at chip startup. Table 3.1 shows the three sizes of the feedback capacitors used in the integrator. The three capacitors can be connected in any combination to obtain 7 different net feedback capacitances. The minimum capacitance implementable in 130 nm is 26 fF. To obtain a transimpedance gain of 196-dB Ω , a feedback capacitance of 7.5 fF is needed. This is not feasible in this technology, so the gain from the CDS has been used to further amplify the signal. The CDS also has 7 gain settings ranging from 2X-8X.

A folded-cascode operational transconductance amplifier (OTA) topology was used for the integrator and CDS. A folded cascode arrangement provides the high gain

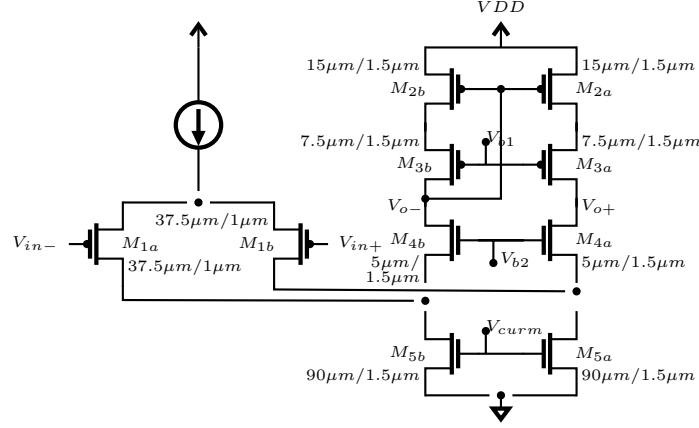


Figure 3.4: Transistor-level schematic of the folded cascode OTA used in the TIA.

needed to cancel the effect of the input capacitance of the nanopore sensor (that is, C_I shown in Fig. 3.2). It also does not require a compensation capacitor for stability, which reduces the area of the pixel compared to a two-stage OTA.

Fig. 3.4 shows the design of the opamp used in the ASP. In the folded cascode, I have used PMOS devices in the input stage because of their lower flicker noise. The W/L ratios of the input devices was set to $37.5 \mu\text{m}/1 \mu\text{m}$ to reduce flicker noise. The input devices are biased to operate in moderate inversion to maximize the transconductance of the input devices. Devices M_{5a} and M_{5b} also have large aspect ratios to minimize flicker and thermal noise by biasing them in moderate inversion.

The OTA consumes $105 \mu\text{A}$ current from a 1.2 V power supply. The opamp has been optimized for low noise. An input PMOS differential pair and large devices are used to reduce flicker noise. The opamp has a simulated thermal noise of $7.7 \text{ nV}/\sqrt{\text{Hz}}$ while the corner frequency is approximately 5 kHz . The open-loop DC gain of the opamp is 65 dB while the unity gain bandwidth is 100 MHz .

LPF

To implement an RC filter in the range of tens of kHz requires a large resistor and hence a large area. The resistor can also be implemented using a transconductor or active resistor. As a result, the LPF is implemented in the form of a G_m -C filter. In

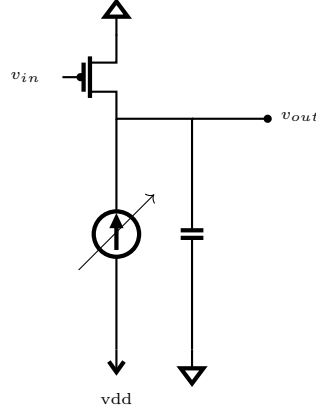


Figure 3.5: G_m -C filter transistor-level schematic.

my case a PMOS device configured as a source-follower was used to realize the G_m component. Though a MOSFET-C filter has better linearity, G_m -C filter methods typically demonstrate faster settling times [110]. Fig. 3.5 shows the schematic of the low-pass filter. The time constant of a G_m -C filter is given by

$$\tau_{\text{LPF}} = \frac{C_{\text{LPF}}}{g_m} \quad (3.3)$$

where C_{LPF} is the capacitor used in the filter and g_m is the transconductance of the transistor. The filter's time constant can be varied by either changing the capacitor or the g_m of the transistor. In this implementation, the time constant is varied by changing the g_m using the bias current while a $C_{\text{LPF}} = 1$ pF capacitance was used. The W/L of the PMOS device was chosen to be $1\mu\text{m}/2\mu\text{m}$. The PMOS source follower transistor was biased in the sub-threshold region and has a g_m that can be varied from 100 nS to 5 uS. The g_m of the voltage follower remains constant over a 0.05 to 1 V input voltage range. The G_m -C filter settles faster compared to a comparable RC filter due to its large V_{GS} during reset.

CDS

As mentioned in § 3.4, it is not possible to obtain a transimpedance gain of 196 dB only from an integrator stage. Hence, an active CDS was employed in the front-end

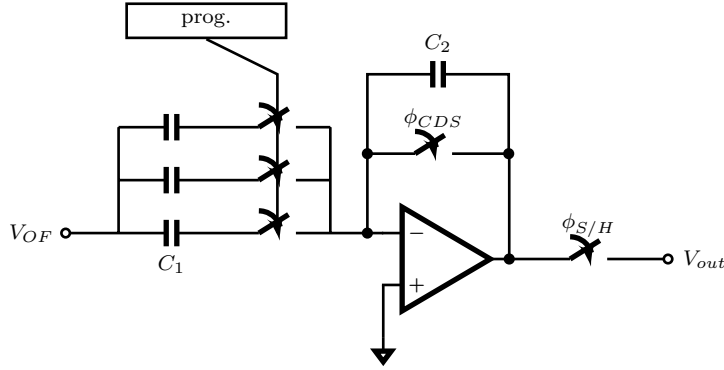


Figure 3.6: CDS component for each channel of the AFE with gain options determined by the C_1 capacitor bank settings.

which is shown in Fig. 3.6. By using an active, opamp-based, CDS, the signal can be further amplified before data conversion. The CDS uses the same opamp design as used in the integrator. The value of C_1 used is 350 fF while C_2 can be varied from 50 fF to 150 fF which can provide gain between $2\times$ - $8\times$. The effect of kT/C noise of C_2 is negligible.

3.4.1 AFE Timing

As noted above, the channel readout sequence is labeled in Fig. 3.7. The left side of this figure conveys the general nature of the voltage signal at the output of the TIA, while the right side of the figure conveys the clock phases driving the TIA and CDS reset switches, ϕ_1 and ϕ_{CDS} . Note that Fig. 3.7 only shows some of the readout system's controls that are being operated during read mode. In particular it only focuses on those controls used to regulate the TIA, LPF, CDS, and T/H components of a readout channel. Other timings related to programming of the AFE and the control of the ADC are not shown.

In summary, the four main AFE timing phases identified in Fig. 3.7 adhere to the following sequence

1. Reset the whole AFE chain with a high ϕ_1 setting. This flushes the AFE capacitors of voltage levels remaining from previous samples.

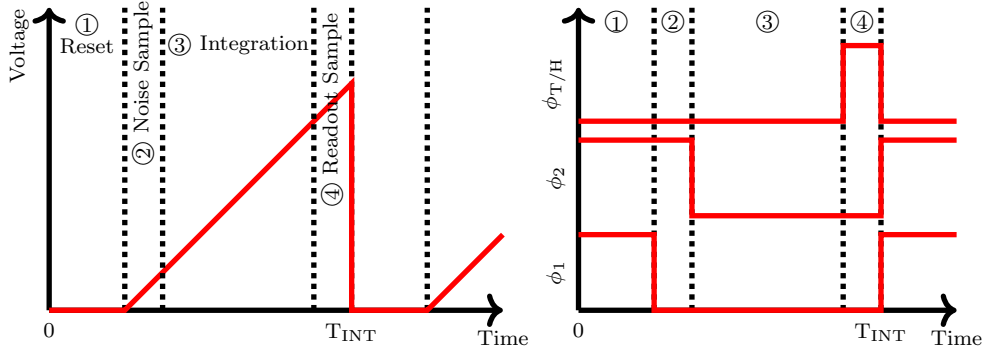


Figure 3.7: Illustration of the TIA output (related to the voltage across C_F) (left) and the timing of the clocks driving the TIA's reset switch (right). A high clock signal implies the switch is closed, while a low clock signal implies the switch is open.

2. Turn on the TIA and LPF with a low setting on ϕ_1 and ϕ_2 . This period serves to allow the TIA and LPF circuitry to settle once taken out of reset. The motivation being to prevent the contribution of transients to the sampled signal.
3. Turn on the CDS with a high ϕ_2 setting. With this, the integrated signal is actually being tracked.
4. At end of integration period sample the signal onto C_{TH} .

3.4.2 AFE Signal and Noise Analysis

In this section, I discuss the signal processing potential of the design in more detail. In particular, I focus on arguably the most important characteristic of nanopore signal processing AFEs: the noise behaviour. The noise transfer function of the TIA is different from the signal transfer function. Firstly, I start by calculating noise transfer of the TIA.

Noise Transfer Function

The **noise transfer function** of the TIA can be calculated in three steps:

- Noise of the integrator opamp amplified due to parasitic input capacitance, C_{IN} .
- Noise filtering due to the filter
- Noise shaping due to CDS and sampler

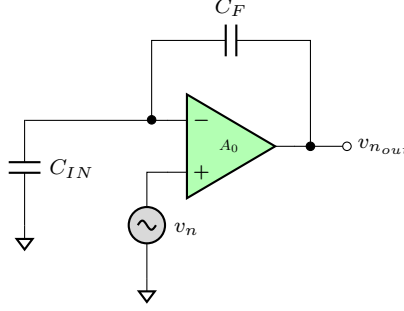


Figure 3.8: Equivalent circuit of the AFE's first-stage integrator opamp with input-referred opamp noise.

Since the TIA has a synchronous reset, the noise analysis of the AFE can assume the first-stage integrator circuit shown in Fig. 3.8. The input-referred noise of the opamp, v_n , is amplified and filtered by the transfer function (TF) of the integrator arrangement in which the opamp is used. The TF of the integrator is given by

$$H_i(\omega) = \frac{C_T}{C_F + C_T/A_0} \cdot \frac{1}{1 + \omega/\omega_c} \quad (3.4)$$

where

$$C_T = C_F + C_{IN} \quad (3.5)$$

and where C_F is the integrator feedback capacitor, C_{IN} , is the nanopore parasitic capacitor, A_0 is the DC gain of the opamp and ω_c is the 3-dB cut-off frequency of opamp. This noise is also filtered by the LPF following the integrator (neither the LPF nor the CDS are shown in Fig. 3.8). Accounting for the LPF, the TF in (3.4) can be expanded to

$$H_{LPF}(\omega) = \frac{C_T}{C_F + C_T/A_0} \cdot \frac{1}{1 + \omega/\omega_{LPF}} \quad (3.6)$$

The power spectral density (PSD) at the output of LPF is given by

$$S_{LPF}(\omega) = |H_{LPF}|^2 \cdot v_n^2 \quad (3.7)$$

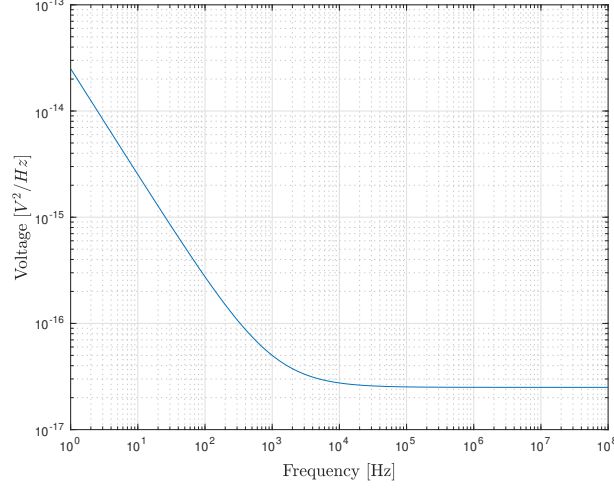


Figure 3.9: Integrator opamp noise model

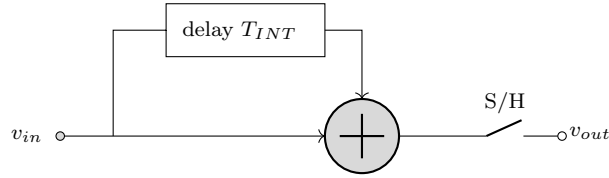


Figure 3.10: CDS equivalent circuit

The spectral density of amplifier noise (v_n) can be modelled using [111]

$$v_n(\omega) = v_{V_0} \left(1 + \frac{\omega_{flc}}{\omega} \right) \quad (3.8)$$

where v_{V_0} is the amplifier's thermal voltage noise density and ω_{flc} is the flicker noise corner frequency. Representative values for these terms in the technology I used for this work (TSMC 130-nm CMOS) are $S_{V_0} \approx 2.5 \times 10^{-17} \text{ V}^2/\text{Hz}$ (i.e., $v_{V_0} \approx 5 \text{ nV}/\sqrt{\text{Hz}}$) and $\omega_{flc} \approx 10 \text{ kHz}$. The PSD modelled by (3.8) is shown in Fig. 3.9.

The transfer function of the CDS is given by [112]

$$H_{CDS}(\omega) = |2 \cdot G_{CDS} \cdot \sin(\omega T_{INT})| + |2 \cdot G_{CDS} \cdot H_{ThN}| \quad (3.9)$$

where G_{CDS} is the gain of the CDS stage and H_{ThN} is the TF of thermal noise from the LPF to the CDS output. Eq. (3.9) has two parts, its first addend corresponds to

the high pass filtering imposed by the CDS on the flicker noise. As thermal noise is uncorrelated noise, it is not cancelled by the CDS. In fact, it is doubled. Hence, a second addend is present in (3.9) to represent the amplified thermal noise.

The PSD at the output of CDS is given by

$$S_{CDS}(\omega) = |H_{CDS}|^2 \cdot S_{LPF} \quad (3.10)$$

Finally, the PSD at the output of S/H is given by

$$S_{OUT}(\omega) = |H_{S/H}|^2 \cdot S_{CDS} = |\text{sinc}(\omega T_S/2)|^2 \cdot S_{CDS} \quad (3.11)$$

Signal Transfer Function

The **signal transfer function** can be calculated in two steps:

- Integration stage
- Differentiation (CDS) stage

The signal transfer function is given by

$$H_{SIG}(\omega) = R_{TIA} \cdot |\text{sinc}(\omega T_{INT})| \quad (3.12)$$

where

$$R_{TIA} = \frac{K \cdot T_{INT}}{C_F} \cdot G_{CDS} \quad (3.13)$$

here R_{TIA} is equivalent resistance of TIA and, as discussed earlier, K is the fraction of the sampling period where integration is performed. The signal transfer function at various sampling frequencies is shown in Fig. 3.11.

Fig. 3.12a shows the input referred noise density of the DT-AFE for various sampling frequencies, f_S , with C_{IN} set to 5 pF. The flat profile at low frequencies is indicative of the degree to which the system suppresses flicker noise. At $f_S = 1\text{-kHz}$ sampling frequencies the system can achieve a sub 0.1 fA/ $\sqrt{\text{Hz}}$ spot noise. Naturally,

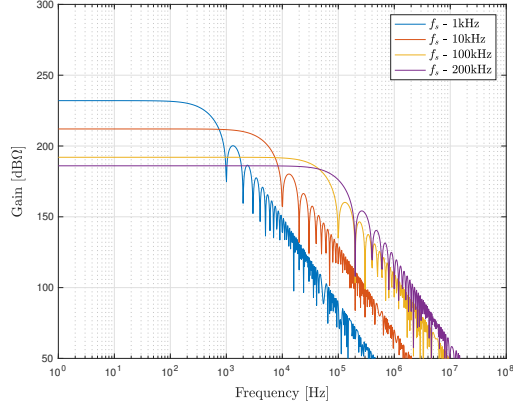


Figure 3.11: Signal transfer function of the DT-TIA.

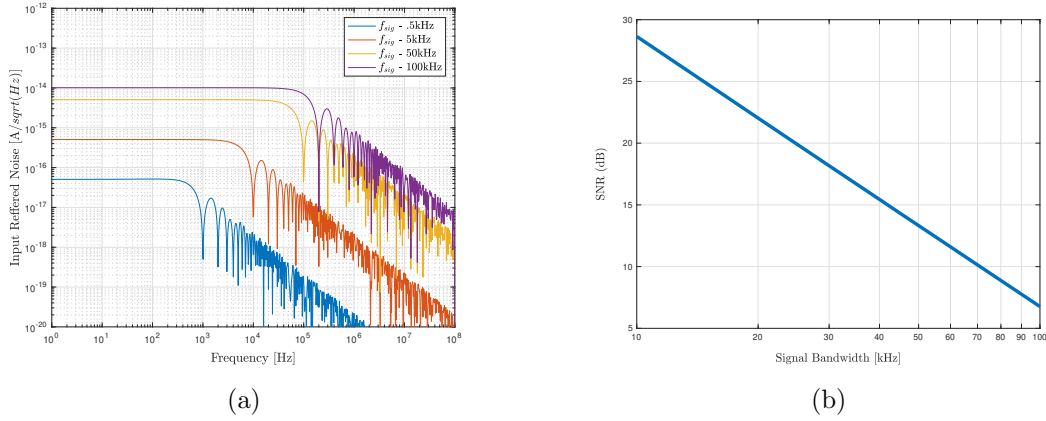


Figure 3.12: a) Input referred noise of DT-TIA. b) SNR with respect to signal bandwidth for DT TIA model.

this value rises in proportion to the sampling frequency as a result of the diminishing transimpedance gain. At $f_{sig} = 50$ kHz this parameter reaches $6 \text{ fA}/\sqrt{\text{Hz}}$.

Integrating the input-referred noise density across operating bandwidth we approximate the system SNR as a function of signal bandwidth in Fig. 3.12b. This estimate demonstrates the potential of DT-AFEs for future nanopore sequencers. For DT-AFEs based on $5 \text{ nV}\sqrt{\text{Hz}}$ amplifiers, a 20-dB SNR is possible for 25-kHz signals, 6.25 times greater than the ONT's Minion (4 kHz).

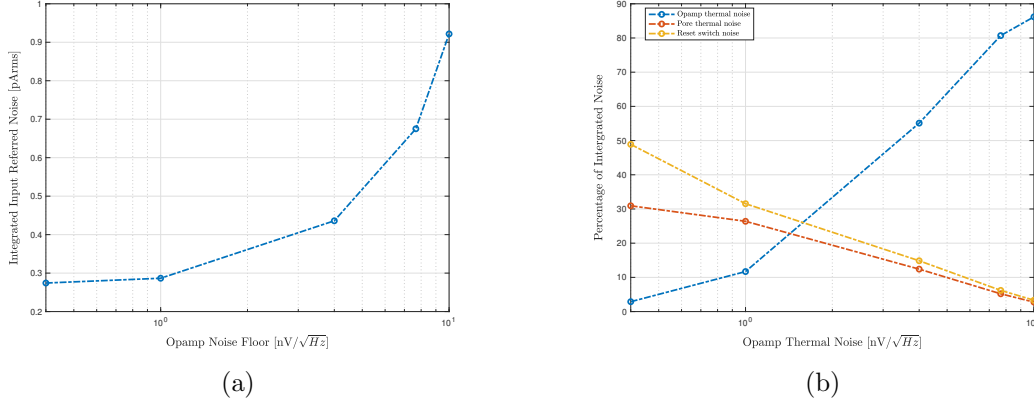


Figure 3.13: (a) Integrated input-referred noise with respect to opamp thermal noise floor at 10 kHz sampling rate, 5 pF input capacitor and 20 fF integrator feedback capacitance (b) major noise contributors [in percentage] with respect to the opamp thermal noise floor.

System Noise Simulation with a Modelled Opamp

The system performance is dependent on the noise of the opamp, as captured in the noise analysis just above. There are other noise sources as well that contribute to the input noise of the system. As the opamp noise is reduced, these noise sources become limiters to the performance of the system. To investigate this, the opamp was modelled using Verilog-A. Its thermal and flicker noise were captured in a macromodel.

Using the modelled opamp, the performance of the amplifier was simulated using periodic steady state (PSS) analysis in Spectre. The resulting noise behaviors, integrated noise and noise components, are shown in Fig. 3.13. It is evident from Fig. 3.13a, which shows the integrated input referred noise(0-10 kHz) as a function of the opamp noise floor, shows that reducing opamp noise below $1 \text{ nV}/\sqrt{\text{Hz}}$ does not provide a significant improvement in overall performance. The thermal noise of the nanopore and the shot noise of the reset switch become the major contributors, as shown in Fig. 3.13b.

Using $1 \text{ nV}/\sqrt{\text{Hz}}$ as the opamp noise, the maximum bandwidth of the nanopore system with a synchronous DT amplifier was estimated. From behavioural models of opamp, it was discovered that DT amplifier can achieve approximately 50 kHz

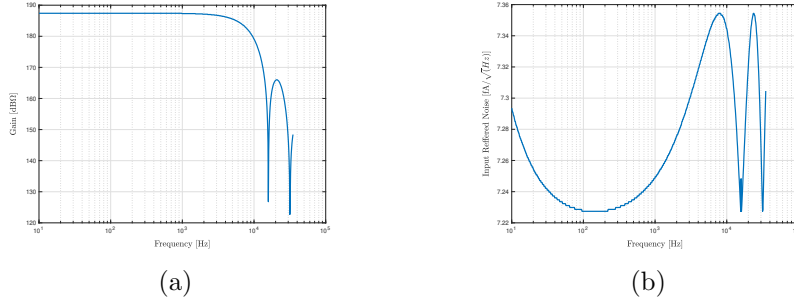


Figure 3.14: (a) Simulated gain of the TIA and (b) simulated input referred noise of the TIA.

bandwidth (maximum attainable bandwidth with synchronous reset amplifier) at a SNR of 20 dB (i.e., integrated input referred noise of 1.5 pArms).

In my design, I have used an opamp with a noise floor of $7.7 \text{ nV}/\sqrt{\text{Hz}}$. This was chosen to trade off power consumption with performance. Implementing an opamp with $1 \text{ nV}/\sqrt{\text{Hz}}$ would require significant power and this could cause heating issues for an array with hundreds of channels.

3.4.3 AFE Simulation Results

Simulations of the amplifier from Fig. 3.2 were carried out using IC EDA tools from Cadence, mainly Virtuoso and Spectre. As noted above, the target technology for this work was TSMC 130-nm CMOS.

The simulated gain and input-referred noise of the TIA are shown in Figs. 3.14a and 3.14b, respectively. The noise and gain of the amplifier were simulated using periodic steady-state (PSS) analysis in Spectre. To avoid incorrect simulation results, special attention is needed on the control signals used to operate the amplifier. These controls act as large-signal inputs and can result in incorrect beat frequency settings for the PSS analysis. The noise was simulated with a 5 pF input capacitance. The flicker noise was significantly reduced as expected and its contribution to total noise was approximately 5%.

Fig. 3.15 displays the eye diagram resulting from the transient simulation of the

integrator, filter, and CDS. This simulation was conducted with transient noise enabled, and the signal was superimposed on multiple integration periods to generate the eye diagrams. As illustrated in Fig. 3.15(a), significant noise is evident after the reset due to the reset noise of the switch.

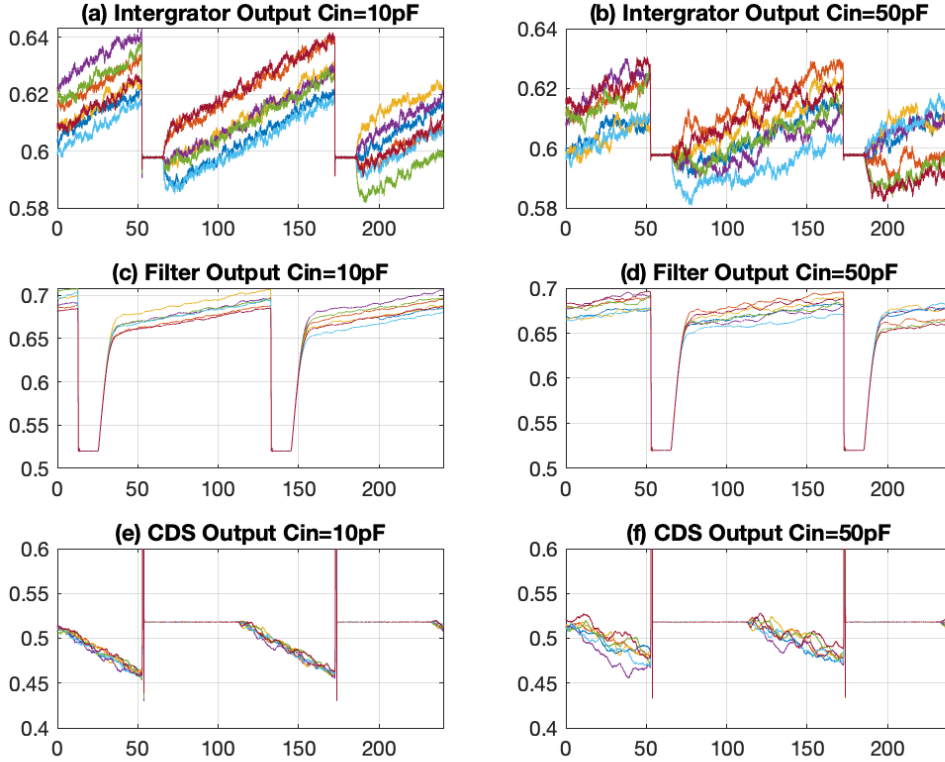


Figure 3.15: Eye-diagram of AFE transients with noise from form the integrator, filter, and CDS included.

Following the reset, fluctuations arise from the noise of both the opamp and the sensor. An increase in input capacitance also elevates the noise, as indicated in Eq. (3.4) and evident from Fig. 3.15b, comparing $C_{in} = 10$ pF to $C_{in} = 50$ pF. The filter reduces this noise by lowering the corner frequency, as shown in Fig. 3.15c and 3.15d.

Finally, CDS is employed to mitigate the effects of reset switch noise and flicker noise, as demonstrated in Fig. 3.15e and 3.15f. If the signal were sampled at the end of the integration period from the LPF, the noise width would be substantially

greater than that observed after the CDS.

3.5 ADC

The accuracy of the ADC needed to digitize the signal is dictated by the basecalling algorithm used. According to [77], about 8 bits are needed to basecall with acceptable accuracy. Thus, a 10-bit ADC gives extra design headroom. The choice of ADC architecture is driven by resolution, power, area and disturbances caused by its digital blocks. To integrate 100s of channels on-chip, each block needs to be low power and have small area. But the ultra-sensitive amplifiers call for another important factor to be considered: their sensitivity to substrate noise and capacitive couplings. Therefore, an architecture with low clock rate and low power digital blocks would be preferred to reduce disturbance. SAR ADC emerges as a candidate that fits the requirements.

SAR ADC

A successive-approximation-register (SAR) ADC converts an analog signal to a digital representation using a binary search algorithm. SAR ADCs are usually used for medium resolution and data rates in the range of a few mega samples per second (MSps) while operating at low power. There are various architecture options for SAR ADCs but the simplest architecture is shown in Fig. 3.16. This SAR ADC consists of a capacitive digital-to-analog converter (DAC), a comparator and digital circuits to perform a binary search algorithm. The digital output of the ADC can be in serial or parallel form.

An illustration of a 5-bit analog-to-digital conversion by a SAR ADC is shown Fig. 3.17. The high supply of the inverter is connected to a high reference voltage (v_{refp}) and low supply of inverter is connected to (v_{refn}). First, the input voltage is sampled on the DAC. During the first clock cycle of conversion only the MSB bit of the

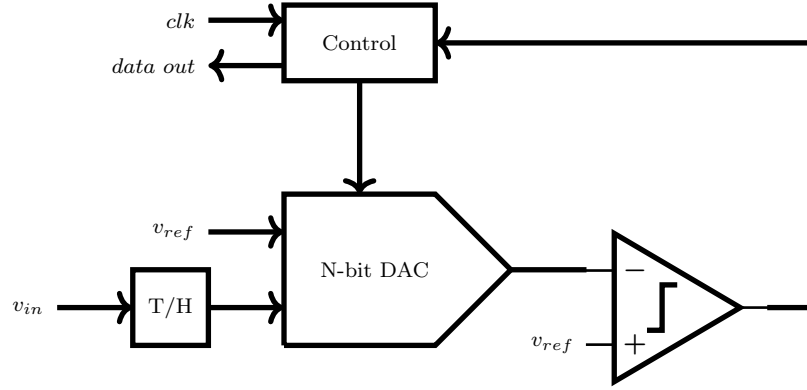


Figure 3.16: SAR ADC block diagram.

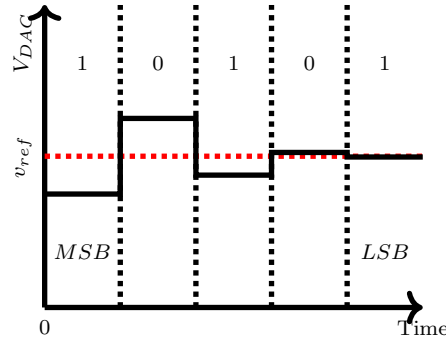


Figure 3.17: Illustration of a 5-bit analog-to-digital conversion by a SAR ADC.

DAC is connected to the high reference voltage (v_{refp}) (a more detailed explanation of DAC operation is provided later in this section). If the voltage is less than the comparator reference voltage (v_{refh}), the comparator output is high (logic 1). This is recorded by the control logic. For the next cycle, the DAC configuration from the last conversion is loaded; as well, the next significant bit is connected to $v_{refhigh}$. If the output of the comparator is low, this bit of the DAC will be connected to a lower reference voltage (v_{refn}) in next conversion period. This sequence of actions continues until all the SAR bits are determined. At the end of conversion, the output of the SAR (*dataout*) can be accessed from serial or parallel outputs.

Capacitive DAC

Usually, in a capacitor bank, multiple switches are needed to first sample the input voltage and then connect it to the high or low reference voltages. To simplify

the design we have used an inverter-based technique proposed in [113]. For this inverter-based method no comprehensive theoretical explanations regarding its operation have been presented in the literature. Hence, I provide a more detailed discussion of inverter-based capacitor bank operation below.

In this design, the sampling of the input voltage is done from the top plate of the DAC capacitors. In common textbook discussions of typical SAR operation, the DAC references are assumed to be taken from the bottom plate. Hence, the governing equations for inverter-based capacitor bank operation differ from the ones found in data converter textbooks.

As noted, the sampling of the input voltage for the inverter-based design is conducted from the top plate of DAC capacitors, while references are applied to their bottom plate as shown in Fig. 3.18. The DAC has two main operation modes: Sampling Mode and Redistribution Mode. During sampling mode, the input voltage is sampled on the DAC while in the redistribution mode, the binary search is performed. These modes are now further detailed.

Sampling Mode: For simplicity, a 5-bit binary-weighted DAC is used in this analysis, the configuration of its capacitor bank is shown in Fig. 3.18. During the initial sampling phase, the MSB capacitor is connected to V_{refp} , and all other capacitors are grounded. The input voltage is then sampled on the top plate of these capacitors.

Redistribution Mode: In this phase, the output voltage of the DAC is compared with $V_{refh} = \frac{V_{refp} + 0}{2}$.

- Clause 1: $V_{in} < V_{refh}$: The output of the comparator would be low. Under this condition, the MSB is inferred as zero.
- Clause 2: $V_{in} > V_{refh}$: The output of the comparator would be high. In this case, the MSB is inferred as one.

Subsequently, the analysis proceeds to the next bit. Depending on the inferred value of the MSB, two scenarios are possible, and adjustments to the capacitor bank

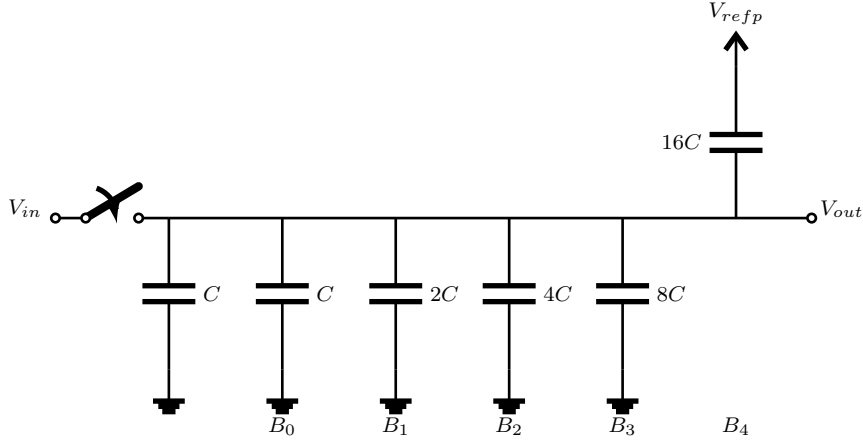


Figure 3.18: Initial DAC configuration during sampling phase

are made accordingly:

- Clause 1: $MSB = 0$: In this step, both the 16-unit and the 8-unit capacitor banks are connected to V_{refp} , as illustrated in Fig. 3.19. The output voltage of the DAC after redistribution is determined by equating the initial and final charges in the capacitor bank. The initial charge, Q_I , is given by:

$$Q_I = 16C(V_{refp} - V_{in}) + 16C(0 - V_{in}) \quad (3.14)$$

This equation reflects the charge across all capacitors when the MSB capacitor is connected to V_{refp} and the others to ground.

The final charge, Q_F , after the redistribution is:

$$Q_F = 24C(V_{refp} - V_{in}) + 8C(0 - V_{in}) \quad (3.15)$$

This equation accounts for the connection of the 24-unit capacitor to V_{refp} and the 8-unit capacitor to ground in the redistribution phase.

By the principle of charge conservation, the initial charge must equal the final charge:

$$Q_I = Q_F \quad (3.16)$$

Solving the charge conservation equation:

$$16C(V_{refp} - V_{in}) - 16CV_{in} = 24C(V_{refp} - V_{in}) - 8CV_F \quad (3.17)$$

From this, we derive the final voltage, V_f :

$$V_f = V_{in} + \frac{V_{refp}}{4} \quad (3.18)$$

The MSB-1 is then determined based on V_f relative to V_{refh} :

- If $V_f < V_{refh}$, then MSB-1 is inferred as zero.
- If $V_f > V_{refh}$, then MSB-1 is inferred as one.
- Clause 2: $MSB = 1$: In this configuration, the 16-unit capacitor bank remains connected to GND , and the 8-unit capacitor bank is switched to V_{refp} , while all remaining capacitors continue to connect to GND as depicted in Fig. 3.20.

To analyze this scenario, we again apply the principle of charge conservation and equate the initial and final charges in the capacitor bank:

$$16C(V_{refp} - V_{in}) - 16CV_{in} = 8C(V_{refp} - V_{in}) - 24CV_F \quad (3.19)$$

Simplifying this equation, the final voltage, V_f , is determined as follows:

$$V_f = V_{in} - \frac{V_{refp}}{2} + \frac{V_{refp}}{4} \quad (3.20)$$

Here, V_f represents the redistributed voltage which is subsequently compared against V_{refh} to infer the next significant bit (MSB-1):

- If $V_f < V_{refh}$, then MSB-1 is inferred as zero.
- If $V_f > V_{refh}$, then MSB-1 is inferred as one.

These steps are repeated iteratively to determine the remaining bits of the DAC's output.

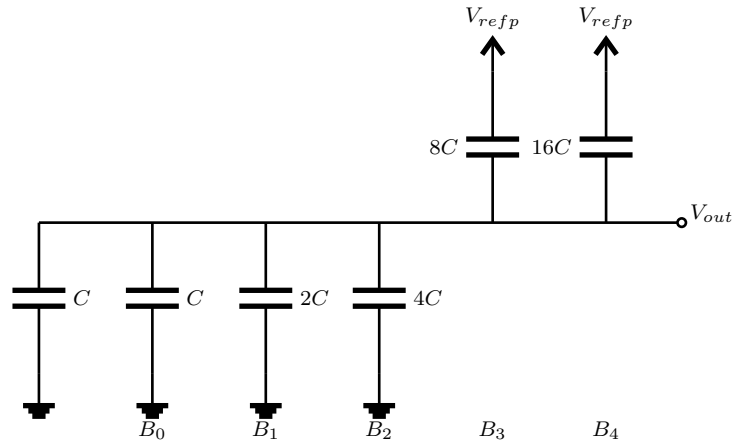


Figure 3.19: DAC in second bit conversion when MSB = 0

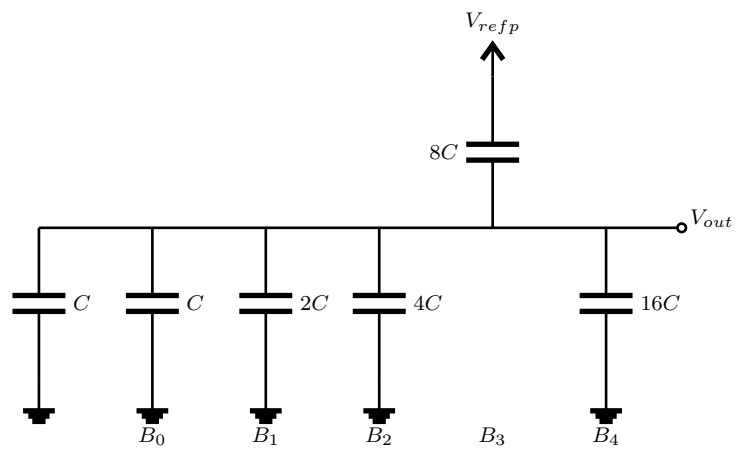


Figure 3.20: DAC in second bit conversion when MSB = 1

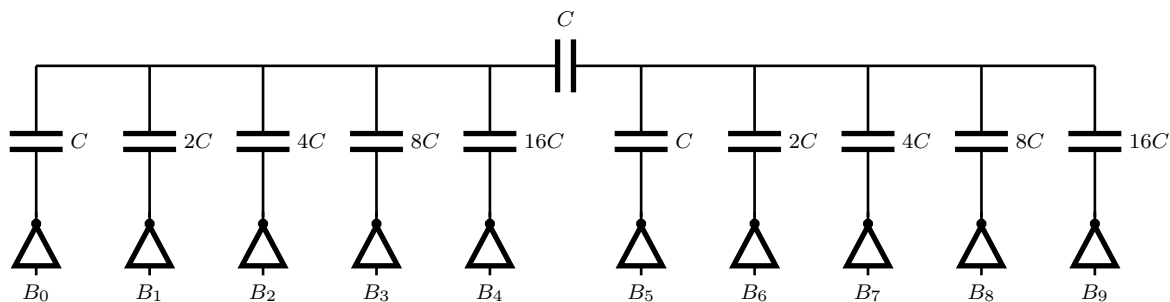


Figure 3.21: Split Attenuated DAC

In a SAR ADC, a binary weighted capacitive array is used. The use of a capacitive array provides the opportunity for low power operation, but can consume a significant portion of a chip's area. Increasing ADC resolution by one bit usually doubles the area of the capacitive DAC. A N -bit binary weighted capacitive array require 2^N unit capacitors. There are ways to reduce the area of a capacitive array. Area can be reduced using a 'spilt capacitor' technique or C2C capacitive array technique [114]. C2C usually results in the lowest area requirements but is very sensitive to parasitic capacitance causing the effective number of bits (ENOB) to degrade. In this design, a spilt capacitor array was used as shown in Fig. 3.21. In a spilt capacitor array, a series capacitor is used to separate the capacitor banks. The series capacitor acts as an attenuator and reduces the size of capacitors required. Precisely, for a N -bit DAC the capacitance needed goes from 2^N to $2 * 2^{(N/2)} - 1$ [114].

To reduce the area of the DAC, a small unit capacitor should be used. But making a unit capacitor small makes the design more susceptible to parasitic capacitance. To mitigate the effect of parasitics, routing needs to be planned carefully. An interesting method to overcome this problem has been shown in [7]. I have used this layout structure in my implementation. The layout described there implements a common centroid plan to reduce the effect of fabrication process gradients. The array is divided into two parts, and the routing is done between them. This helps in reducing the inter-bit coupling parasitics.

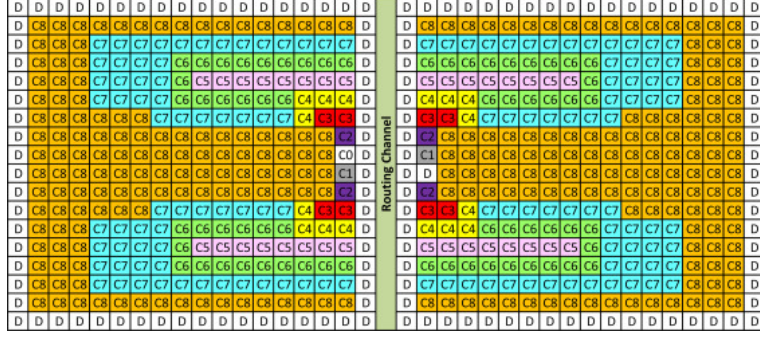


Figure 3.22: DAC layout for SAR ADC with routing consideration [7].

Latched Comparator

A latched comparator is used in the SAR ADC to update the conversion register based on the DAC output. Such a comparator design uses positive feedback to regenerate an analog input signal to a digital signal. It works in two phases: a reset phase and a regeneration phase. In the reset phase, the comparator acts as an amplifier. In the regeneration phase the small amplified signal is converted to a digital level using positive feedback.

There are three main types of latched comparators found in the literature [115]:

1. Static latch comparator - Static power, low regeneration speed and high kickback noise.
2. Class AB latch comparator - More power efficient than static latch comparator, medium kickback noise and medium regeneration speed.
3. Dynamic latch comparator - High power efficiency, low regeneration speed and high kickback noise.

For this design, a class AB latch comparator was implemented. It has acceptable kickback noise and high regeneration speed. A dynamic latch comparator has very high kickback noise which corrupts the signal for a split capacitor bank. The schematic of the implemented latch is shown in Fig. 3.23.

During this comparator's reset phase, clk is low and M_4 is in the cutoff region while M_5 is in the triode region. This means that the input differential pair, M_{1a} and M_{1b} ,

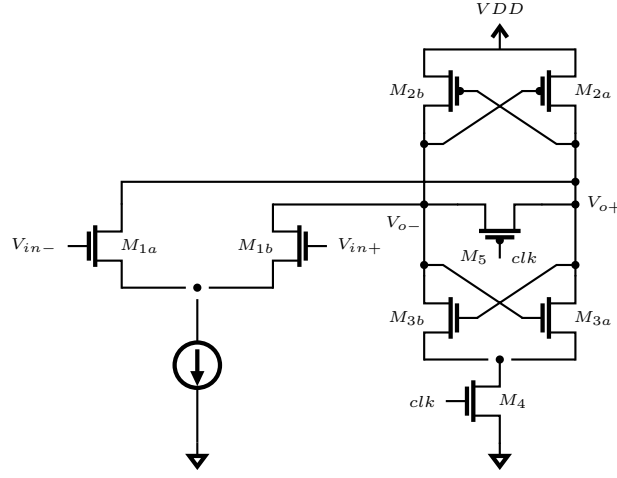


Figure 3.23: Class AB latched comparator schematic.

acts as an amplifier with M_{2a} & M_{2b} acting as its load. During the regeneration phase, clk is high and the voltage between nodes V_{o+} & V_{o-} is amplified due to positive feedback. The large voltage swing from the M_{2a} & M_{2b} is not completely isolated from the drain of the input devices. Hence, kickback is noticed in this type of amplifier.

SAR Logic

The SAR Logic was implemented in Verilog. The Verilog code was synthesised using Synopsys Design Compiler while the layout was generated using Cadence Encounter.

RC filter on ADC Digital supply

As highlighted several times, the sensitive nature of circuits was discovered in post-layout chip level simulations that transient currents from 30 ADCs can cause errors in analog-to-digital conversions as well as in amplification. To fix this problem, I have added the RC filter to the digital supply of the ADCs. Each ADC contains its own RC filter implemented using an active resistor and MOS capacitor. The RC filter slows the current transients as a result of the switching of digital circuits.

3.5.1 Simulation Results

3.5.1.1 Dynamic ADC Performance

I have compared the dynamic performance of the ADC with a simple binary weighted DAC (BW-DAC) and an attenuated capacitor DAC (AC-DAC). The post-layout simulation results comparison between BW-DAC and AC-DAC are shown in Table 3.2. The AC-DAC banks suffer from heavy distortion due to kickback noise due to smaller total capacitance. The BW-DAC shows better performance compared to the AC-DAC, but requires a much larger area. The AC-DAC demonstrates a SINAD of only 45.6 dB while the BW-DAC reaches a SINAD of 59.65 dB. Thus, according to standard estimates, the AC-DAC experiences about 2.5 bits of degradation in ENOB relative to the BW-DAC.

Although BW-DAC has better ENOB compared to AC-DAC, to minimize the area of each channel, I have implemented the AC-DAC based ADC to trade of performance with area of each channel. AC-DAC ENOB can be improved with some digital correction which I have presented in § 4.5.1. The post-layout transient simulation result and the output spectrum of the AC-DAC based ADC is shown in Fig. 3.24. To obtain worst-case performance, the sine-wave input is close to the sampling frequency used. Also, to minimize the effect of measurement on the signal, the coherent sampling technique is used. The input sine-wave frequency was set to $(251/512) \times 100$ kHz as the spectrum was obtained using 512 samples and the sampling rate was 100 kHz.

The importance of capacitor bank layout parasitics and matching is also demonstrated by measuring the ENOB in Monte Carlo simulations. Fig. 3.25 shows the ENOB of DAC only simulation.

3.5.1.2 Comparator Noise Results

The noise and gain of the latched comparator are shown in Fig. 3.26. This simulation was performed using sampled periodic AC and periodic noise analysis in Spectre. The

	BW-DAC	AC-DAC
ENOB	9.61 bits	7.29 bits
SINAD	59.65 dB	45.6 dB
SNR	60.52 dB	57 dB
SFDR	69.94 dB	48.85 dB
Noise Floor	-90.55 dB	-86 dB

Table 3.2: Simulated dynamic performance of ADC with BW-DAC & AC-DAC

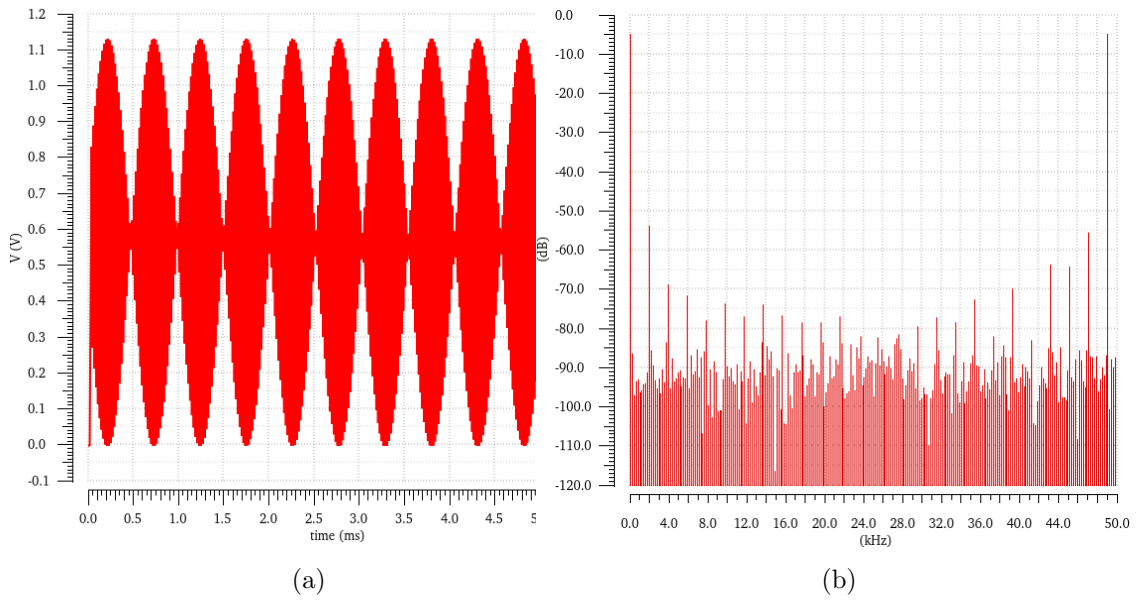


Figure 3.24: a) Transient Output of $(251/512) * 100$ -kHz input sine wave with 1V pk-pk b) Spectrum of $(251/512) * 100$ -kHz input sine wave with 1V pk-pk.

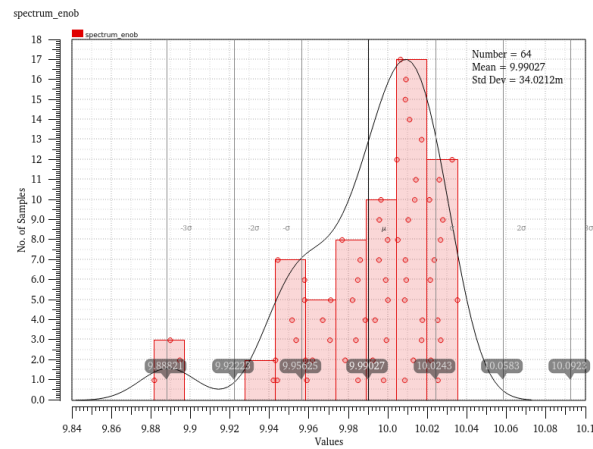


Figure 3.25: Histogram of ENOB for matched capacitive BW-DAC only generated using MC simulation.

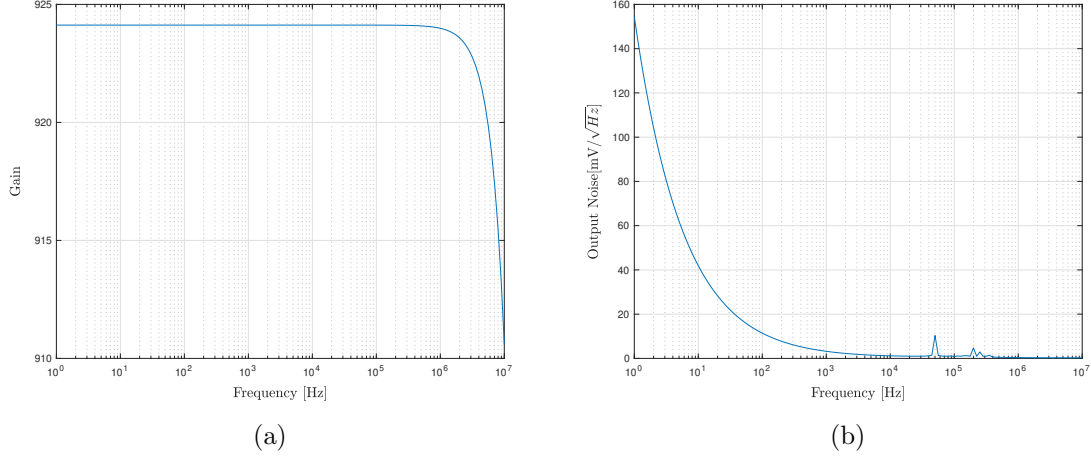


Figure 3.26: a) Gain of the latched comparator b) Output noise of the latched comparator

gain and noise presented in Fig. 3.26 are measured during latch regeneration when the two phases are 50 mV apart after reset. Fig. 3.26 provides the small noise and gain of the comparator. Fig. 3.27 shows the cumulative distribution function (CDF) obtained using transient noise method. The noise of latch comparator was measured to be 2.9 mV_{rms} using this method. To achieve a readout rate of 100 kSps with a 10-bit ADC, the comparator must perform 10 comparisons per analog-to-digital conversion. Consequently, the comparator is required to operate at a speed of 1 MSps. The integrated input referred noise of the comparator measured using Pnoise simulation at a sampling rate of 1 MSps is 2.7 mV_{rms} . For a 1 V pk-pk signal, the LSB of a 10-bit ADC is approximately 0.97 mV. Therefore, the noise of the comparator is approximately 8 LSBs ($2.7 mV_{rms} \times 2.828 / 0.97 mV$). Ideally, the comparator noise should much less than 1 LSB but this simulation was performed after the design of the chip.

3.6 System

The area of the implemented chip is $3 \times 2 \text{ mm}^2$. The area of each channel is 0.075 mm^2 ($0.25 \times 0.3 \text{ mm}^2$). The power consumption of each channel include TIA & ADC is 0.3 mW. The layout of the implemented chip is shown in Fig. 3.28. The die

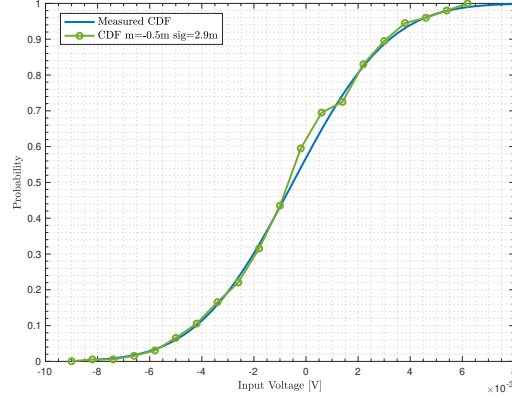


Figure 3.27: Latch comparator noise cumulative distribution simulated to measure integrated noise

Table 3.3: Performance summary for the nanopore detector array

System	
Technology	0.13 μm
Supply Voltage	1.2 V
Chip Dimensions	3 mm $\times$ 2 mm
No. of Channels	30
Power Dissipation of Array	10.25 mW
Interference	0.1%
Channel	
Bandwidth	0-100 kHz
Area	320 $\mu\text{m} \times$ 220 μm
Input-Ref. Noise ($C_{in}=2$ pF)	1.5 pArms @ 7.87 kSps

micrograph of the test chip is shown in Fig. 3.29.

A summary of the system’s main physical and performance characteristics is given in Table 3.3.

3.7 Measurement Setup & Results

High-gain amplifiers require meticulous design choices to ensure accurate signal measurement and minimal noise interference. Critical considerations include the selection of signal sources to mimic DNA sequencing, digital control circuits, and the strategic

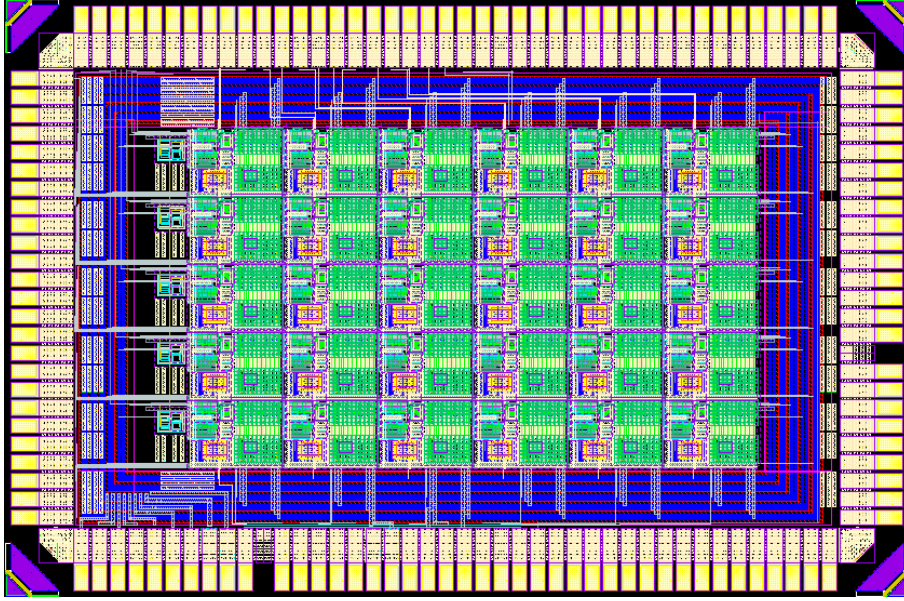


Figure 3.28: Layout of the complete chip.

placement of noisy circuits to avoid unwanted interference. Additionally, it was essential to design a system capable of building a real-time digital readout needed for performing DNA experiments.

Digital Control and Readout System

A programmable logic controller is needed to configure the shift registers in DROIC, to provide control signals to the TIA and ADC, and to forward data to a graphical user interface (GUI) for observations. A complex programmable logic device (CPLD) instead of a field programmable gate array (FPGA) was used in my design. CPLDs do not need any external oscillator on the PCB. This is very useful as it provides isolation from the noisy large signal of the oscillator.

A separate FPGA (Xilinx Zynq 702) was used that sends data to the GUI using Ethernet. The CPLD placed on the testboard PCB connects to the FPGA using two 50 Ohm SMA cables. Specifically, the CPLD serializes the data received from the DROIC ADCs and forwards it to the Xilinx Zynq 702 FPGA board via the two SMA cables. One SMA cable is used to send the clock while the other cable is used

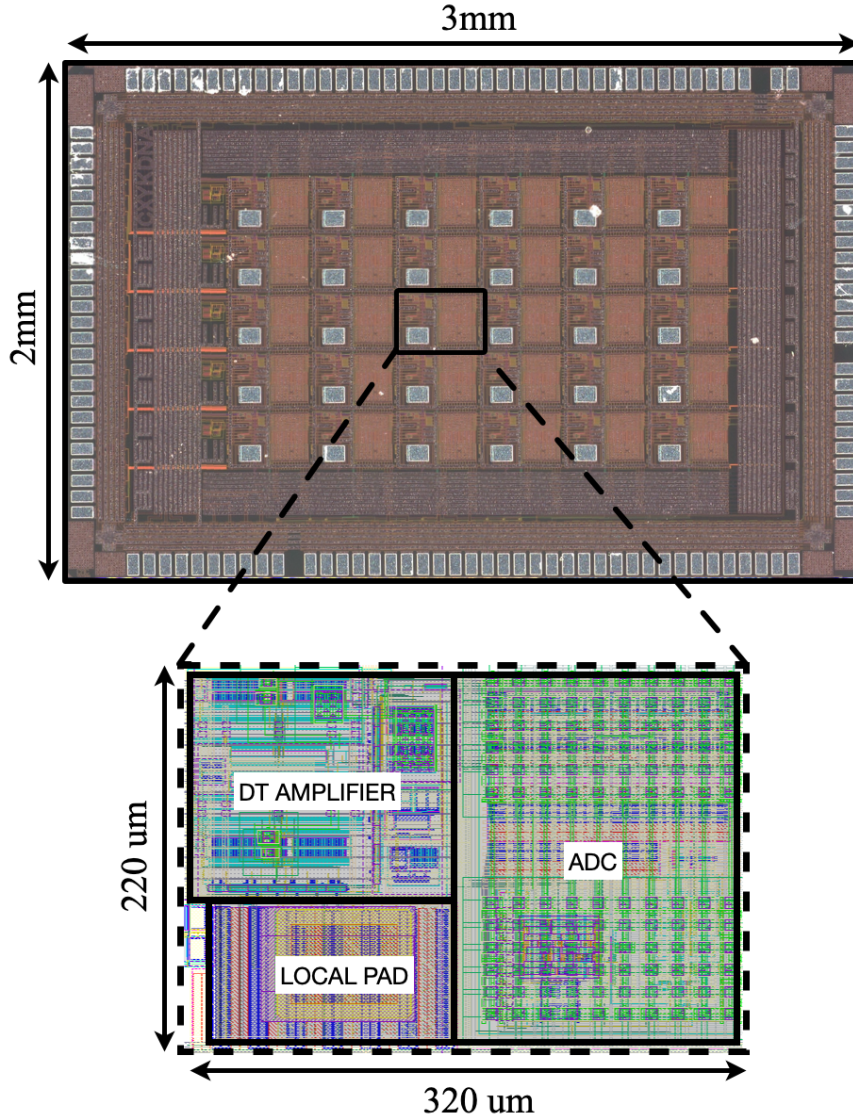


Figure 3.29: Chip micrograph and detailed floorplan of a channel.

for data. A custom communication protocol was designed to minimize noise and help with synchronization by the sampler IP implemented in the FPGA. An example timing diagram of the custom two-wire interface is shown in Fig.3.30. Each packet starts with 9 clock cycles during which the data is asserted high, serving as the start synchronization. The next 50 clock cycles represent the readout data for 5 rows of ADC. Finally, during the last 9 clock cycles, the data is de-asserted, which serves as the end synchronization.

The block diagram of the readout system implemented in the FPGA is shown

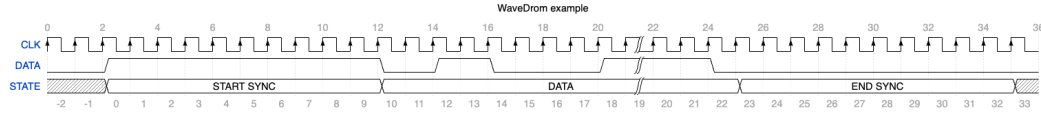


Figure 3.30: Custom two wire interface protocol for readout.

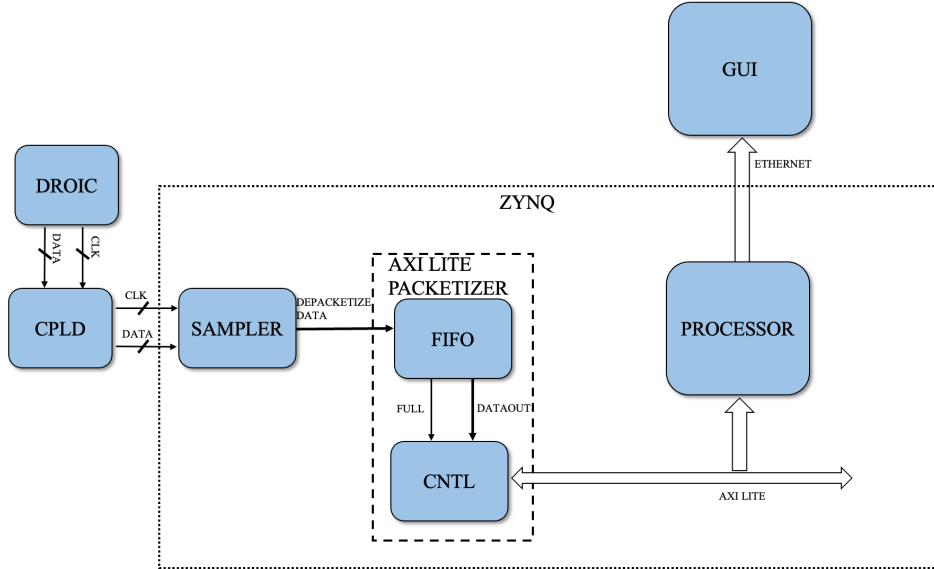


Figure 3.31: DROIC readout system implemented on Zynq FPGA.

in Fig. 3.31. The FPGA receives the serialized data along with its clock from the CPLD and deserializes the data. A custom IP, the *sampler*, was implemented and is responsible for deserializing the data into 10 bit packets. The block diagram of the sampler block is shown in Fig.3.32. The signals *clk* and *data* from CPLD are synchronized using synchronization flip flops to the FPGA clock. These synchronized signals are used by the state machine to find the start of the packet and de-serialize the data. The deserialized data is transmitted to the memory-mapped FIFO buffer via a 10 bit bus. The *sampler* issues an interrupt to FPGA's hardcore ARM processor once every eight ADC samples that have been received from DROIC. The processor services this interrupt and reads the eight ADC sample from the memory-mapped FIFO buffer using an AXI-LITE interface. The AXI-LITE connection allows for an eight-packet burst readout, which reduces the data transfer overhead.

This data is transferred by the FPGA processor via a TCP/IP socket to a JavaScript

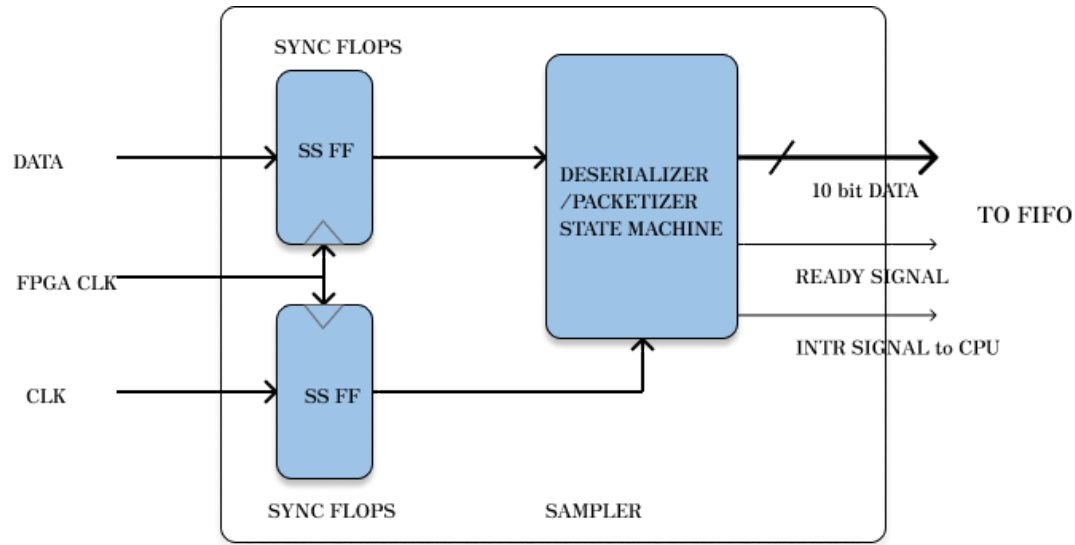


Figure 3.32: Block diagram for *sampler* IP

graphical user interface (GUI) application running on a desktop PC. The data is plotted and saved by the PC's GUI in real-time. To guarantee real-time operation, the FPGA uses a DMA to transfer data from the buffer to a TCP/IP socket.

Input Test Signal Generation

The block diagram for the test setup is illustrated in Fig. 3.33. Fig. 3.34 displays the printed circuit board (PCB) designed to facilitate chip measurement. The PCB was placed in an aluminum Faraday's cage to avoid unwanted interference. On this PCB, I modeled the nanopore sensor using a $1\text{ G}\Omega$ resistor and a 5 pF capacitor to simulate its electrical characteristics. By varying the voltage across the resistor an input current can be generated. For example, applying a 100 mV voltage across the $1\text{ G}\Omega$ resistor a 100 pA input current can be produced. This voltage can be generated using a benchtop voltage source or digital resistors. Digital resistors were chosen over a traditional benchtop voltage source because they produce less noise and allow for independent control of each channel. These digital resistors, which function as voltage dividers, were used in conjunction with $1\text{ G}\Omega$ resistors to generate test signals.

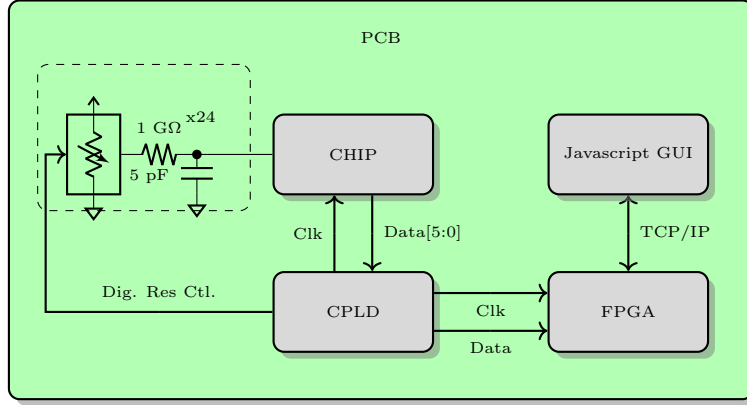


Figure 3.33: TIA test setup block diagram.

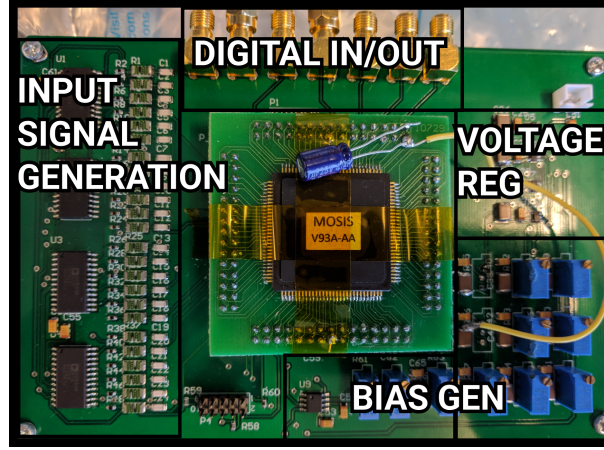


Figure 3.34: PCB testbench for DROICv1

3.7.1 AFE Measurement Results

Fig. 3.35 shows examples of the transient output of the integrator, LPF, and CDS for a DC input current (10 pA). The integration time for this measurement was set to 61 μ s. The reset period of the integrator and filter were 6 μ s while for the CDS it was 15 μ s.

3.7.1.1 Transient Results

For more detail, Fig. 3.36 shows three more examples of transient outputs of the integrator. The plots shown correspond to three different gain settings for this component. As the gain increases, the change in output increases for the same input current (again, 10 pA as above). This increasing gain is evident in the increasing

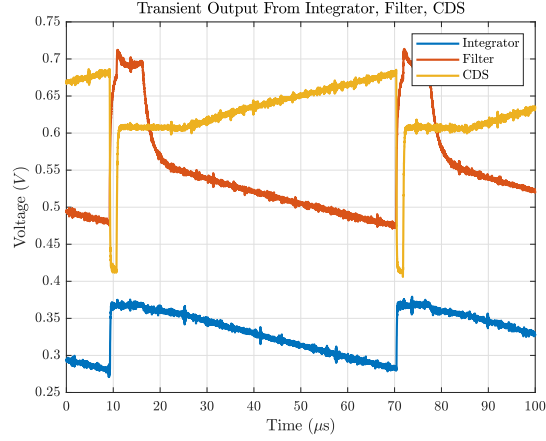


Figure 3.35: Transient output of integrator, LPF and CDS for a 10 pA DC input current.

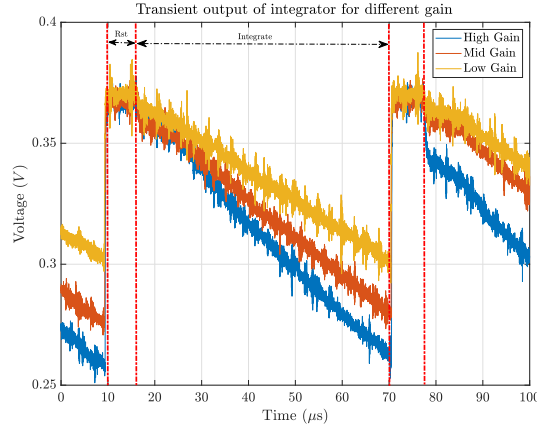


Figure 3.36: Transient output of the integrator at different gain settings for a 10 pA DC input current to the AFE.

slopes of the ramps in Fig. 3.36. The effect of kT/C noise is visible in the blue plot where the integration plot changes after the reset period.

Similarly, Fig. 3.37 shows the transient output of the CDS for various gain settings. The input was also set to 10 pA DC for this measurement. The CDS removes the effect of the reset noise, charge injection observed after reset as can be observed in Fig. 3.35 around 78 μ s.

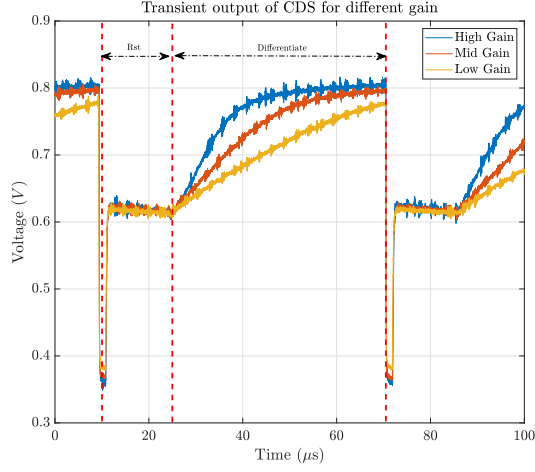


Figure 3.37: Transient output of CDS at different gain settings for a 10 pA DC input current to the AFE.

3.7.2 ADC Measurement Results

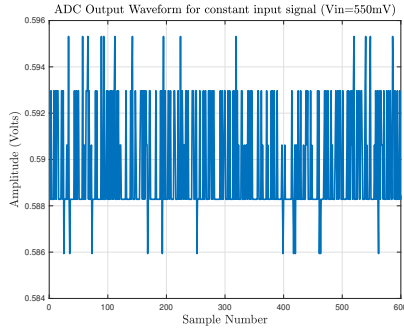
3.7.2.1 DC Test

During measurement I observed random noise in the digital output of the ADC, so a DC input voltage was applied to the ADC to capture the transient output and obtain the spectrum of the ADC.

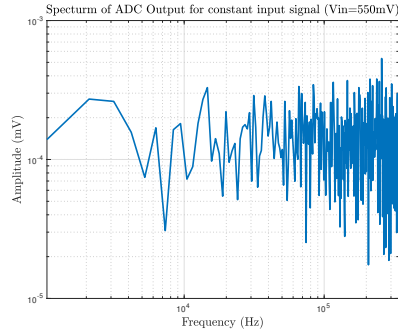
From Fig. 3.38a, it is observed that the output of the ADC varies eight levels for constant input (9.4 mV). This translates to 3 bits. The spectrum of this signal is shown in Fig. 3.38b. The noise seems to be random as the spectrum looks flat. The full-scale range of the ADC in this setup is 1.2 V ($V_{high} = 1.2$ V and $V_{low} = 0$ V).

3.7.2.2 ADC Dynamic Performance Measurement

This section provides the dynamic performance measurement of the ADC. To get the most pessimistic dynamic performance, the spectrum was measured with input signal near the Nyquist frequency. To reduce the effect of the measurement on the results, I have used synchronous, non-coherent sampling. Synchronous sampling means that an even number of periods of the input signal and clock will be used. This reduces



(a)



(b)

Figure 3.38: a) Transient output for constant input voltage (550 mV). b) Spectrum of ADC output for constant input voltage (550 mV).

Amplitude	SINAD	SNR
100mV	21.96 dB	24.14 dB
200mV	27.73 dB	28.96 dB
300mV	31.18 dB	32.18 dB
400mV	31.97 dB	33.75 dB
500mV	34.99 dB	35.19 dB
520mV	35.41 dB	35.65 dB
530mV	35.43 dB	35.86 dB
550mV	35.19 dB	36.02 dB
570mV	34.86 dB	36.05 dB
600mV	33.65 dB	36.05 dB
700mV	29.61 dB	37.24 dB
750mV	27.54 dB	37.83 dB
800mV	27.29 dB	38.28 dB
850mV	25.22 dB	37.02 dB

Table 3.4: SNR & SINAD for various amplitude input voltage.

spectral leakage in the spectral estimation. Non-coherent sampling means that the input frequency and the clock frequency are not harmonically related. If the input and clock frequencies are harmonically related, the quantization noise of the data converter will be in tones that are harmonically related to the clock frequency. As a result, the simulated SINAD estimate will be correct but the distortion will be over-estimated, and the noise will be under-estimated. Typically, the input frequency is chosen to be proportional to a prime number to assure that the input frequency and the clock frequency are not harmonically related.

Table 3.4 shows the SNR and SINAD for the amplitude sweep of the signal.

Fig. 3.39 shows the ADC output for synchronous, non-coherent input signal. The

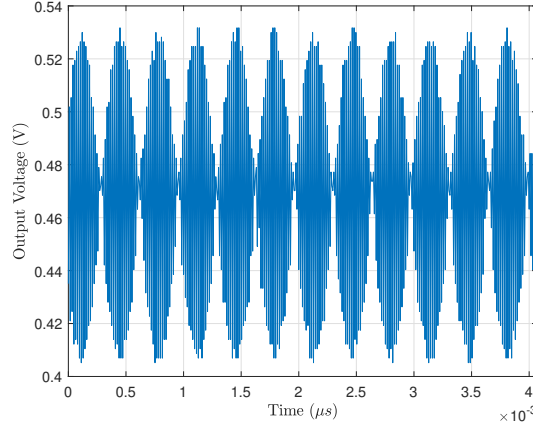


Figure 3.39: ADC output voltage for $(1999/4096) \cdot 125$ kHz sine input sampled synchronously.

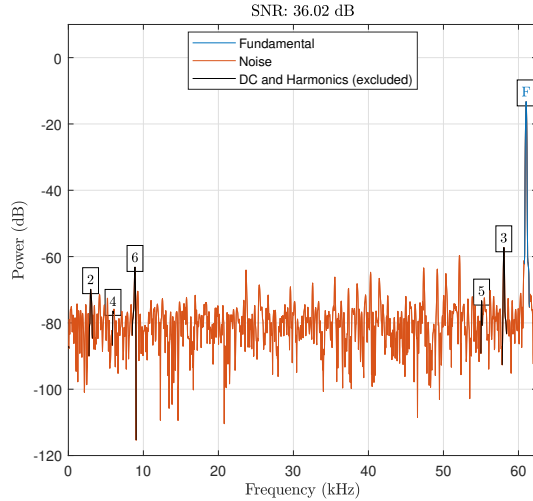


Figure 3.40: SNR for ADC at 550 mV pk-pk $(1999/4096) \cdot 125$ kHz sine input near the Nyquist frequency.

ADC was operated at 125 KSps.

Fig. 3.40 and Fig. 3.41 shows the SNR and SINAD respectively.

3.7.3 Complete Chain Digitized Result

3.7.3.1 Noise Measurement Result

The noise measurements for various integrator gain settings are shown in Table 3.5. The measurements were done in open-input configuration, i.e. the amplifier is disconnected from the ESD and pad. This was done because ESD leakage, PCB surface

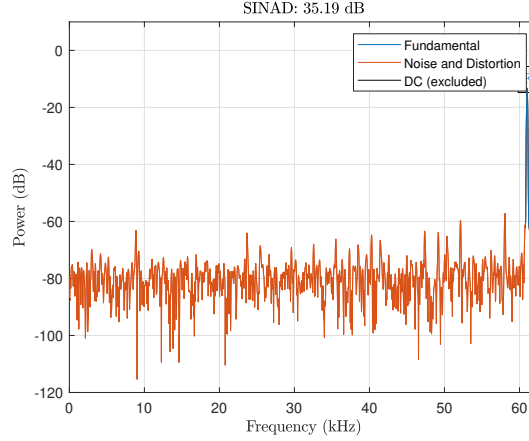


Figure 3.41: SINAD for ADC at 550 mV pk-pk $(1999/4096) \cdot 125$ kHz sine input near the Nyquist frequency.

contaminants, PCB surface charge, and substrate can induce leakage current and add significant noise [116]. In an integrated sensor and CMOS setup such issues are not observed as the ESD and PCB are not present.

The lowest noise can be obtained from the '100' setting for integrator as it uses the smallest feedback capacitor, but it wouldn't satisfy the amplitude requirement input signal. The optimal gain setting of integrator is '010' as this maximizes the gain without clipping the signal, even though setting '100' provides the maximum gain. The LPF bandwidth for measurement was set to 13.95 kHz. The least noise observed in this bandwidth is $1 \text{ pA}_{\text{rms}}$.

The input capacitance of an open input amplifier is about 1 pF. ONT Minion system have an input capacitance of 2 pF. To do a calculation of the throughput density, I have scaled the noise by a factor of two to $2 \text{ pA}_{\text{rms}}$ because of the larger input capacitance. This would imply the input referred noise density would be $23.9 \text{ fA}/\sqrt{\text{Hz}}$. To obtain an SNR of 20 dB with input referred noise density of $23.9 \text{ fA}/\sqrt{\text{Hz}}$ the sampling rate should be 7.87 kSps ($\text{BW} = (1.5 \text{ pA}/23.9 \text{ fA}/\sqrt{\text{Hz}})^2$).

ONT's system operates at 4 kHz while consuming 2 mW/channel. As mentioned in Section 1.3.1, throughput density is the speed of DNA translocation per sq. mm of chip at a given SNR. It has a throughput density of 1700 bp/s/mm^2 .

Table 3.5: Gain and open-input input referred noise for various gain and filter settings

Gain Setting (binary)	Filter Setting (kHz)	Gain ($G\Omega$)	Inp. Ref. Noise ($pARms$)	Bandwidth (kHz)
110	90	6	1.49	13.95
	500	6	2.15	13.95
	90	6	1.4	13.95
	15	6	1.33	13.95
100	90	13	1.73	13.95
	500	13	1.94	13.95
	90	13	1.71	13.95
	15	13	1.5	13.95
010	90	8.5	1.29	13.95
	500	8.5	1.7	13.95
	90	8.5	1.27	13.95
	15	8.5	1	13.95

My AFE operates 7.87 kSps (787 bp/s) with an SNR of 20 dB. Each channel has area of 0.0704 mm^2 while consuming 0.34 mW/channel. The throughput density of AFE is 11.1 kbp/s/ mm^2 at 20 dB SNR. Hence, improving throughput density by approx. 6.5x, while consuming 5.8x lower power, compared to ONT's system.

3.7.4 Channel Interference

The transient output and spectrum of nine DROIC channels measured simultaneously are shown in Figs. 3.42 and 3.43 respectively.

It was also noted that two channels in the same row have a feedthrough signal which is about 1000 times smaller (60 dB suppression) than the signal in the active channel. This is due to capacitive coupling from wire routing for the input signal. The effect of this coupling is negligible on the performance of the amplifier. Nonetheless, If local pads are used, there will be no source of electrical coupling.

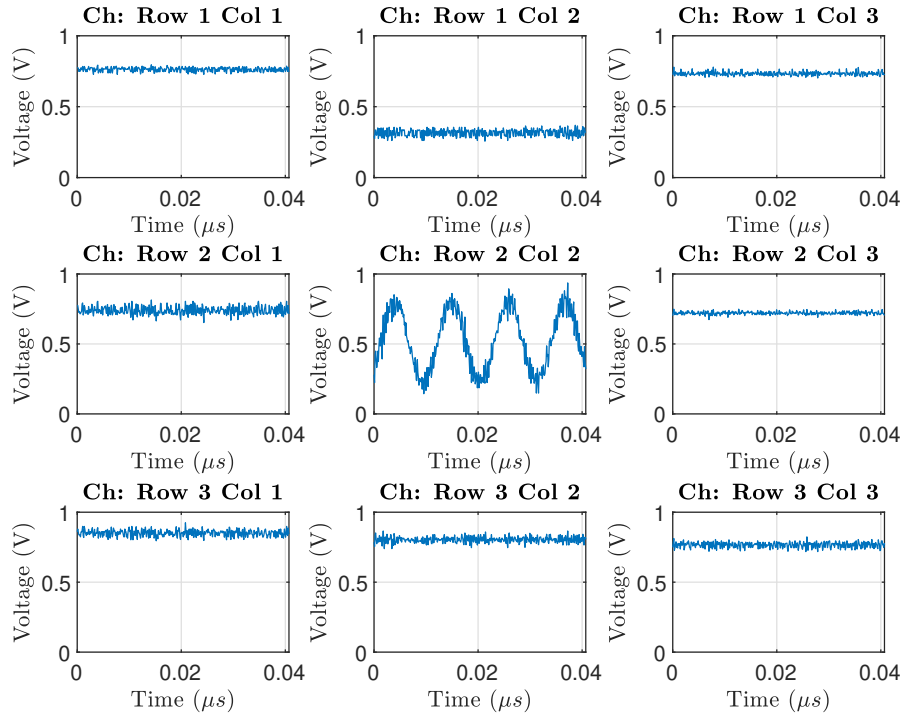


Figure 3.42: Transient output for multiple channels operating in parallel.

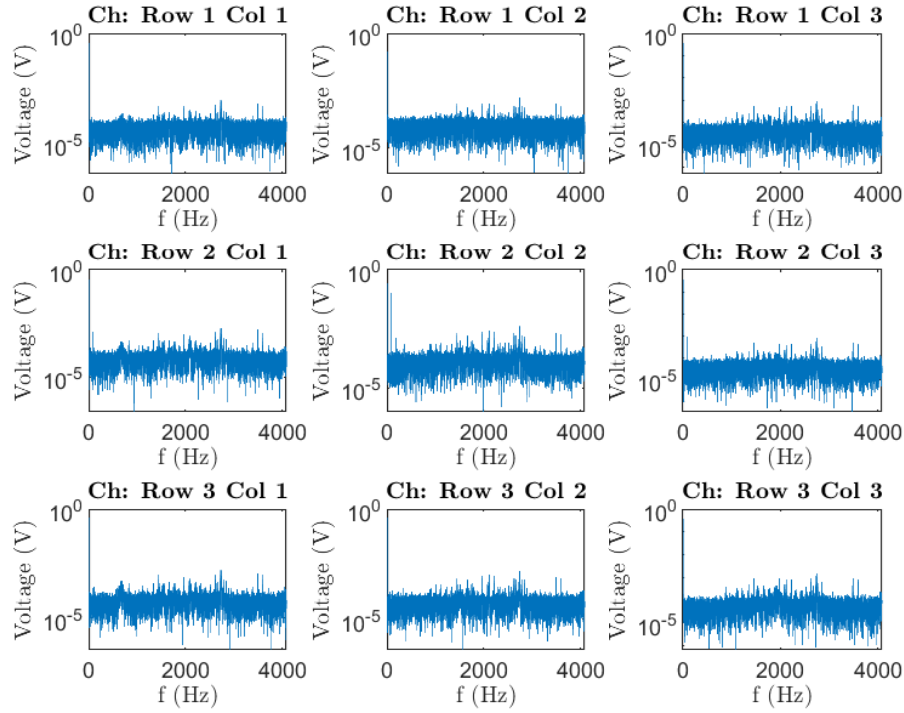


Figure 3.43: Spectrum of multiple channels operating in parallel.

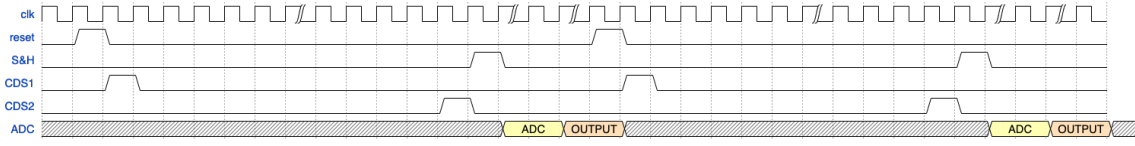


Figure 3.44: Timing diagram for serial ADC operation scheme.

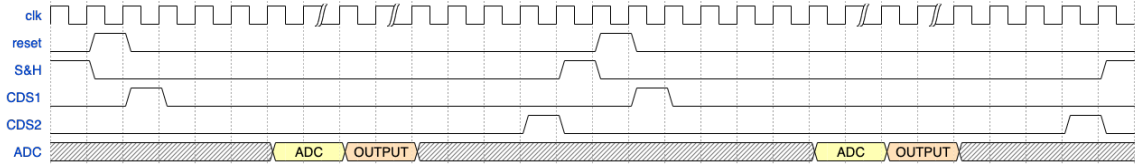


Figure 3.45: Timing diagram for parallel ADC operation scheme.

3.7.4.1 Performance with different ADC operation modes

The amplifier is sensitive to digital noise produced by the action of the ADC. To overcome this problem, this section discusses two ADC operation modes: serial mode and parallel mode. In serial operation mode, ADC conversion and data transfer is done right after the output is sampled. The amplifier is not operated while the ADC is performing the conversion. This leaves some dead-time when the amplifier is non-operational. In parallel mode, ADC conversion and data transfer are performed between CDS1 and CDS2.

The temporal responses to the sine wave input (100 pA) for parallel and serial operation modes are shown in Fig.3.46. The Parallel ADC operation causes a larger DC offset in the output signal. During the serial ADC operation the DC level (DC offset) was at 410 mV while for parallel operation DC level was at 700 mV. This is probably due to unwanted current injection during ADC operation but with proper circuitry it can be corrected easily. One such correction technique has been proposed in Section 4.6.5.

By operating the ADC in parallel, the dead time is reduced, and thus improves the performance of the system. But this comes with added distortion. Since the SNR of the system is so poor, the detectors should be able to handle such deterministic distortions.

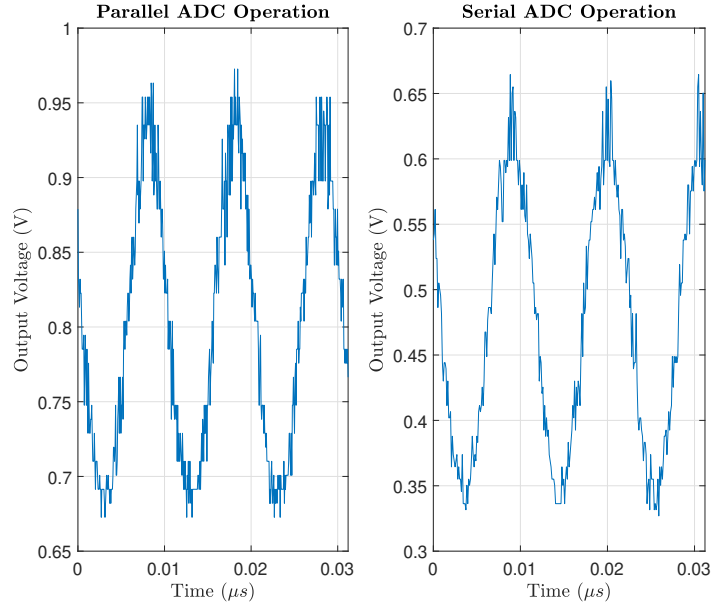


Figure 3.46: Temporal responses to sine wave input (100 pA) for parallel and serial operation modes.

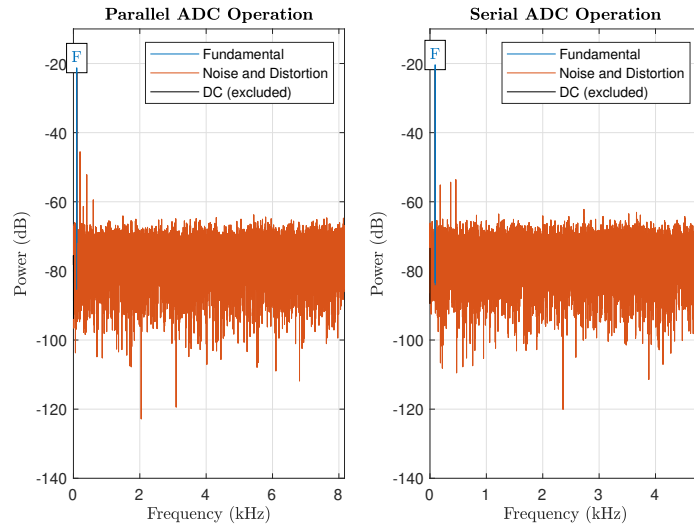


Figure 3.47: Spectra responses to sine wave input (100 pA) for parallel and serial operation modes.

Chapter 4

Digital Readout Integrated Circuit (DROIC) with Column ADCs

4.1 Chapter Summary

In this chapter, I explore the evolution of the Digital Readout Integrated Circuit (DROIC) architecture, highlighting key advancements from DROICv1 to DROICv2. To address these limitations, DROICv2 introduced a column ADC architecture, significantly enhancing throughput density. This design reduced the average area per channel and improved the system performance.

In addition to architectural improvements, this chapter delves into the amplifier design, ADC enhancements, and measurement setup and results. DROICv2 incorporated improved opamp design, noise reduction techniques, and digital calibration methods for robust performance. In particular, the introduction of a two-stage opamp and a custom metal-on-metal (MOM) capacitor in the ADC significantly improved gain, ENOB, and area efficiency. The SNDR of improved ADC before calibration is 41.47 dB while after digital calibration improves to 51.38 dB.

A new PCB was designed for DROICv2 to remotely configure the DROIC, change its bias voltage, and increase the range of input currents provided to DROIC. Further-

more, the chapter discusses the implementation of a Direct Memory Access (DMA) based readout system using a Xilinx FPGA, which ensures efficient data transfer and real-time readout capabilities essential for high-throughput applications.

The measurement results demonstrate significant improvements in ADC SNDR and overall system accuracy. The throughput density of DROICv2 is 14.5 kbp/s/mm², which gives approx. 8.5x improvement compared to ONT's system. The chapter concludes with a comprehensive analysis of the LMS-based digital calibration algorithm, which effectively corrects gain and offset errors, further enhancing the reliability and precision of the DROIC system.

4.2 Introduction

This chapter examines the progression of the Digital Readout Integrated Circuit (DROIC) architecture, focusing on the advancements made from DROICv1 to DROICv2. To overcome the limitations of its predecessor, DROICv2 implemented a column ADC architecture, which substantially increased throughput density. This innovation optimized the design by reducing the average area per channel and enhancing overall system performance. I present the system and circuit level improvements in the following sections.

4.3 System

The first version of DROIC, DROICv1 for brevity, implements an in-pixel ADC architecture. That is, each AFE has a dedicated ADC used to digitize the amplified signal. The area of each channel is 0.0704 mm² (0.32×0.22 mm²). It is split equally between the AFE (0.16×0.22 mm²) and the ADC (0.16×0.22 mm²).

As mentioned in § 1.3.1, throughput density is the speed of DNA translocation per sq. mm of chip at a given SNR. Building on the design experience of DROICv1, I

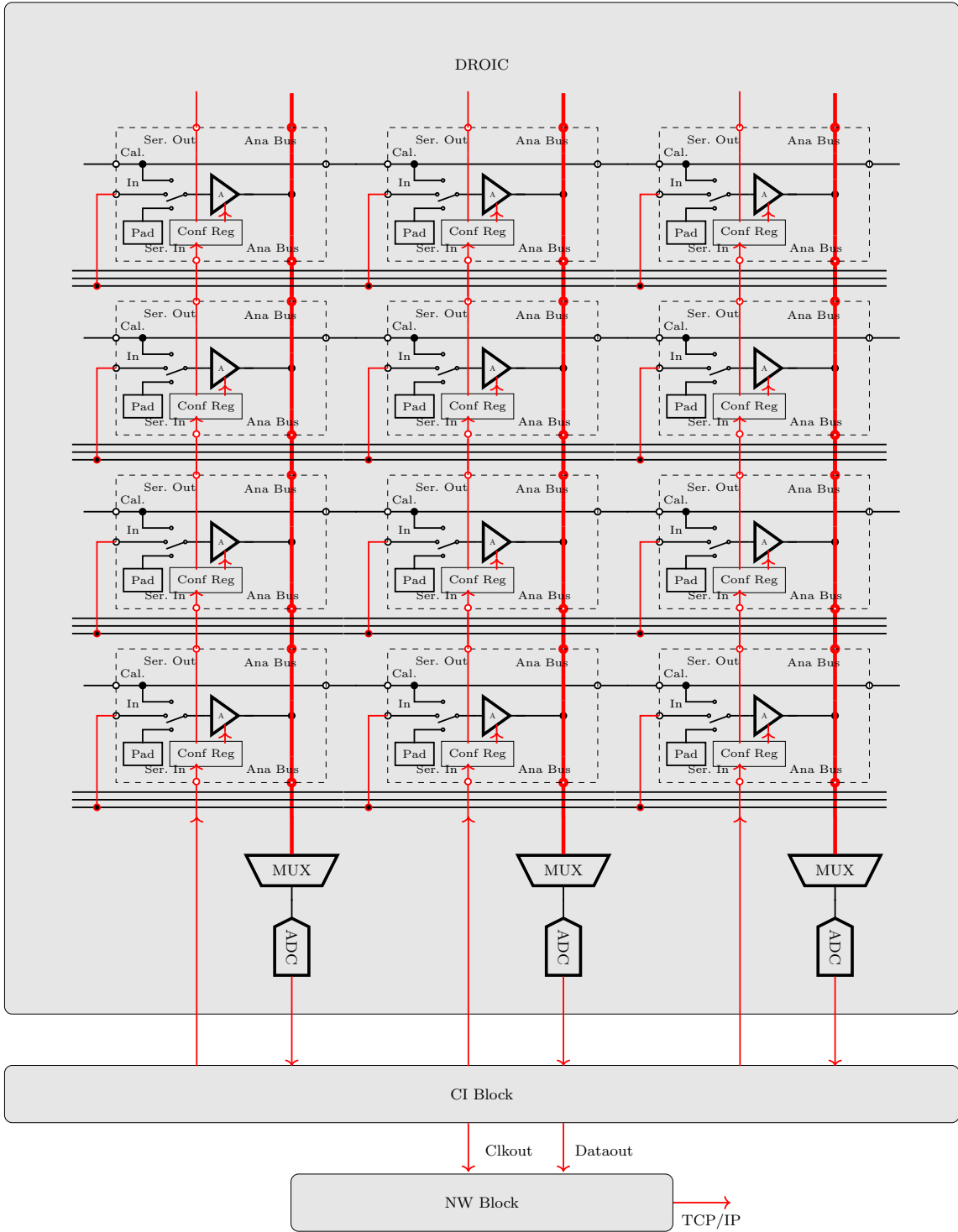


Figure 4.1: A simplified overview of a nanopore readout system based on column-ADC arrangements. Only four rows and three columns have been shown to keep the image simple.

attempted a more sophisticated for second version of the chip. For brevity, I will refer to this new design as DROICv2. To improve the throughput density of DROICv2, I

have implemented a new system architecture that employs column ADCs. DROICv2 shares an ADC between four channels that is connected to AFEs using an analog multiplexer. A simplified system overview showing three rows and three columns of DROICv2 is shown in Fig. 4.1. As shown in Fig. 4.1, each ADC is shared between four TIA pixel using an analog MUX. The ADC outputs the digitized signal using a 1-bit serial bus.

In DROICv2, a single AFE occupies 0.0399 mm^2 ($0.23 \times 0.19 \text{ mm}^2$) and the column ADC occupies 0.0418 mm^2 ($0.22 \times 0.19 \text{ mm}^2$). This reduces the average area of 4 channels to 0.0542 mm^2 , about a $1.3\times$ area efficiency. Hence, the throughput density of DROICv2 is 14.5 kbp/s/mm^2 ($787 \text{ bp/s/0.542 mm}^2$), which gives 10x improvement compared to ONT's system. The layout of the chip is shown in Fig.4.2. It contains 106 channels, divided into four quadrants. The ADCs were placed on the top and bottom sides for the column-based readout.

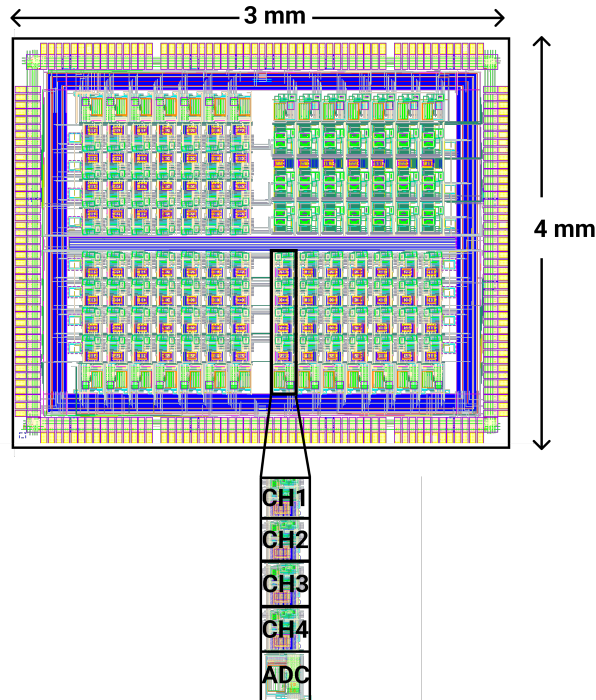


Figure 4.2: DROICv3 chip layout

The timing diagram for DROICv2 is shown in Fig. 4.3. DROICv2 works similar to DROICv1 in its amplification phase. The main difference is during the readout

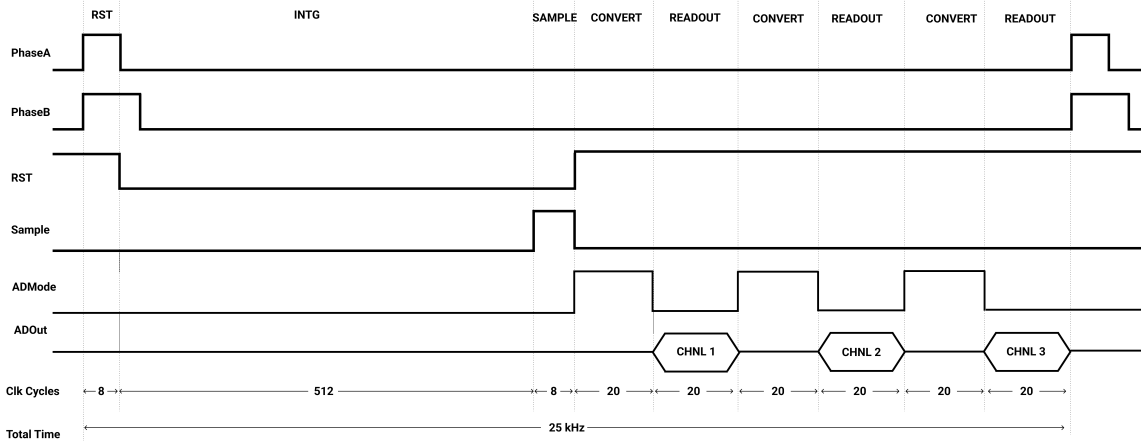


Figure 4.3: Timing diagram for the DROICv2 array readout.

phase. After the amplified signal is sampled by each AFE in its T&H, the analog signal is digitized and read out sequentially by the ADC before the next reset of the AFE. The operating frequency of the ADC has been increased upto 20 MSps in DROICv2 to reduce the time needed for sequential readout.

4.4 Amplifier

The front-end amplification design used in DROICv2 follows the same general topology as used in DROICv1. That is, an integration, filtering, correlated double sampling chain. To increase the sensing range from ~ 100 -pA to ~ 20 nA, a low gain setting was added in the integrator and CDS. This was achieved by adding a larger feedback capacitor to the integrator and a smaller capacitor to the CDS input.

The opamp used in DROICv1 used a folded cascoded amplifier. This amplifier provides high gain, but suffers from limited output voltage headroom. To address this issue, I have implemented a two-stage opamp topology. Two-stage opamps provide higher voltage headroom, and thus allow the integrator to produce a larger output.

The schematic of DROICv2's two-stage opamp is shown in Fig. 4.4. Similarly to the opamp in DROICv1, PMOS devices were used to form the input differential pair and

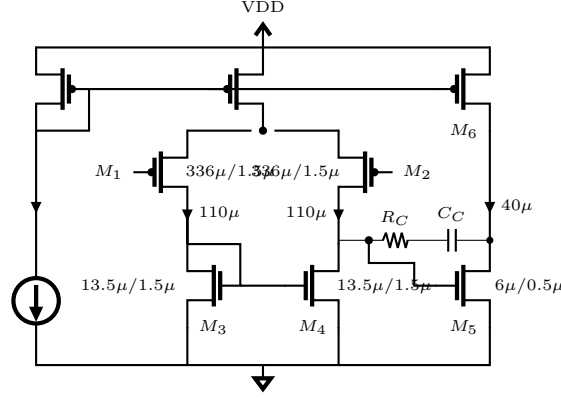


Figure 4.4: Miller-compensated two-stage opamp schematic.

large W/L aspect ratios were used to minimize flicker noise. The current in the input differential pair was increased to reduce the thermal noise floor of the opamp. The opamp consumes $280 \mu\text{A}$ of current compared to $105 \mu\text{A}$ in DROICv1. The DC gain of the opamp is about 70 dB while unity gain bandwidth is 56 MHz. The noise floor of the opamp is $4.2 \text{ nV}/\sqrt{\text{Hz}}$ and the flicker noise corner frequency is approximately 5 kHz.

4.5 ADC

As mentioned in the previous chapter, the ADC used in DROICv1 had two main performance limitations. The ADC suffered from low SNR due to layout parasitics of the split-attenuated DAC. The split-attenuated DAC array was used to minimize the area needed for the capacitor bank. In the ADC built for DROICv2, we employed a binary array which normally requires more area, but this was mitigated by minimizing the unit capacitor physical layout size. As a result, a significant reduction in the DAC's capacitor bank area was realized. The process design kit (PDK) for the 130-nm technology node does not provide a metal-on-metal (MOM) capacitor. The minimum sized metal-insulator-metal (MIM) capacitor available by technology PDK was 28 fF. They also consume much higher area. The technology PDK does not provide a MOM capacitor. Hence, a custom MOM capacitor was implemented using metal layer 6, as

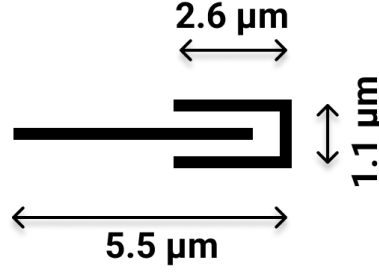


Figure 4.5: Metal-on-metal (MOM) unit capacitor physical arrangement.

shown in Fig. 4.5. The unit size of this capacitor is 0.5 fF.

The floorplan of the complete DAC is shown in Fig. 4.6. The unit caps have been abutted to create an array of MOM capacitors. These arrays are placed on the top and bottom, while the output of the capacitor is routed through the middle. This reduces any unwanted parasitic coupling to the output DAC, which can introduce gain and offset errors. The DAC occupies a $120 \times 75 \mu\text{m}^2$ (0.009 mm^2) area.

The second limitation of the ADC used in DROICv1 was the random noise in three least-significant bits (LSB) of its output. From rigorous simulations, it was discovered that the noise of the latched comparator handling the ADC's capacitive bank signal was much higher than the LSB of the ADC. Moreover, the latched comparator also cause kickback noise and hence distortion in the ADC conversion. To fix the issue of comparator noise and kickback, the DROICv2 ADC uses a differential amplifier as the first stage of the latched comparator. The block diagram of the SAR ADC is shown in Fig. 4.7.

To further improve the performance of the new ADC, I have also implemented a digital correction algorithm. The LMS based digital correction improves performance by adapting the weight of the bits. Details of the algorithm are explained in following section.

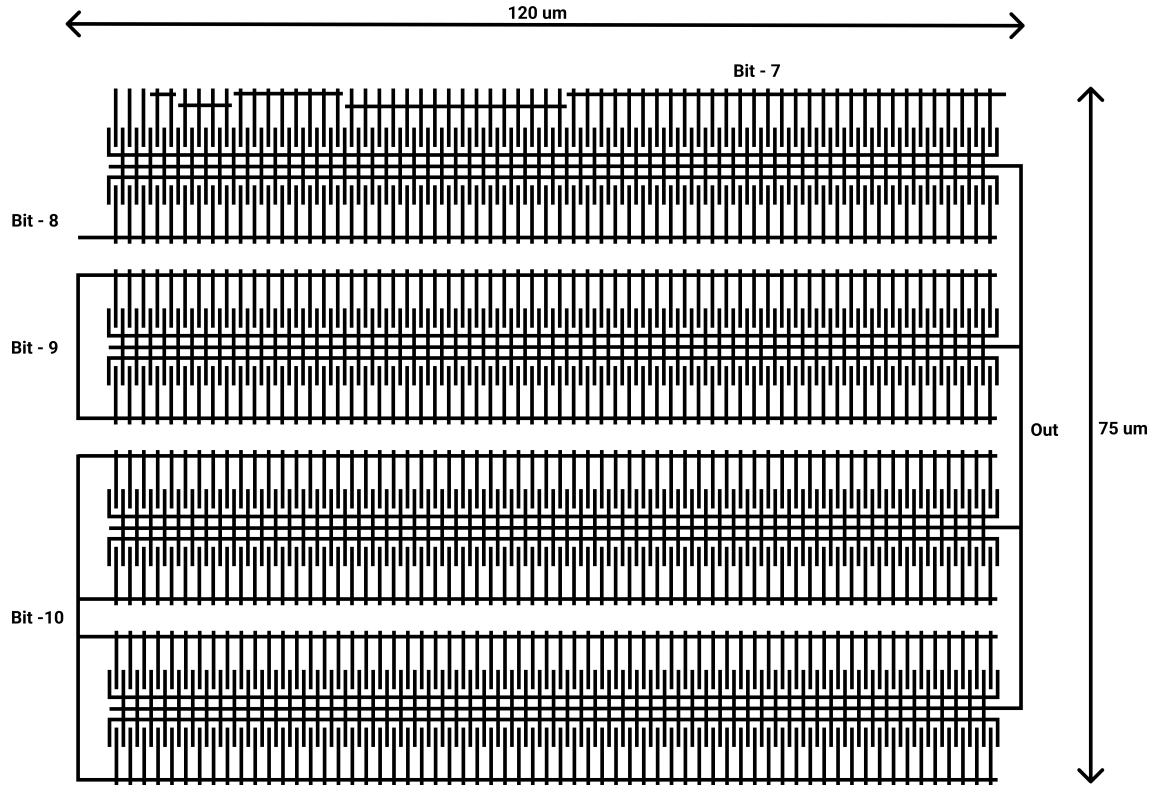


Figure 4.6: DAC capacitor bank layout.

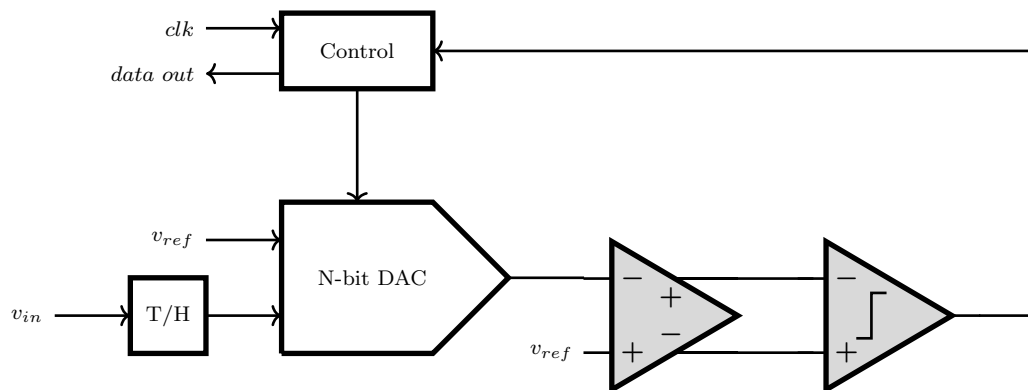


Figure 4.7: SAR ADC block diagram with added pre-amplifier

4.5.1 LMS-Based Digital Calibration

Generally, SAR-ADC designs suffer from gain error due to layout parasitics and random mismatch. Furthermore, the ADC performance is also degraded by offset error from the latched comparator. This leads to incorrect bit conversions at the ADC output. Instead of leaning entirely on analog circuit methods to deal with this problem, post-processing methods are also an option.

To consider the use of such approaches, consider the following formalization of a typical Nyquist-rate N -bit ADC output

$$y[k] = \sum_{n=0}^{N-1} A_n[k] \cdot \alpha_n \quad (4.1)$$

where $A_n(k)$ represents binary output $n \in \{0, \dots, N-1\}$ from the ADC for sample k , α_n represents the corresponding weight coefficients of each bit and $y[k]$ is the equivalent converted sampled analog output. For an ideal ADC, $\alpha_n = 2^n$ where n varies from 0 to $N-1$.

The errors in binary outputs, A_n , can be corrected by adjusting the values of coefficient α_n with some adaptive algorithm such as LMS algorithm.

4.5.1.1 LMS Algorithm

The LMS algorithm gained prominence with the work of Bernard Widrow and Marcian Hoff in 1960 [117–119]. They introduced the concept of adaptive filtering using the LMS algorithm in the context of developing adaptive filters for communication systems. Since then, LMS has been used for various applications, including ADC digital correction [120, 121].

LMS Algorithm Steps

1. Initialization:

- Initialize the filter coefficients $w_0, w_1, \dots, w_{N-1}$ to some initial values, often

set to zero or small random values.

- Choose a learning rate μ (small positive constant).

2. Adaptation Loop:

- For each new sample at time index k , perform the following steps:
 - **Input Signal:** Let $x[k]$ be the input signal at time k .
 - **Filter Output:** Compute the output of the filter $y[k]$ using the current coefficients: $y[k] = \sum_{i=0}^{N-1} w_i[k] \cdot x_i[k]$.
 - **Error Calculation:** Calculate the error signal $e[k]$ as the difference between the desired signal $d[k]$ and the filter output: $e[k] = d[k] - y[k]$.
 - **Coefficient Update:** Update the filter coefficients using the LMS update rule:

$$w_i[k+1] = w_i[k] + \mu \cdot e[k] \cdot x_i[k]$$

for $i = 0, 1, \dots, N-1$.

3. Convergence:

- The adaptation process continues for a specified number of iterations or until the filter coefficients converge to values that minimize the mean squared error.

The LMS update rule for each filter coefficient is given by:

$$w_i[k+1] = w_i[k] + \mu \cdot e[k] \cdot x_i[k]$$

where:

- $w_i[k]$ is the i -th coefficient at iteration k .
- μ is the learning rate or step size.
- $e[k]$ is the error signal at time k .
- $x_i[k]$ is the i -th input signal at time k .

The learning rate μ determines the step size of the coefficient updates. It needs to be carefully chosen to balance the speed and stability of convergence. LMS is

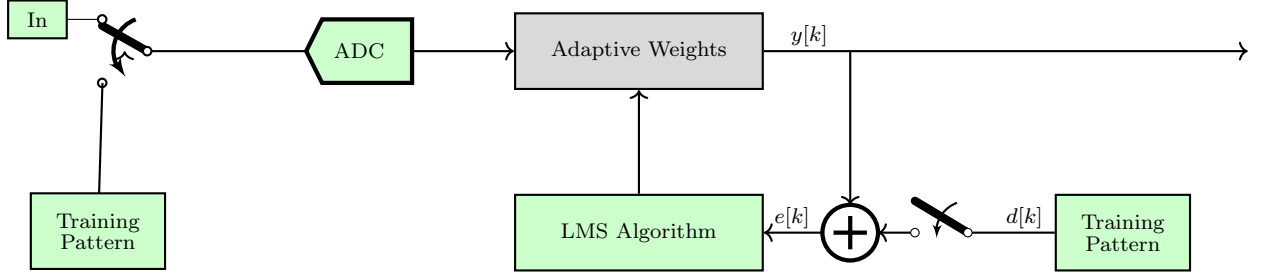


Figure 4.8: Block diagram with LMS based ADC calibration.

computationally simple and requires relatively low memory, making it suitable for real-time applications in low-power portable systems. The block diagram of the system used for the adaption algorithm is shown in Fig. 4.8.

However, an ADC as described by (4.1) provides only N coefficients for adaptation and is not very effective in removing static nonlinearities [122]. To endow the adaptive algorithm with more degrees of freedom, the output $y[k]$ in (4.1) can be represented with thermometer weighted codes

$$y[k] = \sum_{i=0}^{2^N-1} B_i[k] \cdot \beta_i \quad (4.2)$$

where $B_i[k]$ refers to the digital thermometer code representation of the ADC output at time k and β_i represents the weight coefficient assigned to each bit i in the digital thermometer code. The weight coefficients reflect the importance of each bit in contributing to the overall value.

The weights β_i can be adapted using a known reference available that serves as a training pattern for an LMS algorithm. It has been shown in [122] that thermometer-based calibration is more effective compared to binary weighed calibration. For ADC calibration in DROICv2, I have used 1023 thermometer-based weight to maximize performance.

4.6 Measurement Setup & Results

4.6.1 PCB Testboard

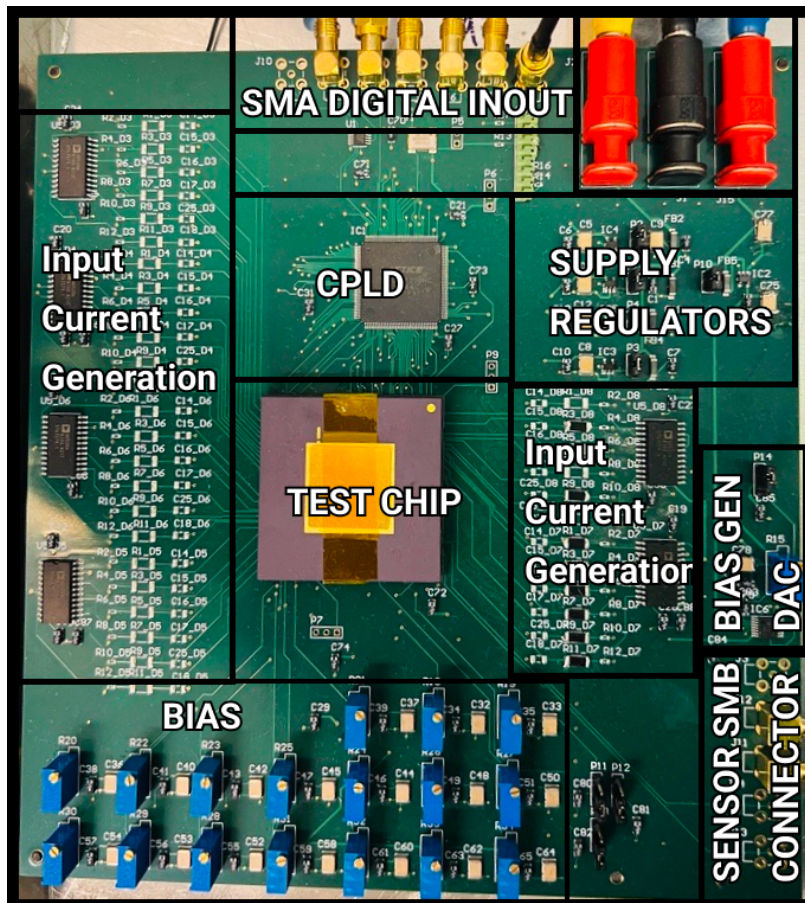


Figure 4.9: PCB testboard for DROICv2

For the DROICv2 design, the PCB testboard was further refined from version used to test DROICv1. The PCB testboard has been shown in Fig. 4.9. It shows the location of various components such as bias generators, test input generator, sensor connectors, etc. The DROICv1 testboard had 1.2 V and 3.3 V regulators and also contained a digital resistor connected to a gigohm resistor to produce picoampere test currents. The positive reference of the digital resistor was connected 1.2 V while the negative reference was connected to the ground. This range of voltages allowed for the limited generation of negative input currents, but, it turns out, not enough for thorough testing and system evaluation.

Thus, for the DROICv2 tests, I have added a -3.3 V regulator along with a potentiometer which is used to generate negative reference voltages for the digital resistor. This allows for up to 3 nA of negative current to be supplied to the amplifier (with $1\text{G}\Omega$ resistor on PCB). This can allow for a higher dynamic range in offset cancellation, which is discussed below.

Another improvement to the PCB testboard was the Lattice CPLD MachXO2. The DROICv1 testboard used an Intel CPLD. This CPLD only supports a 5 MHz on-chip clock which isn't sufficient for high-speed readout. The Lattice MachXO2 CPLD has a on-chip oscillator that can go up to 133 MHz. The MachXO2 Lattice CPLD also has a higher number of logic cells compared to the Intel CPLD used in DROICv1 (1280 vs. 240 LUTs). The CPLD transmits the data to a computer via a custom

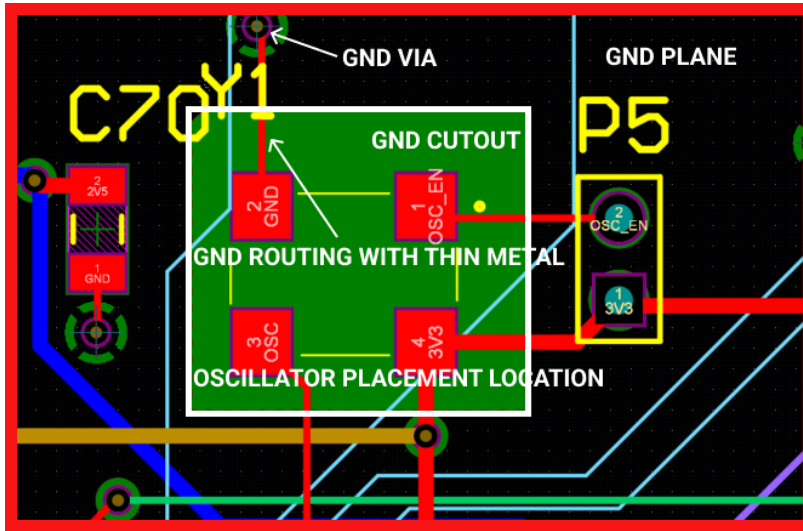


Figure 4.10: PCB ground plane cutout as a RF choke to minimize noise from oscillator

two-wire interface discussed in § 3.7. To configure the ROIC via CPLD remotely, an interface from a PC to the CPLD was needed. For this purpose, I have added a UART connection from the computer to the CPLD using a USB-to-UART TTL cable. This interface can be used to set the DROICv2's configuration registers for programming the gain & reset period setting, set the voltage of digital resistors on the PCB and set the bias voltage of that AFE using DACs. The opcodes for each command along with the command sizes are shown in Table. 4.1. The 'Program Onchip Register' Function

Table 4.1: Opcode for controlling the functions on board via the GUI using UART

Function	Opcode	Command
Program Onchip Register	0x0001	7 Byte (1 Byte Column Address & 6 Byte Data)
Set Onboard Bias Voltage	0x0002	3 Byte (1 Byte Channel Ad. & 2 Byte Data)
Set Offset Current	0x0003	4 Byte
Set Sampling Rate	0x0004	1 Byte

is used for various functions such as selecting input source, setting the gain, adjusting filter bandwidth, adjusting the bias currents. The 'Set Onboard Bias Voltage' function is used to set the bias voltages for amplifiers using the 16 bit high resolution DAC on the PCB. The 'Set Offset Current' function is used to set the current to the amplifier using a digital resistor. And finally 'Set Sampling Rate' function is used to set the sampling rate of the amplifier.

A 50 MHz crystal oscillator was integrated onto the PCB testboard to serve as an external clock source for the CPLD. To mitigate power supply noise in the input signals, which can be introduced by the oscillator's high-amplitude signal, an inductive choke was implemented in the ground and supply connections of the oscillator. This was achieved by creating a cutout in the ground plane directly beneath the oscillator and routing the ground and supply lines using narrow traces. Fig.4.10 shows the ground plane cutout (in green highlighted by the white box). The ground connection is routed with a thin metal-to-ground plane shown with red color. I have also placed cutout under the amplifier inputs to reduce coupling from ground plane noise to the input of the amplifier. The green region in Fig.4.11 shows the PCB plane cutout while the amplifier routing are shown in red.

I also added a 4-channel 16-bit DAC (Analog Devices AD5678) on the DROICv2 testboard. This DAC is used to generate a bias voltage for the opamps and a reset voltage for the filter in DROIC. It can be controlled using the GUI via the UART connection from PC to CPLD. This allows for remotely setting bias voltage, canceling offset currents, adjust amplifier gain and sampling rate while performing experiments with ease.

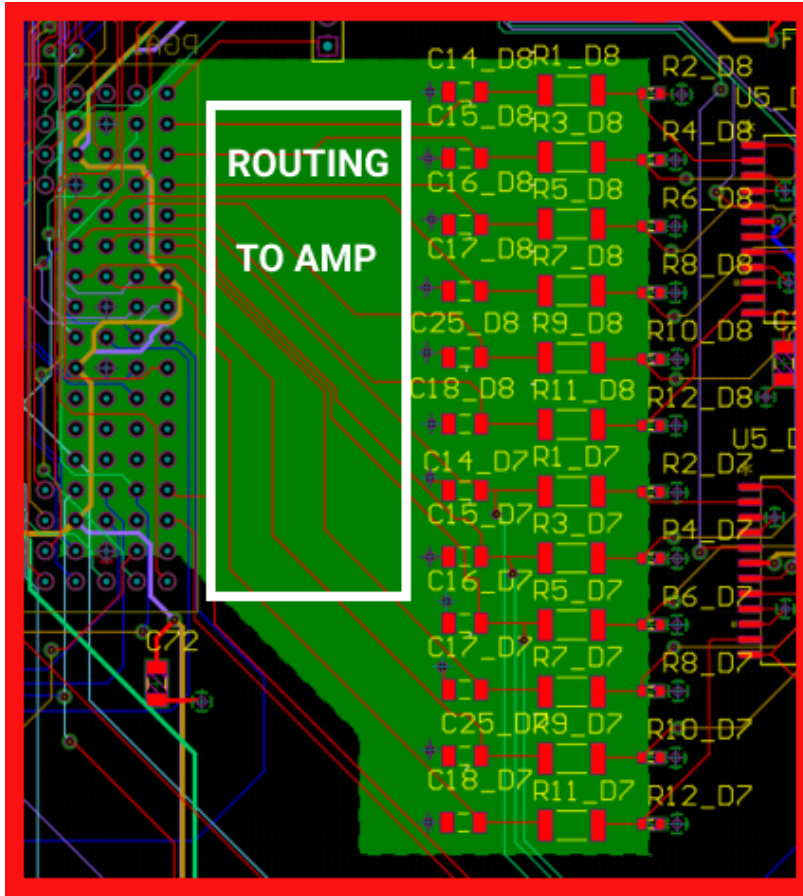


Figure 4.11: PCB ground plane cutout under amplifier inputs to reduce effect of ground fluctuations

4.6.2 FPGA Readout System

In ion-channel experiments, the initial step involves creating a lipid bilayer. The quality of the bilayer is inferred from the electrical signal measured in real-time. Hence, the need for a real-time readout system and GUI to help user's monitor DROIC's output arises for these experiments.

Additionally, data must be written to a file on the computer's hard drive. However, managing data from hundreds of channels, including deserialization and streaming to the computer running the GUI, poses a challenge. Simple readout interfaces like SPI, UART, or I2C lack the necessary bandwidth. Consequently, a system was implemented using an Xilinx FPGA, which deserializes the data and forwards it to the GUI over Ethernet.

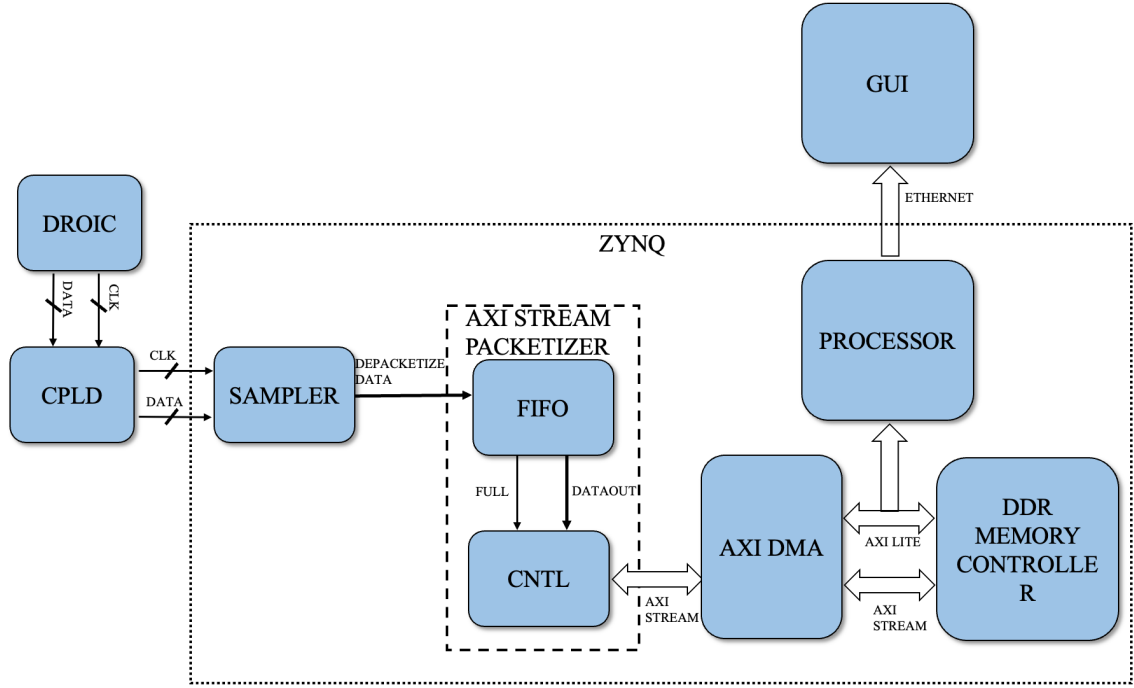


Figure 4.12: Block diagram of DROICv2 FPGA readout system

One potential approach to implementing a deserializer in the FPGA is to construct a simple AXI-based memory-mapped readout, as shown in § 3.7. However, this method is inadequate for providing real-time readout for a large number of channels (100+ channels), as each memory-based transaction in burst mode can only transfer 32 bits with a maximum burst of 8 packets per AXI transfer. This necessitates AXI headers for every 8 ADC readouts (assuming one ADC readout per register), introducing significant overhead and limiting the maximum achievable throughput.

For efficient data transfer within the FPGA without CPU involvement, a Direct Memory Access (DMA) based streaming readout in the Xilinx FPGA becomes crucial. A DMA controller is a dedicated hardware block responsible for managing data transfers between different memory locations within the FPGA without CPU intervention. This is particularly beneficial for high-throughput data streaming applications, such as the ion-channel experiments noted above. The implementation of a DMA-based readout system is depicted in Fig. 4.12.

To minimize digital noise in DROIC, a proprietary two-wire interface between

CPLD and Xilinx FPGA was established shown in § 3.7. One connection provides the clock, and the other provides the data. The clock and data are not switching when the DROIC is in the process of analog amplification. The *sampler* block on the Xilinx FPGA was developed to synchronize and deserialize the data from the CPLD, producing a 10-bit parallel data packet together with a valid signal.

The output of the *sampler* is directed into an *AXI stream packetizer* block. This block, equipped with a FIFO for data storage and a control block for generating signals required by the AXI DMA Streaming interface, facilitates continuous data flow between different FPGA blocks.

In Xilinx FPGAs, the DMA controller is part of the programmable logic, and Xilinx provides IP (Intellectual Property) cores for this purpose. The DMA controller is configured with details such as the source and destination addresses, data width, burst size, and other parameters by the on-FPGA processor using a C program implemented by me. Once the DMA controller is configured, the processor monitors for an interrupt. Once the data is copied to Double Data Rate Synchronous Dynamic Random-Access Memory(DDR) by the DMA controller, an interrupt is triggered in the processor which provides the address of data.

The FPGA processor also runs a TCP/IP client socket that connects to the TCP/IP server running on the PC where the GUI is hosted. The FPGA processor then moves the data via DMA transfer to GUI using a TCP/IP socket.

4.6.3 System Measurement Results

Noise Measurement Results

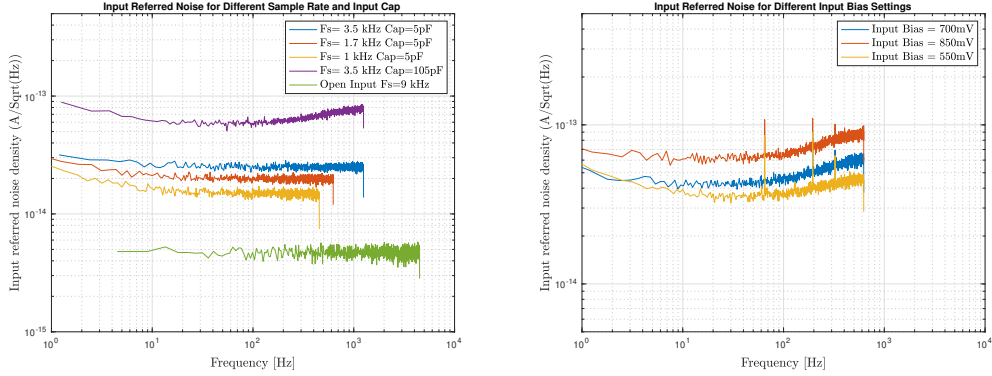
Biological Nanopore Rates: The noise measurements were conducted on the complete system by applying a constant voltage to the amplifier and capturing the digitized output noise from the ADC. The DC transimpedance gain of the amplifier was measured by applying a 100 pA square wave input and observing the output volt-

age of the amplifier. The input-referred noise spectrum is calculated as the ratio of the output noise spectrum of the digitized noise to the DC transimpedance gain of the amplifier. Fig. 8.1a depicts the measured input-referred noise current for the DROICv2 front-end for different sampling rates and input capacitances. At a sampling rate of 1 kSps with a 5 pF input capacitance, the front-end exhibits a noise floor of $15 \text{ fA}/\sqrt{\text{Hz}}$. As shown in Eq. 3.13, the noise floor increases with the sampling rate, attributed to the inverse proportionality of the gain to the sampling rate.

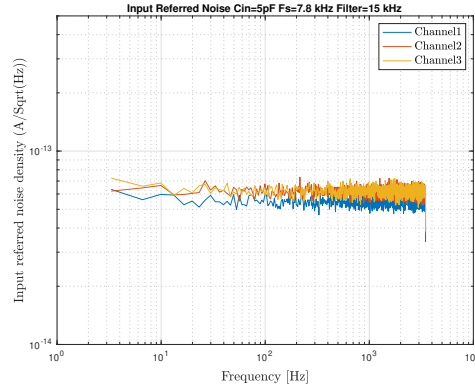
When the sampling rate is 3.5 kSps and the input capacitance is 105 pF, the noise floor increases to $60 \text{ fA}/\sqrt{\text{Hz}}$ due to noise amplification from the input capacitor. At a sampling rate of 9 kHz, the open input noise floor remains as low as $5 \text{ fA}/\sqrt{\text{Hz}}$. The presence of external PCB routes, ESD circuits and input capacitance for non-open-input measurement cases leads to a substantial increase in the noise floor. In an integrated DNA measurement setup, the nanopore sensor is placed directly on top of the chip, eliminating the need for PCB traces, ESD circuits and significantly reducing the input capacitance. The noise performance of such a setup is expected to be similar to that of an open input amplifier.

Fig. 8.1b illustrates the effect of op-amp bias on input-referred noise. An input bias of 550 mV exhibits the lowest noise. This is because a lower input bias provides a higher gate-source voltage to the device M_1 & M_2 in Fig. 4.4, consequently affecting the transconductance of the MOSFET and reducing noise.

Solid-state Nanopore Rates: To verify the electrical functionality of AFE for solid-state nanopore, nanoampere level currents were applied and the sampling frequency was increased. Fig. 4.14c displays the input-referred noise for an amplifier connected to a 5 pF input capacitance and a $100 \text{ M}\Omega$ resistance while sampling at 72.4 kSps. The noise floor at 72.4 kSps is approximately $0.6 \text{ pA}/\sqrt{\text{Hz}}$. Higher sampling rates are suitable for solid-state nanopores, which have a higher current output and can therefore accommodate more noise. The rms noise at 72.4 kSps is 120 pArms, as shown in Fig. 4.14a. The output of a 10 nA square-wave current



(a) Input referred noise for various sampling rate and input capacitance combinations. (b) Input referred noise for various input bias settings with a 105 pF input capacitance.



(c) Input referred noise for 7.8 kSps with 5-pF input capacitance at different channels.

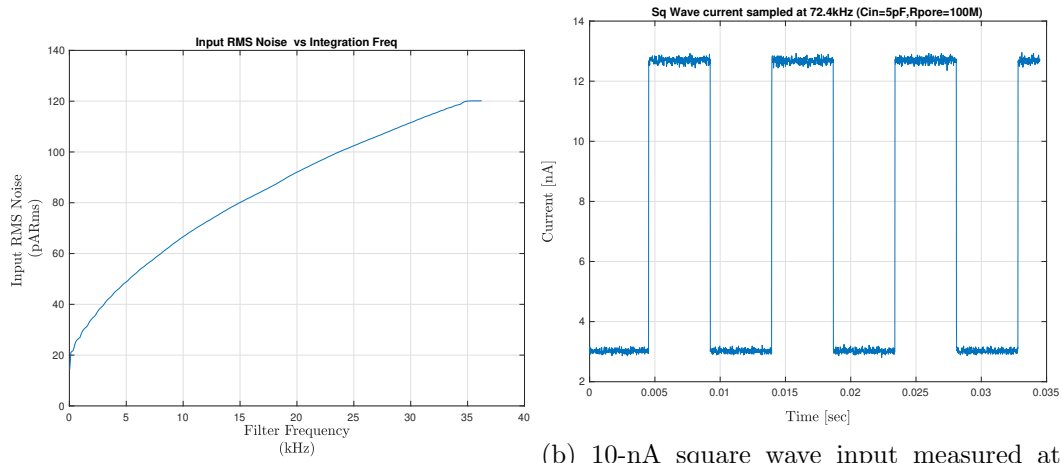
Figure 4.13: Input referred noise at various front-end settings.

sampled at 72.4 kSps is depicted in Fig. 4.14b.

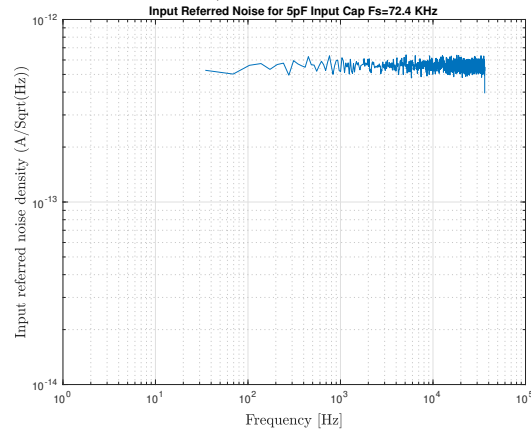
4.6.4 Digital Calibration of the ADC

The raw performance of the ADC (i.e., with no attempt at adaptive correction) for a 500-Hz signal is shown in Fig. 4.15. Even with the custom capacitor bank, the ADC SNDR is only 41.47 dB which comes up to ENOB of 6.59 bits. Hence, digital correction was applied to recover more performance.

To train the adaption weights, an 10 Hz sine was applied to the ADC and the digitized output was captured. The 10-bit binary digital code was converted to a 1024-bit thermometer digital code. Using MATLAB, the LMS training was performed to adapt the 1024 thermometer weights ($w[k]$). Fig. 4.16 shows the calibrated ADC



(a) Input referred RMS noise with-respect-to 72.4 kSps to bandwidth ($C_{in} = 5 \text{ pF}$, $F_s = 72.4 \text{ kHz}$).
 (b) 10-nA square wave input measured at



(c) Input referred noise for 72.4 kSps with 5-pF input capacitance

Figure 4.14: Input referred noise, integrated noise and transient output for solid state nanopores

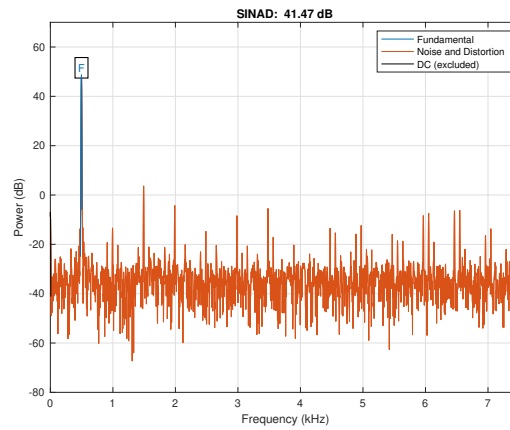


Figure 4.15: SNDR plot before calibration.

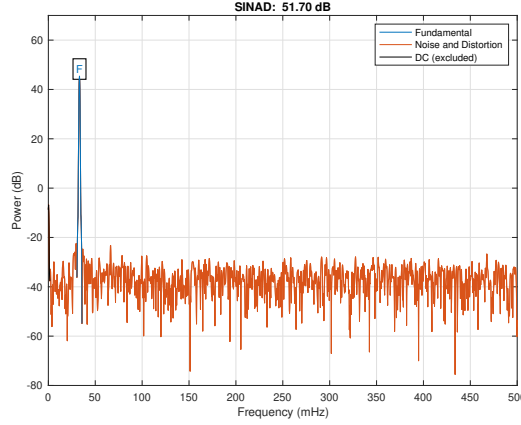


Figure 4.16: SNDR plot after calibration (calibration with a 10-Hz signal).

output for a 500 Hz sine-wave input signal.

For calibration, the μ parameter was set to 10^{-7} and LMS was run for 10^8 iterations in MATLAB. Fig. 4.17 shows the error over a number of iterations. After calibration, the ENOB improves by approximately 10 dB to 51.38 dB, an ENOB of 8.23 bits.

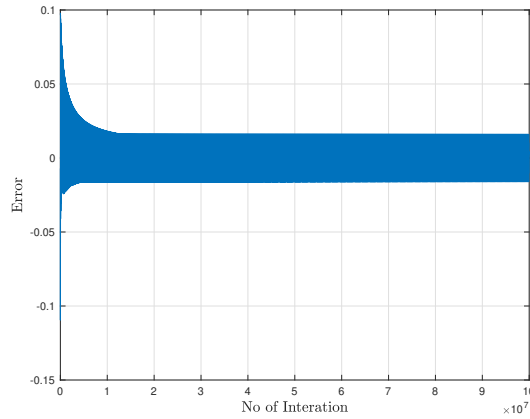


Figure 4.17: LMS calibration error vs iteration.

4.6.5 Coarse Offset Correction Using a Lookup Table

Due to the sensitive nature of the amplifier when operated in high gain settings, the leakage currents through ESD circuits, the substrate, and the PCB traces [116] can cause the amplifiers to have offset. There can also be systematic offsets, based on the location of the channel in the chip and, ultimately, the wafer. In some cases,

the offset leakage currents can be so large that they can saturate the amplifiers. To fix this issue, I have implemented an off-chip loop using DAC and $1\text{ G}\Omega$ resistor. As mentioned in § 3.7, to generate an input current, a $\text{G}\Omega$ resistor is connected to a DAC. The same circuit can also be used to cancel the offset current. A lookup table for the digital code for DAC was created to cancel the offset of each channel by sweeping DAC voltages.

The top row of Fig. 4.18 shows the uncorrected output currents of three different channels (i.e., the signals captured from the ADC output of each channel). In contrast, the bottom row shows the offset leakage-corrected outputs of the same channels.

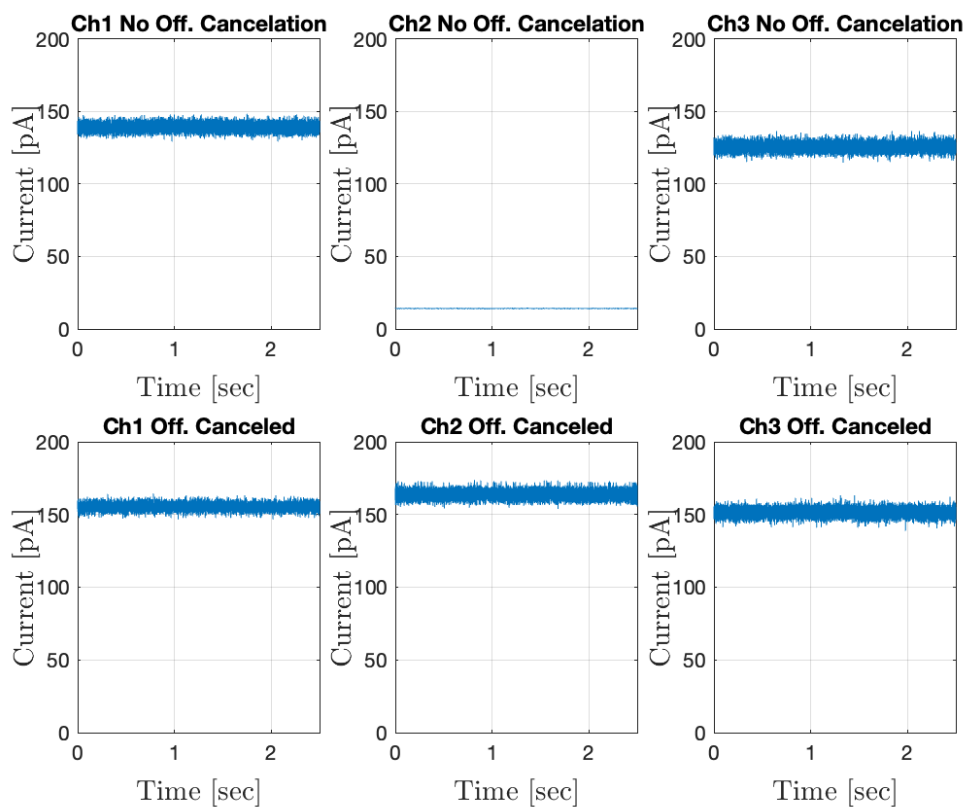


Figure 4.18: Coarse offset correction showing before and after offset cancellation for three channels

The current in channel 2 is very low as the amplifier in that channel is saturated due to leakage currents at its input. This has been corrected by injecting current using the offset cancellation circuits shown in Fig. 4.18 in second row. There is some

residue offset between channels, but this can be taken care of by the gain and offset calibration presented in next section.

4.6.6 Amplifier and ADC Gain and Offset Calibration Combined

As mentioned above, the amplifier suffers from offset error due to leakage from ESD circuits. Also, there are gain errors from variation of circuit elements (i.e. feedback capacitors) due to fabrication and ADC gain error. These errors can be corrected with a similar method as shown in § 4.5.1. For LMS based ADC calibration, the training analog signal is applied to ADC and adaptation is done to the digital output. To correct the errors from the amplifier and ADC combined, I proposed a novel calibration method. In this method, the training sequence is applied to the amplifier and digital adaptations is performed on the digitized output from ADC. This corrects both the offset and gain error from the amplifier and ADC.

The block diagram of the calibration system is shown in Fig. 4.19. A training pattern is amplified using AFE and digitized by the ADC. The expected output data $d[k]$ is subtracted from digitized input $y[k]$ to obtain the error signal $e[k]$. The LMS algorithm performs gradient descent to minimize the error signal $e[k]$ by changing the adaptive weights. In this implementation, I have used 1024 adaptive weights ($w_i[k]$) that are added with equal weights to obtain the output signal. A sine wave of frequency 500 Hz is used as the input training pattern with a μ set to 10^{-7} and the LMS was run for 10^8 iterations in MATLAB.

Fig. 4.20 shows the output square wave before and after calibration. The weights are obtained from adaptation using a sine wave input of frequency 500 Hz is used to calculate the post-calibration signal. The first three rows in Fig. 4.20 shows the corrected and uncorrected signal for three channels. It is evident that the gain and offset of the uncorrected signal of the three channels are varying a lot. The figure in

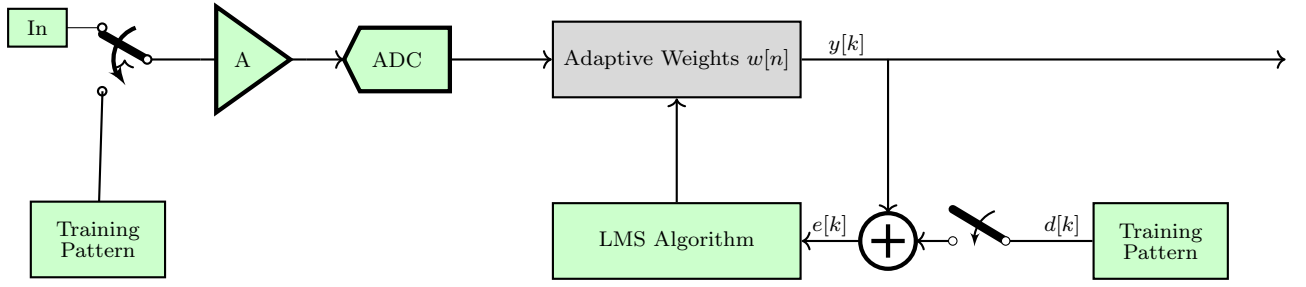


Figure 4.19: Block diagram for LMS based correction with AFE & ADC

the last row shows that all three channels post digital calibration. All gain and offset errors were fully corrected postcalibration as is evident from the figure in the last row. The aforementioned circuit improvements and digital calibration techniques improve the overall accuracy and robustness of the system.

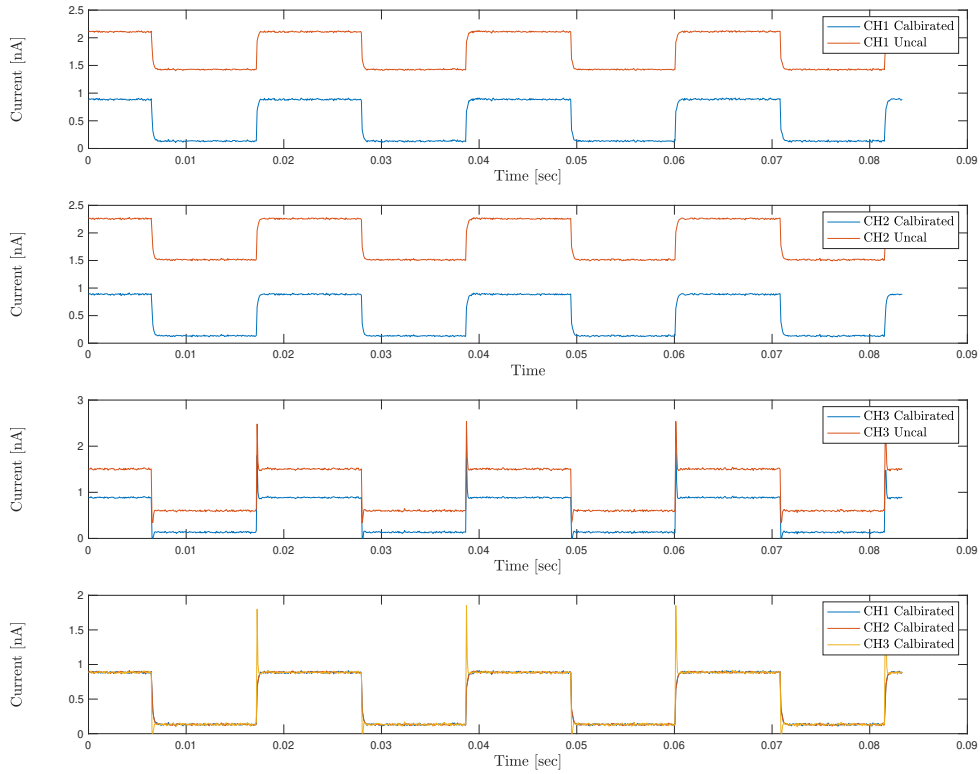


Figure 4.20: Digitized output corrected for amplifier & ADC gain and offset error across 3 channels.

Chapter 5

Asynchronous Reset Amplifier

5.1 Chapter Summary

This chapter introduces a novel amplifier design that employs an asynchronous reset technique to enhance noise performance. Unlike synchronous reset amplifiers, which operate with a periodic clock and suffer from noise issues at high frequencies, the asynchronous design resets only when necessary, avoiding periodic disturbances. The previous implementation [26] of such an amplifier was done with an analog approach. Here, I present a digital differentiator-based approach, which significantly improved power and area efficiency. Reducing area and power are imperative to build a high-throughput readout array for nanopore based DNA sequencing.

Measurements indicate that the asynchronous design reduces noise by a factor of two compared to synchronous reset amplifiers at same SNR. It consuming 0.7 mW of power per channel compared to 41 mW consumed by all analog approach [26]. The throughput density of the asynchronous reset amplifier is 42.4 kbp/s/mm² at SNR of 20 dB, which gives a 25x improvement compared to ONT's system.

5.2 Introduction

Synchronous reset amplifiers provide low noise at low sampling rates, but at high sampling frequencies the noise is dominated by the disturbances arising from the reset of the opamp's feedback capacitances (e.g., the integrator's C_F). To overcome this issue, an asynchronous reset topology can be used. In an asynchronous amplifier, the system operates continuously, without a periodic clock; it is only reset to prevent the device from saturating due to excessive signal voltage build-up on a capacitor. The reset is still performed periodically, but multiple samples are taken during that period. The illustration of amplifier output and phase timing for the amplifier is shown in Fig. 5.2.

An amplification chain using such an approach was proposed in [26], but this system implements an analog filter, differentiator, and track-and-hold (T&H). This implementation consumes much larger area and power. The amplifier presented in [26] takes up 4.5 mm^2 per channel and consumes 41 mW per channel. To improve power consumption and area requirements while providing comparable noise performance to make it an attractive solution for readout array, I propose an asynchronous reset amplification chain that implements a digital differentiator. My AFE consumes 0.7 mW and each channel takes up area of 0.0542 mm^2 .

The proposed amplifier consists of a discrete-time (DT) integrator, a low-pass filter (LPF), a capacitive variable gain stage and passive track-and-hold. The digital differentiator takes two consecutive samples of the input signal and produces the difference between them. The ratio of the difference in voltage over the gain of the amplifier represents the input current.

An example of amplifier readout timing is shown in Fig. 5.3. The master clock frequency in this example is 4 MHz. The amplifier's reset rate is 25 kHz ($80 \mu\text{s}$), while the sampling frequency is 45.4 kHz. The amplifier is reset for $2 \mu\text{s}$ (8 cycles), and the first sample is taken after a delay of another $2 \mu\text{s}$ (8 cycles) to minimize the

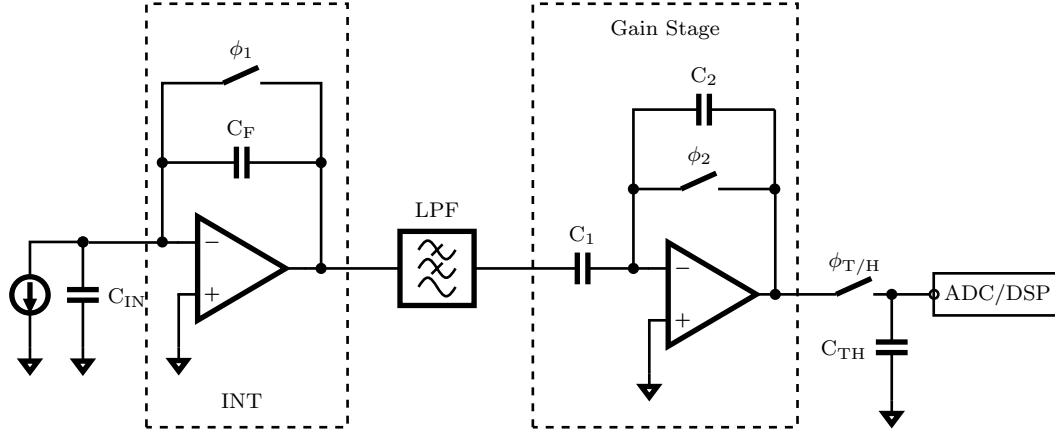


Figure 5.1: Asynchronous DT capacitive feedback AFE.

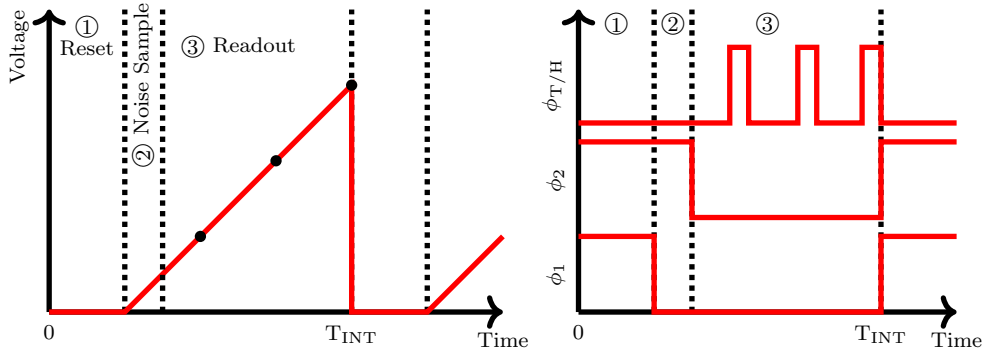


Figure 5.2: Illustration of the amplifier output (left) and phase timing (right) for the amplifier

effects of kT/C and reset switch noise. The difference between 'Sample 2' and 'Sample 1' gives the first readout. Similarly, the difference between 'Sample 3' and 'Sample 2' gives the second readout. In this example, only three samples were taken within one reset cycle, but more samples can be taken within a single reset cycle.

5.3 Amplifier Analysis

The transimpedance gain of the amplifier is given by

$$R_{TIA} = \frac{T_S}{C_F} \cdot G_{GS} \quad (5.1)$$

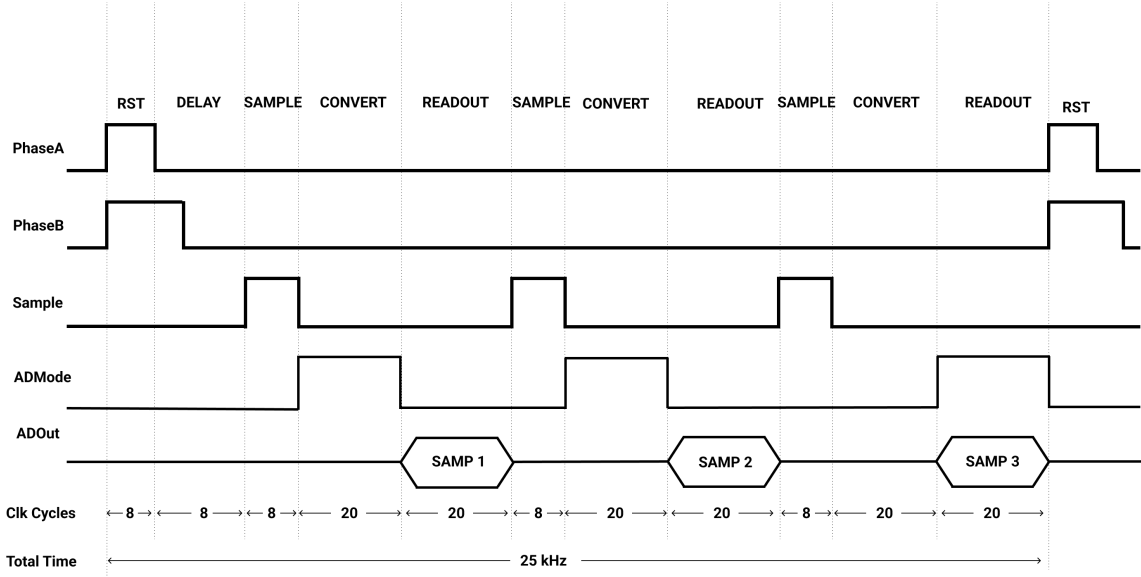


Figure 5.3: Timing diagram for asynchronous reset amplifier.

where R_{TIA} is the TIA's equivalent resistance, T_S in the sampling interval, C_F is the feedback capacitor of the integrator and G_{GS} is the gain of gain-stage amplifier.

The saturation time of the amplifier and the gain stage dictate the maximum reset period. The saturation time of the amplifier is given by

$$T_R < T_{SAT} = \frac{C_F}{G_{GS}} \cdot \frac{V_{MAX}}{I_{IN}} \quad (5.2)$$

For a 200 pA input range, $C_F=200$ fF, second stage gain of 2 and maximum output swing of opamp is 900 mV then the reset period cannot be larger than 450 μs .

$$T_R < T_{SAT} = \frac{200 \cdot 10^{-15}}{2} \cdot \frac{0.9}{200 \cdot 10^{-12}} = 450 \mu sec \quad (5.3)$$

The maximum voltage allowed depends on the technology node and the opamp design and cannot be improved much further in the 130 nm node. To increase the reset period T_R , we have to increase the value of the feedback capacitance. This usually increases the noise but is required to operate the amplifier for longer without reset.

5.3.1 Noise Analysis

The noise spectrum of a continuous time integrator with capacitive feedback is given by

$$S_{min}(f) = (2\pi f)^2 \cdot (C_F + C_{IN})^2 \cdot v_n^2 \quad (5.4)$$

where C_F is the feedback capacitor, C_{IN} is the input capacitance, and v_n^2 is the noise spectral density of the opamp.

The extra noise due to reset is given by [26]

$$S_{reset}(f) = \frac{(\tau_R/T_R)^2 \cdot \text{sinc}^2(\frac{f}{f_R}) \cdot \sum_k S_{min}(f - kf_R) \cdot R_{eq}^2(f - kf_R)}{R_{eq}^2(f)} \quad (5.5)$$

where τ_R is the time for which the amplifier is reset, f_R is the reset frequency.

The input referred noise density of an asynchronous reset amplifier is the sum of noise of a continuous time amplifier noise & extra noise added due to the reset of integrator and is given by [26]

$$S_{in}(f) = S_{min}(f) + \frac{(\tau_R f_R)^2 \cdot \text{sinc}^2(\frac{f}{f_R}) \cdot \sum_k S_{min}(f - kf_R) \cdot R_{eq}^2(f - kf_R)}{R_{eq}^2(f)} \quad (5.6)$$

where $S_{in}(f)$ is the input referred noise, $S_{min}(f)$ is the minimum noise of the integrator. Eq. 5.6 implies that the amplifier reset adds extra noise. At high reset frequencies, the added noise as the factor τ_R/T_R is large. Hence, the asynchronous approach can give lower noise performance compared to synchronous reset.

5.4 Simulation Results

To simulate the noise analysis, transistor level schematics were used in the integrator and filter stage. The digital differentiator was implemented with a verilog model as shown in [123]. Noise and gain were simulated using PSS + PAC & PNoise simulation.

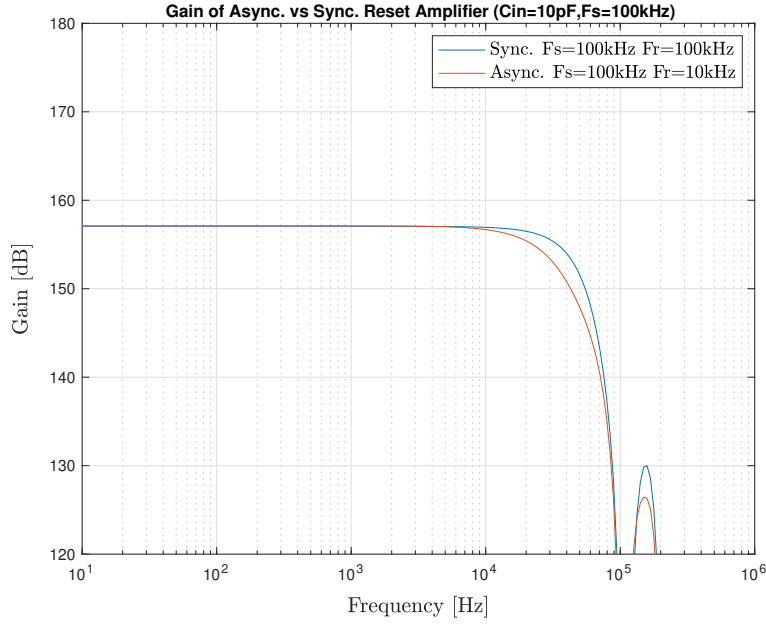


Figure 5.4: Asynchronous reset amplifier vs. synchronous reset amplifier gain comparison.

Fig. 5.4 shows the gain comparison of an asynchronous reset amplifier and a synchronous reset amplifier. The asynchronous reset amplifier was reset every $100 \mu\text{s}$ and is sampling at 100 kHz while the synchronous reset amplifier is sampled *and* reset at a 100 kHz rate. The gain of both amplifiers is similar at low frequencies as expected but the asynchronous amplifier drops off at a lower frequency.

Fig. 5.5 provides a comparison of input-referred noise of the asynchronous reset amplifier and the synchronous reset amplifier. This result was obtained from PSS + PNoise analysis with input capacitance of 10 pF. The noise spectral density for synchronous amplifier is approx. $4.7 \text{ fA}/\sqrt{\text{Hz}}$ while the noise spectral density for asynchronous amplifier is $2 \text{ fA}/\sqrt{\text{Hz}}$. The noise density of the asynchronous noise amplifier is much lower. This is because of the lower reset noise in the asynchronous reset amplifier. The integrated noise of the asynchronous amplifier is 447 fARms while the noise of the synchronous amplifier is 1.05 pARms.

Fig. 5.6 shows the input-referred noise with respect to the input capacitance of 10 pF & 30 pF. The noise spectral density for amplifier with 10 pF input capacitance is $2 \text{ fA}/\sqrt{\text{Hz}}$ while the noise spectral density for amplifier with 30 pF is $5.5 \text{ fA}/\sqrt{\text{Hz}}$.

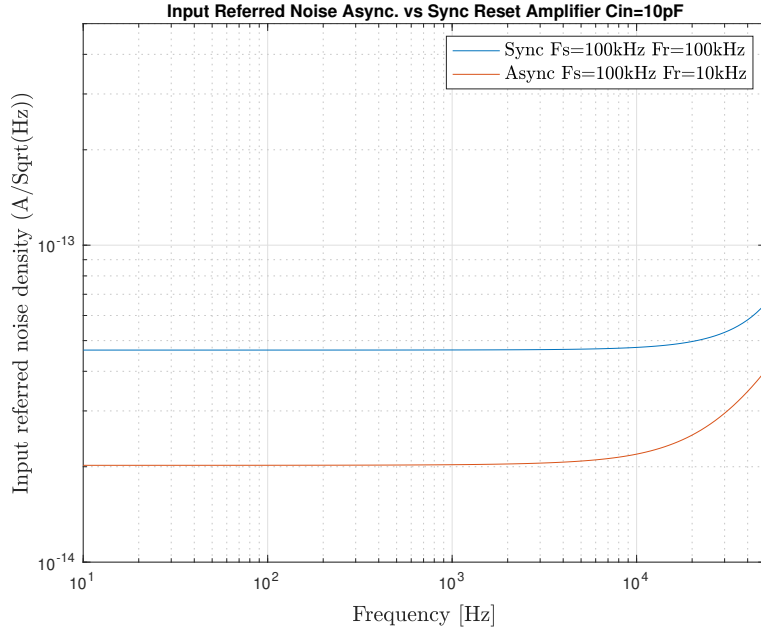


Figure 5.5: Asynchronous Reset amplifier vs Sync Reset Amplifier noise spectral density

As expected, a larger input capacitance increases the input-referred noise density.

5.5 Measurement

5.5.1 Measurement Setup

The amplifier was verified using the chip and test setup implemented in DROICv2. The amplifier was reset asynchronously by altering the firmware on CPLD. For each reset cycle, the amplifier was sampled and digitized eight times. To perform differentiation, the consecutive digitized samples were subtracted in the plotting software.

5.5.2 Asynchronous System Transient

To verify the transient behavior, I applied a 150 Hz square wave with 100 pA amplitude to the amplifier. Fig. 5.7 shows the raw digitized output of the amplifier captured for a 100 pA input square wave sampled at 148.8 kHz. In Fig. 5.7, two distinct levels

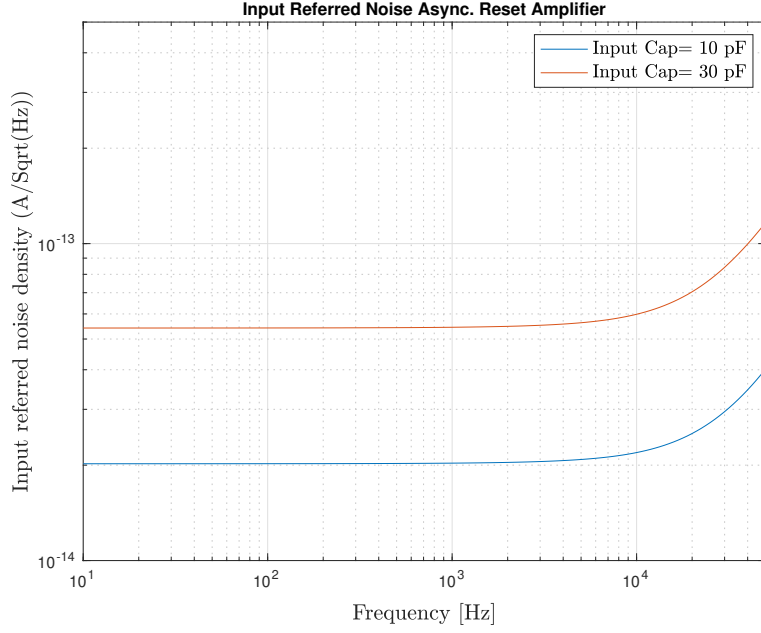


Figure 5.6: Async amplifier noise density wrt. input capacitance

are visible caused by different levels of the square wave. The amplifier's reset rate is 16 kHz.

The consecutive raw digitized samples are subtracted to calculate differentiated digital data. Fig. 5.8 shows the transient output of the amplifier after digital differentiation for an input of 400 pA sampled at 148.8 kHz.

5.5.3 Asynchronous System Noise

Fig. 5.9 shows the input referred noise measured at 100 kSps with an input capacitance of 100 pF. The blue plot shows the noise achieved with a reset frequency of 16 kHz while the yellow plot shows the noise at a reset frequency of 10 kHz. As expected, 10 kHz reset frequency has lower noise density compared to 16 kHz due to larger τ_r/T_R factor. There is a rise in noise at high frequencies due to lower corner frequency in the gain as shown in the § 5.4.

Fig. 5.11 shows the open-input noise wrt sampling frequency. The noise density of the 30 kSps system is lower than that of the 148.8 kSps system. This is due to the lower gain and the higher reset frequency. Furthermore, the open-input noise density

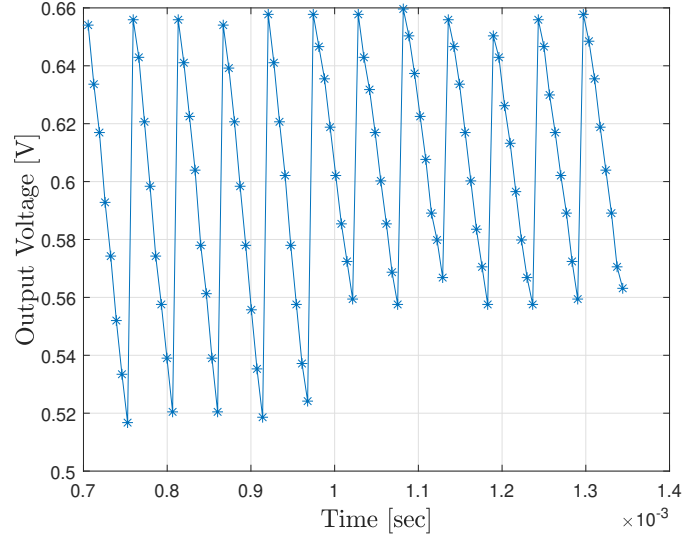


Figure 5.7: Raw output for 100-pA square wave input sampled at $F_s = 148.8$ kHz.

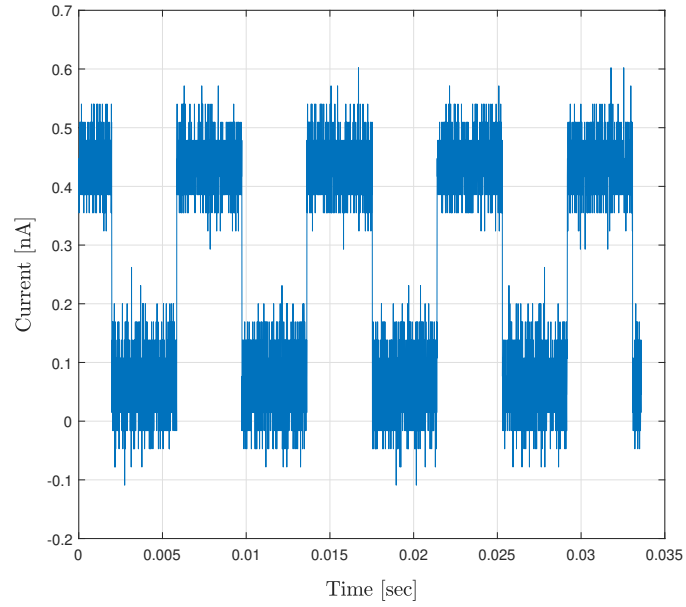


Figure 5.8: Process transient output for a 400-pA square wave input sampled at $F_s = 148.8$ kHz.

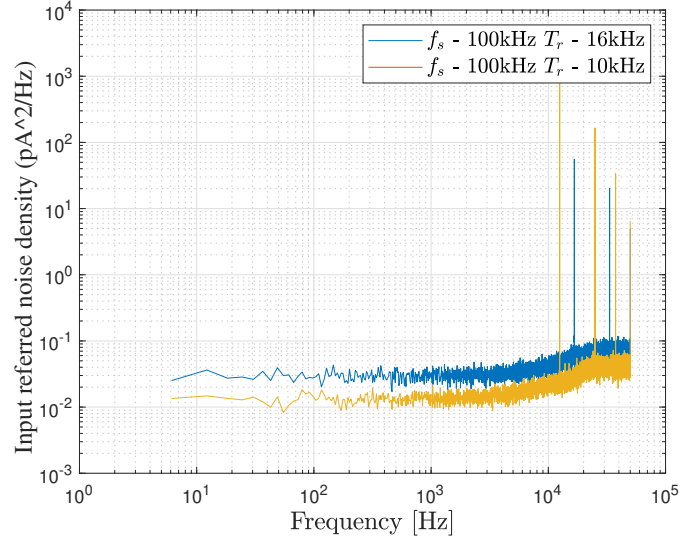


Figure 5.9: Asynchronous noise with respect to the reset frequency. Input capacitance = 100 pF and $F_s = 100$ kHz.

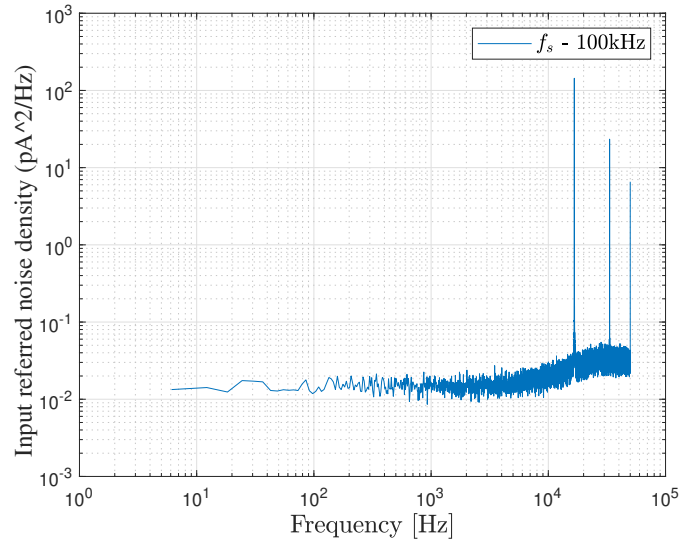


Figure 5.10: Asynchronous noise with respect to the sampling frequency. Input capacitance = 100 pF and $F_s = 10$ kHz.

of the synchronous reset amplifier is $11.95 \text{ fA}/\sqrt{\text{Hz}}$ for 14 kSps while for asynchronous reset amplifier is $7 \text{ fA}/\sqrt{\text{Hz}}$ for 30 kSps. This shows a further improvement in the noise performance by a factor of two compared to the synchronous reset amplifier. The integrated open-input noise for the 30 kSps system is 0.85 pArms while for the 148.8 kSps system it is 114.4 pArms. The integrated noise of the open input synchronous amplifier is 1 pArms for a 14 kSps sampling rate and 112.8 pArms for a 72 kSps sampling rate. Using an asynchronous reset technique, we can improve the bandwidth by approximately a factor of 2 for the same SNR.

As mentioned § 3.7.3.1 to extrapolate the effect of input capacitance noise was scaled by a factor of two. The integrated noise of the asynchronous reset amplifier is $1.5 \text{ pA}_{\text{rms}}$ at 23 kSps ($2 \times 7 \text{ fA}/\sqrt{\text{Hz}} \times 11.5 \text{ kHz}$). The throughput density of the asynchronous reset amplifier is 42.4 kbp/s/mm^2 ($2300 \text{ bps}/0.0542 \text{ mm}^2$) at SNR of 20 dB, which gives a 25x improvement compared to ONT's system.

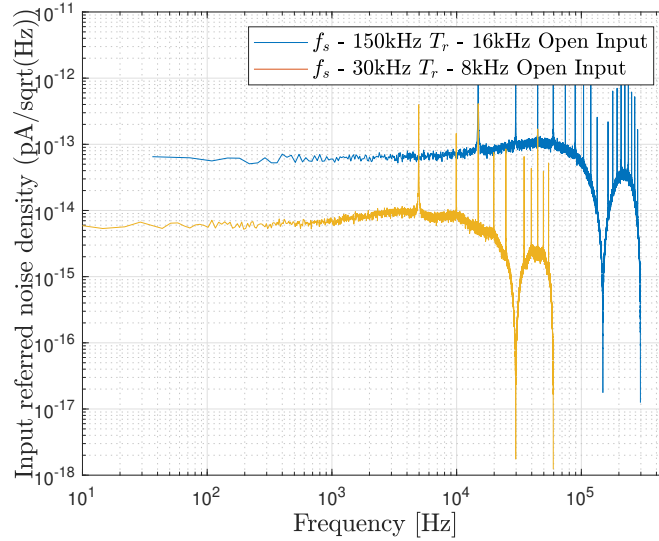


Figure 5.11: Open input noise for $F_s = 30 \text{ kHz}$ and 148.8 kHz .

Chapter 6

Ion-channel and Solid-state Measurements

6.1 Chapter Summary

This chapter focuses on the experimental validation of a DROIC through biological ion channel and solid-state nanopore measurements. I discuss biological ion-channel experiments to measure the noise characteristics and ion-channel activity, which mimic the signals observed in typical DNA sequencing experiments. The lipid bilayer was created using DPhPC in N-hexane and a 1M KCl buffer, and its quality was evaluated by measuring capacitance, where a low capacitance value indicated a properly formed bilayer. Noise measurements were performed on lipid bilayer at different sampling rates (3.5 kSps and 14 kSps), highlighting the relationship between the sampling rate and the integrated noise. The chapter also covers the ion channel activity of Gramicidin, a peptide antibiotic effective against Gram-positive bacteria. The activity of gramicidin mimics the signal generated by a nanopore and demonstrated the capability of the DROIC to perform such measurements.

The next section examines solid-state measurements using three different substrates with varying degrees of PDMS coverage. PDMS is usually applied to reduce the ca-

capitance and noise in the nanopore chip. Transient measurements and noise spectrum analysis further validated the amplifier’s performance in solid-state nanopore setups, demonstrating DROIC’s ability to perform solid-state nanopore experiments aswell.

The chapter concludes with a section on on-chip post-processing, which describes the fabrication of Ag/AgCl electrodes directly on the chip. These electrodes are essential for performing voltage clamp experiments. The process involved etching aluminum pads, electroplating silver, and chlorinating silver to create Ag/AgCl electrodes. The final experiment tested the amplifier using a $1\text{ G}\Omega$ resistor and evaluated its noise performance.

In conclusion, the chapter provides a detailed analysis of how these experiments validated the DROIC in both biological and solid-state contexts.

6.2 Introduction

This chapter delves into the experimental validation of the Digital Readout Integrated Circuit (DROIC) through biological ion-channel and solid-state nanopore measurements, providing a comprehensive assessment of its performance in realistic scenarios. These experiments aim to evaluate the DROIC’s ability to process signals analogous to those encountered in DNA sequencing. By testing the system in a wet environment and conducting on-chip post-processing, the chapter establishes the DROIC’s robustness, sensitivity, and adaptability across various experimental setups. The results not only demonstrate the DROIC’s noise characteristics and signal fidelity but also highlight its compatibility with integrated biological and solid-state platforms, advancing its potential for next-generation molecular sensing applications.

6.3 Biological ion-channel experiments

To validate the functionality of the amplifier in a wet environment, I have performed experiments to measure noise and ion-channel activity. The ion-channel activity mimics the signals produced in typical DNA experiments.

Fig. 6.1a shows a simplified picture of the experimental setup for noise measurements of the lipid bilayer. The fluidic cell used in the experiment shown in Fig. 6.1b was obtained from Elements SRL. The fluidic cell contains a 10- μm Teflon film with 100 μm aperture which separates the *cis* and *trans* chambers. The fluidic cell was connected to the DROIC using an SMB connector. The flow cell has an integrated silver electrode that was chlorinated using Sodium Hydrochloride (bleach).

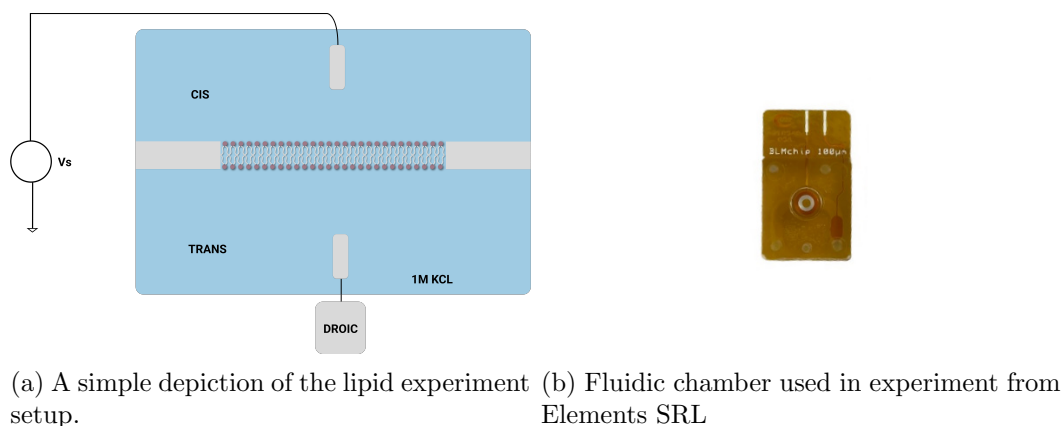


Figure 6.1: Test apparatus and fluidic chamber used in lipid bilayer experiments

The lipid bilayer was created using 10 mg/ml DPhPC in N-hexane (4ME 16:0 PC - 1,2-diphytanoyl-sn-glycero-3-phosphocholine) and formed on a 100- μm Teflon aperture using a pipetting technique in a 1M KCl buffer. In the pipetting technique, a small amount of DPhPC solution (1 μL) is loaded onto a pipette tip. The *cis/trans* wells of the chambers are filled with 1M KCl buffer. The pipette is brought close to the aperture between the *cis/trans* chamber, and a bubble is created to form the lipid.

The quality of the lipid bilayer is investigated by measuring the capacitance and resistance. A perfect bilayer can be treated as capacitor between the *cis* and *trans*

electrodes. By applying a triangular voltage wave to the cis side of the fluidic chamber, a square wave current is applied to the amplifier. The capacitance of the bilayer can be derived from the capacitive current-voltage relation

$$C = I / \left(\frac{dV}{dt} \right). \quad (6.1)$$

Where $\frac{dV}{dt}$ is the frequency of triangular wave applied and I is the current measured by the amplifier.

The resistance of the bilayer can be measured by applying a constant voltage from the cis side of the fluidic chamber and measuring the leakage current through the amplifier.

$$R = \frac{(V_{cis} - V_{trans})}{I}. \quad (6.2)$$

where V_{cis} is the constant voltage applied in the cis chamber, V_{trans} is the amplifier bias voltage and I is the current measured by the amplifier. A capacitance lower than 40 pF for 100 μm could indicate the presence of a lipid plug (a blob of lipid at aperture) instead of a bilayer. The resistance of a good bilayer is in range of 10s G Ω . A leaky bilayer with resistance in the range of M Ω can also indicate the presence of a blob or unstable bilayer.

The noise spectrum of the amplifier connected to a lipid bilayer is shown in Fig. 6.2. The noise of the lipid bilayer was measured with a sampling rate of 3.5 kSps and 14 kSps.

Fig. 6.3 shows the integrated noise as a function of the integration bandwidth. The integrated noise at 3.5 kSps is 1.5 pARms. This noise would be lower in an integrated setup as the input capacitance of the integrated lipid bilayer is in the range of 2 pF and it doesn't not have noise due to PCB traces & ESD circuits.

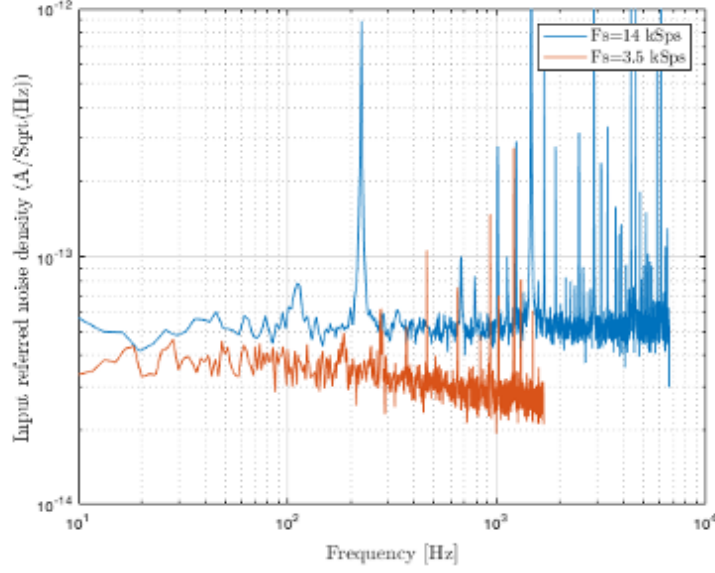


Figure 6.2: Noise spectrum for a lipid bilayer at 14 kSps and 3.5 kSps sampling frequencies.

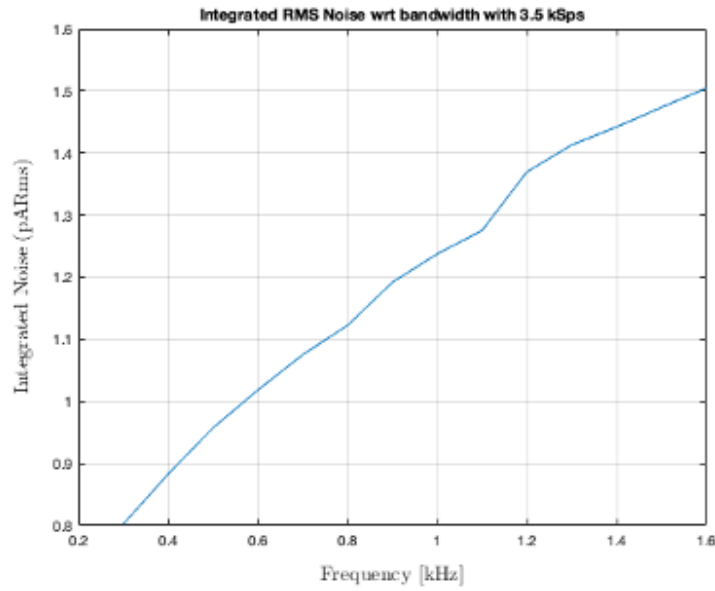


Figure 6.3: Ion-channel integrated noise vs. bandwidth for an input capacitance of 40 pF and $F_s=3.5$ kHz.

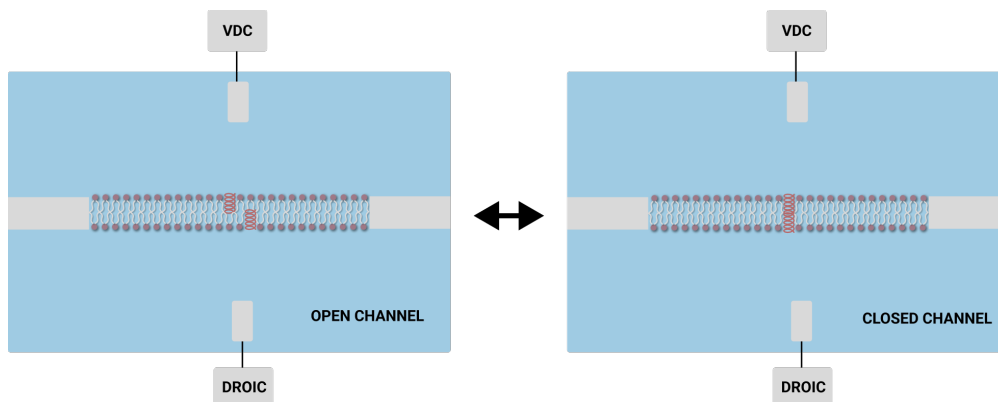


Figure 6.4: Gramicidin ion-channel activity illustration.

6.3.1 Gramicidin Ion-channel Activity

Gramicidin is a peptide antibiotic that is particularly effective against Gram-positive bacteria. The Gramicidin molecule disrupts bacterial cell membranes by forming channels, which leads to the leakage of their cellular contents and eventually cell death. It is commonly used in topical medications, especially in ointments for skin infections. Gramicidin causes this leakage by making a bond between two molecules on each side of the lipid membrane. The activity of gramicidin closely emulates the signal observed from DNA passing through a nanopore. Thus, this experiment demonstrates the AFE's capability to measure signals closely resembling those from a nanopore.

I recreate the action of Gramicidin in the fluidic chamber shown in Fig 6.1b and measure the activity of peptide using DROIC. The illustration of Gramicidin activity is shown in Fig. 6.4. The red coil structures denote Gramicidin peptides. Gramicidin molecules in the *cis* chamber attach with other Gramicidin molecules on the *trans* side of a membrane to form a channel that causes an increase in the ionic current through the membrane.

For this experiment, after forming a bilayer using the pipette method as mentioned in the previous section, 1 μL solution (1 $\mu\text{g}/\text{ml}$ Gramicidin in methanol) was added to the *cis* and *trans* side of the flow cell. A constant voltage of 100 mV is applied through

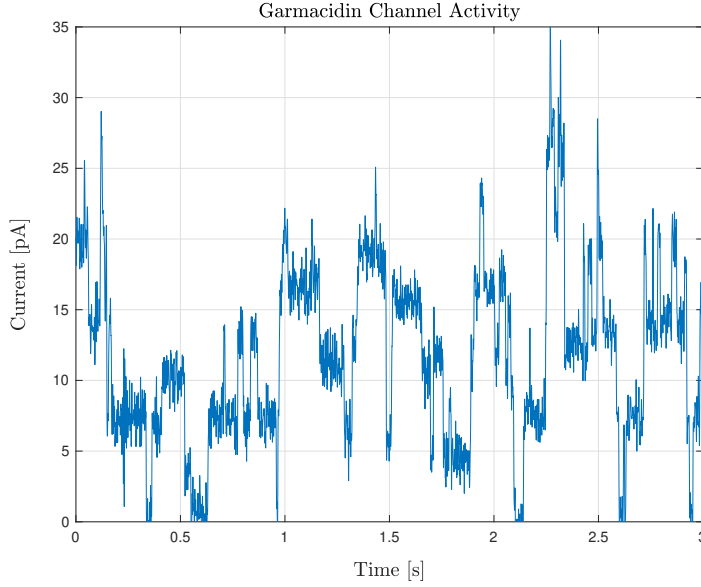


Figure 6.5: Gramicidin ion-channel activity in KCl buffer filtered at 1000 Hz.

the two chambers and across the membrane. The ion-channel activity was recorded and is shown in Fig. 6.5. The changes in the current signal are due to channel activity and can be observed in Fig. 6.5. The signal measured here is very similar to the signal observed from DNA passing through an ion-channel. This demonstrates the ability of DROIC to perform ion-channel experiments.

6.4 Solid state measurement

To validate the functionality of the amplifier with a solid-state nanopore, I have performed experiments using three different solid-state substrates shown in Fig. 6.6.

The first substrate has a $10\mu\text{m}\times 10\mu\text{m}$ window of SiO_2 with a thickness of 60 nm. The second substrate has a $10\mu\text{m}\times 10\mu\text{m}$ window of SiO_2 with thickness of 60 μm which is partially covered with PDMS. In the third substrate the $10\mu\text{m}\times 10\mu\text{m}$ windows is fully covered with PDMS. PDMS is used to cover SiO_2 in order to lower noise by reducing the capacitance of the nanopore chip.

To validate this, I measured the noise of the amplifier by connecting the three differ-

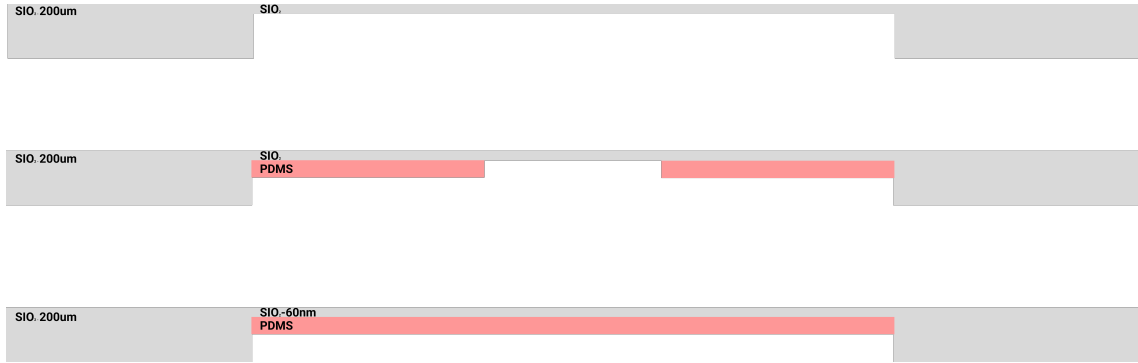


Figure 6.6: Three different substrates used in solid state experiments.

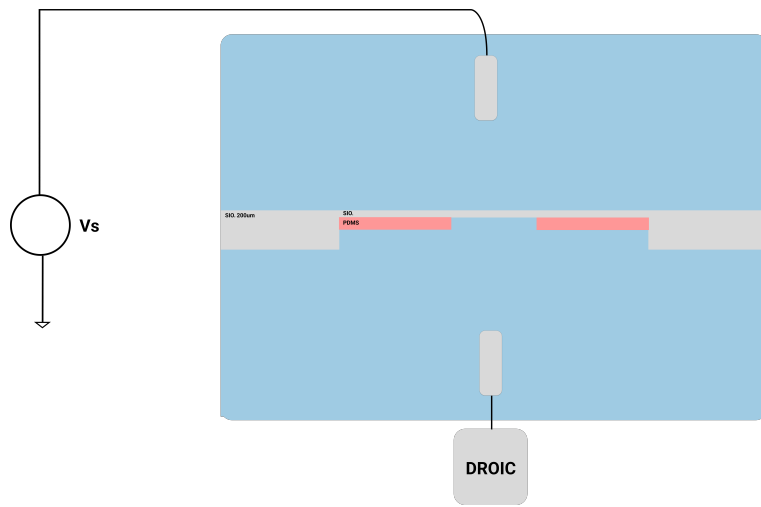


Figure 6.7: Solid state experiment setup

ent substrates to the amplifier using flow cells from Northern Nanopore. Furthermore, I estimate the capacitance of the substrates by probing them with triangular voltage waveforms and analyzing the output of the amplifier. An illustration of the experimental setup is shown in Fig. 6.7.

6.4.0.1 Transient Results

An SiO_2 substrate without a nanopore can be treated as a capacitor. By applying a triangular voltage wave to the capacitor through the fluidic chamber, a square wave current is applied to the amplifier. The amplitude of the square-wave can be derived

from the capacitive current-voltage relation

$$I = C \frac{dV}{dt}. \quad (6.3)$$

The capacitance for the three substrates is different and hence gives different amplitudes of the square-wave current.

Fig. 6.8 shows the current measured by applying a triangular wave with pk-pk amplitude of 200 mV and frequency of 150 Hz and 300 Hz to the PDMS covered substrate. The output was sampled at 36 kSps while the amplifier was operated in 3 nA input current range. A 150 Hz 200 mV input triangular wave results in approximately 0.8 nA square-wave. Using the equation above, the capacitance can be estimated to be around 13 pF. Similarly, the 300 Hz 200 mV triangular-wave results in approximately 1.5 nA current. This also results in approximately 13.5 pF of substrate capacitance.

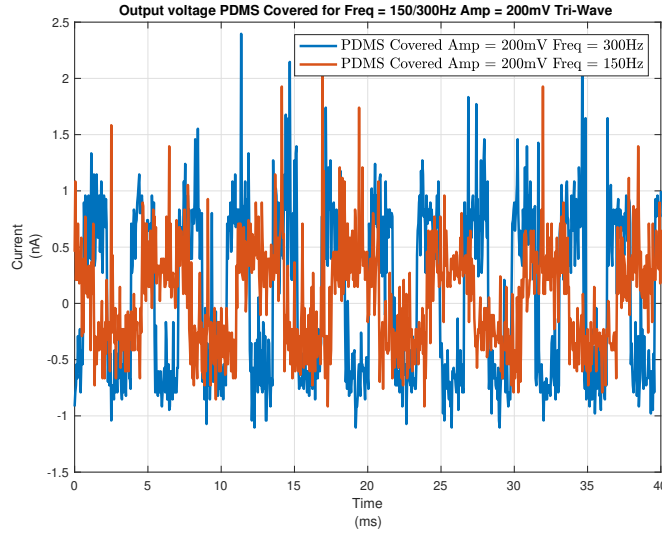


Figure 6.8: Transient output for PDMS-covered substrate for a 200-mV triangular input at frequencies of 150 Hz and 300 Hz.

Fig. 6.9 shows the current measured by applying a triangular wave with pk-pk amplitude of 20 mV and 40 mV and frequency of 100 Hz to a substrate partially covered with PDMS. A 100-Hz 20-mV input triangular wave results in approximately a 0.9 nA

square-wave current. This implies approximately 22.5 pF of substrate capacitance.

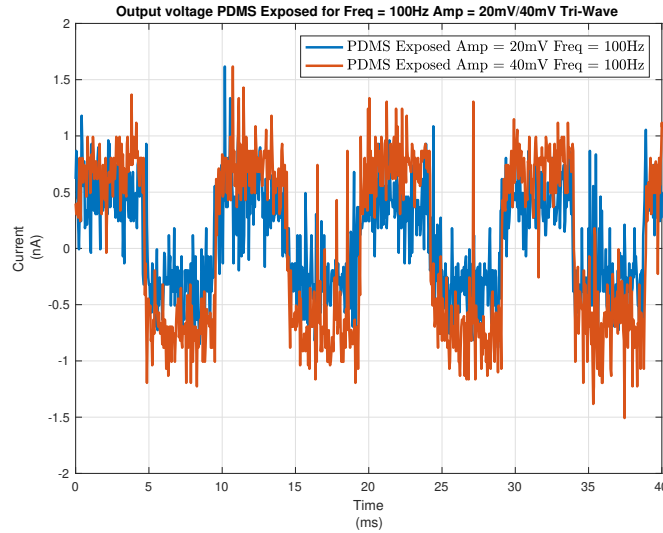


Figure 6.9: Transient output for a PDMS-exposed substrate. The input was a triangular wave with 20 mV and 40 mV pk-pk amplitude and 100-Hz frequency.

6.4.0.2 Noise Measurement Results

The noise of the three substrates was measured by applying a constant voltage from a source and measuring the output noise of the amplifier. The input noise can be obtained by dividing the output noise of the amplifier by the gain of the amplifier.

Fig. 6.10 shows the noise spectrum density of the three chips. The chip covered with PDMS As expected, the chip fully covered with PDMS has the lowest noise while the bare SiO₂ chip had the highest noise. This is because the bare SiO₂ chip has the highest capacitance, followed by the partially covered substrate capacitance. The fully covered PDMS substrate has the lowest capacitance and hence the lowest noise.

Fig. 6.11 shows the integrated noise of solid-state nanopore as a function of bandwidth. Noise for fully PDMS-covered substrate is ~ 145 pArms, for the partially covered substrate it is ~ 170 pArms and for the substrate without PDMS it is ~ 275 pArms.

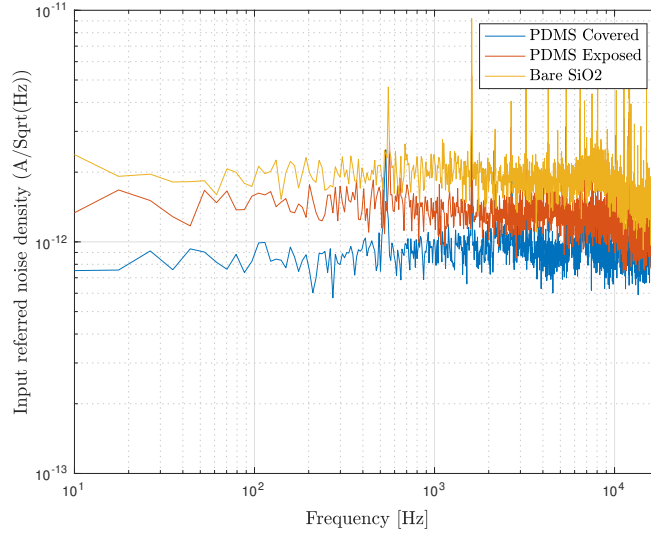


Figure 6.10: Input referred noise for substrates measured at 36 kSps.

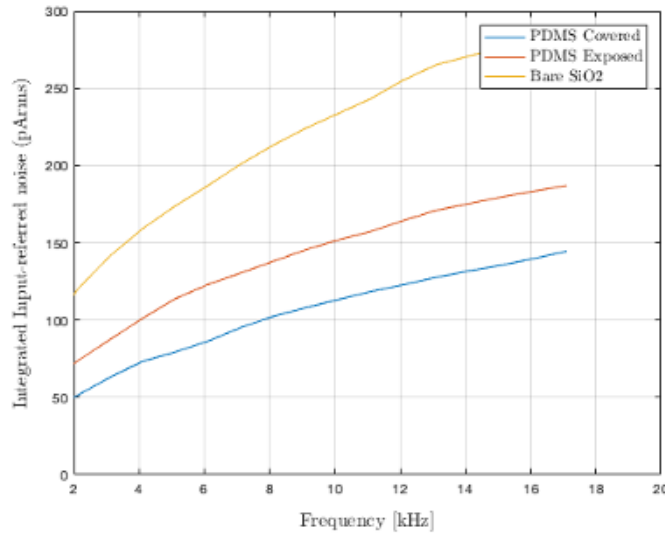


Figure 6.11: Integrated noise with respect to bandwidth.

6.5 On-Chip Post-processing

The DROIC chip has dedicated pads that could facilitate on-chip Ag/AgCl electrode fabrication. In a standard CMOS process, the pads are typically made up of Aluminum or aluminum-Copper alloy. Ag/AgCl forms appropriate electrochemical interfaces needed for voltage clamp experiments.

First the chip was encapsulated with epoxy covering the bond wires using dam-and-

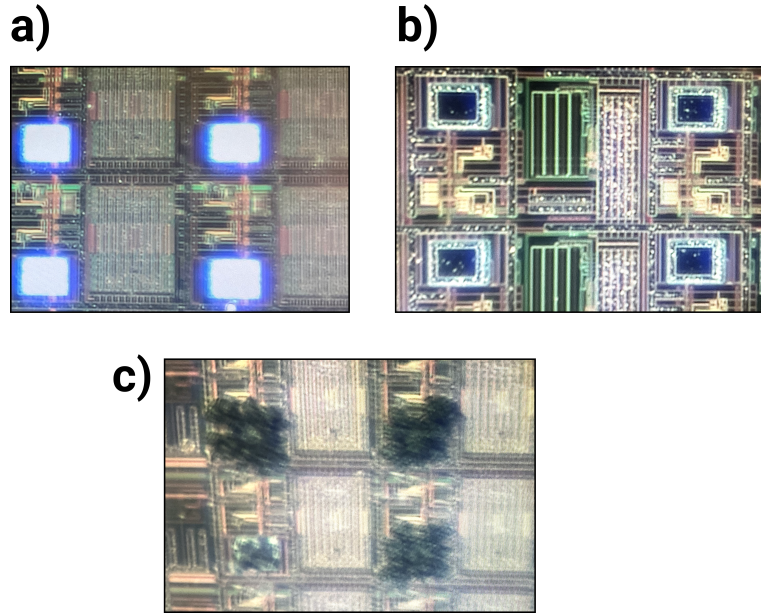


Figure 6.12: Post processing of the chip to remove aluminium and deposit Ag/AgCl a) Micrograph of chip with aluminium electrode before etching b) Micrograph of chip after etching aluminium electrode c) Micrograph of chip after electroplating Silver

fill while exposing the pads in the center of the chip. The aluminum on the exposed pads was etched off using an acidic aluminum etchant (Type A, Transene). The chip was exposed to an aluminum etchant for 20-25 minutes to remove the aluminum pads while not affecting the layers below. The chip was flushed with DI water to remove any remaining etchant. The etched pads are shown in Fig. 6.12b.

The silver was electroplated using an electroplating solution (PNPCS9 Caswell Canada). The electroplating solution was added to the chamber created over the chip. Using a DC current source, a $1\ \mu\text{A}$ current was injected for a few minutes to create a layer of silver. The deposited silver was chlorinated using commercially available bleach. The electroplated Ag/AgCl electrode is shown in Fig. 6.12c.

To test the amplifier, a $4\ \text{pA}$ current was injected in DROIC by applying 4-mV square-wave through a $1\ \text{G}\Omega$ resistor. The output current is shown in Fig. 6.13.

The noise spectral density amplifier with electrode and $1\ \text{G}\Omega$ at $7\ \text{kSps}$ is shown in Fig. 6.14. Integrated noise for $7\ \text{kSps}$ is $1.7\ \text{pArms}$. This noise is higher than expected

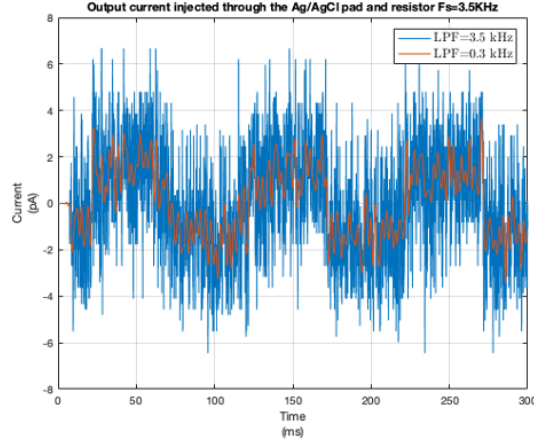


Figure 6.13: Output current injected through Ag/AgCl pad and 1-G Ω resistor.

but is caused by extra capacitance from the buffer to the top metal layers of the chip. This could be reduced by creating a layer of SU-8 on the chip only by exposing the pad shown in [23, 82].

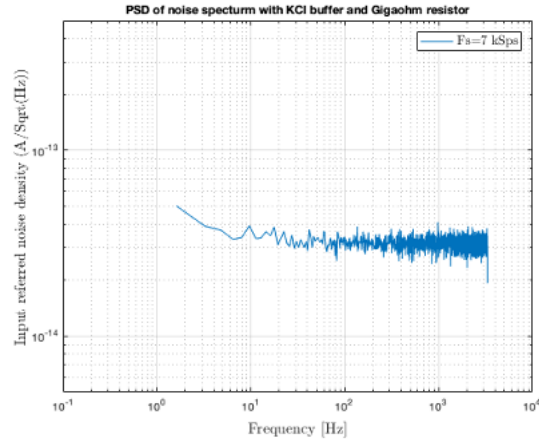


Figure 6.14: Input referred noise for Ag/AgCl pad and 1G Ω resistor.

Chapter 7

Digital Back-end - Basecaller

7.1 Chapter Summary

This chapter focuses on integrating digital computation on SoC into miniature sequencers. The specifications for such a SoC are demanding, as it must process data in real-time while operating under stringent power constraints, typically under 100 mW. The proposed SoC is designed using 22-nm CMOS technology to balance speed, power efficiency, and cost. It includes a RISC-V core for general-purpose processing and a custom accelerator for specific bioinformatic tasks, such as extracting DNA base sequences from ASIC signals. This architecture allows the SoC to handle high-throughput sequencing data efficiently, enabling real-time pathogen detection and reducing the need for external data transmission.

The SoC's system organization integrates the RISC-V core and accelerator through the RoCC interface, allowing for efficient communication and data exchange. The accelerator is responsible for intensive bioinformatic processing, significantly improving performance compared to traditional processors. The chip was tested and demonstrated a 10x speed improvement over an ARM Cortex-A53 processor, even when operating at a lower clock speed of 200 MHz, and achieved a 200x improvement in energy efficiency, consuming less than 19 mW during operation. These results un-

underscore the potential of the SoC to support mobile DNA sequencing applications, offering significant benefits in speed, energy efficiency, and real-time analysis capabilities. This work represents a crucial step towards the development of self-contained DNA sequencing systems, laying the foundation for future advancements in mobile health monitoring and personalized medicine.

7.2 Introduction

Hand-sized DNA sequencers weighing less than 100 grams are being increasingly used in research laboratories around the world. Although not as accurate as their large and established counterparts, these miniature sequencers are valued for their ability to read much longer strands of DNA. Their low-cost and their portability are also prized advantages.

A block diagram conveying the main parts of a modern miniature DNA sequencing system is shown in Fig. 7.1. As illustrated, on the device's printed circuit board (PCB) there are four main chips: i) a sensor array that converts DNA sample molecules into electronic-current equivalents; ii) a mixed-signal application-specific integrated circuit (ASIC) capable of amplifying, filtering, and digitizing the sensed electronic currents; iii) a field-programmable gate array (FPGA) to control, buffer and organize the sampled signals emerging from the ASIC; and iv) a universal-serial bus (USB) chip that communicates the gathered DNA measurements off-board [28].

In a typical existing use-case, DNA samples are intermittently introduced across the sensor array via a miniature flow apparatus. Within seconds, corresponding sampled electronic-current signals emerge as packet data from the USB device for further bioinformatic processing off-board. Such a stream of output data can continue uninterrupted for hours effectively making this a real-time measurement device with exciting potential for continuous health monitoring in personalized medicine or community health contexts.

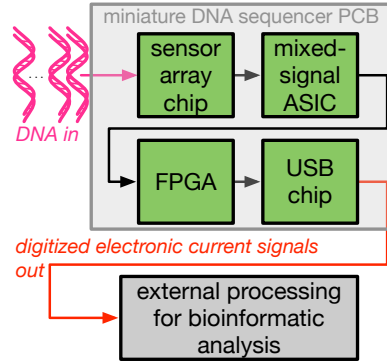


Figure 7.1: Block diagram of a miniature DNA sequencer’s main components.

A challenge to such a vision, however, is the fact that existing miniature sequencers do not presently contain any substantial embedded computing, and thus themselves do not carry out any bioinformatic analysis on the measurements they pass through their chassis. Consequently, as Fig. 7.1 shows, for any relevant analysis of DNA equivalent currents, the data must be sent to some external processing resource (e.g., desktop, laptop, cloud, etc.).

Although this circumstance has not been a major roadblock to research carried out in well equipped scientific laboratories, it has complicated field work (e.g., epidemiological research) where wireless communications can be absent and where commodity computers do not have a ready supply of power [124]. Given that on-board digital computations are many orders of magnitude more efficient than wireless transmissions of data [125], the absence of sufficiently powerful embedded computing also frustrates the future development of this technology towards mobile self-contained DNA monitoring systems [126]. In this vision, a large amount of analysis would be done internally, within the sequencing device itself, and key results or summary analyses would only intermittently be communicated to the outside via efficient low-bandwidth links.

To help advance progress towards a suitable embedded computing solution for future mobile DNA sequencing devices I present the design of a system-on-chip (SoC) for this purpose (i.e., focusing on the digital computation). To my knowledge no chip designed for such a use has yet been seriously explored or reported. The presented

chip has been realized in a 22-nm CMOS technology and experimentally evaluated for performance and energy efficiency. To maximize the utility of example for other developers I have based my construction around the open-source RISC-V instruction set architecture (ISA) and open-source component blocks.

7.3 Background

7.3.1 Rocket Core

Rocket core is open-source implementation of RISC-V ISA. Rocket Core is a 5-stage in-order processor which implements RV32G and RV64G ISAs. In RV32G and RV64G, RV stands for RISC-V, 32 or 64 stands for 32 or 64 bit instruction and G stands for general purpose instruction.

RISC-V has four main types of instruction sets: R-type, I-type, S-type and U-type shown in Fig. 7.2. R-type instruction are purely register type instruction. I-type, S-type and U-type allow for immediate values passed to the instruction. The position of operands in the instruction was chosen to make the decoding easier.

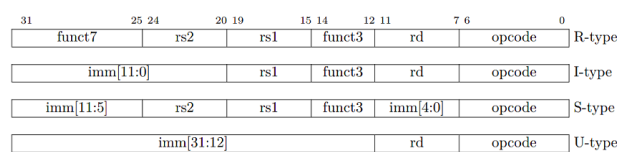


Figure 7.2: The four basic types of RISC-V instructions

One of the impressive features of RISC-V is that it allows easy implementation of a custom instruction. This can be used to extend instruction set or can also be used to implement instruction for Rocket Custom Coprocessor Interface (RoCC) based accelerator.

7.3.2 Rocket Custom Co-processor Interface

The RoCC facilitates tight integration of accelerator to processor through custom instruction. Each Rocket core can have upto four accelerator attached to it. The RoCC interface signals are grouped into two main types: default RoCC and extended RoCC. Default RoCC has three sub groups: Core Control, Register Mode and Memory Mode. Extended RoCC interface has four subgroups: Floating Point Unit (FPU), Uncached Tilelink (UTL), Control Status Register (CSR) for Linux, Page Table Walker (PTW).

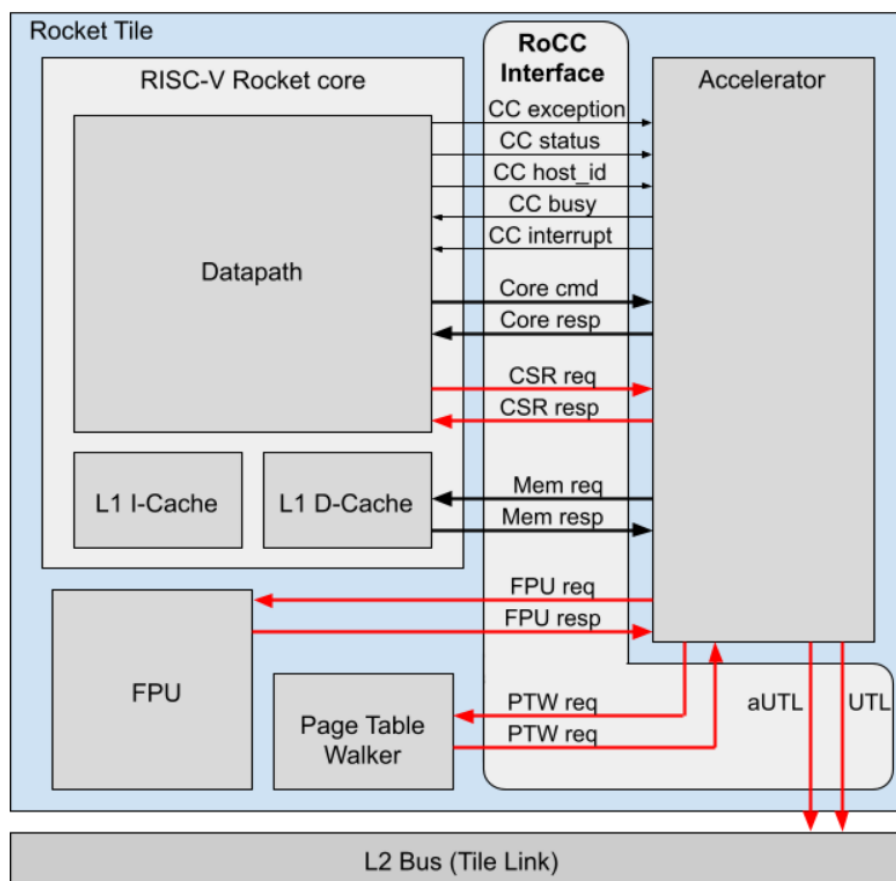


Figure 7.3: The RoCC Interface showing the default Interface (in black) and the extended Interface (in red).

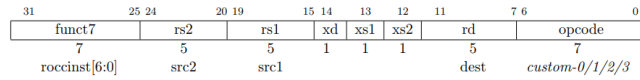


Figure 7.4: The custom instruction format

7.4 Design and Architecture

7.4.1 Specifications

Presently no formal standards have been established for miniature DNA sequencers. Nonetheless, their existing functionality and their performance levels offer practical guides for forward-looking SoC specifications. Most importantly, popular miniature sequencers can sense up to 230K DNA bases per second¹; even smaller model versions operate at a fourth of this throughput. Bases are the fine-grain representatives of the genomic information contained within each measured DNA sample. The signals indicative of sensed bases emerge from the ASIC at top rates of about 25 Mbits/s in an uninterrupted streaming fashion. These values indicate the rates that presumptive embedded SoCs targeting real-time operation should be able to ingest data and the rates at which their bioinformatic analyses should execute per measured base. Many benefits accrue if data analyses can be carried out in real-time including faster time to pathogen detection, more efficient use of sensor resources, less off-chip storage requirements, etc.

The power available for these embedded SoC calculations is an important consideration. Presently, miniature sequencers do not contain any internal battery supply and a standard device has a maximum rated power of 4.5 W with an average draw of about 1 W [28], values on-par with typical smartphone power draw. Clearly, the lower this requirement gets, the more suitable the device becomes for mobile applications. I approximate that if added computing resources use less than a tenth of nominal power, they will serve as practical additions towards future mobile applications. Therefore

¹*Bases* are the four molecular building blocks of DNA, their chemical name abbreviations being A, C, G, and T, respectively.

at present I seek SoCs that can operate below 100 mW.

The ease with which the performance and power specifications outlined above can be met depends on the complexity of functions that the SoC is asked to execute. The computational functionality of existing, sub-5-W, sequencers has not been detailed in the open literature, but operating manuals imply that it presently deals with ASIC control and I/O management [127]. Although code related to bioinformatic analysis of data gathered by miniature sequencers has been published online, it has been targeted for running on externally connected computers. This code covers a broad range of uses ranging across low-level sample filtering, through signal detection, to high-level genomic pattern extraction. The current and foreseeable state of the field therefore presents the need for an accompanying processor that can accommodate a variety of computations. In the near-term however, I expect that future embedded SoCs will most need to address methods that operate on data shortly after it has been gathered, a typical example being the detection of the base sequences present within the measured current emerging from the ASIC. This change from electronic current time-series to base sequence achieves about a 50X reduction in signal bandwidth [128]. It thus affords not only the opportunity for ensuing, higher-level, analysis, but also offers a lower-bandwidth signal that may more efficiently be transmitted to off-board computing for further processing.

The specifications outlined above influenced my high-level SoC design choices in several ways. First, I targeted work for implementation in a 22-nm CMOS technology. The speed and low-voltage potential of this process presents ample opportunities for complex low-power designs suitable for at least near-future embedded sequencing uses [78]. Its maturity also provides a significant costs savings over finer technology nodes while ongoing back-end-of-line improvements hold potential for longer-term performance benefits. Second, I decided to err on the side of flexibility and committed to including a heterogeneous processing core in SoC that facilitates easier programming via the ability to host an operating systems and support for a virtual memory scheme.

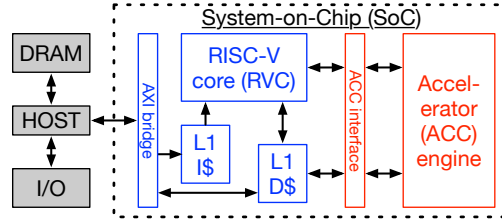


Figure 7.5: Exploratory embedded sequencing SoC organization overview.

Given the evolving repertoire of functions that miniature sequencer data may still benefit from, too early a specialization may unnecessarily preclude functionalities with reasonable chances of meeting desired performance and power specifications. Third, a demonstration of some specialized computing was necessary to examine the potential of accelerating functions suitable for miniature sequencers. To that end I settled on including extra hardware for extracting base content from electronic current data. Ultimately, this required not only efficient mapping of algorithms to hardware, but also including suitable hardware and software interfaces between the accelerator and the remaining system components. Finally, a suitable means of communicating programs and data from/to external components as may be arranged on future sequencers had to be implemented. I elaborate on these below.

7.4.2 System Organization

An overview of my exploratory SoC is shown in Fig. 7.5. Primarily, the design includes a RISC-V core (RVC) for general-purpose processing and, as noted above, an accelerator (ACC) for extracting base sequences from ASIC outputs. The SoC’s RVC adheres to the 5-stage in-order scalar microarchitecture available from within the open-source Rocket Chip generator [129]. Again, with a preference for flexibility, I adopted a 64-bit architecture for my work, included integer multiply and divide units in the datapath and retained the floating-point unit. However, I eliminated all memory and network components after the L1 cache which was implemented using SRAM macrocells and set to 32 KiB, half of the setting used in application SoC cores like the ARM Cortex A53 [130]. As discussed below, these savings was instead dedicated

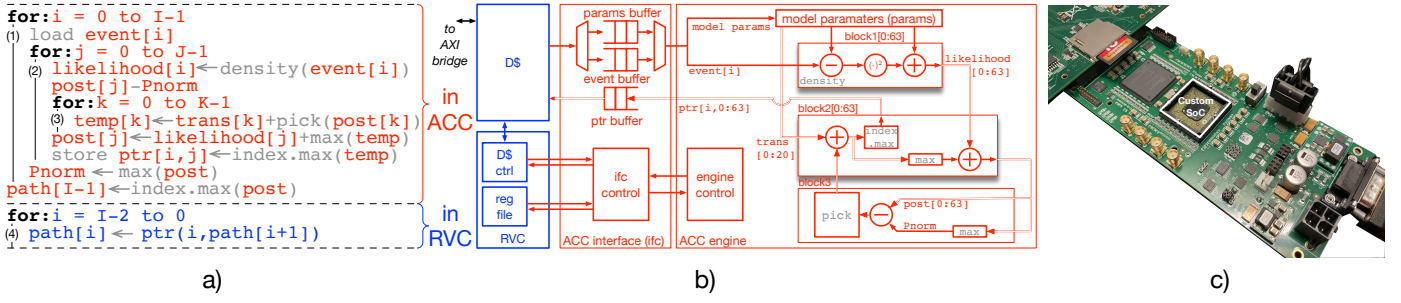


Figure 7.6: a) A bioinformatic analysis for base extraction from ASIC output, b) its implementation in ACC hardware, c) implementation of the SoC on a test board.

for the needs of the accompanying accelerator block.

The RVC and ACC are connected via the Rocket Custom Coprocessor (RoCC) [131] interface, a hardware facility amenable to RVC control via extensions to the core RISC-V ISA. Through RoCC, the ACC is programmed by instructions from user code running on the RVC. Once initiated, ACC interacts directly with system memory (through the data cache) to carry out its computations. RoCC also supports integration within the processor virtual memory space through a connection to the page table walker.

As also indicated in Fig. 7.5, RVC and ACC communications to external memory and I/O is managed by a cache coherency controller which arbitrates signals to/from the cache and also serves as an AXI4 bridge. Ensuing open-source communications components available from the BaseJump repository [132] serve to package and communicate the data off-chip using source-synchronous links. For test purposes, this data is connected to DRAM and I/O via an external host as per the tethering scheme discussed in [133]. This link is capable of working at 4.2 Gb/s and thus matches maximum USB speeds available to existing miniature DNA sequencer devices.

7.4.3 Accelerator (ACC) Design

Pseudocode for the bioinformatic analysis to which I dedicated custom ACC hardware is listed in Fig. 7.6a). The code implements a Viterbi sequence detector capable of converting a streaming time-series of `event[i]` values from ASIC (possibly pre-processed

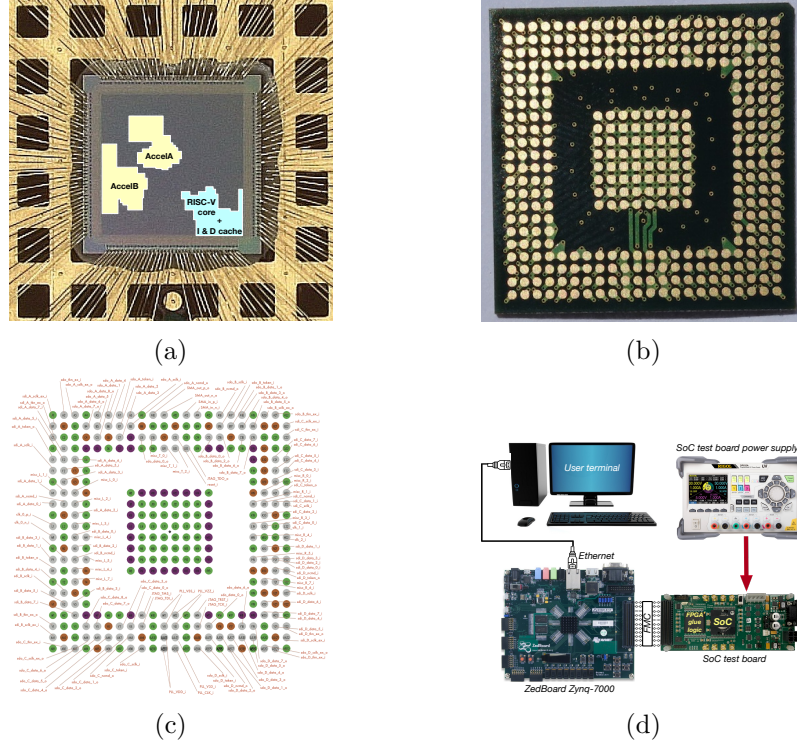


Figure 7.7: a) Micrograph of test chip with floorplan of accelerators highlighted b) Backside of the chip package showing the BGA [8] c) BGA pinout for the package [8] d) The packaged SoC within its test system.

by RVC in chunks of I event at-a-time) to an equivalent sequence of bases [134]. These bases are represented by the computed integer array `path` in Fig. 7.6a). As noted above, to accommodate peak demand in modern miniature sequencers an algorithm such as this would effectively need to produce elements `path[i]` at a rate of 230K per second. For the values adopted in this work (streaming i , $J=64$, $K=21$) maintaining this throughput requires about 350M arithmetic and memory operations per second, respectively.

The Viterbi procedure in Fig. 7.6a) consists of four loops. Loops (1)-(3) build a $J \times I$ trellis, `ptr`, cataloging the set of most likely bases to associate with `I event[i]` inputs. Based on posterior probability estimates (`post`), also computed across loops (1)-(3), loop (4) extracts the integer array, `path`, by executing a pointer chase across the `ptr` matrix. In more detail, loop (1, i sweep) loads events (partitioned into I -long chunks). For each `event[i]`, loop (2, j sweep) computes $J=64$ (log) likelihood probabilities

`likelihood[j]`. Its update to `post` and `ptr` is aided by loop (3), which makes $K=21$ new probability computations for each `j` through the addition of `trans[k]` model parameters. The 64 iterations of loop (2) reflect the 3-base sub-sequence that the analysis tries map individual `event[j]` data to, while the 21 iterations of loop (3) reflect the different ways in which sub-sequence estimates at time `i` may be related to estimates at time `i+1`.

A block diagram of my proposed accelerator (ACC) solution is shown in Fig. 7.6b). The ACC consists of two main components, the ACC engine where the analysis' computations are carried out and the ACC interface (ifc) which manages the exchange of commands and data between the RVC and the engine. The engine itself consists of three main parts, an engine control that orchestrates computations and I/O, a model parameter memory which retains additional constants like `trans` (others not shown in Fig. 7.6a)) needed to operate on the data, and the datapath blocks responsible for the core arithmetic manipulations. As indicated in Fig. 7.6b), the engine's datapath consists of three parallel and pipelined blocks (1-3). This implementation benefits from the amenability of loops (2) and (3) to full unrolling. For each `i` all computations in these inner loops can be carried out in parallel, only the need to re-use `post` calculations from one iteration of loop (1) to the next imposes dependence constraints. Specifically, the `likelihood` calculations are managed by 64 block1 units, while 64 block2 units produce `post` and `ptr` results. Block3 is responsible for normalization of `post` values to prevent overflow and then the distribution of these values via a crossbar (the `pick` function) to the appropriate block2 inputs.

The ACC implements a RoCC interface to communicate to RISC-V. The interface between the RoCC interface controller and Basecaller is shown in Fig. 7.8. The interface controller holds the scratch pad memories for temporarily storing the parameter, events data from the RISC-V and pointer data from the Basecaller. The size of the parameter buffer, event buffer and pointer data buffer is 136 bytes, 4 and 32 kbytes respectively.

The RoCC interface controller also implements state machine needed to control the RoCC interface and the basecaller. There are two main state machines. The first state machine is responsible for decoding the commands RISC-V. Fig. 7.10 shows the state machine implemented to decode the command based on their function. Table 7.2 gives the description of each state in Fig. 7.10. States s_1 - s_4 hold the function of configuring the HMM algorithm parameter in the accelerator. State s_5 gets the event data and starts basecalling operation. The controls during the state s_5 will be discussed in below implemented by second state machine. The accelerator implements six functions highlighted in Table. 7.1. These commands are used to load configuration or perform basecalling. The data is transferred using RoCC memory interface between the accelerator and L1 Cache.

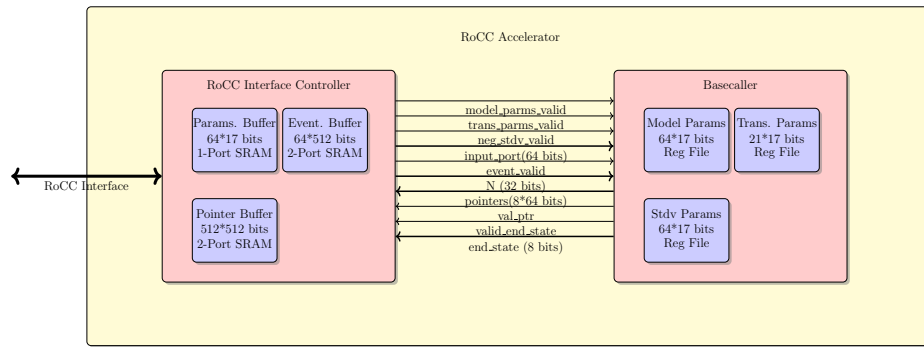


Figure 7.8: The interface between RoCC Interface Controller and Basecaller

funct	rs1	rs2	rd	Description
0	-	-	-	Reset
1	No. of events	-	-	Get number of events
2	Model param. addr.	-	-	Get model parameters
3	Trans. param. addr	-	-	Get transition parameters
4	Stad. devia. addr	-	-	Get negative standard deviations
5	Event Data Ad.	Ptr. Data Ad.	End State Ad.	Send the event & pointer address and start the BC.

Table 7.1: Custom command functions implemented by the accelerator

7.5 Implementation and Measurements

A picture of the completed and packaged 22-nm SoC, connected within its test board, is shown in Fig. 7.6c). The SoC is tethered to an external ARM processor through

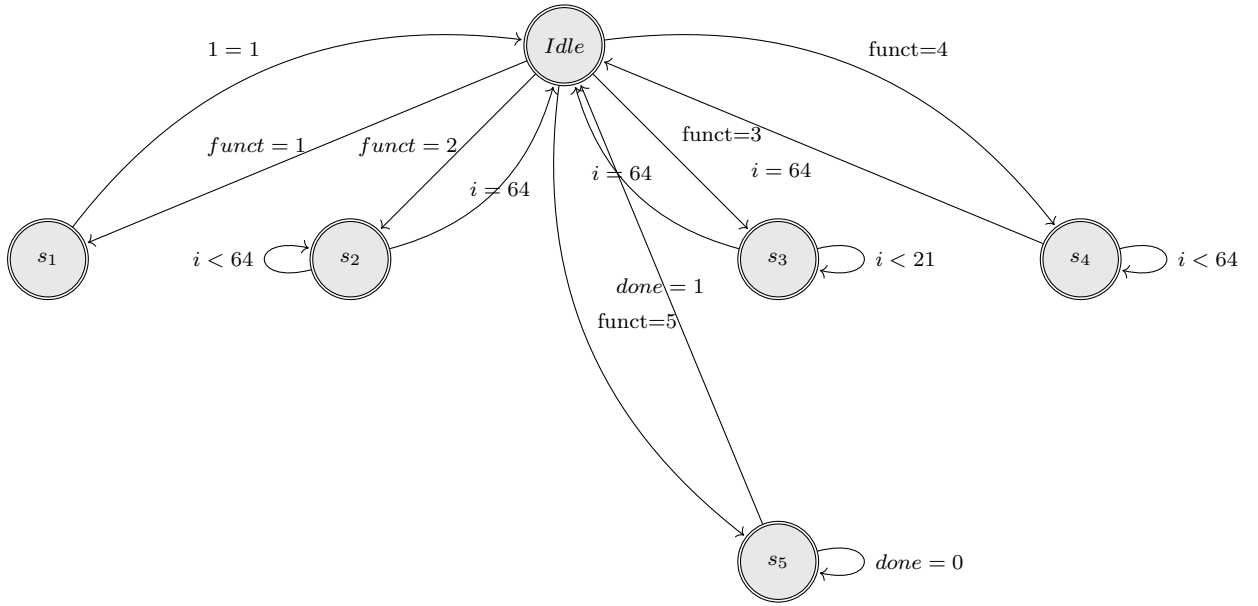


Figure 7.9: State machine for processing custom command issued to configure and execute basecaller

State	Description
<i>Idle</i>	Reset
<i>s₁</i>	Get number of events
<i>s₂</i>	Get model parameters
<i>s₃</i>	Get transition parameters
<i>s₄</i>	Get negative standard deviation parameters
<i>s₅</i>	Get ptr. address and event data address and run the basecaller

Table 7.2: State descriptions for state machine shown in Fig. 7.10

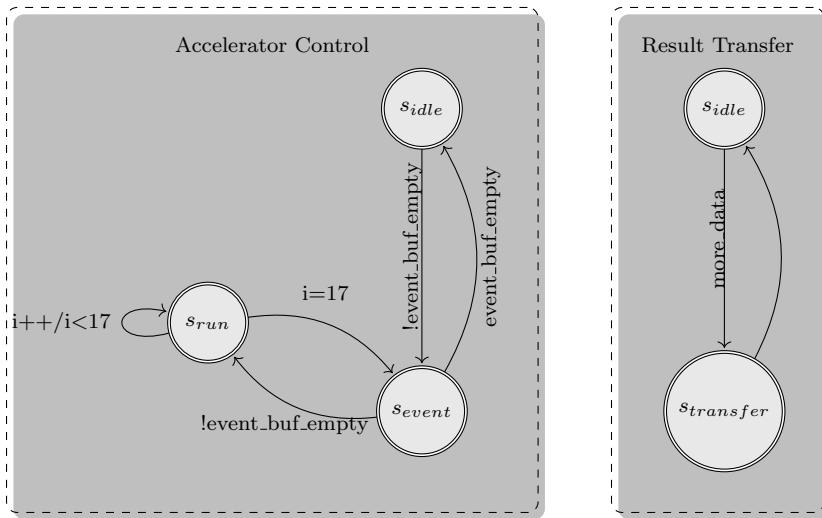


Figure 7.10: State machines for reading and writing on memory RoCC interface

which system calls are serviced and through which program and data connections to DRAM are facilitated. Basic system instructions are also carried through this link. The total area consumed by the design is evenly split between RVC and ACC which, in total, takes up 1.3 mm^2 of chip space. The chip micrograph with accelerator floorplan highlighted is shown in Fig. 7.7a). The chip was packaged on open-source package developed by BSG group [8]. Fig. 7.7b) & Fig. 7.7c) shows the backside of the package and pinout of package respectively. This package contains 352 pins. The chip is externally clocked and has been successfully tested up to 200-MHz while operating from a 0.65-V supply. Absence of on-chip clocking resources have prevented this version of the SoC from reaching higher operating speeds and simulations indicate a potential operating speed up to 1 GHz.

Nonetheless, measured head-to-head performance results demonstrate that the proposed SoC can achieve a significant speed-up, by a factor of 10X at 200 MHz, over comparable embedded system chips. Specifically, I compare my performance in terms of Kbases/second on the analysis algorithm in Fig. 7.6a) to an ARM Cortex-A53 (a 16-nm implementation present in the Xilinx XCU-106 development board)² [130]. Even with the A53 clocked at 1200 MHz, my SoC's performance maintained a 1.8X advantage, 31.0 Kbases/second for the SoC and 16.7 Kbases/second for the 1.2 GHz ARM processor.

When running at 200-MHz the power consumption of the SoC was less than 19 mW. Of this, the accelerator contributed only 1 mW while operating on the analysis in Fig. 7.6a). The minuscule overhead imposed by the accelerator bodes well for more sophisticated uses in future mobile sequencing. To underscore the potential, I consider the *efficiency* of my proposed design. I define this metric as the performance (bases/second processed) divided by the additional power (over and above quiescent power) needed to execute the computation at this rate. For the ARM A53, I measured

²Board limitations prevented running my A53 below 300-MHz. For a more convenient comparison, I present extrapolated A53 performance values based on my measurements of its performance at 300-1200 MHz.

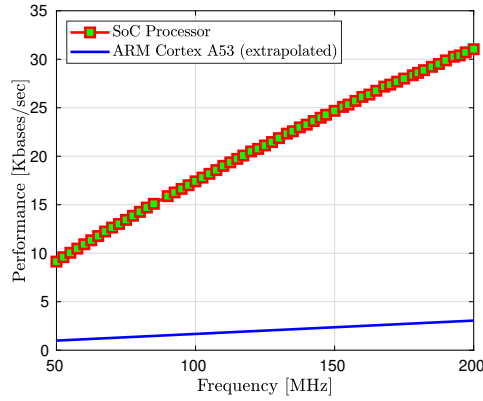


Figure 7.11: Measured basecalling speed as a function of clock frequency.

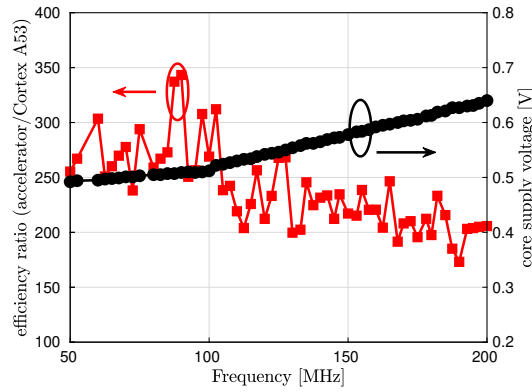


Figure 7.12: Ratio (red) of SoC efficiency to optimal ARM A53 efficiency and associated (black) minimal SoC supply voltage settings.

a best efficiency of 182 Kb/s/W at 1-GHz. I did the same for my accelerated SoC over its frequency of operation and show the SoC-to-ARM efficiency ratio (red) in Fig. 7.12. At each frequency of operation I manually sought the minimum SoC operating voltage which is also recorded in Fig. 7.12 (black). The measurement fluctuations (averages of three separate runs) present in the plot are due to varying RVC cache memory and communications block activities, but still underscore a substantial efficiency advantage of a factor of 200X.

Chapter 8

Conclusion

In this thesis, I have presented CMOS analog readout arrays and a embedded digital accelerator system to optimize the cost, speed, and size of nanopore based sequencers. Lowering the cost of sequencing to under \$ 100 without need for initial large capital investments is essential to democratizing DNA sequencing. This will open various avenues in medical diagnostics and personalized medicine, improving the lives of billions of people.

8.1 Contributions

8.1.1 DROIC

To readout pico-ampere currents of the type encountered in practical nanopore-based DNA sequencers, ultra-high gain amplifiers are needed. The ultra-high gain of transimpedance amplifiers makes them sensitive to digital noise and leakage currents. Two versions of the analog readout array consisting of amplifiers and ADCs have been implemented. The first version consists of 30 channels, while the second version has 106 channels.

- **DROICv1 in-pixel ADC based array:** I presented an 30 channel in-pixel architecture along with parallel and serial readout modes. The performance of an

Table 8.1: Performance comparison with state-of-art nanopore arrays and amplifiers

	This Work - Sync	This Work - Async	MinION,'14	[23], '12	[30], '16	[27], '14	[83], '12 ¹	[24], '09	[89], '16
Technology	0.13 μm	0.13 μm	-	0.18 μm	0.18 μm	0.35 μm	0.5 μm	0.35 μm	.18 μm
Supply Voltage	1.2 V	1.2 V	-	1.5 V	1.5 V	3.3 V	3.3 V	3.3 V	1.8 V
No. of Channels	106	106	512	4	25	1	2	1	1
Power/Channel	340 μW	700 μW	2 mW	4.5 mW	5.1 mW	40 mW	1.5 mW	-	5.22 mW
Bandwidth	0-7.87 kHz	0-23 kHz	0-4 kHz	0-1 MHz	0-1MHz	0-10 kHz	0-10 kHz	0-1 MHz	0-10 kHz
Channel Area	0.054 mm^2	0.054 mm^2	0.5 mm^2	0.25 mm^2	0.16 mm^2	-	0.13 mm^2	0.35 mm^2	0.0912 mm^2
Input-Ref. Noise	~ 1.5 pArms	~ 1.5 pArms	~ 1.5 pArms	~ 155 pArms	~ 129.4 pArms	1.2 pArms	2.44 pArms	-	1.25 pArms
Noise Floor	4.5 fA/ $\sqrt{\text{Hz}}$ @ 10 kHz	7 fA/ $\sqrt{\text{Hz}}$ @ 30 kHz	-	~ 31 fA/ $\sqrt{\text{Hz}}$	~ 31 fA/ $\sqrt{\text{Hz}}$	6 fA/ $\sqrt{\text{Hz}}$	5 fA/ $\sqrt{\text{Hz}}$	6 fA/ $\sqrt{\text{Hz}}$	11.6 fA/ $\sqrt{\text{Hz}}$
Input Capacitance	2 pF	2 pF	2 pF	3 pF	10 pF	3 pF	-	0 pF	0 pF
Integrated ADC	Yes	Yes	Yes	No	No	Yes	No	No	No

amplifier (and ADC) can be quantified using “throughput density”. Throughput density is the speed of sequencing (bp/s) per sq. mm of chip area at a particular signal to noise ratio (SNR). The system has an SNR of 20 dB for 7.87 kSps bandwidth. This means the DNA can translocate at 787 bp/s through the nanopore (considering a ten times higher sampling rate). The throughput density of the chip at an SNR of 20 dB is 11.1 kbp/s/mm^2 ($787 \text{ bp/s} \cdot (1/0.075 (1/\text{mm}^2)) = 11.1 \text{ kbp/s/mm}^2$). Hence, there is an improvement of ~ 6.5 fold compared to state-of-art Oxford Nanopore Technologies chip.

- DROICv3 column ADC based array:** To improve the throughput density of the DROICv1 array, I implemented column ADC based DROIC. It contains 106 channels, the largest array for nanopore-based sequencing presented in any open literature. For each column, an ADC is connected to four TIAs via an analog multiplexer. This reduced the equivalent area of the channel from 0.075mm^2 to 0.0542mm^2 . Hence, improving the throughput density to 14.5 kbp/s/mm^2 and ~ 6.5 fold compared to state-of-art ONT’s chip. The ultra-gain amplifiers are sensitive to leakage current. In technology with a 1.2 V power supply, these leakage currents can easily saturate the amplifiers. To further improve the accuracy of measurements and boost the reliability of array, I have also presented a coarse offset correction and LMS based offset & gain correction algorithm. It cancels the offsets caused by the leakage current and corrects the gain of each channel.

- Asynchronous Amplifier based Array:** To improve the bandwidth of the

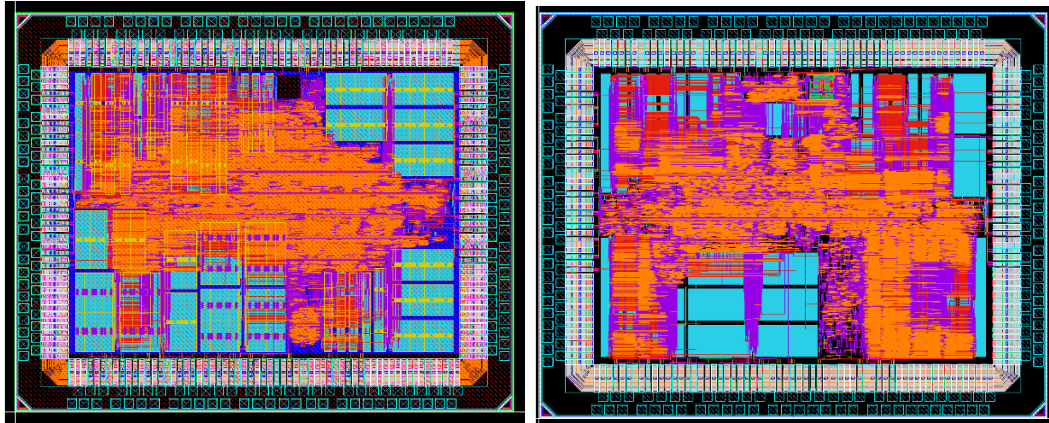
amplifier and further boost the throughput density, I presented an asynchronous amplifier based on digital differentiator. Using asynchronous reset technique, the noise floor is reduced to $14 \text{ fA}/\sqrt{Hz}$ at 23 kSps sample rate for an 2 pF input capacitance. Previous attempts at such an amplifier were made in all- analog domain consuming much higher area and power (area of 4.5 mm^2 per channel while consuming 41 mW). My implementation consumes 0.7 mW with an area of 0.0542 mm^2 . This makes such an implementation feasible in a large readout array. This gain in area and noise performance boosts the throughput density to 42.4 kbp/s/mm^2 by a factor of 25x compared to ONT’s system.

- **Biological Ion-channel Measurements:** To validate the functionality of the amplifier, biological ion-channel measurements were performed. I presented noise measurements for lipid bilayer created on a Teflon aperture. I also presented a measurement of the activity of the gramicidin channel.
- **Solid-state Noise Measurements:** Furthermore, the amplifiers were also validated with a solid-state nanopore substrate. Noise measurements were done on substrates with different input capacitance.
- **Electrode Fabrication On-Chip:** The top metal layer in standard CMOS process is made of aluminum. Aluminum forms a capacitive interface with the fluid, and hence cannot be used for ion-channel measurements. Therefore, I have presented a process for fabricating on-chip Ag/AgCl electrodes using etching and electroplating.

8.1.2 Digital Backend Basecaller

- **RISC-V based Accelerated Basecaller:** A mobile DNA sequencing solution requires an energy-efficient and sophisticated computing device co-located with the DNA sensing and measurement hardware. For this purpose, I present a highly energy efficient RISC-V 64-bit application system taped-out in Global-

Foundries 22-nm FDX technology. Among its ability to process generic programs in realtime my system incorporate a specific bioinformatics accelerator. Evaluating the efficiency of the proposed application processor relative to published basecalling solutions is another essential part of my analysis. The comparison emphasizes the superiority of my proposed basecalling processor with respect to other existing implementations. It is worth mentioning that, to the best of my knowledge, my solution was found to be the only embedded basecalling implementation until writing this article. My proposed processor has surpassed the performance-per-watt compared to ARM A53 by a factor of 200X while achieving a 10X boost in clock-normalized performance. This comparison confirms that my basecalling processor strikes a relatively better balance between performance and energy consumption compared to existing solutions.



(a) Arctic - Dual core RISC-V with systolic array (b) Abacus - Quad Core RISC-V with systolic array, sequence aligner and analog circuits

Figure 8.1: Layout of following chips developed with digital design framework

- **Framework for Future Accelerator Systems:** The RISC-V-based accelerator system that I have presented is a silicon-proven framework for much more sophisticated systems. This will significantly reduce the effort needed to build accelerated digital systems, allowing more focus to be put on the accelerators themselves. Two chips have already been taped out based on this framework. The first chip, Arctic, contains two RISC-V cores with a systolic array for ac-

celerated neural network inference. The second chip, Abacus, contains four RISC-V cores with a systolic array, a sequence aligner, and analog circuits for DNA sequencing. The layout of both chips is shown in Fig. 8.1.

8.2 Publications

- Y. Dawji, M. Habibi, E. Ghafar-Zadeh and S. Magierowski, "A Scalable Discrete-Time Integrated CMOS Readout Array for Nanopore Based DNA Sequencing," in **IEEE Access Journal**
- Y. Dawji, Z. Wu, A. Beyene, K. Hammad, E. Ghafar-Zadeh and S. Magierowski, "An SoC Design for Future Mobile DNA Detection," in **IEEE Embedded Systems Letters**
- Y. Dawji, E. Ghafar-Zadeh and S. Magierowski, "Ion-channel Readout Array" **In preparation (IEEE SENSORS Journal)**
- Abel Beyene, Z. Wu, Y. Dawji, K. Hammad and S. Magierowski, "A High-Efficiency SoC for Next-Generation Mobile IoT DNA Sequencing" **Submitted (IEEE Transactions on Consumer Electronics)**
- Y. Dawji et al., "A 65-nm CMOS Low-Power Front-End for 3rd Generation DNA Sequencing," **2019 IEEE SENSORS**
- Nanopore-based DNA sequencing sensors and CMOS readout approaches - Mehdi Habibi, Yunus Dawji, Ebrahim Ghafar-Zadeh, Sebastian Magierowski - **Sensor Review**
- Z. Wu, K. Hammad, A. Beyene, Y. Dawji, E. Ghafar-Zadeh and S. Magierowski, "An FPGA Implementation of A Portable DNA Sequencing Device Based on RISC-V," **2022 20th IEEE Interregional NEWCAS Conference (NEW-CAS)**
- Z. Wu, K. Hammad, Y. Dawji, E. Ghafar-Zadeh and S. Magierowski, "Hardware Accelerated DNA Sequencing," **2018 IEEE 61st International Midwest**

Symposium on Circuits and Systems (MWSCAS)

- S. Atiwa, Y. Dawji, A. Refaey and S. Magierowski, "Accelerated Hardware Implementation of BLAKE2 Cryptographic Hash for Blockchain," **2020 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)**

8.3 Future Work

- **Improve Throughput Density and Reducing Area by using Digital CDS** - To future improve throughput density, the front-end can be implemented by integrator, LPF and S&H. The second amplifier can be removed and CDS can be performed in the digital domain by subtracting consecutive digital samples. Increasing the ADC resolution to 12 bit and speed of conversion can improve the performance in the context of large readout arrays.
- **Implement On-chip Offset Cancellation** - A method for offset cancellation has been proposed in [27]. This method relies on an adjustment of the integrator bias voltage and is implemented in technology with 3.3 V supply. This method does not provide enough range in technology with 1.2 V supply. The offset can be canceled using an active giga-ohm resistor shown in [135] and a DAC to generate voltage for the active resistor.
- **On-chip well fabrication using SU-8** - Adding SU-8 wells on the chip with automated ion channel fabrication can allow for more complicated experiments.

Bibliography

- [1] Jay Shendure, Shankar Balasubramanian, George M. Church, Walter Gilbert, Jane Rogers, Jeffery A. Schloss, and Robert H. Waterston. Dna sequencing at 40: past, present and future. Nature, 550(7676):345–353, 2017. ISSN 1476-4687. doi: 10.1038/nature24286. URL <https://doi.org/10.1038/nature24286>.
- [2] David A Fish and Steven Paul White. Apparatus and methods for measuring an electrical current, May 24 2018. US Patent App. 15/573,332.
- [3] The isc9717 roic is novel in its design flexibility, digital output, compatibility with various flat panel arrays and solid- state detectors materials (selenium, cesium iodide, silicon, amorphous silicon, gallium arsenide, and cadmium zinc. 2004. URL <https://api.semanticscholar.org/CorpusID:219953157>.
- [4] Sophie Demarche, Kaori Sugihara, Tomaso Zambelli, Louis Tiefenauer, and Janos Vörös. Techniques for recording reconstituted ion channels. Analyst, 136:1077–1089, 2011. doi: 10.1039/C0AN00828A. URL <http://dx.doi.org/10.1039/C0AN00828A>.
- [5] Kei Funakoshi, Hiroaki Suzuki, and Shoji Takeuchi. Lipid bilayer formation by contacting monolayers in a microfluidic device for membrane protein analysis. Analytical Chemistry, 78(24):8169–8174, Dec 2006. ISSN 0003-2700. doi: 10.1021/ac0613479. URL <https://doi.org/10.1021/ac0613479>.
- [6] Sebastian Magierowski, Yiyun Huang, Chengjie Wang, and Ebrahim Ghafar-

- Zadeh. Nanopore-CMOS interfaces for DNA sequencing. Biosensors, 6(3), 2016. ISSN 2079-6374. doi: 10.3390/bios6030042. URL <https://www.mdpi.com/2079-6374/6/3/42>.
- [7] Hesham Omran, Muhammad Arsalan, and Khaled N. Salama. An integrated energy-efficient capacitive sensor digital interface circuit. Sensors and Actuators A: Physical, 216:43 – 51, 2014. ISSN 0924-4247. doi: <https://doi.org/10.1016/j.sna.2014.04.035>. URL <http://www.sciencedirect.com/science/article/pii/S0924424714002180>.
- [8] Bespoke Silicon Group. BaseJump: Building the DNA For Open Source ASIC Systems. <https://bjump.org>, 2023.
- [9] Julian Koch, Silvan Gantenbein, Kunal Masania, Wendelin J. Stark, Yaniv Erlich, and Robert N. Grass. A dna-of-things storage architecture to create materials with embedded memory. Nature Biotechnology, 38(1):39–43, 2020. ISSN 1546-1696. doi: 10.1038/s41587-019-0356-z. URL <https://doi.org/10.1038/s41587-019-0356-z>.
- [10] Leroy Hood and David Galas. The digital code of dna. Nature, 421(6921): 444–448, 2003. ISSN 1476-4687. doi: 10.1038/nature01410. URL <https://doi.org/10.1038/nature01410>.
- [11] Artem E. Men, Peter Wilson, Kirby Siemering, and Susan Forrest. Sanger DNA Sequencing, chapter 1, pages 1–11. John Wiley & Sons, Ltd, 2008. ISBN 9783527625130. doi: 10.1002/9783527625130.ch1. URL <https://onlinelibrary.wiley.com/doi/abs/10.1002/9783527625130.ch1>.
- [12] Sara Goodwin, John D. McPherson, and W. Richard McCombie. Coming of age: ten years of next-generation sequencing technologies. Nature Reviews Genetics, 17(6):333–351, 2016. ISSN 1471-0064. doi: 10.1038/nrg.2016.49. URL <https://doi.org/10.1038/nrg.2016.49>.

- [13] Cliff Meldrum, Maria A. Doyle, and Richard W. Tothill. Next-generation sequencing for cancer diagnostics: a practical perspective. The Clinical biochemist. Reviews, 32(4):177–195, Nov 2011. ISSN 1838-0212. URL <https://pubmed.ncbi.nlm.nih.gov/22147957>. PMC3219767[pmcid].
- [14] J. M. Rothberg et al. An integrated semiconductor device enabling non-optical genome sequencing. Nature, 475(7356):348–352, July 2011.
- [15] Jerzy K. Kulski. Next-generation sequencing — an overview of the history, tools, and “omic” applications. Open Access pear reviewed chapter, 8(2):278–292, Jan 2016. ISSN 1932-4545. doi: 10.1109/TBCAS.2013.2262998.
- [16] Clive G Brown and James Clarke. Nanopore development at Oxford Nanopore. Nature Biotechnology, 34(8):810–811, Aug 2016.
- [17] Alexander S. Mikheyev and Mandy M. Y. Tin. A first look at the oxford nanopore minion sequencer. Molecular Ecology Resources, 14(6):1097–1102, 2014. doi: 10.1111/1755-0998.12324. URL <https://onlinelibrary.wiley.com/doi/abs/10.1111/1755-0998.12324>.
- [18] G. Church, D. W. Deamer, D. Branton, R. Baldarelli, and J. Kasianowicz. Characterization of individual polymer molecules based on monomer-interface interactions, Aug. 1998. Filed: Mar. 17, 1995.
- [19] John J. Kasianowicz, Eric Brandin, Daniel Branton, and David W. Deamer. Characterization of individual polynucleotide molecules using a membrane channel. Proceedings of the National Academy of Sciences, 93(24):13770–13773, 1996. ISSN 0027-8424. doi: 10.1073/pnas.93.24.13770. URL <https://www.pnas.org/content/93/24/13770>.
- [20] Brown CG. Oxford nanopore technologies: a wafer thin update. 4, 2016.

- [21] Camilla L.C. Ip, Matthew Loose, John R. Tyson, Mariateresa de Cesare, Bonnie L. Brown, Miten Jain, Richard M. Leggett, David A. Eccles, Vadim Zalunin, John M. Urban, Paolo Piazza, Rory J. Bowden, Benedict Paten, Solomon Mwaigwisya, Elizabeth M. Batty, Jared T. Simpson, Terrance P. Snutch, Ewan Birney, David Buck, Sara Goodwin, Hans J. Jansen, Justin O'Grady, and Hugh E. Olsen and. MinION analysis and reference consortium: Phase 1 data release and analysis. F1000Research, 4:1075, October 2015. doi: 10.12688/f1000research.7201.1. URL <https://doi.org/10.12688/f1000research.7201.1>.
- [22] Antonio Canas and Simon Adrian Wells. Lipid bilayer sensor array, Sep. 2014.
- [23] J. K. Rosenstein, M. Wanunu, C. A. Merchant, M. Drndic, and K. L. Shepard. Integrated nanopore sensing platform with sub-microsecond temporal resolution. Nat. Methods, 9(5):487–492, May 2012.
- [24] G. Ferrari, F. Gozzini, A. Molari, and M. Sampietro. Transimpedance amplifier for high sensitivity current measurements on nanodevices. IEEE J. Solid-State Circuits, 44(5):1609–1616, May 2009.
- [25] G. Ferrari, M. Farina, F. Guagliardo, M. Carminati, and M. Sampietro. Ultra-low-noise cmos current preamplifier from dc to 1 mhz. Electronics Letters, 45(25):1278–1280, December 2009. ISSN 0013-5194. doi: 10.1049/el.2009.2353.
- [26] Marco Crescentini, Marco Tartagni, Hywel Morgan, and Pier Andrea Traverso. A compact low-noise broadband digital picoammeter architecture. Measurement, 100:194–204, 1 2017. doi: 10.1016/j.measurement.2016.12.040.
- [27] M. Crescentini, M. Bennati, M. Carminati, and M. Tartagni. Noise limits of cmos current interfaces for biosensors: A review. IEEE Transactions on Biomedical Circuits and Systems, 8(2):278–292, April 2014. ISSN 1932-4545. doi: 10.1109/TBCAS.2013.2262998.

- [28] James Clarke. Development of multipore sequencing instruments. In Nanopore Sequencing: An Introduction, chapter 6, pages 75–89. World Scientific, 2019.
- [29] J. Clarke, H.-C. Wu, L. Jayasinghe, A. Patel, S. Reid, and H. Bayley. Continuous base identification for single-molecule nanopore DNA sequencing. Nat. Nanotech., 4:265–270, Apr. 2009.
- [30] Siddharth Shekar, David J. Niedzwiecki, Chen-Chi Chien, Peijie Ong, Daniel A. Fleischer, Jianxun Lin, Jacob K. Rosenstein, Marija Drndić, and Kenneth L. Shepard. Measurement of dna translocation dynamics in a solid-state nanopore at 100 ns temporal resolution. Nano Letters, 16(7):4483–4489, 2016. doi: 10.1021/acs.nanolett.6b01661. URL <https://doi.org/10.1021/acs.nanolett.6b01661>. PMID: 27332998.
- [31] S. W. Kowalczyk, A. Y. Grosberg, Y. Rabin, and C. Dekker. Modeling the conductance and DNA blockade of solid-state nanopores. Nanotechnology, 22: 1–5, July 2011.
- [32] G. R. Willmott and B. G. Smith. Comment on ’modeling the conductance and DNA blockade of solid-state nanopores’. Nanotechnology, 23:1, Feb. 2012.
- [33] S. W. Kowalczyk, A. Y. Grosberg, Y. Rabin, and C. Dekker. Reply to comment on ’modeling the conductance and DNA blockade of solid-state nanopores’. Nanotechnology, 23:1, Feb. 2012.
- [34] K. Venta, G. Shemer, M. Puster, J. A. Rodriguez-Manzo, A. Balan, J. K. Rosenstein, K. Shepard, and M. Drndic. Differentiation of short, single-stranded DNA homopolymers in solid-state nanopores. ACS Nano, 7(5):4629–4636, May 2013.
- [35] Michael Zwolak and Massimiliano Di Ventra. Electronic signature of dna nucleotides via transverse transport. Nano Letters, 5(3):421–424, 2005. doi:

- 10.1021/nl048289w. URL <https://doi.org/10.1021/nl048289w>. PMID: 15755087.
- [36] Jariyane Prasongkit, Anton Grigoriev, Biswarup Pathak, Rajeev Ahuja, and Ralph H. Scheicher. Transverse conductance of dna nucleotides in a graphene nanogap from first principles. *Nano Letters*, 11(5):1941–1945, May 2011. ISSN 1530-6984. doi: 10.1021/nl200147x.
- [37] M. Di Ventura and M. Taniguchi. Decoding DNA, RNA and peptides with quantum tunnelling. *Nat. Nanotech.*, 11:117–126, Feb. 2016.
- [38] Makusu Tsutsui, Masateru Taniguchi, Kazumichi Yokota, and Tomoji Kawai. Identifying single nucleotides by tunnelling current. *Nature Nanotechnology*, 5: 286–290, Mar 2010. URL <https://doi.org/10.1038/nnano.2010.42>.
- [39] Shuo Huang, Jin He, Shuai Chang, Peiming Zhang, Feng Liang, Shengqin Li, Michael Tuchband, Alexander Fuhrmann, Robert Ros, and Stuart Lindsay. Identifying single bases in a dna oligomer with electron tunnelling. *Nature Nanotechnology*, 5:868–873, Nov 2010. URL <https://doi.org/10.1038/nnano.2010.213>.
- [40] Aleksandar P. Ivanov, Emanuele Instuli, Catriona M. McGilvery, Geoff Baldwin, David W. McComb, Tim Albrecht, and Joshua B. Edel. Dna tunneling detector embedded in a nanopore. *Nano Letters*, 11(1):279–285, 2011. doi: 10.1021/nl103873a. URL <https://doi.org/10.1021/nl103873a>. PMID: 21133389.
- [41] Yi Cui, Qingqiao Wei, Hongkun Park, and Charles M. Lieber. Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species. *Science*, 293(5533):1289–1292, 2001. ISSN 0036-8075. doi: 10.1126/science.1062711. URL <http://science.sciencemag.org/content/293/5533/1289>.

- [42] P. Bergveld. Development of an ion-sensitive solid-state device for neurophysiological measurements. IEEE Trans. Biomed. Eng., 17:70–71, 1970.
- [43] Tammie Nelson, Bo Zhang, and Oleg V. Prezhdo. Detection of nucleic acids with graphene nanopores: Ab initio characterization of a novel sequencing device. Nano Letters, 10(9):3237–3242, 2010. doi: 10.1021/nl9035934. URL <https://doi.org/10.1021/nl9035934>. PMID: 20722409.
- [44] Ping Xie, Qihua Xiong, Ying Fang, Quan Qing, and Charles M. Lieber. Local electrical potential detection of dna by nanowire-nanopore sensors. Nature Nanotechnology, 7(2):119–125, Feb 2012. URL <https://doi.org/10.1038/nnano.2011.217>.
- [45] F. Traversi, C. Raillon, S. M. Benameur, K. Liu, S. Khlybov, M. Tosun, D. Krasnozhan, A. Kis, and A. Radenovic. Detecting the translocation of dna through a nanopore using graphene nanoribbons. Nature Nanotechnology, 8(12):939–945, Dec 2013. URL <https://doi.org/10.1038/nnano.2013.240>. Article.
- [46] William M. Parkin and Marija Drndić. Signal and noise in fet-nanopore devices. ACS Sensors, 3(2):313–319, 2018. doi: 10.1021/acssensors.7b00708. URL <https://doi.org/10.1021/acssensors.7b00708>. PMID: 29322780.
- [47] Elaine R. Mardis. Dna sequencing technologies: 2006-2016. Nature Protocols, 12(2):213–218, Feb 2017. URL <https://doi.org/10.1038/nprot.2016.182>. Perspective.
- [48] Jay Shendure, Shankar Balasubramanian, George M. Church, Walter Gilbert, Jane Rogers, Jeffery A. Schloss, and Robert H. Waterston. Dna sequencing at 40: past, present and future. Nature, 550(7676):345–353, Oct 2017. URL <https://doi.org/10.1038/nature24286>. Review Article.

- [49] Gautam V. Soni and Amit Meller. Progress toward ultrafast dna sequencing using solid-state nanopores. Clinical Chemistry, 53(11):1996–2001, 2007. ISSN 0009-9147. doi: 10.1373/clinchem.2007.091231. URL <http://clinchem.aaccjnls.org/content/53/11/1996>.
- [50] Ben McNally, Alon Singer, Zhiliang Yu, Yingjie Sun, Zhiping Weng, and Amit Meller. Optical recognition of converted dna nucleotides for single-molecule dna sequencing using nanopore arrays. Nano Letters, 10(6):2237–2244, 2010. doi: 10.1021/nl1012147. URL <https://doi.org/10.1021/nl1012147>. PMID: 20459065.
- [51] Shuo Huang, Mercedes Romero-Ruiz, Oliver K. Castell, Hagan Bayley, and Mark I. Wallace. High-throughput optical sensing of nucleic acids in a nanopore array. Nature Nanotechnology, 10(11):986–991, Nov 2015. URL <https://doi.org/10.1038/nnano.2015.189>. Article.
- [52] Daniel V. Verschuere, Sergii Pud, Xin Shi, Lorenzo De Angelis, L. Kuipers, and Cees Dekker. Label-free optical detection of dna translocations through plasmonic nanopores. ACS Nano, pages 1–10, Dec 2018. doi: 10.1021/acsnano.8b06758. URL <https://doi.org/10.1021/acsnano.8b06758>.
- [53] Xin Shi, Daniel V. Verschuere, and Cees Dekker. Active delivery of single dna molecules into a plasmonic nanopore for label-free optical sensing. Nano Letters, 18(12):8003–8010, 2018. doi: 10.1021/acs.nanolett.8b04146. URL <https://doi.org/10.1021/acs.nanolett.8b04146>.
- [54] Miten Jain, Sergey Koren, Karen H. Miga, Josh Quick, Arthur C. Rand, Thomas A. Sasani, John R. Tyson, Andrew D. Beggs, Alexander T. Dilthey, Ian T. Fiddes, Sunir Malla, Hannah Marriott, Tom Nieto, Justin O’Grady, Hugh E. Olsen, Brent S. Pedersen, Arang Rhie, Hollian Richardson, Aaron R. Quinlan, Terrance P. Snutch, Louise Tee, Benedict Paten, Adam M. Phillippy,

- Jared T. Simpson, Nicholas J. Loman, and Matthew Loose. Nanopore sequencing and assembly of a human genome with ultra-long reads. Nature Biotechnology, 36(4):338–345, Apr 2018. URL <https://doi.org/10.1038/nbt.4060>.
- [55] Stefan Howorka. Building membrane nanopores. Nature Nanotechnology, 12(6): 619–630, Jul 2017. URL <https://doi.org/10.1038/nnano.2017.99>. Review Article.
- [56] L. Z. Song, M. R. Hobaugh, C. Shustack, S. Cheley, H. Bayley, and J. E. Gouaux. Structure of staphylococcal alpha-hemolysin, a heptameric transmembrane pore. Science, 274:1859–1866, 1996.
- [57] I. M. Derrington, T. Z. Butler, M. D. Collins, E. Manrao, M. Pavlenok, M. Niederweis, and J. H. Gundlach. Nanopore DNA sequencing with MspA. Proc. Natl. Acad. Sci., 107(37):16060–16065, Sept. 2010.
- [58] P. Goyal, P. V. Krasteva, N. Van Gerven, F. Gubellini, et al. Structural and mechanistic insights into the bacterial amyloid secretion channel CsgG. Nature, 516(7530):250–253, Dec 2014.
- [59] Stefan Howorka, Han Remaut, Lakmal Jayasinghe, E Jayne Wallace, James Anthony Clarke, Richard George Hambley, and Jonathan Bankes Pugh. Mutant CsgG Pores, Oct 2017.
- [60] David Stoddart, Giovanni Maglia, Ellina Mikhailova, Andrew J. Heron, and Hagan Bayley. Multiple base-recognition sites in a biological nanopore: two heads are better than one. Angew Chem Int Ed Engl, 49(3):556–559, 2010. ISSN 1521-3773. doi: 10.1002/anie.200905483. URL <https://www.ncbi.nlm.nih.gov/pubmed/20014084>. PMC3128935[pmcid].

- [61] Lakmal Jayasinghe, E Jayne Wallace, and PratikRaj Singh. Modified Nanopores, Compositions Comprising the Same, and Uses Thereof, Aug 2018.
- [62] Lakmal Jayasinghe, E Jayne Wallace, PratikRaj Singh, Richard George Hambley, Michael Jordan, and Han Remaut. Transmembrane Pore Consisting of Two CsgG Pores, Nov 2018.
- [63] Daniel Fologea, James Uplinger, Brian Thomas, David S. McNabb, and Jiali Li. Slowing dna translocation in a solid-state nanopore. Nano Letters, 5(9): 1734–1737, 2005. doi: 10.1021/nl051063o. URL <https://doi.org/10.1021/nl051063o>. PMID: 16159215.
- [64] Sergii Pud, Shu-Han Chao, Maxim Belkin, Daniel Verschueren, Teun Huijben, Casper van Engelenburg, Cees Dekker, and Aleksei Aksimentiev. Mechanical trapping of DNA in a double-nanopore system. Nano Lett, 16(12):8021–8028, Dec 2016. ISSN 1530-6992. doi: 10.1021/acs.nanolett.6b04642. URL <https://www.ncbi.nlm.nih.gov/pubmed/27960493>. PMC5523128[pmcid].
- [65] Paolo Cadinu, Giulia Campolo, Sergii Pud, Wayne Yang, Joshua B. Edel, Cees Dekker, and Aleksandar P. Ivanov. Double barrel nanopores as a new tool for controlling single-molecule transport. Nano Letters, 18(4):2738–2745, 2018. doi: 10.1021/acs.nanolett.8b00860. URL <https://doi.org/10.1021/acs.nanolett.8b00860>. PMID: 29569930.
- [66] Xu Liu, Yuning Zhang, Roland Nagel, Walter Reisner, and William B. Dunbar. Controlling DNA Tug-of-War in a Dual Nanopore Device. arXiv e-prints, art. arXiv:1811.11105, Nov 2018.
- [67] J. A. Rodriguez-Manzo, M. Puster, A. Nicolai, V. Meunier, and M. Drndic. DNA translocation in nanometer thick silicon nanopores. ACS Nano, 9(6): 6555–6564, June 2015.

- [68] Tal Gilboa, Adam Zrehen, Arik Girsault, and Amit Meller. Optically-monitored nanopore fabrication using a focused laser beam. Scientific Reports, 8(1):9765, 2018. doi: 10.1038/s41598-018-28136-z. URL <https://doi.org/10.1038/s41598-018-28136-z>.
- [69] Hirohito Yamazaki, Rui Hu, Qing Zhao, and Meni Wanunu. Photothermally assisted thinning of silicon nitride membranes for ultrathin asymmetric nanopores. ACS Nano, 12(12):12472–12481, 2018. doi: 10.1021/acsnano.8b06805. URL <https://doi.org/10.1021/acsnano.8b06805>. PMID: 30457833.
- [70] Harold Kwok, Kyle Briggs, and Vincent Tabard-Cossa. Nanopore fabrication by controlled dielectric breakdown. PLoS One, 9(3):e92880–e92880, Mar 2014. ISSN 1932-6203. doi: 10.1371/journal.pone.0092880. URL <https://www.ncbi.nlm.nih.gov/pubmed/24658537>. PONE-D-13-51563[PII].
- [71] Yuning Zhang, Yoichi Miyahara, Nassim Derriche, Wayne Yang, Khadija Yazda, Zezhou Liu, Peter Grutter, and Walter Reisner. Nanopore fabrication via tip-controlled local breakdown using an atomic force microscope. arXiv e-prints, art. arXiv:1901.07071, Jan 2019.
- [72] C. A. Merchant, K. Healy, M. Wanunu, V. Ray, N. Peterman, J. Bartel, M. D. Fischbein, K. Venta, Z. Luo, A. T. C. Johnson, and M. Drndic. DNA translocation through graphene nanopores. Nano Lett., 10(8):4916–4924, July 2010.
- [73] Grégory F. Schneider, Stefan W. Kowalczyk, Victor E. Calado, Grégory Pandraud, Henny W. Zandbergen, Lieven M. K. Vandersypen, and Cees Dekker. Dna translocation through graphene nanopores. Nano Letters, 10(8):3163–3167, 2010. doi: 10.1021/nl102069z. URL <https://doi.org/10.1021/nl102069z>. PMID: 20608744.
- [74] S. Garaj, W. Hubbard, A. Reina, J. Kong, D. Branton, and J. A. Golovchenko.

- Graphene as a subnanometre trans-electrode membrane. Nature, 467:190–193, Sep. 2010. URL <https://doi.org/10.1038/nature09379>.
- [75] S. J. Heerema and C. Dekker. Graphene nanodevices for DNA sequencing. Nat. Nanotech., 11:127–136, Feb. 2016.
- [76] Jiandong Feng, Ke Liu, Roman D. Bulushev, Sergey Khlybov, Dumitru Dumcenco, Andras Kis, and Aleksandra Radenovic. Identification of single nucleotides in MoS₂ nanopores. Nature Nanotechnology, 10:1070–1076, Sep 2015. URL <https://doi.org/10.1038/nnano.2015.219>.
- [77] Z. Wu, K. Hammad, E. Ghafar-Zadeh, and S. Magierowski. Fpga-accelerated 3rd generation dna sequencing. IEEE Transactions on Biomedical Circuits and Systems, 14(1):65–74, Feb 2020. ISSN 1940-9990. doi: 10.1109/TBCAS.2019.2958049.
- [78] Z. Wu, K. Hammad, E. Ghafar-Zadeh, and S. Magierowski. FPGA-Accelerated 3rd Generation DNA Sequencing. IEEE Transactions on Biomedical Circuits and Systems, 14(1):65–74, Feb. 2020. ISSN 1940-9990. doi: 10.1109/TBCAS.2019.2958049.
- [79] Y. Huang, S. Magierowski, and E. Ghafar-Zadeh. Cmos for high-speed nanopore dna basecalling. In Proc. IEEE ISCAS, pages 1–4, May 2016.
- [80] F. J. Sigworth. Electronic design of the patch clamp. In B. Sakmann and E. Neher, editors, Single-Channel Recording. Springer, New York, 2 edition, 1995.
- [81] G. Ferrari, F. Gozzini, and M. Sampietro. A current-sensitive front-end amplifier for nano-biosensors with a 2mhz bw. In 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, pages 164–165, Feb 2007. doi: 10.1109/ISSCC.2007.373345.

- [82] J. K. Rosenstein, S. Ramakrishnan, J. Roseman, and K. L. Shepard. Single ion channel recordings with CMOS-anchored lipid membranes. Nano Lett., 13(6): 2682–2686, June 2013.
- [83] B. Goldstein, D. Kim, J. Xu, T. K. Vanderlick, and E. Culurciello. Cmos low current measurement system for biomedical applications. IEEE Transactions on Biomedical Circuits and Systems, 6(2):111–119, April 2012. ISSN 1932-4545. doi: 10.1109/TBCAS.2011.2182512.
- [84] J. Lu and J. Holleman. A wideband ultra-low-current on-chip ammeter. In Proceedings of the IEEE 2012 Custom Integrated Circuits Conference, pages 1–4, Sep. 2012. doi: 10.1109/CICC.2012.6330668.
- [85] J. Kim, R. Maitra, K. D. Pedrotti, and W. B. Dunbar. A patch-clamp ASIC for nanopore-based DNA analysis. IEEE Trans. Biomed. Circuits Syst., 7(3): 285–295, June 2013.
- [86] C. Hsu and D. A. Hall. A current-measurement front-end with 160db dynamic range and 7ppm inl. In 2018 IEEE International Solid - State Circuits Conference - (ISSCC), pages 326–328, Feb 2018. doi: 10.1109/ISSCC.2018.8310316.
- [87] C. Hsu, H. Jiang, A. G. Venkatesh, and D. A. Hall. A hybrid semi-digital transimpedance amplifier with noise cancellation technique for nanopore-based dna sequencing. IEEE Transactions on Biomedical Circuits and Systems, 9(5): 652–661, Oct 2015. ISSN 1932-4545. doi: 10.1109/TBCAS.2015.2496232.
- [88] M. Taherzadeh-Sani, S. M. Hussain Hussaini, H. Rezaee-Dehsorkh, F. Nabki, and M. Sawan. A 170-db ω cmos tia with 52-pa input-referred noise and 1-mhz bandwidth for very low current sensing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 25(5):1756–1766, May 2017. ISSN 1063-8210. doi: 10.1109/TVLSI.2017.2654452.

- [89] S. Dai, R. T. Perera, Z. Yang, and J. K. Rosenstein. A 155-db dynamic range current measurement front end for electrochemical biosensing. IEEE Transactions on Biomedical Circuits and Systems, 10(5):935–944, Oct 2016. ISSN 1932-4545. doi: 10.1109/TBCAS.2016.2612581.
- [90] Y. Dawji, F. Zetterblom, S. Benages, B. Morral, S. Tan, H. Sjöland, and S. Magierowski. A 65-nm cmos low-power front-end for 3rd generation dna sequencing. In 2019 IEEE SENSORS, pages 1–4, Oct 2019. doi: 10.1109/SENSORS43011.2019.8956544.
- [91] J. Bausells, J. Carrabina, A. Errachid, and A. Merlos. Ion-sensitive field-effect transistors fabricated in a commercial CMOS technology. Sens. Actuat. B, 57: 56–62, 1999.
- [92] M. J. Milgrew, D. R. S. Cumming, and P. A. Hammond. The fabrication of scalable multi-sensor arrays using standard CMOS technology. In Proc. IEEE Custom Integrated Circuits Conf., pages 513–516, 2003.
- [93] M. J. Milgrew, P. A. Hammond, and D. R. S. Cumming. The development of scalable sensor arrays using standard CMOS technology. Sens. Actuat. B, 103: 37–42, 2004.
- [94] J. M. Rothberg, W. Hinz, K. L. Johnson, and J. Bustillo. Methods and apparatus for measuring analytes using large scale FET arrays, May 2011. Filed: Dec. 14, 2007.
- [95] W. Richard McCombie, John D. McPherson, and Elaine R. Mardis. Next-generation sequencing technologies. Cold Spring Harbor Perspectives in Medicine, 2018. doi: 10.1101/cshperspect.a036798.
- [96] B. Merriman and J. M. Rothberg. Progress in Ion Torrent semiconductor chip based sequencing. Electrophor., 33:3397–3417, Dec. 2012.

- [97] Roger Chen. Noise shielding techniques for ultra low current measurements in biochemical applications, Sep 2013. US Patent 8,541,849.
- [98] Hui Tian. Nanopore-based sequencing chips using stacked wafer technology, October 1 2015. US Patent App. 14/225,263.
- [99] Dongsoo Kim, Brian Goldstein, Wei Tang, Fred J Sigworth, and Eugenio Culurciello. Noise analysis and performance comparison of low current measurement systems for biomedical applications. IEEE Transactions on Biomedical Circuits and Systems, 7(1):52–62, 2013.
- [100] Sina Parsnejad, Haitao Li, and Andrew J Mason. Compact cmos amperometric readout for nanopore arrays in high throughput lab-on-cmos. In Circuits and Systems (ISCAS), 2016 IEEE International Symposium on, pages 2851–2854. IEEE, 2016.
- [101] PAUL MUELLER, DONALD O. RUDIN, H. TI TIEN, and WILLIAM C. WESCOTT. Reconstitution of cell membrane structure in vitro and its transformation into an excitable system. Nature, 194(4832):979–980, 1962. ISSN 1476-4687. doi: 10.1038/194979a0. URL <https://doi.org/10.1038/194979a0>.
- [102] Hiroaki Suzuki, Kazuhito V. Tabata, Hiroyuki Noji, and Shoji Takeuchi. Highly reproducible method of planar lipid bilayer reconstitution in poly-methyl methacrylate microfluidic chip. Langmuir, 22(4):1937–1942, 2006. doi: 10.1021/la052534p. URL <https://doi.org/10.1021/la052534p>. PMID: 16460131.
- [103] Hiroaki Suzuki, Bruno Le Pioufle, and Shoji Takeuchi. Ninety-six-well planar lipid bilayer chip for ion channel recording fabricated by hybrid stereolithography. Biomedical Microdevices, 11(1):17, 2008. ISSN 1572-8781. doi: 10.1007/s10544-008-9205-4. URL <https://doi.org/10.1007/s10544-008-9205-4>.

- [104] Ryuji Kawano, Yutaro Tsuji, Koki Kamiya, Taiga Kodama, Toshihisa Osaki, Norihisa Miki, and Shoji Takeuchi. A portable lipid bilayer system for environmental sensing with a transmembrane protein. PloS one, 9(7):e102427–e102427, Jul 2014. ISSN 1932-6203. doi: 10.1371/journal.pone.0102427. URL <https://pubmed.ncbi.nlm.nih.gov/25072468>. PONE-D-14-14741[PII].
- [105] Xiao-feng Kang, Stephen Cheley, Allison C. Rice-Ficht, and Hagan Bayley. A storable encapsulated bilayer chip containing a single protein nanopore. Journal of the American Chemical Society, 129(15):4701–4705, 2007. doi: 10.1021/ja068654g. URL <https://doi.org/10.1021/ja068654g>. PMID: 17375923.
- [106] Sangbaek Choi, Sunhee Yoon, Hyunil Ryu, Sun Min Kim, and Tae-Joon Jeon. Automated lipid bilayer membrane formation using a polydimethylsiloxane thin film. Journal of visualized experiments : JoVE, (113):54258, Jul 2016. ISSN 1940-087X. doi: 10.3791/54258. URL <https://www.ncbi.nlm.nih.gov/pubmed/27501114>. PMC4993438[pmcid].
- [107] James Anthony Clarke Steven Paul White Gurdial Singh Sanghera Stuart William Reid, Terence Alan Reid. Formation of layers of amphiphilic molecules, September 2015. US 2015,0265,994 A1.
- [108] P.M.O.; Brown C.G.; Heron A.J.; Mackett P.R. Hyde, J.R.; Bahamon. Formation of array of membranes and apparatus therefor., September 2015. US 2015,0265,994 A1.
- [109] Configurable analog signal processing, Jan 2007. URL <https://www.sciencedirect.com/science/article/pii/S105120040700142X>.
- [110] R. Gregorian and G. C. Temes. Analog mos integrated circuits for signal processing. In Analog MOS Integrated Circuits for Signal Processing, 1986.
- [111] Lars Wanhammar. Analog filters using matlab. Springer, 2014.

- [112] H. Wey and W. Guggenbuhl. Noise transfer characteristics of a correlated double sampling circuit. IEEE Transactions on Circuits and Systems, 33(10):1028–1030, October 1986. ISSN 1558-1276. doi: 10.1109/TCS.1986.1085840.
- [113] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta. A 10-bit charge-redistribution adc consuming 1.9 μW at 1 ms/s. IEEE Journal of Solid-State Circuits, 45(5):1007–1015, 2010.
- [114] Circuits for Data Converters, pages 209–252. Springer US, Boston, MA, 2007. ISBN 978-0-387-32486-9. doi: 10.1007/978-0-387-32486-9_5. URL https://doi.org/10.1007/978-0-387-32486-9_5.
- [115] P. M. Figueiredo and J. C. Vital. Kickback noise reduction techniques for cmos latched comparators. IEEE Transactions on Circuits and Systems II: Express Briefs, 53(7):541–545, July 2006. ISSN 1558-3791. doi: 10.1109/TCSII.2006.875308.
- [116] Corentin Pochet et al. Ultra-low leakage esd protection achieving 10.5 fa leakage. IEEE ISCAS, 34(5):123–456, May 2021. ISSN 1234-5678. doi: 10.1109/XXXX.2021.XXXXXXX.
- [117] Bernard Widrow and Marcian E Hoff. Adaptive switching circuits. In 1960 IRE WESCON Convention Record, Part 4, pages 96–104. IEEE, 1960.
- [118] Simon Haykin. Adaptive filter theory. Prentice Hall, 2002.
- [119] Ali H. Sayed. Fundamentals of adaptive filtering. Wiley-Interscience, 2003.
- [120] Xun Xu, Jasper Chiu, and Boris Murmann. Lms-based adaptive digital background calibration of pipelined adcs. IEEE Transactions on Circuits and Systems I: Regular Papers, 54(7):1410–1418, 2007.

- [121] Boris Murmann. A/d converter trends: Power dissipation, scaling and digitally assisted architectures. IEEE Custom Integrated Circuits Conference (CICC), pages 105–112, 2007.
- [122] URL https://tspace.library.utoronto.ca/bitstream/1807/100913/4/Chen_Paul_Wenbo_202006_MAS_thesis.pdf.
- [123] Ken Kundert. Hidden state in spectrerf. 2019. URL <https://designers-guide.org/analysis/hidden-state.pdf>.
- [124] Joshua Quick et al. Real-time, Portable Genome Sequencing for Ebola Surveillance. Nature, 530:228–232, 2016. doi: doi:10.1038/nature16996.
- [125] Gunther Auer et al. How much energy is needed to run a wireless network? IEEE Wireless Communications, 18(5):40–49, 2011.
- [126] Yaniv Erlich. A vision for ubiquitous sequencing. Genome Res., 25(10):1411–1416, 2015.
- [127] Nanopore Community. Oxford Nanopore Tech., Apr 2023. Available at <https://nanoporetech.com/community>.
- [128] Yunus Dawji, Mehdi Habibi, Ebrahim Ghafar-Zadeh, and Sebastian Magierowski. A Scalable Discrete-Time Integrated CMOS Readout Array for Nanopore Based DNA Sequencing. IEEE Access, PP:1–1, 11 2021. doi: 10.1109/ACCESS.2021.3129171.
- [129] Krste Asanovic, Rimas Avizienis, Jonathan Bachrach, Scott Beamer, David Biancolin, Christopher Celio, Henry Cook, Daniel Dabbelt, John Hauser, Adam Izraelevitz, et al. The Rocket Chip Generator. Technical Report UCB/EECS-2016-17, EECS Department, University of California, Berkeley, 2016.

- [130] Zynq UltraScale+ MPSoC Data Sheet: Overview. Xilinx Inc., Nov 2022. Available at <https://docs.xilinx.com/v/u/en-US/ds891-zynq-ultrascale-plus-overview>.
- [131] Andrew Waterman, Krste Asanović, and SiFive Inc. The RISC-V Instruction Set Manual, Volume I: Unprivileged ISA. Version 20191213, Dec 2019.
- [132] Michael Bedford Taylor. Basejump STL: Systemverilog needs a standard template library for hardware design. In Proceedings of the 55th Annual Design Automation Conference, pages 1–6, 2018.
- [133] Luis Vega and Michael Bedford Taylor. RV-IOV: Tethering RISC-V Processors via Scalable I/O Virtualization. In Workshop on Computer Architecture Research with RISC-V (CARRV), 2017.
- [134] R. Durbin, S. Eddy, A. Krogh, and G. Mitchison. Biological Sequence Analysis. Cambridge, 1998.
- [135] F. Gozzini. Linear transconductor with rail-to-rail input swing for very large time constant applications. Electronics Letters, 42:1069–1070(1), September 2006. ISSN 0013-5194. URL https://digital-library.theiet.org/content/journals/10.1049/el_20061709.