

INTEGRATED CIRCUITS AND SYSTEMS FOR
ADAPTIVE OPTIMIZATION OF ENERGY STORAGE EFFICIENCY
IN RESONANT INDUCTIVE WIRELESS POWER RECEIVERS

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Abstract

Recent developments in highly-miniaturized implantable neuro-stimulators has led to a rapid rise in their required power and data transmission throughput resulting in an increase of instantaneous-to-average ratio in their power consumption. Motivated by crucial role of efficient energy storage in such systems, we introduce energy management strategies in wireless powering links, in which the key performance measure is the energy stored during a limited time interval rather than the average energy delivered to the load.

First, the development of an algorithmic scheme for maximizing energy storage in current-mode (CM) resonant inductive power receivers is presented. The efficacy and precision of the presented analytical model is confirmed with CAD-based simulation results and validated using experimental measurements. Furthermore, a 0.45 mm^2 integrated circuit (IC) fabricated in $0.18 \text{ }\mu\text{m}$ CMOS is presented that performs the above-mentioned optimization. By continuous monitoring of incident waveform dynamics, the IC automatically adapts its optimal solution on-the-fly to any change in the inductive link's physical or electrical parameters. The computations are implemented using analog circuits which minimize IC's power consumption while making it needless of high-speed ADC/DAC. Our measurement results show that by using the IC, the energy storage efficiency is improved by 53% and 67% for the two tested links, compared to the conservative schemes, while consuming two orders of magnitude smaller energy than it saves through optimization. To the best of our knowledge, this is the first reported link-adaptive calibration-free IC for optimizing energy storage efficiency in CM receivers.

Second, a $2 \times 2 \text{ mm}^2$ IC is fabricated in $0.18 \text{ }\mu\text{m}$ CMOS that maximizes the energy storage efficiency in resonant inductive links with voltage-mode receivers. The IC automatically stores the maximum possible energy while simultaneously providing the required continuous load's power. In the proposed scheme, the optimal operation is maintained by detecting and operating the receiver at a specific optimal voltage, eliminating the need for direct power measurements and

adaptive matching circuits. The power reception and delivery phases are isolated which ensures maximum power reception independent of the actual loading at the receiver. The measurement results demonstrate up to 48.44% and 93.97% improvements for the charging time and the stored power, respectively.

*To my Father for his Generosity,
To the Memory of my Mother for her Love & Care,
To my Wife and our Son for their unconditional Support.*

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List of Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
BCI	Brain Computer Interface
CAD	Computer Aided Design
CLK	Clock
CLR	Clear
CM	Current-Mode
CMOS	Complementary Metal Oxide Semiconductor
CMP	Comparator
DAC	Digital-to-Analog Converter
DBS	Deep Brain Stimulation
DC	Direct Current
DCM	Discontinuous Conduction Mode
DFP	D-type Flip Flop
DSP	Digital Signal Processing
EM	Electromagnetic
ESR	Equivalent Series Resistance

FPGA	Field Programmable Gate Array
GND	Ground
IC	Integrated Circuit
IMD	Implantable Medical Device
IR-UWB	Impulse Radio Ultrawideband
KVL	Kirchhoff's Voltage Law
LDO	Low Dropout
LUT	Lookup Table
PA	Power Amplifier
PCE	Power Conversion Efficiency
PDL	Power Delivered to the Load
PMU	Power Management Unit
PNS	Peripheral Nervous System
POR	Power-On-Reset
PTE	Power Transfer Efficiency
PVT	Process Voltage Temperature
Q	Quality Factor
RST	Reset
Rx	Receiver
SAR	Specific Absorption Rate
Tx	Transmitter
VCE	Voltage Conversion Efficiency
VM	Voltage-Mode
ZCD	Zero-Crossing Detector

Chapter 1

Introduction

1.1 Implantable Medical Devices

1.1.1 Introduction and Background

Over the past two decades, implantable medical devices (IMD) have been advancing to address specific medical conditions. For instance, The Peripheral Nervous System (PNS), consisting of sensory and motor divisions, serves as the crucial communication network connecting IMDs to the body, facilitating sensory feedback and motor control. As another example, implantable brain-computer interfaces (BCIs), deep brain stimulation (DBS), and closed-loop neuro-stimulators have been proven effective in real-time neural activity recording, as well as in the responsive modulation of brain states through electrical stimulation, which have made them

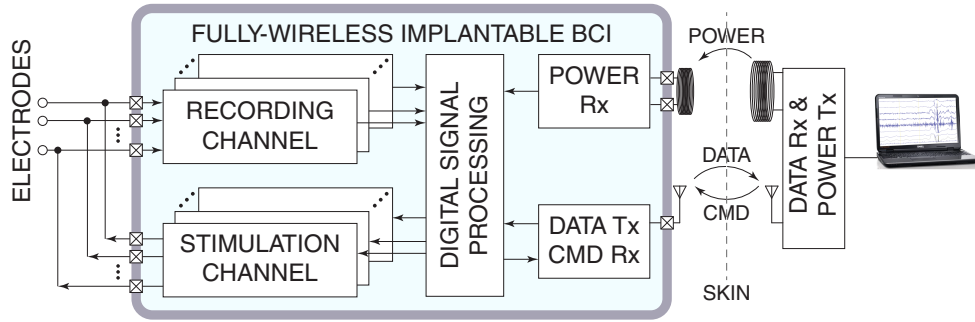


Figure 1.1: Top-level block diagram of a generic wirelessly-powered IMD.

a promising technology for diagnosis and treatment of neurological disorders (e.g., epilepsy, Parkinson’s disease, stroke, etc.) [1–15]. Accurate detection and effective control of neurological events (e.g., an epileptic seizure) that emerge from interactions among large populations of neurons in widespread networks across the brain often require hundreds to thousands of recording/stimulation channels, which has motivated the pursuit of many-channel (i.e., >100) integrated solutions. Considering the wireless nature of IMDs (for both power and data), such an aggressive channel count scaling is expected to have serious implications on the requirements for power delivery and data communication throughput [16–20].

The block diagram of a generic wirelessly-powered IMD is shown in Fig. 1.1. Typically, such a system consists of an array of recording and stimulation channels for neuro-physiological signal acquisition and responsive neuro-modulation, respectively, a digital signal processing block (DSP), and modules for wireless data communication and power telemetry. The IMD wirelessly communicates with an external unit that receives its recorded neural data and transmits configu-

ration commands to it. The external unit also provides power wirelessly to the implant. While capacitive, acoustic, optical, and far-field electromagnetic (EM) radiative methods have been investigated for wireless powering of IMDs [21–28], the most extensively studied and commonly-used method for their powering is near-field resonant inductive coupling [29–32]. This is mainly because of its robustness in penetrating through the skull bone, and reliability in efficient and adequate power delivery to millimeter-to-centimeter-sized implants within human’s safety exposure limits [33, 34].

1.1.2 IMD’s Power Consumption Profile

Besides the overall average power of an IMD (typically, a few μW to a few mW , depending on the application), the instantaneous power consumption is also a critical parameter in the design of wireless power delivery and management blocks. Fig. 1.2(a) and (b) show the transient power consumption and the power consumption profile of a typical IMD with closed-loop stimulation capability, respectively. In both figures, P_{Low} represents the power consumption of blocks such as recording and DSP that have a continuous-low power profile [35–39], while P_{High} represents the power consumption of blocks such as stimulators and data transmitter, that have a high-intermittent power profile [40–43]. Furthermore, $P_{Average-Receiveable}$ represents the average power that could be delivered via the inductive link under its optimally designed conditions. Based on the above definitions, the difference between $P_{Average-Receiveable}$ and P_{Low} is considered as the

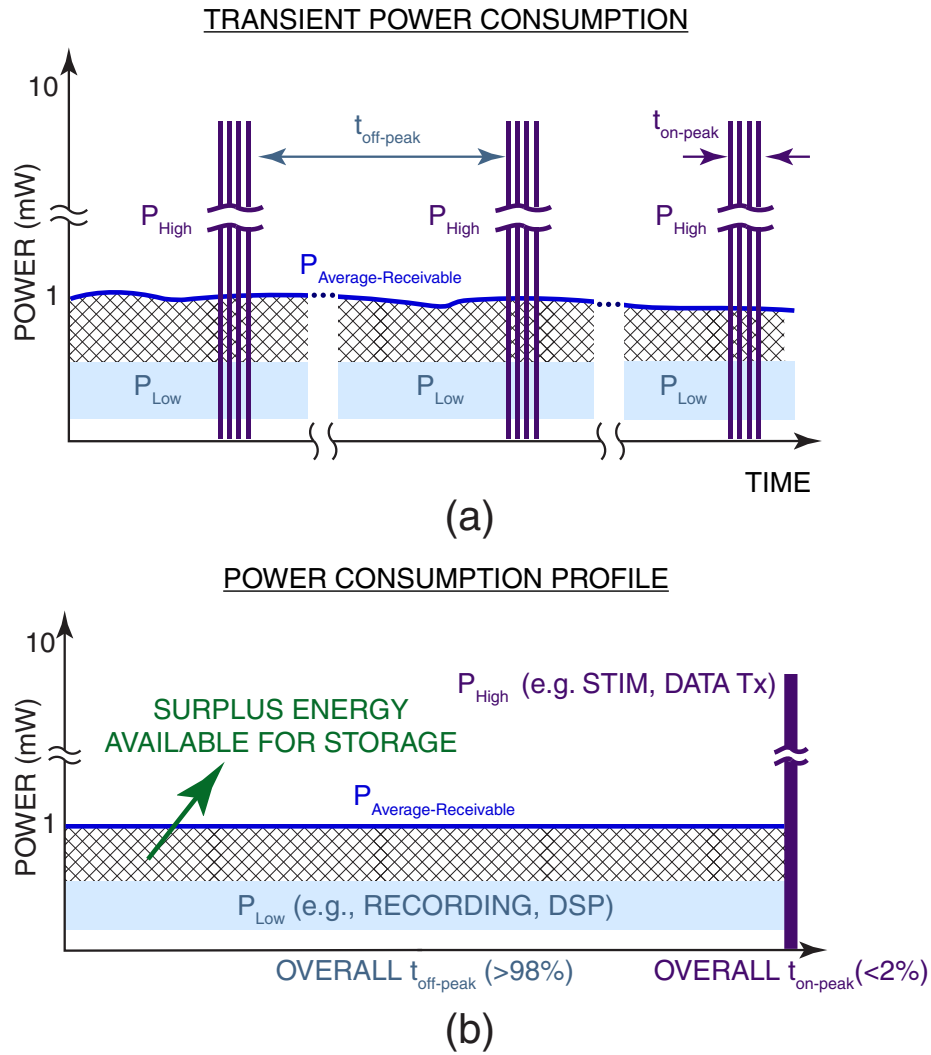


Figure 1.2: (a) Transient power consumption and (b) power consumption profile of a typical wirelessly powered IMD.

surplus power which would be available for storage if the link manages to operate at its optimal condition while simultaneously supplying P_{Low} .

Fig. 1.2(a) indicates that unlike the relatively-steady and continuous P_{Low} , P_{High} bursts result in tremendously-large short-time peaks in power consumption (during $t_{on-peak}$). Due to the continued need for miniaturization of brain implants, which involves using smaller inductive coils for power transfer, the intermittent power peaks have already exceeded the maximum that can be delivered by weakly-coupled inductive links (i.e., $P_{Average-Receiveable}$) without exceeding specific absorption rate (SAR) safety limits [44–47]. This has motivated for power management schemes that can store energy between two intermittent P_{High} episodes (i.e., during $t_{off-peak}$) and release it during $t_{on-peak}$, when the system requires large instantaneous power [48–51]. Accordingly, the efficiency of energy storage is a critical factor in determining the frequency and magnitude of high-power events. It is defined as the ratio of the total energy that is stored in a storage element (such as a battery or a capacitor) to the energy generated by the external power transmitter (Tx) over a fixed period of time, represented by $t_{off-peak}$.

Maximizing the overall link's energy storage efficiency would allow for adopting design choices that offer several advantages for IMDs but are rarely utilized because of their high instantaneous power requirements. For example, impulse radio ultrawideband (IR-UWB) transmitters are highly energy efficient for wireless communication (< 30 pJ/b [52]), and also offer wide bandwidth and miniature antennas, which make them ideal for implantable applications.

However, they are rarely used in IMDs because they transmit data using short-time bursts, which require a very large power for a very short time. This power cannot be delivered continuously using inductive links and can only be sustained if sufficient energy is stored between the bursts [33], [48]. Improved overall link's energy storage efficiency enables faster energy accumulation for each data transmission burst, allowing for increased burst frequency (higher data rate) and expanding the IMDs channel count.

1.2 Resonant Inductive Power Transfer Architectures

The above discussions motivate for a novel strategy in the design of wireless powering links, in which the key performance measure is the *energy stored during a limited period of time* rather than the *average energy delivered to the load*. This requires revising the design decisions both for the system-level architecture and the energy management strategy employed in the power-receiving circuits.

1.2.1 Wireless Power Management and Importance of Link Adaptivity

Fig. 1.3(a) depicts a simplified circuit diagram of the wireless power transfer for a generic IMD utilizing a resonant inductive link architecture. Major power loss elements in the process are depicted in Fig. 1.3(b). As illustrated, the power management unit (PMU) supplies two loads:

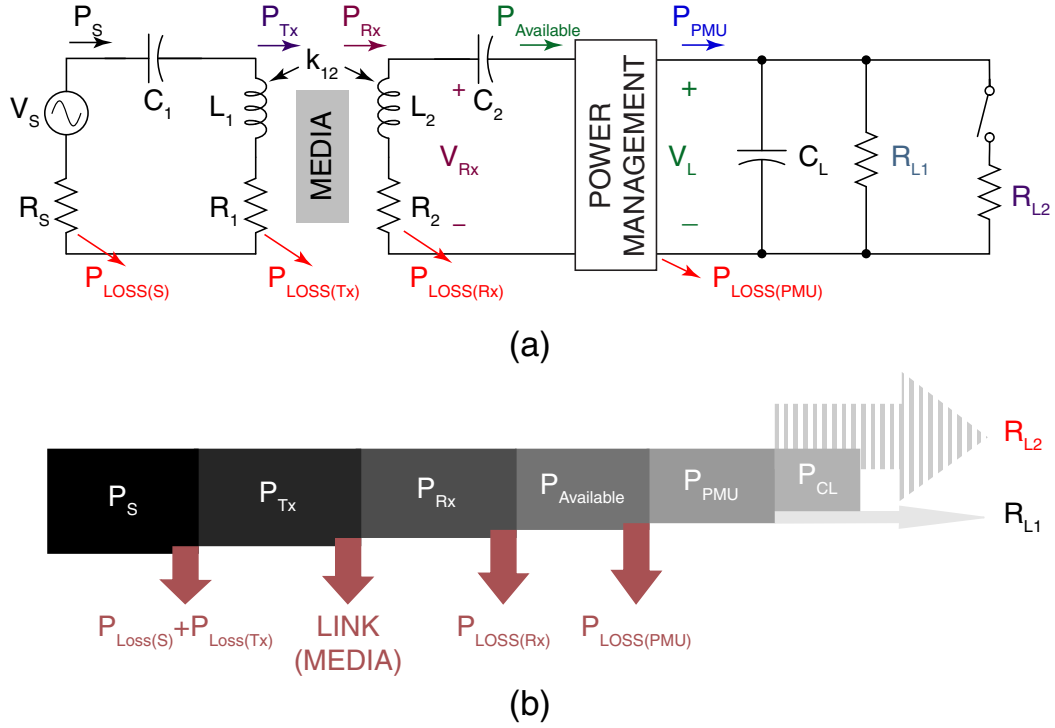


Figure 1.3: (a) Simplified circuit diagram of a generic resonant inductive link supplying two loads representing different power consumptions in an IMD and (b) power losses in the wireless power delivery path.

R_{L1} and R_{L2} . R_{L1} represents the average low-continuous power consumption of the implant, such as recording and DSP blocks, while R_{L2} represents the high-power intermittent bursts, such as electrical stimulation and data transmission. The switch in series with R_{L2} represents the intermittent nature of this type of loads.

Since R_{L1} requires a relatively constant power, which is normally less than what is continuously supplied by the link, a sufficiently-large capacitor C_L (or a rechargeable battery) is typically

used to store the excess/surplus incident power (i.e., $P_{CL} = P_{PMU} - P_{RL1}$) while simultaneously supplying R_{L1} [51]. The stored surplus energy is later recycled to either supply the implant during power peaks (P_{RL2}) or when the receiving power (P_{Rx}) is disrupted, likely due to misorientation, misalignment, or change in the coupling distance [53, 54]. It is shown in [54] that by storing and recycling energy when Tx power is interrupted, the system's peak output power could be extended by as much as 750%. Therefore, it is critical to ensure that the method used for energy storage optimization is adaptive to variations in the inductive link's parameters and the available time between two power peaks (i.e., $t_{off-peak}$).

To better understand the challenges involved in optimizing energy storage in PMUs, in the following subsections, we will provide a brief overview of the architecture and the principle of operation of two most common types of PMUs, which are voltage-mode (VM) and current-mode (CM) receivers. Following that, we will review the prior art on VM, CM, and hybrid architectures, with the emphasis on works aimed at energy storage.

1.2.2 Voltage-Mode Receivers

Fig. 1.4 depicts the circuit diagram of a resonant inductive link with a voltage-mode (VM) receiver connected to conventional power management blocks including a rectifier (shown by a diode symbol) and a low-dropout (LDO) voltage regulator or a DC-DC converter. The induced voltage at the receiver (V_{Rx}) must maintain a minimum voltage swing to ensure proper oper-

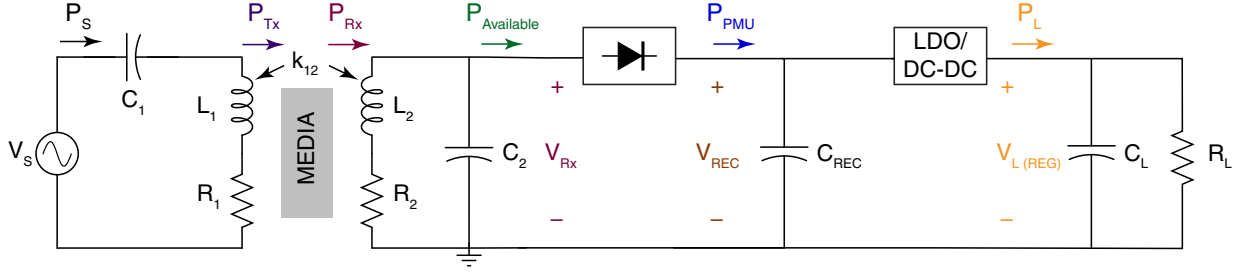


Figure 1.4: Circuit diagram of a generic resonant inductive link with VM receiver.

ation of the subsequent PMU blocks (i.e., rectifier and voltage regulator). The ultimate goal of this architecture is to deliver a sufficiently-constant controlled voltage (V_L) across the load R_L , which sets the power delivered to the load ($PDL = P_L = V_L^2/R_L$), with the highest possible power transfer efficiency (PTE). PTE is defined as the ratio of the PDL at the receiver side (Rx) over the generated source power at the transmitter side (Tx) at different coupling distances and orientations, and is shown by $\eta_{tot} = P_L/P_s$ [55].

AC-to-DC Conversion

The choice of AC-to-DC converter configuration is greatly dependent on the magnitude of the induced V_{Rx} compared to the required load voltage (V_L). If $V_{Rx(peak)} > V_L$, maintaining a high power conversion efficiency ($PCE = P_L/P_{Available}$) is most critical. However, when $V_{Rx(peak)} < V_L$, achieving a voltage conversion efficiency ($VCE = V_L/V_{Rx(peak)}$) greater than unity is of higher priority, simply to ensure the required V_L for proper operation of the IMD is delivered. For cases

with $V_{Rx(peak)} > V_L$, a rectifier circuit with a high PCE is typically used as the first rectification stage [56–59]. Extensive research has been conducted in the literature on integrating and improving rectifiers in CMOS technology as an alternative to off-chip diodes for further miniaturization. This includes exploring methods such as threshold cancellation and adaptive or partial biasing [60–62], as well as utilizing active rectifiers with synchronous active switches to control the rectifier’s conduction angle and enhance PCE by reducing leakage current [63–69]. For cases with $V_{Rx(peak)} < V_L$, a voltage multiplier is typically utilized to boost the induced voltage level (e.g., [70, 71]) and achieve a relatively-high V_L (e.g., 3.3 - 20 V) that is required for applications such as current-mode deep brain stimulation [72–79].

For an implantable device, the inductive link’s parameters (e.g., coil separation, angle, etc.) could easily change over time, which may result in large variations in the magnitude of the induced V_{Rx} , driving it lower/higher than the required V_L . To address this issue, reconfigurable AC-to-DC converters have been reported in recent years that adapt their configuration depending on the magnitude of the induced V_{Rx} [80–82]. This leads to adaptive robust solutions (i.e., high PCE when $V_{Rx(peak)} > V_L$ and high VCE when $V_{Rx(peak)} < V_L$) and extends the receiver’s functionality at different coupling situations.

Voltage Regulation

The AC-to-DC converter's output DC level is not fixed and varies depending on the incident waveform's (V_{Rx}) magnitude, which is a function of different link's parameters such as coupling coefficient, actual load at the Rx, and the Tx power. Therefore, linear or switching voltage regulators have been employed at the output of the rectifiers to deliver the required current at the target voltage level to the load [83–86]. Recently, several regulating rectifier architectures have also been proposed in literature to miniaturize the PMU architecture and to eliminate the losses associated with two-stage cascaded conversion in the system [87–90]. These circuits combine rectification and regulation by directly controlling the pass elements in the rectifier through pulse-width- and pulse-frequency modulations. This allows for a controlled turn-on of the rectifier based on input-output conditions.

Maximum Efficiency and PDL

Over the past two decades, there have been extensive research and theoretical works to formulate the optimal loading for resonant inductive links to attain the highest possible PTE or PDL, depending on the target. [91–94]. It has also been shown that the optimal load is different when the design target is to maximize PTE or PDL. The measurement results in [54] show that the inductive wireless power delivery becomes inefficient when the load consumes relatively lower

power compared to the maximum power that the link is capable to deliver under the optimal loading condition. This is mainly due to the fact that the majority of induced energy at Rx gets dissipated in the coil's resistive element due to its un-matched condition with the load in addition to impedance mismatch between the source and reflected impedance on Tx, which lowers P_{Rx} .

If the optimal load for the inductive link (Z_{opt}) is known, then an impedance matching network (built using passive LC components) is typically used to match the actual load Z_L to Z_{opt} , resulting in minimization of power reflections at both the Tx and Rx sides [45, 95]. Multi-coil resonator structures have also been employed to perform the required impedance matching by the use of additional high quality factor resonators [91, 96, 97]. By having an additional degree of freedom compared to two-coil systems, the added resonators can separate the load and source impedances from the link and transfer arbitrary loads to the optimal condition [91, 96].

However, Z_{opt} is a function of coils' quality factor, the coupling coefficient, and the actual load condition, all of which could change over time (e.g., due to changes in relative Tx-Rx coil distance, misalignments, and misorientations). This has motivated for making the impedance matching mechanism adaptive to link variations [98–102]. Moreover, besides the changes in the inductive link, the loading (Z_L) may undergo fluctuations over time, necessitating the impedance matching mechanism to be adaptable to these changes as well. A Q-Modulation technique is presented in [103, 104], in which the load transformation is achieved by dynamically modulating the loaded quality factor of the receiving coil by duty cycling the load that the receiver's LC tank

sees until the maximum V_{REC} is achieved at a certain R_L . In [105], the optimal load is achieved by dynamically manipulating the duty cycle of the utilized DC-DC converter (placed after the rectifier) and measuring the output and input powers at each step until the maximum PTE is observed. However, [105] needs an additional wireless data link, which is required to transfer the load's power information to the Tx to perform efficiency calculation. Therefore, a reliable wireless communication link is necessary to track the optimal loading conditions and accordingly adjust the Tx power. To eliminate the need for this data link, the work in [106] sweeps the input power and accordingly manipulates the duty cycle of DC-DC converter until the required regulated voltage is achieved at the minimum Tx's input power. However, [106] does not provide a solution for estimating the coupling information, which needs to be extracted in real-time to identify the Rx power-related information (i.e., Tx loading) and achieve a reliable optimal power delivery solution when the wireless data link is eliminated [107].

1.2.3 Current-Mode Receivers

The other category of architectures used for inductive power reception are current-mode receivers, which directly utilize the induced current in the Rx coil to generate DC voltage supply [108–113]. This enables power delivery to the load even when the incident waveforms are not large enough to turn on the diodes of a rectifier, making the receiver's performance independent of V_{Rx} . The direct conversion also allows for achieving a VCE greater than unity without the

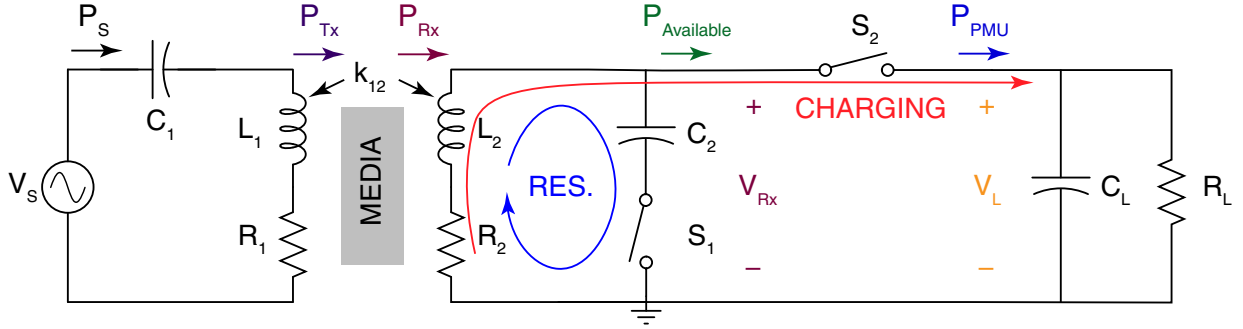


Figure 1.5: Circuit diagram of a generic resonant inductive link with CM receiver.

need for an extra boost converter, which is particularly advantageous for weakly-coupled inductive links in mm-scale IMDs.

Fig. 1.5 depicts the circuit diagram of a resonant inductive link with a current-mode receiver. Operation of these receivers is divided into two modes of resonance and charging. During the resonance mode (S_1 : ON, S_2 : OFF), a high-Q resonator is formed at the Rx to boost and accumulate the incident energy by the use of induced current in the Rx's coil. When sufficient energy is accumulated in the resonator, the receiver is taken to the charging mode (S_1 : OFF, S_2 : ON) where the accumulated energy is transferred to the load (i.e., power is delivered).

Unlike VM receivers, which deliver power continuously and steadily in each cycle of the power carrier, CM receivers operate cyclically, thereby isolating the load from the inductive link and enabling load-independent power reception. However, this cyclic operation is not suitable when the induced power at Rx increases, as a high portion of the induced power gets dissipated

in the coil's and switches' parasitic resistances during the resonance mode resulting in efficiency degradation. Therefore, CM receivers are suitable for light loads with high voltage requirements while they suffer from efficiency and PDL degradation at heavy loads, where a better impedance matching with the link's optimal impedance and accordingly performance improvements (i.e., higher PDL and PTE) could be achieved by VM receivers [114].

1.2.4 Hybrid Solutions

As discussed, the choice between VM and CM architectures heavily depends on the load's power requirements. For applications with varying load conditions, VM receivers with adaptive impedance matching can perform load transformation to achieve a better PTE and PDL. However, the range of load transformation is limited and might not be sufficient for robust and broad operation. On the other hand, CM receivers perform better for weakly-coupled conditions with lower levels of induced power and when a VCE greater than unity is needed. However, they suffer from efficiency degradation with the increase in the load's power demand or the induced power at the receiver. Therefore, hybrid power management solutions that switch between VM and CM topologies have been recently implemented for robust operation (e.g., guaranteeing PTE/PDL to be above a value at all times, while maintaining the required load voltage) against coupling and loading variations [53, 115, 116].

The design in [115] uses a closed-loop architecture in which a controller continuously mon-

itors V_{Rx} and compares it with the required V_L to decide VM or CM operation in Rx, in contrast with the open-loop strategy adopted in [116] where the Rx switches between VM and CM modes for pre-defined durations for simultaneous power delivery to two high- and low-power resistive loads, respectively. Based on the implemented inductive link parameters in [116], it is shown that due to inherent difference in their operations, VM is more suitable for delivering high power ($\sim 4x$ higher PDL compared to CM) at low voltages while CM provides a better solution for delivering low power at higher voltages ($\sim 12x$ higher load voltage compared to VM) when the induced V_{Rx} magnitude is lower than the required load voltage.

It should be noted that in addition to variations in the link's coupling coefficient and the load value, the magnitude of the induced waveform at the receiver, V_{Rx} , is also dependent on the source power. This implicates that the induced voltage/current ratio at Rx (i.e., P_{Rx}) is proportional to the input power at Tx while the optimal impedance (i.e., optimal voltage/current ratio) is unaffected. Hence, relying solely on load voltage criteria may lead to deviations from the optimal conditions. This is considered as one of the main challenges that should be addressed in the design of hybrid receivers to effectively select VM/CM architecture and enable the link to function at its optimal capacity under varying circumstances.

1.3 Thesis Objectives

As discussed, optimizing overall link's energy storage efficiency of PMUs is essential for IMDs' channel count scaling and improving their diagnostic and treatment capabilities. A major issue with energy storage in a capacitor and reusing its stored energy is that it results in a varying voltage, which results in a dynamic load across the receiver. On the other hand, the amount of induced power at Rx is a function of its actual loading, coils' quality factors, coupling coefficient, and the generated power at the Tx, therefore, it could change significantly over time. Simultaneously, to maximize overall link's energy storage efficiency, it must be ensured that the R_L 's actual power requirement and the V_{REC} level also do not deviate $P_{Available}$ from its highest possible level. Therefore, isolating the capacitive load from the inductive link is an essential step towards achieving a high induced power with a highly efficient charging process at Rx.

Accordingly, as summarized below, this thesis presents two distinct on-chip circuit solutions that perform link-adaptive on-the-fly optimization of overall link's energy storage efficiency of resonant inductive links for two classes of current-mode and voltage-mode receivers. Below, we have briefly summarized the challenges for energy storage optimization in each case (i.e., CM and VM), followed by the introduction of our proposed solutions.

- As mentioned, a CM architecture is typically utilized for cases with low levels of incident energy at the receiver. It has two modes of operation and its power transfer efficiency

mainly depends on performing the switching between the resonance and the charging modes with an optimal timing. As will be discussed in Chapter 2 in details, this optimal timing depends on many parameters (e.g., link's physical parameters, rate of energy accumulation, etc.), hence varies over time and across different links. Finding an optimal solution for their specific inductive link parameters has been investigated in [108] and [114]. However, both works present solutions only for continuous low-power loads (i.e., the storage capacitor discharges with a slow steady rate) and do not consider intermittent high-power loads. Intermittent loads are considered in the solution presented in [109], but their solution requires a calibration phase to measure the instantaneous Rx power and to digitize it so that a controller can choose the best solution from a lookup table. As a result, the solution is not adaptive to changes that happen after calibration. The design proposed in [53] uses a CM architecture and aims to store the surplus energy in a capacitive load after delivering sufficient power to a resistive load. However, the presented solution does not guarantee that the CM receiver's operation and timing is optimized to maximize energy storage in a capacitive load.

In this work, we present a self-contained, link-adaptive methodology (outlined in Chapter 2) that accurately identifies the optimal timing solution for the CM cyclic operation to achieve maximum overall link's energy storage efficiency of a weakly-coupled inductive link regardless of load being low-continuous, high-intermittent, or a mixture of the two.

Moreover, an integrated circuit (IC) is designed and characterized (described in Chapter 3) that is capable of automatically updating the optimal solution on-the-fly and needless of pre-calibration, making the solution adaptive to the link's physical or electrical properties variations over time. The accuracy and link-adaptivity of the fabricated IC is cross-validated with theoretical calculations and experimental measurements for two different links. The sensing and processing blocks of the presented solution are implemented in the analog domain, which eliminates the need for high-speed, high-resolution, and power-hungry analog-to-digital converters (ADC). Moreover, it has been demonstrated that even under worst-case scenarios, the power consumption of the IC is two orders of magnitude lower than the energy it saves through optimization. Our measurement results show that by using the presented IC, the overall link's energy storage capability is improved by 53% and 67% for the two tested links, respectively, when compared to the conservative schemes used for the receiver's operation control. To the best of our knowledge, this is the first reported integrated link-adaptive calibration-free solution for optimizing the overall energy storage efficiency in weakly-coupled inductive links.

- A VM architecture is typically utilized for cases with highly-sufficient levels of incident energy at the receiver. Here, the PMU's main task is to strike a balance between its power loss ($P_{LOSS(PMU)}$ in Fig 1.3(a)) and the PDL to yield a high PTE and adjust its loading on Tx to maximize PDL. Due to the continuous loading in VM receivers, both P_{Rx} and

PTE are directly affected by the load's current and voltage, which means that the optimal solution is sensitive not only to variations in the link's parameters but also to changes in the load value. As discussed in 1.2.2, several techniques such as adaptive impedance matching, employing additional resonators in the inductive link (i.e., three- and four-coil architectures), and closed-loop control of power management are proposed in the literature to achieve the optimal operation while delivering the required power at the target load voltage [91, 100, 117]. However, all these solutions are devised for a resistive load that requires a fixed load voltage for operation. Here, the main challenge is that with the addition of the storage element, the load is a mixture of resistive and capacitive components, hence, its voltage varies significantly during the intermittent high-power events (due to charging and discharging), requiring the optimal solution to be not only link adaptive, but also load adaptive. In [118] and [119], it was demonstrated that removing the voltage regulator and directly connecting the energy storage element at the output of the rectifier speeds up the charging process. However, the link and load are not isolated from each other and the varying load voltage during energy storage and consumption still affects the receiver's power level (i.e., P_{Rx}) and accordingly the charging efficiency. Moreover, the optimal operating point for maximizing the energy storage is not defined as well. Meanwhile, techniques such as adaptive impedance matching used in [92] require manipulating the Rx's resonator during charging (which increases the Rx form factor as it requires multi-resonators to op-

erate at a single power carrier frequency) and real-time power measurement on the load side (which requires continuous monitoring of the charging current and voltage across the load and on-the-fly power calculations).

In Chapter 4 of this work, we introduce a self-contained and efficient solution for energy storage in VM receivers by separating the effect of the load on the link, allowing for load-independent optimization of the power link during capacitor charging. The method eliminates the need for direct power measurements at the load by determining the optimal V_{Rx} that sets the rectifier's conduction angle at the optimal loading condition. To maintain the optimal V_{Rx} , the method controls the drawn current from the Rx's LC tank at every power cycle, hence guaranteeing continuous power reception without interfering/stopping the resonance. Therefore, the optimal loading of the link could be achieved without the need for manipulating the Rx's LC resonators.

1.4 Dissertation Organization

The rest of this dissertation is organized as follows. In Chapter 2, first, we present a step-by-step development of an analytical model for a CM power receiving circuit in different modes of operation. This has resulted in closed-form expressions for the energy lost at any moment of time during the operation, and the energy stored in the capacitive load over time. In each step of development, we have validated the precision of the model by comparing its time-domain

estimation of different key performance parameters with CAD-based circuit simulation results. Next, we have furthered our analytical model by calculating the optimal timing sequence for the operation of the CM power-receiving circuit that results in maximizing the energy storage and its efficiency over a fixed period of time (e.g., the interval between two data transmission bursts) and confirmed our model's prediction with simulation results. Moreover, the optimal operating point predicted by the algorithm for two different inductive links are confirmed with measurement results. We have utilized discrete components and a general-purpose processor to control the operation of our inductive resonance power receiving circuit based on our theoretical results. Our experimental results show that the proposed operation scheme yields maximum energy storage in a capacitive load for any given period of time.

Since the entire model is developed with no assumptions on the link's physical or electrical parameters, the obtained solution is universal and applicable to any inductive link independent of the coils' quality factors, coupling variations, and medium properties. Additionally, since the optimization algorithm monitors real-time values of certain electrical quantities at the receiver side of the link, its optimal solution has the potential to offer adaptiveness to random changes to the link parameters during operation, which makes it advantageous over a pre-programmed scheme. To complement the task, Chapter 3 presents the detailed design, development, and experimental characterization of a fabricated 0.45 mm^2 IC in a standard $0.18 \text{ }\mu\text{m}$ CMOS process that is used to evaluate the developed energy optimization algorithm. To minimize the IC's power

consumption, all the high-speed blocks for monitoring, optimization point computation, and system control are implemented using analog circuits, making the solution needless of a high-speed ADC/DAC. Furthermore, circuit- and system-level discussions are provided and system's robustness and accuracy are validated using different simulations such as process-voltage-temperature (PVT) variations along with practical measurements.

In Chapter 4, first, we provide a review on the theory and modeling of wireless resonance inductive links with VM receivers. The accuracy of developed model along with formulation of different parameters have been validated by comparing the calculated versus CAD-based circuit simulation results. Next, we provide a discussion on the optimal operating condition which needs to be maintained to achieve an efficient wireless power transfer and delivery in the system. Then, the optimal condition is related to achieving a high overall link's energy storage efficiency while simultaneously delivering the required load power in the system. These requirements include link-load isolation which prevents the loading effect on the link's operation and detection of the optimal voltage to be maintained at the receiver without the need for a direct power measurement in the system. Next, the undertaken strategy to achieve these requirements is demonstrated and the validity of the proposed scheme is supported with CAD-based simulation results. Additionally, the detailed circuit-level design and system-level implementation of a fabricated 4 mm^2 IC in a standard $0.18\text{ }\mu\text{m}$ CMOS process that is used to perform the proposed optimization scheme is presented. The measurement results demonstrate 19.61% and 24.39% improvements in charg-

ing time and stored power, respectively. These improvements can reach as high as 48.44% for the charging time and 93.97% for the stored power when considering different reference points for comparison.

Chapter 5 concludes the dissertation by listing the thesis contributions and relevant publications. In addition, this chapter highlights future work trends and suggestions such as performing recycling of the stored energy without affecting energy storage and link operation, enhancing simultaneous energy storage and power delivery in VM and CM receivers, implementing hybrid VM-CM systems that automatically operate under optimal conditions for both cases, and optimizing energy storage of surplus energy and recycling in multi-Rx systems.

Chapter 2

A Real-Time-Link-Adaptive Operation Scheme for Maximum Overall Link's Energy Storage Efficiency in Resonant CM Wireless Power Receivers

2.1 Introduction

In this chapter, first, we describe the principle of operation and present a detailed analytical model for a current-mode (CM) power receiving circuit in different modes of operation. We will show how these analyses result in closed-form expressions for the energy lost at any moment of time during the receiver's operation, and the energy stored in the capacitive load over time. We will

then confirm the precision of the model by comparing its time-domain estimation of different key performance parameters with circuit simulation results, and later, experimental measurement results.

Next, we further extend our analytical model by calculating the optimal timing sequence for the operation of the CM power-receiving circuit that maximizes the energy storage over a fixed period of time (e.g., the interval between two data transmission bursts). The efficacy of our theoretical work is validated by both circuit simulation and experimental measurement results. We have utilized discrete components and a general-purpose processor to control the operation of our inductive resonance power receiving circuit based on our theoretical results. Our experimental results show that *the proposed operation scheme yields maximum energy storage in a capacitive load for any given period of time.*

Since the entire model is developed with no assumptions on the link's physical or electrical parameters, *the obtained solution is universal* and applicable to any inductive link independent of the coils' quality factors, coupling variations, and medium properties. Additionally, since the optimization algorithm monitors real-time values of certain electrical quantities at the receiver side of the link, its optimal solution has the potential to offer *adaptiveness to random changes to the link parameters during operation*, which makes it advantageous over a pre-programmed scheme. Of course, such an advantage is conditional to a low-power circuit implementation of the presented solution, which is the main purpose of Chapter 3 to complete the presented energy

optimization scheme.

The rest of the chapter is organized as follows. Section 2.2 includes the principle of operation of CM receivers and provides a critical review of the state of the art solutions for CM receivers and their optimization. Section 2.3 provides a step-by-step development of the presented analytical model for the operation of CM receivers and a detailed theoretical discussion on maximizing the overall link's energy storage efficiency. In each step of development, the theoretical predictions are validated by CAD-based simulation results. Section 2.4 presents the experimental measurement results where the optimal operating point predicted by the algorithm for two different links are confirmed with measurement results. Section 2.5 concludes this chapter.

2.2 Current-Mode Receivers

2.2.1 Principle of Operation

As discussed in Chapter 1, CM receivers act as current sources and do not require a minimum incident wave magnitude (i.e., induced voltage at the receiver) to start the process of energy storage in the capacitive load, which makes them a better choice for energy storage in mm-scale wireless brain-implantable devices that normally operate under weak coupling due to the receiver's size constraints and implantation depth [108–113]. Hence, they can achieve a VCE greater than unity without the need for an additional charge pump or a DC-DC converter stage

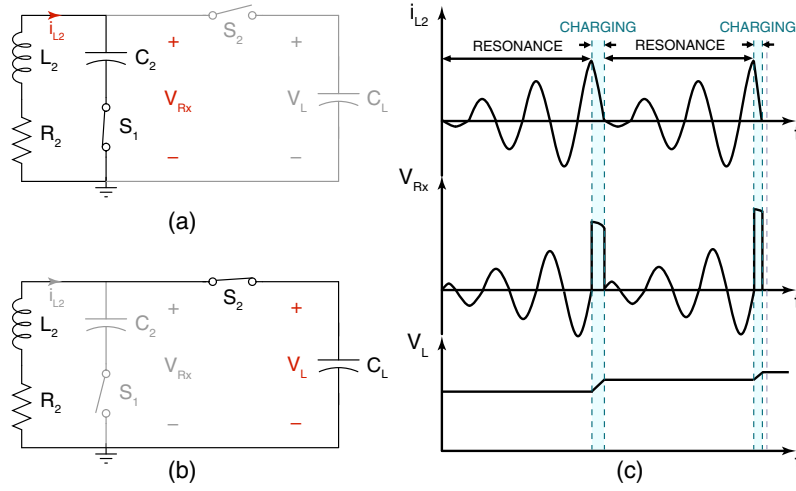


Figure 2.1: Conventional CM receiver operation in (a) resonance-mode and (b) charging-mode. (c) Conceptual waveforms in both modes.

[120]. Furthermore, thanks to the cyclic operation of CM receivers, charging the load capacitor does not load the receiver's resonating tank as they are isolated during the resonance mode (i.e., the power receiving phase), which results in having a constant reflected load on the transmitter side at all times.

During their operation, CM receivers frequently switch back and forth between two modes, namely the resonance and the charging [109]. CM operation is depicted in Fig. 2.1, where L_2 and C_2 form the Rx's resonating tank, R_2 represents the parasitic or ohmic losses in Rx coil, and C_L is the load capacitor. As shown in Fig. 2.1(a), during the resonance mode, the switch S_1 is closed while the capacitive load C_L is disconnected from the link resulting in the energy to be built up (accumulated) in the L_2C_2 tank while it is being exchanged between L_2 and C_2 . To transfer the

accumulated energy to the load capacitor C_L , the circuit switches from resonance mode to the charging mode every N cycles. During the N^{th} cycle that the mode switching is conducted, the best moment to make the transition is when all the accumulated energy is stored in L_2 , i.e., when the receiver current peaks and the voltage across the receiving coil (V_{Rx}) is zero, indicating zero energy in C_2 . As shown in Fig. 2.1(b), during the charging mode, S_1 is opened and S_2 is closed to transfer the stored energy in L_2 to C_L in a boost converter fashion by pumping L_2 current (i_{L2}) into C_L . At the onset of charging mode, V_{Rx} promptly jumps up to the previous voltage value on C_L (V_L) plus the voltage drop on S_2 . The associated waveforms of i_{L2} , V_{Rx} , and V_L are also shown in Fig. 2.1(c).

It is worth mentioning that a parallel-secondary CM receiver (shown in Fig. 2.1) results in a higher efficiency compared to a series-secondary CM receiver (i.e., L_2 and C_2 connected in series) as the latter suffers from residual energy in C_2 , as C_2 remains in the charging path and prevents complete transfer of L_2 's energy to the load. On the contrary, S_1 in the parallel-secondary architecture is exposed to V_{Rx} which limits the receiver's maximum voltage rating in accordance to the breakdown voltage of the utilized devices [121].

2.2.2 Optimal Energy Management Strategy

Maximizing the overall charging efficiency in cyclic architectures (i.e., CM receivers) requires careful selection of the optimal number of cycle (N_{opt}) at which the switching from resonance to

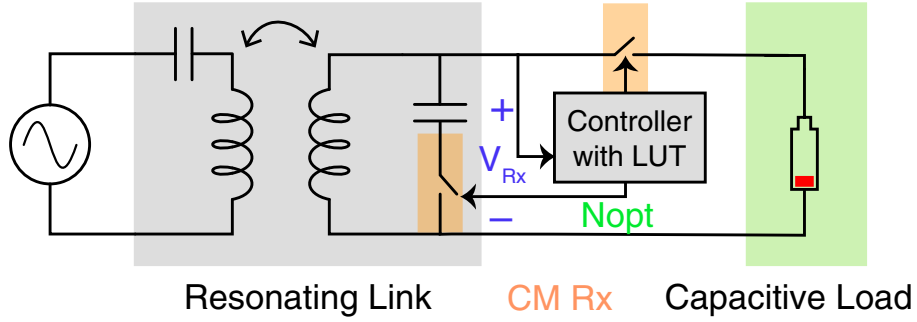


Figure 2.2: The controller in [109] determines N_{opt} in a CM receiver by going into calibration phase to measure the incident power and compare with stored data in LUT.

charging occurs. Reviewing the literature, the CM receiver in [108] is proved to enhance VCE by achieving a higher V_L at resistive loads compared to $V_{Rx(peak)}$. While it is shown that the maximum PTE occurs at the highest achievable V_L at an optimal switching frequency between resonance and charging modes, the optimal switching moment is not modeled in the analysis. In [109], a maximum efficiency tracker is designed to determine N_{opt} that maximizes the overall charging efficiency of a battery at very low input powers. The power receiver controller works based on a pre-programmed lookup table (LUT) where the N_{opt} values associated with different levels of incident power are stored (Fig. 2.2). This means that the design in [109] is specific to a single link and any changes to the physical or electrical parameters of the link, or due to coil movements or environment variations will deviate the operation from the optimal point. It also means that a calibration must be performed to update the N_{opt} values before using the power receiver or after any of the above changes happens. In [114], a closed form expression is presented

in order to determine N_{opt} that results in the highest delivered power to a resistive load. Since the targeted load is resistive, the energy efficiency is maximized for a single charging event, and not for multiple charging events over a period of time. However, since V_L directly affects the energy loss during a charging event, this approach is not suitable for energy storage in capacitive loads where the overall charging period is an additional important parameter to be considered.

In this work, a generic optimization algorithm is developed that is capable of detecting the optimal capacitor charging moment in a CM receiver. Intuitively speaking, to maximize the energy that the receiver can transfer to the load during a fixed period $t_{ov} = t_{off-peak}$, the resonance-to-charging transition should happen when the product of accumulated energy in the receiver's L_2C_2 tank (E_{LC}) and the number of charging events (m) is maximum. Since these parameters vary between different links and also over time for the same link, the algorithm for N_{opt} (i.e., the cycle at which the mode switching must happen) calculation should take into account link-specific parameters such as quality factor, as well as the real-time value of transient electrical parameters such as induced current/voltage at the receiving coil.

2.3 Analytical Optimization of CM Receivers Operation

2.3.1 Circuit Parameters and Simulation Setup

In this section, we describe the analytical model that is developed to theoretically determine the optimal operation of a CM power receiver for maximum overall link's energy storage efficiency. Inductive links with a CM receiver are used to compare the estimated behaviour of various parameters by the analytical model and the CAD simulation results from transient simulations in Cadence Spectre.

It must be pointed out the link parameters values that are used here should be seen as examples, and the developed model and optimization method are independent of them and is applicable to any weakly-coupled inductive link with a CM receiver. Similarly, for the storage capacitor, a C_L of 100 nF is used in order to reduce the overall simulation time and memory, while the presented model and optimization method work with other C_L values as well. It should be noted that the C_L is used as an storage element where its voltage is set by the available energy to be stored (E_{Load}). The available energy for storage depends on the link parameters and is obtained by subtracting the overall energy losses in the receiver from the incident energy. V_L is set according to the amount of energy transferred for storage based on $E_{Load} = 0.5C_LV_L^2$. Therefore, a larger C_L will result in a smaller V_L and vice versa. Hence, the optimal operation of a CM receiver in a specific inductive link is not affected by the size of C_L . This is further validated later in the paper

by providing simulation results for different C_L values.

For simulation, the resonance inductive link (mutually coupled Tx-Rx inductors) along with the associated switches in the CM receiver were excited using a voltage source (on the Tx side) and the transient currents at the Tx and Rx sides along with the voltages at different nodes were monitored. Accordingly, all the power and energy waveforms (including the total supplied power and energy to the Tx, the total received power and energy at the Rx, the power and energy losses in different modes of operation at both sides, etc.) were obtained using the transient data and the calculator tool in Cadence to perform the required integration and mathematical operations. Furthermore, a five-bit counter along with an ideal conditioning circuit were used to control the number of resonance cycle and the timing of the required controlling signals. Then, the obtained simulation data from sweeping the number of resonance cycles, frequency of operation, load capacitor, etc. were imported in MATLAB to compare the simulation results with their calculated counterparts. The results of these comparisons are provided in the following subsections.

2.3.2 Resonance Mode

Fig. 2.3 depicts the equivalent circuit of an inductive link with a CM receiver operating in the resonance mode with coupled coils ($M = k_{12}\sqrt{L_1L_2}$) modeled as dependent voltage sources and the switch S_1 is replaced with its equivalent ON resistance (R_{SW1}). Writing Kirchhoff's voltage law (KVL) for the two loops results in:

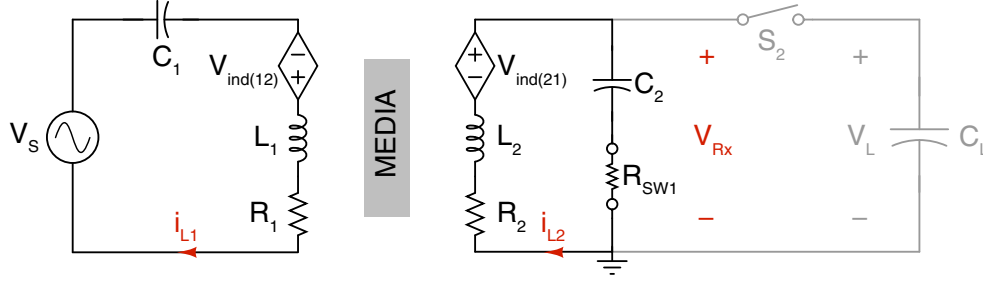


Figure 2.3: Equivalent circuit of the CM inductive link in resonance-mode.

$$\begin{aligned} \left(j\omega L_1 + R_1 + \frac{1}{j\omega C_1} \right) i_{L1} - V_{ind(12)} &= |V_s|, \\ \left(j\omega L_2 + R_2 + R_{SW1} + \frac{1}{j\omega C_2} \right) i_{L2} - V_{ind(21)} &= 0, \end{aligned} \quad (2.1)$$

where $\omega = 2\pi f$ is the angular frequency with f being the frequency of the power carrier, with $V_{ind(12)} = j\omega M i_{L2}$ and $V_{ind(21)} = j\omega M i_{L1}$ indicating the induced voltages at both sides. At resonance frequency f_o ($\omega_o = 1/\sqrt{L_1 C_1} = 1/\sqrt{L_2 C_2}$), the magnitude of $V_{ind(21)}$ at the receiver is found to be:

$$|V_{ind(21)}| = \frac{\omega_o M |V_s|}{R_1 + \frac{(\omega_o M)^2}{(R_2 + R_{SW1})}} = \frac{|V_s| k_{12} \sqrt{Q_1 Q_{2eq}} \sqrt{R_{2eq}}}{(1 + k_{12}^2 Q_1 Q_{2eq}) \sqrt{R_1}}, \quad (2.2)$$

where $R_{2eq} = R_2 + R_{SW1}$ is the total equivalent resistance of the receiver during resonance mode, $Q_1 = \omega_o L_1 / R_1$ and $Q_{2eq} = \omega_o L_2 / R_{2eq}$ are the quality factors of Tx and Rx coils, respectively. The transient current i_{L2} that will be developed at Rx due to the induced voltage $V_{ind(21)}$ during resonance mode can be found by solving the following differential equation,

$$V_{ind(21)}(t) = L_2 \frac{di_{L2}(t)}{dt} + R_{2eq} i_{L2}(t) + \frac{1}{C_2} \int i_{L2}(t) dt. \quad (2.3)$$

For an efficient wireless power transmission, Q_{2eq} should be maximized by lowering R_{2eq} as there is a limit on increasing L_2 due to the size constraints in medical implants. Therefore, Rx circuit during resonance will have an underdamped response and the solution of i_{L2} in (2.3), including the complementary and particular (due to $V_{ind(21)}$ and assuming a sinusoidal V_s) solutions with the coefficients from the initial conditions, could be written as

$$i_{L2}(t) = e^{-\alpha t} \left[-\frac{|V_{ind(21)}|}{R_{2eq}} \cos \left(\left(\sqrt{\omega_o^2 - \alpha^2} \right) t \right) - \frac{\alpha |V_{ind(21)}|}{R_{2eq} \sqrt{\omega_o^2 - \alpha^2}} \sin \left(\left(\sqrt{\omega_o^2 - \alpha^2} \right) t \right) \right] + \frac{|V_{ind(21)}|}{R_{2eq}} \cos(\omega_o t), \quad (2.4)$$

where $\alpha = R_{2eq}/(2L_2)$ is defined as the neper radian frequency in series RLC circuit.

In a high-Q resonator, the $\sqrt{\omega_o^2 - \alpha^2}$ term approximately equals ω_o . Therefore, $\alpha |V_{ind(21)}| / (R_{2eq} \sqrt{\omega_o^2 - \alpha^2})$ could be safely ignored compared to $|V_{ind(21)}| / R_{2eq}$ resulting in (2.4) to be approximated as

$$i_{L2}(t) \cong \left(-\frac{|V_{ind(21)}|}{R_{2eq}} e^{-\alpha t} + \frac{|V_{ind(21)}|}{R_{2eq}} \right) \cos(\omega_o t), \quad (2.5)$$

Table 2.1: Simulation parameters of the inductive links with a CM receiver used to validate the modeling versus simulations.

Parameter	Link1	Link2	Link3
t_{ov}	2.0 ms	1.0 ms	1.0 ms
f_o	1 MHz	1 MHz	6.78 MHz (1-20) MHz
$V_{s(peak)}$	1.5 V	0.2 V	0.5 V
k_{12}	0.01	0.01	0.01
L_1, L_2	205/4.2 μ H	205/39 μ H	8.0/7.4 μ H
C_1, C_2	123 pF/6 nF	123 pF/649.5 pF	68.88 pF/74.46 pF
C_L	100 nF-200 μ F	100 nF	100 nF
R_1, R_2	30/1.1 Ω	30/4.0 Ω	30/10 Ω
$R_{SW1,2}$	1.0 Ω	2.5 Ω	2.0 Ω

with its envelope defined as

$$i_{L2(peak)}(t) \cong -\frac{|V_{ind(21)}|}{R_{2eq}} e^{-\alpha t} + \frac{|V_{ind(21)}|}{R_{2eq}}. \quad (2.6)$$

The complementary response in (2.4) or (2.5) will eventually vanish at an exponential rate proportional to the Rx's time constant ($\tau = 1/\alpha = 2L_2/R_{2eq}$) and the current will reach its steady-state with a magnitude equal to $|V_{ind(21)}|/R_{2eq}$ as a result of the particular solution due to the induced voltage $V_{ind(21)}$. In steady-state, L_2 and C_2 are fully resonating which results in a purely resistive reflected impedance on the Tx side. It is noted that the received voltage V_{Rx} across the

coil and C_2 will have the same waveform as i_{L2} with a 90° lagging phase, as was also depicted in Fig. 2.1(c).

Fig. 2.4(a) compares the theoretically-calculated transient i_{L2} in (2.4) along with its calculated envelope approximation in (2.6) with their counterparts from CAD-based circuit simulations for link1 in Table 2.1. As shown, the calculated values closely match the simulation results, verifying the validity of the provided signal and envelope approximations. Fig. 2.4(b) shows the same curves for V_{Rx} .

2.3.3 Charging Mode

The simplified equivalent circuit of the receiver during charging mode is depicted in Fig. 2.5. When operating in this mode, the stored energy in L_2 is transferred to the load by pumping i_{L2} into the load capacitor C_L through S_2 ($R_{ON} = R_{SW2}$). When the energy transfer is completed, i_{L2} will be zero and S_2 should be immediately turned off to prevent C_L from discharging back into the L_2C_2 tank. Since the charging time (t_{ch}) is very short, i_{L2} is approximated to be linearly decreasing as

$$i_{L2(ch)} = i_{L2(peak)} - \left(\frac{i_{L2(peak)}}{t_{ch}} \right) t. \quad (2.7)$$

As the receiver is not resonating during the charging mode, the induced $V_{ind(21)}$ under non-resonance weakly coupled condition results in a negligible energy compared to the accumulated

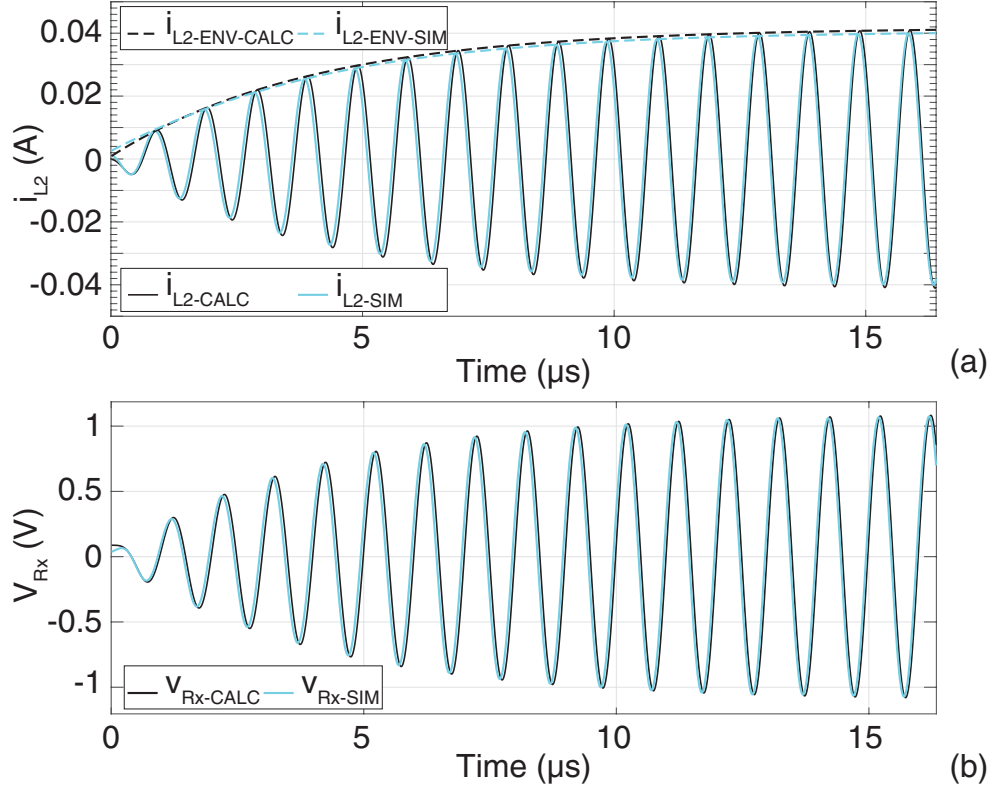


Figure 2.4: Simulated and calculated transient results of induced (a) i_{L2} and its envelope approximation, and (b) V_{Rx} , both in resonance mode.

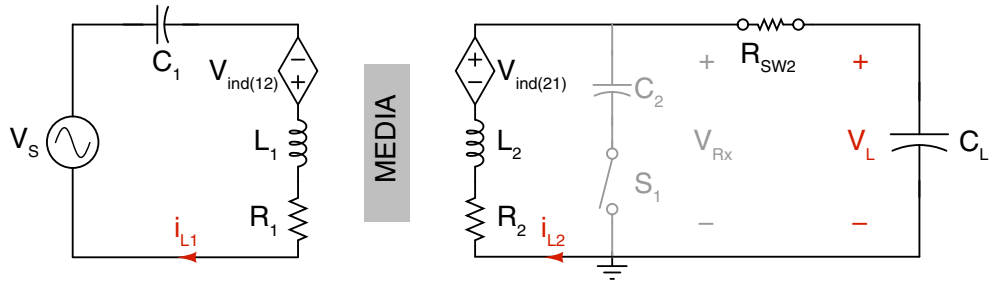


Figure 2.5: Equivalent circuit of the CM inductive link in charging-mode.

energy in L_2 during the resonance mode and the circuit is modeled as a series RLC circuit.

Therefore,

$$L_2 \frac{di_{L2}(t)}{dt} + (R_2 + R_{SW2})i_{L2}(t) + V_{L(k)} = 0, \quad (2.8)$$

where $V_{L(k)}$ is the final voltage on C_L after k charging events, defined as,

$$V_{L(k)} = \frac{1}{C_L} \int_0^{t_{ch}} i_{L2(ch)}(t) dt + V_{L(k-1)} = \frac{1}{2C_L} i_{L2(peak)} t_{ch} + V_{L(k-1)}, \quad (2.9)$$

and $V_{L(k-1)}$ is the voltage on C_L after $k-1$ charging events. Combining (2.8) and (2.9), we get

$$t_{ch} = \frac{L_2 i_{L2(peak)}}{V_{L(k)}}, \quad (2.10)$$

and consequently,

$$V_{L(k)} = 0.5 \left[V_{L(k-1)} + \sqrt{V_{L(k-1)}^2 + 4E_{LC(peak),N}/C_L} \right], \quad (2.11)$$

with $E_{LC(peak),N}$ being the stored energy in L_2 at the end of resonance mode after N resonance cycles, just before switching to the charging mode.

Fig. 2.6 shows the calculated and simulated V_L for link1 in Table 2.1, indicating stored energy on C_L , for different number of resonance cycles N , and for the overall time period of $t_{ov} = 1 \text{ ms}$. Similar trends and proximity in increasing V_L is observed for all cases of N . The small difference

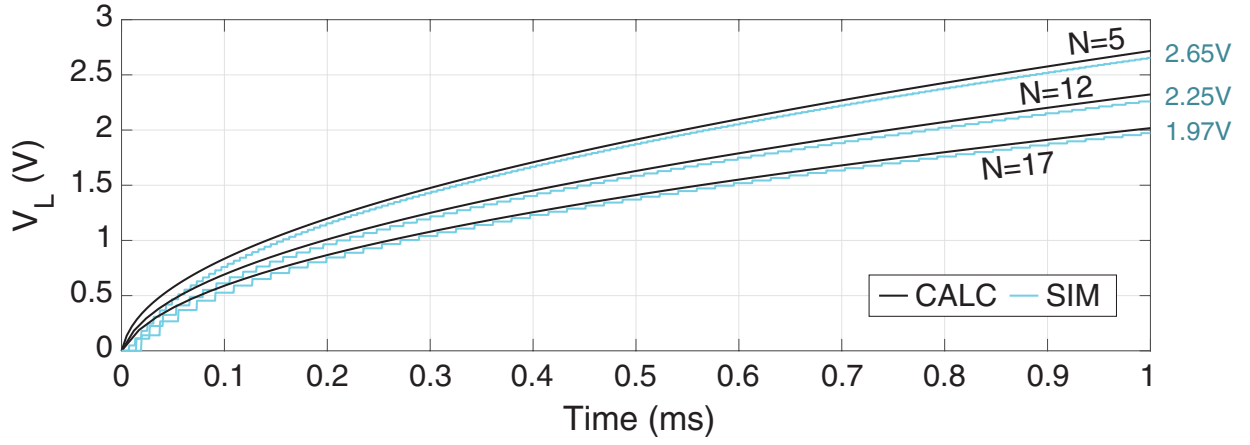


Figure 2.6: Calculated and simulated capacitive load voltage V_L over time, for different N values.

between the two curves in each case is due to the applied approximations in calculations.

2.3.4 Energy Analysis

The envelope of the accumulated energy in L_2C_2 tank during resonance mode is obtained from

$$E_{LC(peak)} = 0.5L_2i_{L2(peak)}^2. \quad (2.12)$$

Therefore, by using (2.6), the maximum stored energy in L_2 after N resonance cycles will be

$$E_{LC(peak),N} = 0.5L_2 \left(-\frac{|V_{ind(21)}|}{R_{2eq}} e^{-\alpha N/f_o} + \frac{|V_{ind(21)}|}{R_{2eq}} \right)^2. \quad (2.13)$$

on the other hand, the ohmic energy loss of $R_{2eq} = R_2 + R_{SW1}$ during resonance mode is

$$E_{Loss(res)} = \int_0^{t_{res}} i_{L2}^2(t) R_{2eq} dt, \quad (2.14)$$

where t_{res} is the duration of the resonance mode calculated as N/f_o . As i_{L2} amplitude is not constant for all N resonance cycles, the losses should be evaluated separately for each cycle i ($1 \leq i \leq N$):

$$\begin{aligned} E_{Loss(res)} &\cong \int_0^{t_{res}} \left(\left(-\frac{|V_{ind(21)}|}{R_{2eq}} e^{-\alpha t} + \frac{|V_{ind(21)}|}{R_{2eq}} \right) \cos(\omega_o t) \right)^2 R_{2eq} dt \\ &= 0.5 R_{2eq} \sum_{i=1}^N \left(-\frac{|V_{ind(21)}|}{R_{2eq}} e^{-\alpha i/f_o} + \frac{|V_{ind(21)}|}{R_{2eq}} \right)^2 T. \end{aligned} \quad (2.15)$$

From the above analysis, the total incident energy (E_{in}) at the Rx coil after N resonance cycles could be written as the sum of expressions in (2.13) and (2.15). Fig. 2.7(a) represents a comparison between simulated $E_{Loss(res)}$ and its calculated value from (2.14) along with its approximated value in (2.15) for link1 in Table 2.1. It is noted that all curves follow the same trend despite the small difference between them.

The energy loss during charging mode ($E_{Loss(ch),k}$) is due to $i_{L2(ch)}$ in (2.7) passing through R_2 and R_{SW2} . To consider the losses due to C_L 's equivalent series resistance (ESR) during this mode, ESR value could be added to R_{SW2} as the two are in series. The conduction loss during k^{th} charging event is therefore calculated by integrating the dissipated power over the charging time

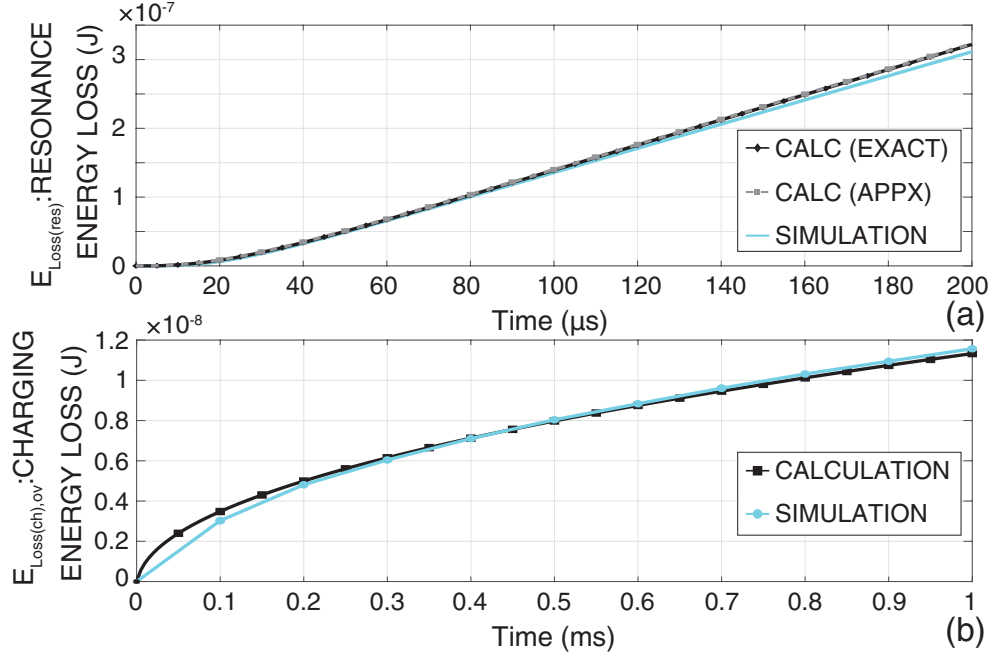


Figure 2.7: Calculated and simulated energy loss over time during (a) resonance-mode (b) charging-mode.

(t_{ch}) ,

$$\begin{aligned}
 E_{Loss(ch),k} &= \int_0^{t_{ch}} i_{L2(ch)}^2(t) (R_2 + R_{SW2} + R_{ESR}) dt \\
 &= (R_2 + R_{SW2} + R_{ESR}) \left(\frac{L_2 i_{L2(peak),N}^3}{3V_{L(k)}} \right).
 \end{aligned} \tag{2.16}$$

From (2.16), it is concluded that $E_{Loss(ch),k}$ is cubically proportional to $i_{L2(peak)}$ at the onset of the charging mode (i.e., end of resonance mode) and is inversely proportional to $V_{L(k)}$ which would be the final voltage on C_L at the end of k^{th} charging event, as defined in (2.11). Therefore, $E_{Loss(ch),k}$ does not remain constant and decreases over the entire charging period as V_L is

growing. This is the main reason that we must consider the overall time (t_{ov}) in our optimization process and N_{opt} cannot be calculated by only considering a single pair of resonance-charging events. The overall charging loss $E_{Loss(ch),ov}$ for m charging events during t_{ov} is

$$E_{Loss(ch),ov} = \sum_{k=1}^m E_{Loss(ch),k} \neq m \times E_{Loss(ch),N}. \quad (2.17)$$

Fig. 2.7(b) depicts the simulated and calculated $E_{Loss(ch),ov}$ versus elapsed time. For this plot, equations (2.11), (2.13), (2.16), and (2.17) are used for $E_{Loss(ch),ov}$ calculation and N is selected to be 5.

2.3.5 Maximizing Available Energy to the Load

Having modeled the expressions for energy accumulation and loss during both modes of operation, we are ready to find the expression for the theoretically-maximum possible energy that could be stored in C_L during a fixed charging period (t_{ov}). A conceptual timing diagram of energy storage in a CM receiver for different resonance-to-charging switching moments is illustrated in Fig. 2.8(a). As shown, for the same overall charging time t_{ov} (e.g., the time between two data transmission bursts), adopting different switching timing could considerably vary the overall stored energy (i.e., $V_{L(max2)} > V_{L(max1)} > V_{L(max3)}$).

In this figure, the periods with a white background represent the resonance episodes where

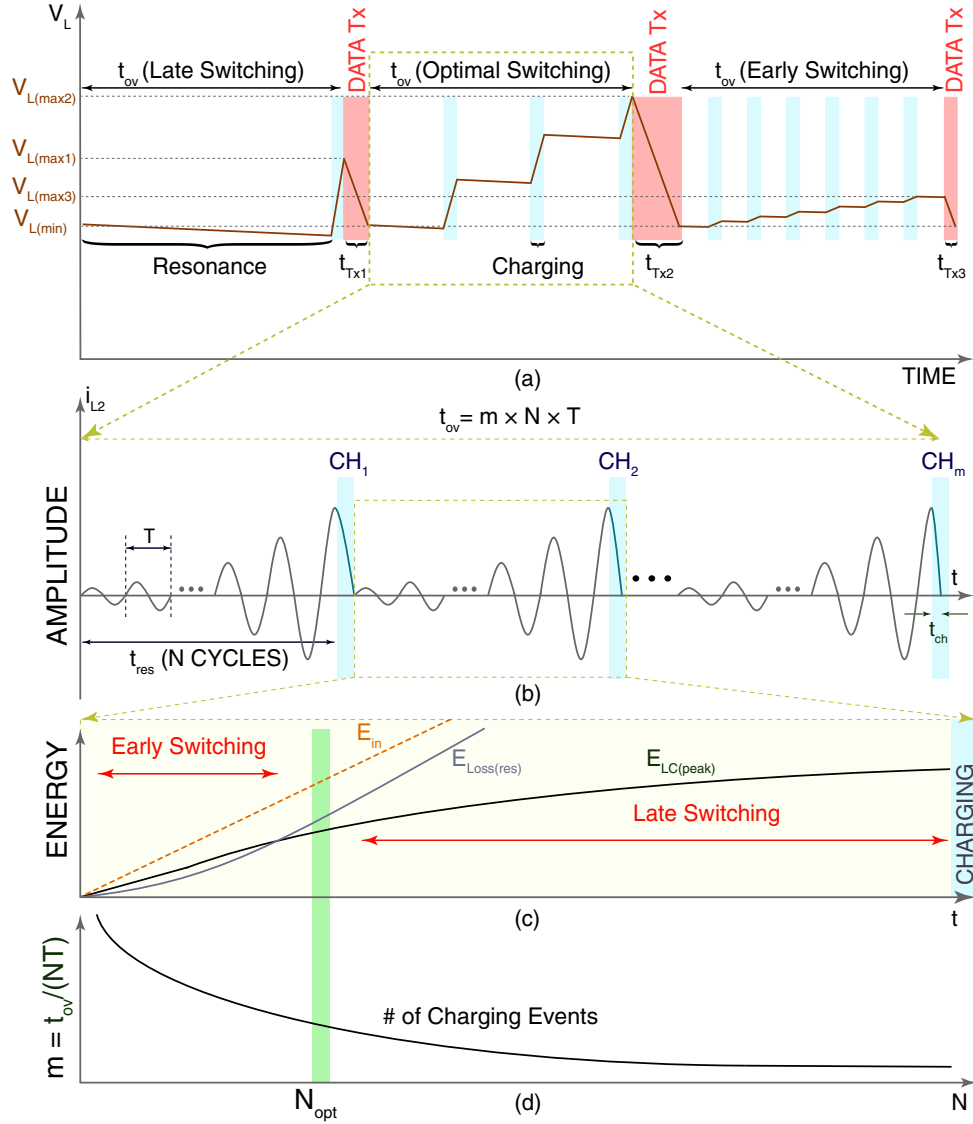


Figure 2.8: Capacitive load charging in CM receivers: (a) conceptual timing diagram of energy storage and consumption for optimal, early, and late switching (b) transient waveforms during multiple charging and resonance episodes during t_{ov} ; (c) energy accumulation and loss during resonance mode, illustrating early, optimal, and late switchings; (d) number of charging events versus N .

the Rx resonance tank is accumulating the incident energy and does not provide anything to the load. During this time, the slow decay in V_L represents the required power for R_{L1} -type of loads (i.e., the low-continuous type of loads defined in Chapter 1), which is supplied by C_L . During the light blue periods, which represent the charging episodes, the C_L is charged despite the small discharge current due to R_{L1} -type loads.

Comparing the given cases, it is evident that the occurrence rate of these charging events has a critical role in the final energy available for data transmission (or other high-intermittent loads represented by R_{L2} -type loads) at the end of each t_{ov} (e.g., $t_{Tx2} > t_{Tx1} > t_{Tx3}$). Therefore, maximizing the overall energy storage during t_{ov} is strongly dependent on the cycle that the resonant-to-charging transition takes place and hence, defining the N_{opt} cycle that is associated with it provides a potential for adaptively detecting the optimal charging condition for any CM receiver.

Fig. 2.8(b) shows the time-domain illustration of receiving coil's current (i_{L2}), which represents the energy build-up and depletion in the receiver's L_2C_2 tank during resonance and charging modes, respectively. Fig. 2.8(c) provides a graphical representation of the total received energy (E_{in}), the total accumulated energy that gets exchanged in the receiver's L_2C_2 tank ($E_{LC(peak)}$) from (2.12) or (2.13), and the total dissipated energy ($E_{Loss(res)}$) from (2.14) or (2.15), all during resonance mode versus elapsed time. The figure illustrates that $E_{Loss(res)}$ surpasses $E_{LC(peak)}$ long before i_{L2} plateaus. Therefore, the longer (higher number of cycles) we stay in the resonance

mode, the peak value of induced current will increase, hence, the resistive losses will increase. In other words, with increasing the resonance cycles, N , the energy exchange between the capacitor and the inductor in the L_2C_2 tank becomes increasingly lossy, therefore, the E_{LC} growth and the energy build-up pace slows down and eventually plateaus. A non-growing E_{LC} means that the entire incident energy is wasted on the ohmic losses of the resonance circuit. Therefore, switching to the charging mode after reaching a certain i_{L2} threshold value is considered as late switching which will result in the majority of the incoming energy to be wasted in the Rx rather than getting efficiently transferred to the load.

On the other hand, going to the charging mode temporarily takes the link out of resonance, which is a discouraging factor for too frequent switching. Furthermore, the resonance-to-charging transition is a lossy process, which is another incentive for reducing the number of times the link goes to the charging mode during a fixed period t_{ov} . The above indicates that the resonance-to-charging transition must happen after the first few cycles (i.e., not too early) and before the energy accumulation process is slowed down (i.e., not too late).

To find the optimal number of cycles (N_{opt}) that results in maximum overall link's energy storage efficiency, all resonance and charging episodes during the overall time period t_{ov} must be considered. For a given t_{ov} , N , and resonance frequency f_o at which the link is tuned, the number

of charging events m (shown in Fig. 2.8(d)) is

$$m = \frac{t_{ov}}{t_{res}} = \frac{t_{ov}}{NT} = \frac{t_{ov}f_o}{N}, \quad (2.18)$$

neglecting the very short charging time t_{ch} , compared to the resonance time, t_{res} . Thus, using (2.12), the total energy made available by m resonance episodes is equal to:

$$\begin{aligned} E_{Available} &= \left(0.5 \frac{Q_{2eq}R_{2eq}}{\omega_o} i_{L2(peak),N}^2 \right) \times \frac{t_{ov}\omega_o}{2\pi N} \\ &= \frac{Q_{2eq}R_{2eq}}{4\pi} \frac{i_{L2(peak),N}^2}{N} t_{ov} = \frac{1}{4\pi(Q_{2eq}R_{2eq})} \frac{V_{Rx(peak),N}^2}{N} t_{ov}. \end{aligned} \quad (2.19)$$

The dependency of $E_{Available}$ on the inductive link's physical parameters is apparent in $Q_{2eq}R_{2eq} = \omega_o L_2$ term, which would be a constant value at the link's frequency of operation. Therefore, it is concluded from (2.19) that to maximize the $E_{Available}$ for a given inductive link with invariant physical parameters (e.g., coil geometry, quality factor, etc.) at a fixed resonance frequency, the $i_{L2(peak)}^2/N$ term must be maximized. Intuitively, the equation suggests that $E_{Available}$ is proportional to $i_{L2(peak)}^2$ (or $V_{Rx(peak)}^2$), which defines the peak accumulated energy after N cycles, and is proportional to $1/N$, which defines the overall number of times that Rx is able to switch to charging mode. The energy transferred to the load (E_{Load}) is then obtained by subtracting the total charging loss ($E_{Loss(ch),ov}$) from the $E_{Available}$. As a result, if Rx remains in resonance mode for N_{opt} number of cycles, $E_{Available}$ and consequently E_{Load} will be maximized. It should be

noted that the peak of E_{Load} might not occur when the rate of E_{LC} growth is maximum and is solely defined by $i_{L2(peak)}^2/N$.

To demonstrate the effectiveness of $E_{Available}$ expression in (2.19), $E_{Available}$ and E_{Load} are calculated for different N values while keeping the overall time to $t_{ov} = 2\text{ ms}$ (a reasonable arbitrary value). Fig. 2.9(a) plots the calculated $E_{Available}$ and E_{Load} along with $E_{LC(peak)}$ for different resonance mode durations in terms of N and compares them with simulated E_{Load} based on the link1 parameters in Table 2.1. As inferred from the graph, both analytical model and simulation results agree that the N value (i.e., $N = 5$ here) that maximizes the energy storage in load capacitor is the same N value that results in maximum $E_{Available}$. As expected, the $N = 5$ is nowhere close to when the energy accumulated in the L_2C_2 tank is close to its maximum. The plot makes it clear that if we follow the conventional method for CM receivers and wait until a certain level of energy is accumulated in the L_2C_2 tank (e.g., $N = 20$ when we are close to the plateau), we will have $\sim 50\%$ less energy stored in the load capacitor at the end of 2ms interval.

2.3.6 Overall Charging Efficiency

The overall Rx efficiency (η_{Rx}) could be divided into resonance and charging efficiencies. The resonance efficiency (η_{res}) is the ratio of the accumulated energy in L_2C_2 tank to the total incident energy during resonance mode (E_{LC}/E_{in}). The charging efficiency (η_{ch}) is the ratio of the stored energy in C_L to the accumulated energy in L_2C_2 tank ($E_{Load(Final)}/E_{LC}$). Therefore, for m

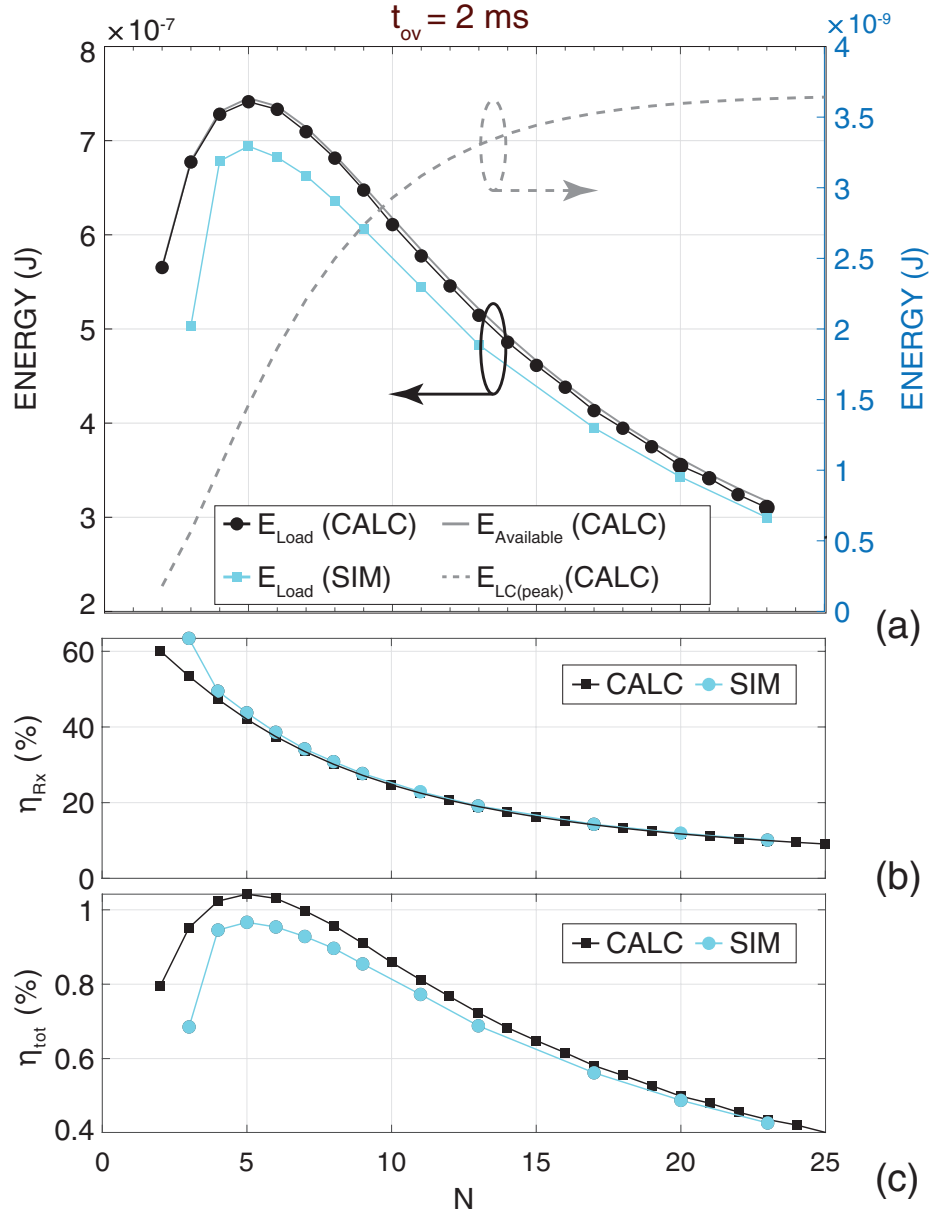


Figure 2.9: Comparison between calculated and simulated (a) $E_{Available}$, E_{Load} , $E_{LC(peak)}$ (b) η_{Rx} and (c) η_{tot} for different resonance cycles N for link1 (described in Table 2.1) resonating at 1 MHz.

charging events, each preceded with N resonance cycles,

$$\eta_{Rx} = \frac{E_{Load(Final)}}{E_{in(Rx)}} = \frac{mE_{LC,N} - E_{Loss(ch),ov}}{m(E_{LC,N} + E_{Loss(res),N})} \quad (2.20)$$

where the total incident energy at the receiver ($E_{in(Rx)}$) is m times the sum of accumulated energy in L_2C_2 tank ($E_{LC,N}$) and the total resistive loss ($E_{Loss(res),N}$) during each N -cycle resonance episode, and the total accumulated energy in L_2C_2 tank ($m \times E_{LC,N}$) will be divided between the load ($E_{Load(Final)}$) and the overall charging losses ($E_{Loss(ch),ov}$). It must be noted that $E_{Loss(ch),k}$ in (2.16) decreases with increasing $V_{L(k)}$ during the charging process and is not the same for different charging events k . Hence, $E_{Loss(ch),ov}$ could not be considered as $m \times E_{Loss(ch),N}$ and (2.20) could not be further simplified. This is the main reason that the optimization cannot be done for each charging event and needs to be done for the overall charging time.

Fig. 2.9(b) shows that the simulated η_{Rx} along with its calculated counterpart closely match, which validates the performed energy analysis and circuit modeling. From this plot, it is clear that η_{Rx} could be misleading for small N values, as it indicates that minimizing N , i.e., maximizing the number of transitions between resonance and charging modes, results in a better charging efficiency. What is not captured by η_{Rx} is the fact that the inductive link goes out of resonance every time the receiver goes to the charging mode. Therefore, while decreasing N might result in increasing the portion of the incident energy that is stored in the load, it also means that the portion of transmitted energy that reaches the receiver coil is reduced. This is why the total

energy efficiency (i.e., from the source in the transmitter to the load in the receiver) must be considered and measured. Fig. 2.9(c) shows the $\eta_{tot} = E_{Load(Final)}/E_s$. As illustrated, the N_{opt} decided by our proposed algorithm results in maximizing the total energy efficiency from source to the load. It should also be noted that this optimization is regardless of the inductive link's efficiency, which depends on the coils physical and electrical parameters and the power transfer medium and is defined as P_{Rx}/P_{Tx} in Chapter 1.

Effect of C_L on the optimal cycle N_{opt}

To verify the accuracy of the proposed optimal solution, the C_L size was increased by three orders of magnitude above 100 nF and the simulated N_{opt} along with the simulated E_{Load} are shown in Fig. 2.10. As the figure shows, the N_{opt} is not changed for the entire C_L range, indicating the validity of the optimization model and its independency from C_L value. Although the stored energy is relatively steady up to 10 μ F, the level of stored energy is reduced by further increase in the C_L size. This is due to increase in the time required for charging a bigger C_L as a result of increase in the time constant of the charging circuit, which consequently reduces the overall possible number of resonance-charging episodes during a fixed t_{ov} . Fig. 2.11 shows how the simulated E_{Load} and η_{tot} are affected for different N when C_L size was changed to 200 μ F. Clearly, the N_{opt} still occurs at $N = 5$, as it was predicted by the model when simulated with a $C_L = 100$ nF (Fig. 2.9).

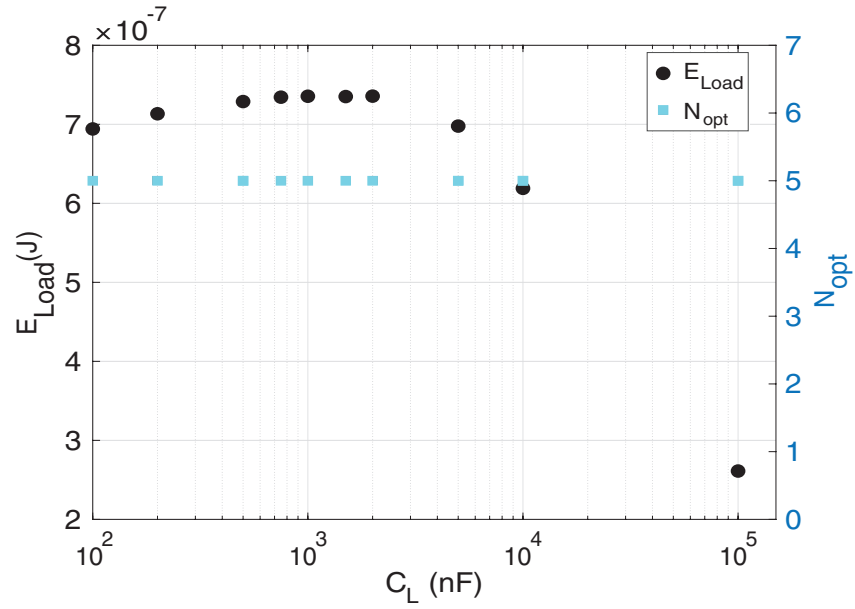


Figure 2.10: Simulated E_{Load} and N_{opt} vs. C_L sweep for link1.

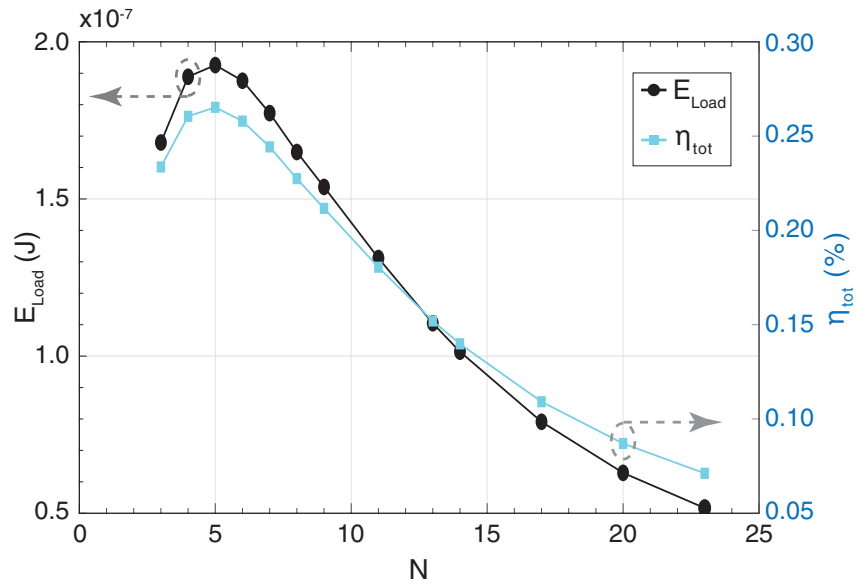


Figure 2.11: Simulated E_{Load} and η_{tot} vs. N for $C_L = 200 \mu\text{F}$ for link1.

Proposed Optimization versus Frequency and other Circuit Parameters

To further validate our model and optimization solution for different links with various geometries and operation frequencies, we studied the same performance metrics after changing the frequency of operation to 2 MHz, and C_1 and C_2 to 30.89 pF and 1.5 nF, respectively. Fig. 2.12 depicts the results for $t_{ov} = 1$ ms. Fig. 2.13 shows the obtained results when the Rx's L_2 , C_2 , R_2 , and $R_{SW1\&2}$ were changed to 39 μ H, 649.5 pF, 4 Ω , and 2.5 Ω respectively, and V_s was changed to 200 mV_(peak) at 1 MHz for $t_{ov} = 1$ ms. For the former case, maximum $E_{Available}$, E_{Load} , and η_{tot} occur at $N = 10$ for both calculation and simulation. For the latter case, maximum calculated $E_{Available}$, E_{Load} , and η_{tot} occur at $N = 14$ while the simulated maximums occur at $N = 13$.

The validity of the optimization model at a higher frequency of operation is examined for link3 with the parameters given in Table 2.1 at 6.78 MHz. Fig. 2.14 shows that the calculated and simulated N_{opt} closely match, which indicate the accuracy of the model in predicting the optimal condition with the increase in the frequency of operation. This is further verified by sweeping the frequency at which the link is tuned and comparing the model prediction with the N_{opt} cycle at which E_{Load} and η_{tot} are maximum. As shown in Fig. 2.15, both calculated and simulated results closely predict the optimal cycle when the frequency is changed from 1-20 MHz range.

It should be noted that for these cases the results are not shown up to the saturation point of i_{L2} , as both $E_{Available}$ and E_{Load} are clearly following a downward trend beyond the N_{opt} . This indicates that the optimal number of cycles for these links is much further away from the satu-

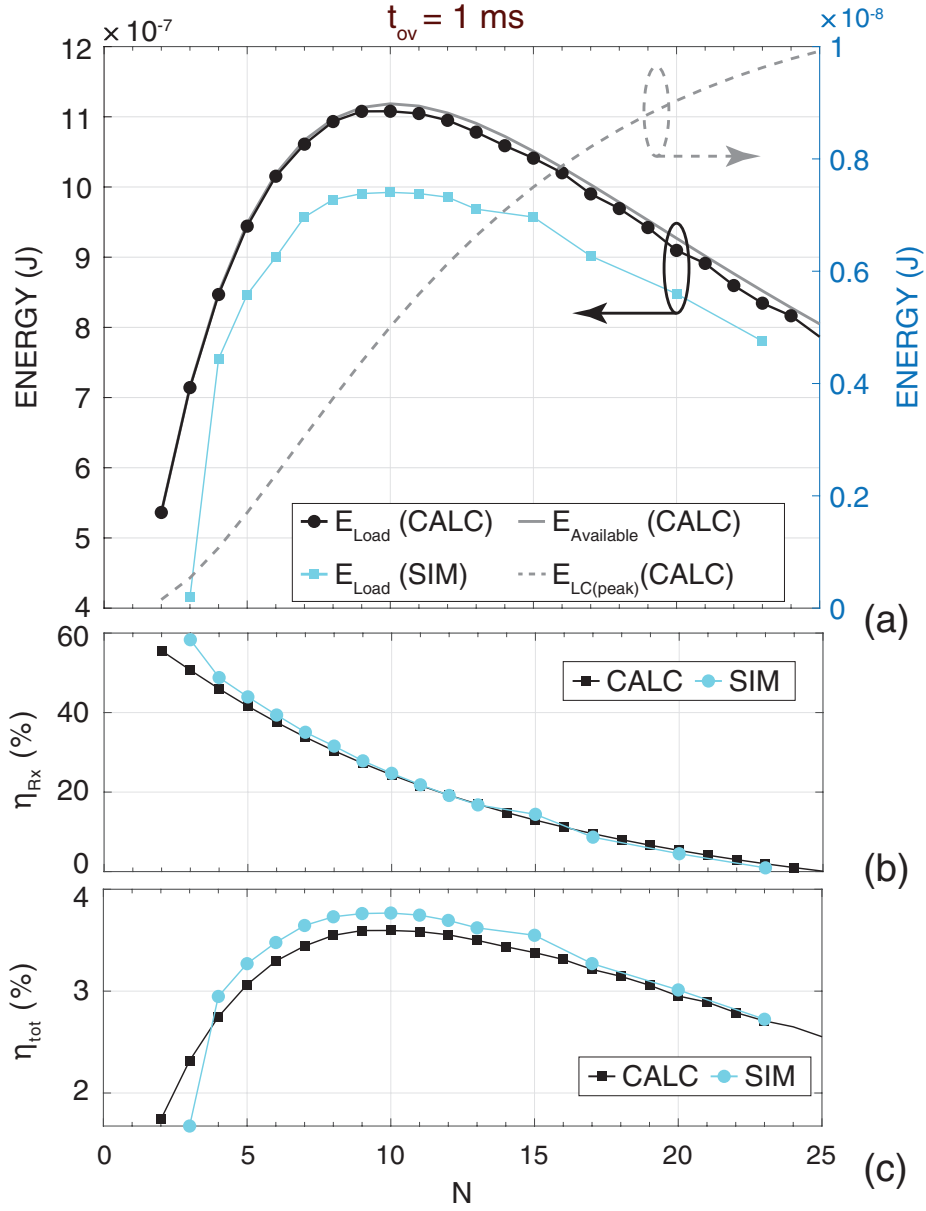


Figure 2.12: Comparison between calculated and simulated (a) $E_{Available}$, E_{Load} , $E_{LC(peak)}$ (b) η_{Rx} and (c) η_{tot} for different resonance cycles N for link1 (described in Table 2.1) modulated to resonate at 2 MHz by changing C_1 and C_2 .

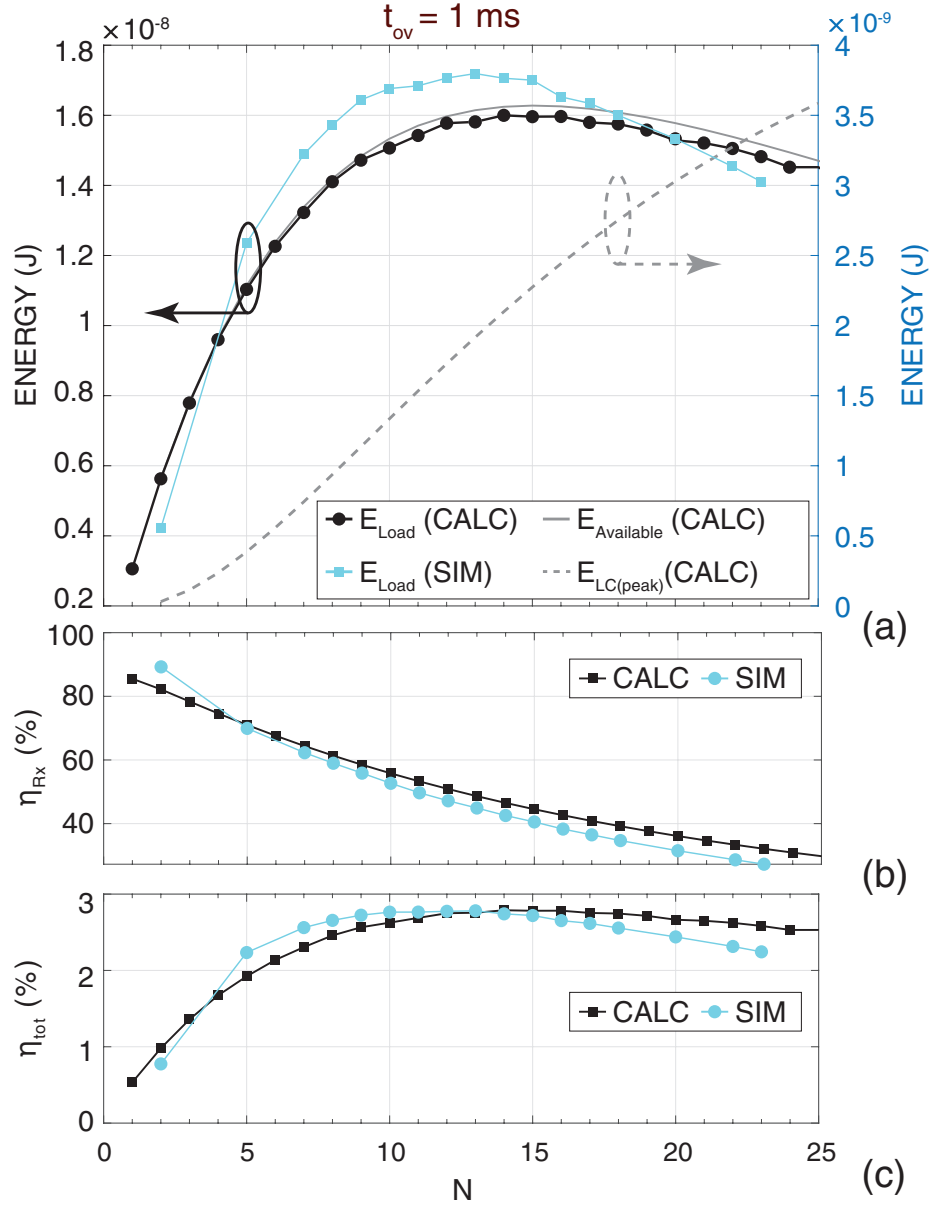


Figure 2.13: Comparison between calculated and simulated (a) $E_{Available}$, E_{Load} , $E_{LC(peak)}$ (b) η_{Rx} and (c) η_{tot} for different resonance cycles N for link2 (described in Table 2.1) resonating at 1 MHz.

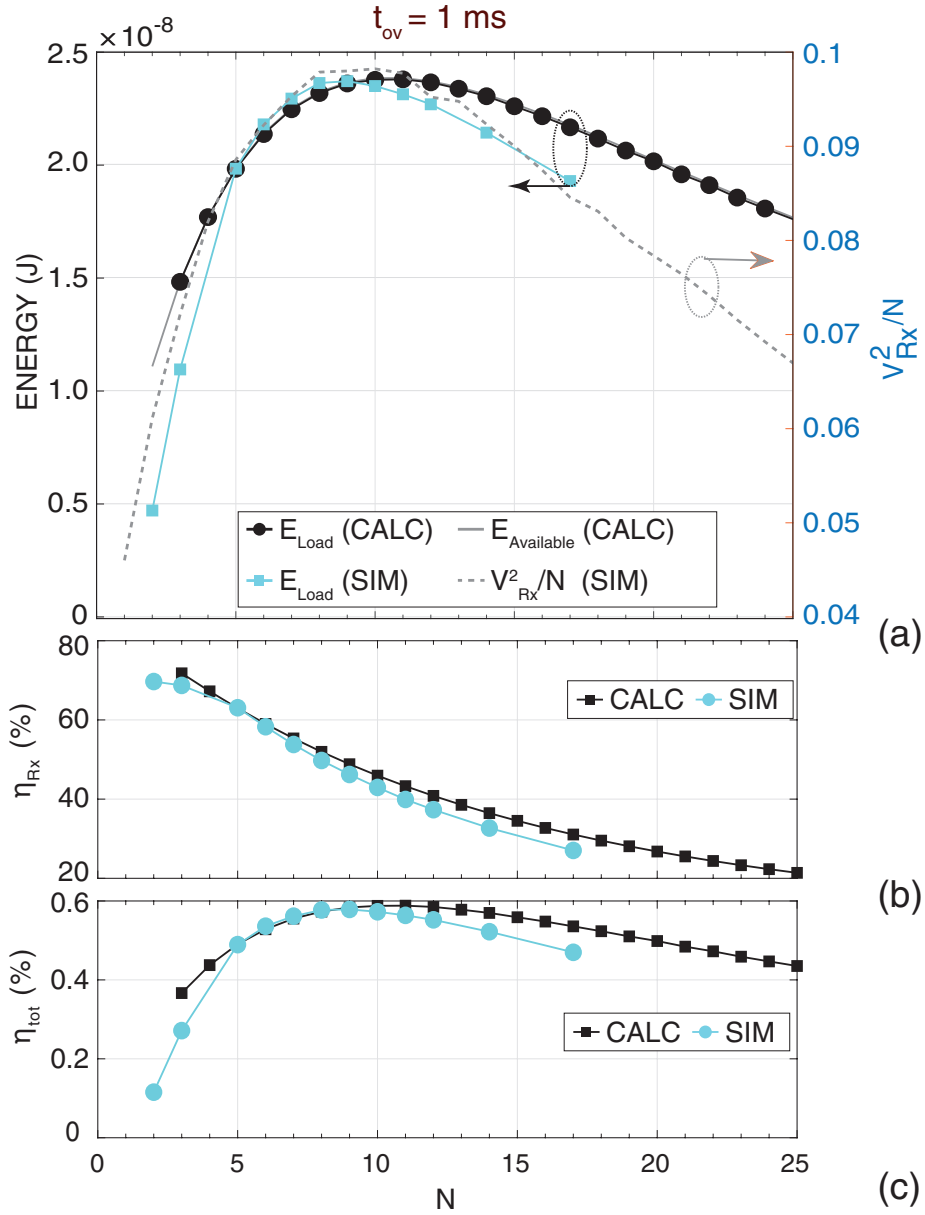


Figure 2.14: Comparison between calculated and simulated (a) $E_{Available}$, E_{Load} , $V_{Rx(peak)}^2/N$ (b) η_{Rx} and (c) η_{tot} vs. N for link3 (Table 2.1) resonating at 6.78 MHz.

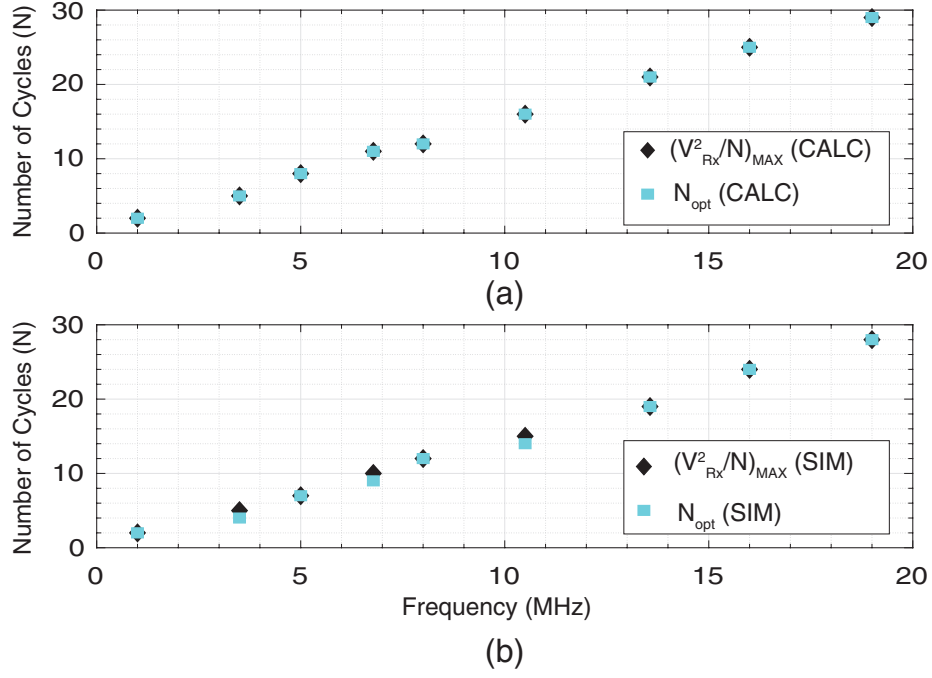


Figure 2.15: $V^2_{Rx(peak)}/N$ and N_{opt} vs. frequency sweep for link3 (a) calculated (b) simulated.

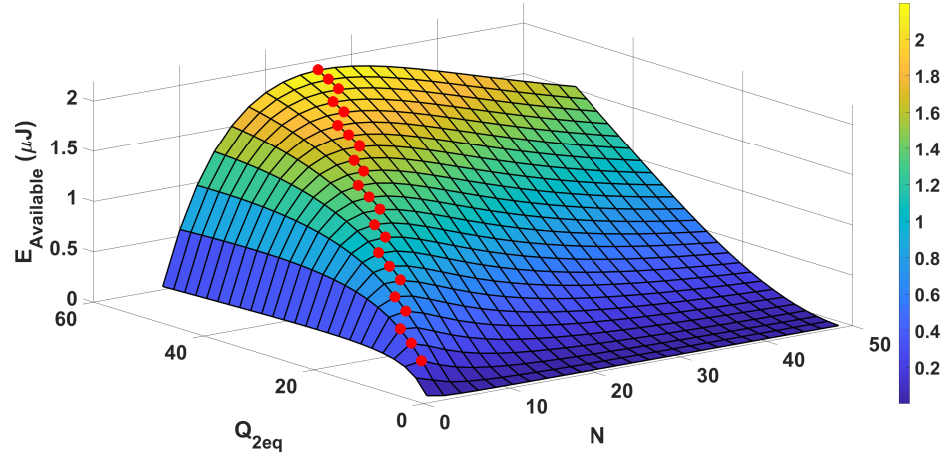


Figure 2.16: $E_{Available}$ vs. N and Q_{2eq} at $f_o = 1$ MHz and $t_{ov} = 2$ ms with N_{opt} annotation.

ration point of i_{L2} , therefore, the presented optimization scheme is more effective for receiving coils with higher quality factors. The effect of Q_{2eq} is shown in the 3-D plot of Fig. 2.16 where the maximum $E_{Available}$ at N_{opt} shifts to a higher N with the increase in the quality factor of Rx for a fixed resonance frequency.

Since V_{Rx} (or i_{L2}) is dependent on the supplied energy to the link (by the V_s source) and the link efficiency (η_{Link}) which is proportional to k , Q_1 , and Q_{2eq} , monitoring $V_{Rx(peak)}^2/N$ (or $i_{L2(peak)}^2/N$) presented in this work could facilitate the automatic detection of the optimal operation for energy storage in CM receivers in real-time, eliminating the need for any pre-programming or calibration phase. In addition, the provided solution has the potential of being adaptive to any inductive link with different coil parameters, physical distance, transmission medium, frequency of operation, and input power level, contingent to a low-power hardware implementation for $V_{Rx(peak)}^2/N$ calculation.

2.4 Measurement Results

As N_{opt} is shown to be dependent on the physical parameters of the Rx, two inductive links with different physical parameters were established to experimentally validate the provided maximum energy storage capability in CM receivers for two distinct cases. The coils (Würth Elektronik - WE-WPCC series: 760308103146, 760308102207, 760308100111, 760308102210) were con-

Table 2.2: Inductive links circuit parameters in measurements.

Parameters	Link4	Link5
f_o (MHz)	1.07	0.99
L_1/L_2 (μH)	8.0/8.6	8.0/6.4
R_1/R_2 (Ω)	1.76/0.67	0.40/0.32
C_1/C_2 (nF)	3.2/3.0	3.2/4.0
$R_{SW1(max)}$ (Ω)	0.48	0.48
C_L (nF)	100	100

nected to appropriately sized capacitors to resonate at ~ 1 MHz. The coil parameters (inductance and quality factor) were extracted from the manufacturer's datasheet. Table 2.2 provides the circuit parameters of the two established links. Due to the components' tolerance and parasitics, the resonance frequencies were measured to be 1.07 MHz and 0.99 MHz for link 4 and 5, respectively. The two links were used to charge a 100 nF capacitor using CM power Rx circuit. As mentioned in Section 2.3 and supported with simulation results, the N_{opt} cycle is not affected by the size of C_L as it only acts as an storage element in the circuit. It must be noted that the link's selected parameters are simply proof-of-concept examples and the presented optimization is applicable to various inductive links with different coil geometries and storage capacitor size, as long as they use a CM architecture.

Fig. 2.17 shows the measurement setup and top-level block diagram. The timing of the

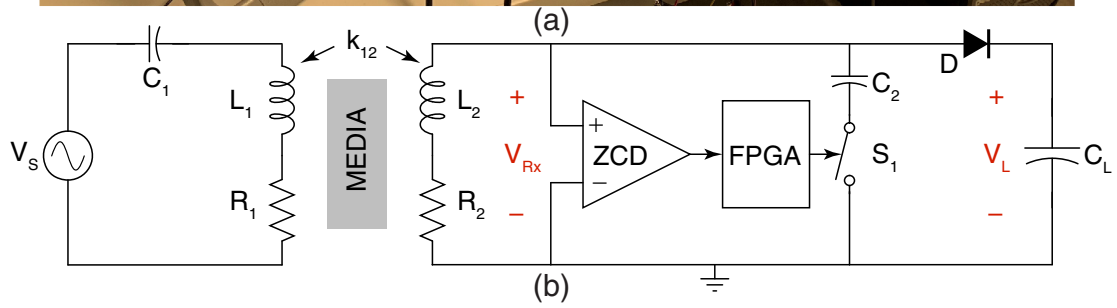
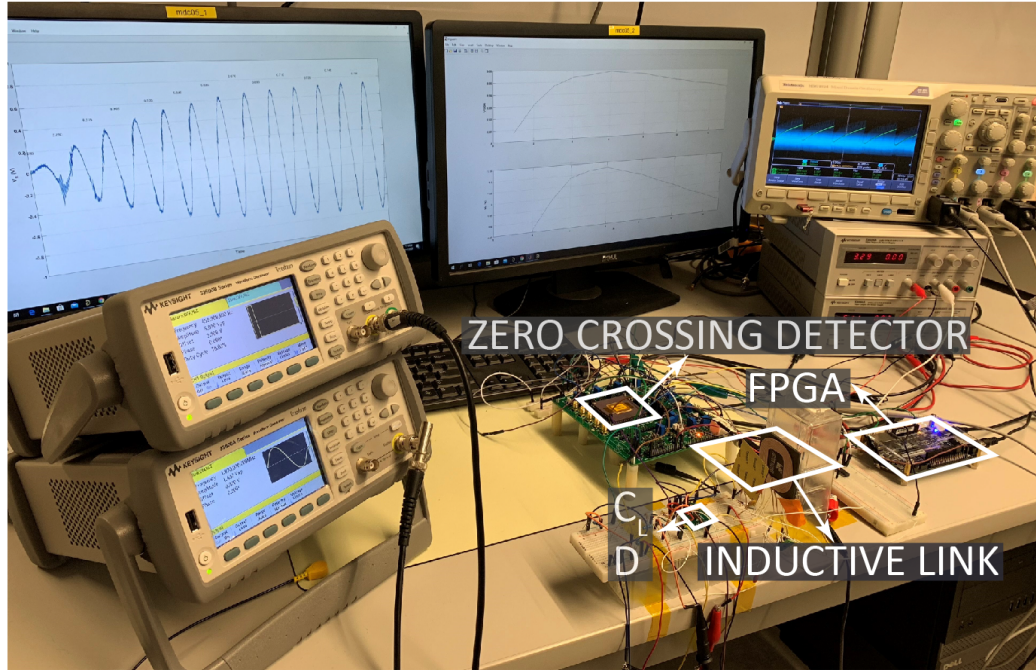


Figure 2.17: (a) Measurement setup and (b) its simplified block diagram (circuit parameters listed in Table II).

Rx circuit is controlled by an FPGA. A clockless comparator is used as a zero-crossing detector (ZCD) and its output is fed to the FPGA to be used for (a) counting the number of resonance cycles passed, (b) terminating the resonance mode by opening S_1 at the right cycle N and the right moment, and controlling the charging time. The switch S_1 (Analog Devices ADG842) and diode D are used to control the operating modes of the CM power receiver. The fast switching discrete diode (ON Semiconductor 1N4148) with V_D of 0.75 V at 10 mA forward current was preferred over another switch (S_2) to allow current only in one direction and prevent the C_L from discharging.

The main reason for implementing S_2 as a diode is that once all the accumulated energy in L_2 from the resonance mode is transferred to the load capacitor C_L (i.e., end of charging and perfect moment to start the next resonance episode), the diode prevents the C_L from discharging back as it does not allow current to flow in the reverse direction. However, if a MOS switch is used for S_2 , then it has to be turned off exactly when the charging is over, otherwise it could result in a significant part of the stored energy to discharge back in the power receiving circuit.

While, based on the above, using the diode makes the late switching relatively harmless, early switching (back to resonance) is still something that needs to be avoided, otherwise, only a fraction of the accumulated energy in L_2 will be transferred to the C_L . To avoid early switching, we programmed the link turn ON S_1 and to go back to the resonance mode $t_{ch(max)}$ seconds after the charging started, where $t_{ch(max)}$ is the worst case scenario (i.e., the longest charging time) that

happens at the smallest V_L based on (2.10). The fact that we can afford a slight late switching is a great advantage as it makes us needless of a power-hungry high-speed comparator to compare V_{Rx} and V_L and turn OFF the switch when the two voltages are equal (indicating end of charging) in order to prevent C_L from discharging [53]. Of course, all diodes have a very small reverse current that should be considered. But it should be noted that (a) the magnitude of the reverse current is typically negligible (e.g., 0.00025% of the forward charging current for 20 V reverse voltage across the diode in the links we tested) and definitely much smaller than the loss that could happen due to late/early turn-off for S_2 , and more importantly (b) it causes a very small offset in the magnitude of the stored energy and not the optimal operating point (i.e., the N_{opt}). Therefore, it won't change the presented optimization solution.

Fig. 2.18(a) shows the measured V_{Rx} for $N = 13$ (as an example). For the overall time of $t_{ov} = 2\text{ ms}$, making the transition at $N = 13$ translates into ~ 162 consecutive charging events (each one allowed to last for $\sim 240\text{ ns}$). At the end of 2 ms interval, the combined effect of these charging events results in the load capacitor voltage of 0.91 V , as shown in Fig. 2.18(b). Fig. 2.19(a) shows the measured voltage on the load capacitor C_L over the 2 ms interval for different N values. Fig. 2.19(b) shows the simulated and measured final voltage on C_L at $t_{ov} = 2\text{ ms}$ for each N . The simulation and measurements confirm that $N = 7$ and $N = 6$ result in the highest amount of energy to be transferred into the load capacitance, respectively.

We ran several tests to experimentally find the optimal N value for resonance-to-charging

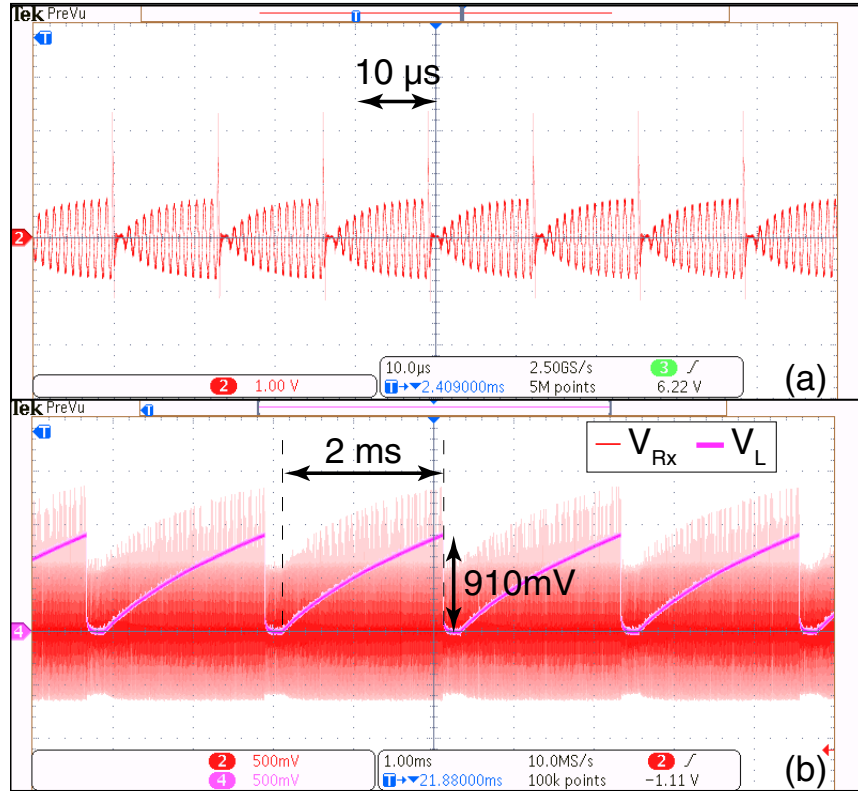


Figure 2.18: Measured waveforms of inductive link4 for $N = 13$ (a) V_{Rx} for a few resonance-charging episodes, and (b) V_L and V_{Rx} for $t_{ov} = 2\ \text{ms}$.

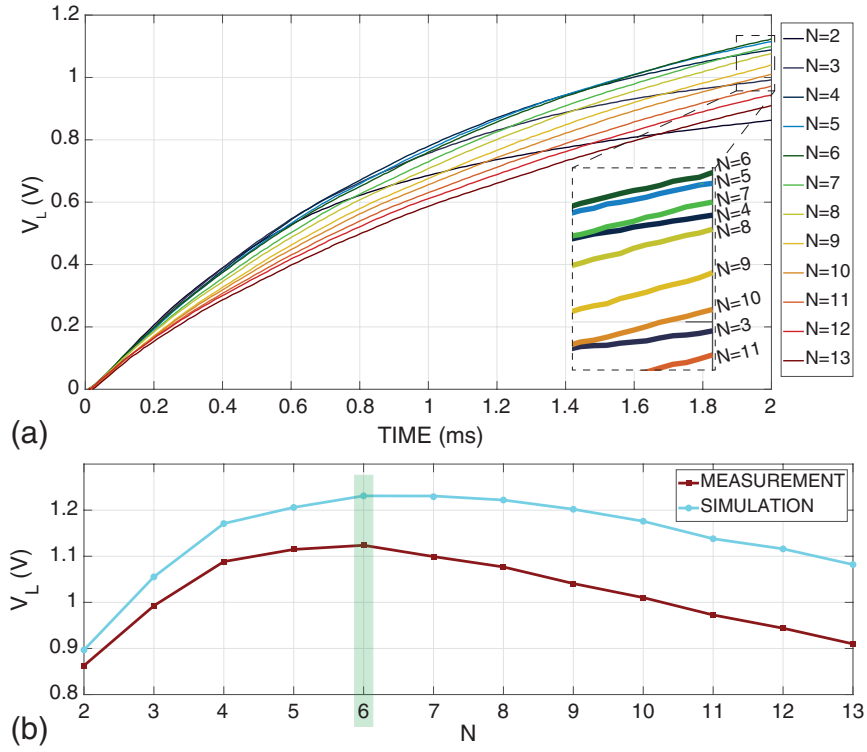


Figure 2.19: Link4's (a) measured voltage on the load capacitor C_L for different N values, and (b) measured and simulated V_L vs. N resonance cycles for $t_{ov} = 2$ ms.

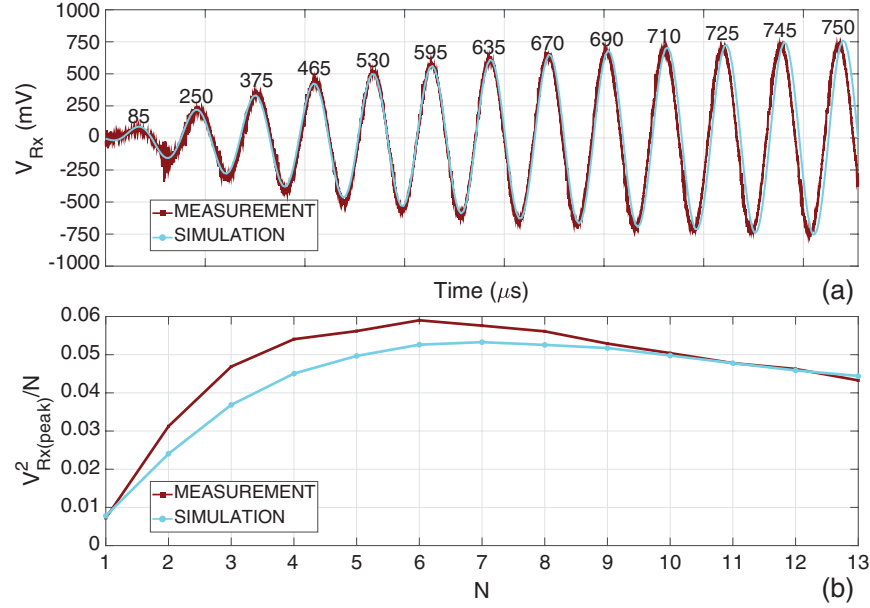


Figure 2.20: Measured vs. simulated waveforms of link4: (a) induced transient V_{Rx} with measured peak annotated for each cycle, and (b) $V_{Rx(peak)}^2 / N$ versus number of resonance cycles N .

transitions, and compared the result with the value obtained from our analytical model. In doing so, the FPGA was programmed to operate the CM receiver (in link4) with $N = 2$ to 13 and the voltage on C_L was monitored for each case.

To cross-validate our model's result with the experimental data, according to (2.19), we needed to find the N that maximizes the $i_{L2(peak)}^2 / N$. Instead, we decided to calculate the N that maximizes $V_{Rx(peak)}^2 / N$, since in the receiver's L_2C_2 tank, the $i_{L2(peak)}$ and $V_{Rx(peak)}$ increase at the exact same rate during resonance (shown in Fig. 2.1(c)). This allows for replacing ac current measurement with simple voltage measurement using oscilloscope. Fig. 2.20(a) shows the transient simulated and measured V_{Rx} with annotation of the measured peak values at each resonance

cycle for 13 cycles (link4). Fig. 2.20(b) shows the calculated $V_{Rx(peak)}^2/N$ for the simulated and measured V_{Rx} , both confirming the same optimal N values as what was observed in Fig. 2.19(b). As evident from figures 2.19 and 2.20, early or late switching either before or after N_{opt} would result in a significant reduction in V_L and hence E_{Load} , as well as η_{tot} of the link. For the measured case, switching at N_{opt} results in 69.68% and 52.54% improvements in E_{Load} compared to early switching at $N = 2$ and late switching at $N = 13$, respectively. As expected, the model is perfectly capable of predicting that switching at $N = 2$ results in a lower V_L compared to $N = 13$, $N = 12$, etc. in addition to predicting N_{opt} .

To verify the precision of the model in N_{opt} prediction, Fig. 2.21 shows the measurement results for link5 for $t_{ov} = 1.5\ ms$ in addition to the measured results of link4 for $t_{ov} = 2\ ms$ for the sake of comparison. As shown, the measured V_L (Fig. 2.21(b)) and what the model predicts (Fig. 2.21(a)) both indicate the same value for N to maximize the energy storage in the load capacitor. This figure also illustrates how accurate the model is in predication of the N_{opt} as the value was changed only by one (i.e., from $N = 6$ to $N = 5$). For this link, switching at N_{opt} results in 41.42% and 67.47% improvements in E_{Load} compared to early switching at $N = 2$ and late switching at $N = 13$, respectively. As expected from the model prediction, switching at $N = 2$ resulted in a higher V_L compared to $N = 11, 12, 13$ for this link.

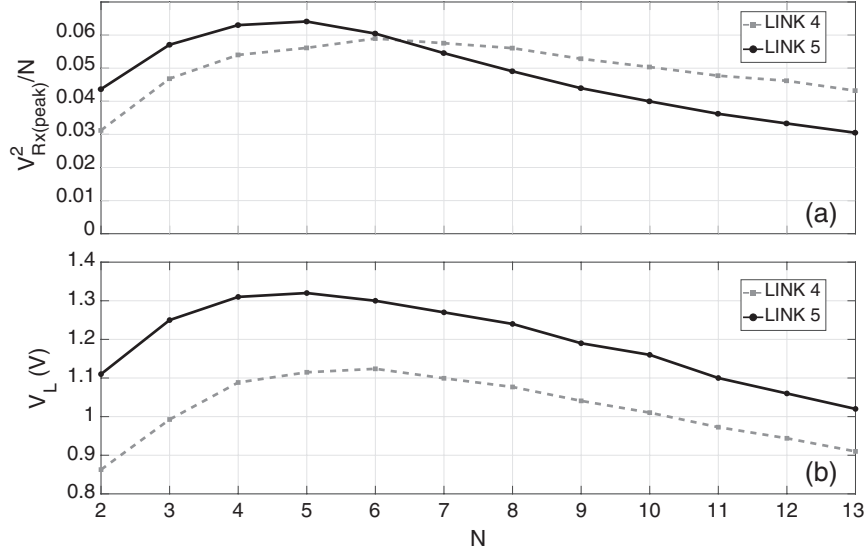


Figure 2.21: Measured waveforms of links 4 and 5: (a) $V_{Rx(peak)}^2/N$, and (b) V_L , both versus N ($t_{ov} = 2 \text{ ms}$ for link4 and $t_{ov} = 1.5 \text{ ms}$ for link5).

2.5 Conclusion

In this chapter, we presented the development and validation of an energy storage optimization algorithm for inductive current-mode power receivers. A detailed description of theoretical analysis considering various types of energy loss and storage during different operation phases of these receivers was provided. The proposed optimization scheme yield a timing solution that results in maximizing the stored energy in a capacitive load at the maximum possible charging efficiency within a pre-determined period of time. Since the algorithm continuously receives key electrical parameters of the inductive receiver as inputs, its solution is adaptive to any intentional or random changes in the link or the environment, conditional to a low-power circuit implemen-

tation for evaluating the presented optimal condition (which is the main topic of Chapter 3). We have validated the precision and efficacy of the algorithm in maximizing overall link's energy storage efficiency using both simulation and measurement results. Compared to the state of the art, the proposed method has the advantage of being applicable to any generic current-mode inductive power receiver, while being needless of pre-programming or calibration.

Chapter 3

A Calibration-Free Energy-Efficient IC for Link-Adaptive Real-Time Overall Link's Energy Storage Optimization of CM Inductive Power Receivers

3.1 Introduction

As discussed in the previous chapter, CM receivers operate in two modes of resonance and charging. Mode transitions are performed by a controller through two switches S_1 and S_2 as shown in Fig. 3.1. The work described in this chapter is the design and implementation of the on-chip "operation and timing controller" block, shown in Fig. 3.1, that is responsible for optimally con-

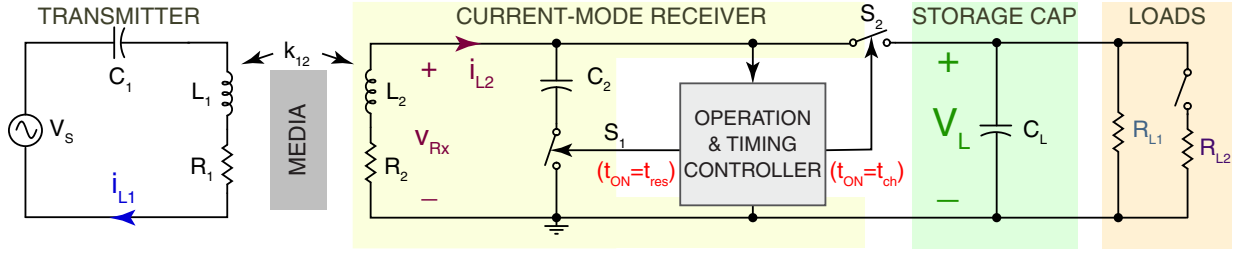


Figure 3.1: A simplified circuit diagram of a CM receiver and how it is interfaced with a controller module that decides the receiver's mode of operation (resonance or charging) through S_1 and S_2 .

trolling the timing of these mode transitions in real time and in an adaptive fashion. During the resonance mode, S_1 must be closed to allow the energy build-up at the receiver by forming the L_2C_2 resonant tank. The receiver should stay in this mode for a multitude of cycles to accumulate sufficient energy while S_2 is open to isolate the load capacitor C_L from the link. After N cycles, the receiver is switched to the charging mode by opening S_1 and closing S_2 to transfer the accumulated energy to the load in a boost converter fashion. Once the charging is completed, the receiver goes back to resonance again and the process is repeated. During charging mode, the energy transfer to the capacitive load (C_L) is done through the Rx inductor's current (i_{L2}). Therefore, the perfect moment in a cycle for resonance-to-charging transition is when all the accumulated energy is stored in L_2 (i.e., when i_{L2} peaks and $V_{Rx} = 0$). In addition, as discussed in the previous chapter, the number of cycles (N) that the receiver stays in resonance is a decisive factor in its overall power delivery performance.

To the best of our knowledge, no integrated design has been yet reported in literature that

can provide a universal (i.e., link independent) and adaptive (to any random or intentional variations) solution for on-the-fly detection and adoption of an N_{opt} that maximizes the overall link's energy storage efficiency. In this chapter, the practical challenges and considerations for on-chip implementation of the optimal operation scheme is discussed. Next, we present the design and development of a low-power analog integrated circuit that automatically determines a CM receiver's optimal timing scheme (based on the theoretical model presented in Chapter 2), and steers it accordingly to achieve maximum energy storage. The IC continuously monitors the waveform at the receiver (Rx) coil, hence, yields an optimal solution that is adaptive to random/intentional variations in the link's parameters. The circuit is designed and fabricated in a standard $0.18\ \mu\text{m}$ CMOS process and its optimization precision, efficacy in energy storage maximization, and adaptiveness are verified using experimental measurements.

The rest of the chapter is organized as follows. Section 3.2 provides an overview of the required system-level architecture for optimal condition detection based on the theoretical modeling and experimental verification presented in Chapter 2. Section 3.3 describes the detailed design and implementation of the low-power mixed-signal circuits used in the presented IC. Section 3.4 presents the experimental validation of the fabricated chip and Section 3.5 concludes the chapter.

3.2 System-Level Architecture for Optimal Point Detection

3.2.1 Theory Recap

Fig. 3.2(a) shows the Rx inductor's current waveform for a few resonance episodes and charging events [122]. Fig. 3.2(b) shows both the energy lost ($E_{Loss(res)}$) and accumulated (E_{LC}) in L_2C_2 tank during multiple resonance cycles of one resonance episode. As illustrated, E_{LC} initially grows fast, but with the gradual energy build-up, the ohmic losses of R_2 (L_2 's resistance) and R_{SW1} (S_1 's resistance) also increase, thus the accumulation slows down and eventually saturates. Even before E_{LC} 's saturation, the energy loss surpasses it, meaning that more energy is lost than accumulated. So it is rational to stop the resonance at this point and transfer the accumulated energy to a storage capacitor and start over. Therefore, late resonance-to-charging switching (i.e., staying in the resonance mode until energy accumulation plateaus) is highly inefficient [122]. On the other hand, early (too frequent) resonance-to-charging switching is not desired either, as it results in an inadequate energy accumulation in L_2C_2 tank by not allowing enough time for the tank to effectively resonate. Moreover, the charging process is not lossless and going to charging too frequently results in wasting the little accumulated energy on overcoming the charging losses.

If only one charging event (i.e., $m = 1$ as defined in Fig 3.2(a)) is considered, the optimal cycle for switching from resonance to charging would be the cycle at which $E_{Loss(res)}$ surpasses

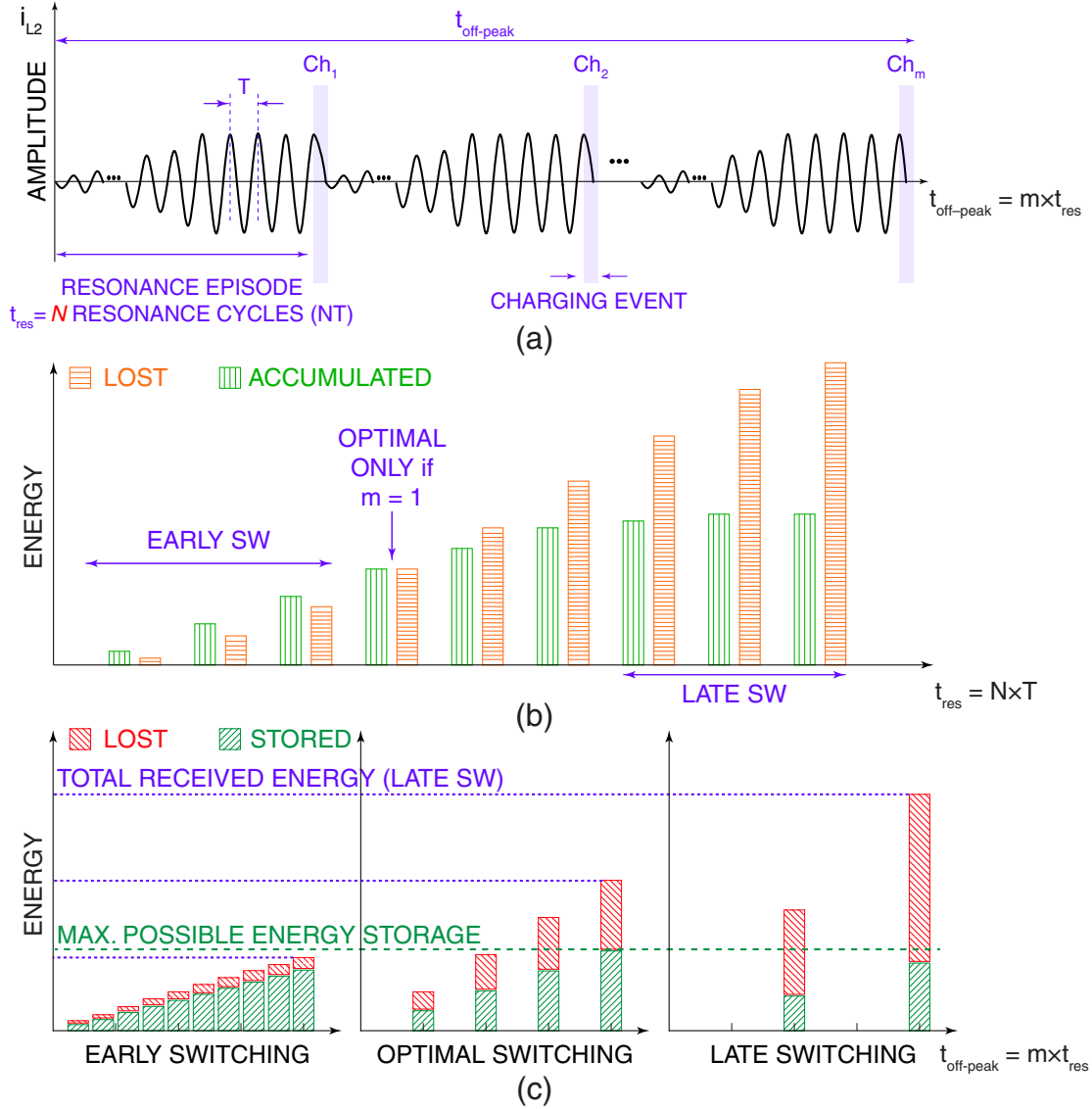


Figure 3.2: (a) Rx inductor's current waveform during $t_{off-peak}$ that includes multiple resonance episodes and charging events. (b) Energy accumulation and loss during one resonance episode. (c) Comparing the stored energy after multiple charging events for three scenarios of optimal, early, and late resonance-to-charging switching.

E_{LC} , as labeled in Fig. 3.2(b). However, for a fixed overall time (i.e., $t_{off-peak}$), there could be $m = (t_{off-peak} \times f)/N$ charging events, with N being the number of resonance cycles between two charging events. Therefore, the longer the receiver stays in resonance (larger N), the lower the number of charging events (smaller m) and their associated energy loss. It should be noted that R_{L1} discharges C_L at a very slow rate during the resonance mode and R_{L2} is only connected to the C_L when the CM receiver is in the resonance mode, hence, they have no/negligible effect on the V_L value during the charging periods [122], [108].

Therefore, there exists an N_{opt} where the overall energy made available to the capacitive load over m charging events is maximum. This N_{opt} not only depends on the effective energy accumulation rate during resonance, but also on the charging losses, which are a function of (i) the number of charging events m , and (ii) the storage capacitor's voltage (V_L) at the beginning of each charging event. As Fig. 3.2(c) shows, although late switching results in a higher level of received energy at Rx, a higher portion of this energy gets dissipated. On the other hand, while early switching results in a higher stored-over-lost ratio, the total received energy (stored+lost) is very low.

Once we choose N , the overall available energy ($E_{Available}$) for storage in the load capacitor over a fixed period (i.e., $t_{off-peak}$) is the product of E_{LC} at the end of each resonance episode and m , which is the number of charging events (refer to equation 2.19). As the Rx coil's physical geometry ($Q_{2eq}R_{2eq} = \omega L_2$) does not vary for a given link operating at its resonating frequency,

it was shown in Chapter 2 that $E_{Available}$ is maximum when the $V_{Rx(peak),N}^2/N$ term is maximum. As this optimization scheme requires continuous monitoring of $V_{Rx(peak),N}$ (i.e., the Rx coil's peak voltage in each resonance cycle), the effect of variations in link's physical parameters (e.g., coils movement/rotation) and electrical parameters (e.g., quality factors, media conductivity/permittivity, etc.) are implicitly taken into account [122]. Therefore, the optimization solution is adaptive to any variations in the link parameters during operation and is applicable to any inductive link. It should be noted that while the inductive link's efficiency (E_{Rx}/E_{Tx}) could vary due to many reasons, operating the CM receiver at an N_{opt} that maximizes (2.19) results in maximizing the total charging efficiency from the source to the load ($\eta_{tot} = E_{Load}/E_s$) for a given link efficiency [122].

3.2.2 Evaluation Requirements

All the advantages of the described link-adaptive optimization scheme are contingent on its efficient circuit implementation. Fig. 3.3 depicts the flowchart for optimal operating point detection in CM receivers. The circuit should (i) sample and hold the peak voltage at the receiver coil in each resonance cycle (i.e., $V_{Rx(peak),N}$), (ii) compute $V_{Rx(peak),N}^2/N$ expression (as in (2.19)), (iii) take its derivative with respect to N to detect the N_{opt} that maximizes the expression, and (iv) control the link operation timing accordingly to achieve the maximum overall link's energy storage efficiency. Hence, the circuit for N_{opt} detection must operate fast enough to perform the

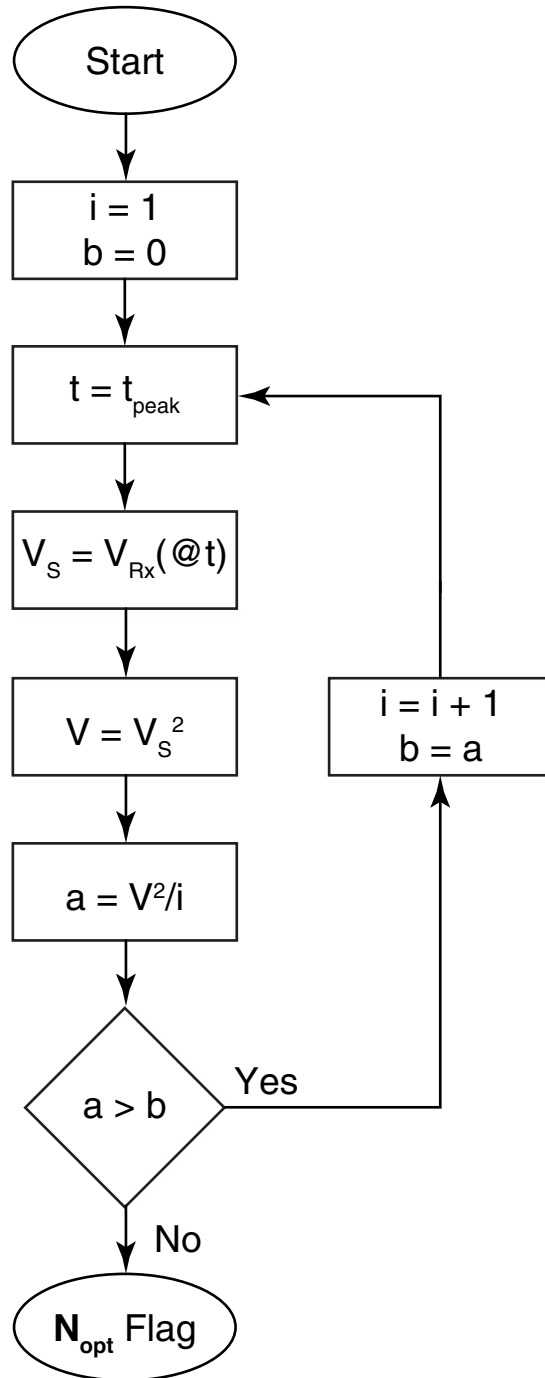


Figure 3.3: Flowchart for optimal operating point detection in CM receivers.

above four tasks in each resonance cycle while consuming minimal power (certainly less than what it saves by optimizing the operation). Since a digital solution would require a power-hungry high-speed analog-to-digital converter (ADC) (i.e., one high-resolution conversion per resonance cycle), all the circuits (including the V^2/N and its derivative computation) must be implemented in the analog domain.

3.3 On-chip analog implementation of the optimal operating point detection and adoption

In this section, the detailed design and implementation of different stages of our proposed analog solution are presented, followed by discussions on the design considerations and integration with the CM receiver.

3.3.1 A Hybrid Peak Voltage Sampler

The described N_{opt} calculator requires sampling of V_{Rx} at the peak time. Considering that the sinusoidal V_{Rx} takes both positive and negative values, using a simple N-, P-, or C-MOS switch for peak sampling could lead to unintended conduction or possible device breakdown. Fig. 3.4 compares a PMOS, an NMOS, and a diode-connected MOS for the $V_{Rx(peak)}$ sample and hold circuit.

As shown, the PMOS switch fails to turn ON for $V_{Rx(peak)}$ magnitudes smaller than V_{th} even when the gate is grounded. Additionally, it could face oxide breakdown when V_{Rx} takes large negative magnitudes. In contrast, the NMOS switch is capable of turning ON and properly sampling low $V_{Rx(peak)}$ values. However, it does not turn OFF during the negative half cycle when the absolute magnitude of V_{Rx} has sufficiently grown, leading to loss of the sampled voltage. Also, with the sampled voltage on C_s , using a negative V_G to prevent the switch from turning ON could lead to oxide breakdown at high V_{Rx} magnitudes. A diode-connected NMOS (or PMOS) solves the above issues, but fails at sampling voltages with amplitudes less than the transistor's V_{th} , which results in losing the initial cycles of V_{Rx} . Additionally, the voltage drop across the diode varies with the input voltage magnitude, leading to an inaccurate sample. Implementing the diode using a low- V_{th} transistor partially solves the problem but at the cost of high return-path leakage and post-peak conduction, both causing serious performance degradation.

Based on the above discussions, a hybrid approach is employed where an NMOS (with dynamic body biasing) is used to sample $V_{Rx(peak)}$ during the positive half cycle of V_{Rx} and the same transistor is diode-connected to hold the sampled voltage during the negative half cycle. Fig. 3.5(a) shows the detailed circuit diagram of the peak sampler stage along with the relative timing of the control signals ϕ_1 and ϕ_2 . During ϕ_1 (sample phase), M_1 and M_2 are turned ON and $V_{Rx(peak)}$ is sampled on C_s . As ϕ_2 is low in this phase, V_{GP} is tied to V_{dd} through M_{13} . The sampled peak voltage on C_s needs to be held for the remaining 3/4 cycle of V_{Rx} (hold phase) i.e.,

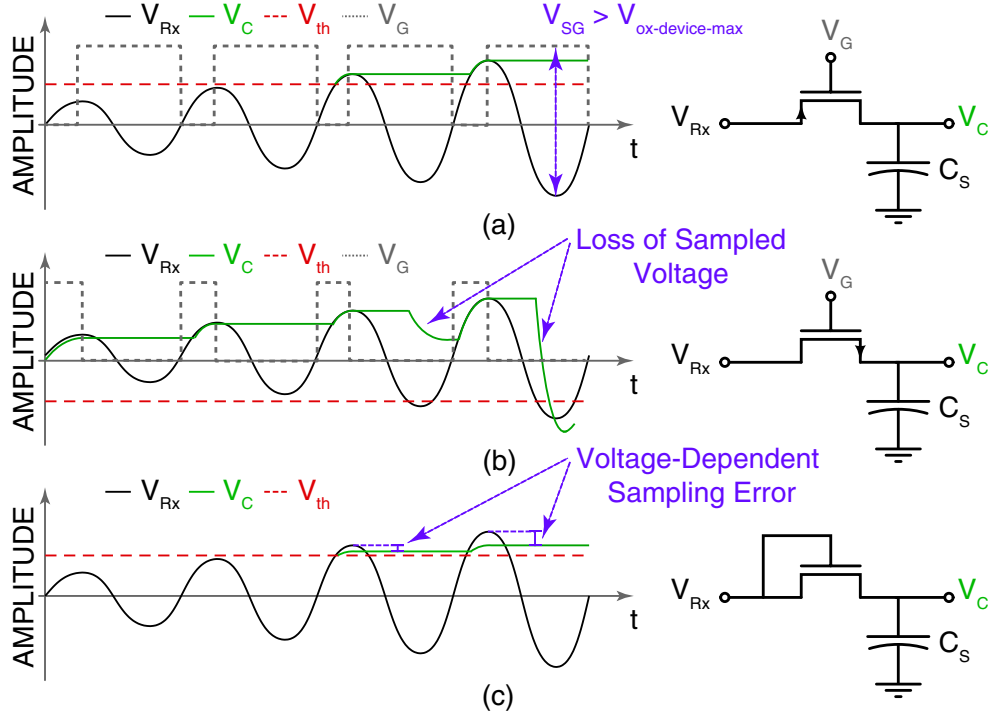


Figure 3.4: Comparison of: (a) PMOS, (b) NMOS, and (c) diode-connected MOS for peak voltage sampling.

after ϕ_1 returns to zero. To prevent C_s from discharging back into L_2C_2 tank when V_{Rx} is negative, and to avoid the need for a negative voltage for ϕ_1 to keep M_1 OFF, M_1 is diode-connected by shorting its drain and gate together through M_{11} . During ϕ_2 , which is ON in the final quarter of V_{Rx} ($t_{\phi_2} = T/4$), M_{13} turns OFF, M_{21} and M_{22} turn ON, hence, V_{GP} becomes equal to $V_{dd} - |V_{th}| - V_{Rx(peak)}$. At the start of the next V_{Rx} cycle and before the subsequent ϕ_1 , C_s is reset using M_{31} and M_{32} .

To prevent leakage current through the bulks, deep N-well transistors are used for M_1 , M_{11} ,

M_{12} , M_{14} , and M_{15} . The body of M_1 and M_{12} are connected to the lower voltage between V_{Rx} and ground using a dynamic body-bias generator circuit consisting of M_{14} and M_{15} . The body of M_{11} is tied to V_{Rx} which is always guaranteed to be less than or equal to V_G . This is because during ϕ_1 , V_G is pulled up to V_{dd} through M_{12} , and otherwise, V_G is connected to V_{Rx} .

3.3.2 V^2/N Calculation

Fig. 3.5(b) shows the schematic of the implemented analog V^2/N calculator circuit and how it is connected to the voltage peak sampler. As shown in the timing diagram (Fig. 3.5(c)), during ϕ_1 , $V_{Rx(peak)}$ is sampled on C_s and during ϕ_2 , $V_{GP} = V_{dd} - |V_{th}| - V_{Rx(peak)}$ is applied to the gate of a long channel PMOS device (M_{SQ}) biased in the saturation region. In each resonance cycle, M_{SQ} 's I_{DS} , which is proportional to $(|V_{GS}| - |V_{th}|)^2 = (V_{dd} - V_{dd} + |V_{th}| + V_{Rx(peak)} - |V_{th}|)^2 = V_{Rx(peak)}^2$ charges one of the capacitor banks on the left or right of the M_{SQ} for the duration of ϕ_2 , resulting in

$$V_{CHG(N)} = \frac{I_{DS(N)}}{(N \times C_{CHG})} t_{\phi_2}, \quad (3.1)$$

where $V_{CHG(N)}$ is the voltage across the capacitor bank at the end of ϕ_2 in the N^{th} resonance cycle. For each new cycle, all the capacitors in the bank are discharged and a unit capacitor is added in parallel to them (i.e., N is increased by one) through $\phi_{2(N)}$ switches. Given the quadratic relationship of I_{DS} and $V_{Rx(peak)}$, the linear increase in $V_{CHG(N)}$ during ϕ_2 is proportional to $V_{Rx(peak)}^2/N$

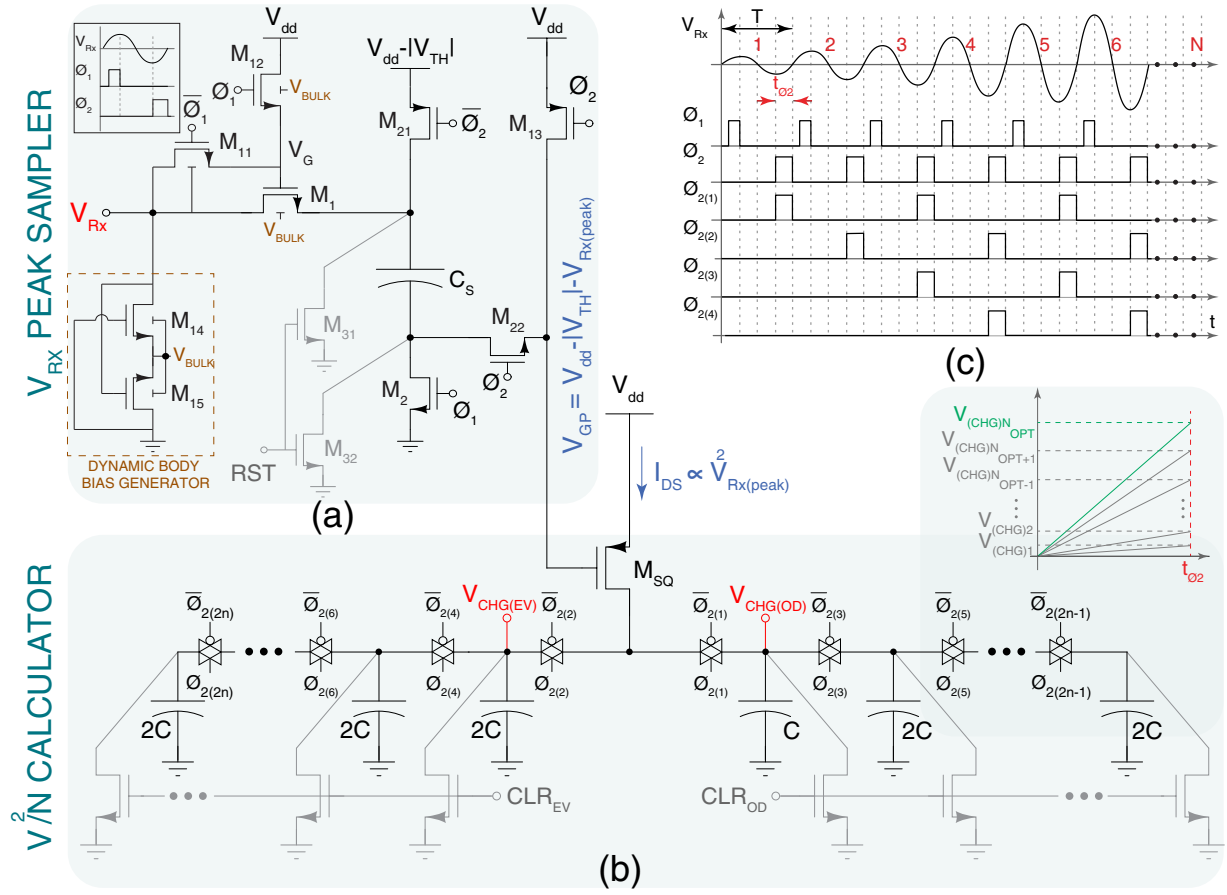


Figure 3.5: Analog implementation of the (a) peak sampler, and (b) V^2/N calculator circuits, with (c) the timing diagram of different operation phases.

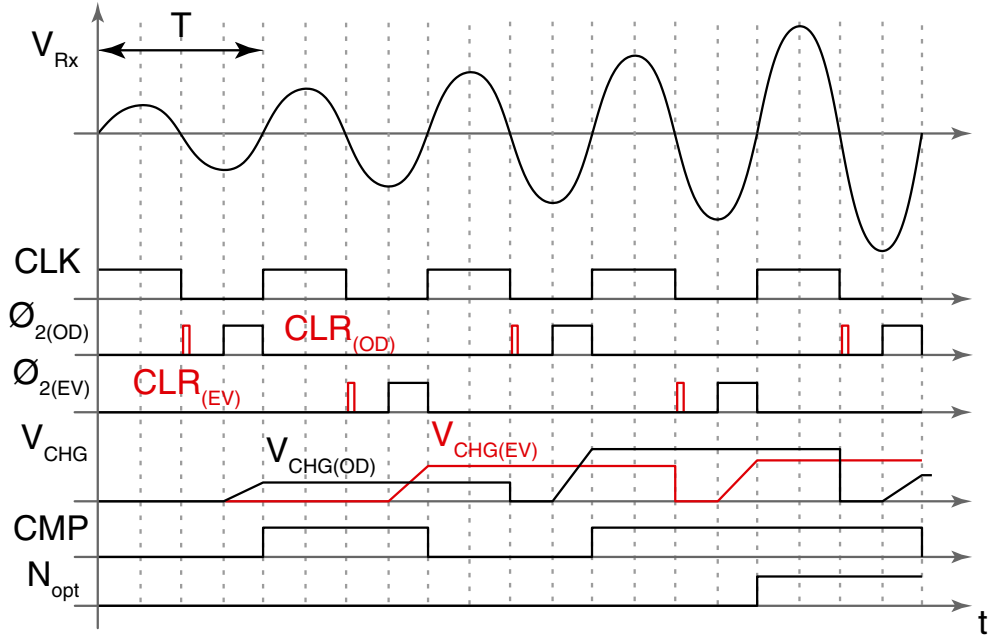


Figure 3.6: Relative sequence of different timing and control signals (used in Fig. 3.5 and 3.7 circuits) in a scenario where N_{opt} is detected.

with its highest value occurring at $N = N_{opt}$ cycle (as shown in the inset of Fig. 3.5(b)). To find the maximum value, consecutive V_{CHG} s should be compared with each other. Therefore, (a) two capacitor banks are used to store the V_{CHG} for two consecutive cycles, and (b) each bank's capacitance was increased by $2C$ so that division by odd and even N values are done using right and left banks, respectively.

Transmission gates used for $\phi_{2(N)}$ switches were sized to strike a trade-off between their ON resistance and parasitic capacitance. All capacitors on one side of the circuit are reset in an alternating manner using $CLR_{(EV/OD)}$ control signals, prior to getting charged by the new value

of the sampled voltage.

Fig. 3.6 summarizes the timing diagram of the system's operation sequence. In each positive half cycle of the clock (CLK), C_s is discharged using RST before $V_{Rx(peak)}$ is sampled during ϕ_1 . During the final quarter of the CLK cycle, ϕ_2 is high and capacitor banks are charged in an alternating manner. CLR signals are used to reset one of capacitor banks after each comparison. The figure also shows a scenario where the consecutive similar outputs of the comparator (indicating maximum $V_{Rx(peak)}^2/N$) is detected and N_{opt} flag is appropriately triggered.

3.3.3 Differentiation and N_{opt} Detection

Fig. 3.7 shows the block diagram of the circuit that detects the N_{opt} and controls the CM receiver's timing accordingly. A comparator is used to compare the two outputs of V^2/N calculator (i.e., $V_{CHG(OD)}$ and $V_{CHG(EV)}$) and a D-type flip-flop (DFF) is used to store the comparator's output for one cycle. The occurrence of two consecutive similar states of the comparator implies the peak of $V_{Rx(peak)}^2/N$, as it is an indication of $V_{CHG(j)}$ being greater than both $V_{CHG(j-1)}$ and $V_{CHG(j+1)}$. Hence, the depicted digital logic circuit flags this cycle as the N_{opt} cycle and generates a control signal to open S_1 and close S_2 in order to terminate the Rx's resonance mode and initiate the charging operation.

As shown in Fig. 3.7, the comparator is implemented using a strongArm architecture with a power-cycled pre-amplifier. It burns ~ 3 pJ per comparison at 1 MHz (power = 3 μ W) with an

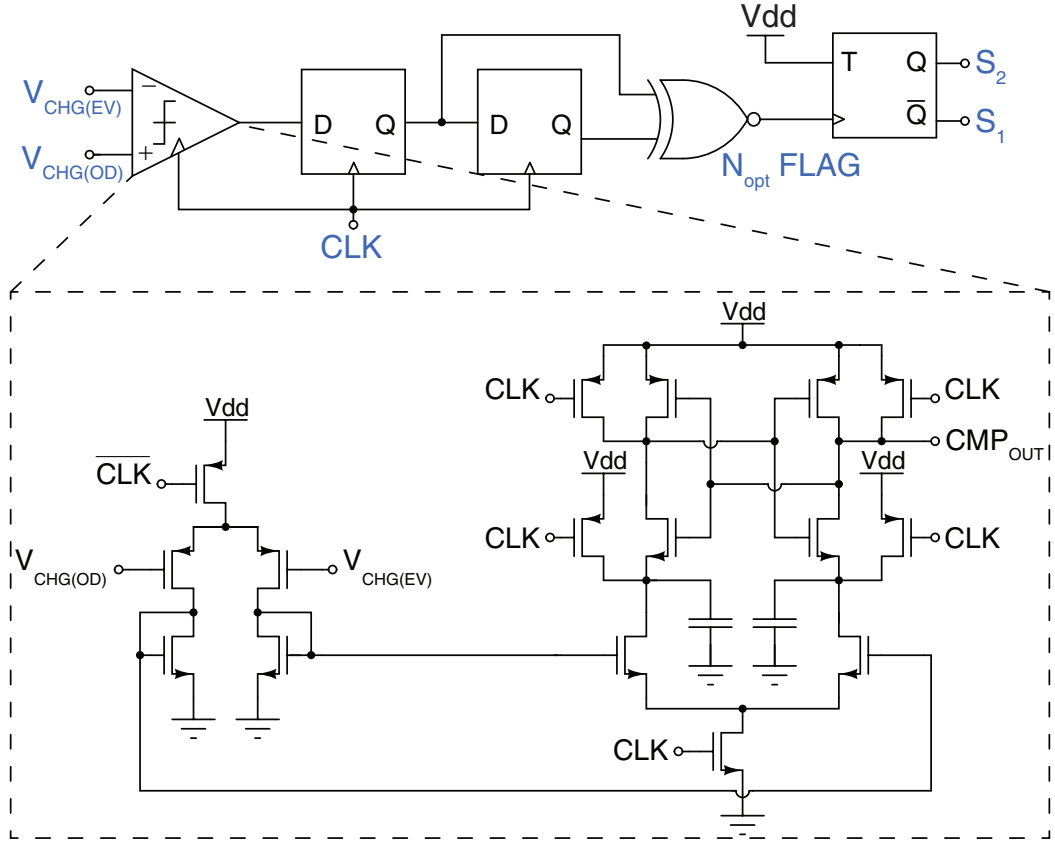


Figure 3.7: Block diagram of the N_{opt} detector stage along with circuit diagram of the comparator.

input-referred noise of $187.09 \mu V / \sqrt{Hz}$, $1 \mu V$ hysteresis, and offset voltage of $724 \mu V$. The comparator's low hysteresis is essential as its output should alter state in each CLK cycle before N_{opt} occurrence. Furthermore, we have ensured that the comparator's offset is less than the difference between $V_{CHG(j)}$ and $V_{CHG(j\pm 1)}$ nodes in the V^2/N stage.

3.3.4 Design Considerations and Trade-offs

Various design trade-offs in sizing and biasing of the M_{SQ} , the circuit's power consumption, the capacitor bank, and the sampling capacitor were considered. Fig 3.8(a) and (b) show the M_{SQ} 's drain current i_d , for different channel lengths, versus $V_{Rx(peak)}$ where the source of M_{21} is set to $V_{dd} - V_{th}$ (compensated V_{th} at the gate) and V_{dd} (no V_{th} compensation at the gate), respectively. As expected, increasing the channel length and compensating for M_{SQ} 's V_{th} result in a more accurate quadratic behavior. However, not compensating for the V_{th} (i.e., no V_{th} subtraction in the source of M_{21}) has the advantage of significantly smaller power consumption and leakage at the cost of yielding a less accurate quadratic behavior, particularly during the first few cycles. Fortunately, for the first few cycles, N (i.e., the denominator of $V_{Rx(peak)}^2/N$) is changing significantly (e.g., by 100% from 1 to 2, or by 50% from 2 to 3), hence, inaccuracies of V^2 in the numerator will have a negligible impact on the fraction and cannot change the results. Therefore, we decided to set the source of M_{21} to V_{dd} in our experiments to further reduce the circuit's power consumption without a loss of accuracy.

Since the M_{SQ} 's current is proportional to $V_{Rx(peak)}^2$, as the receiver stays longer in resonance, the V^2/N calculator circuit's power consumption increases. Therefore, we calculated the required energy for N_{opt} detection by integrating the consumed energy at individual cycles up to the N_{opt} cycle. From the power consumption perspective, a small W/L is preferred for M_{SQ} , which is in agreement with having a long L desired for accurate quadratic relationship. However,

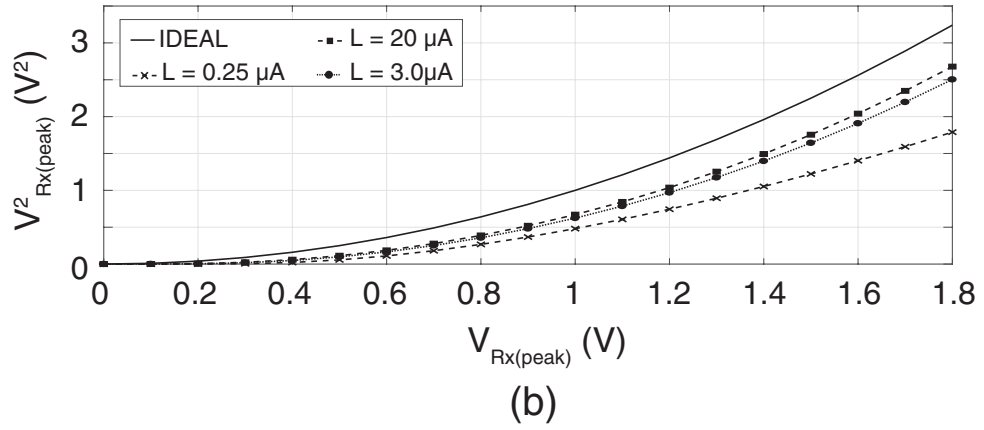
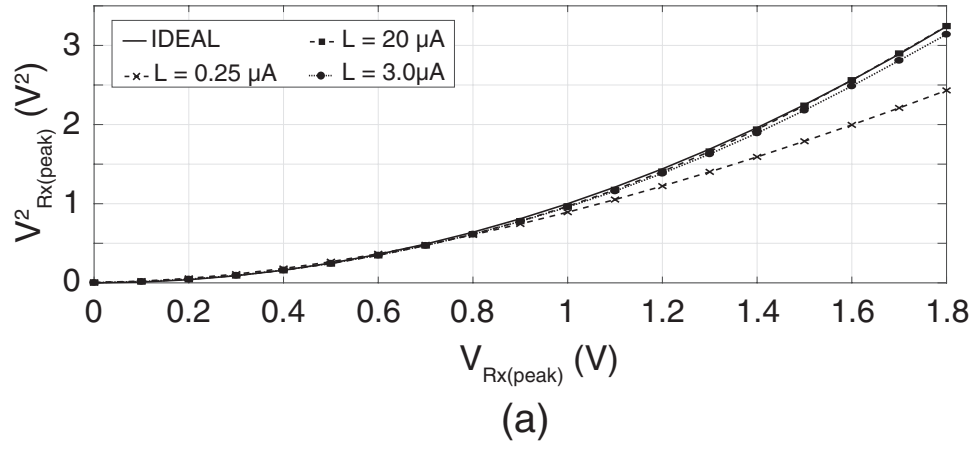


Figure 3.8: Current-voltage relationship of a PMOS in saturation region with (a) V_{th} compensation and (b) no V_{th} compensation at the gate.

making W/L too small results in a small I_{DS} , consequently a small difference between $V_{CHG(OD)}$ and $V_{CHG(EV)}$. This puts pressure on the required accuracy for the comparator, hence, translates into a higher power consumption. On the other hand, while we are motivated to reduce the unit capacitor size in the bank to increase the charging slope and relax the comparator's required accuracy, too small capacitance could result in a high voltage (especially for high $V_{Rx(peak)}$ values) that could push M_{SQ} closer to the triode region.

In sizing M_{SQ} , the parasitic capacitance at the gate was also considered as it could deviate V_{GP} from its intended $V_{dd} - V_{Rx(peak)}$ value,

$$V_{GP} = \frac{C_s(V_{dd} - V_{Rx(peak)}) + C_g V_{dd}}{C_s + C_g}. \quad (3.2)$$

Although (3.2) infers a larger C_s is of interest to prevent voltage deviation, it should be considered that increasing C_s will increase the RC delay in the voltage sampler stage, which results in a wrong sampling moment compared to the peak value. In addition, C_s should be chosen to be significantly smaller ($\sim < 0.5\%$) than C_2 (the Rx's resonating capacitor) to prevent deviations in the resonance frequency of the receiver.

3.3.5 Clock Recovery, System Integration, Verification, and PVT Simulations

Fig. 3.9 shows the high-level block diagram of the presented IC and the way it is interfaced with a CM inductive receiver. An on-chip timing controller is designed that uses the recovered CLK and its 90° -phase-shifted version and generates various control signals for the voltage peak sampler, V^2/N calculator, and N_{opt} detector stages. An inverter-capacitor chain delay circuit with a tunable supply voltage (for adjustable delay) is used to create the 90° -phase-shifted version of the CLK. As shown, the output of the N_{opt} detector is used to control the resonance-to-charging transitions in the CM receiver. The clock is recovered from the incident waveform at the Rx coil using a zero-crossing detector (ZCD) that consists of a two-stage open-loop operational amplifier where V_{Rx} and GND are applied to its PMOS input pair to perform the comparison at low V_{Rx} amplitudes (Fig. 3.10). It is worth mentioning that for the current ZCD circuit with 1.8 V rating transistors, a maximum V_{Rx} amplitude of 1.6 V is tolerable at its input pair. This amplitude is considered reasonable for CM receivers with loosely-coupled links [53]. For future versions, thick-oxide transistors (3.3 V rating) could be used to replace the PMOS input pair to tolerate larger input amplitudes.

Fig. 3.11(a) depicts the simulated open-loop gain magnitude and phase of the amplifier at different bias currents. As expected, extending the bandwidth requires consuming more power.

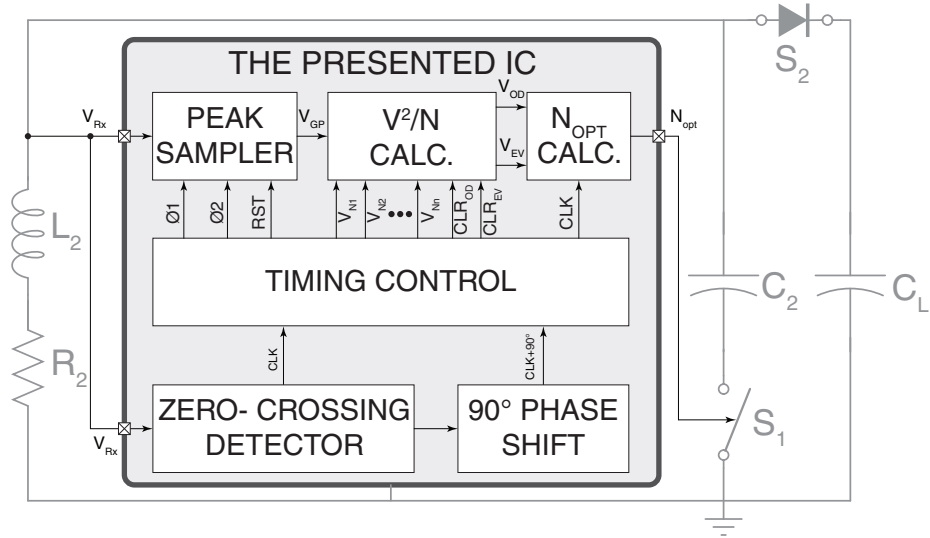


Figure 3.9: Block diagram of the presented overall link's energy storage efficiency maximizer IC and how it is interfaced with a CM receiver.

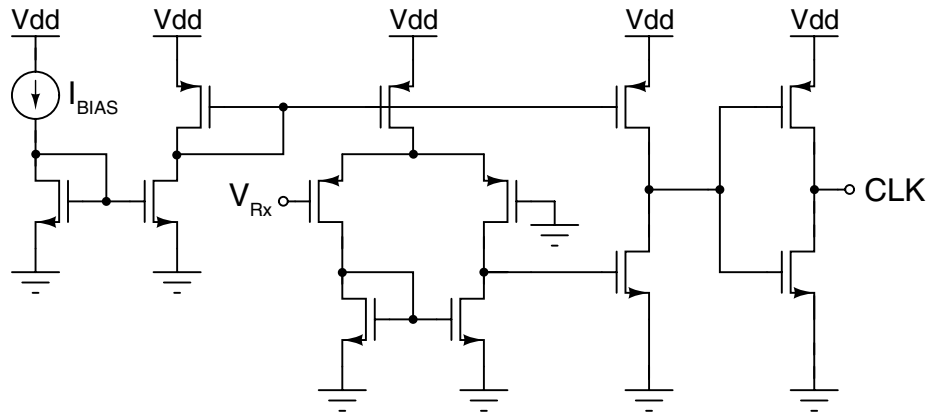


Figure 3.10: Circuit diagram of the zero-crossing detector (ZCD).

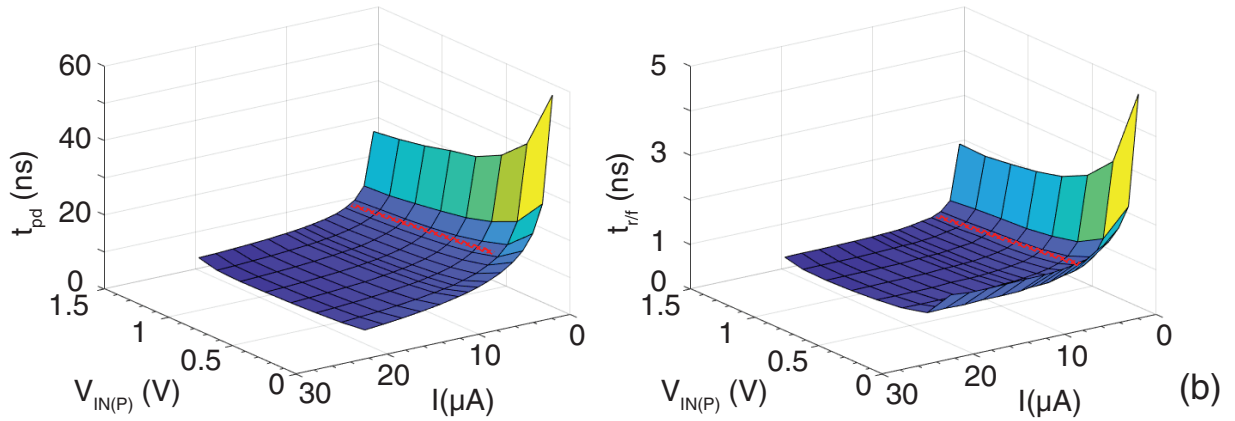
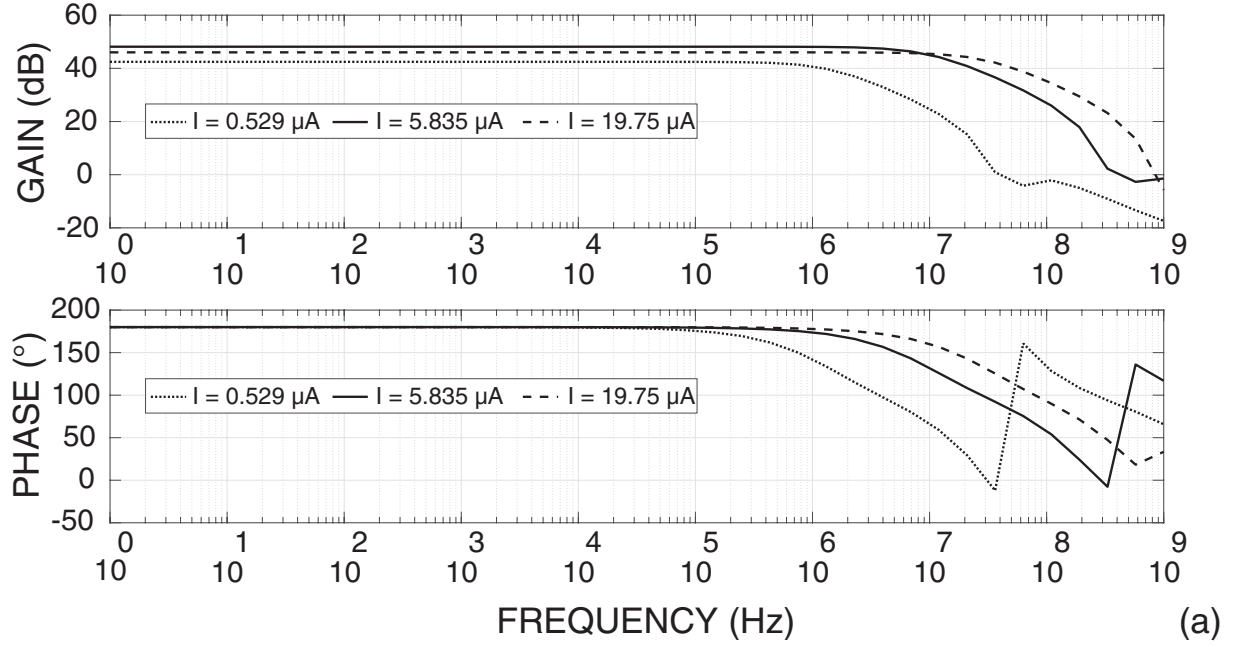


Figure 3.11: Post-layout simulation results of the ZCD's (a) gain magnitude and phase for different bias currents, (b) propagation delay and rise/fall time vs. power consumption and V_{IN} , highlighted with the chosen knee area.

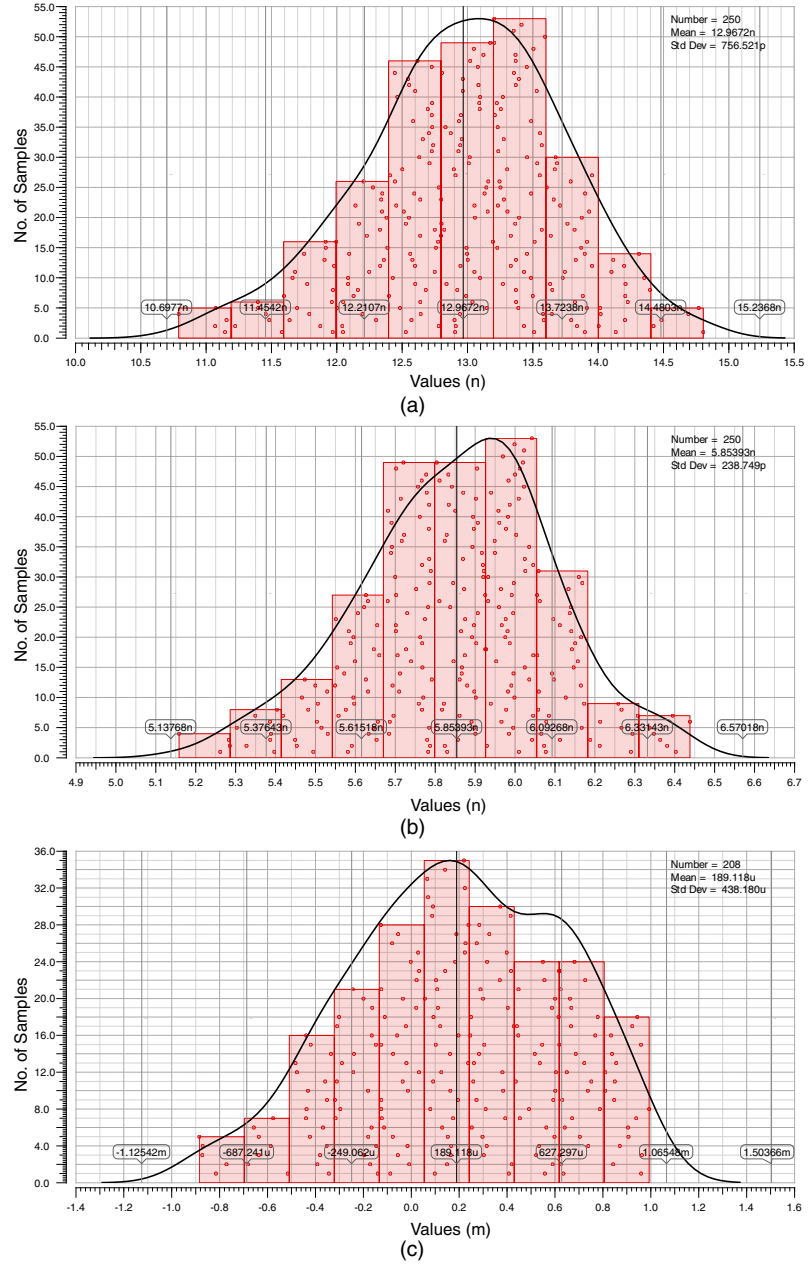


Figure 3.12: Monte Carlo simulation results for ZCD's (a) propagation delay for 100 mV_P and (b) 1.5 V_P sinusoidal inputs, (c) offset voltage.

This is further illustrated by showing the simulated propagation delay (t_{pd}) along with rise/fall time ($t_{r/f}$) of the circuit in Fig 3.11(b), where sinusoidal waveforms with different amplitudes ranging between 0.1-1.5 V at 1 MHz were applied to the circuit. From this figure, it is concluded that the power consumption of the ZCD could be reduced as far as the t_{pd} in zero-crossing time is within an acceptable range ($\sim 1\%$ error). We have chosen the knee point of this plot where delay is significantly reduced and further increase in the power is not beneficial anymore. From post-layout simulations, a total current of $5.84 \mu\text{A}$ in ZCD results in 13 ns and 6 ns delay for 100 mV_P and 1.5 V_P input signals, respectively. These correspond to 1.3% and 0.6% of a cycle at 1 MHz. The Monte Carlo simulation results for these conditions are shown in Fig. 3.12(a) and (b), respectively. As seen from the plots, the variations are scattered around the reported typical values. Furthermore, the worst case delays are too insignificant to cause any inaccuracy in N_{opt} detection. Using post-layout simulations, later confirmed by measurement results, we confirmed that the ZCD's input offset is sufficiently small ($327 \mu\text{V}$) not to affect the energy stored in C_L due to resonance-to-charging timing inaccuracies. Fig. 3.12(c) shows the Monte Carlo simulation results for the ZCD's offset voltage. As the graph shows, the average offset is around $190 \mu\text{V}$ and the maximum offset voltage of ZCD is 1 mV for the worst case scenario at this low voltage amplitude. It is worth mentioning that this low input amplitude possibly occurs at the very first few cycles when the resonance mode is getting initiated during which highly precise timing for resonance-to-charging switching and V^2/N calculation is not required, as V_{opt} occurs when

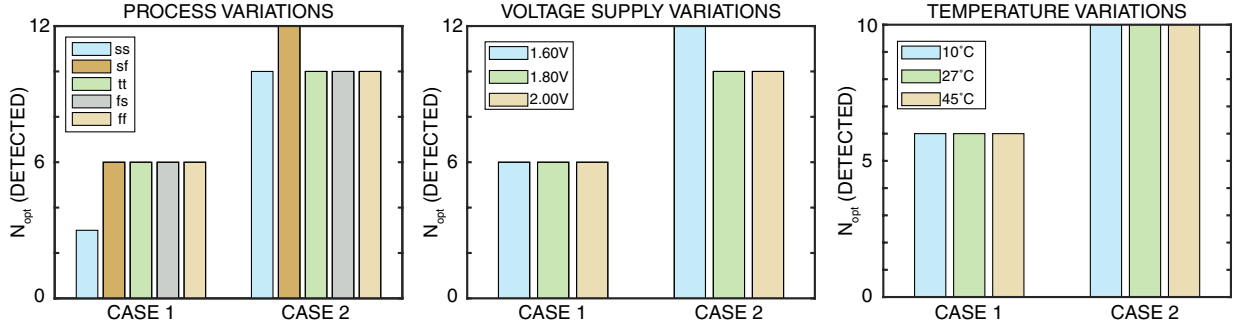


Figure 3.13: Post-layout simulation results vs. PVT variations for the implemented system.

reasonable energy level is accumulated at the receiver. On the other hand, the N_{opt} detection is not sensitive to small deviations (e.g., $<1\%$ of the resonance cycle period) as V^2/N and calculation of its maximum value are performed relative to the values from the current, previous, and the next cycle. Of course, the circuit performance significantly improves at larger input voltages when the timing and V^2/N calculation are critical.

The functionality and accuracy of the implemented system is verified using transient simulations. Fig. 3.13 shows how the flagged N_{opt} by the chip is affected versus process, voltage supply, and temperature (PVT) variations for two different cases. As illustrated, the system shows an acceptable performance in N_{opt} detection against such variations.

3.4 Measurement Results

The presented IC is designed and fabricated using a standard $0.18\mu\text{m}$ CMOS process. The chip's micrograph is shown in Fig. 3.14(a). The active circuits (excluding the pads) occupy $750 \times 600 \mu\text{m}^2$. Fig. 3.14(b) shows the measurement setup which consists of an inductive link with a CM receiver and the developed IC for automatically maximizing the energy storage. The experimental validation of the presented work was done using three test scenarios.

In the first scenario and prior to testing the chip using a real inductive link, an arbitrary waveform generator was used to provide V_{Rx} waveforms that mimicked the incident signal for different inductive links. This approach is an alternative to experimentally implementing several links with different parameters (e.g., coils size, quality factors, coupling coefficient, etc.) to verify the chip's performance in detecting different N_{opt} . For each input excitation (V_{in}), the N_{opt} detected by the IC was compared to its known value that was calculated using the theoretical model described in Chapter 2 (the model's accuracy is experimentally proven in Section 2.4). The results are shown in Fig. 3.15. For each case, the oscilloscope snapshot shows ϕ_1 (the peak-sampling moment), the comparator's output (CMP_{out}), and the N_{opt} flag signal. As expected, the comparator's output changes in every cycle except for the N_{opt}^{th} cycle, confirming the chip's accuracy and capability in computing $V_{Rx(peak)}^2/N$. Fig 3.15 shows how the IC successfully detects the maximum $V_{Rx(peak)}^2/N$ cycle which represents the N_{opt} for different input waveforms

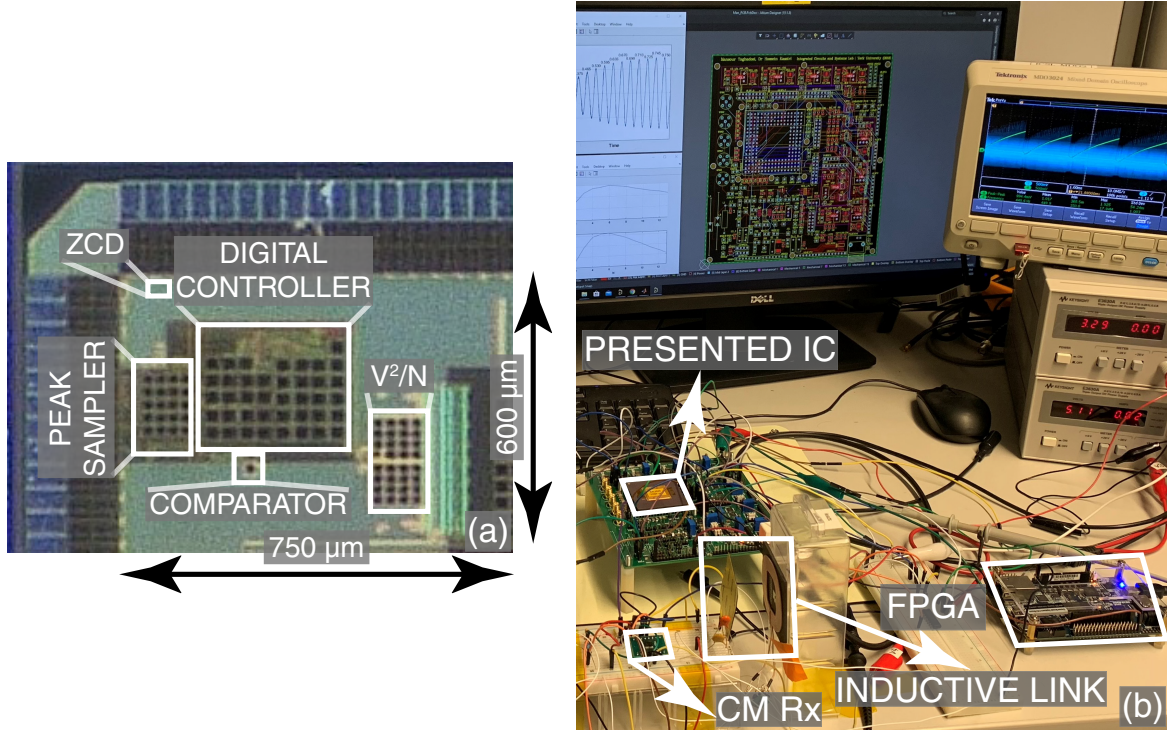


Figure 3.14: (a) Annotated chip micrograph of the presented IC. (b) Measurement setup for experimental validation.

with N_{opt} ranging from 3 to 10. It should be noted that the oscilloscope snapshots show higher number of V_{Rx} cycles beyond the detected N_{opt} to illustrate that the IC does not have a false flagging for any other cycle and the calculation of $V_{Rx(peak)}^2/N$ function along with detection of its maximum point is perfectly executed for multiple times under the same excitation.

For the second measurement scenario, we implemented two inductive links with different physical and electrical parameters and tried to experimentally find their N_{opt} by operating the links while sweeping N values and observing the N that results in the maximum stored energy

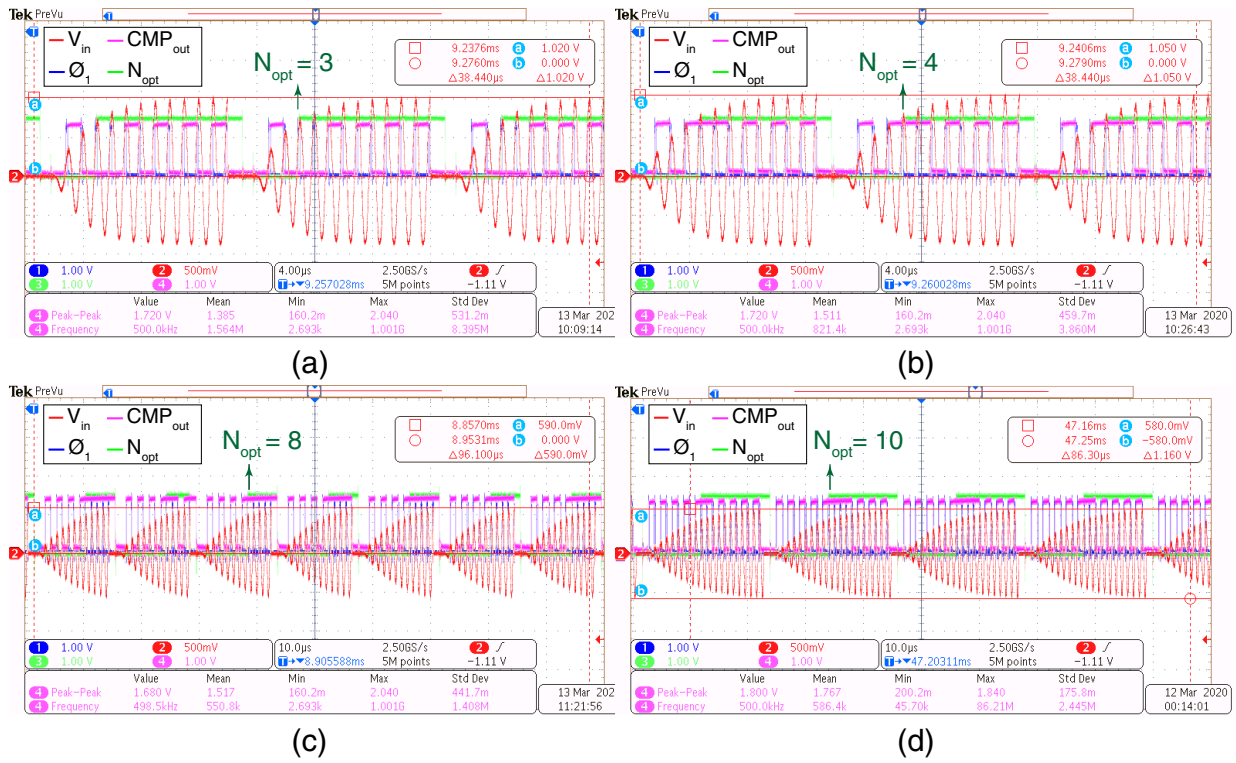


Figure 3.15: Measurement results showing accurate N_{opt} detection by the IC for four different V_{Rx} waveforms with N_{opt} ranging from 3 to 10.

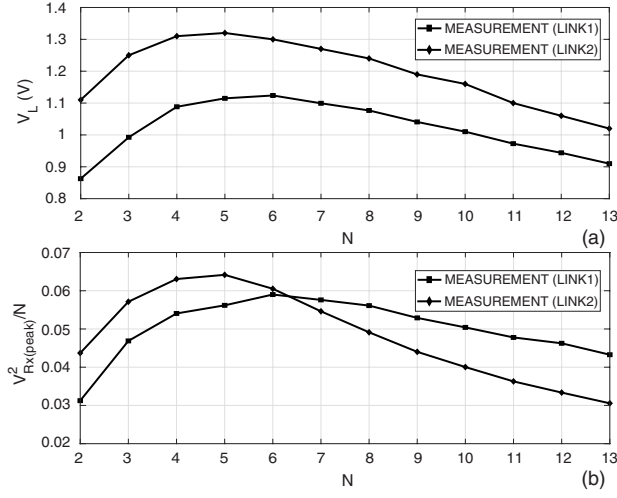


Figure 3.16: Measured (a) V_L and (b) $V_{Rx(peak)}^2/N$, both vs. N resonance cycles, for the two implemented links ($t_{off-peak} = 2\text{ ms}$ for link1 and $t_{off-peak} = 1.5\text{ ms}$ for link2).

over $t_{off-peak}$ (i.e., collecting empirical evidence). This observation was later used as the ground truth in the third testing scenario to compare it to the N_{opt} detected by the IC. It should be noted that the inductive link's physical or electrical parameters optimization is not the focus of this work and the presented IC is responsible for operating CM receivers to achieve their maximum possible overall link's energy storage efficiency, independent of the links' parameters. Therefore, commercially available Würth Elektronik coils (WE-WPCC series) which have reasonable quality factors (~ 100 for Tx and ~ 30 for Rx, both measured at 1 MHz) were used to realize a weakly-coupled link as a proof-of-concept implementation. While 1 MHz was used as an implementation example similar to [53] and [108], the proposed optimization scheme is applicable to other frequencies as well [122]. It is worth mentioning that in the practical implementation,

a fast switching diode was preferred over a MOS switch for S_2 similar to [108] and [114], as the MOS switch requires a very precise and high-speed comparator to detect the end-of-charging moments and avoid energy discharge from C_L back to the Rx's L_2C_2 tank. To empirically find the N_{opt} , an FPGA was used to switch the CM receiver connected to each link from resonance to charging mode after N cycles ($N = 2 - 13$) and re-initiate the resonance mode after allowing t_{ch} as the charging time. For each N , this resulted in $m = (t_{off-peak} \times f)/N$ charging events for an overall operation time of $t_{off-peak}$. As shown in Fig. 3.16(a), it was experimentally observed that at the end of $t_{off-peak}$, the storage capacitor's voltage (V_L) was the highest for $N = 6$ and $N = 5$, for link1 and link2, respectively, which are well predicted by the $V_{Rx(peak)}^2/N$ model (Fig. 3.16(b)).

For the third measurement scenario, the IC was connected to the two inductive links as shown in Fig. 3.9 to automatically detect the optimal operation of the CM receivers. Fig. 3.17 shows the N_{opt} values detected by the chip when it is connected to the two links, which are perfectly matched with the empirical data shown in Fig. 3.16. It should be noted that similar to Fig. 3.15, the oscilloscope snapshots in Fig. 3.17 show the detected N_{opt} for both links while the resonance mode was allowed for 13 cycles to demonstrate the chip's detection accuracy. As the measurement results show, N_{opt} is successfully flagged by the chip for both links while there is only one cycle difference in the optimal values (i.e., $N_{opt(link1)} = 6$, and $N_{opt(link2)} = 5$), attesting to the precision of the presented IC in V^2/N computation and differentiation, and its ability to adapt to

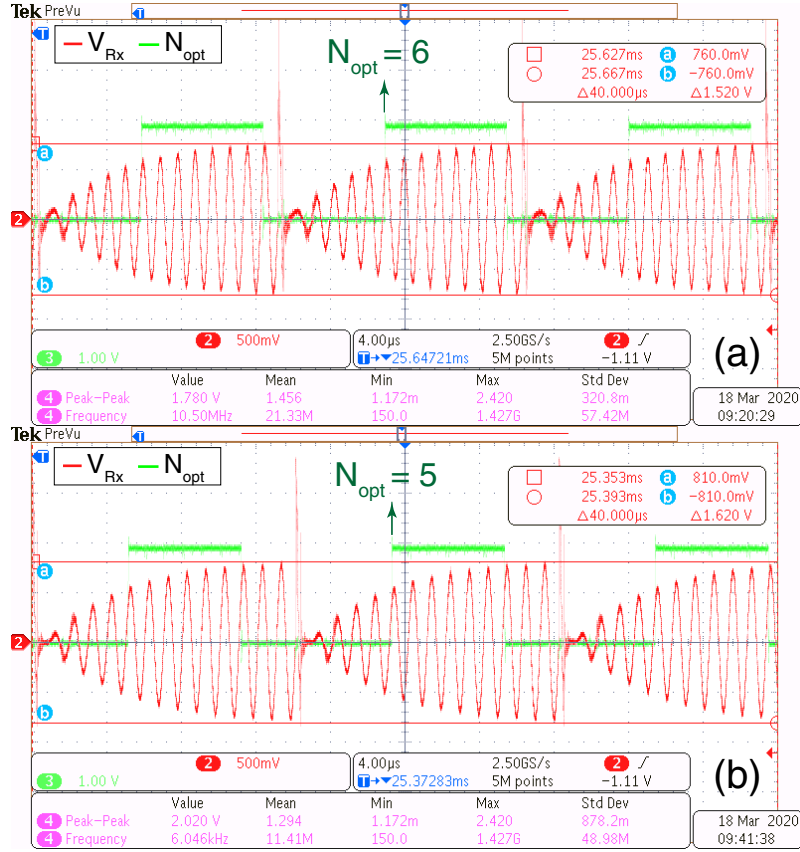


Figure 3.17: Measurement results showing precise N_{opt} detection by the presented IC when connected to (a) link1 and (b) link2, exactly matching the empirical measured data from Fig. 3.16.

any variation in the link parameters while eliminating the need for pre-calibration.

A measured example of energy storage gain achieved by employing the presented IC is presented in Fig. 3.18(a). The figure shows the measured E_{Load} versus N , which is normalized to the highest measured value at N_{opt} . In these measurements, E_{Load} is obtained by recording the final voltage across C_L at the end of $t_{off-peak}$ for each N for the two implemented links. From this

figure, the sensitivity of accurate detection around the N_{opt} cycle is also shown. As the reflected impedance of a CM receiver on the Tx is almost constant in a loosely-coupled link, maximizing E_{Load} results in maximizing the overall link's energy storage efficiency from the source in the Tx to the load in the Rx as well ($\eta_{tot} = E_{Load}/E_s$). Fig. 3.18(b) shows the percentage change in E_{Load} compared to the two extreme cases. The figure shows that switching at N_{opt} results in 70% and 53% improvements in E_{Load} for $t_{off-peak} = 2\text{ ms}$ in link1, and 41% and 67% improvements in E_{Load} for $t_{off-peak} = 1.5\text{ ms}$ in link2, both compared to early switching at $N = 2$ and late switching at $N = 13$, respectively.

Table 3.1 shows the IC's total energy consumption and breakdown when used to operate the two described example links. The energy consumption varies depending on the V_{Rx} dynamics and the N_{opt} value. However, even when the detection system is continuously working, its energy consumption is always a small portion of the energy storage gain achieved by using the IC (i.e., the total consumed energies for N_{opt} detection is 1.73% and 0.90% of the additional stored energy in C_L if operated by the IC at N_{opt} for links 1 and 2, respectively). Furthermore, since it is not expected for the changes in the link parameters or environment to happen every millisecond (or even every second), the IC does not need to be always ON and the process of N_{opt} calculation can be performed as frequent as required (e.g., every second, minute, or an hour) and the N_{opt} value could be stored until the next calculation. Therefore, the IC's energy consumption will be practically negligible (i.e., orders of magnitude smaller than 1%) in the long run. Table 3.2

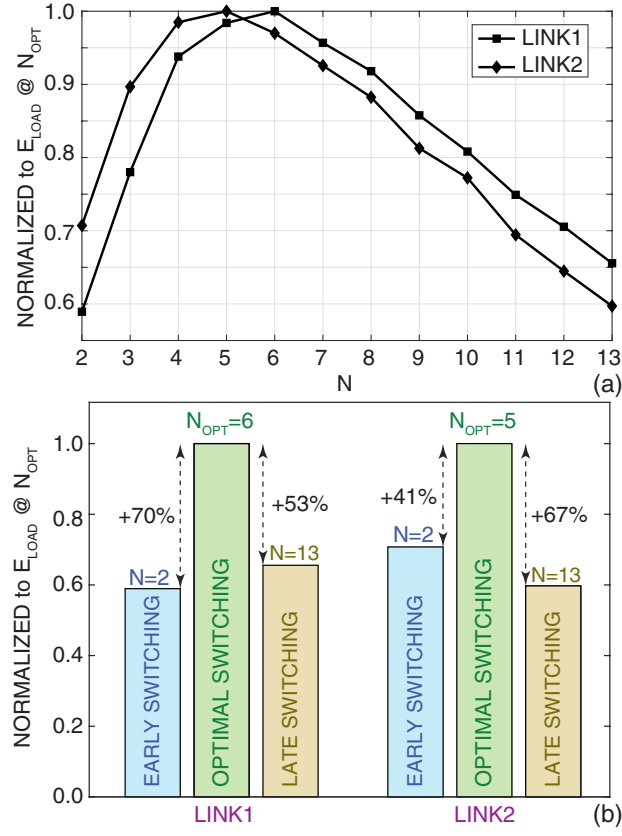


Figure 3.18: Measured data showing: (a) normalized E_{Load} to E_{Load} @ N_{opt} vs. N , (b) improvements in E_{Load} at N_{opt} compared to early switching at $N = 2$ and late switching at $N = 13$ ($t_{off-peak} = 2\text{ ms}$ and 1.5 ms for links 1 and 2).

compares the presented energy optimization scheme with other works in the literature.

Table 3.1: Breakdown of simulated energy consumption by the IC for N_{opt} detection of the two implemented links.

	ZCD	90° Phase Shifter	Peak Sampler & V^2/N	Digital Controller	Comparison	Total
Link1	63 pJ (16.75%)	256.08 pJ (68.10%)	15.11 pJ (4.02%)	23.82 pJ (6.33%)	18.00 pJ (4.80%)	376.00 pJ 188 nW
Link2	52.50 pJ (16.66%)	213.40 pJ (67.71%)	14.41 pJ (4.57%)	19.85 pJ (6.30%)	15.00 pJ (4.76%)	315.16 pJ 210.11 nW

Table 3.2: Comparison of CM energy optimization with the state of the art.

	[123]	[114]	[109]	[110]	This Work
Rx Architecture	VM	CM	CM	CM	CM
Load Type	Capacitive	Resistive	Capacitive	Capacitive	Capacitive
Optimization Target	Energy storage	Power delivery	Energy storage	Energy storage	Energy storage
Optimization:					
Automatic	Yes	No	Yes	No	Yes
Link-Adaptive	Yes	No	No	No	Yes
Implementation	Analog	Off-chip	Digital	Analog	Analog
Requires Calibration	No	Yes	Yes	Yes	No
Technology (μm)	0.35	N/A	0.18	0.18	0.18
Active Area (mm^2)	2.10	N/A	0.544	0.211	0.450
Frequency (MHz)	2.00	6.78	0.05	13.56	1.00
V_{DD} (V)	± 2.1	N/A	1.2 & 3	1.8	1.8
$\eta_{Rx(max)}$ (%) @ P_{IN}	82 @ 11.6 mW	N/A	67.70 @ 4.2 μW	92.60 @ 10.89 mW	70.62 @ 46 μW
Rx Coil Size	$d_o = 10 \text{ mm}$	$d_o = 10 \text{ mm}$	2.6 x 3.5 x 11.7 mm^3	6 x 6 mm^2	$d_o = 28 \text{ mm}$
Tx-Rx Coil Distance (cm)	1.5	1.3	8.5	1.5	1.0

3.5 Conclusion

In this chapter, we presented the design, development, and characterization of an integrated circuit that maximizes the overall link's energy storage efficiency in resonant inductive CM power receivers. A brief analytical formulation of energy reception and storage in CM receivers was presented prior to a detailed system-level design and circuit-level implementation of the IC. A detailed discussion on various design choices and trade-offs for device sizing and biasing was also included. The IC's capability in real-time evaluation and on-the-fly adoption of optimal operation scheme allows for guaranteeing maximum overall link's energy storage efficiency for CM receivers, regardless of their link efficiency. The IC was fabricated in a standard $0.18\ \mu\text{m}$ CMOS process. Its adaptability to changes in various link's parameters was experimentally validated, where it could precisely detect the optimal operating point for several cases with a wide range of input waveform dynamics. The IC was connected to two different inductive links and it was experimentally shown that it can accurately detect their optimal operation point and control their mode of operation accordingly. The energy efficiency of the presented solution was also investigated and it was shown that through receiver operation optimization, the IC saves two orders of magnitude more energy than what it consumes.

Chapter 4

Simultaneous Power Delivery and Optimal Overall Link's Energy Storage Efficiency in VM Inductive Power Receivers

4.1 Introduction

As mentioned in Chapter 1, VM receivers are widely used for applications where the induced power at the receiver is high and a high PCE is required. Due to uninterrupted loading of this architecture, the amount of induced power at the receiver (due to Rx's reflected load on Tx) is heavily dependent on its equivalent load (i.e., induced voltage and drawn current at the load) at a certain coupling condition. Conversely, charging a capacitor, for the sake of surplus energy storage requires a real-time-adaptive impedance matching at the receiver (since, unlike resistive

loads, the effective load of a capacitor continuously changes as it gets charged) or L_2C_2 manipulation to achieve an efficient charging process. Furthermore, a real time power measurement is essential to identify the peak power conditions.

In this chapter, it is proposed to provide a solution that isolates the charging capacitor's loading on the Rx, while concurrently maintaining the optimal loading on Tx for maximum power reception. This is achieved regardless of the amount of stored energy and the specific loading conditions of the Rx. By retaining maximum received power, this method facilitates optimal energy storage by directing excess energy through the storage pathway, particularly effective when received power surpasses continuous load consumption. This enables efficient energy storage, preventing wastage of energy in the receiver's parasitic components. However, attaining the required information for the optimal operation point necessitates initiating a calibration phase to achieve standalone functionality. A notable advantage is that this calibration phase involves voltage comparison rather than power measurement.

This chapter reviews the operational principles of inductive links with VM receivers and presents an strategy aimed at enhancing the storage of excess energy. Moreover, it provides a detail discussion at both system and circuit levels of a fabricated chip that enables the implementation of the proposed energy storage optimization scheme. The measurement results demonstrate notable enhancements, with charging time and stored power experiencing 19.61% and 24.39% improvements, respectively. When considering different reference points for com-

parison, these improvements can reach as high as 48.44% for the charging time and 93.97% for the stored power. Remarkably, this approach eliminates the need for manipulating the receiver's LC tank and the need for an additional wireless data communication.

The rest of this chapter is organized as follows. Section 4.2 provides a revision on modeling of resonant inductive links with VM architecture with emphasize on its optimal loading conditions to achieve a high PTE or PDL. Moreover, the undertaken strategy for loading isolation during the overall charging time of a storage capacitor to achieve a high overall link's energy storage efficiency (beneficial for supplying R_{L2} -type loads) while simultaneously delivering the low-continuous power to R_{L1} -type loads is further discussed. Furthermore, the efficacy of the proposed scheme is validated using CAD-based simulation results. Section 4.3 presents the system- and circuit-level implementation of the IC that is designed to achieve these requirements. Section 4.4 presents the experimental validation of the presented energy optimization scheme using the fabricated chip and off-the-shelf components. Finally, Section 4.5 concludes the chapter.

4.2 VM Theory and Operation

4.2.1 Conventional Architecture and Optimal Loading Conditions

It is commonly known that the inductive link's overall power transfer efficiency (PTE), defined as the ratio of the power delivered to the load (PDL) at the Rx over the generated source power at the Tx, could be further enhanced by driving both the Tx and Rx in resonance by adding series or parallel compensating capacitors [94]. This results in four different possible resonators namely series-series, series-parallel, parallel-series, and parallel-parallel architectures for the Tx-Rx link [124, 125]. While resonant series-secondary performs better for high-power (heavy loads) with a higher current demand, the resonant parallel-secondary is useful for low-power (light loads) with a higher voltage demand, which is the case for biomedical implants [126–129].

Fig. 4.1(a) shows the circuit diagram of a conventional resonant inductive link with a parallel-secondary VM power receiver architecture. The primary (i.e., transmitter) side is typically driven with a highly-efficient class-E power amplifier (PA), represented by V_s [130–132]. A rectifier and voltage regulator circuits are used for AC-DC conversion and load's voltage regulation, respectively. The ripple rejection capacitor at the output of the rectifier (C_{REC}) prevents a sudden drop in the voltage at the input of the voltage regulator in case of a momentary increase in the load current.

The VM receiver operates in two different regions, namely the transient and the steady-state.

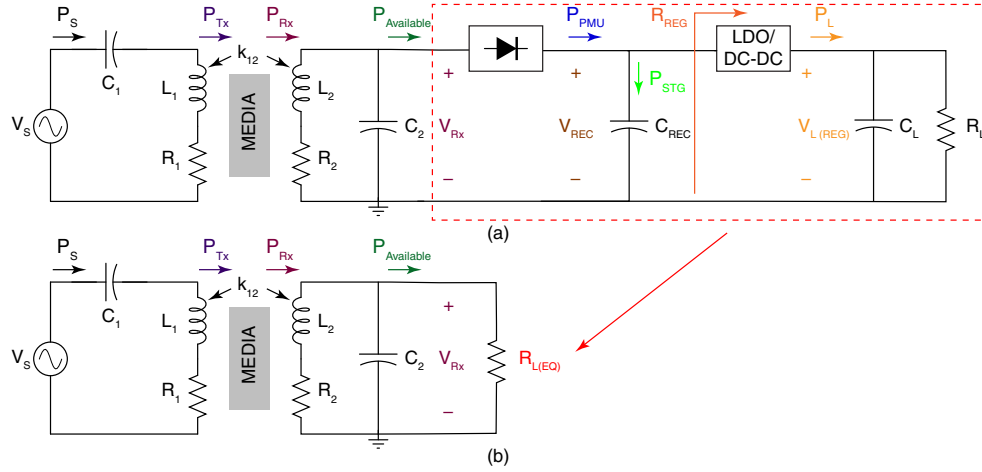


Figure 4.1: Simplified circuit of resonant inductive link with (a) VM receiver and its (b) equivalent loading when operating in steady state region.

The transient region is when the voltage across capacitors at the output of the rectifier and regulator circuits (i.e., C_{REC} and C_L) have not reached their final voltage levels. When operating in transient region, first, C_L reaches the regulated voltage level $V_{L(REG)}$, which implies that it is capable of sustaining $V_{L(REG)}$ across the load R_L . After that, C_{REC} continues to charge and it might take some time until it reaches a final value (i.e., steady state), which is the maximum V_{Rx} the inductive link can generate for a specific R_L . During this period, the rectifier (hence the link) sees a capacitive load. After reaching steady state, the average current through C_{REC} becomes zero (due to cyclic small charge/discharge) rendering the load to be effectively resistive.

The simplified circuit diagram of the resonant inductive link during steady-state operation is shown in Fig. 4.1(b), where $R_{L(EQ)}$ represents the equivalent load at the receiver (modeling the rectifier and its successive power consuming elements). For simplicity of analysis, let's assume

that a loss-less half-wave rectifier is used which results in $V_{Rx(peak)} = V_{REC}$. The load current which is supplied by the voltage regulator is $I_L = V_{L(REG)}/R_L$, where $V_{L(REG)}$ is the target regulated voltage to be maintained across the load for its proper functionality. Hence, the equivalent loading on the rectifier is the series combination of R_L and the voltage regulator's equivalent resistance (i.e., R_{REG}), which is obtained by dividing the voltage difference across the regulator and its current (i.e., I_L) as,

$$R_{REG} = \frac{(V_{Rx(peak)} - V_{L(REG)})}{V_{L(REG)}/R_L}. \quad (4.1)$$

Given that the rectifier is assumed to be lossless, the input power to the rectifier ($P_{In(REC)} = \frac{V_{Rx(peak)}^2}{2R_{L(EQ)}}$) equals to the regulator's power loss ($P_{Loss(REG)} = \frac{(V_{Rx(peak)} - V_{L(REG)})V_{L(REG)}}{R_L}$) plus the delivered power to the load ($P_L = \frac{V_{L(REG)}^2}{R_L}$). Therefore,

$$R_{L(EQ)} = \frac{V_{Rx(peak)}R_L}{2V_{L(REG)}}. \quad (4.2)$$

The above equation shows that the equivalent load at the receiver is a function of induced $V_{Rx(peak)}$, the value of actual load R_L , and the value of the regulated voltage level.

Fig. 4.2(a) shows the wireless inductive link's model along with Rx's equivalent circuit, where the series parasitic resistance of the receiving coil is converted to its parallel equivalent value, i.e. $R_{2P} = R_2(1 + Q_2^2)$, which is approximated as $\sim R_2Q_2^2$ considering a high-quality factor Rx coil ($Q_2 \gg 1$), which is necessary for an efficient wireless power transmission and re-

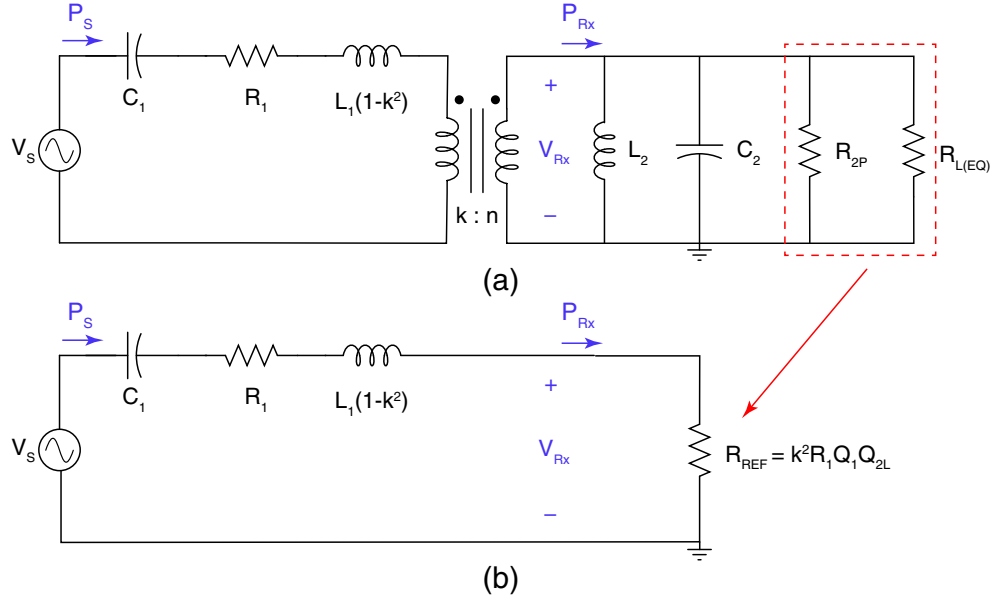


Figure 4.2: Equivalent circuit of resonant inductive link with (a) VM receiver and (b) reflected load.

ception [93, 133]. When both sides are tuned at the resonance frequency ($\omega_o = 1/\sqrt{L_1 C_1} = 1/\sqrt{L_2 C_2}$), the transmitter will experience a purely resistive load consisting of R_1 and R_{REF} , where $R_{REF} = k^2 R_1 Q_1 Q_{2L}$ represents the reflected impedance of the receiver side on the transmitting circuit [91, 92], and $Q_{2L} = Q_2 Q_L / (Q_2 + Q_L)$ with $Q_L = R_{L(EQ)} / (\omega L_2)$ are the receiver's parallel equivalent and the receiver's loaded quality factors, respectively. Therefore, the induced voltage at the receiver (V_{Rx}) and consequently, the voltage gain of the inductive link could be obtained by finding the voltage across R_{REF} and its equivalent secondary voltage by using k:n ratio ($n = \sqrt{L_2/L_1}$),

$$V_{Rx(peak)} = V_s \sqrt{\frac{L_2}{L_1}} \frac{k Q_1 Q_{2L}}{(1 + k^2 Q_1 Q_{2L})}, \quad (4.3)$$

which is going to be the amplitude of induced sinusoidal voltage at the receiver or at the input of the rectifier. As (4.3) implies, V_{Rx} and accordingly, the induced power at the receiver is dependent on its equivalent load, Tx's excitation voltage (represented by V_s), the two-coils parameters and their coupling conditions. By using (4.1) and (4.2), the relationship between $V_{Rx(peak)}$ at the input of rectifier ($V_{In(REC)}$) with its load R_L at a certain regulated voltage ($V_{L(REG)}$) is obtained as

$$V_{Rx(peak)} = \frac{V_s \sqrt{\frac{L_2}{L_1}} k Q_1 Q_2 R_L - 2V_{Reg} \omega_o L_2 Q_2}{R_L (1 + k^2 Q_1 Q_2)}. \quad (4.4)$$

The above equation indicates that even at a fixed coupling condition (i.e., distance, orientation, etc.) and Tx input voltage (V_s), V_{Rx} (and accordingly, $V_{In(REC)}$) would vary for different R_L or regulated voltage levels (i.e., $V_{L(REG)}$).

At resonance with a low coupling coefficient due to a miniaturized receiving coil (i.e., $L_1(1 - k^2) \approx L_1$), as shown in Fig. 4.2(b), the generated power by V_s divides between R_1 (including the source resistance R_s) and R_{REF} , where the latter represents the amount of transferred power to the receiver, which later gets divided between R_2 and $R_{L(EQ)}$. Therefore, the overall power transfer efficiency from the source to the load $R_{L(EQ)}$ (η_{tot}) and the delivered power to it (PDL) are [91]

$$\begin{aligned} \eta_{tot} = \eta_{Tx} \eta_{Rx} &= \frac{k^2 Q_1 Q_2}{(1 + k^2 Q_1 Q_2 + \frac{Q_2}{Q_L})} \frac{Q_2}{(Q_2 + Q_L)}, \\ PDL &= \frac{V_s^2}{2R_1} \frac{k^2 Q_1 Q_{2L}}{(1 + k^2 Q_1 Q_{2L})^2} \frac{Q_{2L}}{Q_L}. \end{aligned} \quad (4.5)$$

Accordingly, optimal $Q_L(Q_{L(opt)} = \frac{R_{L(EQ),opt}}{\omega_0 L_2})$ for maximum η_{tot} and PDL occur when the derivative of (4.5) with respect to Q_L are zero. These lead to [91]

$$\begin{aligned} Q_{L(opt,\eta)} &= \frac{Q_2}{\sqrt{1 + k^2 Q_1 Q_2}}, \\ Q_{L(opt,PDL)} &= \frac{Q_2}{1 + k^2 Q_1 Q_2}. \end{aligned} \tag{4.6}$$

Clearly, $Q_{L(opt)}$ is different for maximum η_{tot} and PDL, implying that maximum η_{tot} and PDL could not be simultaneously satisfied [91, 92], however, with high-Q coils at weak coupling conditions, they could turn out to be very close to each other [45]. Fig. 4.3 depicts the calculated versus simulated PDL, η_{Rx} , and η_{tot} for circuit parameters in Table 4.1 and when $R_{L(EQ)}$ was swept between 0 – 10 k Ω range. As shown, for miniaturized receiving coils, which is the case for biomedical implants, maximum PDL and η_{tot} occur very closely versus $R_{L(EQ)}$ due to a small coupling which results in a smaller R_{REF} compared to R_1 . As inferred from the plots, this optimal load approximately equals to the resistance of the secondary side at full resonance (i.e., Thevenin equivalent), where half of the received power is dissipated in the parasitic resistance of the receiving coil while the other half is delivered to the load ($\eta_{Rx} = 50\%$).

Fig. 4.4(a) represents the calculated $R_{L(EQ)}$ using (4.2) and its simulated counterpart versus R_L at different regulated voltage levels, visualizing the effect of regulated voltage value on the equivalent loading of the receiver. It is worth mentioning that for the case of a load with voltage

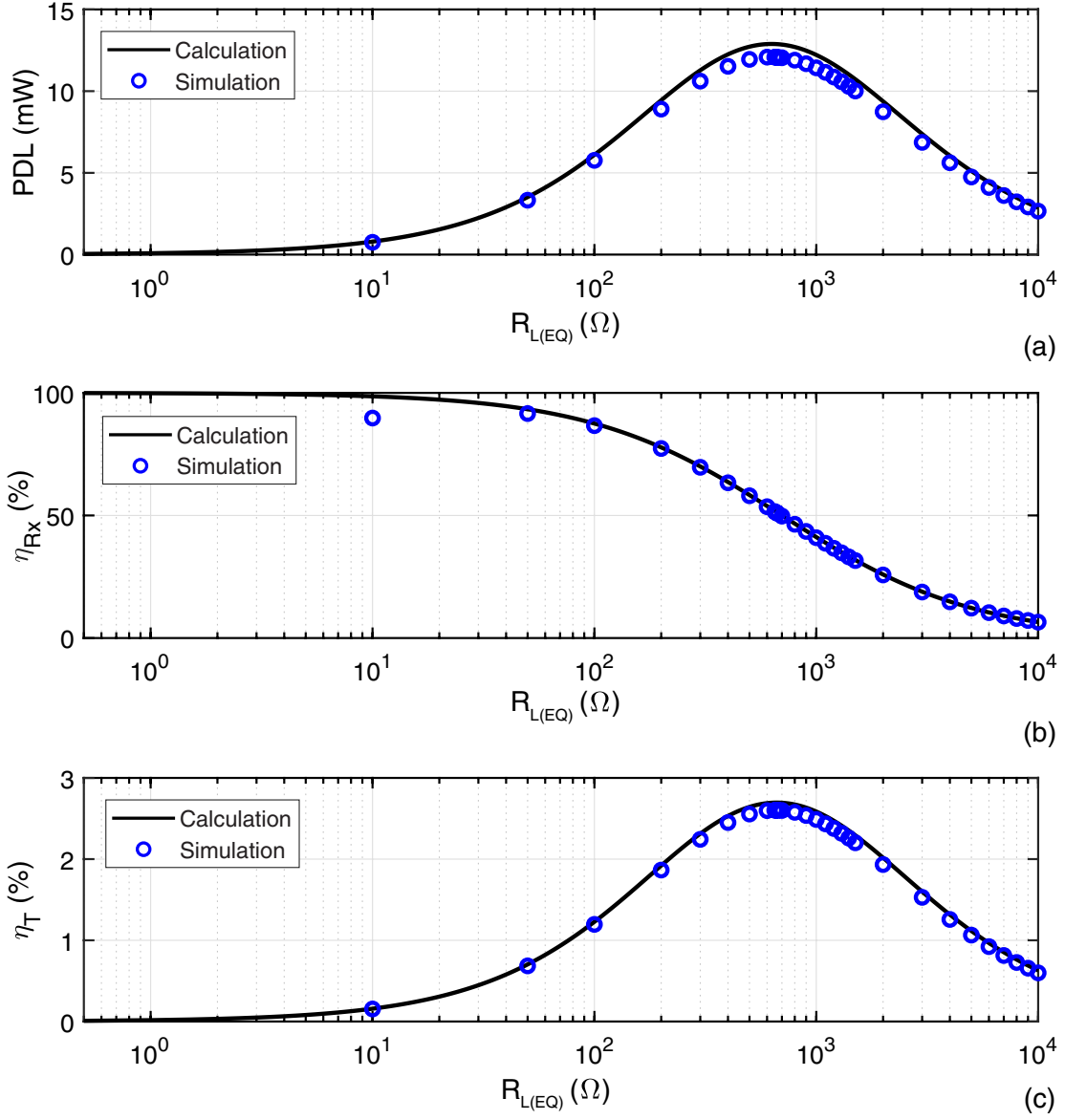


Figure 4.3: Comparison between calculated and simulated (a) PDL, (b) η_{Rx} , and (c) η_{tot} versus $R_{L(EQ)}$ for inductive resonant link with VM Rx with parameters described in Table 4.1.

Table 4.1: Simulation parameters of the inductive link with a VM receiver used to validate the modeling versus simulations.

Parameter	Value
f	1 MHz
$V_{s(peak)}$	5.5 V
k_{12}	0.01
L_1/L_2	205/4.2 μ H
C_1/C_2	123pF/6nF
C_L	1 μ F
R_1/R_2	30/1 Ω

regulation, maximum PDL occurs at the minimum R_L ($PDL = V_{L(REG)}^2/R_L$) at which the voltage regulation is successfully maintained. Fig. 4.4(b) shows the calculated and simulated $V_{Rx(peak)}$ at different $R_{L(EQ)}$, validating the performed analytical model. Fig. 4.4(c) shows η_{tot} ($P_{In(REC)}/P_s$) versus $R_{L(EQ)}$ for two different regulated voltages at which the maximum points occur at the optimal loading for both cases.

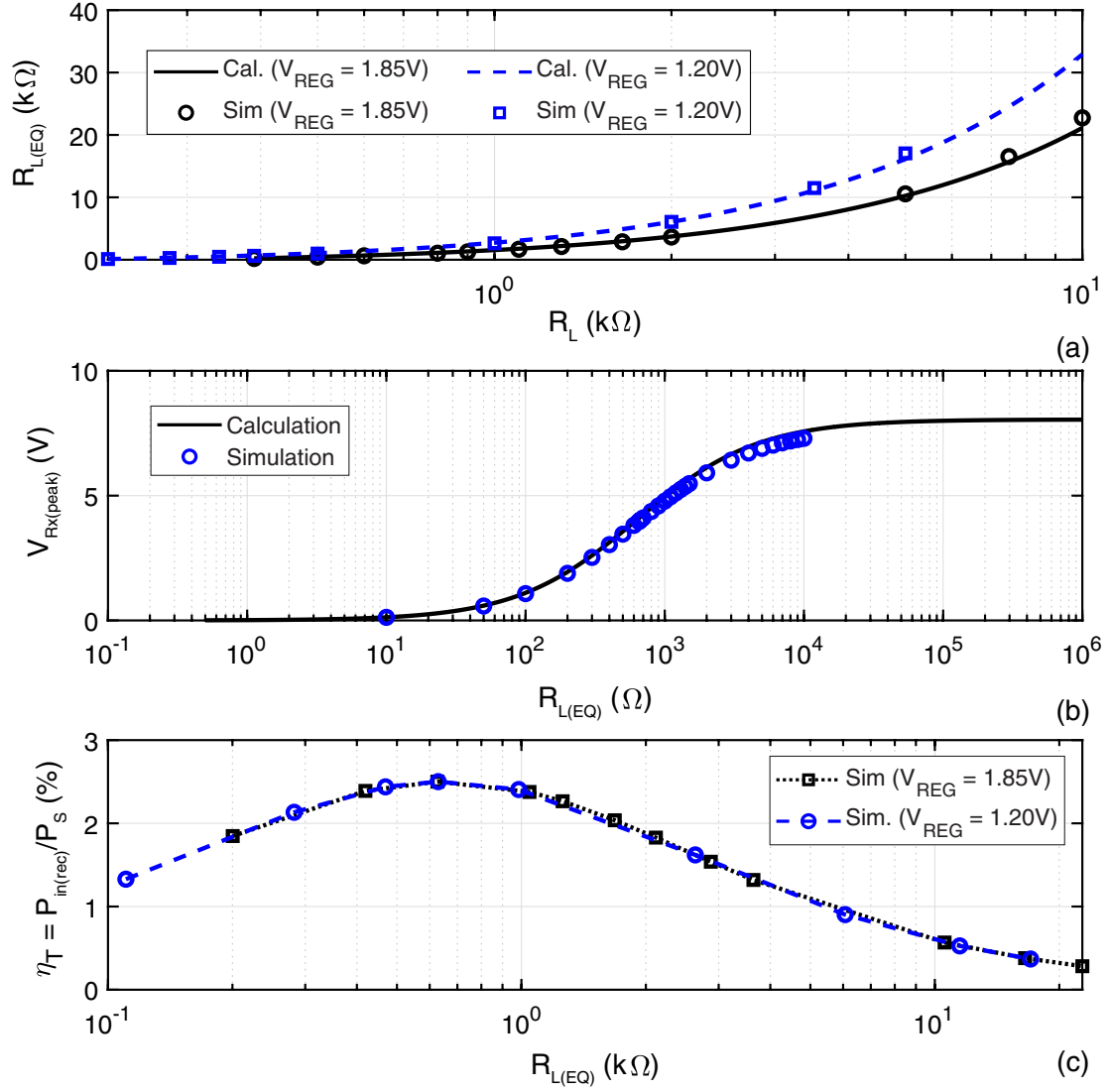


Figure 4.4: Comparison between calculated and simulated (a) $R_{L(EQ)}$ versus R_L , (b) $V_{Rx(peak)}$, and (c) η_{tot} versus $R_{L(EQ)}$ for inductive resonant link with VM Rx with voltage regulator and parameters described in Table 4.1.

4.2.2 Optimal Operation Schemes in Literature

Resistive Loads

Based on the theoretical discussion in the previous subsection, for any coupling condition, there exists an optimal impedance that the receiver needs to be loaded with to achieve the optimal operation. For varying load applications such as medical implants, a simple matching network with fixed discrete LC values at the receiver (such as [45] and [95]) fails to adaptively track the optimal impedance due to the dynamic variations of the load current or the coupling conditions.

Therefore, several works have been implemented in literature that propose adaptive matching schemes to achieve the required dynamic load transformation. In [103], the load transformation is achieved by dynamically modulating the loaded quality factor of the receiving coil by duty cycling a switch that is placed across the rectifier's inputs. By turning on the switch for a specific period of time to intentionally waste a specific amount of power, the load seen by the link is made as close as possible to the optimal loading condition. While this scheme helps in manipulating the reflected impedance on Tx at different R_L values, the efficiency degrades, particularly when longer turn-on duration of the switch is needed to achieve better matching.

Alternatively, an adaptive duty-cycled rectifier topology is proposed in [134] that is helpful in achieving the required complex impedance matching at different conditions. In [105] and [135], the optimal load is achieved by dynamically manipulating the duty cycle of the utilized DC-

DC converter (placed after the rectifier). To enhance the overall efficiency, both works need an additional wireless data link, which is required to transfer the load's power information to the Tx to perform efficiency calculation. To eliminate the need for the wireless link, the work in [106] sweeps the input power and accordingly manipulates the duty cycle of DC-DC converter until the required regulated voltage is achieved at the minimum Tx's input power. However, [106] does not provide a solution for estimating the coupling information. Therefore, a load estimation algorithm at the transmitter is proposed in [107] by which the Tx's input power is dynamically adjusted according to its estimated loading conditions.

Capacitive Loads

Regardless of the differences mentioned in their implementation, all the methods described in the previous section can be applied to scenarios involving resistive loads. However, as discussed earlier in Chapter 1, the primary objective of this thesis is to *efficiently store surplus energy* for high-intermittent loads after supplying the required power to low-continuous loads. When energy storage comes into play, the load becomes capacitive. Unlike resistive loads, which benefit from a fixed regulated voltage, the voltage of capacitive loads varies as they charge. This results in a continuously variable loading condition, influenced by the charging process itself [92, 118, 136]. Consequently, the loading condition changes after each or every few resonance cycles (depending on the rate of change in the capacitive load's voltage), necessitating an adaptive

matching network capable of sensing and adjusting with a wide range of impedances, which is impractical to implement efficiently. This differs greatly from adapting to load variations caused by random and infrequent changes in power consumption of the implanted device or changes in the inductive link's coupling condition due to coil movement, among other factors. Therefore, maintaining an optimal loading condition for power delivery and storage is considerably more challenging than with resistive loads.

In [92], a multi-tapped inductor is used in the receiver to adjust the parameters of its LC tank in response to the loading of the charging capacitor. This adjustment aims to optimize the power transfer in accordance with the maximum power condition or profile specific to the charging capacitor. Consequently, modifying the resonating capacitor in the receiver becomes essential in order to maintain resonance frequency alignment between the receiver's LC tank and the transmitter's (resulting in increasing Rx's form factor), as the inductor value in the receiver is changed to perform the required impedance matching. Furthermore, real-time processing is required at the receiver to measure the actual power being delivered to the charging capacitor, which requires high speed and high computation power.

In [118], it is demonstrated that connecting the energy storage element (e.g., rechargeable battery) directly to the rectifier's output, without any control scheme (i.e., no constant current and constant voltage operations), speeds up the charging process. Similarly, in [119, 137], high-demanding load events (e.g., data Tx) are activated when the voltage on C_{REC} reaches a certain

high threshold. They continue until C_{REC} discharges to a predefined lower threshold to maintain implant's (or Rx) functionality. The charging of C_{REC} introduces an instantaneously varying load on the L_2C_2 tank during the transient period between the two voltage levels. This load depends on the charging capacitor's voltage and current, which affects the induced V_{Rx} level (according to equation (4.4)) and the received power (P_{Rx}). However, the optimal loading for the receiver depends on the wireless link's parameters (as per equation (4.6)), which may not align with the voltage across the charging capacitor. Induction of maximum power at the receiver is only possible when the voltage across C_{REC} is close to the optimal voltage from the link's perspective (i.e., $V_{Rx(opt)}$, discussed in the next subsection).

While the above mentioned approach minimizes rectifier losses by avoiding the need for an additional stage, however, the voltage on the storage unit is not guaranteed to be in a close proximity of $V_{Rx(opt)}$. This results in sub-optimal loading at the receiver, resulting in a lower power available at the input of the rectifier. Therefore, simultaneously maximizing the received power and efficient energy storage is challenging without proper isolation between the L_2C_2 tank and the storage element. Accordingly, using C_{REC} or directly connecting the rechargeable battery at the rectifier's output is not advantageous for efficient wireless energy storage. Uncontrolled charging of C_{REC} leads to inefficient energy storage as it results in lower P_{Rx} when the voltage of C_{REC} deviates from its optimal value, i.e., $V_{Rx(opt)}$, representing the optimal loading for the link.

To control the charging current profile, [123] replaces the AC-to-DC converter stage in the

inductive wireless power receiver with a single capacitor and switches connected in a way to work as a current source that charge two different storage capacitors with positive and negative polarities. However, an adaptive resonance capacitor tuner is required to compensate for the variations in the effective capacitance across the receiver's coil during charging. Additionally, the voltage on the storage capacitor can never exceed the magnitude of the incident waveform V_{Rx} , similar to the VM receivers that employ rectifiers for the sake of AC to DC conversion (Fig. 4.1(a)).

4.2.3 Optimal Operation for Simultaneous Energy Storage and Power Delivery — Principle of Operation

Fig. 4.5 shows simulated PDL and η_{tot} versus $V_{Rx(peak)}$ for inductive resonant link with VM receiver with parameters described in Table 4.1. The voltage level at the receiver could swing between zero (i.e., short circuit), where all induced current at the receiver is passed to the load and no resonance circuit is formed, and its maximum level (i.e., open circuit), where no load is connected across the receiver coil (or no current is drawn from L_2C_2 tank) and all the received power is dissipated in the parasitic resistance of the coil R_2 . As the plot shows, the maximum PDL and efficiency occur at approximately the same $V_{Rx(peak)}$ value across the load, which is considered as the optimal voltage level $V_{Rx(opt)}$ for the receiver to maintain the optimal opera-

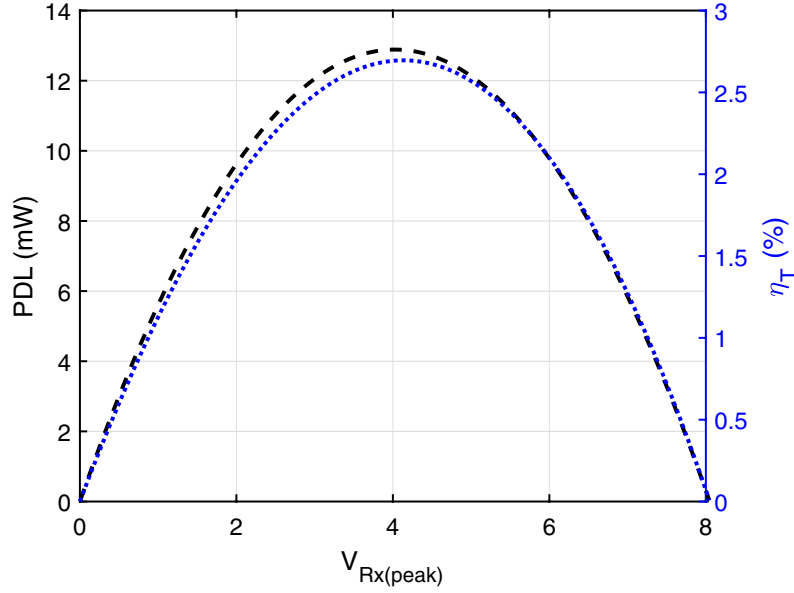


Figure 4.5: Simulated PDL and η_{tot} versus $V_{Rx(peak)}$ for inductive resonant link with VM Rx with parameters described in Table 4.1.

tion.

In summary, achieving a controlled and efficient charging process requires two key elements. First, maintaining $V_{Rx(opt)}$ across the receiver (or at the rectifier's output) to impose optimal loading on the transmitter, hence guarantee maximum power delivered to the Rx coil (i.e., max P_{Rx}). Second, isolating the energy storage element from the L_2C_2 tank to prevent it from varying the reflected load on the transmitter during the overall charging/discharging periods, i.e., energy storage/recycling. By doing so, the optimal loading for L_2C_2 tank will be maintained without the need for manipulating their values, which eliminates the need for an adaptive impedance matching network for maximum power reception and delivery, while different voltage levels could be

achieved by proper voltage level conversions.

Fig. 4.6(a) illustrates a conceptual block diagram of the proposed system and demonstrates how the storage capacitor (C_{STG}) can be added to the receiver. The main purpose of the charger block is to have a controlled charging that results in the maximum power at the input of the rectifier, and consequently, energy storage in C_{STG} , while having different load values (i.e., R_L) at the receiver. As mentioned earlier, maintaining $V_{Rx(opt)}$ is critical for having the maximum received power. After determining $V_{Rx(opt)}$ in the calibration phase (will be discussed later), it is necessary to maintain the output of the rectifier at this voltage level to ensure a fixed optimal conduction angle of the rectifier at all times, thus guaranteeing maximum P_{Rx} . When maximum possible P_{Rx} is induced (i.e., maximum $P_{Available}$), the surplus power which is $P_{PMU} - P_{RL1}$ needs to be diverted towards C_{STG} . This needs to be done without changing V_{REC} (i.e., some form of voltage isolation between C_{REC} and C_{STG}) and regardless of V_{STG} being smaller or larger than V_{REC} .

In the absence of the charging circuit and C_{STG} , during each resonance cycle, part of the power at the output of the rectifier (P_{PMU}) is absorbed by the load (P_{RL1}), and the remaining surplus is automatically directed to C_{REC} , resulting in C_{REC} 's voltage (V_{REC}) to start to increase. This increase is not desired as we ideally aim to keep V_{REC} , hence V_{Rx} , constant at $V_{Rx(opt)}$. Therefore, once such an increase is detected (by CMP1), the charger circuit must be activated to direct all the surplus power to a storage capacitor, which is isolated from the rest of the circuit,

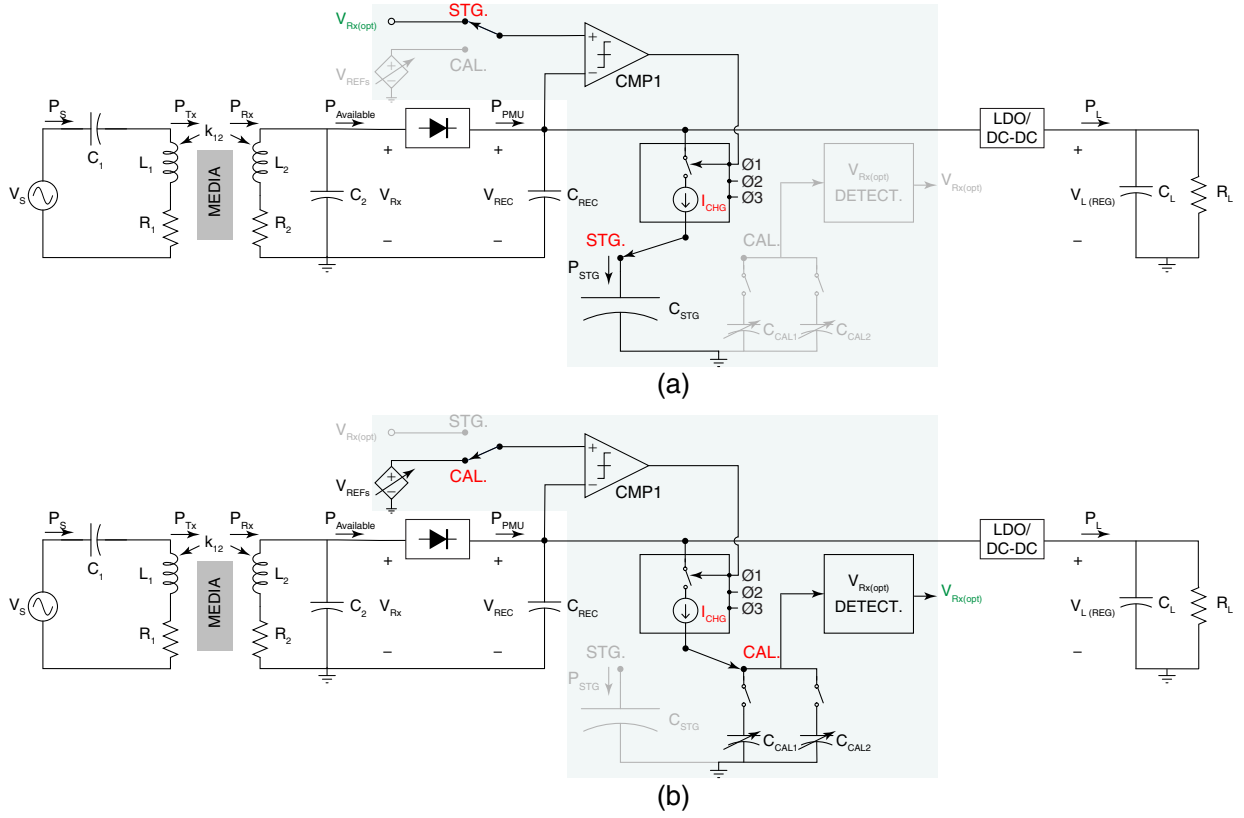


Figure 4.6: Conceptual block diagram of the proposed energy storage for VM receivers: (a) normal operation, (b) calibration phase.

so its charging/discharging does not affect the V_{REC}/V_{Rx} . Further increase of voltage across the receiver is prevented as the current is pulled by the charger unit. On the other hand, this current pulling needs to be stopped when V_{REC} reduces back to $V_{Rx(opt)}$ to avoid deviation from the optimal loading condition. As the comparator provides the timing (ϕ_1) for current pulling based on its voltage comparison result, a voltage-controlled current-mode charging process is realized. Of course, the charger unit needs to isolate C_{REC} and C_{STG} with different voltages from each other while being capable of pulling sufficient current for bringing V_{REC} to its optimal level prior to conduction of the rectifier in the next resonance cycle.

As shown in Fig. 4.6(b), the circuit also requires a calibration phase to detect $V_{Rx(opt)}$ level as a result of infrequent coupling variations. During this phase, the comparator's reference voltage is swept and the charger circuit is used to charge two capacitors with smaller capacitances, to speed-up the charging process, while maintaining V_{REC} at each V_{REF} . The size of the capacitor bank could be varied depending on the input power to develop suitable voltage ranges for comparison during the specified period for charging each calibration capacitor. The detailed implementation of this stage is discussed in the next subsection.

4.2.4 $V_{Rx(opt)}$ Detection and Loading Isolation – Circuit Implementation

The theoretical discussions up to now suggest that by maintaining a constant optimal V_{Rx} across the receiver (i.e., $V_{Rx(opt)}$) and consequently, at the output of the rectifier (V_{REC}), the conduction

angle of the rectifier (i.e., $t_{ON(Rec)}$) is automatically fixed to its optimal duration, thus the current being pulled from the L_2C_2 tank is optimal, hence the $R_{L(EQ)}$. This optimal loading results in the highest possible energy reception and delivery from L_2C_2 tank. This means that the voltage across C_{REC} (i.e., V_{REC} , which represents V_{Rx}) needs to be continuously monitored, and once it reached the optimal value, the current supplied by the rectifier is directed towards an energy storage element by the charger unit to maintain the V_{Rx} at $V_{Rx(opt)}$ without operating at sub-optimal loading, wasting the extra received energy, or changing the inductive link's loading. This strategy also eliminates the need for any back-communication link or other methods for achieving an efficient wireless charging as well as the need for manipulating the receiving LC tank.

Charger Unit

The implementation of the charger unit is not feasible with a simple switch. This limitation arises from the inability of a simple switch to effectively isolate the voltages across C_{REC} and C_{STG} . Additionally, it necessitates an extremely high-speed comparator to precisely deactivate the switch at the appropriate instant and prevent unwanted deviation in V_{REC} , as the discharging/charging duration is going to be very short due to the capacitance difference between the two mentioned capacitors.

Fig. 4.7 shows an inductor with four different switches, which are used in a discontinuous

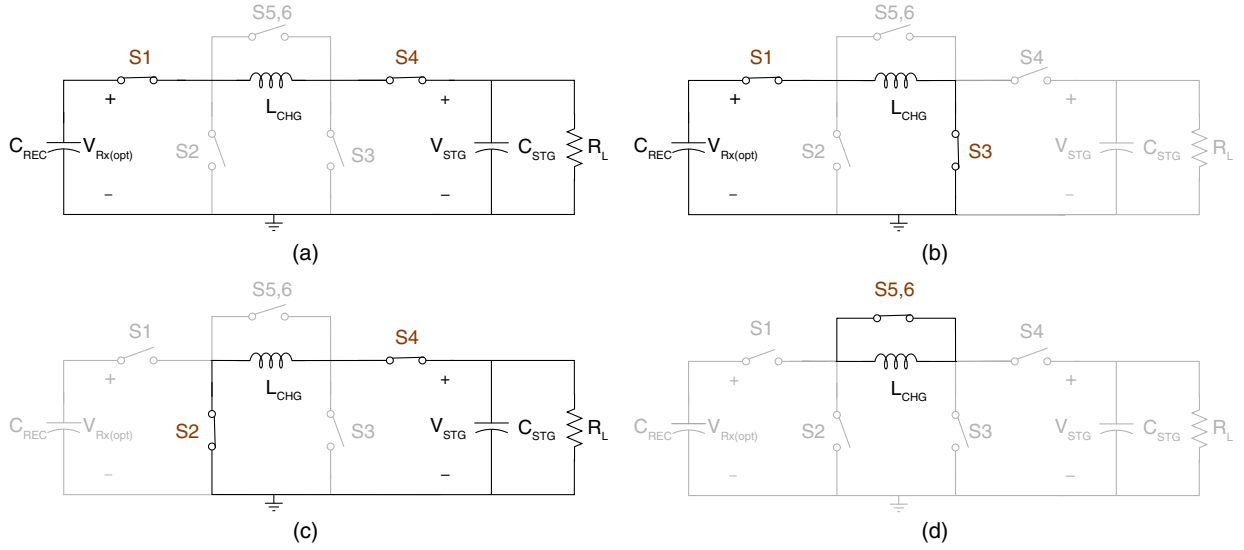


Figure 4.7: Circuit diagram of power converter used for maximizing energy storage in VM receivers: (a) buck operation - ϕ_1 , (b) boost operation - ϕ_1 , (c) ϕ_2 for both buck/boost operations, and (d) freewheeling - ϕ_3 in discontinuous conduction mode for both modes.

conduction mode (DCM) for the purpose of charging the storage capacitor without interfering with the link's optimal operation. If $V_{Rx(opt)} > V_{STG}$, the circuit should be operated in a buck mode to efficiently charge the storage capacitor with a lower voltage level. If $V_{Rx(opt)} < V_{STG}$, the circuit needs to be operated in a buck/boost mode to facilitate charging of the storage capacitor with a higher voltage level [138–141]. Assuming $V_{REC} = V_{Rx(opt)}$ from previous cycle (or more precisely $V_{REC} = V_{Rx(peak)} - V_{REC(Drop)}$, where $V_{REC(Drop)}$ represents the voltage drop across the rectifier), V_{REC} increases above $V_{Rx(opt)}$ as the rectifier starts to conduct, which is going to be captured by the comparator (CMP1 from Fig. 4.6). Accordingly, S_1 turns ON to initiate the energy storage path in parallel with C_{REC} and divides the current through the rectifier between

C_{REC} and the power converter. As shown in Fig. 4.8, when the rectifier turns-off (i.e., when V_{Rx} goes below V_{REC}), ϕ_1 continues as long as $V_{REC} > V_{Rx(opt)}$ by keeping S_1 ON in order to transfer the additional energy in C_{REC} through the converter and discharge V_{REC} back to $V_{Rx(opt)}$ for optimal loading of the inductive link in the next upcoming cycle. The figure also shows that the current through the power converter is supplied from C_{REC} during ϕ_1 until V_{REC} comes back to $V_{Rx(opt)}$ while the rectifier is not conducting. It is worth mentioning that for the aforementioned discussion, it is assumed that C_{REC} is capable of providing the required continuous current by R_{L1} without experiencing a noticeable voltage drop across it. If the power demand of R_{L1} surpasses the maximum incoming power, V_{REC} could not reach $V_{Rx(opt)}$. In this scenario, all the incoming power must be directed to the load, leaving no surplus energy for storage. Consequently, the charger unit needs to be disabled.

In buck mode, S_4 is always ON to directly transfer the energy to C_{STG} during ϕ_1 (Fig. 4.7(a)). In buck/boost mode, the inductor is first charged by turning S_3 ON during ϕ_1 and S_4 is OFF to prevent discharge of C_{STG} due to its higher voltage level than $V_{Rx(opt)}$ (Fig. 4.7(b)). During ϕ_1 , the inductor current increases linearly proportional to the voltage difference across its terminals ($V_L = L di/dt$). When V_{REC} equals $V_{Rx(opt)}$, S_1 turns OFF and as the inductor opposes any sudden change in its current, S_2 is instantly turned ON to transfer the remaining energy in the inductor to C_{STG} and complete the charging process during ϕ_2 (Fig. 4.7(c)). Eventually, ϕ_2 is terminated when a zero current condition is detected in the inductor (using a zero-current detector, which

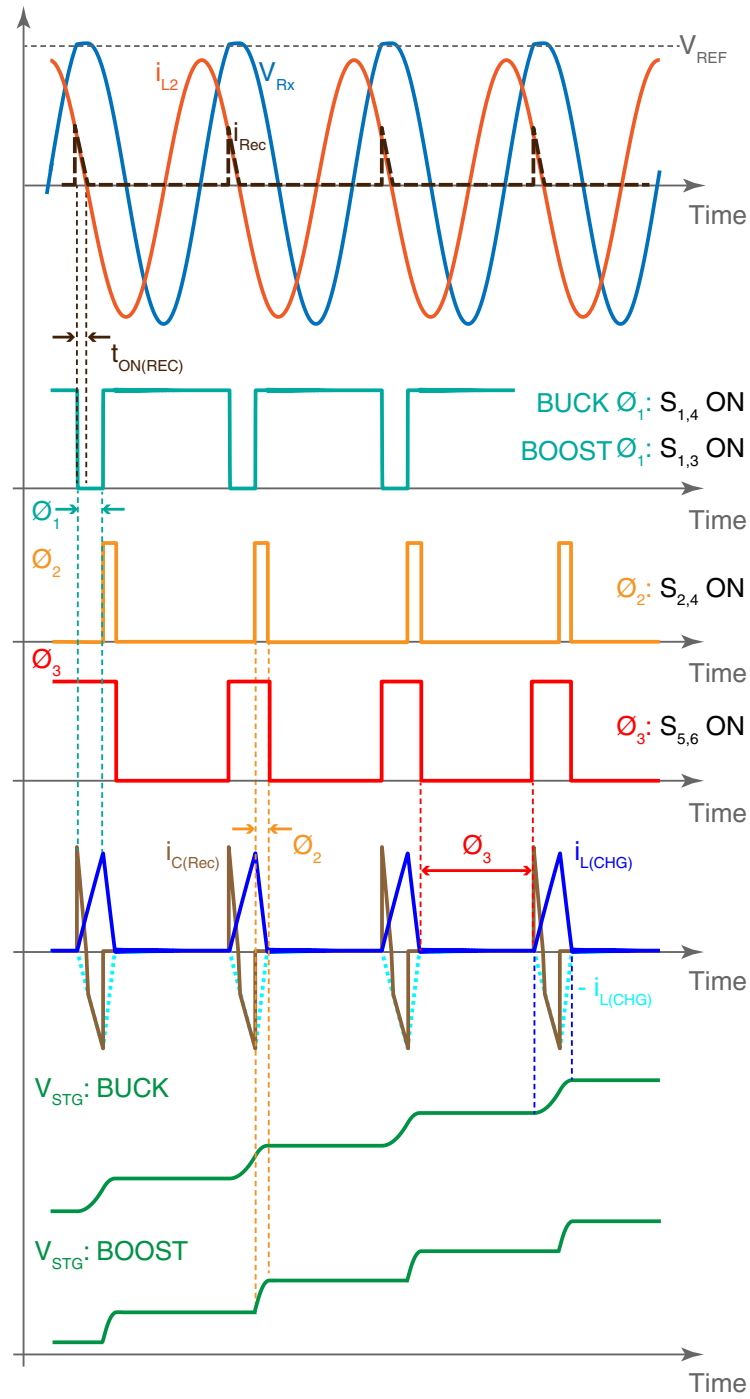


Figure 4.8: Conceptual waveforms for energy reception and storage.

will be discussed later). It should be noted that this step is not required if a low threshold diode is used instead of S_2 and S_4 for an efficient operation of the power converter. Finally, as shown in Fig. 4.7(d), the inductor's terminals are connected through $S_{5,6}$ during ϕ_3 to prevent possible ringing in the system prior to the next energy transfer cycle [142]. The conceptual waveforms when the rectifier is loaded with the charger unit for energy storage are depicted in Fig. 4.8. The same waveforms are valid for both buck and boost modes, except for the charging duration, which are annotated to distinguish between the two cases.

Calibration Unit

As explained above, the loading variation of the charging capacitor is isolated from the inductive link by the use of the inductor-based charging circuit described above. However, the optimal loading and $V_{Rx(opt)}$ are related to the coupling coefficient as well. Therefore, the main task of the calibration unit is to determine the $V_{Rx(opt)}$ level as a result of possible coupling variations between Tx-Rx coils due to an unexpected change in distance and alignments. Furthermore, this block is designed in a way to simplify the required power measurement at the load to a simple voltage measurement and comparison.

Fig. 4.9(a) shows the block diagram of the calibration unit. In general, it consists of a digital controller and two capacitor banks to perform the charging and voltage comparison. In summary, we need to set the voltage across the receiver to a certain V_{REF} , run the link for a

few cycles and perform capacitor charging with the charger unit and small C_{STG} (to get a higher voltage suitable for comparison in shorter duration), increase V_{REF} and perform the charging with another capacitor (with the same size as the previous one), and compare the two voltages across the two capacitors. This process should start with the minimum V_{REF} value and should be repeated as long as the amount of energy stored in capacitor banks over a fixed period of time is higher for $V_{REF(i)}$ compared to $V_{REF(i-1)}$. Once this is not correct (i.e., for $V_{REF(k)}$, $V_{C_{STG(k-1)}} < V_{C_{STG(k)}} > V_{C_{STG(k+1)}}$), then $V_{REF(k)}$ is the optimal reference that sets $V_{Rx(opt)}$ that leads to maximum V_{STG} . It is worth mentioning that to generate higher reference voltages, a voltage doubler is essential to supply the multi-reference generator. An analog multiplexer is used to connect each V_{REF} according to the sweeping condition at to the input of the comparator.

Fig. 4.9(b) shows how the required timing for the calibration unit is generated. The timing generation consists of a clock recovery (zero-crossing detector), n-bit counter, non-overlap clock generation, and logic flops for signal conditioning associated with each alternate cycle. Similar to the presented scheme in Chapter 3, two different capacitor banks with same capacitances are charged in an alternative fashion for the two successive V_{REF} levels. The size of the capacitor banks could be modified by orders of magnitude depending on the input power to reach a sensible voltage level at the end of charging time at the input of a strongArm comparator, i.e., $V_{CAL(R),(L)}$. By maintaining the same overall charging time for all cases, the voltage levels on each capacitor bank at the end of the pre-defined charging period are compared. Accordingly,

the capacitor banks are discharged alternately to be used for the next V_{REF} ($CLR_{(R),(L)}$) after the comparison. The highest voltage across the capacitors occurs when $V_{REF} = V_{Rx(opt)}$, when no change is observed at the comparator's output state for two consecutive cycles (Fig. 4.9(c)). Fig. 4.9(d) illustrates an example for the timing diagram of the calibration unit. It is worth mentioning that when the comparison is performed, the receiver needs to be loaded with another capacitor, preferably C_{STG} to have an actual load and prevent energy loss with a dummy capacitor.

4.2.5 Verification of Optimal Operation

The effectiveness of the presented scheme was verified using Cadence simulation and experimental measurement. Fig. 4.10(a) shows the input power of the rectifier ($P_{In(REC)}$) and the power stored in C_{STG} (P_{STG}) versus $V_{Rx(peak)}$. As the plot shows, $V_{Rx(opt)} = 3.84$ V results in the highest power delivery and storage in the receiver. Fig. 4.10(b) shows the simulation results for the overall induced power at the receiver (P_{Rx}) as well as P_{STG} and the delivered power through a voltage regulator ($P_{RL(REG)}$) for different R_L s. For all cases, the regulating voltage across the loads (i.e., $V_{L(REG)}$) was 1.85 V, while V_{Rx} was maintained at $V_{Rx(opt)} = 3.84$ V. As shown, a fixed level of P_{Rx} is maintained independent of R_L loading variations, which verifies successful load isolation during the overall energy storage in the receiver, resulting in a constant R_{REF} on the transmitter. As the plot shows, the surplus energy than what consumed by the load is successfully directed to the storage element summing up to the maximum possible P_{Rx} under different loading condi-

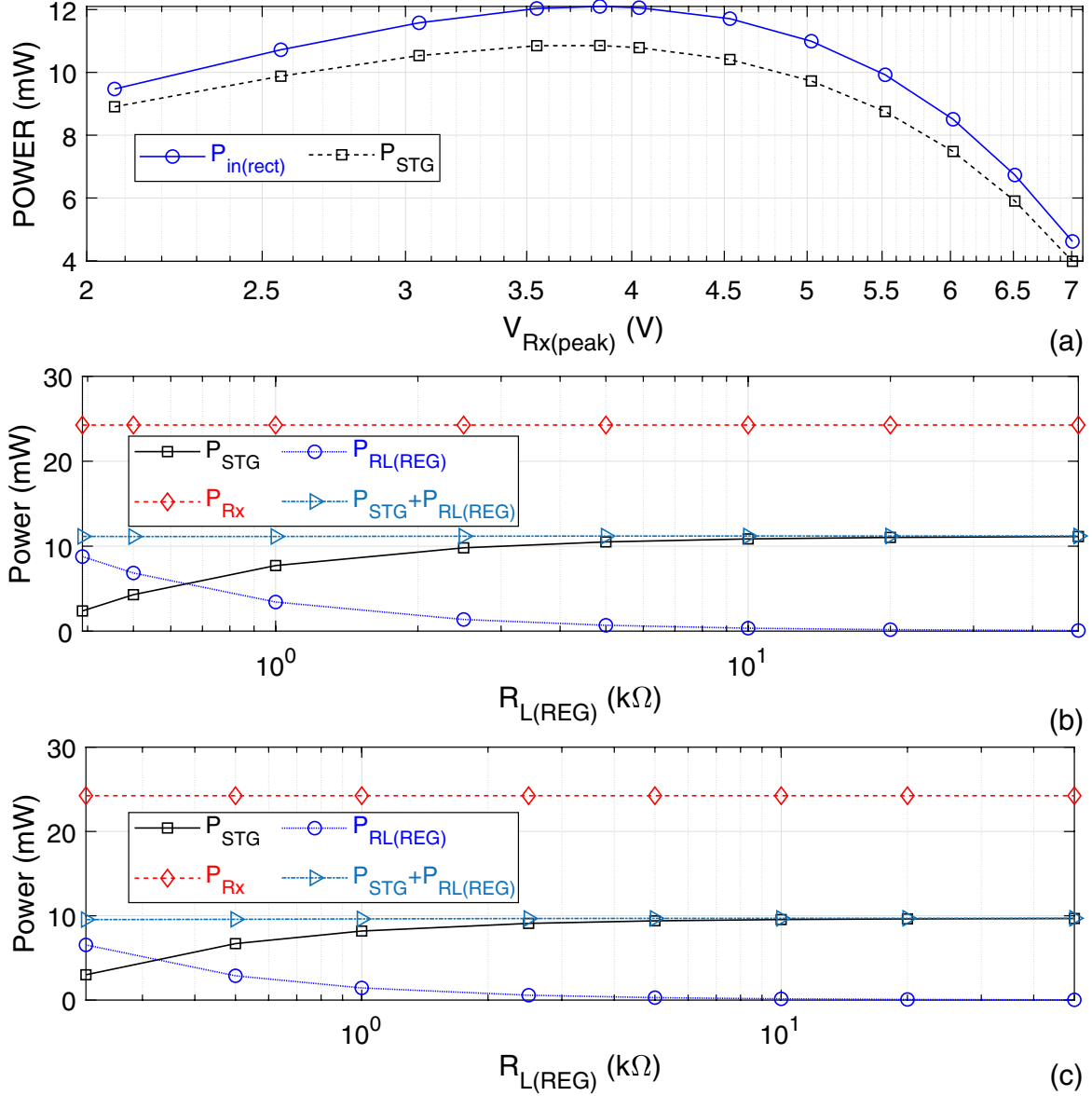


Figure 4.10: Simulated results verifying VM receiver's optimal operation (a) input power of rectifier and stored power versus $V_{Rx(peak)}$, and power breakdown versus $R_{L(REG)}$ when operating at $V_{Rx(opt)}$ for (b) $V_{L(REG)} = 1.85$ V, and (c) $V_{L(REG)} = 1.20$ V.

tions. Fig. 4.10(c) confirms the same results and validates maximum P_{Rx} reception when a 1.2 V regulator was used at the receiver.

4.3 Implementation of Simultaneous Optimal Energy Storage and Power Delivery

4.3.1 System-Level Integration

Fig. 4.11 shows the block diagram of the developed IC and the way it is interfaced with a VM inductive power receiver. The IC is designed and fabricated in a standard $0.18\ \mu\text{m}$ CMOS technology, and comprises of a buck/boost power converter with integrated power switches, a calibration unit to flag $V_{Rx(opt)}$, a low drop-out voltage regulator (LDO), a multi-level voltage reference generator, a digital controller to control the operational mode of the power converter according to $V_{Rx(opt)}$ and V_{STG} levels (i.e., buck or buck/boost) with the help of voltage comparators. Moreover, for a battery-less receiver, a voltage doubler and level shifters are necessary in order to achieve a boosted voltage level in the system to properly control the power switches and prevent them from un-intentional conduction in addition to generating higher reference voltages than V_{REC} .

Fig. 4.12 shows the annotated chip's micrograph, which occupies $2 \times 2\ \text{mm}^2$ area including the pads. For the charging inductor (L_{CHG}) and the storage capacitor (C_{STG}) we used off-chip

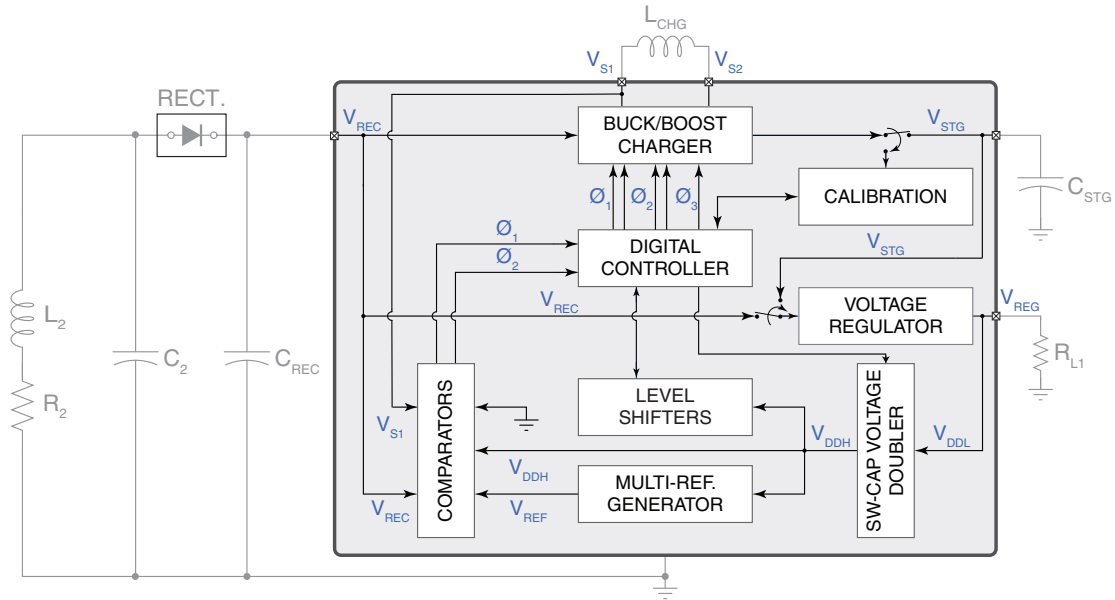


Figure 4.11: Block diagram of the presented overall link's energy storage efficiency maximizer IC and how it is interfaced with a VM receiver.

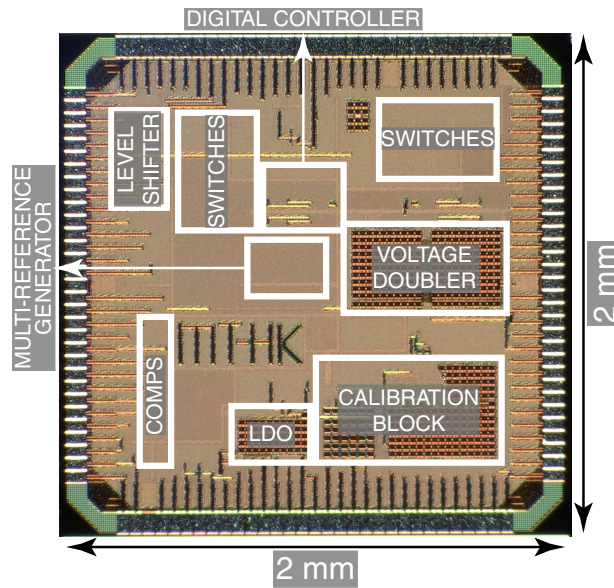


Figure 4.12: Annotated chip micrograph of the presented IC for VM receivers.

components, which allows for adjusting their size depending on the link parameters and application.

4.3.2 Transistor-Level Implementation

Buck-Boost Power Converter

To achieve a highly-efficient energy storage, it is critical that the losses in the power converter are minimized. For the case of an integrated buck/boost power converter, the required switches could be implemented using MOS devices. Conduction and switching losses are considered as the main sources of efficiency degradation in such power converters. Lowering the MOS ON-resistance by utilizing wider devices would lower the conduction loss. However, wider device sizes result in an increase of the gate capacitance, which would consequently increase the switching losses at higher switching frequencies in the controlling circuitry [143]. Hence, the actual trade-off is considered in balancing the conduction and switching losses by properly sizing the power MOS switches for the target application [144]. Alternately, low-threshold Schottky diodes could be used instead of S_2 and S_4 (Fig. 4.7) for non-integrated solutions as well.

Fig. 4.13 shows the integrated buck/boost charger implemented using CMOS switches. As shown, a CMOS switch is used for implementing S_4 to further reduce the conduction losses for different ranges of output voltages and allow for its full turn-ON independent of the voltage difference across it. While NMOS transistors are sufficient for pulling down purposes of S_2 and



The shown comparators (CMP1 and ZCD) in Fig. 4.13 are necessary for generating ϕ_1 and ϕ_2 to activate the storage path and terminate the charging process, respectively. As explained earlier, the first comparator is required to trigger the converter and provide an asynchronous clock (i.e., ϕ_1) for the highest possible power extraction from L_2C_2 tank through the rectifier. The second comparator is used as a zero-current detector to flag the zero current status and terminate the charging process (i.e., end of ϕ_2). At the onset of ϕ_2 and when L_{CHG} is already charged due to ϕ_1 , V_{S1} becomes negative to allow for $i_{L(CHG)}$ discharge to the load. With the flow of current, V_{S1} gradually increases until it reaches zero, indicating a zero current condition. Therefore, this point could be detected by comparing V_{S1} with GND to terminate ϕ_2 and prevent the discharge

Table 4.2: Optimized device sizes of the integrated buck/boost charger.

Transistor	W/L	$f \times m$	Transistor	W/L	$f \times m$
S_1	$4\mu\text{m}/300\text{nm}$	100×10	$S_{2,3}$	$4\mu\text{m}/600\text{nm}$	60×4
$S_{4(P)}$	$20\mu\text{m}/300\text{nm}$	50×50	$S_{4(N)}$	$4\mu\text{m}/600\text{nm}$	60×4
S_5	$20\mu\text{m}/300\text{nm}$	50×1	S_6	$20\mu\text{m}/300\text{nm}$	50×1

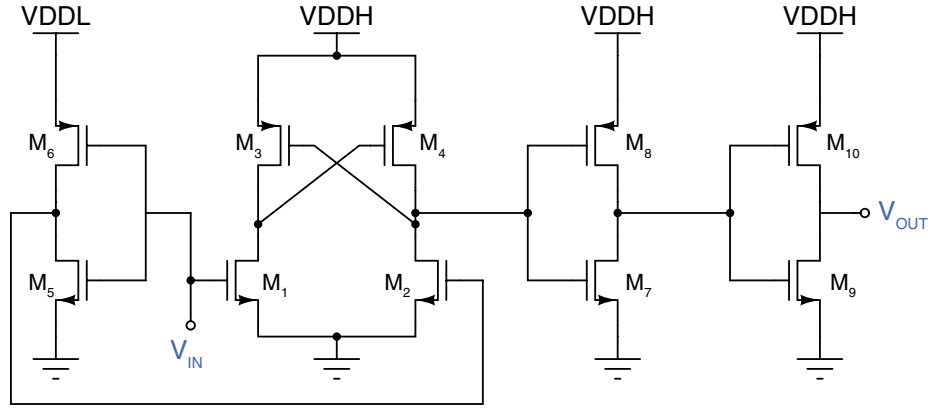


Figure 4.14: Circuit diagram of the used level shifter.

of load through L_{CHG} . It is worth mentioning that a zero-current detection is not required if low-threshold diodes are used instead of S_2 and S_4 in the power converter.

Furthermore, gate driving circuits are implemented using level shifters [145] (Fig. 4.14 with sizes in Table 4.3) and cascaded inverters with increasing device sizes.

To illustrate the effectiveness of the proposed energy storage optimization and the operation of the power converter in the buck/boost mode, we conducted simulations using the power

Table 4.3: Device sizes of the level shifter circuit.

Transistor	W/L	Transistor	W/L
$M_{1,2}$	$3\mu\text{m}/1.2\mu\text{m}$	$M_{3,4,7,9}$	$1\mu\text{m}/350\text{nm}$
M_5	$1\mu\text{m}/1.2\mu\text{m}$	$M_{6,8,10}$	$3\mu\text{m}/350\text{nm}$

converter and the inductive link parameters detailed in Table 4.1 in Cadence. Fig. 4.15 shows the simulated stored power (P_{STG}) in scenarios with $C_{REC} = 50$ pF while charging a $C_{STG} = 100$ μF with 3 V initial voltage supplying $R_L = 50$ k Ω at $V_{L(REG)} = 1.85$ V, while $V_{s(peak)}$ was set to 1.5 V and 2.5 V at the transmitter. The horizontal axis represents V_{REF} , the reference voltage set at CMP1 for comparison purposes of current pulling at the receiver. The results obtained validate the direct proportionality of $V_{Rx(opt)}$ to V_s , which determines the Tx power. Furthermore, they affirm the advantages of operating at $V_{Rx(opt)}$ to maximize input power to the rectifier and efficiently charge C_{STG} at a higher voltage on the receiver end. This is particularly beneficial in scenarios where interruptions in the inductive link might lead to reduction of induced power at the receiver.

Voltage Comparator (CMP1)

Fig. 4.16 shows the schematic of the implemented voltage comparator, which serves as the required asynchronous clock generator for optimal energy storage. The sizing of the used tran-

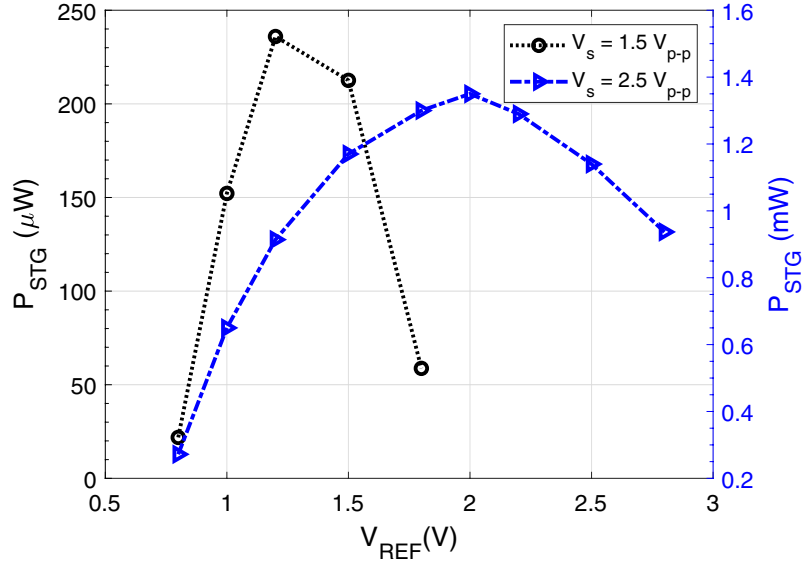


Figure 4.15: Simulated P_{STG} versus V_{REF} using buck/boost converter for inductive resonant link with VM Rx with parameters described in Table 4.1 for $V_{s(peak)} = 1.5$ and 2 V.

sistors are provided in Table 4.4. The output of the circuit remains at GND level to control the turn-ON window of S_1 as long as V_{REC} remains higher than $V_{REF} = V_{Rx(opt)}$. With little deviation between V_{REC} and V_{REF} , which are applied to the gates of M_1 and M_2 , respectively, the cross-coupled M_3 and M_4 help in faster current steering in the differential pair resulting in a fast settlement of the output voltage to the desired voltage level based on the difference between the input voltages.

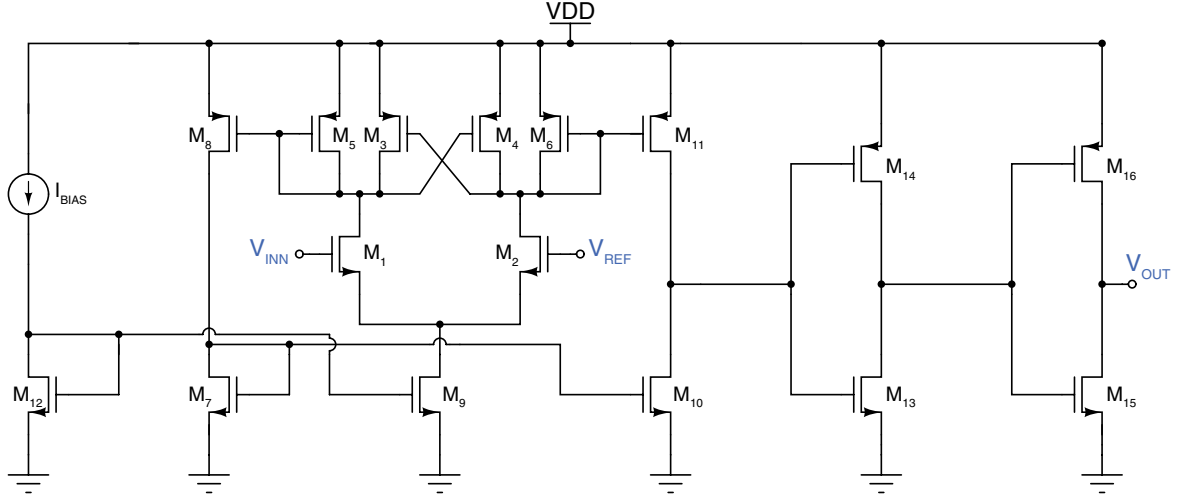


Figure 4.16: Circuit diagram of voltage comparator serving as asynchronous clock generator for optimal energy storage.

Table 4.4: Device sizes of the comparator circuit used for ϕ_1 .

Transistor	(W/L)	Transistor	(W/L)
$M_{1,2}$	(28.4 μ m/350nm)	M_9	2.03 μ m/350nm
$M_{3,4,5,6}$	(580nm/350nm)	M_{12}	9.5 μ m/3 μ m
$M_{7,10}$	735nm/350nm	$M_{13,15}$	350nm/350nm
$M_{8,11}$	1.28 μ m/350nm	$M_{14,16}$	300nm/300nm

Zero-Current Detector

Fig. 4.17 shows a voltage comparator with a differential common-gate input stage. Based on the differential inputs, the cross-coupled $M_{8,9}$ along with the output buffers help in achieving a comparison decision. As explained earlier (Fig. 4.13), this circuit is used as a zero-current detector to terminate ϕ_2 in the buck/boost power converter operation by comparing V_{S1} node with respect to GND. It is worth mentioning that M_1 and M_2 need to be thick-oxide transistors, as V_{S1} could increase proportional to the output voltage during ϕ_1 . In the shown circuit, ϕ_{2EN} is used to turn-OFF the top PMOS transistors, which prevent current flow in the comparator and results in a power-gated operation that is useful for reducing its power consumption. When $\phi_{2EN} = V_{DD}$, the current in M_5 (if GND connected to VINP) would be fixed and the current flowing in $M_{1,6}$ is V_{S1} dependent. As this current reduces with increase in V_{S1} (implying inductor discharge into the load side), the cross-coupled connection between $M_{8,9}$ help in turning OFF M_9 , which results in low-to-high transition at the output. To achieve a higher detection speed and prevent reverse current in the power converter, intentional offset is introduced by having device size mis-match between the input differential pair [142]. Table 4.5 details the designed sizing of this circuit.

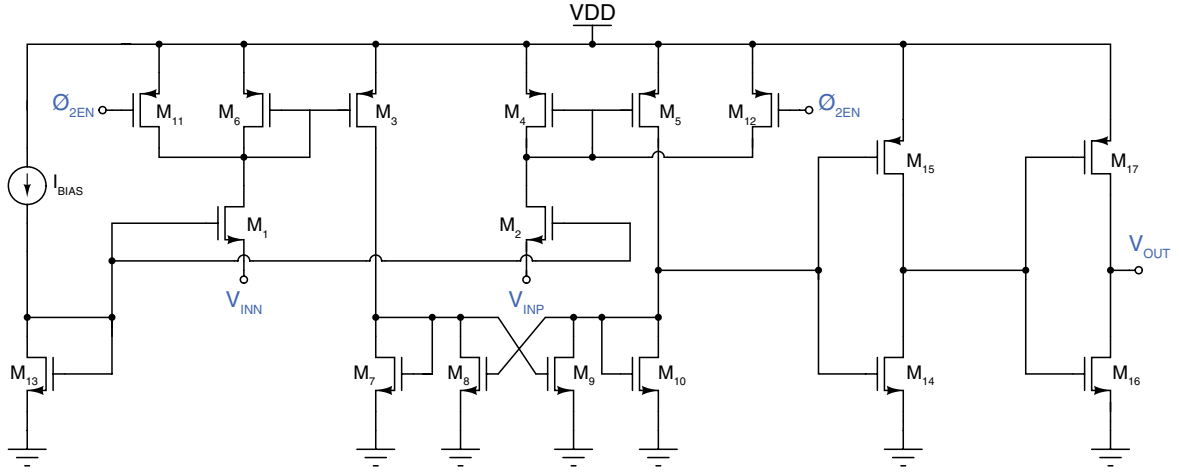


Figure 4.17: Circuit diagram of zero current detector to terminate ϕ_2 in buck/boost power converter.

Table 4.5: Device sizes of the comparator circuit (zero-current detector) used for ϕ_2 .

Transistor	(W/L)	Transistor	(W/L)
M_1	(9.5 μ m/3 μ m)	M_2	(9.75 μ m/3 μ m)
$M_{3,4,5,6}$	(1 μ m/1 μ m)	$M_{7,8,9,10}$	(350nm/3 μ m)
$M_{11,12}$	(220nm/200nm)	M_{13}	(9.5 μ m/3 μ m)
M_{14}	(1.32 μ m/200nm)	M_{15}	(440nm/200nm)
M_{16}	(220nm/200nm)	M_{17}	(660nm/200nm)

Switched-Capacitor Voltage Doubler and Bootstrap Circuit

For a battery-less system with single supply operation, it is essential to generate a higher voltage level than the system's operating voltage to properly control the intended MOS switch operations in the power converter. To do so, an integrated switched-capacitor circuit is used to achieve a higher voltage level in the system (V_{DDH}). As shown in Fig. 4.18(a), three PMOS and one NMOS transistors along with two integrated 100 pF capacitors are utilized for this circuit. During its two-phase operation, C_1 is first charged to V_{DDL} by closing M_1 and M_3 transistors in the first phase. In the second phase, the charged C_1 is placed in series with V_{DDL} by closing M_2 and M_4 to achieve V_{DDH} . Non-overlap clocks with slight delays are needed to properly control the switches operation. Furthermore, dynamic body-biasing circuits with PMOS transistors, as shown in Fig. 4.18(b), are used to appropriately connect the bulk of M_1 (highest potential between V_M and V_{DDL}) and M_4 (highest potential between V_M and V_{DDH}), preventing leakage currents through their bulks. As M_2 and M_3 are not exposed to V_{DDH} , their bodies are tied to V_{DDL} and GND, respectively. Moreover, controlling signals with higher voltage levels are essential at the gates of M_1 and M_4 for properly turning them OFF and ON, respectively, during the second phase of operation. To achieve this, the bootstrap circuit shown in Fig. 4.18(c) with two integrated 10 pF capacitors is utilized [146]. Table 4.6 summarizes the transistor sizes of these circuits.

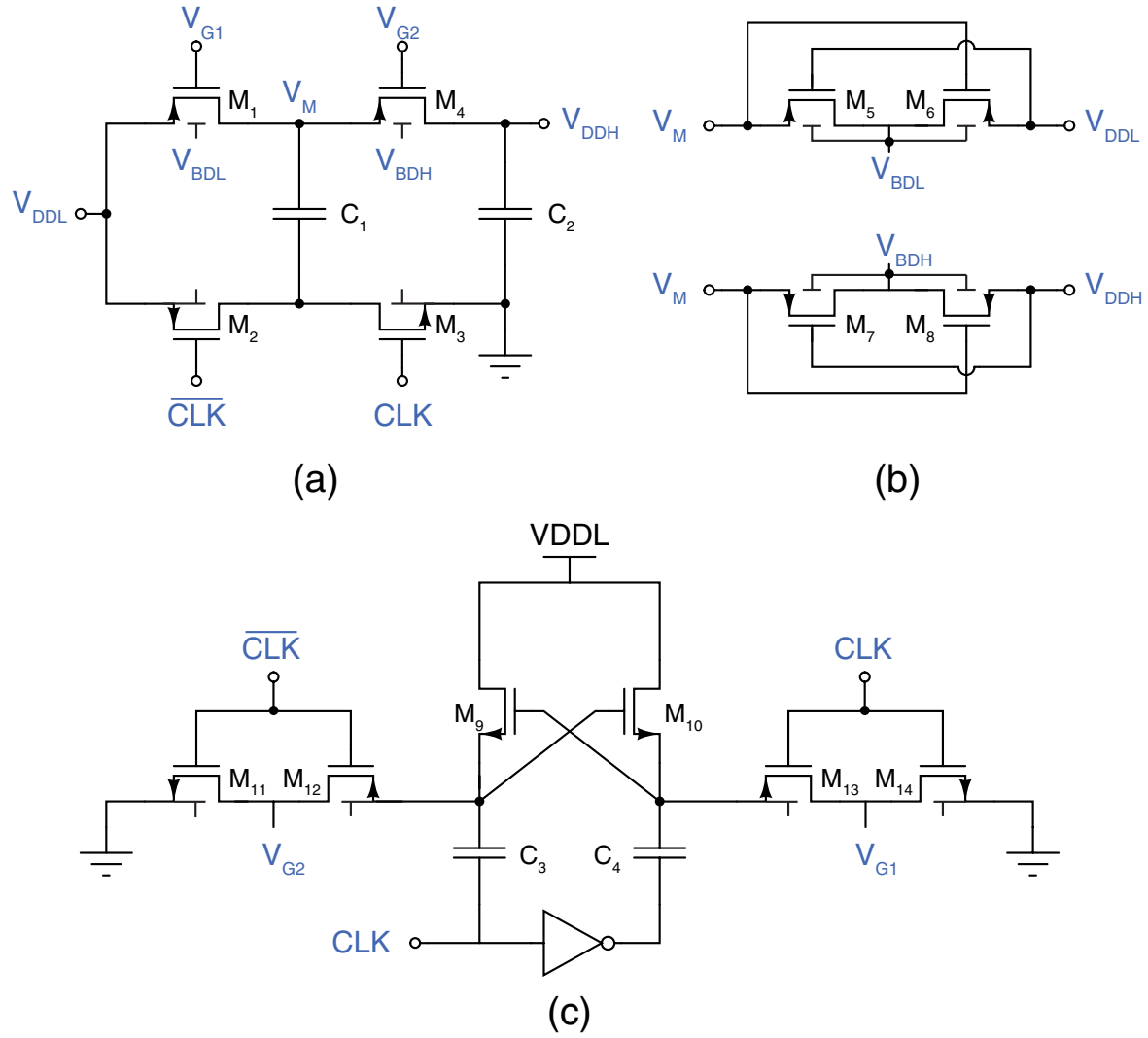


Figure 4.18: Circuit diagram of (a) switch-capacitor voltage doubler, (b) used PMOS dynamic biasing, and (c) bootstrap used for proper controlling [146].

Table 4.6: Device sizes of the integrated switch-capacitor voltage doubler and bootstrap circuit.

Transistor	$(W/L) \times f$	Transistor	$(W/L) \times f$
$M_{1,2,4}$	$(2\mu\text{m}/300\text{nm}) \times 15$	M_3	$(2\mu\text{m}/350\text{nm}) \times 10$
$M_{5,6,7,8}$	$(2\mu\text{m}/300\text{nm}) \times 5$	$M_{9,10}$	$(2\mu\text{m}/350\text{nm}) \times 1$
$M_{11,14}$	$(2\mu\text{m}/350\text{nm}) \times 1$	$M_{12,13}$	$(2\mu\text{m}/300\text{nm}) \times 1$

Voltage Regulator and Multi-Reference Voltage Generator

Low-dropout voltage regulator with PMOS switch similar to [147] is designed and integrated in this chip as well (Fig. 4.19). The PMOS regulator $((W/L_{(M1)}) \times f = (50\mu\text{m}/300\text{nm}) \times 10)$, is preferred over its NMOS counterpart due to its lower voltage drop and being needless of charge pump circuitry for its gate driving. The regulator's stability is achieved by adding Miller RC feedback frequency compensation network between the output nodes of the op-amp and the voltage regulator [148, 149].

To achieve multi-level reference voltages (V_{REF}), the shown circuit in Fig. 4.20 which was proposed in [150] and [151] and converts the V_{GS} -reference current into supply-independent voltage references is used. As each circuit is capable of generating four different reference voltages, two circuits with different V_{DDL} and V_{DDH} supplies are used to cover higher voltage ranges. As a clear signal is essential for resetting the digital controller in the calibration block, a single NMOS switch is used as the power-ON-reset (POR) circuitry in the reference generators

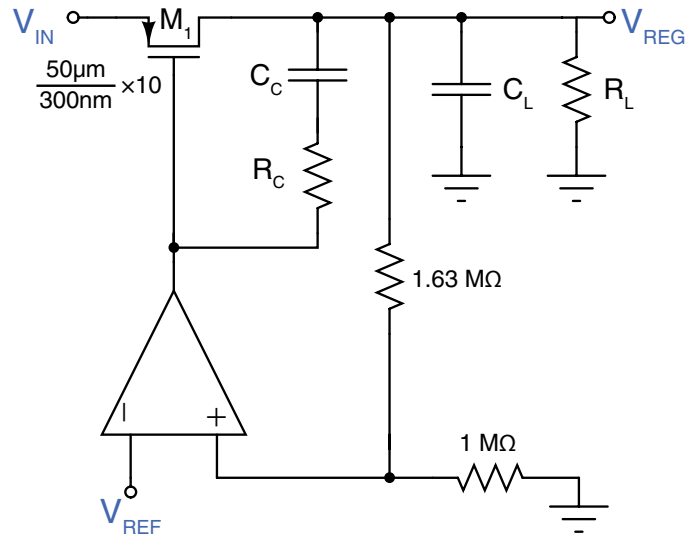


Figure 4.19: Circuit diagram of voltage regulator with PMOS device.

for this design. Table 4.7 summarizes the size of transistors for the two mentioned circuits.

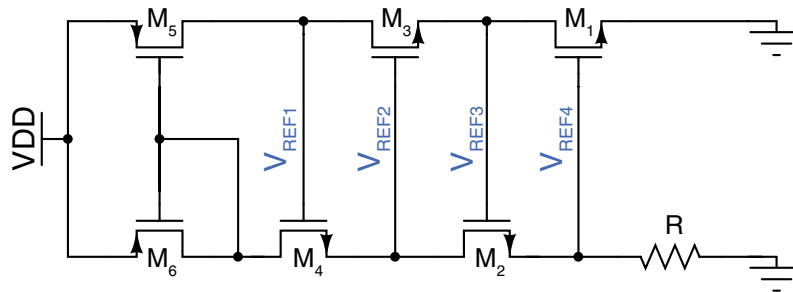


Figure 4.20: Circuit diagram of multi-reference voltage generator [150].

Table 4.7: Device sizes of the two multi-reference voltage generators.

Transistor	$(W/L)_{Circuit1}$	$(W/L)_{Circuit2}$
M_1	(500nm/20 μ m)	(1.25 μ m/20 μ m)
M_2	(560nm/20 μ m)	(35.54 μ m/10 μ m) $\times 4$
M_3	(620nm/20 μ m)	(2.8 μ m/20 μ m)
M_4	(1.55 μ m/20 μ m)	(1.74 μ m/20 μ m)
$M_{5,6}$	(168.4 μ m/10 μ m)	(39.25 μ m/10 μ m)

4.4 Measurement Results

In order to verify the energy storage optimization approach outlined for VM receivers, an inductive link (depicted in Fig. 4.21) was designed and fabricated. It should be mentioned that the presented approach for optimizing the energy storage in VM receivers is developed to work with any inductive link and the presented link only serves as an example. The Tx and Rx coils dimensions were set for a visual prosthesis application [152], with the Tx and Rx positioned at 1.5 cm apart. The extracted parameters of the implemented link along with the physical dimensions of the wire-wounded coils are provided in Table 4.8. It is worth mentioning that a parallel resonance tank at the primary was realized for a better impedance matching with the 50 Ω source impedance.



Figure 4.21: Implemented inductive link with wire-wounded coils for visual prosthesis application.

Table 4.8: Implemented inductive link parameters for validation of energy storage optimization in VM receivers.

Circuit Parameters	VM Inductive Link	Physical Parameters	Dimension
f_o (MHz)	1	L_1 Wire Diameter (mm)	1.024 (18 AWG)
L_1/L_2 (μ H)	2.86/1.52	L_2 Wire Diameter (mm)	0.404 (26 AWG)
R_1/R_2 (Ω)	1.811/0.326	L_1 Diameter (mm)	60
C_1/C_2 (nF)	8.00/15.68	L_2 Diameter (mm)	25
k_{12}	0.085	N_1/N_2 Turns	5/6

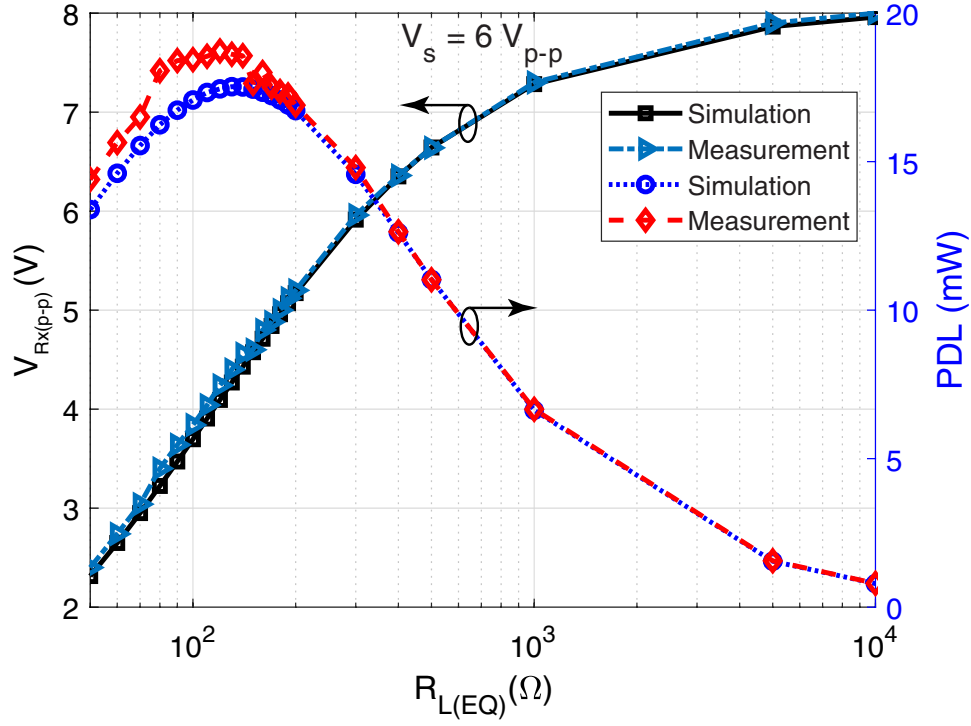


Figure 4.22: Measured versus simulated V_{Rx} and PDL, both versus $R_{L(EQ)}$ for the implemented inductive link for $V_s = 6 V_{p-p}$.

4.4.1 Inductive Link Characterization

The implemented inductive link was characterized by sweeping $R_{L(EQ)}$ connected across the receiver's L_2C_2 tank, as shown in Fig. 4.1(b). Furthermore, the circuit was simulated in Cadence using the extracted circuit parameters in Table 4.8. Fig. 4.22 shows the simulated versus measured peak-to-peak voltage across the receiver ($V_{Rx(p-p)}$) in addition to the PDL, calculated using $PDL = 0.5 \times (0.5 \times V_{Rx(p-p)})^2 / R_{L(EQ)}$, when the source voltage V_s at the Tx was set to $6 V_{p-p}$. As shown, the measured values closely match the simulated results, both confirming $R_{L(opt)}$ to be

between 120 - 130 Ω range. Fig. 4.23 and 4.24 show the same results when Tx was excited with $V_s = 3 - 10 V_{p-p}$ range. As expected, $R_{L(opt)}$ is constant for the inductive link, while $V_{Rx(opt)}$ varies according to the V_s magnitude, implying higher maximum possible PDL at the Rx.

4.4.2 Verification of the Optimal Energy Storage Scheme

After inductive link's characterization, the proposed energy storage scheme was verified. Fig. 4.25 shows the measurement setup and its associated block diagram. The setup consists of the inductive link along with a half-wave rectifier, a buck converter used for C_{STG} charging, and the presented IC. The on-chip comparator and S_1 switch were used for the following measurements. Furthermore, a snubber circuit was added across the diode (D_2) to reduce voltage ringings as much as possible. In addition, a function generator was employed to generate the V_{CLEAR} signal, which was used to periodically discharge C_{STG} through the additional switch placed in parallel and after the specified charging interval.

For the verification purpose, V_{REF} was swept to maintain the voltage across Rx at different voltage levels. Accordingly, the charging of C_{STG} was monitored for each case to indicate the optimal V_{REF} , which results in maximum P_{STG} . Fig. 4.26 shows the measured V_{STG} snapshot for $V_s = 6 V_{p-p}$, $V_{REF} = 1.4$ V, and $C_L = 1.1$ mF. As 0.96 V was used as the minimum V_{REF} , C_{STG} charging was monitored until V_{STG} reached 0.96 V to have a fair comparison of different V_{REF} values. Therefore, the comparison was to see how fast the same amount of energy

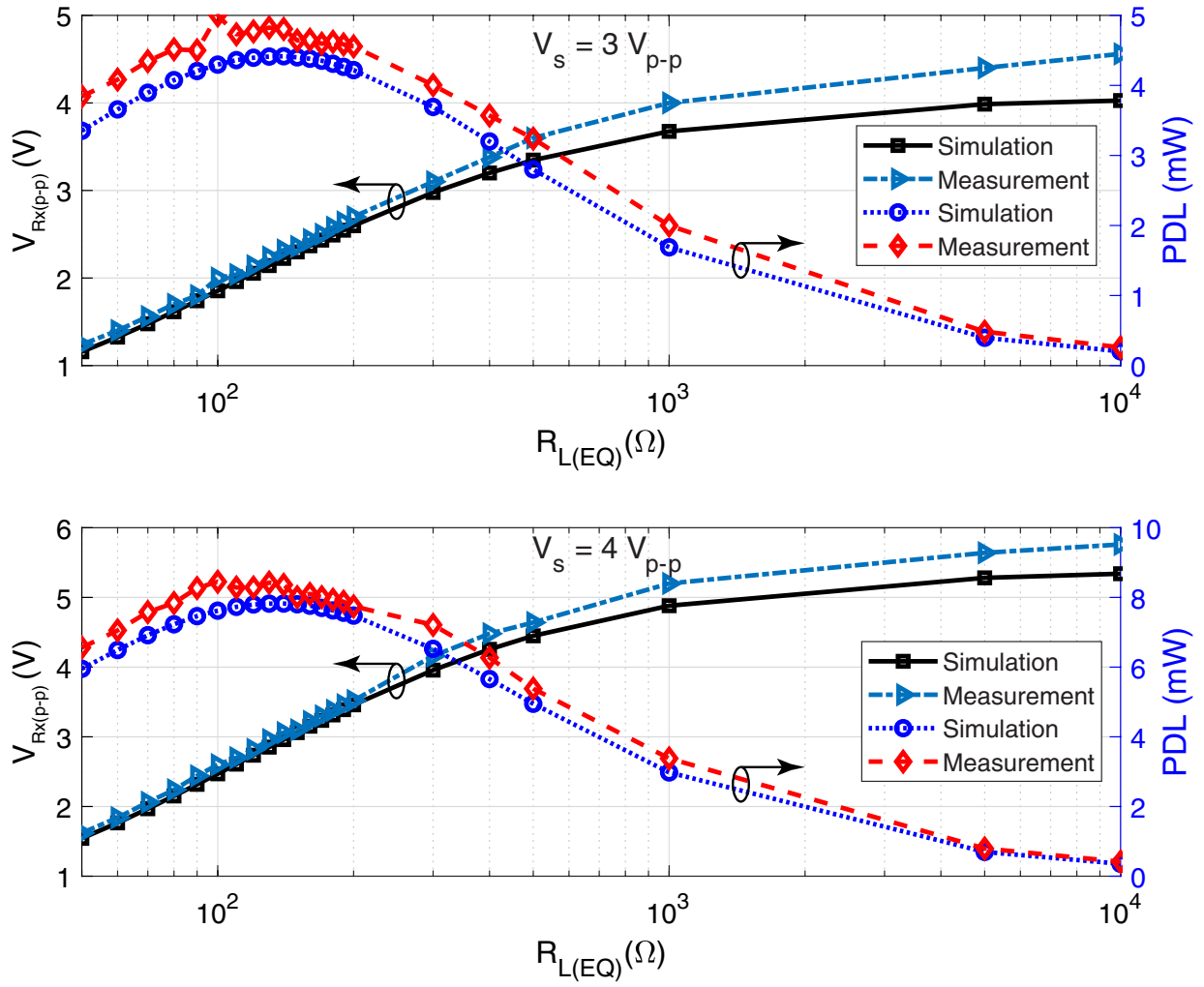


Figure 4.23: Measured versus simulated V_{R_x} and PDL, both versus $R_{L(EQ)}$ for the implemented inductive link for $V_s = 3 V_{p-p}$ and $V_s = 4 V_{p-p}$.

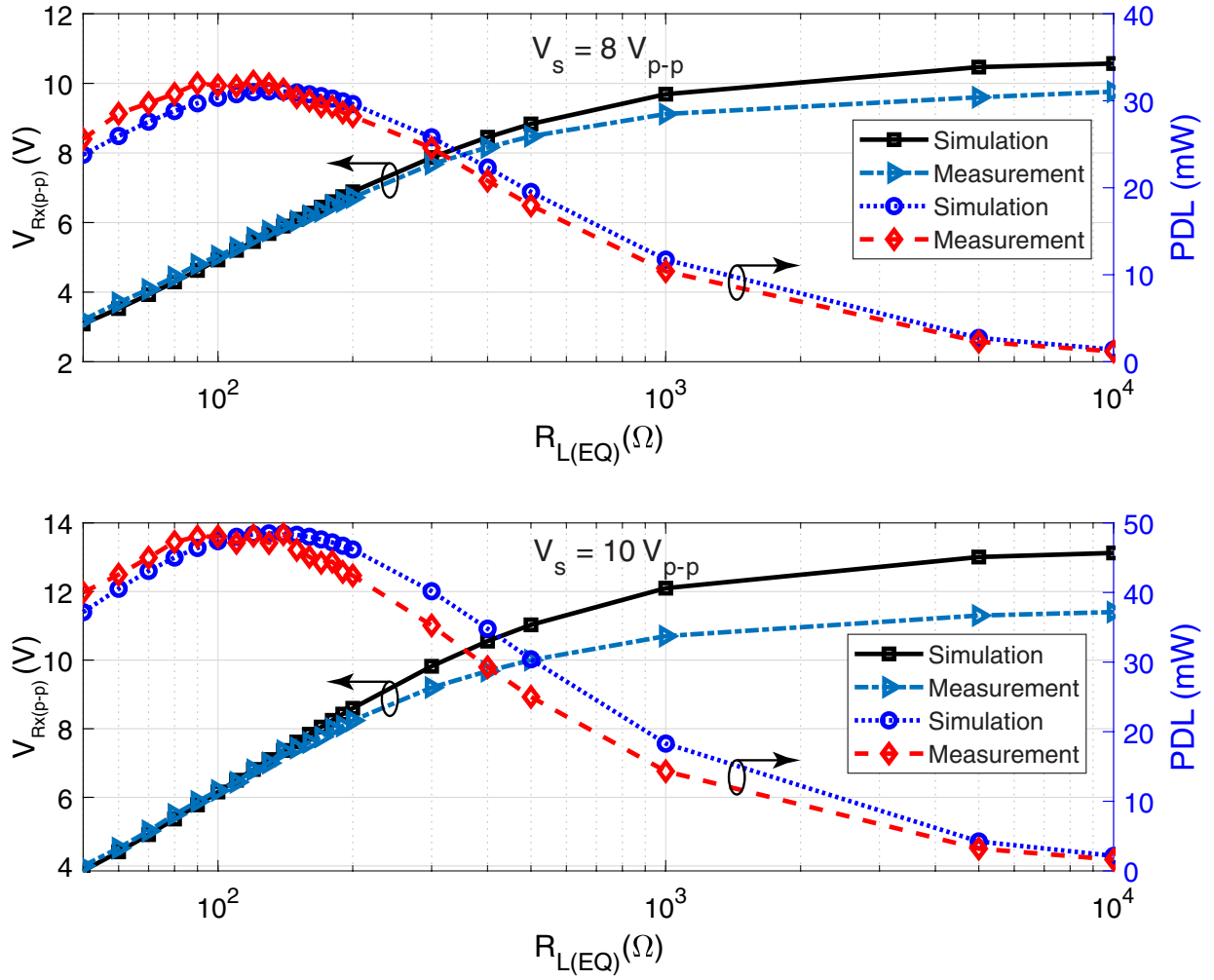


Figure 4.24: Measured versus simulated V_{Rx} and PDL, both versus $R_{L(EQ)}$ for the implemented inductive link for $V_s = 8 V_{p-p}$ and $V_s = 10 V_{p-p}$.

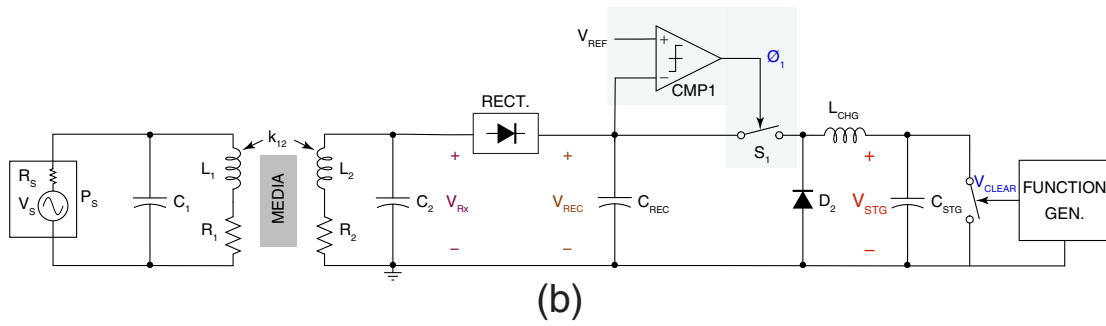
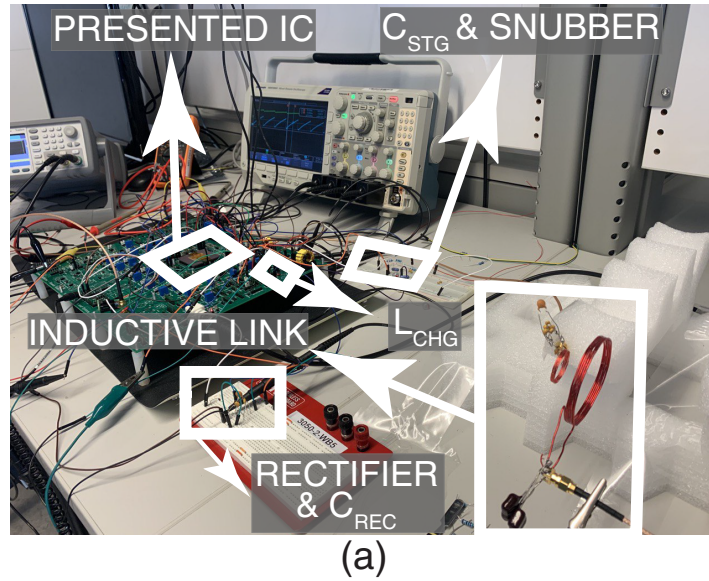


Figure 4.25: (a) Measurement setup for energy storage optimization in VM receivers, and (b) its associated block diagram.

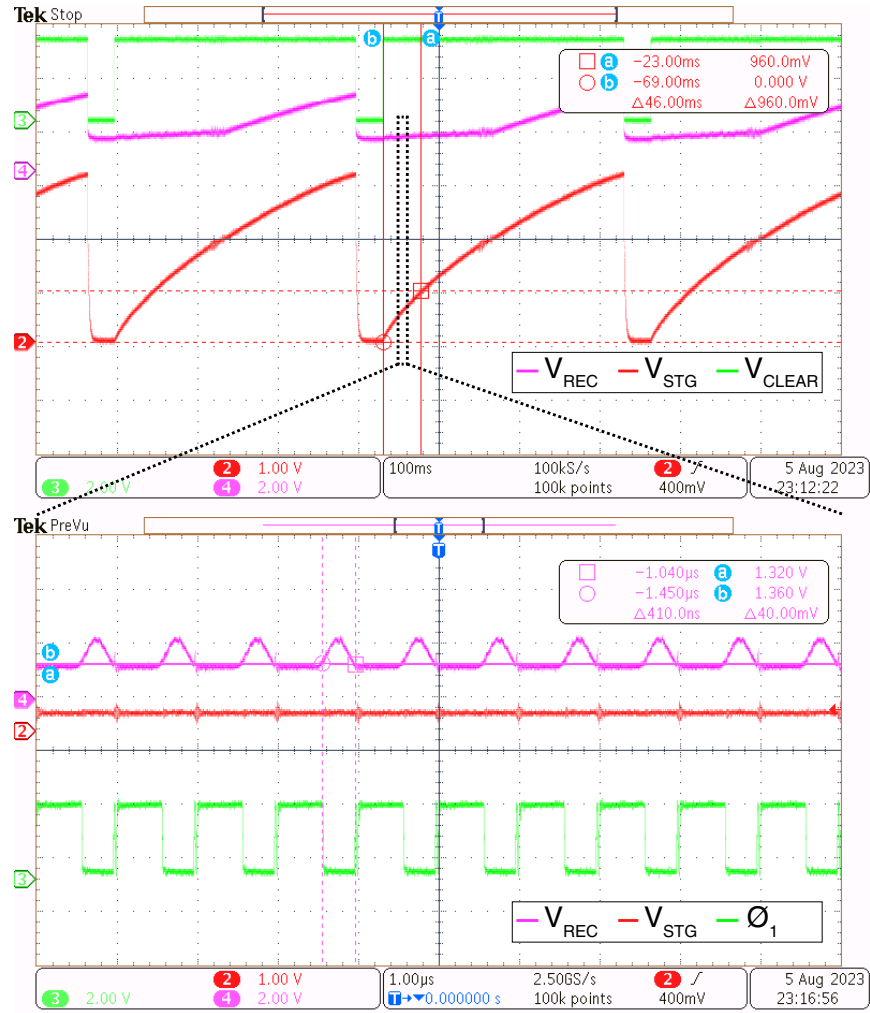


Figure 4.26: Measured V_{STG} for $V_s = 6 V_{p-p}$, $V_{REF} = 1.4 V$, and $C_{STG} = 1.1 mF$.

($E_{STG} = 0.5C_{STG}V_{STG}^2$) could be stored for different V_{REF} values. The charging duration t_{CHG} is indicated by the cursors in the oscilloscope snapshot in Fig. 4.26 (top). The scope's snapshot in Fig. 4.26 (bottom) shows the annotated zoomed-in window, where the cursors show that the comparator, i.e., CMP1 in Fig. 4.25(b), indicates ϕ_1 (the green signal) such that C_{STG} charging is performed when V_{REC} increases above $V_{REF} = 1.4$ V at each resonance cycle. Fig. 4.27 shows the same measurements for $V_s = 4 V_{p-p}$, $V_{REF} = 1$ V, and $C_L = 1.1$ mF, verifying that sufficient amount of current was drawn from the L_2C_2 tank for storage, such that V_{REC} remained close to V_{REF} and was prevented from additional rise during the intended energy storage period (i.e., $0 < V_{STG} \leq 0.96$ V).

Fig. 4.28(a) shows the superimposed measured V_{STG} for different V_{REF} while Fig. 4.28(b) shows the measured t_{CHG} and the calculated $P_{STG} = E_{STG}/t_{CHG}$ versus V_{REF} . As the results show, V_{STG} reaches the targeted fixed voltage (i.e., 0.96 V) faster when V_{REF} is between 1.4 V and 1.6 V, indicating a higher PDL and a higher charging efficiency for these cases.

For further validation, the same experiments were performed while V_s at Tx was swept between 3–10 V_{p-p} . Fig. 4.29(a) and (b) show the measured V_{STG} for $V_s = 4 V_{p-p}$ and $V_s = 10 V_{p-p}$, respectively. Fig. 4.30 and 4.31 show the measured t_{CHG} and the calculated P_{STG} versus V_{REF} for each V_s value. It is worth mentioning that $C_{STG} = 2.1$ mF was used at higher P_s (i.e., $V_s = 8 - 10 V_{p-p}$) to have longer t_{CHG} duration for a better measurements reliability. As expected, the optimal V_{REF} , which results in the highest P_{STG} , varies according to the V_s value,

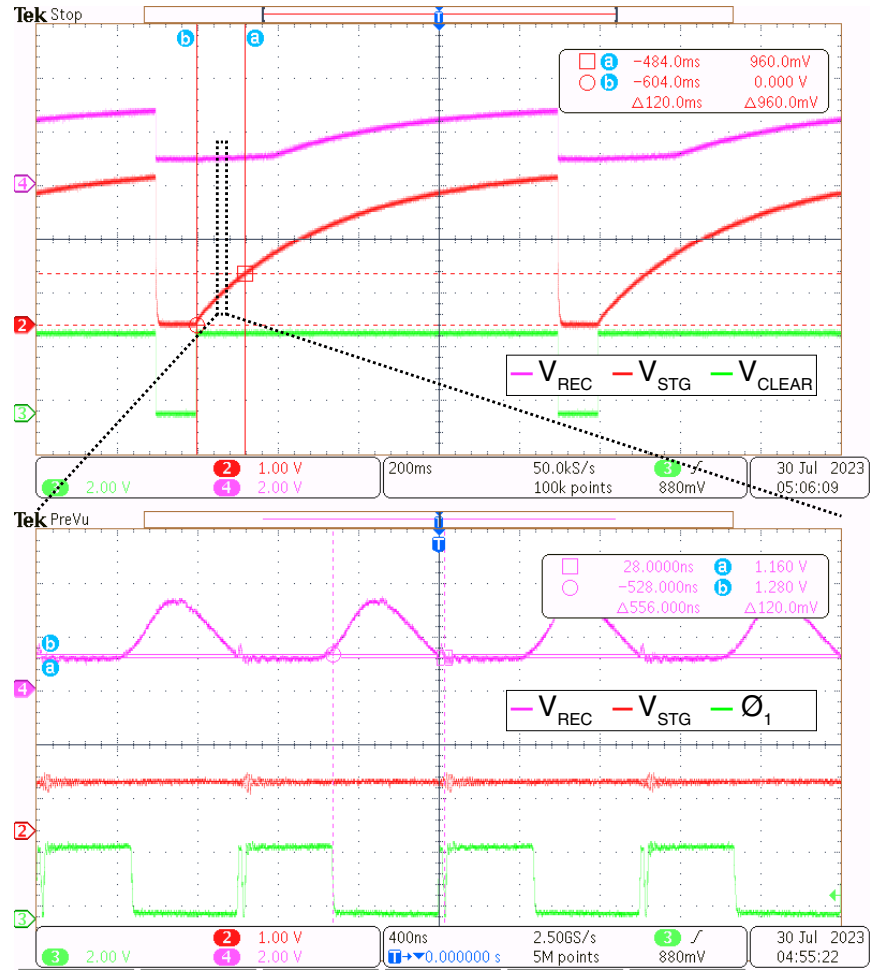


Figure 4.27: Measured V_{STG} for $V_s = 4 V_{p-p}$, $V_{REF} = 1$ V, and $C_{STG} = 1.1$ mF.

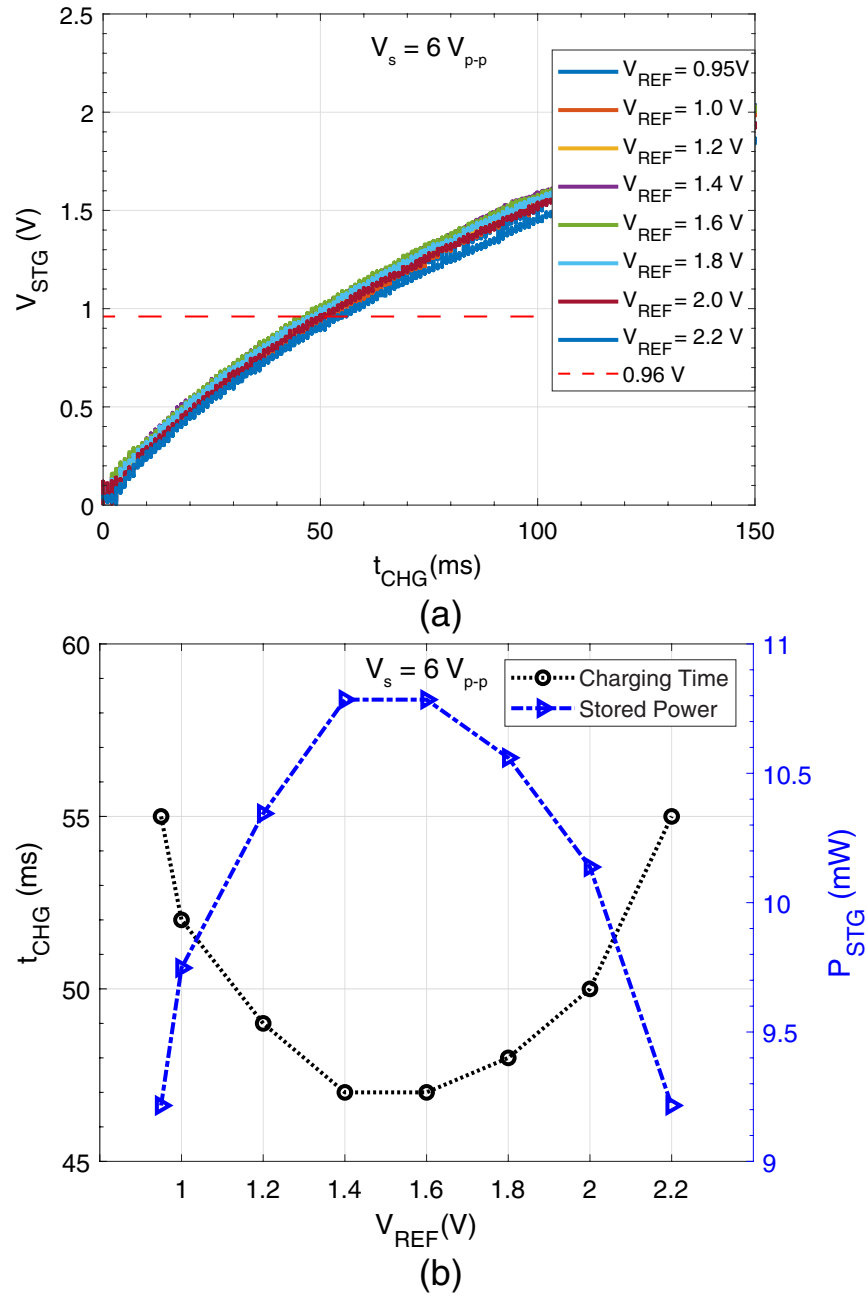


Figure 4.28: Measured (a) overall charging slope for different V_{REF} , and (b) t_{CHG} and P_{STG} versus V_{REF} for $V_s = 6 V_{p-p}$.

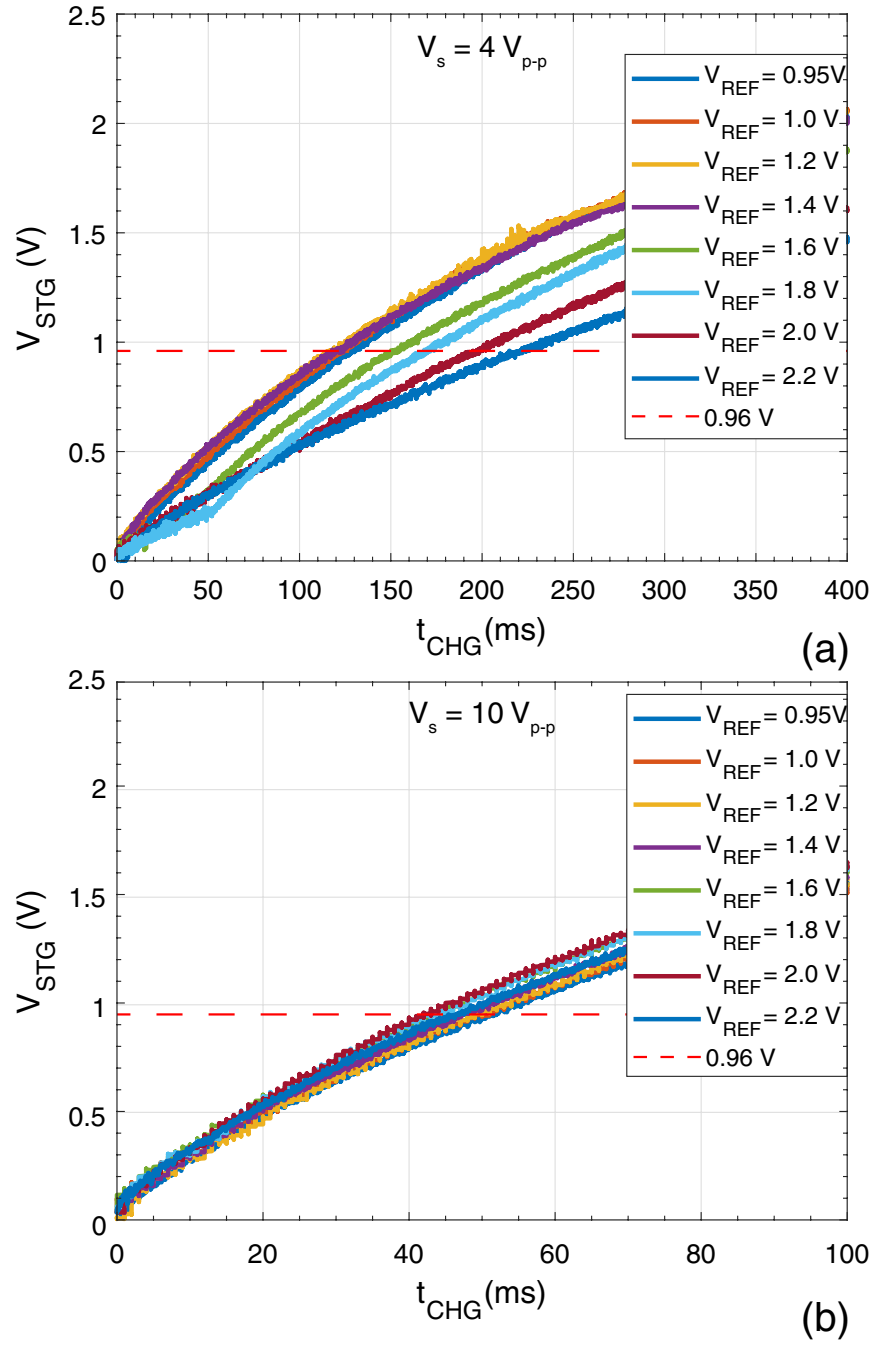


Figure 4.29: Measured V_{STG} versus V_{REF} for (a) $V_s = 4 V_{p-p}$, and (b) $V_s = 10 V_{p-p}$.

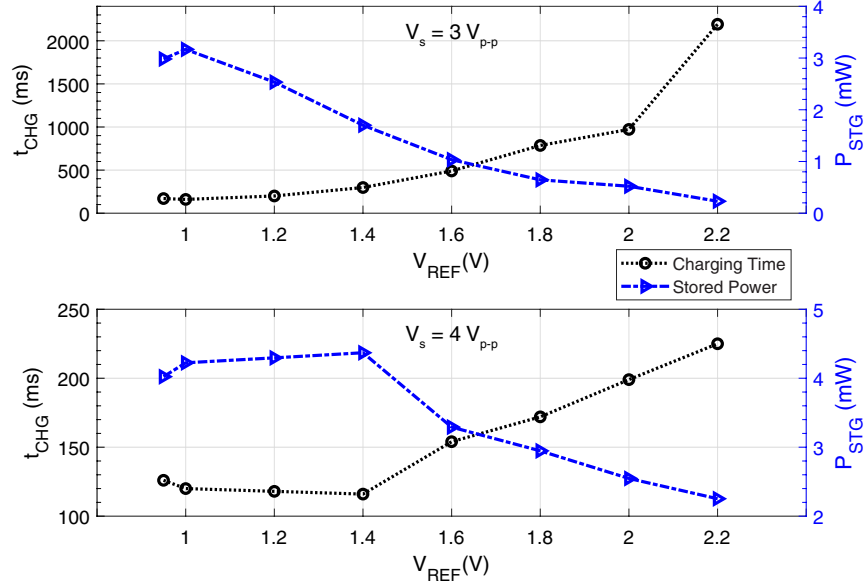


Figure 4.30: Measured t_{CHG} and P_{STG} versus V_{REF} for (a) $V_s = 3 V_{p-p}$, and (b) $V_s = 4 V_{p-p}$.

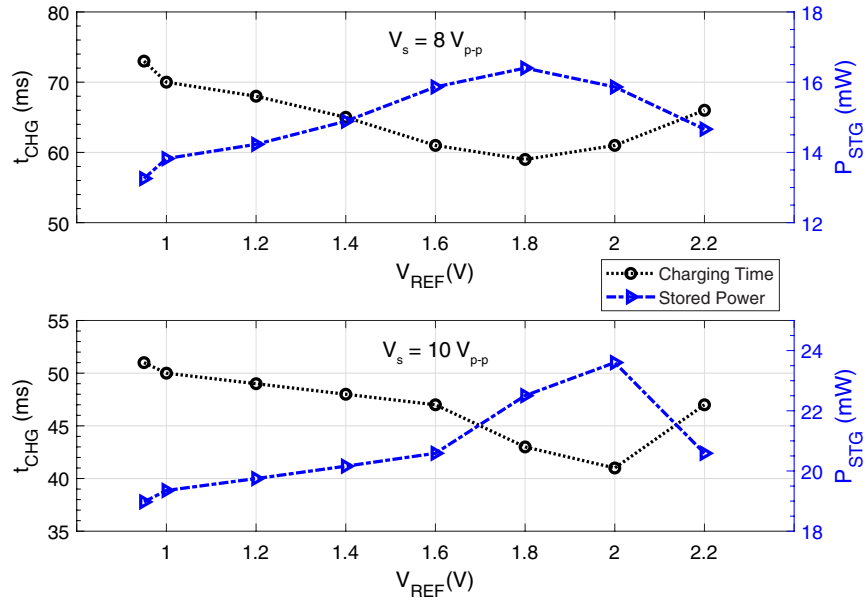


Figure 4.31: Measured t_{CHG} and P_{STG} versus V_{REF} for (a) $V_s = 8 V_{p-p}$, and (b) $V_s = 10 V_{p-p}$.

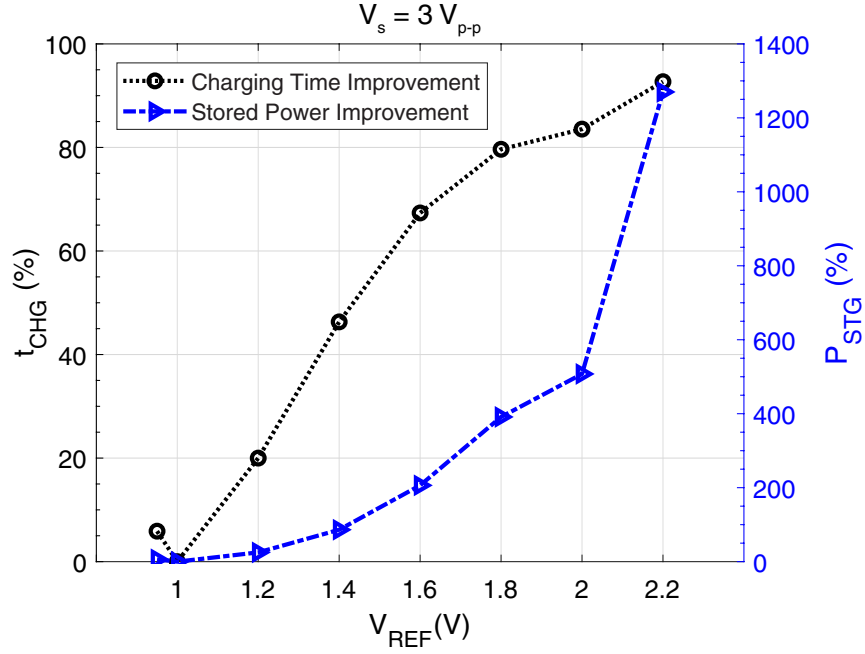


Figure 4.32: Percentage improvements of the charging time and stored power at each V_{REF} compared to their optimal values at $V_{REF} = 1$ V, i.e., achieved minimum t_{CHG} and maximum P_{STG} , for $V_s = 3 V_{p-p}$.

indicating the optimal R_L for each input power.

Fig. 4.32 illustrates the percentage enhancements of t_{CHG} and P_{STG} for $V_s = 3 V_{p-p}$ at each V_{REF} compared to their optimal values (i.e., minimum t_{CHG} and maximum P_{STG}), which is $V_{REF} = 1$ V for this particular case. It is worth noting that there are no improvements (0% improvements) at $V_{REF} = 1$ V, which serves as an indicator of the optimal point. The graph shows that the smallest improvement occurs at $V_{REF} = 0.95$ V, with improvements of 5.88% for t_{CHG} and 6.25% for P_{STG} . This is because this point is in the close proximity of $V_{Rx(opt)}$. Conversely, the most substantial improvement is observed for $V_{REF} = 2.2$ V, boasting significant improve-

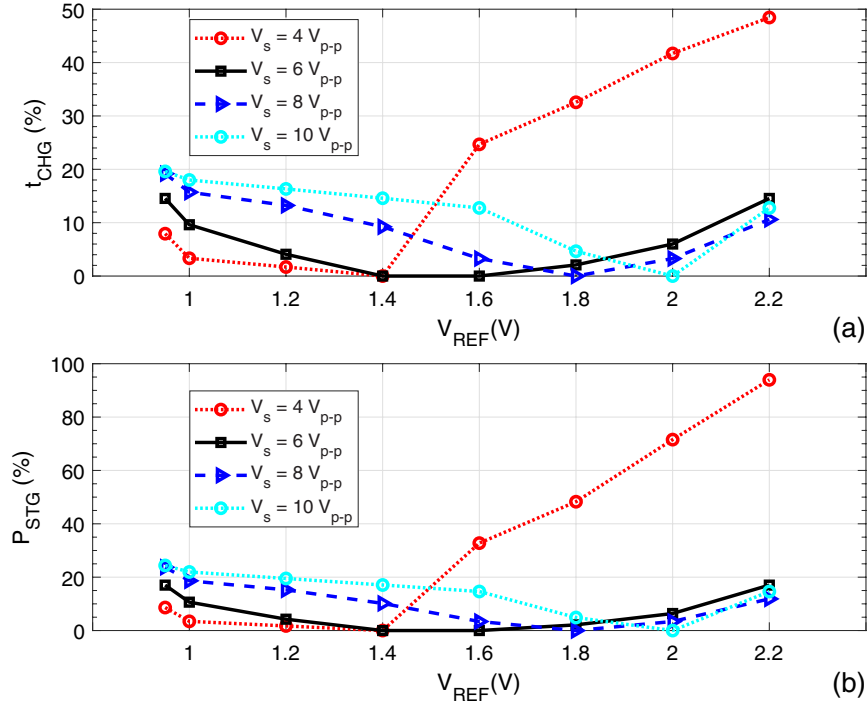


Figure 4.33: Percentage improvements of (a) charging time (t_{CHG}), and (b) stored power (P_{STG}), at each V_{REF} for different V_s values, both compared to their respective achieved optimal values (i.e., minimum t_{CHG} and maximum P_{STG}) using the proposed optimization scheme.

ments of 92.70% and 1270% for t_{CHG} and P_{STG} , respectively. This improvement is remarkable due to the notable deviation of V_{REF} from its optimal condition, which significantly degrades the overall link's energy storage efficiency and increases the charging time accordingly.

Fig. 4.33(a) and (b) show the percentage improvements of t_{CHG} and P_{STG} at each V_{REF} , respectively, compared to their achieved optimal values (i.e., minimum t_{CHG} and maximum P_{STG}) using the proposed optimization scheme for $V_s = 4\text{--}10$ V_{p-p} range. These improvements are compared to the corresponding achieved optimal values in each scenario, linked with 0% im-

provements in the graph. For $V_s = 4 V_{p-p}$, the smallest improvement occurs at $V_{REF} = 1.2$ V, with improvements of 1.69% for t_{CHG} and 1.72% for P_{STG} , while the highest improvements occur for $V_{REF} = 2.2$ V, with improvements of 48.44% for t_{CHG} and 93.97% for P_{STG} . For $V_s = 6 V_{p-p}$, the least improvement occurs at $V_{REF} = 1.8$ V, with improvements of 2.08% for t_{CHG} and 2.13% for P_{STG} , while the highest improvements occur for both $V_{REF} = 0.95$ V and 2.2 V, with improvements of 14.55% for t_{CHG} and 17.02% for P_{STG} . For $V_s = 8 V_{p-p}$, the least improvement occurs at $V_{REF} = 1.6$ V and 2 V, with improvements of 3.28% for t_{CHG} and 3.39% for P_{STG} , while the highest improvements occur for $V_{REF} = 0.95$ V, with improvements of 19.18% for t_{CHG} and 23.73% for P_{STG} . Finally, for $V_s = 10 V_{p-p}$, the least improvement occurs at $V_{REF} = 1.8$ V, with improvements of 4.65% for t_{CHG} and 4.88% for P_{STG} , while the highest improvements occur compared to $V_{REF} = 0.95$ V, with improvements of 19.61% for t_{CHG} and 24.39% for P_{STG} .

Based on these results, it can be concluded that maintaining a consistent $V_{Rx(opt)}$ across Rx is more advantageous at higher input powers. This is particularly relevant because, in such cases, the range of maximum P_{Rx} becomes narrower compared to deviations in V_{REF} . This relationship is further illustrated in Fig. 4.34, where the percentage improvements of the achieved optimal t_{CHG} and P_{STG} with respect to V_s are presented compared to their respective non-optimal values at $V_{REF} = 0.95$ V. The choice of this voltage for comparison is motivated by its association with the lowest power loss in the buck converter, making it a suitable choice for this analysis.

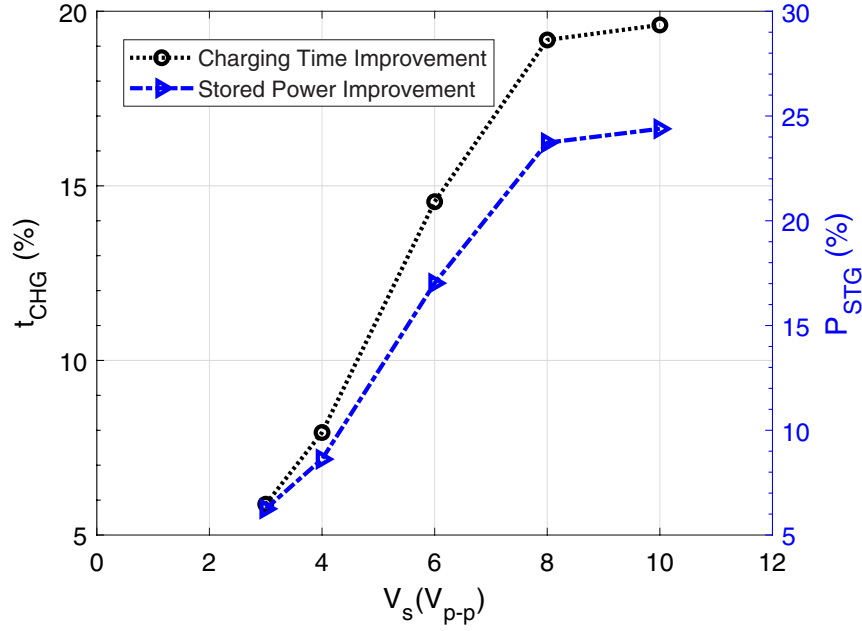


Figure 4.34: Percentage improvements of the achieved optimal t_{CHG} and P_{STG} , both versus V_s compared to their respective values at $V_{REF} = 0.95$ V.

4.4.3 Optimal Energy Storage versus Rx Loading

To verify the efficacy of the presented energy storage optimization scheme under varying Rx loading, we introduced additional load conditions to the rectifier in Fig. 4.25. This entailed loading the rectifier with a 1.2 V voltage regulator (featuring a 0.085 drop-out voltage) along with different R_L values to manipulate PDL at a regulated load voltage ($V_{L(REG)}$). Concurrently, we charged $C_{STG} = 2.1$ mF using the same buck converter in Fig. 4.25 with employing different V_{REF} values across the Rx using CMP1, as described in the previous subsection.

Fig 4.35 depicts oscilloscope snapshots for the mentioned scenarios while powering different regulating R_L values. These snapshots are associated with $V_s = 10 V_{p-p}$ and $V_{REF} = 1.8$ V,

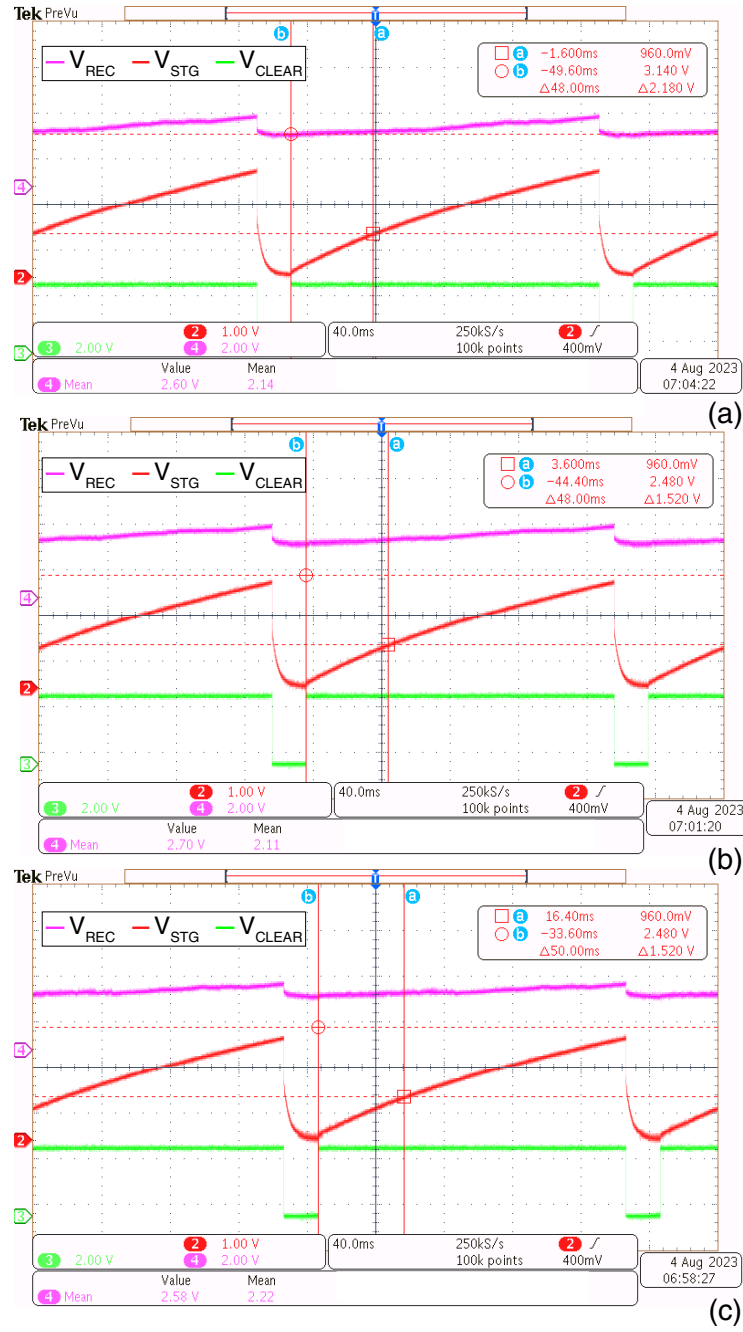


Figure 4.35: Measured V_{STG} for $V_s = 10 V_{p-p}$, $V_{REF} = 1.8 V$, $C_{STG} = 2.1 mF$, and $V_{L(REG)} = 1.2 V$ with: (a) $R_L = 10 k\Omega$, (a) $R_L = 5 k\Omega$, (a) $R_L = 1 k\Omega$.

corresponding to $R_L = 10\text{ k}\Omega$, $5\text{ k}\Omega$, and $1\text{ k}\Omega$, for (a), (b), and (c), respectively, with a 1.2 V regulated voltage and while simultaneously storing the surplus energy in $C_{STG} = 2.1\text{ mF}$. The measurements validate that, regardless of Rx loading, the increase of V_{REC} was prevented through the utilization of CMP1 and the storage pathway, while V_{REC} and V_{STG} are successfully isolated. Furthermore, the cursors highlight that t_{CHG} for an equivalent stored amount of energy increases proportionally to the PDL, indicating reduced surplus energy available for storage.

Fig. 4.36 and 4.37 show the measurement results for t_{CHG} and P_{STG} with $V_s = 8\text{ V}_{p-p}$ and $V_s = 10\text{ V}_{p-p}$, respectively. As evidenced by the results, the longer t_{CHG} and reduction in P_{STG} correlate with both the PDL and the power dissipation across the regulator, particularly under higher load currents (specifically, $R_L = 1\text{ k}\Omega$). Conversely, when the PDL is at a lower level, as is the case for $R_L = 5\text{ k}\Omega$ and $R_L = 10\text{ k}\Omega$, the P_{STG} values demonstrate a notably close alignment, which verify the regulation of the received power based on the specified V_{REF} . It is important to note that this observation is in line with our expectations and helps confirm the underlying principles of the proposed optimization scheme, in which the excess energy, after the PDL and its associated power delivery losses, effectively gets directed towards the storage element C_{STG} . The results also illustrate that, regardless of the R_L value, the stored power from the surplus energy is greater at the optimal V_{REF} , similar to situations without any R_L . This further validates the effectiveness of the proposed energy optimization scheme for VM receivers, specially at higher input powers. Table 4.9 compares the presented energy optimization scheme

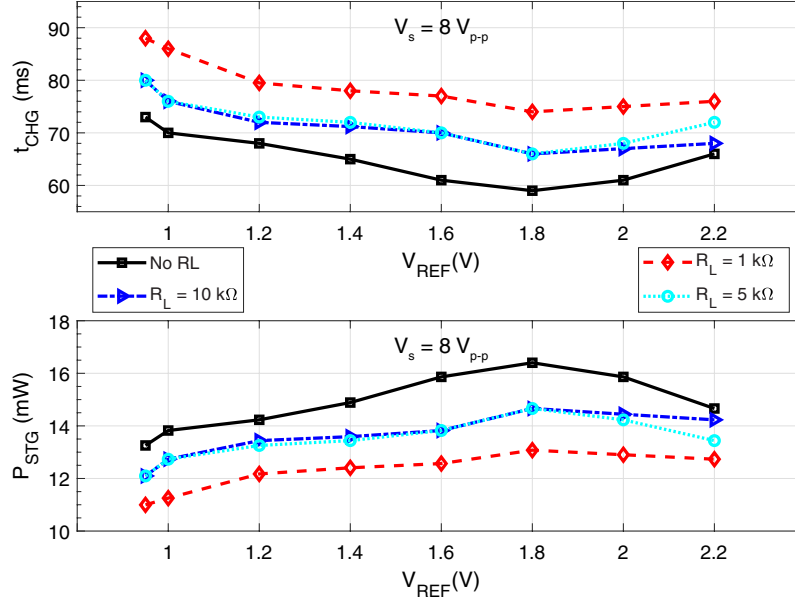


Figure 4.36: Measured (a) t_{CHG} , and (b) P_{STG} , both versus V_{REF} at different regulated R_L for $V_s = 8 V_{p-p}$.

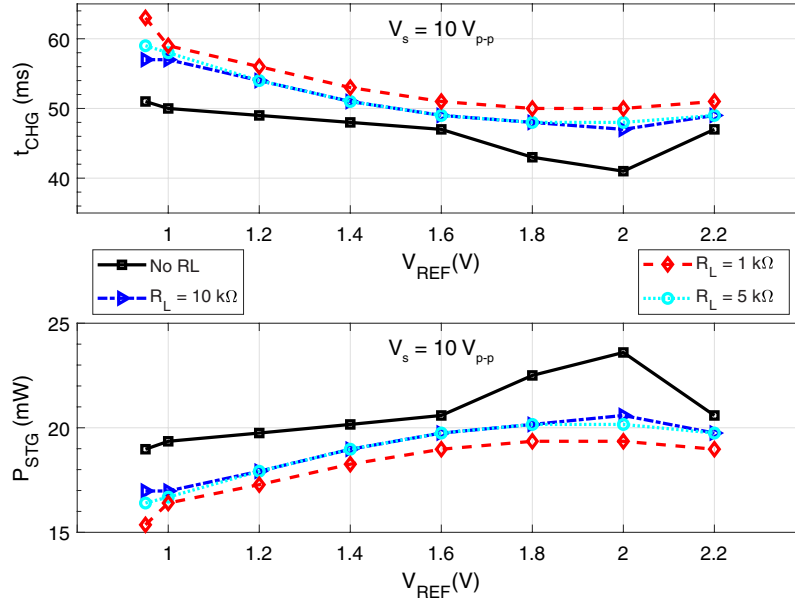


Figure 4.37: Measured (a) t_{CHG} , and (b) P_{STG} , both versus V_{REF} at different regulated R_L for $V_s = 10 V_{p-p}$.

Table 4.9: Comparison of VM energy storage optimization with the state of the art.

	[123]	[92]	[118]	This Work
Rx Architecture	VM	VM	VM	VM
Load Type	Capacitive	Capacitive	Capacitive	Capacitive
Technology (μm)	0.35	0.35	N/A	0.18
frequency (MHz)	2.00	6.78	6.78	1.00
V_{DD} (V)	± 2.1	N/A	4.1	1.8
Rx Coil Size (mm)	10	2.5	3.3	2.5
Tx-Rx Coil Distance (cm)	1.5	0.95	0.6	1.5
V_{CHG} (V)	± 1.0	5.0	1.4	1.0
η_{STG} (%) @ P_{IN}	63 @ 12 mW	95 @ 227.4 mW	52 @ 1.06 W	57.55 @ 18.73 mW
Optimal Loading	No	Yes	No	Yes
Calibration Type	Voltage	Power	N/A	Voltage
Rx LC Tweaking	Yes	Yes	N/A	No
Up-Conversion Capability	No	No	Yes	Yes

with other works in the literature. To the best of our knowledge, the implemented optimization provides a solution that results in continuous optimal loading of the Rx without the need for tweaking its LC tank parameters for the sake of energy storage. Furthermore, it replaces power measurements with simple voltage measurement while providing up-conversion capability.

4.5 Conclusion

In this chapter, we presented the design, development, and characterization of an energy storage optimization scheme for resonant inductive wireless power receivers with VM architecture. Using simulation and measurement results, it is shown that there exists an optimal voltage for the receiver and consequently at the output of the rectifier, which needs to be maintained for maximum power transfer to occur through the wireless link. By detecting and maintaining this optimal voltage, the conduction angle (i.e., the turn-ON period) of the rectifier is automatically set such that the optimal loading occurs both at the receiver as well as its reflected impedance on the transmitter. For the proposed solution, the optimal voltage at the output of the rectifier is continuously maintained at each cycle of the power carrier by isolating the storage capacitor along with its voltage from the receiver's resonating LC tank by the help of a buck/boost power converter stage. This isolation helps in receiving the maximum power while delivering the required continuous power to the resistive load (either directly from the rectifier or the storage element)

and simultaneously directing the surplus energy for storage into the capacitive load.

A detailed system-level and circuit-level implementation of an IC which was fabricated in a standard $0.18\ \mu\text{m}$ CMOS process is also presented. The IC controls the receiver's operation to maximize the energy storage and delivery regardless of the link efficiency. Finally, the effectiveness of the proposed approach is validated by providing simulation and measurement results for different cases. The measurement results utilizing the presented scheme demonstrate notable enhancements, with charging time and stored power experiencing 19.61% and 24.39% improvements, respectively. When considering different reference points for comparison, these improvements can reach as high as 48.44% for the charging time and 93.97% for the stored power. Remarkably, this approach eliminates the need for adjusting the receiver's LC tank and the need for any additional wireless data communication, in addition to obviating the need for direct power measurements at the receiver.

Chapter 5

Conclusions and Future Work

5.1 Contributions and Relevant Publications

With recent developments of IMDs and the need for increased number of channels for precise electrical activity recording and stimulation, the required instantaneous power consumption in such systems is well above the level that could be continuously supplied through the resonant inductive links without violating safety limits. Therefore, energy storage and its optimization are essential tasks to be considered in the design and implementation of PMUs to improve the required precision and functionality of the mentioned systems. On the other hand, the induced power level at the receiver with miniaturized geometry is subject to variations due to the change in different parameters such as distance, misalignment, and mis-orientation between Tx-Rx coils, as well as the required load power which result in deviation of the wireless link's operation from

its optimally designed conditions. Thus, the PMU needs to be resilient against such un-controlled variations and offer an adaptive and robust solution by accordingly adjusting its functionality under different situations. Hence, the main goal of this thesis was to provide solutions for CM and VM receivers that are adaptive to variations in the link's parameters and loading conditions in a way that maximum possible overall link's energy storage efficiency over an arbitrary predefined time window is guaranteed despite these variations. The details of each chapter and contributions are described below.

- Chapter 2 presented a step-by-step development and CAD-based verification of an analytical model for CM power receivers that has resulted in closed-form expression for maximizing the energy storage and its efficiency over a fixed period of time. Furthermore, the precision, efficacy, and adaptivity of the presented solution are experimentally validated using discrete components and a general-purpose controller implementation where the algorithm was capable of detecting the optimal operating point for two inductive links with different parameters. This work has resulted in a journal paper that is published in the IEEE Transactions on Circuit and Systems-I (TCAS-I) [122].
- Chapter 3 presented the design, development, and characterization of a $0.18\ \mu\text{m}$ CMOS IC that occupies $750 \times 600\ \mu\text{m}^2$ active area and is capable of implementing the verified algorithm in Chapter 2 without the need for high-speed and power-hungry ADCs and compu-

tational resources. The implemented IC is capable of automatically detecting the optimal operation that results in maximizing the energy storage of a CM receiver over a fixed time interval on-the-fly without the need for pre-calibration and back communication channel. The accuracy and link-adaptivity of the fabricated IC is cross-validated with theoretical and measurement results. This work has resulted in a conference paper and an extended journal paper that are published in 2021 Custom Integrated Circuits Conference (CICC) [153] and the IEEE Journal of Solid-State Circuits (JSSC) [154], respectively.

- Chapter 4 presented the design and development of a stand-alone $0.18\ \mu\text{m}$ CMOS IC that occupies $2 \times 2\ \text{mm}^2$ area and is capable of operating a VM receiver to result in its maximum possible overall link's energy storage efficiency while being capable of simultaneously delivering the required power to its load. The IC is capable of automatically controlling the receiver's operation to maximize the energy storage of the surplus energy that gets induced in the receiver at different load powers, without the need for direct power measurements or a back communication channel. Furthermore, the energy reception and delivery are performed in two different phases that isolates the actual loading of the receiver and results in optimal power reception and delivery independent of the actual power consumption level. The conventional implementation of the inductive link with an on-chip coil and PMU was included as part of an optogenetic neuro-stimulator that is published in 2020 CICC [155] and the IEEE Transactions on Biomedical Circuits and Systems (TBioCAS) [147].

The VM's energy storage optimization work will be submitted to the IEEE ISSCC/CICC and the extended version will be submitted to IEEE JSSC/TBioCAS.

5.2 Future Work

Future work trends that could be conducted in continuation of this thesis are summarized below.

5.2.1 Energy Recycling

After utilizing the maximum possible inductive link's capacity at a certain coupling distance towards energy storage that resulted in maximizing the overall link's energy storage efficiency, the major task of the PMU is to effectively recycle this stored energy for power consumption during high power events or when the source power is disturbed/insufficient. Recently, [53] has proposed and implemented an energy recycling technique in inductive power delivery for the first time in which the receiver's LC tank is reused to recycle the stored energy in the storage capacitor and deliver power to the load when necessary. While this approach eliminates the need for an off-chip inductor and improves the PMU's form factor, the receiver's LC tank could not be used for simultaneous wireless power reception and energy recycling without interrupting the wireless link. On the other hand, energy recycling would certainly affect the voltage levels at different essential nodes in the system. Therefore, the main challenge is to introduce energy

recycling techniques that could be performed without severely affecting the optimal operating point of the wireless power link and facilitate simultaneous wireless power delivery and energy recycling in the system.

5.2.2 Improvements to Energy Storage and Power Delivery in VM and CM

Power Receivers

Another important aspect to be revisited while performing energy storage could be the undertaken methodology for continuous power delivery to R_{L1} -type loads (defined in Chapter 4, Section 4.2) in the system. As mentioned in the Introduction chapter, the power loss in the voltage regulators is directly proportional to the voltage difference between their input/output terminals. As the voltage at the input of voltage regulator (i.e., the voltage on the storage capacitor) is proportional to the stored energy level, the power loss in the voltage regulator is un-controlled and inevitable. Therefore, alternative power delivery solutions with lower losses should be considered for having a highly efficient system that could possibly adjust their performance according to different voltage levels on the storage capacitor (i.e., voltage tracking) while simultaneously achieving the required voltage regulation at the load side.

VM Architecture

After defining the target application and desired power levels, the controller and its sensing circuitry can be fine-tuned to prioritize the reduction of total power losses in the energy storage optimizer system for VM receivers. This adjustment holds the potential to further enhance overall link's energy storage efficiency across different voltage levels within the system. Alternatively, other power converter topologies such as utilization of flying capacitors could be investigated. Moreover, the efficacy of possible alternative architectures such as switched-capacitor power converters could be investigated as well to eliminate the off-chip inductor and achieve a fully-integrated solution for the overall link's energy storage efficiency maximizer stage. Alternatively, combining the rectifier and DC-DC converter stages for the sake of achieving an optimal operation of the inductive link for simultaneous power delivery and maximizing the overall link's energy storage efficiency would be among possible research directions as well.

CM Architecture

For CM receivers, possible improvements include replacing the diode with controlled power switches and a low power controller that automatically adjusts its switching frequency and timing considering both energy storage maximization and power delivery in the system in addition to preventing residual energy in the receiver's LC tank. Furthermore, voltage regulation approaches

similar to [54] at the load side needs to be considered as well for proper power delivery to the load while considering optimal energy reception and storage over a predefined period of time.

5.2.3 Hybrid VM-CM Implementation

To extend the robustness of PMU against coupling and loading variations, implementing a hybrid solution that combines VM and CM architectures is essential. While hybrid solutions have been recently implemented in [53, 115], possible improvements include devising such systems towards maximizing the overall link's energy storage efficiency and power delivery at the same time. Further studies to be conducted to automatically and adaptively identify the VM/CM modes for different scenarios and design a compact integrated PMU for seamless VM/CM operation, while preventing the use of off-chip bulky components by sharing common resources for the two different modes of operation.

5.2.4 Multi-Rx Links

With development of neural dust concept, a single transmitter could be used to wirelessly power an array of receivers within an enclosed area. In such systems, the transmitter power is typically adjusted based on the weakest link which includes the farthest receiver for a robust operation. Therefore, PMUs in the nearer receivers with higher induced power level could employ energy

storage schemes to store the surplus energy and recycle it when needed contrary to cutting-off the extra power. Therefore, extending the theoretical model and operation for links with multi-receivers could be considered among a future research trend as well.

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