

A HIGH-SPEED AND LOW-NOISE NANOPORE AMPLIFIER AND EVENT DETECTOR

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A thesis submitted to the Faculty of Graduate Studies
in partial fulfilment of the requirements
for the degree of

Master of Computer Engineering

Graduate Programme in Computer Science and Engineering
York University
Toronto, Ontario
November, 2015

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Abstract

This thesis focus on the design of an improved-accuracy algorithm for real-time nanopore-based signal detection (e.g. base calling) and high-speed nanopore signal measurement circuits with low-noise. First, the proposed approach is based on the cumulative sum technique but employs a decision-directed policy coupled with a post-decision correction mechanism to achieve at least a $10\times$ accuracy improvement over a previously reported method. As a result the new technique can better accommodate high-speed embedded nanopore measurement applications such as DNA sequencing.

For the circuit design, we apply the CMOS technology since the nanopore-based molecular sensing affords a close coupling between DNA sequencing and semiconductor signal processing. The key analog front-end components of such an ASIC are described herein. In particular, the design of a 3-MHz 130-nm CMOS front-end with reduced area, $2\times$ reduction in power, and 25% noise improvement compare with state-of-the-art designs.

Acknowledgements

I would like to express my ultimate gratitude to my supervisors Prof. Sebastian Magierowski and Prof. Ebrahim Ghafar-Zadeh for their continuous support throughout this thesis. Without their effort, this thesis would not have been possible. Especially, Prof. Sebastian helped me a lot not only in the research region but also taught me how to balance the study and life at the same time. Also, thanks for your patience and kind about my poor English writing and helped me to revise the papers. Without those, it is impossible for me to finish my master study.

I would also like to thanks Hossein Pourmodheji and Giancarlo Ayala who were always there when I needed and gave me endless support to continue the work. They showed me a huge interest in the research itself. This inspired me a lot from the very beginning. They taught me how to tackle the problem from different angles and showed me different possible ways to solve them. They were always willing to help whenever I needed. Thanks for your kind help during these two years.

I want to thank my colleagues for lending me a hand whenever I needed one. Specially thanks to Chenjie Wang and Mingbin Xu who always cheered me up in times when I looked gloomy due to the pressure of meeting deadlines.

I would like to thank the Canadian Microelectronics Corporation (CMC) for providing the simulation tools and the York technique staff for providing the technique support whenever I needed. Without their works this project would never be there.

My beloved parents, Weiru Huang and Yanping Yang, deserve a special thank you for their unlimited supports during my entire life. I also like to thank all of my family members in China for their encouragements. Last but not at least, I appreciate continuous love and supports from my fiancée, Yang Jie, who has been always with me patiently enduring hardships.

Dare and the world always yields.

If it beats you sometimes, dare it again and again and it will succumb.

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Chapter 1

Introduction

1.1 Motivation

Finding the underlying structure and components of complex molecules is a critical objective in many biological sciences. Discovering and analyzing molecules to such constituent detail answers fundamental scientific questions about biological life and has critical applications to medicine and health care. The process by which the components of such underlying structures are elucidated is generally referred to as sequencing. The molecules to which it is applied are typically the cell's nucleic acids: the deoxyribose nucleic acid (DNA) [1, 2] — the so-called “blueprint of life” — and the ribonucleic acid (RNA) [3], a key messenger in cellular activity and pre-cursor to the realization of more complex molecules (e.g. proteins). And the key constituents identified are the sequence of monomers (i.e. nucleotides) consisting of adenine (A),

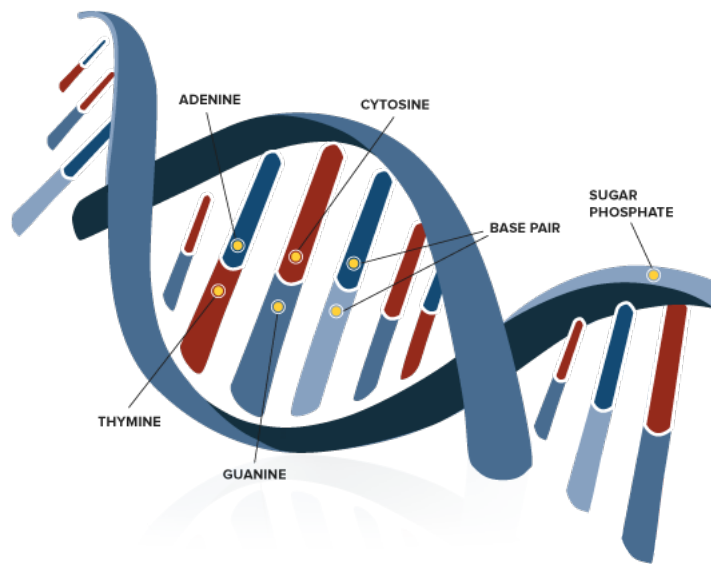


Figure 1.1: A basic illustration of the base (i.e. nucleotide) sequence [4].

cytosine (C), guanine (G), or thymine (T). An illustration of the DNA molecule along with its constituent base (i.e. nucleotide) sequence is shown in Fig. 1.1 [4].

A famous sequencing technique was originally proposed and demonstrated on a 5000-base-pair bacteriophage by Sanger in 1977 [5] and ushered a useful, for the time, means to experimentally analyze nucleic acid molecules. Since the introduction of Sanger's method, the sequencing process has undergone many important developments intended to increase its efficiency and speed while lowering cost.

Technological progress since the Human Genome Project (HGP) is a particularly vivid example of this advance. The HGP was a multi-year, multi-billion dollar se-

quencing effort [6] to analyze the three-billion base-pair human genome. The equivalent of this project can be accomplished today in a matter of weeks at a cost of thousands. This improved state and indeed the completion of the HGP itself was accelerated in no small part due to a variety of advances to the sequencing process (e.g. shotgun sequencing). The emergence of so-called “next-generation sequencing” (NGS) or *2nd generation sequencing* roughly 10 years ago [7, 8, 9] (i.e. after the completion of the HGP) ushered in yet another boost to sequencing efficiency in terms of cost and speed.

Although impressive, these advances still leave sequencing far short of being available to the broad population for a large range of applications like Disease-targeted sequencing, whole-genome sequencing and noncoding RNA expression profiling, etc. To achieve deployment scales capable of making sequencing available to many, cost must still drop by orders of magnitude [10]. Fortunately sequencing technology continues to advance, a critical example of this being the nanopore sequencing method — one of the so-called *3rd generation sequencing* techniques [11] — that forms the main concern of this thesis. In particular, as elaborated below, this work presents electronic and algorithmic means by which nanopore-based sequencers (NBS) [12, 13, 14] can be made to operate at rates several orders-of-magnitude higher than its contemporary performance levels without suffering in accuracy or cost.

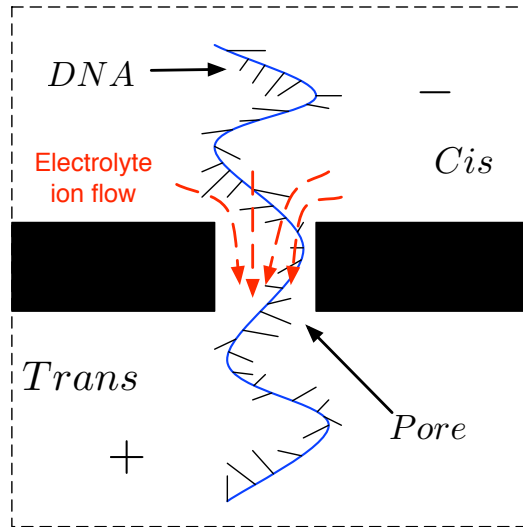


Figure 1.2: An illustration of the nanopore setup.

1.2 Nanopore Sequencing

As illustrated in Fig. 1.2, NBS employs a nanoscale aperture (the nanopore) through which a single molecule can be electronically threaded. The charged nature of a DNA molecule allows this movement to be facilitated through the application of a bias voltage. The pore is created (or embedded) in a thin membrane which effectively creates a porous wall separating two chambers both of which are filled with an ionic fluid (e.g. KCl) in which the molecule under test floats. The chamber in which the molecule originates is referred to as the *cis* while the chamber to which it is moved (i.e. translocated) is the *trans*.

The passage of a particle (and, generally speaking, *analyte*) through such a hole modulates an otherwise constant electrochemical current established by an ionic solution in which the hole is immersed. An illustrative sketch of these current fluctuations as a function of time is shown in Fig. 1.3 [15]; the current levels (i.e. *event levels*) and their temporal duration (i.e. *dwell times*) are indicative of the threaded molecule's component parts (e.g. monomers) passing through the nanopore over time. These levels achieve values between the 10s of picoamperes (pA) and 10s of nanoamperes (nA) depending on the nanopore sensor design and the measurement apparatus. Naturally, such current signatures (red *eventline* trace in Fig. 1.3) can be used to identify the structure of a translocating molecule. For example, in the case of DNA an ideal measurement scenario would be such that only four unique event levels are observed, each corresponding to a unique base (i.e. A, C, G, or T).

As shown in Fig. 1.3 the ideal piecewise constant eventline is corrupted by noise fluctuations around its ideal settings. These disturbances are caused by both the sensor and the electronics of the measurement apparatus. A core focus of this thesis is how such fluctuations can be reduced and mitigated especially as the rate of measurement is increased. We elaborate on this below.

Coupled with traditional microelectronic technology (i.e. CMOS: complementary metal-oxide-semiconductor) [16] nanopore sensors present the opportunity for realiz-

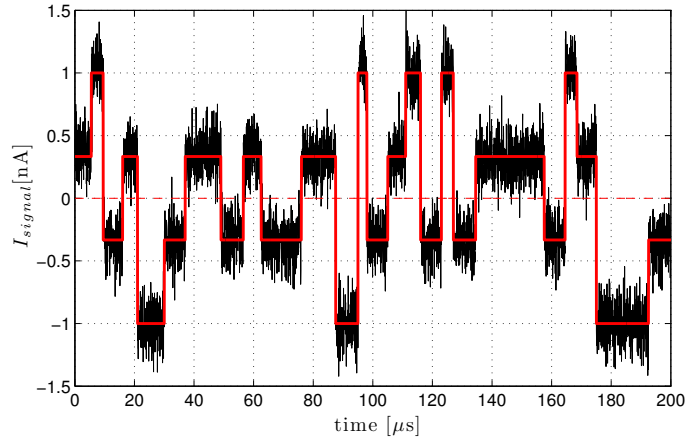


Figure 1.3: An illustration of the current fluctuations in function of time. The step-wise levels in red identify the ideal signal (i.e. *eventline*) while the black trace denotes the eventline corrupted by noise.

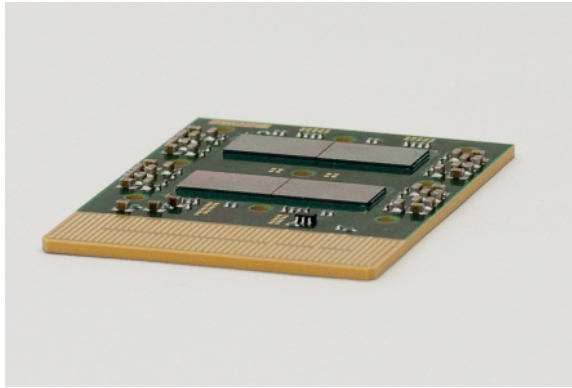


Figure 1.4: ONT DNA strand sequencer on a board

ing an extremely compact embedded molecular sensing system. Thus, a key part of this thesis focused specifically on CMOS electronics for high speed nanopore sequencing applications. A prominent example of NBS is Oxford Nanopore Technologies' (ONT) DNA strand sequencer, now in pre-commercial release [17]. A photo of this miniaturized ONT sequencer, the MinION, is shown in Fig. 1.4. This product demonstrates a sequencing technology approaching a footprint on par with standard mobile computing devices.

Although the ONT machine demonstrates the feasibility of a miniaturized nanopore sequencer many improvements remain to be realized. At the moment the machine can obtain a reading rate (i.e. event rate) of roughly 70 bases-per-second (bps) using a biological (i.e. protein based) nanopore. The accuracy of the device, roughly 70% at the base-calling stage has also been good enough to sequence microbial and even human genomes [18]. However this has come at the cost of increased delay (to gather more redundant samples) and bioinformatics effort (more extensive downstream computations) in order to assemble final sequences of reasonable quality.

As with any technology, the need to improve performance and decrease cost persists with nanopore sequencers as well. The biological pores currently used can be made to process molecules at event rates approaching 10,000 bps. Even more aggressively, nanopore sequencers based on solid-state apertures can be made to operate at

speeds in excess of 1 Mbps [19, 15]. These options present significant opportunities for the scaling of nanopore sequencer performance to future applications.

Such elevated measurement rates however introduce significant challenges for the circuitry needed to process the electronic signals. In fact two interrelated challenges can be identified. As the event rates being processed go up, circuit and sensor limitations tend to increase the noise contribution present in conjunction with the eventline. This challenge become particularly acute at Mbps rates, a speed increase $10,000\times$ greater than the state-of-the-art ONT machines. Thus one clear challenge for the CMOS is to devise electronic circuits capable of somehow reducing the noise contributions at high operating speeds. The second related challenge is concerned with event identification, that is, the accurate estimation of the eventline from noisy measurements. Naturally these two aspects are related in that a less noisy circuit requires a less robust identification scheme and vice versa.

As outlined and elaborated throughout the rest of the thesis, this research approaches the improvement of the semiconductor hardware by proposing low-noise analog circuit designs and accurate event identification algorithms for digital implementation.

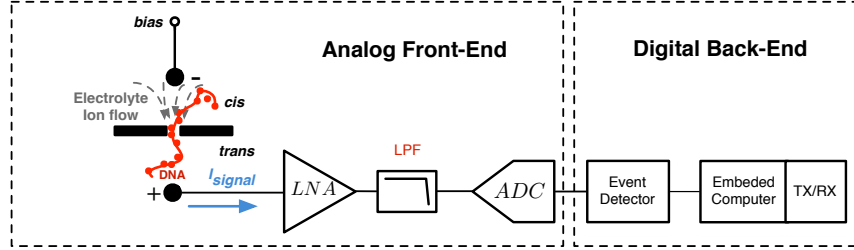


Figure 1.5: An illustration of the NBS Hardware

1.3 NBS Hardware

The basic NBS hardware employs two separate functional blocks by which the nanoampere constant electrochemical current will be amplified and detected. Such small ionic current will be measured and amplified by the *analog front-end* (AFE) amplifier and the order of the translocated molecule will be recognized by the following *digital back-end* (DBE) detector. A basic illustration of this NBS hardware is shown in the Fig. 1.5 and the AFE and DBE elements outlined further below.

1.3.1 Analog Front-End (AFE)

As we can see, the AFE block consists of the nanopore sensor, a low-noise amplifier (LNA), a low-pass filter (LPF) and an analog-to-digital converter (ADC). These three elements constitute the basic construct of an analog-signal processing chain and their

overarching goal is to produce a digital signal with as little loss in signal-to-noise ratio (SNR) as possible. For this to happen a suitably large signal must be presented to the ADC such that it may quantize the signal with sufficient accuracy. This signal magnitude is provided by the action of the LNA in conjunction with the LPF; the LNAs primary function being to provide an initial signal boost with minimal additional noise and the LPFs job being a combination of (further) amplification and filtering as a means of noise and aliasing control.

As is discussed in ensuing chapters the LNA design for NBS is complicated by the electronic properties of nanopore sensors. These sensors tend to have very large equivalent resistances which makes initial LNA stages extremely sensitive to bandwidth killing capacitive contributions. A general strategy has evolved over the years to deal with such scenarios and this approach is adapted in this thesis to NBS applications.

1.3.2 Digital Back-End (DBE)

In the Fig. 1.5, the DBE block [20] is shown consisting of an event detector and an embedded computer. In this part, the main event detector will process the quantized signals by the ADC and throughout its results to the embedded computer to analyze the proper order of the nucleotides where the TX refers to transmit signals and the RX

refers to receive signals. However, most state-of-the-art detector designs are suffering a lot from the input parasitic noise. Thus, the means of achieving better performance lies in not only the improvement of the input amplifier but also the design of high-noise-tolerant event detector.

1.4 Thesis Contributions

In this following, a brief overview of the key contributions of this work is given.

- A high-noise-tolerant edited cumulative sum (CUSUM) on-line detection and estimation algorithm for real-time nanopore-based signal processing is proposed. This algorithm is amenable to embedded hardware implementation in the DBE. Under a key performance metric (the transition error rate discussed in Ch. 3) simulations show that this detection and estimation approach shows $20\times$ better accuracy than a standard method for a 4-level signal processed by a 2-bit ADC.
- The design of a 3-MHz 130-nm CMOS low-noise amplifier (LNA) is presented in the thesis. This LNA occupies a very small area that makes it possible to have dozens of them to accomplish the arrayed nanopore system. Also, this chip design achieves around $2\times$ reduction in power, and 25% noise improvement compared with some known novel LNA designs [16, 21].

1.5 Thesis Outline

The rest of the thesis is organized as follows:

Chapter 2 introduces a standard nanopore-based sequencer (NBS) signal processing chain and the noise distribution of this processing system.

Chapter 3 discusses a overview of the cumulative sum (CUSUM) algorithm event detector. Several issues of that CUSUM event detector are discussed afterwards and in order to solve those problems, a novel CUSUM adjustment, the reshaping CUSUM (RC), is introduced. Finally, certain key component characteristics in the detection chain are settled by comparing the simulation results between the RC detector and the CUSUM approach.

Chapter 4 presents the system and circuit design of the analog front-end (AFE). Then, the detail transistor design of the operational amplifier (op-amp) from which the AFE is built is proposed. Finally, the AFE implementation and its performance in a $0.13 - \mu\text{m}$ CMOS process is explained.

Chapter 5 summaries the current work and gives some suggestions for the future work.

Chapter 2

Nanopore Systems And Signals

This chapter presents a standard NBS signal processing chain elaborating on device and key block constituents. It introduces certain key non-idealities in the analog front-end that are ultimately faced by the detector including different varieties of noise and chain induced bandwidth limits.

2.1 Sensor Model

A utilitarian nanopore sensor model for circuit-level design is a Norton equivalent circuit as sketched in Fig. 2.1. The source I_s represents the effective electrochemical current through the pore. For state-of-the-art solid-state pores it is possible for unobstructed ionic currents around 10 nA to flow through the pore. As nucleic acids translocate through the pore current may drop by roughly 5 nA [19].

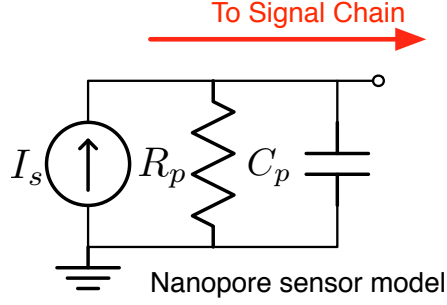


Figure 2.1: A Norton equivalent circuit of nanopore sensor model

The equivalent resistance of the unobstructed pore is modelled by R_p . For solid-state nanopores this element is primarily related to the diameter, d , and thickness, t , of the opening [22] and can obtain a relatively broad range of values. For a state-of-the-art pore with $d \approx 1.5$ nm and $t \approx 4$ nm an $R_p \approx 100$ M Ω .

The pore's equivalent circuit also includes a capacitance, C_p , which lumps in the effect of the insulating membrane in which the hole is embedded as well as any extrinsic wiring capacitance imposed by the sensory apparatus before encountering the signal processing chain. Recent work has reported values as small as 1.5 pF [23] for this parameter, but capacitances around 5 pF have also been noted for nanopore systems interfaced to a CMOS apparatus [16].

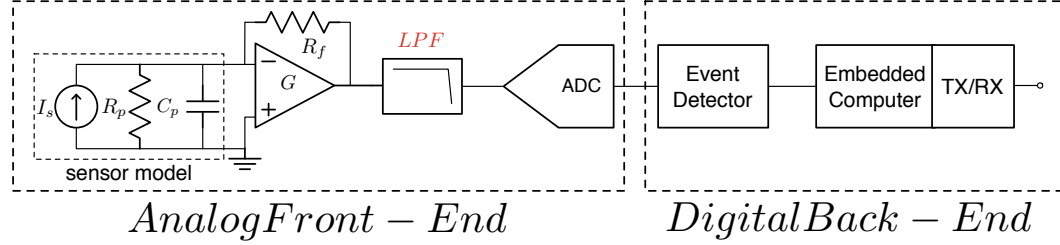


Figure 2.2: The CMOS NBS signal processing chain.

2.2 NBS Signal Chain

Another simplified representation of a CMOS NBS signal processing chain is shown in Fig. 2.2.

The typical chain structure (after the sensor itself) starts with a current pick-up electrode (not explicitly indicated in Fig. 2.2) connected to a low-noise transimpedance pre-amplifier (TIA) (the LNA block discussed in Chapter 1) of the analog front-end (AFE). Following typical strategies, a transimpedance architecture is used in order to convert a current signal to a voltage signal. For the NBS in particular the TIA's job is to amplify the tiny $10^{-11} - 10^{-8}$ ampere electrochemical current flowing through the electrode and convert it to a voltage on the order of 1 V. This will make it possible for the following circuitry to adequately process the (boosted voltage) signal (e.g. ensuring filtering, sampling, and digitization). Invariably however such a pre-amplification stage adds electronic noise.

After the TIA a low-pass filter (LPF) is used to bandlimit the signal such that the ensuing sampling process is not overly burdened with aliased noise. As always a tradeoff exists between the amount of noise filtered and the amount of desired signal passed for downstream processing (i.e. base calling, alignment, etc.).

The LPF analog output is then funnelled into an analog-to-digital converter which outputs a digital representation of a sampled discrete time version of the signal. The ADC's resolution (the number of bits used to represent its output) is a critical consideration. The lower the quantizing resolution, the cheaper the overall signal chain, the higher its possible sampling rate, the smaller its silicon footprint, and the lower its power consumption. Clearly many benefits accrue to a system capable of running at higher noise incurred by lower quality data conversion.

Finally, with the signal transformed to a digital representation we can implement our event detector and embedded computer in the digital back-end (DBE) whose job is to extract the underlying eventline signal from the noisy input and to thus accurately predict the level and duration of events.

2.3 Noise and Signal Characteristics of the Nanopore

In NBS system research, the noise presented by the sensor and the noise introduced in the AFE have become the dominant issues for the accomplishment of accurate base

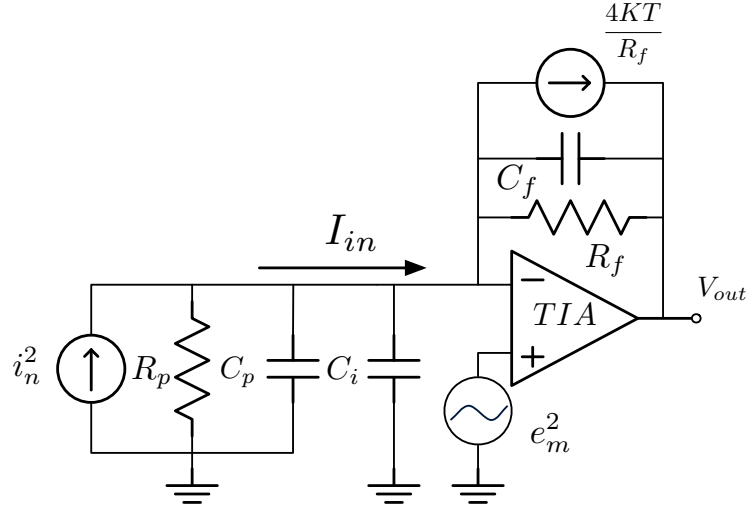


Figure 2.3: Noise model for the NBS system

calling. This is especially the case for solid-state NBS systems as the proclivity of these sensors to work at high speeds, and hence high event rates, leaves them susceptible to egregious levels of high frequency noise. We elaborate on this high frequency noise component as well as other key contributors to NBS signal noise presently.

2.3.1 Noise Distribution

As mentioned above, our ability to extract information from NBS signals is compromised by noise additions incurred during the sensing and measurement process. The nanopore sensor's thermal and flicker noise are well-known contributors [24]. The contributions from the CMOS TIA are also important. In fact as detailed below, when

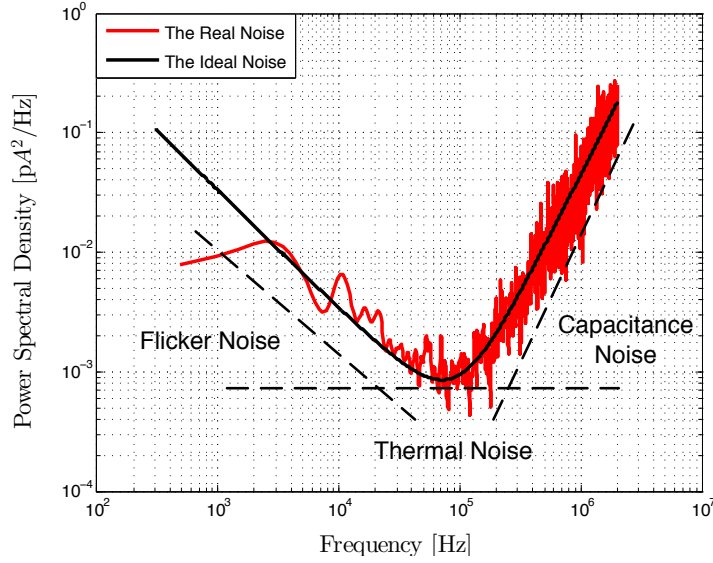


Figure 2.4: The PSD of the input current noise.

we seek to operate at increasing measurement speeds the amplifier noise becomes the critical factor [25]. For example, the noise, modelled as an equivalent input current noise with power spectral density (PSD) $\overline{i_n^2}$ (see Fig. 2.3 which highlights the key noise contributors: the sensor and the TIA [26]) assumes a spectral distribution typical of the PSD shown in Fig. 2.4. As demonstrated, there is a decreasing low-frequency noise component (the *flicker* noise), a noise “trough” at “mid-frequencies” (*shot* or *thermal* noise), and a rapid increase in noise at high frequencies of operation (*capacitance* or *blue/violet* noise).

Formally the main noise contributors can be expressed as the sum of various current

noise spectral densities

$$\overline{i_n^2} = \overline{i_f^2} + \overline{i_t^2} + \overline{i_{cap}^2} \quad (2.1)$$

where $\overline{i_t^2}$ denotes to the thermal noise coming from the nanopore and the CMOS TIA's constituent transistors, $\overline{i_f^2}$ refers to the flicker noise from the sensor and $\overline{i_{cap}^2}$ is the overall capacitance noise.

Specifically, the standard flicker noise model formalizes this noise contribution with [27, 28]

$$\overline{i_f^2} = \frac{A(I_{dc})^2}{f} \quad (2.2)$$

where I_{dc} refers to the DC current and f denotes the operating frequency and A is an empirical scaling factor. The physical origins of this source are not definitive, but typically associated with a trapping process wherein translocating molecules are momentarily stopped (trapped) by the nanopore aperture. The overall effect of such a mechanism is to introduce an inverse frequency relationship.

Referring to Fig. 2.3 (a basic sketch of a nanopore sensor and TIA along with key passive elements), for the thermal noise we have the expression

$$\overline{i_t^2} = \frac{4kT}{R_p} \quad (2.3)$$

where $k = 1.38^{-23}$ J/K is the Boltzmann constant, T is the temperature (in Kelvin) and R_p is the equivalent resistance of the pore's channel and the mouth of the nanopore [16].

The e_m term refers to the equivalent input noise voltage source associated with the TIA. Three main thermal noise contributors are identified in (2.3): the op-amp comprising the TIA, the feedback resistance, R_f , and the sensor itself (R_p and R_a).

Finally there is the capacitive noise [16] component which can be expressed with

$$\overline{i_{cap}^2} = (C_{total}e_m2\pi f)^2 \quad (2.4)$$

where C_{total} refers to the summation of the membrane capacitance C_p , the amplifier input C_i and feedback C_f capacitances (see Fig. 2.3) presented by the TIA to the nanopore. As indicated, this contributor has its origin with the TIA's op-amp (i.e. via its e_m noise equivalent). In particular, the capacitive noise is a reflection of the decreasing TIA closed-loop gain with frequency due to the signal shunting impact of C_{total} . As the frequency increases more signal flows through C_{total} rather than participating in feedback via R_f . Thus the gain of the amplifier drops and, effectively, the noise contribution goes up. As already noted above, and clearly demonstrated by (2.4) this noise source increases with f^2 making it particularly egregious for high-speed NBS applications.

The spectral current noise density contributed by each component of (2.1) is shown in the Fig. 2.5. As we can see from the graph, the dominant noise is the flicker noise when the sequencing is made to work at rates under 100 kHz. The capacitance noise becomes dominant once the frequency exceeds 100 kHz. Disturbances having such a

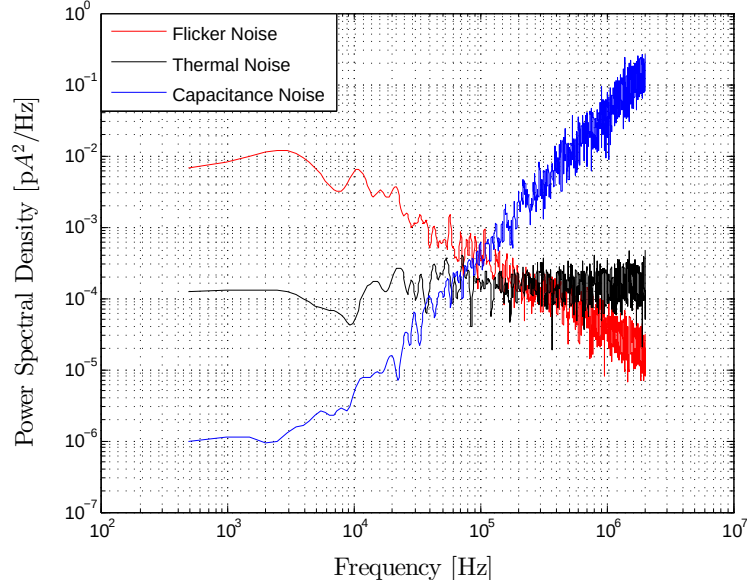


Figure 2.5: The PSD of various components in the NBS input-referred current noise.

$\propto f^2$ frequency dependence are sometimes referred to as *violet noise*.

2.3.2 SNR and Measurement Event Rate

What are the implications of the noise characteristics discussed above for the detection stages that follow the AFE? A popular criterion upon which detection algorithms rely is the signal-to-noise ratio (SNR) [29]. Maximizing this value (at the input to the detector's decision logic) leads to improved accuracy (reduced error rate) at the output of the detector. An example of the general SNR characteristics exhibited by a high-speed embedded NBS system (at the input to the detector as a whole) is shown in

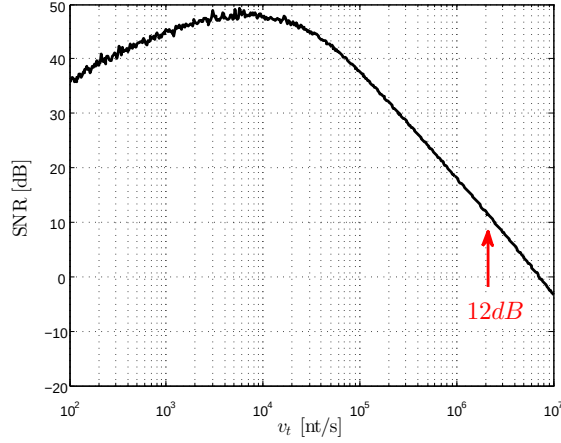


Figure 2.6: A plot of the NBS SNR dependence on the event rate, v_t , being processed by the system. A 12-dB SNR is obtained at event rates of 2 Mnt/s.

Fig. 2.6. This curve is calculated using

$$SNR_{dB} = 10 \cdot \log \left[\frac{\text{var}(I)}{2\sigma_n^2} \right] \quad (2.5)$$

where $\text{var}(I)$ is the variance of the electrode's eventline input current [30, 31] (see Fig. 1.3) and σ_n is the standard deviation of noise disturbance. The SNR is depicted as a function of the fastest *event rate*, v_t , present in the measurement. That is, the maximum speed at which features of interest create the level modulations I . For DNA sequencing applications the primary events refer to the passage of nucleotides (nt) through the pore and thus we employ nt/s as a catch-all measure of v_t .

Assuming Nyquist sampling, the sensor and TIA signal frequencies that must be captured by the detector must be $2v_t$. As a result the SNR profile of Fig. 2.6 resembles

the noise characteristics exemplified by Fig. 2.4 as the system's maximum operating event rate determines the amount of sensor and TIA noise we allow to perturb our eventline. As the NBS system's event rate is increased from 10^2 nt/s the SNR improves since the signal energy outpaces the declining flicker noise contribution. Continuing this event rate increase above 10^4 nt/s introduces a precipitous drop in SNR due to the influx of capacitive noise.

Chapter 3

Event Detection

The preceding chapter highlighted the characteristics of noise, especially violet noise in high-speed CMOS NBS. We now consider the algorithmic means of extracting the eventline event levels and their transitions from highly corrupted signals in real time. Such means are to be ultimately implemented in the DBE but their tolerance to noise can simplify the AFE specifications (e.g. amplifier noise, filter order, ADC resolution, etc.)

3.1 Real-Time Detection

A unique aspect of NBS systems is their ability to generate measurement signals directly on their molecular samples as the nucleic acid analyte is being processed by the device (i.e. translocating through the nanopore). This is unlike 2nd generation

(2G) sequencing systems which must first subject the analyte to an elaborate chemical treatment before proceeding with measurements. As such, the amenability of NBS to real-time sensing applications is significantly greater than 2G technologies. To fully exploit this advantage it is imperative that NBS be fitted with real-time (i.e. on-line) detection methods capable of making signal approximations as the samples stream through the device.

Naturally on-line methods suffer compromises not faced by their off-line detection counterparts. In particular, on-line approaches can't benefit from a global analysis of the data before making local decisions/approximations. For example, an on-line detection scheme may be able to run a statistical analysis on a large time series and with this information better determine the thresholds for a decision scheme. In their purest form, on-line methods are confined to decision-making based only on the confluence of past samples which tends to affect their accuracy.

3.2 NBS Detection Overview

We now formalize somewhat the goal and structure of the NBS detection system. First, as already outlined in Chapter 1, the goal of the detector is to extract as accurately as needed the eventline from the noisy signal accrued via the measurement and AFE processing stages. Ideally the eventline is a piecewise constant waveform as sketched

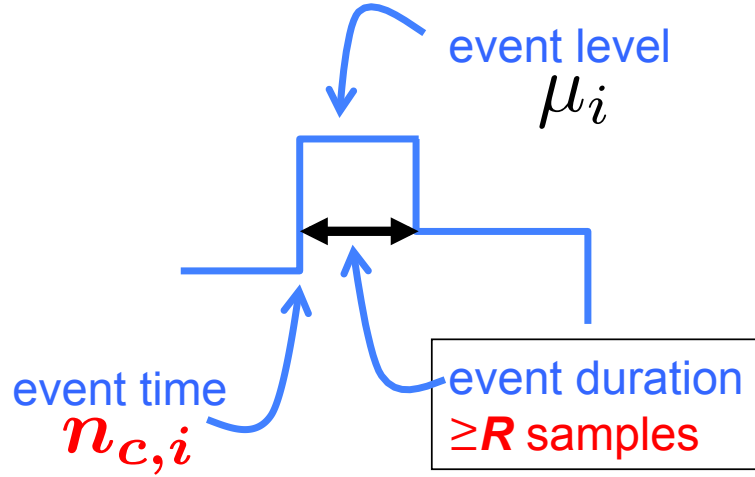


Figure 3.1: The signal eventline (corrupting noise not shown). The *event level* and its corresponding *event time* are to be extracted by the DBE’s detector.

in Fig. 3.1 consisting of a sequence of discrete *events* with integer index i and two key features per event, i : the *event level* μ_i and the time (index) at which that event starts, the so-called *event time*, $n_{c,i}$.

We also assume that the detector works on a sampled signal and the the shortest *event duration* between adjacent event times $n_{c,i+1} - n_{c,i}$ can be captured with at least R samples which we refer to as the *oversampling rate*.

The on-line approach to nanopore event detection ultimately taken in this work employs methods from adaptive filtering and quality control. The high-level architecture of such a detector is shown in Fig. 3.2. The two main constituents of the detector are

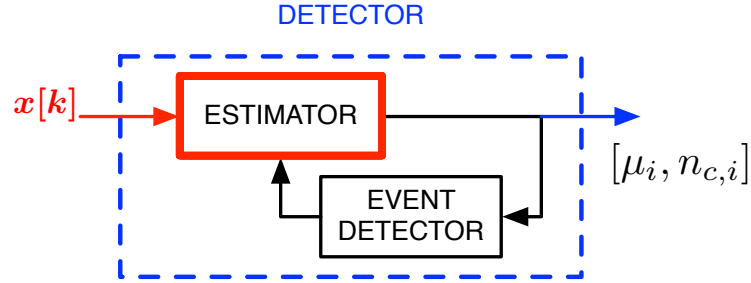


Figure 3.2: The high-level architecture of a real-time NBS eventline detector. Input signal samples $x[k]$ are converted to eventline feature estimates μ_i and $n_{c,i}$.

the *estimator* block and the *event detector* (in contrast to the overall system to which we refer to as the *detector*) block.

The job of the estimator is to take (noisy) input signal samples $x[k]$ (k is the sampling index) and produce estimates of the even levels μ_i . The job of the event detector is to sense the *event time* $n_{c,i}$ (i.e. when a transition from event $i - 1$ to event i is made) and thus to update any dependent estimator parameters needed for the estimation of the ensuing event level. Of course, $n_{c,i}$ is useful for ensuing computations as well. In particular both μ_i and $n_{c,i}$ are needed to ultimately complete base-calling in an NBS situation. The computational concern of this thesis however is only up to the detection stage.

3.3 The CUSUM Algorithm On-Line Detector

A powerful strategy for real-time even detection employs the cumulative sum (CUSUM) algorithm originally introduced in [32]. In general, CUSUM detects level changes by accumulating statistics on its input data and subjecting these to a simple hypothesis test in seeking abrupt changes.

A log likelihood ratio test is often used to enable this where an instantaneous test statistic shown in Fig. 3.3 is expressed as

$$s_u[k] = \ln \left[\frac{p_X(x[k]; \hat{\mu}_X[k] + \delta_{min})}{p_X(x[k]; \hat{\mu}_X[k])} \right] \quad (3.1)$$

where k denotes the sampling index and $p_X(x[k]; [\cdot])$ refers to the probability density function (PDF) of the random variable, X , at the data sample $x[k]$ with some parameter $[\cdot]$. The PDF is assumed Gaussian with standard deviation, $\sigma = \sigma_n$ where σ_n is the variance of the noise disturbance present in the measurement.

The parameters considered are, in the denominator of (3.1), the estimated signal average, $\hat{\mu}_X[k]$ (updated every k during the course of an event) which approximates an event level in the nanopore baseline,

$$\hat{\mu}_X[k] = \frac{1}{k} \sum_{m=1}^k x[m], \quad (3.2)$$

and the minimum expected deviation δ_{min} from this level (as seen in the numerator of (3.1)).

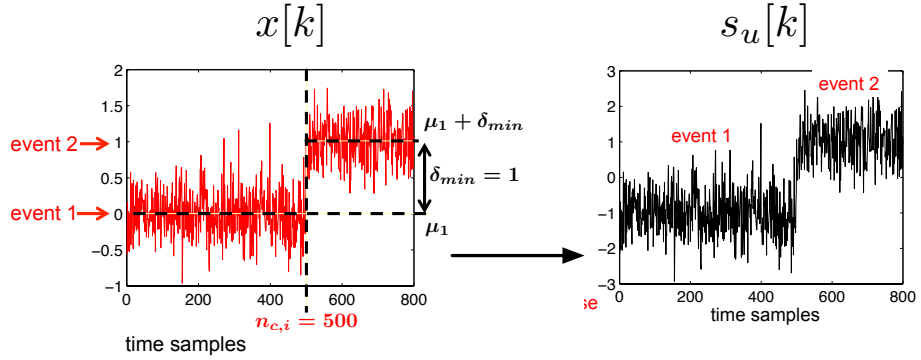


Figure 3.3: A simple illustration of a log likelihood ratio test

The test statistic, $s_u[k]$, in turn, is used to construct a cumulative test statistic [32]

$$G_u[k] = S_u[k] - \min_{1 \leq n_c \leq k} S_u[n_c - 1] \quad (3.3)$$

where n_c (the *transition* or *change index*) denotes the sample at which a change occurs and

$$S_u[k] = \sum_{n=0}^k s_u[n]. \quad (3.4)$$

Since, the change index, n_c , is a measurement feature we are in search of and is clearly not known at the outset, some iterative approximation to (3.3) is needed. Perhaps not surprisingly it can be shown [32] that (3.3) can be re-expressed in the recursive form

$$G_u[k] = G_u[k - 1] + s[k] \quad (3.5)$$

and thus indeed solved using an iterative procedure.

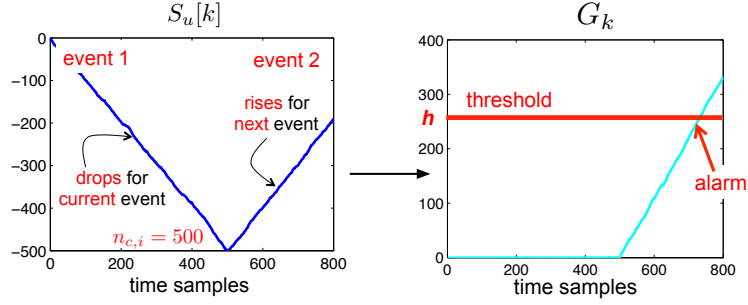


Figure 3.4: The construction of a cumulative test statistic

This standard CUSUM-based detector reports the occurrence of a transition when $G[k]$ exceeds some threshold, h . Once a threshold crossing in Fig. 3.4 is detected, the actual transition index can be found using the estimator

$$\hat{n}_c = \arg \min_{1 \leq n_c \leq k} S_u[n_c - 1]. \quad (3.6)$$

Of course, the basic CUSUM lacks the facility to detect whether a positive (*up*) or negative (*down*) change occurred, hence a complementary test utilizing

$$s_d[k] = \ln \left[\frac{p_X(x[k]; \hat{\mu}_X[k] - \delta_{min})}{p_X(x[k]; \hat{\mu}_X[k])} \right] \quad (3.7)$$

is employed to account for change polarity. This augmentation is referred to as the double-sided CUSUM (DSC) algorithm and this approach has been applied to real-time nanopore base-calling in [33]. We present the performance of this approach relative to our own CUSUM variation (described in Section 3.4) in Section 3.5. As

outlined in [34], DSC's optimum threshold setting is

$$h = \delta_{min}/\sigma_n \quad (3.8)$$

where σ_n , as already mentioned, is the noise induced standard deviation of the corrupted input signal (i.e. V_{out} as shown in our Fig. 2.3 example).

Although DSC is popular by virtue of its simplicity (i.e. only two signal parameters, δ_{min} and σ_n , are considered), it faces a number of serious challenges for NBS applications. First, DSC is designed to handle additive white Gaussian disturbances; its performance degrades significantly when subject to signals corrupted by coloured noise as present in high-speed CMOS NBS systems. Second, DSC performance is very sensitive to the choice of h , hence its calculation via (3.8) and uncertainties in δ_{min} and σ_n can markedly affect performance. Third, DSC is prone to the accuracy of the data it is given to process and hence requires expensive high-resolution ADCs if considered for embedded real-time NBS. A new algorithm designed to address these issues is described below.

3.4 The Reshaper-based CUSUM

To solve the DSC issues outlined above we introduce a new CUSUM technique – we refer to it as the reshaping CUSUM (RC) – that employs oversampling to achieve

Algorithm 3.1 The novel reshaper CUSUM (RC) Algorithm

```

1: Initialization
2: set  $C$  to contain the known discrete DNA event levels
3: set  $\sigma = 1$  and  $\delta_{min}$  = minimum level difference in  $C$ 
4: set  $R \geq 1$ 
5: set  $h = R \times (\delta_{min}^2 - (\delta_{min}/2)^2)/2 \times \sigma^2$ 
6: set  $S[-1] = G[-1] = \hat{n}_c[-1] = 0$  and  $i = -1$ 
7: initialize the estimator's  $\hat{\mu}_i$  using (3.9)
8: end
9: while the algorithm is not stopped do
10:   set  $k = \hat{n}_c[i] + 1$ 
11:    $\hat{\mu}_i = \arg \min_{l \in C} \{d(x_i|_1^R, l)\}$ 
12:   while the algorithm is not stopped do
13:      $s[k] = \ln \left[ \frac{p_X(\hat{\mu}_i + \delta_{min}/2; \hat{\mu}_i)}{p_X(x[k]; \hat{\mu}_i)} \right]$ 
14:      $S[k] = \sum_{n=0}^k s[n]$ 
15:      $G[k] = S[k] - \min_{1 \leq n_c \leq k} S[n_c - 1]$ 
16:     if ( $G[k] > h > 0$ ) then
17:        $\hat{n}_c = \arg \min_{1 \leq n_c \leq k} S[n_c - 1]$ 
18:       stop or reset the inner while
19:     end if
20:      $k = k + 1$ 
21:   end while
22:    $i = i + 1$ 
23:   if no more signals feeding in then
24:     stop outer while
25:   end if
26: end while

```

a decision directed parameter estimation coupled with an error correction strategy. In particular, our method assumes the ability to acquire a certain minimum number of samples, R , during the course of each event level. We refer to R as the oversample rate. In the simplest version of our algorithm the actual sampling rate is constant and hence R denotes the number of samples we capture for the briefest expected event level.

As noted above, a key property of RC includes a decision-directed policy whereby each new event (i.e. signal level) $i \in \mathbb{Z}_{\neq 0}$ is predicted (as denoted by $\hat{\mu}_i$ in (3.12) below) after estimating its mean over the R samples that follow the last predicted transition, $i - 1$. Formally, the decision directed mapping can be expressed as

$$\hat{\mu}_i = \arg \min_{l \in C} \{d(x_i|_1^R, l)\} \quad (3.9)$$

where l is an element of the set C containing the discrete signal event levels that we are seeking to identify and $x_i|_1^R$ denotes the sequence of R signal samples after the detection of the i th event. Any of a number of measures are possible for the distance metric, $d(\cdot, \cdot)$, for example the Euclidean measure

$$d(x_i|_1^R, l) = \sqrt{\sum_{n=1}^R (x[n_{c,i} + n] - l)^2} \quad (3.10)$$

or

$$d(x_i|_1^R, l) = |\mu_i - l| \quad (3.11)$$

where

$$\mu_i = \frac{1}{R} \sum_{n=1}^R x[n_{c,i} + n] \quad (3.12)$$

The intuition of the decision-based policy is to quickly identify a candidate level and proceed with the test static calculation. If our decision is correct, we effectively filter out noise from our reference calculation as attested by RC's test statistic [35]

$$s[k] = \ln \left[\frac{p_X(\hat{\mu}_i + \delta_{min}/2; \hat{\mu}_i)}{p_X(x[k]; \hat{\mu}_i)} \right] \quad (3.13)$$

where our test is now made relative to our ostensibly correct and noise-free guess $\hat{\mu}_i$. Of course, a contingency for dealing with incorrect decisions, $\hat{\mu}_i$, must be implemented. In RC, such a contingency depends on some means of identifying errors made by our decision-based policy.

In RC, we detect policy errors by observing the duration of its event prediction. If the policy produces an event guess that lasts less than R samples, chances are that it mapped to a glitch. Hence, a simple correction strategy is to simply reject all event predictions, i lasting less than R samples and replace them with the previous accepted event level, that is the $(i - 1)$ th event. We refer to this housekeeping block as the reshaper.

The intuition of the reshaper strategy is suitable for Nyquist rate systems where anti-aliasing filters minimize the signal contributions at frequencies in excess of $f_s/2$

where f_s is the Nyquist sampling frequency. In such a setting if transients on the order of $1/Rf_s$ are detected it is natural to assume that an error in detection policy has occurred.

An important performance metric of our detection system, the bit-error-rate (BER), estimates how often we correctly predict the event levels present in our signal. In the context of a NBS intended for DNA sequencing we can define this term as

$$\text{BER} = 1 - \frac{\text{LCS}}{\text{BS}} \quad (3.14)$$

where LCS refers to the longest common substring [36] between the detection result and the original input sequence (i.e. the baseline symbols (BS)). That is, BER in this case simply counts the proportion of base calling mistakes to total number of bases sequenced. In other terms it is related to the base-calling quality factor, Q via

$$Q = -10 \log(\text{BER}). \quad (3.15)$$

Fig. 3.5 shows a comparison of the achievable BER for the RC algorithm with and without the resaper block under typical high-speed NBS noise conditions (i.e. flicker, thermal, and capacitive noise). It is clear that the resaper plays a substantial role in helping the scheme improve the error rate. In this scenario a $15\times$ to $50\times$ improvement is achieved depending on R . Note that in this simulation no bandlimiting filter is assumed hence BER degrades with increasing, R , due to increased violet noise

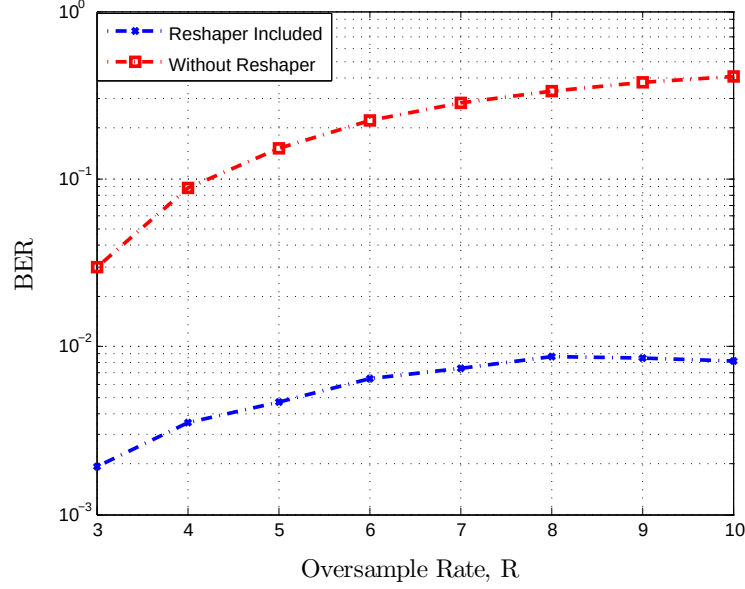


Figure 3.5: A comparison of the new algorithm with and without the reshaper block.

contribution.

The RC algorithm is summarized in Algorithm 3.1 where a couple of further points bear noting. One point involves the fact that both *up* and *down* transitions are sensed with RC's solitary test statistic (3.13). That is, unlike DSC, separate tests for both polarities are not needed. This is a consequence of the decision-directed policy and the assumption of Gaussian distributed noise. By referencing our test statistic to $\hat{\mu}_i + \delta_{min}/2$ in (3.13) we have ensured, due to the symmetry of the normal distribution, that both positive level-crossing deviations in x (e.g. to levels $x[k] > \hat{\mu}_i + \delta_{min}/2$) and negative level-crossing deviations in x (e.g. to levels $x[k] < \hat{\mu}_i - \delta_{min}/2$) equally vary

$s[k]$ and hence contribute to the cumulative test statistic. The polarity of the transition however is ultimately judged by the decision policy.

Another point involves the definition of RC's decision threshold. The choice, which we refer to as the *coarse threshold* setting, shown in line 5 of Algorithm 3.1 is inspired by the minimum change in the log test statistic under the Gaussian noise assumption, that is the reference point, $\hat{\mu}_i + \delta_{min}/2$ compared to a minimum error deviation, $x[k] = \hat{\mu}_i \pm \delta_{min}$. Since a pulse consists of at least R samples we scale the difference by R . A standard deviation term, σ , is retained, as a measure of our baseline signal distribution and for normalized signals is set to 1. Note that unlike DSC, RC's threshold is no longer subject to σ_n suggesting a more robust performance with respect to variations in h . We demonstrate this in Section 3.5.

3.5 Performance Comparison

We now present a comparison of our RC detector and the alternative DSC approach presently outlined in the literature [33] in the context of a basic high-speed NBS design procedure used to settle certain key component characteristics in the detection chain. A typical high-speed NBS detection chain is as already shown in Fig. 2.2 and includes a TIA to boost the weak electronic current measurements into voltage signals of suitable strength; an anti-aliasing LPF to limit out-of-band noise contributions to the measured

signal; the ADC; and finally the detection algorithm (e.g. RC or DSC) to process the sampled noisy data signal.

We present all the following results assuming a NBS system intended to operate at 2×10^6 nt/s, a setting commensurate with recently described nanopore systems leveraging improved amplifier technology [19]. We also assume that the sensory system is endowed with the ability to distinguish between four different uniformly distributed and uniformly spaced levels that in normalized form belong to the set $\{-1, -1/3, +1/3, +1\}$.

3.5.1 LPF Bandwidth Setting

The double-sided PSD of the input signal as well as the noise present at the input of the NBS LPF is shown in Fig. 3.6. As already noted the signal is a random process capable of assuming one of four uniformly distributed levels and whose level-change statistics assume a Poisson distribution (i.e. a *telegraph* signal).

The choice of LPF to process this signal seeks a reasonable balance between performance and cost. A convenient LPF implementation is as a coarse analog filter, ideally integrated directly within the transistor-level arrangement of the CMOS TIA itself. This naturally limits the complexity of such an implementation (as opposed to a digital LPF approach) and herein we consider only a 2nd-order design whose 3-dB

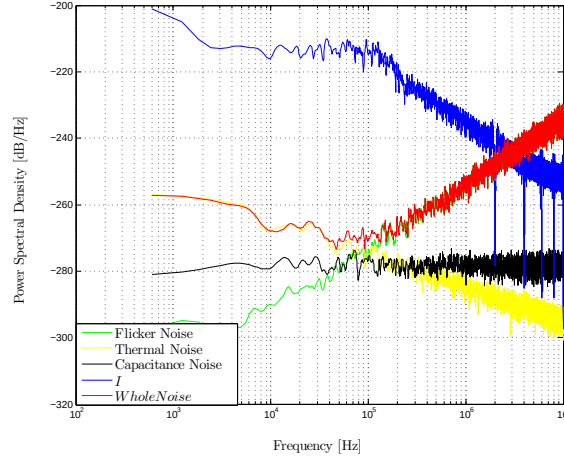


Figure 3.6: The PSD of the input signals and noise ($R = 10$).

frequency is set to 2-MHz in commensuration with our 2 Mnt/s event rate. With this setting more than 98% of the signal power available after the TIA is allowed to continue on to the digital portion of our detector while attenuation the noise. Of course the rapid increase in TIA capacitive noise PSD means that the noise equivalent violet noise bandwidth of this LPF is 2.9 MHz and hence still prone to a noise corruption.

Still, the inclusion of even a coarse LPF is of substantial help to our system as demonstrated by the simulations in Fig. 3.7. As shown, the filter provides at least a 4-dB SNR improvement in the signal presented to the ADC relative to the non-filtered case. This advantage increases as R grows, a result of the fact that higher sampling frequencies capture more noise power.

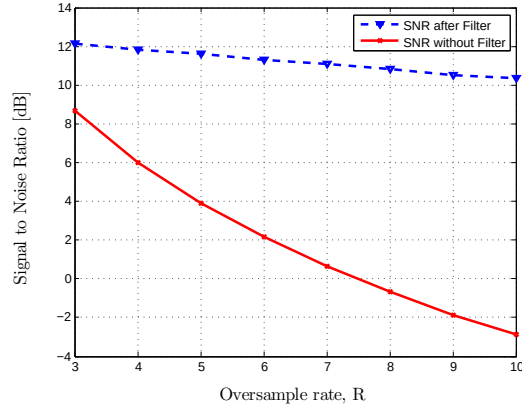


Figure 3.7: The SNR presented to the detector with and without a 2nd-order LPF.

3.5.2 ADC Resolution Requirements

The ADC which follows the LPF and precedes the detector is another critical component. A high-resolution (i.e. many-bit) design is of course ideal as it gives the ensuing digital processor access to an accurate representation of the capture signal; unfortunately high-resolution also imposes many sacrifices (high-cost, high-power, low-speed, difficult to scale, etc.) that can acutely compromise the performance of a high-speed real-time signal measurement system. Thus a detection system robust against low-resolution signal samples can be of significant benefit to our NBS aspirations. The RC algorithm provides such functionality.

One key measure of assessment for our RC algorithm is the transition error rate (TER). The TER provides a measure of the proportion of an event's duration that

is incorrectly predicted normalized to the shortest possible dwell time (as effectively denoted by R). It conveys information about the degree to which event dwell time's are compromised by a detection scheme and is ultimately a quantification of its ability to localize abrupt changes. Formally, we calculate this metric with

$$\text{TER} = \frac{\text{total number of incorrect samples}}{\text{total number of events}} \cdot \frac{1}{R} \quad (3.16)$$

where the first ratio to the right of the equality compares the total number of incorrectly detected samples (i.e. mapped to the wrong signal level $\in \{-1, -1/3, +1/3, +1\}$ at the CUSUM detector output) to the total number of event levels processed over the length of some measured input data stream. This ratio is related to the proportion of an event's duration (i.e. its dwell time) that will be incorrectly identified. For fairness this should be normalized to the oversample rate, R , since higher sampling rates obviously capture more samples of an event and hence reduce the impact of any one sample detection error.

The TER performance of our RC algorithm as a function of the oversample rate, R , under a variety of ADC resolutions (with the 2-MHz 2nd order LPF discussed above present) is shown in Fig. 3.8. Beside RC's TER for an ideal ADC we also show the performance impact of coarse 2-bit, 3-bit and 6-bit ADCs. Clearly, the RC algorithm is very forgiving of ADC coarseness as the increase in TER from perfect to 2-bit resolution is, at worst, less than 10% (at $R = 5$) and still approximates dwell times (relative

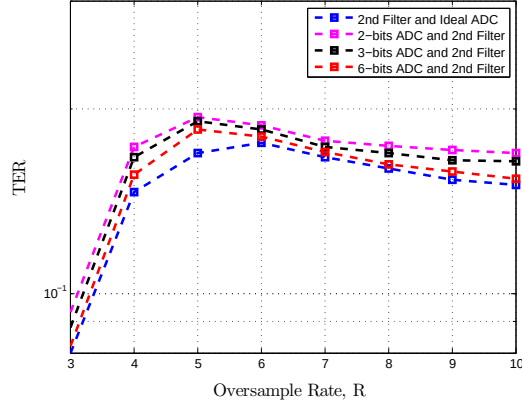


Figure 3.8: The RC algorithm’s transition error rate as a function of the oversample rate under different ADC resolution settings.

to minimum pulse durations) with greater than 90% accuracy (at $R = 3$). RC’s TER also suffers a degradation of roughly 50% as the oversample rate increases from 3 to 5 followed by a relatively stable albeit inferior performance at high R . The reason for this stems from the simple fact that higher operating rates sample more of the violet noise spectrum relative to the signal and hence compromise the detector; as R increases the decision-directed policy is better able to map its estimates to the correct level, but does not manage to return to the previous levels of operation. For white noise and ideal brickwall filtering beyond f_s RC TER performance improves with R .

To reference RC’s TER performance to the reported state-of-the-art in the nanopore literature [33] we provide the comparison shown in Fig. 3.9. In particular the 2-bit and ideal ADC performance of RC is placed along-side DSC’s results under the same

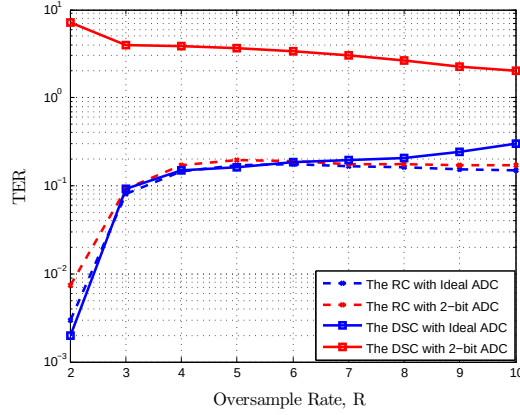


Figure 3.9: The TER comparison between two CUSUM algorithms.

conditions. Under ideal circumstances the two approaches track quite closely, however with a 2-bit ADC presence RC demonstrate at $20\times$ TER improvement over DSC.

The data rates imposed by nanopore applications (roughly 1-MHz in state-of-the-art solid-state realizations) are not overly stressful in the context modern CMOS technology and hence even oversampling by a factor of $10\times$ does not, over a single channel, present a serious implementation issue. For example, to adequately monitor past events may only require a memory of $R\times$ the ADC bit-resolution. Over potentially 1000s of channels this may eventually be a factor for implementation should ADC's on the order or 16-bits be utilized. However the ability of the RC to operate at coarse resolutions significantly mitigates this.

To convey another impression of the RC and DSC performance characteristics time-domain examples of the two algorithms at work under with a 3-bit ADC present

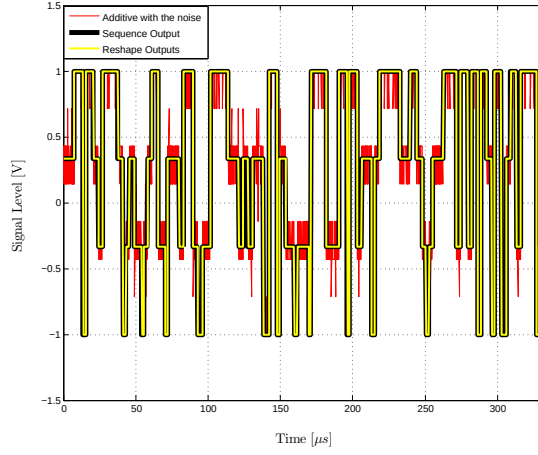


Figure 3.10: A time-domain example of the RC algorithm’s signal recovery characteristics assuming a 3-bit ADC.

are shown in Fig. 3.10 (RC) and 3.11 (DSC). The black line in the plots refers to the underlying ideal signal input (i.e. the baseline), the red line refers to the noise corrupted sampled signals after quantization and the yellow trace refers to the detector (RC or DSC) output. Although the level-prediction characteristics are not obvious to follow in this plot, the superiority of RC in aligning results (yellow) to the underlying signal (black) over time is clear.

3.5.3 Bit Error Rate and Threshold Sensitivity

Another critical high-speed NBS detector performance metric is the BER already discussed in Section 3.4. The ability of CUSUM algorithms to optimize this aspect of

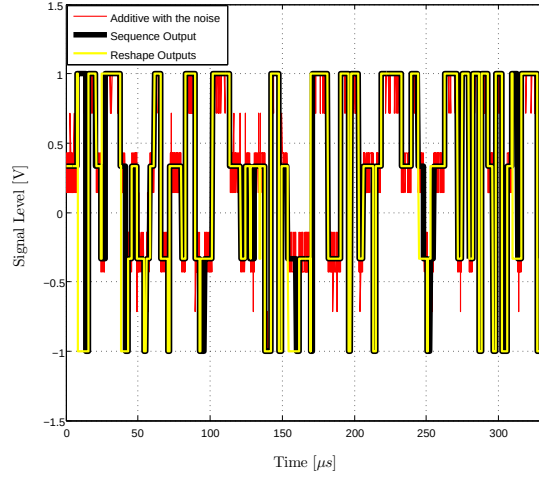


Figure 3.11: A time-domain example of the DSC algorithm’s signal recovery characteristics assuming a 3-bit ADC.

performance relies not only in their estimation mechanisms (e.g. the statistic test), but also in their decision threshold, h , setting. The optimum threshold setting for DSC has already been mentioned in Section 3.3 and, as shown in (3.8), depends on both the minimum expected signal transition and the noise level. The decision-directed mapping strategy employed by RC removes this dependency on noise allowing its performance to be more forgiving of the threshold setting as discussed in Section 3.4.

In Fig. 3.12, the BER performance as a function of h for the RC and DSC algorithms is shown (simulation settings are indicated in the figure). The red dots highlight the optimal and coarse threshold settings discussed in Section 3.5 for the DSC and RC, respectively. As the value of h is varied, significant degradations in DSC performance

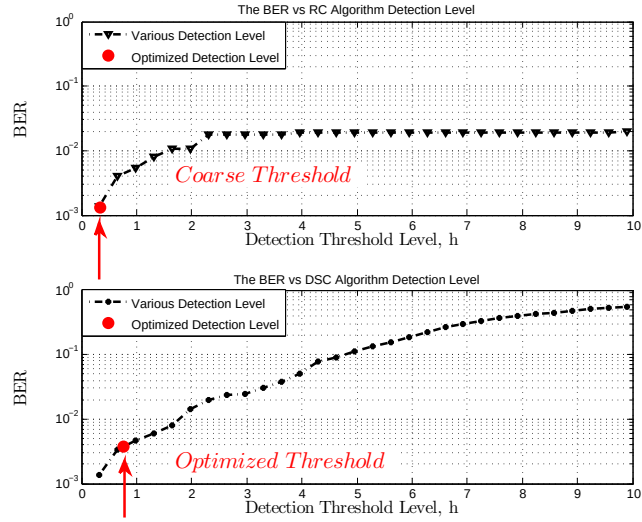


Figure 3.12: The detection threshold level comparison between the two CUSUM algorithms (2nd order LPF, ideal ADC, $R = 3$).

are apparent, unlike the RC.

Chapter 4

Analog Front-End (AFE) Design

4.1 Transimpedance Amplification

The AFE’s fundamental task is to convert the raw electronic pore signals into digital samples of appropriate signal quality. The signal-to-noise ratio (SNR) at the output of the AFE serves as the measure of “quality” and the “appropriateness” of the level reached by this value depends on the downstream processing (e.g. DBE, base caller, aligner, consensus caller, etc.) and accuracy required by the application.

The vast diversity in decision algorithms and end-applications can make AFE requirements highly variable. As an idealized reference, assuming that the DBE employs only a basic maximum likelihood (ML) detection scheme a SNR of roughly 12-dB is needed to obtain a base caller with a 10^{-4} error rate [25]; such a performance level should be sufficient for large-scale genome assembly. To avoid over-specification, in

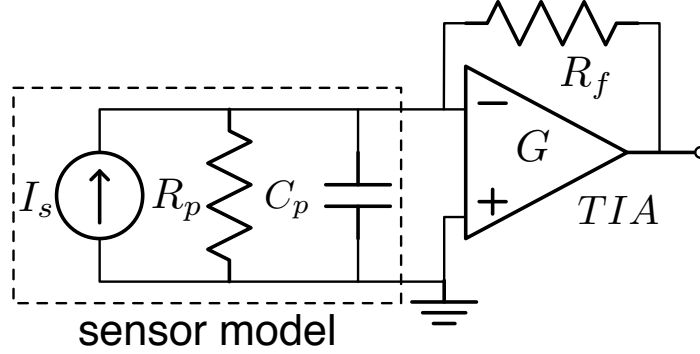


Figure 4.1: An illustration of a transimpedance (TIA) amplification

the following I will present a general AFE design strategy (followed by a specific CMOS example) amenable to adjustment for more specialized scenarios.

The core AFE function outlined above can be more specifically stated as the job of converting a weak current signal to some voltage-equivalent that is sufficient for digitization. As is well known, this task can be addressed with a transimpedance (TIA) amplification stage as sketched in Fig. 4.1.

The transfer function of this scheme can be approximated with

$$\frac{V_{out}}{I_s} \approx \frac{-R_f}{1 + sR_f C_{input}/G} \quad (4.1)$$

where G denotes the TIA op-amp's voltage gain and where $C_{input} = C_p + C_i$, the sum of the pore's capacitance as well as the input capacitance, C_i , of the amplifier itself. To adequately process event rates, f , we expect the need to set the closed-loop pole such

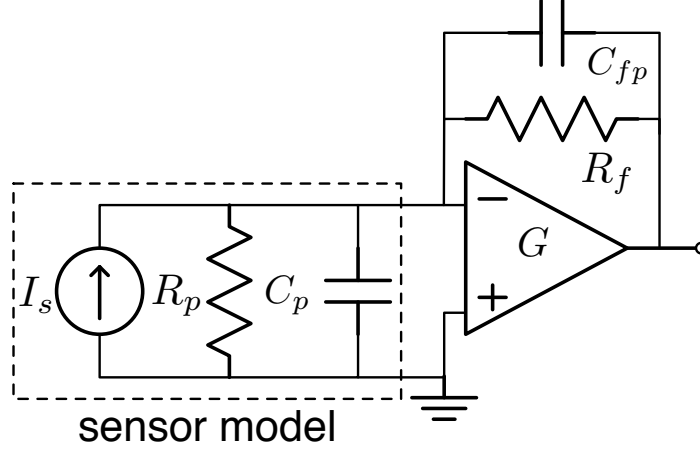


Figure 4.2: An illustration of the parasitic capacitance associated with R_f

that $G/R_f C_{input} > f \times 2\pi$.

Although straightforward, this approach is made very challenging by the high R_f required to produce an output voltage of sufficient magnitude. In particular, the low I_s emerging from the nanopore typically requires $R_f \gtrsim R_p$ to achieve adequate gain for the ADC. This is quite a high setting given the electrical equivalent of the typical nanopore where R_p ranges roughly between 100–1000 M Ω . This coupled with a potentially substantial C_{input} then requires a very high G and associated gain-bandwidth product (GBW) to establish a closed-loop response pole at even rates in the MHz-range needed to handle high-speed solid-state nanopore signals.

Critically, any parasitic capacitance associated with R_f (see Fig. 4.2) itself intro-

duces a feedforward pole around the amplifier from input to output. It can be shown that such a feedforward pole appears as a pole in the closed-loop gain expression factored (i.e. increased) by G and hence leads to

$$\frac{V_{out}}{I_s} \approx \frac{-R_f}{sR_f(C_{input} + C_{fp})/G + sR_fC_{fp}} \quad (4.2)$$

where clearly the influence of R_fC_{fp} is dominant given a large G .

Not only does this further compromise the frequency response and stability, but also undermines design robustness given its parasitic origins and their unpredictable nature. It is arguably this latter point that causes the most concern for design.

4.1.1 Integrator-Differentiator-Gain Cascade

The limitations noted above have a long history. Indeed they were encountered in patch clamp amplifiers for cellular recording, a field with a strong influence on electronics design in the nanopore domain [37]. An approach arising from this field employed a two-stage amplification cascade whose first element purposely imposed a low-frequency pole well below the amplifier's GBW and whose second stage corrected for this with the introduction of a low-frequency zero.

As such, this method acknowledges the need for a high feedback resistance R_f , but accompanies it with a known shunt capacitance C_f that marginalizes the impact

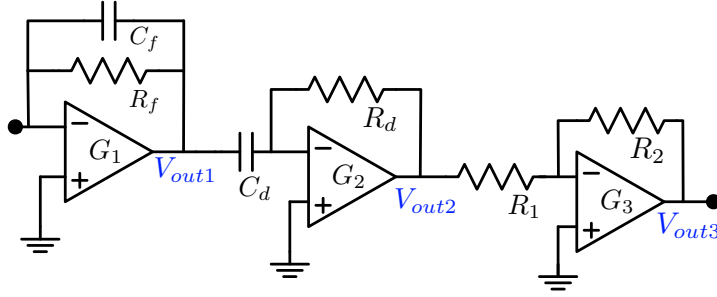


Figure 4.3: Integrator-differentiator AFE cascade.

of variable parasitic contributions from C_{fp} . In effect an integrator function is approximated and thus the bandwidth is purposely sacrificed for robustness. A workable frequency response is then regained by the addition of a differentiator following the integrator as noted immediately above.

In accordance with the above strategy, a schematic of a system adjusted for high-speed solid-state nanopore applications is shown in Fig. 4.3. This three-stage circuit consists of the aforementioned low-pass (integrator approximation) to high-pass (differentiator approximation) cascade followed by a third stage for gain tuning. The transfer functions of the constituent amplifiers are denoted by G_1 , G_2 , and G_3 .

The transfer function of the integrator stage is

$$\frac{V_{out1}}{I_{in}} = \frac{G_1 \cdot R_{dc}}{1 + (C_p + C_i)R_{dc}s + G_1(1 + sC_iR_{dc})}, \quad (4.3)$$

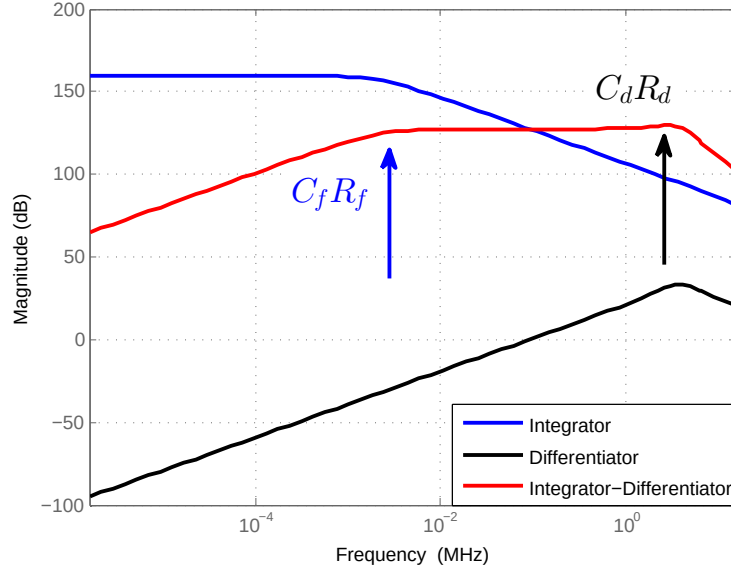


Figure 4.4: Frequency response of the integrator-differentiator AFE.

The second-stage differentiator's transfer function is

$$\frac{V_{out2}}{V_{out1}} = \frac{C_d R_d G_2 s}{1 + G_2 + C_d R_d s}. \quad (4.4)$$

The transfer function of the third gain stage is

$$\frac{V_{out3}}{V_{out2}} = \frac{R_2 G_3}{R_1 + R_2 + R_1 G_3}. \quad (4.5)$$

The transfer function of the system is shown in Fig. 4.4. Through its use of lead compensation the integrator marginalizes the $R_f C_{input}$ contribution instead creating the $R_f C_f$ pole at low frequencies well below even a low-power amplifier's GBW. The differentiator then recovers the bandwidth needed to sustain the desired event rate.

Without the burden of the nanopore equivalent circuit, the design of the differentiator is simplified relative to that of the integrator. Typically, layout considerations restrict the net size of the differentiator's C_d and R_d . In particular, limiting $C_d < 1$ pF prevents a complete recovery of the integrated signal. This is corrected by the final gain stage in Fig. 4.3.

4.2 AFE CMOS Chip Design and Performance

4.2.1 Circuit Design

As with the majority of signal processing chains the first stage — here, the integrator amplifier — plays a key role because of its magnified influence on the noise factor, bandwidth, and sensor DC bias. In this case, the basic two-stage op-amp (Fig. 4.5 with associated device width-to-length ratios shown) implemented in a 0.13- μm CMOS technology is sufficient as the underlying active component even for high-speed event rates, a reflection of the design relaxation allowed by the integrator-differentiator pair.

According to the small-signal simulation shown in Fig. 4.7, the integrator amplifier demonstrates around 34 dB gain and a flat response within 20 MHz; this results in a gain bandwidth product of 1-GHz.

Although a purely capacitive feedback term would succeed in more closely ap-

proximating an ideal integrator, its use for high f applications (with proportionally little signal content at low frequencies) is not warranted as either extra switching circuitry would be needed or sophisticated DC conductance elements [21] introduced to deal with streaming signals.

Fig. 4.7 shows the small-signal simulations of the integrator and the differentiator. As we can see, the differentiator amplifier has wider (i.e. higher frequency) flat bandwidth response than the integrator. This is because we would like to achieve the flat closed-loop response in a certain bandwidth (e.g. 2 kHz - 3 MHz) as shown in Fig. 4.4. Applying the integrator op-amp design to the differentiator will create complex poles due to the presence of the R_d and C_d pair and thus compromise the desired flat frequency response at the output of the differentiator.

In order to avoid this problem, we make the diff-pairs of the differentiator's op-amp have smaller size to achieve larger flat bandwidth and for the second stage of that (differentiator) op-amp a gain compensation is made. In essence, we separate the poles of the differentiator's op-amp and the $R_d C_d$ to make sure to achieve a flat frequency response in the frequency domain and achieve around 80° phase margin for the integrator and 60° phase margin for the differentiator which are shown in the Fig. 4.8.

An NMOS input pair is chosen in order to minimize the amplifier's input capaci-

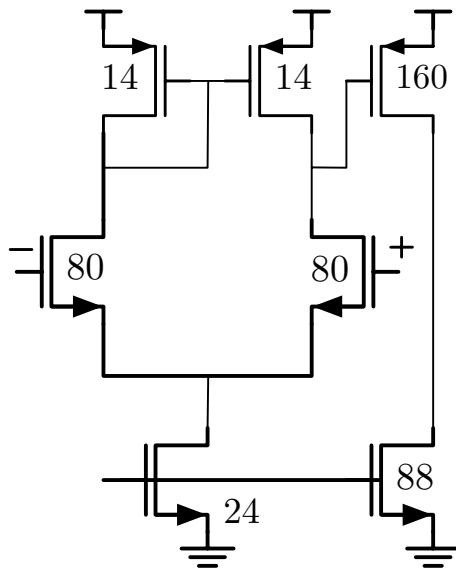


Figure 4.5: The integrator op-amp.

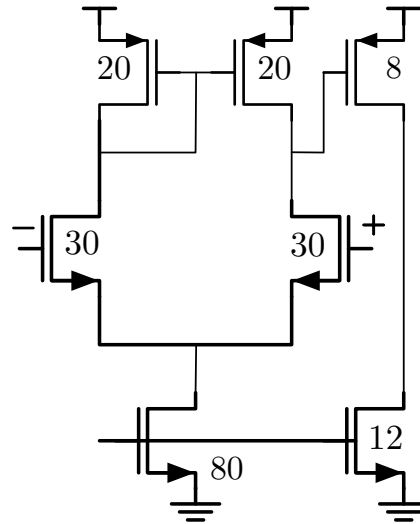


Figure 4.6: The differentiator op-amp.

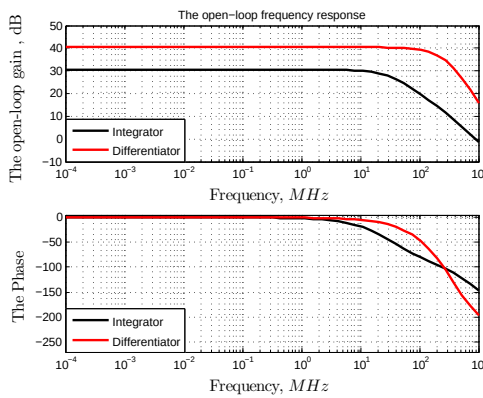


Figure 4.7: The open-loop frequency response of the op-amp (integrator and differentiator).

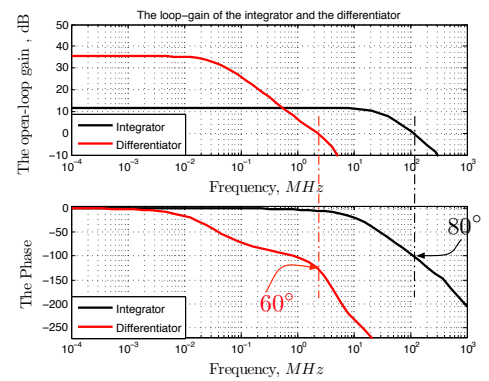


Figure 4.8: The loop-gain of the integrator and differentiator.

R_f , in the hundreds $M\Omega$ range. As mentioned earlier, this is needed to achieve the gain in light of the high pore resistance R_p .

Since there are significant technological limitations of implementing such a high value resistor in a small silicon area, it has been implemented with a linear transconductor circuit [38] in this work. The core part of this proposed architecture in Fig. 4.9 is that it has source-well and drain-gate short circuited. It means that when the V_{gs} is positive, the drain-well voltage of the PMOSs (T_1 AND T_2) are forward bias like typical (p-n) diodes. The Equation 4.8 shows how to calculate the drain current when the voltage of the gate is higher than the source.

$$I_D = J_{S0}[2TE + W(2T + E)](e^{\frac{V_{gs}}{V_T}} - 1) \quad (4.7)$$

Where J_{S0} is the junction saturation current per unit-area, W and L refer to the width of the transistor and the T and E are referring to the length and width of the diffusion area. Note that $W \gg T$ and $W \gg E$, thus the drain current is always proportional to the width of the transistor and won't be influenced by the length of the transistor. Due to the two MOS-bipolar pseudo-resistors operating with same gate-source voltage, the drain current different between two MOS-bipolar will be determined by the width ratios of them like $I_{D1}/I_{D2} = W_1/W_2 = M$. This important characteristic has been used to design an accurate linear current divider that is ideal for the realization of high performance transconductors. Thus, the full circuit of Fig. 4.9, including the resistor

R_{in} , defines a linear transconductor system which can be expressed as

$$g_m = \frac{I_{out}}{V_{in}} = \frac{1}{R_{in}M} \quad (4.8)$$

4.2.2 Performance Comparison

A comparison of the AFE to some advanced published circuits [16, 21] for NBS applications is shown in Table 4.1.

Firstly, the AFE layout (without ADC) is shown in Fig. 4.10. As we can see, our whole RC-extracted AFE dissipates 12.7 mW from a 1.5-V supply and occupies $402 \times 40 \mu\text{m}^2$. The present AFE area is $21 \times$ smaller with $3.5 \times$ less power dissipation than the system reported in [21] (in $0.35\text{-}\mu\text{m}$ CMOS) while the AFE's integrator stage is $12 \times$ smaller and $2.5 \times$ lower power than the like discussed in [16]. The present AFE integrator's input referred noise is also improved over its nanopore counterpart demonstrating an average spot noise (averaged over 10 kHz – 10 MHz) of $3.93 \text{ nV}/\sqrt{\text{Hz}}$ against $5 \text{ nV}/\sqrt{\text{Hz}}$ [16] and $3 \text{ nV}/\sqrt{\text{Hz}}$ in [21].

Besides the comparisons above, the small-signal and transient simulations of the extracted AFE with various corner processes are shown in Figs. 4.12 and 4.13. For the simulations a sensor model with $R_p = 100 \text{ M}\Omega$ and $C_p = 5.12 \text{ pF}$ is used. Fig. 4.12 shows the AFE's transimpedance gain which demonstrates a flat 165-dB response for 2 kHz – 3 MHz which is approximately $10 \times$ better speed than the state-of-the-art

Table 4.1: Summary Comparisons among three AFEs

	Our AFE Design	Transimpedance Ampli- fier(Rosenstein)	Transimpedance Ampli- fier(Giorgio Ferrari)
Technology	0.13 μ m CMOS	0.13 μ m CMOS	0.35 μ m CMOS
Bandwidth	3 MHz	1 MHz	2 MHz
Power supply	1.5 V	1.5 V	± 1.5 V
Power Consumption of the Integrator Stage	2.335 mW	5 mW	unknown
Core Area	0.016 mm ²	0.2 mm ²	0.34 mm ²
Input Voltage Noise	3.93 nV/ $\sqrt{Hz}$	5 nV/ $\sqrt{Hz}$	3 nV/ $\sqrt{Hz}$

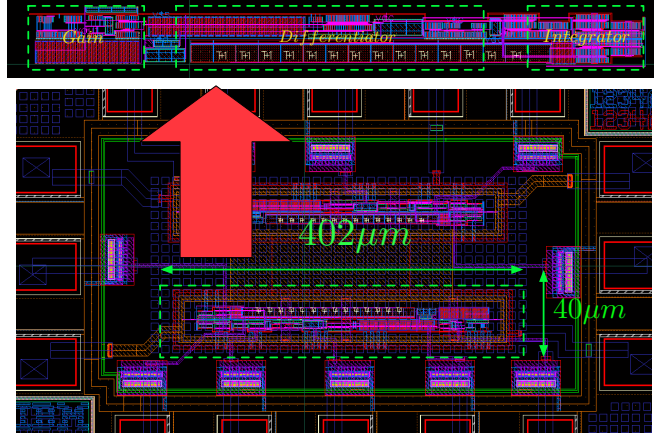


Figure 4.10: The AFE layout.

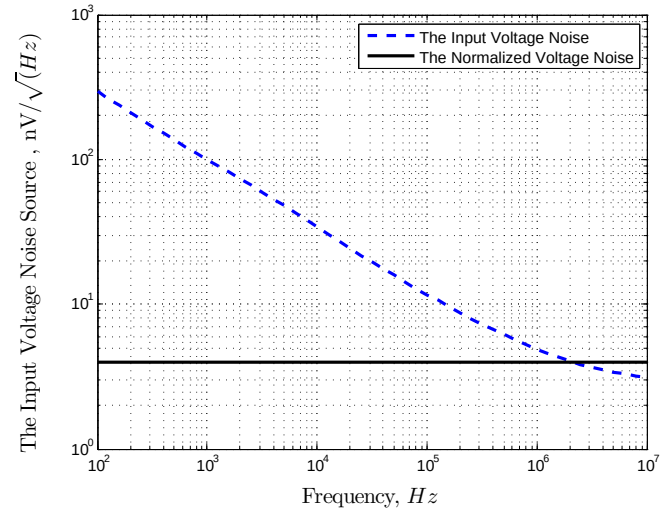


Figure 4.11: An illustration of the Input voltage Noise

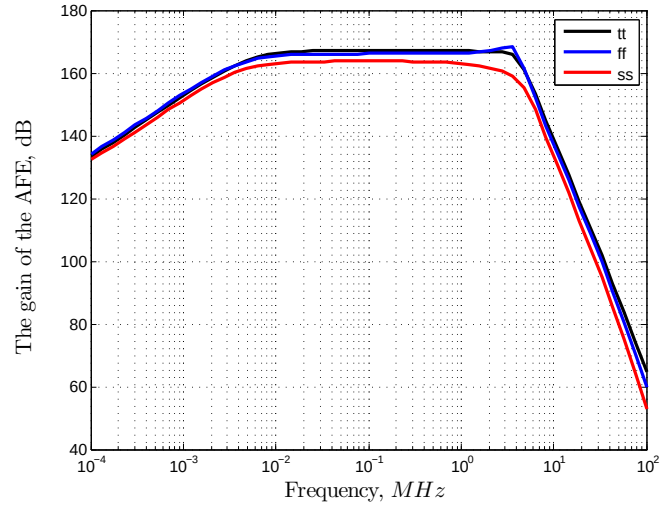


Figure 4.12: AFE frequency response.

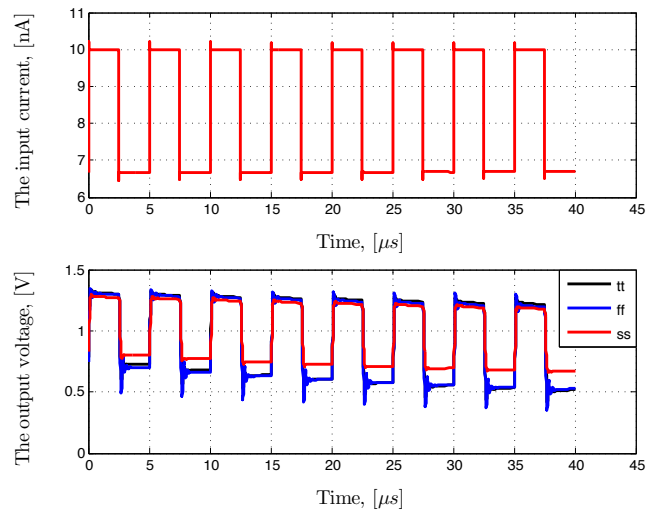


Figure 4.13: AFE transient response.

designs [39, 40]. The transient behaviour example in Fig. 4.13 shows the voltage response to an input square wave current (200 kHz, 3.5 nA).

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In this thesis I have introduced a more robust algorithm for the real-time detection of high-speed translocation data from nanopores and also proposed a variety of circuit and system approaches to high-speed nanopore mixed-signal signal processing ultimately needed to achieve the base calling function of the sequencing pipeline.

Firstly, the approach has shown the potential to handle 4-level nanopore signals with event rates of 2×10^6 nt/s and only a 2-bit ADC at transition error rates (TER) $\approx 2 \times 10^{-3}$ with similar levels reached for the BER. Assuming a measurement chain as it might appear in a typical embedded CMOS implementation we highlighted the critical impact of violet noise on the nanopore measurements at speeds exceeding 10^6 nt/s. A number of steps can be taken in the nanopore measurement chain to mitigate this

problem and thus extract the underlying signal with better accuracy; these include a number of hardware choices such as improved TIA design, superior filtering, high-resolution ADC all of which incur greater cost and limit the potential for arrayed sensor embodiments. In light of this, improved real-time detection algorithms are valuable as means of improved accuracy without added cost.

In terms of the hardware design, a mature 130-nm CMOS technology offers the possibility of improving on reported designs and thus achieve a three-orders increase in nanopore processing speed. In addition roughly a $10\times$ reduction in analog front-end area has been shown accompanied by at least a $2\times$ drop in power consumption and 25% improvement in noise performance. At the same time a digital event identification scheme has been described with the ability to reduce error rates by at least $3\times$.

In a word, the presented cumulative-sum detection algorithm in this thesis achieves good accuracy under the high-noise and low ADC resolution constraints by employing a decision-directed policy and correction (“reshaping”) strategy. It has shown superior performance to a contemporary real-time nanopore detection technique in both its event level of and dwell time predictions and also possess greater tolerance to changes in its decision threshold and it will be more compatible with our analog front-end design.

5.2 Future Work

There are still several developments that should be employed in the future after this work. The first is about the introduced cumulative-sum detection algorithm which has already demonstrated good performance in the simulations. The clear next step is to try to implement the whole detector scheme into hardware and do the test at the same time. The easiest way is to start with the field-programmable gate array (FPGA) and then implement it into a chip for the purpose of parallel arrays in the future.

Due to the time restrictions, the same thing happens to the AFE chip as well. As the thesis mentioned, the post layout simulation is done in Cadence but the better way is to test it with the real NBS system. Finally, we need to make a whole system consisting of the AFE chip compatible with the RC algorithm detection chip to finish the whole base calling.

Bibliography

- [1] W. Saenger. Springer-Verlag, 1984, ISBN: 0-387-90762-9.
- [2] B. Alberts, A. Johnson, J. Lewis, M. Raff, K. Roberts, and P. Walter. Garland Science, 2002, ISBN: 0-8153-3218-1.
- [3] C. T. and J. Schultz, “Pentose nucleotides in the cytoplasm of growing tissues,” *Nature.*, vol. 143, pp. 602–603, 1939.
- [4] T. G. Project, “Genetics overview,” <https://genographic.nationalgeographic.com/science-behind/genetics-overview/>, 2015, [Online; accessed 8-Nov.-2015].
- [5] S. F, N. S, and C. AR, “DNA sequencing with chain-terminating inhibitors,” *Proc Natl Acad Sci U S A.*, vol. 12, pp. 5463–7, 1977.
- [6] S. Tripp and M. Grueber, “Economic impact of the human genome project,” Natelle Memorial Institute, Tech. Rep., May 2011.

- [7] B. Ewing and P. Green, “Base-calling of automated sequencer traces using phred. II. error probabilities,” *Genome Research*, vol. 8, pp. 186–194, 1998.
- [8] R. J. and e. Bruyns E., “Massively parallel signature sequencing MPSS as a tool for in-depth quantitative gene expression profiling in all organisms,” *Brief Funct Genomic Proteomic*, vol. 1(1), pp. 95–104, 2002.
- [9] M. Margulies, M. Egholm, and W. E. Altman, “Genome sequencing in microfabricated high-density picolitre reactors,” *Nature.*, vol. 437, pp. 376–380, 2005.
- [10] M. Kircher and J. Kelso, “High-throughput DNA sequencing—concepts and limitations,” *Bioessays*, vol. 32(6), pp. 524–536, 2010.
- [11] E. E. Schadt, S. Turner, and A. Kasarskis, “A window into third-generation sequencing,” *Hum. Mol. Genet.*, vol. 19, no. R2, pp. 227–240, Nov. 2010.
- [12] J. Li, M. Gershow, and D. Stein, “DNA molecules and configurations in a solid-state nanopore microscope,” *Nature Materials*, vol. 2, pp. 611–615, Aug. 2003.
- [13] C. A. Merchant and e. Ken Healy, “DNA translocation through graphene nanopores,” *Nano Lett.*, vol. 10, no. 8, pp. 2915–2921, Nov. 2010.
- [14] K. Venta, M. Wanunu, and M. Drndi, “Electrically controlled nanoparticle synthesis inside nanopores,” *Nano Lett.*, vol. 13, no. 12, pp. 423–429, Jan. 2013.

- [15] J. K. Rosenstein, S. Ramakrishnan, and J. Roseman, “Single ion channel recordings with CMOS-anchored lipid membranes,” *Nano Lett.*, vol. 13(6), pp. 2682–2686, May 2013.
- [16] J. K. Rosenstein, M. Wanunu, C. A. Merchant, M. Drndic, and K. L. Shepard, “Integrated nanopore sensing platform with sub-microsecond temporal resolution,” *Nature Methods*, vol. 9, pp. 487–492, Feb. 2012.
- [17] A. S. Mikheyev and M. M. Y. T. In, “A first look at the oxford nanopore minION sequencer,” *Molecular Ecology Resources*, vol. 14, no. 6, pp. 1097–1102, Nov. 2014.
- [18] N. J. Loman, J. Quick, and J. T. Simpson, “A complete bacterial genome assembled de novo using only nanopore sequencing data,” *Nature Methods*, vol. 12, pp. 733–735, May 2015.
- [19] K. Venta and e. Gabriel Shemerand Matthew Puster, “Differentiation of short, single-stranded DNA homopolymers in solid-state nanopores,” *ACS Nano*, vol. 7, no. 5, pp. 4629–4636, May 2013.
- [20] Y. Huang, S. Magierowski, G.-Z. Ebrahim, and W. Chengjie, “High-speed event detector for embedded nanopore bio-systems,” pp. 4110–4113, 2015.

- [21] G. Ferrari, F. Gozzini, A. Molari, and M. Sampietro, “Transimpedance amplifier for high sensitivity current measurements on nanodevices,” *Review of Scientific Instruments*, vol. 44(5), pp. 1609–16, May 2009.
- [22] S. Kowalczyk, A. Grosberg, Y. Rabin, and C. Dekker, “Modeling the conductance and DNA blockade of solid-state nanopores,” *Nanotechnology*, vol. 31, Aug. 2011.
- [23] A. Balan, B. Machielse, and D. Niedzwiecki, “Modeling the conductance and DNA blockade of solid-state nanopores,” *Nano Lett.*, vol. 14(12), pp. 7215–7220, Nov. 2014.
- [24] V. Tabard-Cossa, D. Trivedi, M. Wiggin, N. Jetha, and A. Marziali, “Noise analysis and reduction in solid-state nanopores,” *Nanotechnology*, vol. 18, pp. 1–6, June 2007.
- [25] S. Magierowski, S. Islam, Y. Huang, and E. Ghafar-Zadeh, “CMOS-based high-speed nanopore recording: Signals and systems,” in *EMBC (36th)*, Aug. 2014, pp. 1563–1566.
- [26] D. Kim, N. Haven, B. Goldstein, and e. Wei Tang, “Noise analysis and performance comparison of low current measurement systems for biomedical applications,” *Biomedical Circuits and Systems*, vol. 7, no. 1, pp. 52–62, Feb. 2013.

- [27] R. M. M. Smeets, N. H. Dekker, and C. Dekker, “Low-frequency noise in solid-state nanopores,” *Nanotechnology*, vol. 20, pp. 1–4, Feb. 2009.
- [28] R. J. S. K.L., “Temporal resolution of nanopore sensor recordings,” pp. 4110–4113, 2013.
- [29] B. Sklar, *Digital Communications: Fundamentals and Applications*, 2nd ed. Prentice Hall, Jan. 2001.
- [30] V. Tabard-Cossa and D. Trivedi, “Noise analysis and reduction in solid-state nanopores,” *Nanotechnology*, vol. 18(30), June 2007.
- [31] S. R., K. U., and D. N., “Noise in solid-state nanopores,” *Current Issue*, vol. 105(2), pp. 417–421, Jan. 2008.
- [32] E. S. Page., “Continuous inspection schemes,” *Biometrika*, vol. 41, no. 1, pp. 100–115, June 1954.
- [33] C. Raillon, P. Granjon, M. Graf, L. J. Steinbock, and A. Radenovic, “Fast and automatic processing of multi-level events in nanopore translocation experiments,” *Nanoscale*, vol. 4, no. 16, pp. 4916–4924, Aug. 2012.
- [34] D. M. Hawkins and D. Olwell, *Cumulative Sum Charts and Charing for Quality Improvement*. Springer Verlag, 1998.

- [35] Y. Huang, S. Magierowski, G.-Z. Ebrahim, and W. Chengjie, “A high-speed real-time nanopore signal detector,” in *CIBCB 2015*, Aug. 2015, pp. 1–8.
- [36] H. W. H. III and T. G. Szymanski, “A fast algorithm for computing longest common subsequences,” in *CACM 20*, 1977, pp. 350–353.
- [37] F. J. Sigworth, *Single-Channel Recording*, B. Sakmann and E. Neher, Eds. Springer US, 1995.
- [38] F. Gozzini, G. Ferrari, and M. Sampietro, “Linear transconductor with rail-to-rail input swing for very large time constant applications,” *Electronics Letters*, vol. 42(19), pp. 1069 – 1070, Sept. 2006.
- [39] J. Kim, G. Wang, B. D. William, and K. Pedrotti, “An integrated patch-clamp amplifier for ultra-low current measurement on solid-state nanopore,” *International SoC Design Conference*, Aug. 2010.
- [40] J. Kim, R. Maitra, and W. B. Dunbar, “A patch-clamp ASIC for nanopore-based DNA analysis,” *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7(3), June 2013.