

**MODULAR HIGH-DR ARTIFACT-RESILIENT
WEARABLE EEG HEADSET WITH DISTRIBUTED
PULSE-BASED FEATURE EXTRACTION AND
MULTIPLIER-LESS NEUROMORPHIC BOOSTED
SEIZURE DETECTION**

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Abstract

Wearable electroencephalography (EEG) headsets have emerged as a promising technology with the potential to revolutionize outpatient diagnostics. These devices offer real-time insights into the neurological activity of the brain, paving the way for more precise and personalized treatment strategies. One of the critical factors in the success of these diagnostic headsets is their energy-efficient design, especially for long-term recording applications.

Typically, diagnostic headsets consist of multiple active electrodes (AEs) equipped with embedded electronics for functions like amplification and quantization. These electrodes are connected to a central back-end (BE) unit responsible for data processing and, if needed, wireless transmission. A comprehensive analysis of the current state of the art in this field reveals that power consumption in systems with a sufficiently high dynamic range (DR) analog front-end (AFE) and a data-driven classifier, such as a nonlinear support vector machine (NL-SVM) for seizure detection, is mainly dominated by three main components: the AFE (48%), AE-to-BE data communication (26%), and the signal processing required for seizure detection (21%). This underscores the necessity of taking a holistic approach to enhance the efficiency of these key components for an overall energy-efficient design.

This study presents design, development and experimental characterization of a channel-count-scalable modular fully-flexible platform which achieves motion-artifact-resilient 80dB-DR EEG recording and highly-accurate, energy-efficient seizure detection. The innovation lies in a series of strategies that collectively result in a remarkable 72% reduction in overall power consumption: 1) performing feature extraction (FE) in each AE (i.e., distributed) resulting in 99% reduction in AE-to-BE data communication power, 2) using an ultra-low-power pulse-based method for FE resulting in 92% reduction in its power, 3) performing classification using a neuromorphic multiplier-less boosted-SVM that achieves a comparable accuracy to a resource-intensive NL-SVM while consuming 98% less power, 4) adopting an auto-ranging scheme in the AFE that leads to >17dB DR improvement, 5) employing an AE-specific-boosted distributed feed-forward common-mode rejection (CMR) enhancement method achieving >80dB CMRR in the presence of $1\text{M}\Omega$ AE-to-AE input impedance

(Zin) mismatch (89dB without mismatch), and 6) an AE-specific electrode-tissue impedance (ETI)-correlation-based circuit for motion artifact detection and suppression.

To my parents and sister, for their endless kindness and support

To my wife, the love of my life

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List of Abbreviations

ADC: Analog-to-Digital Converter

AE: Active Electrode

AFE: Analog Front-End

BLE: Bluetooth Low Energy

BPF: Band-Pass Filter

BW: Bandwidth

CM: Common Mode

CMRR: Common-Mode Rejection Ratio

DAC: Digital-to-Analog Converter

DC: Direct Current

DEM: Dynamic Element Matching

DRL: Driven Right Leg

DSP: Digital Signal Processing

DSM: Delta-Sigma Modulator

ECG: Electrocardiography

EEG: Electroencephalography

EMG: Electromyography

ESL: Element Selection Logic

ETI: Electrode-Tissue Impedance

EXG: External Electrography (Generic Term for Electrical Recording from the Body)

FAR: False Alarm Rate

FIR: Finite Impulse Response

FPGA: Field-Programmable Gate Array

GTCA-SVM: Guided Time-Channel Averaging Support Vector Machine

HD-EEG: High-Density Electroencephalography

IIR: Infinite Impulse Response

IIRN: Integrated Input Referred Noise

IDAC: Current-Mode Digital-to-Analog Converter

ICA: Independent Component Analysis

LSB: Least Significant Bit

MAC: Multiplication and Accumulation

MSB: Most Significant Bit

NL-B-SVM: Non-Linear Boosted Support Vector Machine

NTF: Noise Transfer Function

OTA: Operational Transconductance Amplifier

PAC: Periodic Alternating Current

PCB: Printed Circuit Board

RBF: Radial Basis Function

SAR ADC: Successive Approximation Register Analog-to-Digital Converter

SBE: Spectral Band Energy

SFDR: Spurious-Free Dynamic Range

SNDR: Signal-to-Noise and Distortion Ratio

SNR: Signal-to-Noise Ratio

SoTA: State-of-the-Art

SRAM: Static Random-Access Memory

STF: Signal Transfer Function

SVM: Support Vector Machine

TCA: Time Channel Averaging

THD: Total Harmonic Distortion

UGBW: Unity-Gain Bandwidth

VCM: Common-Mode Voltage

VDD: Supply Voltage

VRES: Residual Voltage

V/V: Voltage Gain (Volts per Volt)

$\mu\mathbf{V}_{RMS}$: Microvolts Root Mean Square

Chapter 1

Introduction

1.1 Motivation

Epilepsy, one of the most common neurological diseases globally, affects approximately 70 million people worldwide [1]. It manifests as recurrent synchronous bursts of electrical discharge in the brain, commonly referred to as seizures [2]. These seizures differ significantly between individuals in terms of occurrence rate, duration, magnitude, and symptoms. Currently-available options for epileptic patients include pharmacological solutions [3, 4], surgery [5, 6], and neuro-stimulation [7, 8]. Effectively monitoring the occurrence and severity of seizures represents a valuable approach that can substantially enhance the effectiveness of all these solutions.

For patients under medication, the dosage and frequency of drug administration should ideally be specifically tailored based on the severity, frequency, and type of seizures experienced. Current practices involve using the patient's diary entries and responses to behavioral

questions as tools for prescribing the correct dosage of medication [9]. However, this subjective approach has substantial drawbacks, for example, the risk of overlooking seizures occurring during sleep and a lack of precise information for infants.

Brain resection surgeries are performed to remove a segment of brain that is believed to be where seizures are originated for a specific patient. Accordingly, it requires the accurate positioning of the seizure focus, which is typically established through various imaging techniques. Considering the highly-infrequent occurrence rate of seizures (e.g., from a few per day to once a week), patients are often subjected to methods that induce seizures, such as sleep deprivation and photic stimulation, while being tethered to a recording setup for continuous monitoring, which is exceedingly discomforting for the patient and could result in extended hospital stays (i.e., burden on healthcare system).

In the neurostimulation treatment approach, being patient-specific is critical. This personalized approach ensures that the therapy is precisely configured to address individual neurological conditions, optimizing its effectiveness and minimizing potential risks. In this method of treatment, a specific setting would not fit all patients, necessitating the adjustment of various stimulation parameters for each patient. This process requires long-term recording of brain activity and real-time processing of the acquired data to tailor the treatment accurately and ensure the effectiveness of the stimulation.

Based on the above, the significance of patient-specific adaptiveness resonates profoundly across all these treatments, serving as the foundation of their effectiveness. Given the sporadic nature of seizure occurrences, maintaining continuous and long-term monitoring of

the patient’s neuronal activity becomes imperative. Another critical factor in the monitoring process involves enhancing the spatial and temporal resolution, thereby facilitating the precise detection of seizure manifestations. Additionally, the solution should be minimally intrusive and non-invasive, minimizing disruption to the patient’s daily life.

Electroencephalography (EEG) recording is a good candidate for fine-tuning each of these treatments methods as it provides the high spatial and temporal resolution and large spatial coverage. However, a clinical EEG recording practice involves precise placement of several electrodes based on a standardized method (e.g., 10-20 system) by a trained EEG technologist, injection of adhesive conductive gels to the electrode for better (i.e., physically-stable and low-impedance) connection, tethering the patient to a recording setup to save and display the acquired data, and post-experiment cleaning of the patient scalp and the electrodes [10–13]. Additionally, it is required to perform a review and analysis of the entire recording, conducted by a skilled technician under the guidance of an epilepsy specialist. This time-consuming and demanding process has limited the use of clinical EEG recording such that the wait times for a conclusive EEG test could take up to a few months.

Furthermore, standard EEG recording is typically conducted for about an hour, whereas a neurologist might require a more extended EEG monitoring period, for example, 72-hour EEG episode. However, conventional setups are not suitable for such a long-term EEG monitoring, thus put a significant burden on the healthcare system and completely disrupt patient’s life. Additionally, long-term monitoring generates a substantial volume of data, making the interpretation a lengthy process.

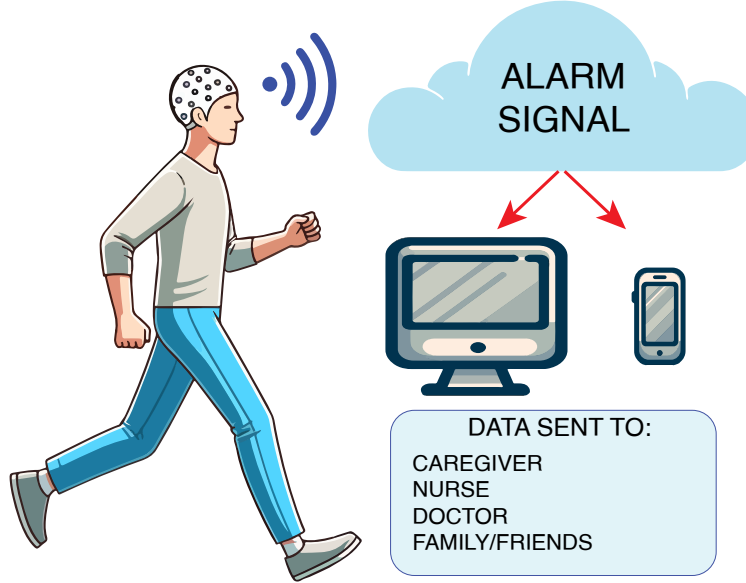


Figure 1.1: Conceptual overview of a wearable EEG recording device with seizure detection capability for long-term application

All the factors mentioned above point to the necessity for a wearable technology, such as a headset, designed for EEG recording. The ideal device would be portable, lightweight, comfortable, and easy to set up for long-term monitoring. In addition, considering the large amount of data generated during long-term monitoring, it is desirable to incorporate an algorithm that could analyze raw EEG data to identify potential seizure events.

An equally crucial aspect that emphasizes the importance of such a device is the potential for reducing secondary injuries in epileptic patients. These injuries, resulting from a lack of consciousness during seizures, can range from head trauma, choking, drowning to cuts, bruises, and burns. By integrating a seizure-detection algorithm into the EEG monitoring device, an alert system could be established to notify either the patient or the caregivers about impending seizures, thereby minimizing the risk of secondary injuries. Fig. 1.1 shows a conceptual overview of such device that monitors patients EEG while let them continue

their daily activities.

1.2 Design Requirement

The design requirements for the device are influenced by a combination of factors. Primarily, the quality of the recording plays an essential role in determining the necessary specifications. The electrodes employed in the recording process also significantly impact the system requirements, adding another layer of complexity to the equation. Finally, the size of the device and its ergonomic design contribute to the overall set of requirements, ensuring not only optimal functionality but also user comfort.

1.2.1 Recording Quality: Noise, Artifacts, and Dynamic Range

For a device designed to monitor EEG signals and perform diagnostic tasks on the recordings, the most critical design target above all others is high-quality(HQ) signal acquisition. HQ recording in the context of EEG data acquisition is characterized by several critical attributes. Firstly, it refers to achieving a high Signal-to-Noise Ratio (SNR), which is crucial for distinguishing neural signals from background and electronic noise, enabling precise and reliable analysis. Secondly, HQ recording implies resilience to mismatch across various recording pathways from different electrodes, ensuring uniformity and consistency in data capture. Thirdly, it requires robustness against interference, guarding the integrity of EEG signals against contamination from external sources. Lastly, it encompasses the system's abil-

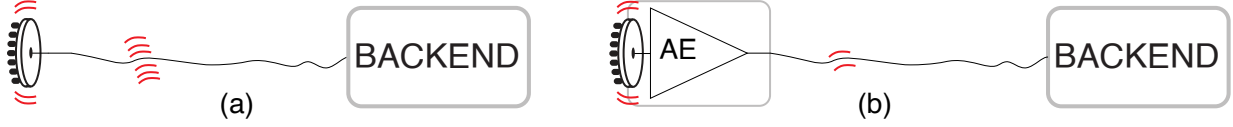


Figure 1.2: (a) The main sources of motion artifact and (b) the commonly applied solution to this problem.

ity to resist noise artifacts, such as those caused by muscle movements or eye blinks. These techniques are vital for the accurate reflection of neural activity in the EEG data, minimizing any potential distortions. The collective goal of these elements is to deliver high-fidelity EEG data that forms the foundation for accurate neurological evaluations and diagnoses.

Frequency range and amplitude of the EEG signals typically falls within the range of 0.5Hz to a few 100Hz and $10\mu\text{V}$ to few $100\mu\text{V}$. To capture a signal with such a low amplitude, it is essential to design a recording system with sufficiently-low noise. As discussed in [14], a system featuring an input-referred noise (IRN) of less than $1\mu\text{V}_{RMS}$ (i.e. $6.6\mu\text{V}_{p-p}$ for less than 0.1% of the time [15]) is necessary for reliable performance.

A major challenge in wearable EEG recording is motion artifact. As shown in Fig. 1.2(a) it affects the recording process in two ways, wire movements and electrode-skin relative movement. The first problem, in the same way as any environmental noise can add artifacts to the recorded signal. As shown in Fig. 1.2(b), a commonly applied solution involves using "active electrodes" (AEs). These AEs are passive electrodes with active electronic circuits attached to them to amplify EEG signals at the recording site before forwarding them for further processing [16–18], which would virtually mitigate the effect of wire movements. However, relative movement between the electrode and skin leads to variations in electrode-skin impedance, which would results in artifacts on the recorded signal that could be as large

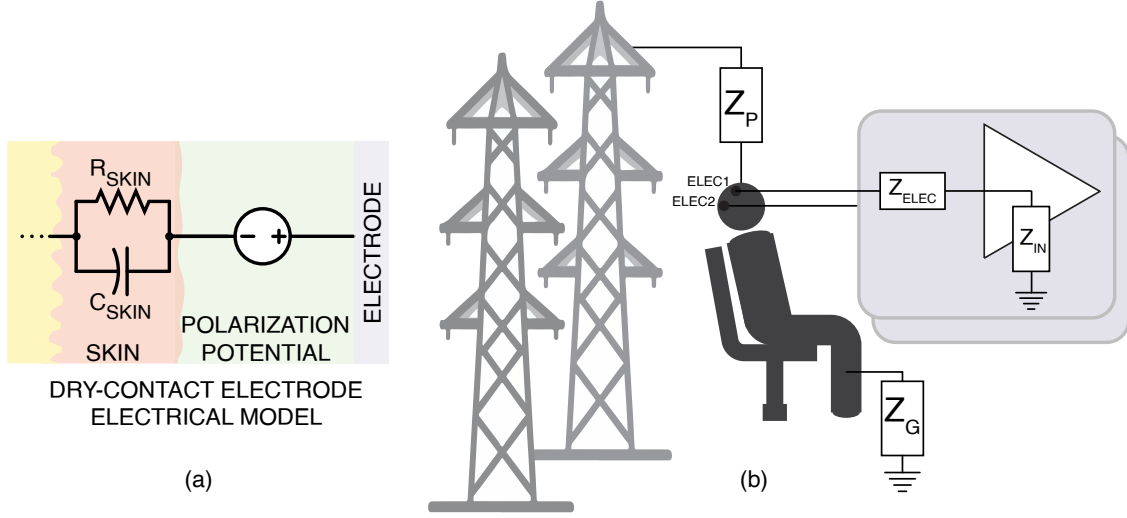


Figure 1.3: Electrode-Skin interface model

as 100mV, resulting in the required input dynamic range (DR) for the recording circuit to exceed 80dB. As these artifacts are added to the signal at the input (i.e., before the amplification) they cannot be removed/attenuated through the use of active electrodes in the system. The intricacies of this challenge and its resolution will be discussed in details in Chapter 3.

1.2.2 Electrodes, Input Impedance, and DC Offset

The common choice for wearable EEG recording is the dry-contact electrode, as it eliminates the necessity for gel injection, thereby minimizing the preparation time for recording. However, this advantage is accompanied by certain associated costs. To focus on these costs, an initial electrical characteristics of dry-contact electrodes is required. Fig. 1.3(a) depicts the electrical model of an electrode-skin interface for dry-contact electrode. The DC voltage generated by the half-cell potential, typical in both dry and wet electrodes, exhibits variabil-

ity across electrodes in the range of -300 mV to $+300$ mV [19]. This DC voltage generally is presented on top of the EEG signals as an offset and should be filtered out, otherwise will be amplified and saturate the output of the recording amplifier.

Compared to wet electrodes, dry electrodes have a higher electrode-skin interface impedance, potentially reaching a few $M\Omega$. As depicted in the Fig. 1.3(b), the EEG signal degradation occurs at the recording input due to the voltage division between the amplifier's input impedance and the electrode. Therefore, the input impedance of the device should be as high as possible to minimize this degradation. On the other hand, a high input impedance, as illustrated in the Fig. 1.3(b), results in an increased power line 60Hz noise. According to [20] the amplitude of power line noise impedance could be in the order of 100mV. This necessitates a Common Mode Rejection Ratio (CMRR) of 80dB, given the low-amplitude nature of EEG signal (typically $10\mu V$ -1mV) and the substantial induced power line noise. Considering that any electrode impedance mismatch (ΔZ_{ELEC}) between two channel results in CMRR of $20 \times \log(\frac{Z_{IN}}{\Delta Z_{ELEC}})$, to achieve CMRR of 80dB the input impedance should be higher than 10,000 times of electrode impedance mismatch. Therefore, if we consider an electrode impedance mismatch on the order of $1M\Omega$ (i.e., the reasonable assumption for dry-contact electrodes), it necessitates that the input impedance be higher than $10G\Omega$.

1.2.3 User Comfort: Battery Life, Wireless Connectivity

Considering that the ultimate goal of developing the described wearable technology is to enhance the quality of life for individuals with epilepsy, the use of the device should not ad-

versely affect the daily life of the patient. As such, a device with lower power consumption is more desirable for the patient, as it necessitates less frequent charging among other benefits. The battery, with a reasonable size and weight for a wearable device, has a capacity of approximately 500mAh, enabling it to power the device for a week while maintaining a current consumption of less than 3mA. This translates into a current budget of $100\mu\text{A}$ per channel (including recording, processing, and communication) in a system featuring 30 channels.

Additionally, it is required to incorporate wireless communication capabilities to facilitate data transfer to mobile phones or computers. This component is identified as a significant consumer of power, which could potentially exceed the allocated power budget. To mitigate this, implementing on-chip processing can substantially alleviate the burden on wireless data throughput and, consequently, its power consumption. Despite the integration of on-device processing, a prominent challenge remains the power consumption associated with transferring data from each AE sensor to the central unit for further processing and communication. This is further elaborated in chapter 4, where we introduce the concept of in-AE processing as a strategic solution to reduce power consumption of AE-to-BE communication.

1.2.4 Embedded Diagnosis

So far, all of the requirements have been discussed are related to a conventional wearable EEG recording. To tailor the wearable EEG recording for patients with epilepsy, a seizure detection feature needs to be incorporated. Incorporating seizure detection algorithms yields a few notable advantages. Most importantly, it enables automatic and timely notification of an upcoming/occurring seizure event to both the patient and their caregiver, significantly

Table 1.1: System level char of EEG recording

CIRCUIT LEVEL	
Dynamic Range	>80dB
IRN	$1\mu V_{RMS}$
Band Width	0.5-500Hz
Input Impedance	$>10G\Omega(@DC)$
SYSTEM LEVEL	
Active Electrode	Yes
Offset Tolerance	$\pm 300mV$
CMRR	>80dB
Power/Ch	$100\mu A$
APPLICATION LEVEL	
Number of Wires	Low
Wireless Communication	Yes
Data-Rate Reduction	Yes
Seizure Detection	Yes

reducing the incidence of secondary injuries. Additionally, it does automatic seizure logging (occurrence, start and end time, etc.) for the doctor, significantly reducing the expert analysis time and patients wait times. Furthermore, the seizure detection algorithm can analyze the raw data, selectively transmitting only essential signal information. This optimization effectively minimizes the communication data rate. Of course, adding these necessary features to the system pose additional constraints on the budgeting of the overall available power, making an energy efficient implementation of seizure detection algorithm vital. Table 1.1 provides a summary of the system-level requirements for a wearable EEG recording with seizure detection.

Table 1.2: Comparison of commercially available EEG Recording Devices

Company	Model	#Ch	Dry/Wet	Structure	Battery	Image
g.tec [21]	g-nautilus	32	Hybrid	Active	10 hrs	
Emotiv [22]	EPOC Flex Gel	32	Dry	Passive	9 hrs	
ABM [23]	B-alert statx	20	Wet	Passive	8 hrs	
NE [24]	Enobio	32	Dry/Wet	Passive	5 hrs	
open BCI [25]	-	16	Dry	Passive	8 hrs	
Cognionics [26]	Quick-32r	32	Dry	Active	8 hrs	
mbt [27]	Smarting Pro	32	Dry	-	10 hrs	
IMEC [28]	-	8	Dry	Active	8 hrs	
Muse [29]	Muse2	5	Dry	Passive	5 hrs	
Neurosky [30]	MindWave Mobile	1	Dry	Passive	8 hrs	

1.3 Review of Prior Art Challenges

There have been many attempts to develop commercialized wearable EEG recording devices over the past decades [21–30].

1.3.1 Application-Level Challenges

As summarized in Table 1.2, the number of channels offered by these devices ranges from a single channel to as many as 128. Due to this and also to variations in their recording precision, compactness, and spatial extent, these devices have distinct applications in various fields such as entertainment, sports, and healthcare. Nevertheless, there are some common challenges for all these wearable devices. Primarily, there is a trade-off between the accuracy of the device and its size (i.e., active electrode systems generally are bulkier than the passive ones). Additionally, the system’s size and its complexity, in terms of interconnecting network, grows rapidly with the number of recording electrodes. Furthermore, none of these devices currently have the capability to record for periods extending beyond 10 hours, which is inadequate for the described outpatient monitoring and diagnostic applications.

In addition to these shortcomings, there are several other challenges that are common in the state-of-the-art commercial and academic wearable EEG devices. A significant number of these challenges relate to the analog front-end circuit and how its performance, and consequently the EEG recording quality, is degraded due to various sources of noise, interference, mismatch, distortion, and artifacts. In the following, we will explore the application-

and system-level challenges and examine how these have been addressed in existing literature.

1.3.2 System-Level Challenges

1.3.2.1 The Ability to Mark Seizure Episodes

An essential aspect of our proposed device is its ability to process recorded data for patient-specific seizure detection. This function not only alerts patients or caregivers prior to seizure onset, thereby mitigating the risk of secondary injuries but also limits the volume of data requiring transmission. Such reduction is pivotal in decreasing the power consumption of the data communication block, a major consumer of power in these systems.

In terms of seizure detection, various systems are reported in literature [31–33] that are engineered for ultra-low power operation. These systems range in complexity from basic linear SVMs to more complex convolutional neural networks and non-linear SVMs [34]. A significant challenge in these systems is balancing accuracy with power consumption in the hardware implementation of the chosen algorithm. Moreover, due to the fact that the computation is done in a centralized fashion in all reported prior art, these structures face scalability issues. This issue and our proposed solution to address it are further discussed in more details in chapter 4.

1.3.2.2 Reducing the Number of Wires

Conventional wearable EEG monitoring resemble their clinical counterparts, employing a centralized architecture in which all electrodes are connected to a main back-end unit for

signal amplification digitization, and processing. This significantly limits the scalability of the system in terms of channel count and prevents practical implementation of high-density EEG recording systems (e.g. 10-10 recording system with 73 electrodes).

Investigating various architectural and system-level ideas to reduce the number of required wires when scaling channel counts of an EEG system is an active research area. One approach to reduce the number of wires is to digitize channels outputs and send the serialized data on common bus [35] to avoid increasing the number of wires. The issue with this implementation is the large power consumption of the communication block (e.g., the communication block power is comparable with the rest of the system even for a 8-channel structure reported in this work). In [36], authors propose another approach to reduce the number of wires, in which, each channel analog output is multiplied by a different frequency and therefore, they can be transmitted the analog data on a single wire without interference. Although they could achieve the minimum reported number of wires however this technique resulted in an order of magnitude increase in the power consumption. This issue and our proposed solution to address it are further discussed in more details in section 2.2.

1.3.3 Circuit-Level Challenges

1.3.3.1 High Common-Mode Rejection Ratio

As mentioned, one frequently employed approach utilizes active electrodes (AEs) to amplify EEG signals directly at the recording site before transmitting them for subsequent processing unit. Although this approach boosts the signal-to-noise ratio, it has limitations. Consider-

ing the single-ended nature of AE (i.e., each individual electrode is directly connected at the recording circuitry), the amplification, which involves both the EEG and common mode (CM) signals, forces a limit on AE's voltage gain to prevent saturation, negatively impacting the SNR and interference resilience. Also due to variations in AE-to-AE voltage gain and electrode-skin impedance at the first stage, achieving a high CMRR would not be possible for the overall system. Attempts to route an unamplified reference signal to all AEs for differential amplification have proven ineffective, remaining susceptible to noise and interference. Additionally, performing the common-mode signal removal in the digital domain after digitization often fails to meet CMRR requirements due to ADC's resolution limits and input impedance variation. This issue and our proposed solution to address it are further discussed in more details in chapter 2.

1.3.3.2 Motion Artifact Removal

As mentioned before, the EEG recording device need to maintain its functionality as the patients perform their normal daily activities. Any physical activity of the patient (e.g., talking, chewing, walking, etc.) could cause electrode movements which results in motion artifacts that is a fairly-large and relatively random undesired variations in the signal's magnitude and DC level. Therefore, removing the effect of these motion artifacts is one of the main challenges in wearable EEG recording devices.

Traditional digital signal processing (DSP)-based pattern recognition algorithms, effective for extracting motion artifacts in bio-signal recordings like ECG [37–39], are not suitable for

EEG due to its lack of specific signal patterns and larger motion artifacts compared to EEG signals. Additionally, recording the EEG signals in the presence of motion artifact require using power-hungry high-dynamic-range and high-resolution ADCs [35, 40]. Alternatively, subtracting an estimated motion artifact from the amplifier’s input signal is common, but this can lead to instability and signal distortion due to feedback loop latency constraints, affecting motion estimation algorithm complexity and resulting in poor correlation with actual EEG signals [41]. This issue and our proposed solution to address it are further discussed in more details in chapter 3.

1.4 Thesis Objective

The primary goal of this thesis is to design and develop an innovative wearable diagnostic device tailored for outpatient epilepsy monitoring. This device aims to embody the technical specifications listed in Table 1.1, including circuit, system, and application levels. Furthermore, it is crafted to tackle several significant challenges inherent in the current landscape of epilepsy monitoring technologies.

At the circuit level, the device targets a dynamic range greater than 80dB, ensuring it can accurately capture a broad spectrum of electrical signals generated by brain activity. It aims for an input-referred noise (IRN) of less than $1\mu V_{RMS}$ to minimize signal distortion and enhance the clarity of the readings. The bandwidth is designed to be between 0.5 to 500Hz, accommodating the full range of relevant neural signals. Additionally, an input impedance of over $10G\Omega$ at DC is specified to reduce signal loss and interference.

Moving to the system level, the design incorporates active electrodes to improve signal quality and fidelity. It targets an offset tolerance of $\pm 300\text{mV}$ and a common-mode rejection ratio (CMRR) of over 80dB, which are crucial for filtering out unwanted noise and interference from the environment. The power consumption per channel is targeted to be less than $100\mu\text{A}$, enabling long-term use for the device without compromising its performance.

At the application level, the device results in a user-friendly, scalable and customizable design with minimal number of wires, thereby enhancing patient comfort and compliance. It integrates wireless communication capabilities to facilitate data transmission and real-time monitoring without the constraints of physical tethering. Furthermore, it features data-rate reduction and seizure detection algorithms, making the device not only efficient in monitoring neuronal activities but also proactive in alerting patients and caregivers to potential seizure episodes. In the following we highlight each of the existing challenges and our proposed solution.

1.5 Existing Challenges and Proposed Solutions

- **Challenge:** Traditional wearable EEG monitoring devices employ a centralized architecture, with all electrodes connected to a central unit. This structure tends to be bulky, uncomfortable, and lacks scalability with an increasing number of channels.

Proposed Solution: The novel EEG monitoring device we have designed minimizes the number of required wires, thus improving both the user’s comfort and the device’s scalability. We have achieved this by incorporating both the recording front-end and the digital processing unit directly within each AE in a distributed manner.

- **Challenge:** Existing wearable EEG devices suffer from issues related to motion artifacts, which can significantly distort the recorded EEG signals, leading to inaccurate readings and analyses.

Proposed Solution: To combat this issue, our device employs a level-crossing technique that prevents amplifier saturation and minimizes the impact of motion artifacts. Additional blocks have been incorporated to remove motion artifacts based on ETI measurements while ensuring the highest possible signal integrity. This solution is described in details in Section 3.3.1.

- **Challenge:** In wearable EEG devices, achieving an high CMRR (i.e., >80) is a crucial but challenging due to the AE to AE gain and ETI mismatch.

Proposed Solution: To address this challenge, our design incorporates a novel in-AE CMRR enhancement technique that is robust against AE to AE gain and ETI mismatches. Our solution is described in details in Section 3.3.1.4.

- **Challenge:** Traditional EEG devices require to transmit and process the raw data from all channels in the central processing unit for seizure detection.

Proposed Solution: To overcome this, our proposed device features a novel in-channel feature extraction approach, along with our innovative boosted linear SVM classification technique (described in details in Section 4.1 and 4.2) which enables the system to perform distributed processing with low power consumption.

1.6 Proposed System-Level Architecture

Given the power consumption profile of traditional EEG recording systems as depicted in Fig. 1.4, it is evident that the analog front-end (i.e. two stages of amplifiers and bias generator circuits) block accounts for the largest share of power consumption. Following closely is the power utilized by the communication link between the active electrode and the digital backend. In light of this distribution, and towards achieving the goal of developing a channel-count-scalable energy-efficient wearable device, we employed various circuit- and system-level techniques to achieve the targeted signal acquisition and processing performance while (a) minimizing analog front-end's power consumption , and (b) reducing data communication power by integrating processing capabilities within the active electrode itself, thus lowering the data transmission rate.

The developed device is composed of several blocks, as presented in the top-level conceptual block diagram in Fig. 1.5. This includes an array of active electrodes (AEs), as well as modules dedicated to seizure classification, wireless communication, and common-mode feedback to the body.

Each AE comprises of two parallel paths for EEG recording and ETI measurement which is used for motion artifact removal. It also includes a digital signal processing unit performing feature extraction to mark the seizure episodes. This structure is a novel approach towards distributed signal processing and allows for greater scalability and flexibility. Lastly, the output from all channels is used to make the final seizure versus non-seizure decision. The details of the implementation of the discussed blocks are elaborated in Chapters 3 and 4.

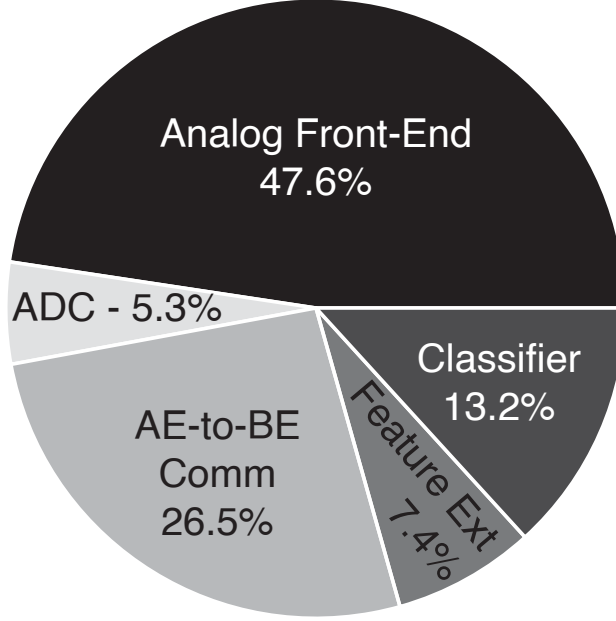


Figure 1.4: Power consumption profile of traditional EEG recording systems.

Fig. 1.5 also shows the interface of the active electrodes with each other through shared wires and to the common units among all the active electrodes. In addition to the AEs, this system hosts three mini-PCBs where the first board is called the CM board and is responsible to realize the DRL loop. The details of the DRL loop is discussed in section 2.2.2. The second one is responsible for wireless data transmission to the mobile device and the third one is the classifier IC which is elaborated in section 4.2.

1.7 Dissertation Organization

The organization of the dissertation is as follows. The second chapter presents the design, development, and experimental characterization of the first generation of our active electrode (AE) IC for wearable ambulatory EEG recording. The proposed architecture features in-AE double common-mode (CM) rejection, making the recording's CMRR independent of

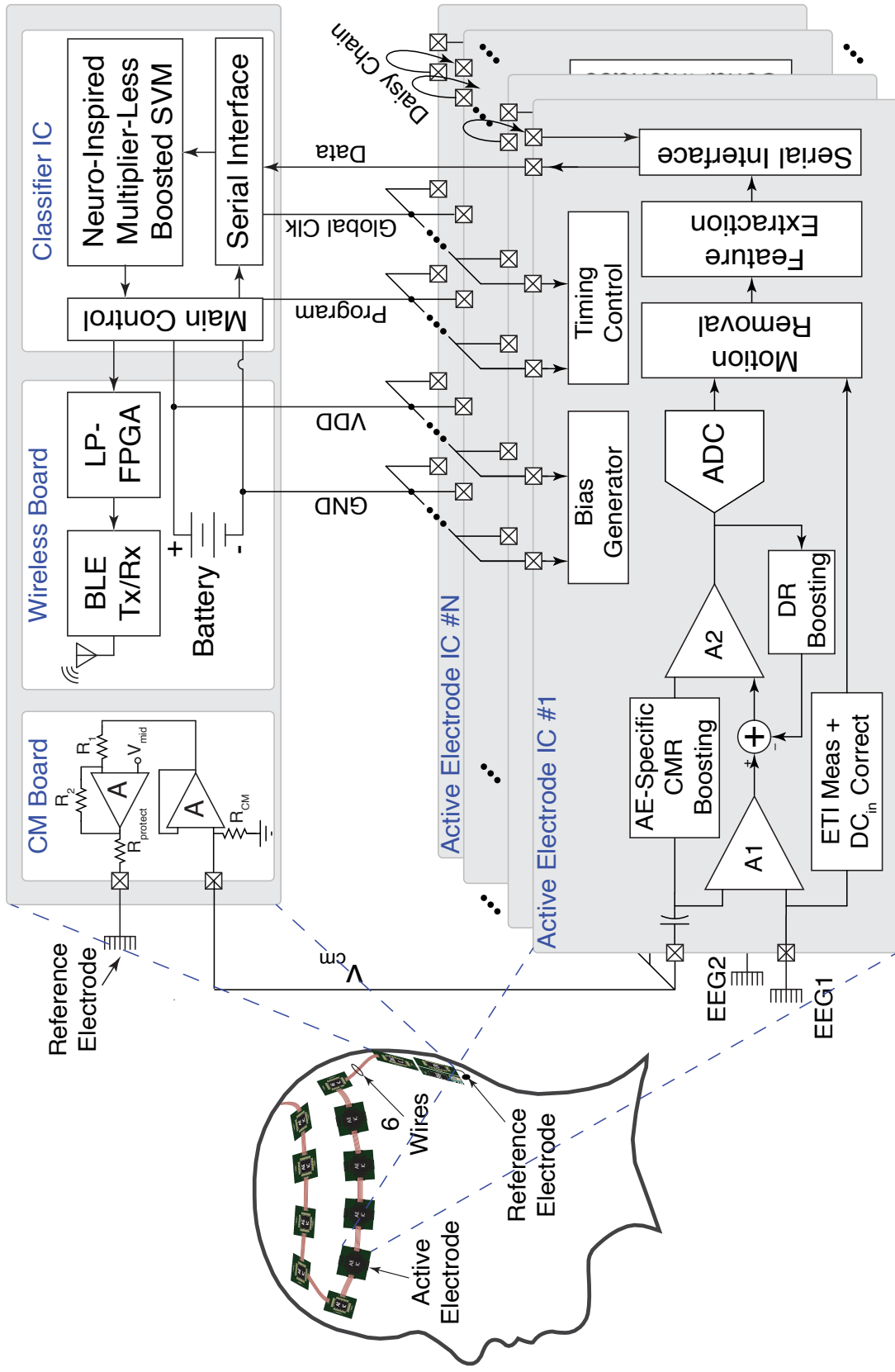


Figure 1.5: Conceptual top-level block diagram of the presented active electrode with distributed digital signal processing.

typically-significant AE-to-AE gain variations. Thanks to being DC coupled and needless of chopper stabilization for flicker noise suppression, the architecture yields a super- $T\Omega$ input impedance. Such a large input impedance makes the AE's CMRR practically immune to electrode-skin interface impedance variations across different recording channels, a critical feature for dry-electrode ambulatory systems. Signal quantization and serialization are also performed in-AE, which enables a distributed system in which all AEs use a single data bus for data/command communication to the backend module, thus significantly improving the system's scalability. Additionally, the presented AE hosts auxiliary modules for (i) detection of an unstable electrode-skin connection through continuous interface impedance monitoring, (ii) dynamic measurement and adjustment of input DC level, and (iii) a CM feedback loop for further CMRR enhancement.

The Third chapter presents the design, development, and experimental characterization of the second generation of our active electrode (AE) IC for wearable ambulatory EEG recording. This architecture not only has the features of the first-generation IC but also incorporate 1) adopting an auto-ranging scheme in the AFE that leads to $>17\text{dB}$ DR improvement, 2) employing an AE-specific-boosted distributed feed-forward common-mode rejection (CMR) enhancement method achieving $>80\text{dB}$ CMRR in the presence of $1\text{M}\Omega$ AE-to-AE input impedance (Z_{in}) mismatch (89.2dB without mismatch), and 3) an AE-specific electrode-tissue impedance (ETI)-correlation-based circuit for motion artifact detection and suppression.

The Fourth chapter presents the software- and hardware level implementation of our

novel energy-efficient seizure detection technique. Our proposed technique includes in-AE pulse-based implementation of the widely-used spectral band energy (SBE)-based feature extraction and a classifier using a combination of neuro-inspired computation idea and adaptive boosting to enhance classification efficiency. This chapter discusses the theoretical aspects of the proposed structure as well as simulation and experimental results of our fabricated IC in 180nm TSMC technology. This chapter also presents our envisaged top-level integration of the system.

The last chapter concludes the dissertation, summarizing the key contributions and publications resulting from this research. It also outlines future work trends and suggestions for further advancement in the field of wearable EEG recording headset and the related applications.

Chapter 2

An Active Electrode with In-Channel Boosted CMRR for Distributed EEG Monitoring

2.1 Introduction

Over the past few years, several wearable EEG monitoring headsets have been developed, aiming to provide a fast, low-cost, and medically-relevant alternative to the existing technology, thus facilitating the widespread use of EEG monitoring for both in-patient and out-patient care [41–43]. As shown in Fig. 2.1(a), similar to the clinical bench-top systems, most conventional wearable EEG monitoring devices have a centralized architecture, in which all electrodes are connected to a central unit that performs signal amplification, filtering, quantization and digital signal processing [37–39]. To enable quick setup time and comfortable

use, these headsets use dry (i.e., gel-free) electrodes, which comes at the cost of having a less-stable electrode-skin contact with a significantly higher interface impedance. This, together with the physical distance between the passive electrodes and the data acquisition module result in the already-weak sensed EEG signals to be significantly distorted by various noise and interference sources before reaching the central unit's recording amplifiers.

A widely-accepted solution for this issue is using "active electrodes" (AEs), i.e., electrodes that have electronic circuits directly attached to them (as shown in Fig. 2.1(b)) to amplify EEG signals at the recording site before sending them to the central module for quantization, processing, wireless communication, etc. [19, 40, 44]. This increases the signal-to-noise ratio (SNR) of the recorded signal, thus reduces the impact of noise/interference. Since the amplification is done at the electrode site, an AE's amplifier typically has a single-input architecture, resulting in amplifying both the site-specific neural signals and the signal common among all electrodes (i.e., the common-mode (CM) signal). Routing an un-amplified reference signal (sensed at a reference electrode) to all AEs to enable differential amplification does not solve the problem as it will be prone to noise/interference in the same way as signals picked up by passive electrode. Additionally, since the CM signal could be significantly larger than the neural signals, AE's voltage gain will be limited to small values (e.g., ~ 10 V/V) to avoid amplifier saturation, which reduces the SNR improvement, hence, limits the aforementioned resilience to interference. It should be noted that EEG recording has very little practical value without removing the CM component, which makes CM rejection a critical design requirement. In this structure, CM rejection is performed in the central unit

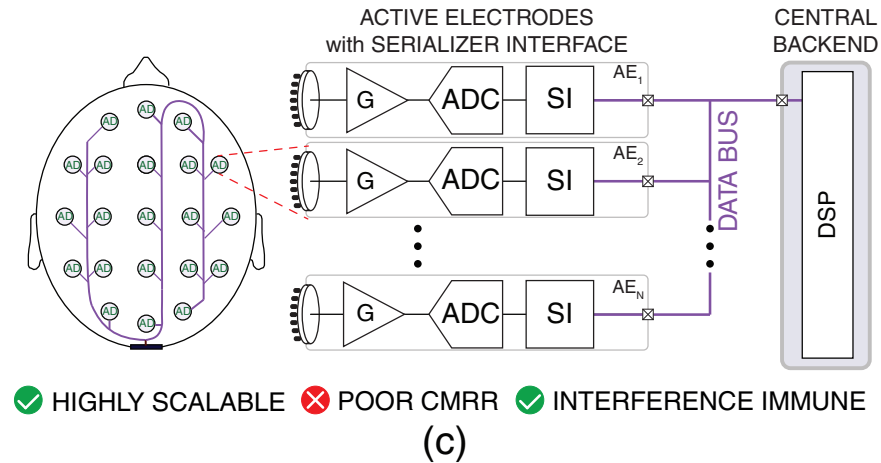
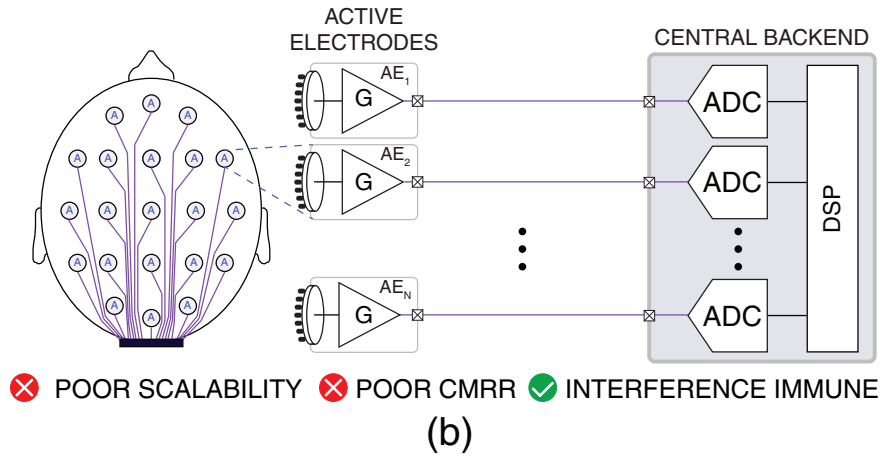
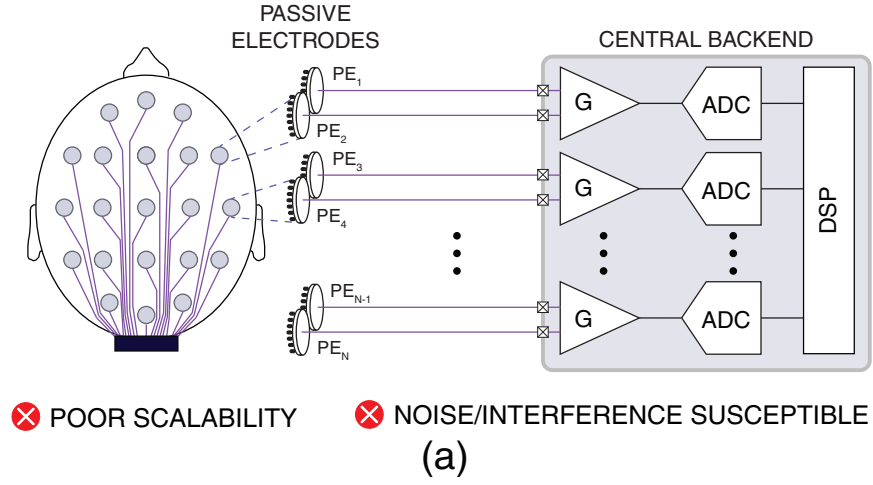


Figure 2.1: State of the art EEG recording architecture using (a) passive electrodes, (b) active electrodes, and (c) active electrodes with digitization.

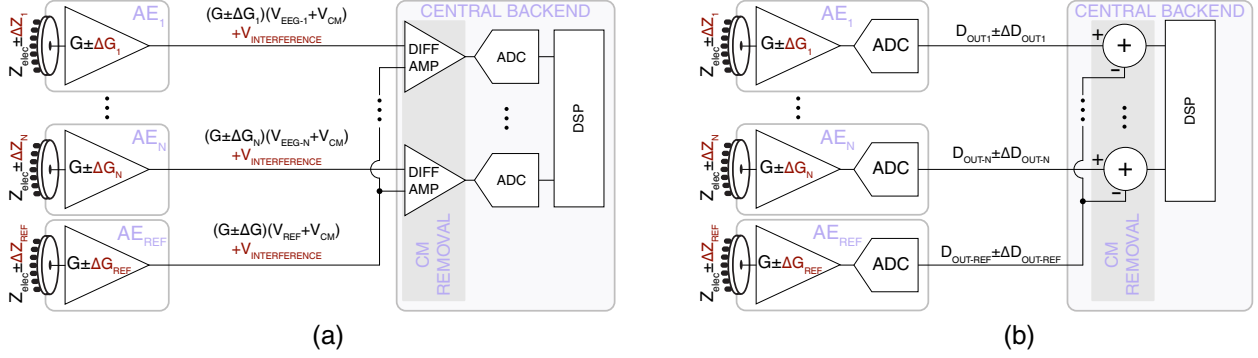


Figure 2.2: CMRR improvement in a centralized EEG recording architecture through (a) analog and (b) digital differentiation.

in digital domain (after digitization) but cannot meet the CMRR requirement, mainly due to the AE-to-AE voltage gain and electrode-skin impedance variations.

The other important challenge with the centralized architecture is the number of wires required for connecting different components of the system, which constraints system's scalability. Recently, there has been an increasing interest in high-density EEG (HD-EEG) as it provides a higher spatial resolution for recording and allows for detecting more localized events compared to standard EEG [45, 46]. With the centralized architecture, the number of required wires for HD-EEG could cause significant SNR degradation due to various interference, noise, and cross-talk. The high wire count also increases the system's complexity, thus makes debugging/repair a serious challenge, and results in heavier/bulkier wearable device. This has motivated for investigating new architectures/techniques for better scalability. Reported solutions include (i) integration of all channels on a single flexible PCB substrate that allows for high-density shielded wiring [43], (ii) using frequency modulation (FM) to send data from all channels on a single wire, which reduces the wire count, but at the cost of a increasing power consumption significantly [36], and (iii) to include an analog-to-digital converter (ADC) in each AE and connect the digitized output of all channels to one data

bus using a digital interfacing protocol, as conceptually shown in Fig. 2.1(c) [35]. While using the last method reduces the number of wires and eliminates the system vulnerability to noise and artifacts, the CMRR degradation due to chip-to-chip variation remains an unsolved challenge.

Fig. 2.2 shows simplified illustrations that represent the commonly-used approaches for CMRR improvement in wearable EEG recording systems. In the first approach (Fig. 2.2(a)), the amplified signals coming from different AEs are fed to a differential amplifier in the central backend, with the second input of the amplifier connected to either the signal from another AE (i.e., bipolar recording) or the signal from a reference AE (i.e., monopolar recording). Despite a limited CMRR improvement due to differential recording, considering the dry electrodes' significant impedance mismatch ($\sim M\Omega$) and the AEs' voltage gain mismatch due to chip-to-chip variations, there will be a substantial difference between the amplified CM signals at the output of different AEs. This difference is further amplified by the differential amplifier, resulting in an overall CMRR that is unacceptably low. Additionally, due to AEs' relatively-small voltage gain (reason was explained above), the recordings are still susceptible to various noise and interference, which could further degrade the CMRR.

Fig. 2.2(b) shows an alternative solution where the signals are digitized in the AE before being sent to the backend (i.e., the architecture shown in Fig. 2.1(c)). Digitizing the recordings eliminates the noise/interference concern, but the voltage gain mismatch concern is still present. Also, since the ADC is quantizing both the EEG and the CM signal, it is required to cover a large dynamic range. This should be achieved without generating substantial noise

at the ADC’s input, as it is preceded by a low-gain amplifier. Considering the above design criteria and the limited power budget of each AE, the ADC’s quantization resolution will be highly constrained. This makes the approach significantly less attractive as its CMRR improvement is limited by the ADC’s resolution.

In this chapter, we will present the design, development, and experimental characterization of a two-stage active electrode architecture with CMRR enhancement in both stages. The architecture conducts CM sensing and rejection early on in the signal path (without degrading noise or input impedance) to prevent CM amplification, and consequently avoid (i) forcing a small maximum voltage gain to prevent output saturation, (ii) CMRR dependency on AE’s gain, resulting in its degradation by AE-to-AE mismatches.

The proposed architecture is also immune to electrode-skin interface impedance (Z_{ESI}) variations across different AEs, thanks to its super- $T\Omega$ input impedance. Such a high impedance is achieved by (i) DC coupling to the electrodes, and (ii) leveraging relaxed area requirements to suppress flicker noise through increasing the gate area and avoiding chopper stabilization. The DC coupling is possible and does not make the performance dependent on input DC levels, as the proposed architecture is inherently tolerant to ± 350 mV input DC variations. Furthermore, and we have integrated auxiliary circuits to boost this range up to ± 500 mV. Through a feedback loop, we also have loose control on the scalp DC level, which prevents the variations to surpass the circuit’s tolerance thresholds. We have experimentally shown the efficacy of the proposed architecture in rejecting common-mode signals in the presence of significant AE-to-AE mismatch.

Each AE also integrates block for (i) detection of an unstable electrode-skin connections, (ii) power line noise/interference removal feedback loop, and (iii) responsive dynamic adjustment of large DC level variations at the input. The CMRR-enhanced amplification in each AE is followed by blocks for quantization, data serialization, and digital interfacing. Together, they enable a fully distributed EEG recording architecture that requires a small number of wires (independent of the number of AEs) to connect all AEs together and to a backend module for wireless data transmission.

2.2 System- and Circuit-level Implementation

In this section, we will explore several key subjects regarding the main challenges and constraints in the circuit and system-level design of the proposed active electrode and how we propose to overcome them.

2.2.1 Centralized vs. Distributed CMRR Enhancement

Fig. 2.3 analytically compares the in-AE CMRR enhancement of a distributed solution with in-backend CMRR enhancement of a centralized architectures. As shown in Fig. 2.3(a), in the centralized scheme, the input signal (i.e., EEG + CM) is amplified at each AE and then subtracted from the amplified signal from the reference electrode in the central backend. In the absence of AEs' gain mismatch (i.e., $G_1 = G_2 = \dots = G_{REF}$), this architecture could yield an infinite CMRR, assuming an ideal backend differential amplifier. However, even a

slight gain mismatch could drastically degrade the CM rejection performance. Quantitatively speaking, considering the expression for V_{OUT} in the conventional design, we have,

$$\begin{aligned} CMRR &= 20 \times \log\left(\frac{A_{dm}}{A_{cm}}\right) \\ &= 20 \times \log\left(\frac{A \cdot G_1}{A \cdot (G_1 - G_{REF})}\right) = 20 \times \log\left(\frac{G_1}{\Delta G}\right). \end{aligned} \quad (2.1)$$

Based on this equation, only a 1% gain mismatch (ΔG) results in a CMRR as low as 40 dB. This means that to achieve a commonly-accepted 80 dB CMRR, the gain mismatch between the two AEs must be smaller than 0.01%, which is practically impossible considering the chip-to-chip variations. It should be noted that G_1 and G_{REF} also account for the signal attenuation resulted from voltage division between the amplifiers' input impedance and the significantly-high impedance of dry electrodes (i.e., $|Z_{IN}/(Z_{IN}+Z_{elec})|$). Therefore, any mismatch between different electrode-tissue impedances affects the ΔG as well. Moreover, as shown in Fig. 2.3(a), both the EEG and the CM are amplified in each AE, which changes the biasing point of the input transistors and therefore, significantly increases the required linear input range for the backend differential amplifier, thus its power consumption. The AEs' gain cannot be reduced below a certain level without their output signals being more susceptible to line interference.

The first part of our proposed solution for in-AE CMRR improvement is shown in Fig. 2.3(b). The idea here is to calculate the common-mode voltage through passive capacitive averaging, and to make this voltage available to all AEs through a shared wire among them. In each AE, this voltage is used as the negative input of differential amplification, which

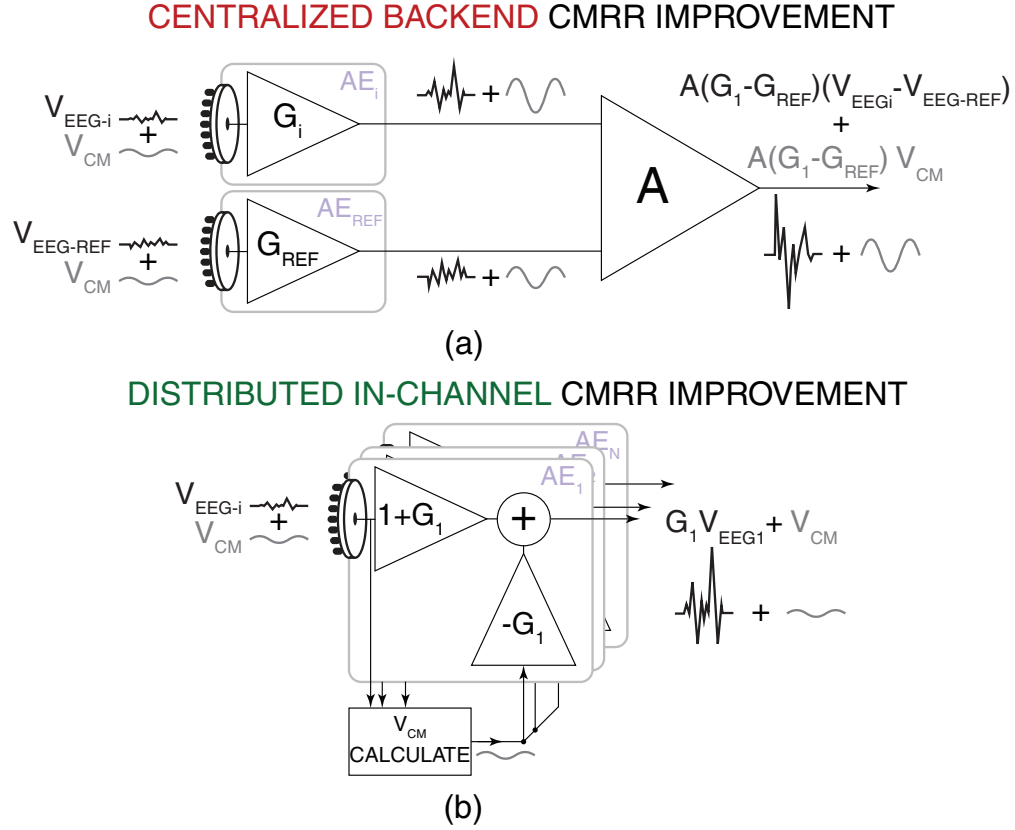


Figure 2.3: (a) Centralized architecture with CMRR improvement using a backend differential amplifier. (b) Conceptual block diagram of the first-stage of the proposed design with in-AE CMRR improvement.

results in effectively removing CM as early as possible in the signal path. As shown, to ensure that the CM is not amplified in AE, it is designed in a way that the signal from each recording electrode is amplified by a gain of $1+G$, while the calculated CM is amplified by $-G$, resulting in the site-specific EEG to be amplified while the CM is fed through with a unity gain. It is critical for effective CM rejection that both $-G$ and $1+G$ are realized using the same circuitry to avoid any gain mismatch.

2.2.2 In-AE CMRR Double Boost

Fig. 2.4(a) shows the circuit schematic of the idea described above. The negative feedback ensures that the two inputs of the low-noise operational transconductance amplifier (LN-OTA) are equal (i.e., $V_1 = V_{EEG-1} + V_{CM}$). The C_{CM} included in each channel are all connected together and the common node is biased through a resistor (R_{CM}). This capacitive structure yields the average of input signals of all electrodes (i.e., the common mode signal) at its common node that is connected to the resistor. The high-pass pole is set by C_{CM} and R_{CM} to ensure that the averaged signal is not filtered out. Fig. 2.4(b) shows the bode plot of V_{CM} estimation transfer function for a 10-channel structure. The cutoff frequency of this filter is calculated as $1/(2\pi NR_{CM}C_{CM})$, where N is the number of channels. In this structure we have $R_{CM}=250\text{ M}\Omega$ and $C_{CM}=250\text{ pF}$ which results in the cutoff frequency of $2.5/N$ (e.g. 0.25 Hz for a 10-channel device) which is safely below the required high-pass pole of the recording front-end.

As highlighted in Fig. 2.4(a), the presented circuit results in a non-inverting amplification

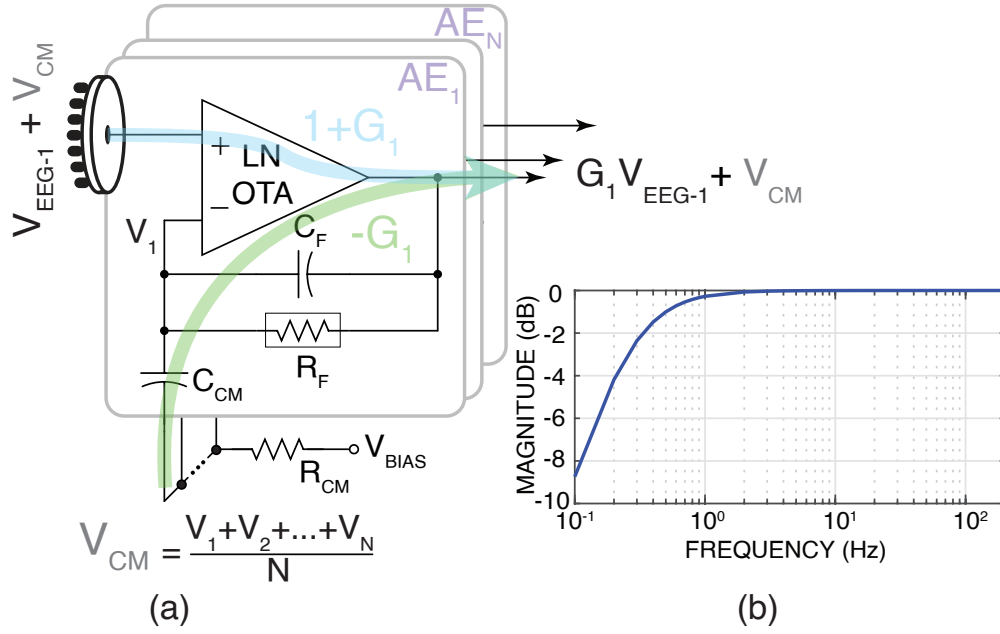


Figure 2.4: (a) The conceptual block diagram of common-mode voltage estimation. (b) The bode plot of V_{CM} estimation transfer function for 10-channel structure.

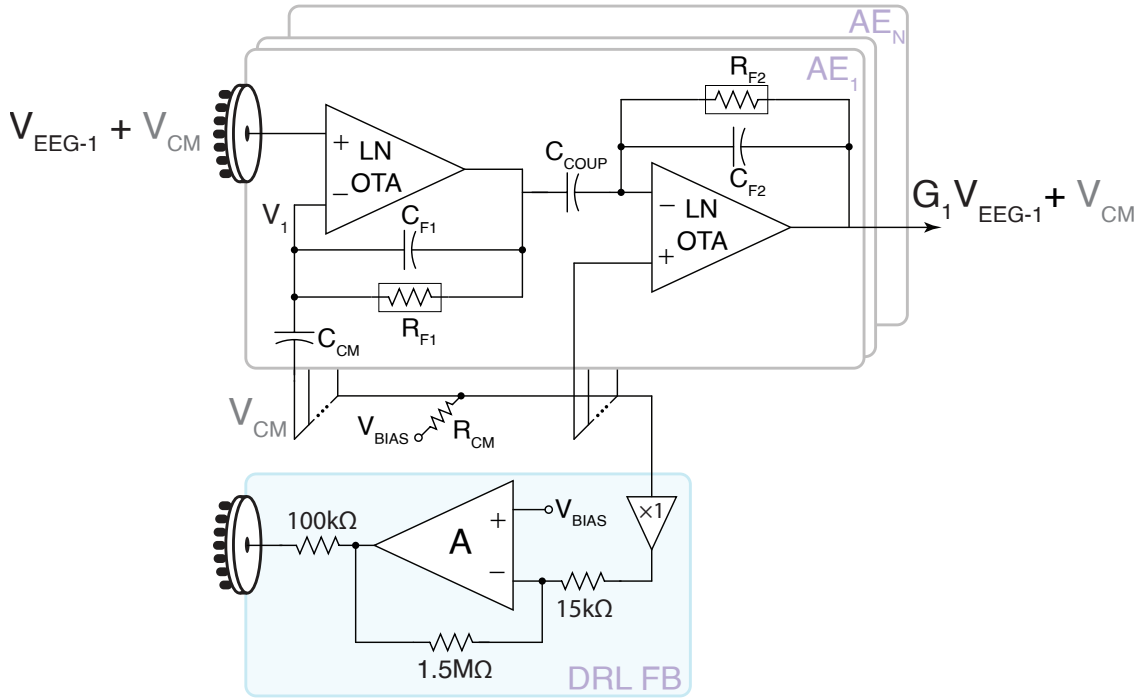


Figure 2.5: (Top) The two-stage amplifier with double-boosted CMRR, employed in each AE. (Bottom) The DRL feedback loop for further CMRR enhancement.

for the input signal (i.e., $V_{EEG} + V_{CM}$) with a voltage gain of $1 + |Z_F/Z_{CM}|$ (i.e., $1 + G_1$), and an inverting amplification for the V_{CM} with a gain of $-|Z_F/Z_{CM}|$ (i.e., $-G_1$). Here, Z_F is defined as the total feedback impedance (i.e., $Z_{RF} || Z_{CF}$), and Z_{CM} is the impedance of C_{CM} .

Based on the above analysis, the amplifier's output is

$$V_{O1} = (1 + C_{CM}/C_F)V_{EEG} + V_{CM}. \quad (2.2)$$

This results in the CMRR to be

$$CMRR = 20 \times \log(1 + C_{CM}/C_F), \quad (2.3)$$

which is independent of any AE-to-AE gain mismatch and as large as voltage gain of the closed-loop amplifier. However, achieving ~ 80 dB gain from the presented single-stage closed-loop amplifier without sacrificing other performance metrics (e.g., area, bandwidth, etc.) is practically impossible. Given that low-frequency high-pass pole of the closed-loop amplifier is set by $1/(C_F \times R_F)$, to be able to record sub-Hz EEG, C_F cannot be made smaller than a certain level without requiring extremely high R_F values that are impractical to implement with a stable value under a reasonable signal swing, even using best pseudo-resistors structures [47–50]. On the other hand, area constraints set a maximum value for C_{CM} . Considering that the voltage gain is proportional to C_{CM}/C_F , the above two constraints set the upper limit for this stage's gain, motivating for a second amplification stage.

It is important to note that amplifying the first stages output will not improve CMRR

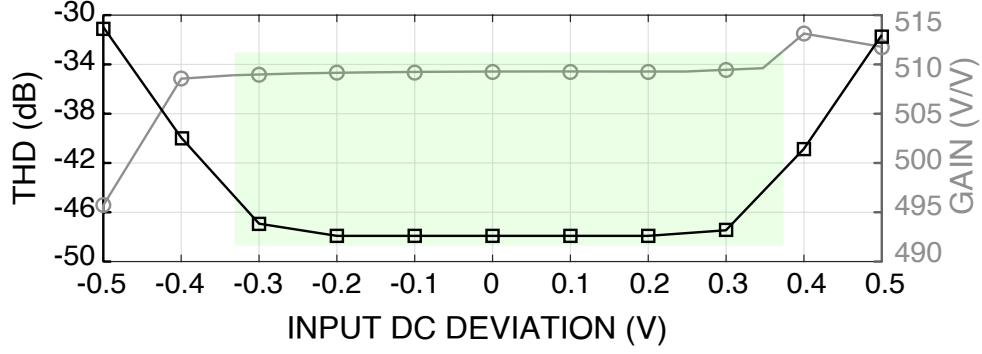


Figure 2.6: Measurement results showing AE's voltage gain and linearity performance for the range of input DC variations tolerated by the presented AE.

as it includes both V_{EEG} and V_{CM} terms. As such, the second amplification stage should also subtract V_{CM} from the input before amplification. Fig. 2.5 shows the circuit implementation of the proposed two-stage amplifier. As shown, AE's CMRR is further improved by connecting the calculated CM to the non-inverting input terminal of the second stage as well. This ensures that the V_{CM} term at the output of the first stage is not amplified in the second stage, resulting in V_{OUT} to be

$$V_{OUT} = V_{CM} - (C_{COUP}/C_{F2})(1 + C_{CM}/C_{F1})V_{EEG}. \quad (2.4)$$

As a result, the overall CMRR of the two-stage amplifier will be $20\log((C_{COUP}/C_{F2})(1 + C_{CM}/C_{F1}))$.

Fig. 2.5 also shows that the calculated V_{CM} is fed back to the scalp to further improve the AE's CMRR. The feedback circuit is named DRL as it works based on the same principles as the popular driven right leg (DRL) feedback loop used in ECG recording [51]. The feedback loop improves CMRR by $20 \times \log(A_{DRL})$, where A_{DRL} is the gain of the DRL path

set to 100 V/V. Without the CMRR boost achieved through the second amplification stage, the DRL loop gain had to be increased by at least an order of magnitude, which results in instability in dry-contact electrodes due to their large interface impedance variations [19].

2.2.3 DC Offset Tolerance

While the DRL loop provides some control on the skin’s potential, the input DC level at different AEs’ could vary by ± 300 mV [19]. For a conventional differential DC-coupled recording front-end architecture, such large variations could significantly degrade the amplification gain and linearity. However, in the presented AE architecture, the first stage OTA’s input terminals are tied together by the negative feedback, removing the need for additional circuitry for DC offset removal. Also, the OTA’s output DC level follows its inputs, thanks to a pseudo resistor (represented as a resistor enclosed by a rectangle) which establishes a DC path. As such, the above-mentioned DC variations could only impact the AE’s performance if they result in extreme changes in the OTA’s open-loop gain (e.g., by causing significant input CM DC variation) such that the AE’s closed-loop gets affected, hence causes amplification nonlinearity. By limiting the first stage gain to 50, as shown in our THD measurement results in Fig. 2.6 an input DC offset tolerance of up to ± 350 mV is achievable before linearity starts to decline (i.e., THD > 0.5% for 2 mVpp sine input). Furthermore, the second amplification stage, which experiences a larger signal swing, is AC-coupled to the preceding stage and therefore, biased with the optimal voltage. Given that the OTA operates within a negative feedback loop (i.e., the gain is set by C_{COUP}/C_{F2}), the nonlinearity issue associated with the

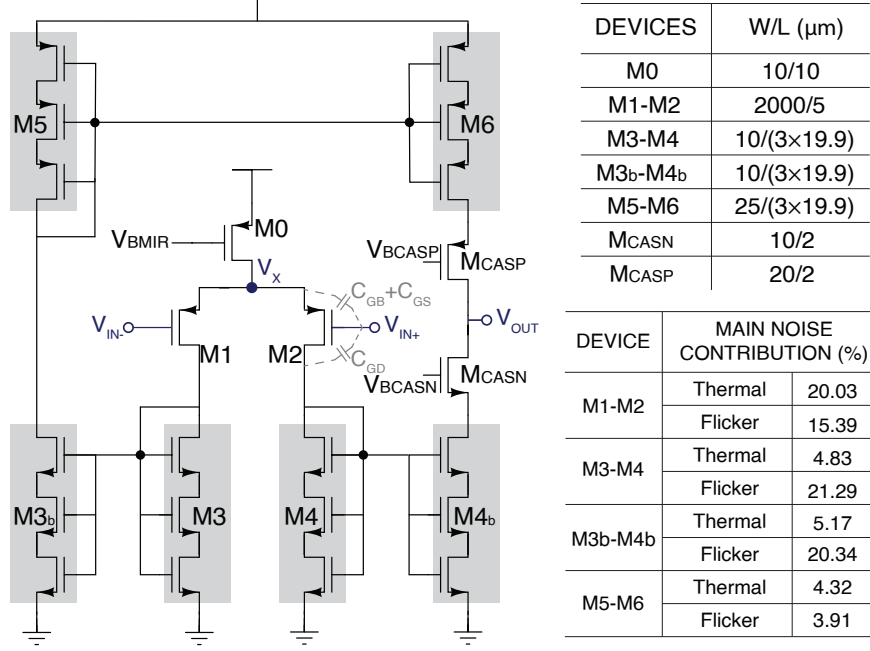


Figure 2.7: The circuit-level implementation of the LN-OTA used in the first stage of the presented AE.

pseudo resistor could only pose a problem if it affects the high-pass pole. To circumvent this, we have designed the pole conservatively to ensure that any changes in the pseudo resistor will not affect the recording.

2.2.4 OTA Design and Flicker Noise Reduction

Since the first-stage OTA is directly connected to the electrodes, it sets the AE's input-referred noise and input impedance (Z_{IN}). To compensate for the high impedance of dry electrodes (Z_{elec}), it is crucial for the active electrodes' common-mode rejection ratio (CMRR) to have a very high input impedance (Z_{IN}) that is orders of magnitude higher than the electrode impedance. This ensures that the voltage division ratio ($|Z_{IN}/(Z_{IN} + Z_{elec})|$) remains relatively constant, regardless of variations in Z_{IN} or Z_{elec} . This is one of the most common

issues in recently-reported wearable EEG recording systems. In the presented design, such high Z_{IN} (e.g., $>1 \text{ T}\Omega$ at DC) are achieved by directly connecting the electrodes to the gate terminal of OTA's input transistor. We intentionally did not use chopper stabilization as it results in Z_{IN} degradation and will require positive-feedback impedance boosting loops that come at the risk of instability and the cost of additional power consumption. Additionally, the use of the OTA in negative feedback effectively makes the inputs of the OTA equal to the V_X voltage (drain of the tail PMOS, as shown in Fig. 2.7). This equality ensures that the voltage across the C_{GS} is zero, which practically eliminates this capacitor's effect on the input impedance. It should be noted that, this feature is inherent to the presented single-ended structure. If a differential configuration was implemented, the V_X would have become a virtual ground, leading to non-zero voltages across the C_{GS} . Furthermore, we opted for PMOS input transistors, which allowed us to connect the source and bulk together. This connection mitigates the effects of the C_{GB} and results in a higher input impedance.

In this design, we leveraged the relaxed area requirement (only one recording channel per chip, thus area scalability is not a concern) to reduce the in-band flicker noise. Fig. 2.7 shows the detailed circuit schematic of the LN-OTA used in this work as well as all transistors' size ratio and a list of main contributors to the overall integrated input referred noise (IIRN). To minimize IIRN, we aimed for maximizing the gm of the input transistors (i.e., M_1, M_2) with respect to the gm of M_3, M_4 and their mirrored transistors, M_{3b} and M_{4b} . As all these transistors share the same bias current, we need to maximize the gm/I_D for the input transistors and minimize it for M_3, M_4, M_{3b} , and M_{4b} . To achieve this, the W/L of

the input transistors and L/W of M_3 , M_4 , M_{3b} and M_{4b} are increased such that the input transistors operate in deep weak inversion and the rest in strong inversion.

To further reduce the flicker noise, the gate areas of all the transistors are increased [52]. To achieve our targeted IIRN (i.e., $<1 \mu V_{rms}$), the length (L) of M_3 , M_4 , M_{3b} and M_{4b} needs to have a higher value than the maximum set by the technology (i.e., $20 \mu m$ in 180 nm TSMC Technology). As a result, three transistors were connected in series to increase the effective gate area and reduce the combined gm/I_D . In addition to above, we considered other factors such as the phase margin (for M_3 , M_4 , M_{3b} , M_{4b}) and the input impedance (for M_1 , M_2) of the OTA in sizing the transistors. This OTA draws $3 \mu A$ current from the supply voltage which is divided equally between the 4 branches. The M_1 and M_2 transistors has gm of $20 \mu S$. Also, the open-loop DC gain of the OTA is 68 dB. For the second-stage OTA, since it receives the amplified version of the EEG signal as the input, its noise requirement is more relaxed compared to the first stage, thus a low power (LP) current-mirror OTA (UGBW: 6.3 kHz, power: $1 \mu W$) was employed.

2.2.5 Lead-Off Detection

A common issue with using dry electrodes in ambulatory wearable EEG recording is unstable electrode-skin connection. This could be due to many reasons (e.g., physical motion [53]) and results in the electrode's signal to be partially or fully corrupted, which could have an adverse effect on the accuracy of CM estimation using the circuit presented in Fig. 2.5. To prevent this, as shown in Fig. 2.8(a), a lead-off detection block is integrated in each AE that

measures the electrode-skin interface impedance (Z_{ESI}) in real time, and upon detection of an abnormally high impedance, disconnects the AE from common-mode signal calculation circuit (loop L1 in Fig. 2.8(a)). As shown, a 3-bit push-pull current-mode digital-to-analog converter (IDAC) is used to source/sink 10 kHz (i.e., out of EEG frequency band) square-wave current pulses to/from the electrode. The resulted high-frequency voltage waveform's peak-to-peak value is correlated with the Z_{ESI} 's magnitude. As shown, this waveform is fed to a closed-loop amplifier (HF-OTA, BW>10 kHz) and then quantized before being fed to digital blocks for peak-to-peak calculation and thresholding.

Considering the fact that dry electrodes have a wide range of size and shapes (hence, impedances), to make the presented design universal, we added a 2-bit mode-selection signal (AE-specific) that controls the range of currents that could be generated by the 3-bit IDAC. This allows for using the same impedance measurement circuit for different types/shapes of dry electrodes. Using this approach, the IDACs can generate currents with a range of 10-500 nA in magnitude with 2+3 bits resolution.

2.2.6 Input DC Level Correction

As discussed previously, large DC level changes at the electrode could cause nonlinear amplification. In addition to the electrode-specific DC offset, electrostatic charges generated on the skin due to many different reason (e.g., patient movement) could also significantly change the static DC level. Additionally, while the current pulses injected to the skin (for Z_{ESI} measurement) are designed to be charge-balanced and biphasic, it has been shown that

they could also result in charge accumulation on the electrode-skin interface in the long term, causing electrode and tissue damage [54].

We have reused part of the lead-off detection circuit to construct another feedback loop (L2, as shown in Fig. 2.8(a)) that is used for input DC level correction. Given that the high-frequency closed-loop amplifier used in the lead-off detection circuit has a resistive feedback path, the average of its output signal represents the DC level at the electrode. As shown in Fig. 2.8(a), the DC control loop calculates the digitized recorded signal's average and checks if it is within a safe range of operation by comparing it with programmable upper/lower threshold values. Upon detection of an unsafe DC level, the IDAC controller makes subsequent adjustments to the current pulses duty cycle (i.e., creates an intentional imbalance in current pulses) to cancel the DC variation. Using this method, our measurement results show an increased tolerance of DC level variation from ± 350 mV to ± 0.5 V.

2.2.7 Digitization and Digital Interface

Fig. 2.8 also shows the signal quantization and communication blocks used for sending the digitized data from different channels to the central unit using the same bus. An ultra-low-power 12-bit SAR ADC (ADS7042) is used for quantization with a sampling period of $990 \mu\text{s}$ (the ADC samples at the negative edge of $\overline{CS}$). The digital output is serialized using $SCLK$, and is turned into a series of 14 bits as shown by SDO in Fig. 2.8(b), starting with two successive zeros followed by 12 bits of data in each period of the $\overline{CS}$.

As shown, $\overline{CS}$ and $SCLK$ are shared among all channels. When $SCLK$ is high, all

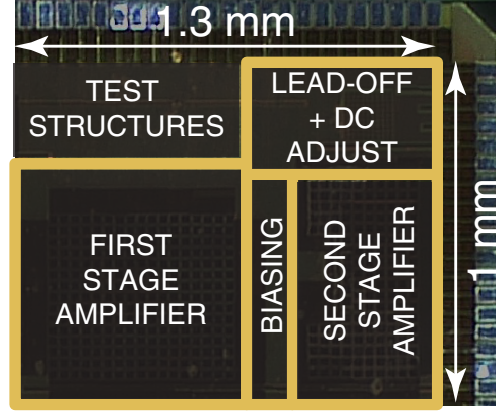


Figure 2.9: Chip micrograph of the proposed recording front-end including the two-stage amplifier and blocks for lead-off detection and DC adjustment.

ADCs' output are valid and represent the same bit position (i.e., the i^{th} bit of the 12-bit output word). This allows for time-multiplexing the ADCs outputs to send their data bit by bit on a single communication line. The time-multiplexing is done using a tri-state buffer in each channel which is controlled by the EN_i signal shown in Fig. 2.8(b). EN_i has the same frequency as the $SCLK$ but its duty cycle is $1/(2 \times f_{SCLK} \times (N + 1))$, where N is the number of channels. Each EN_i is delayed by one duty cycle in order to establish a proper scalable serializing for all channels.

2.3 Experimental Measurement Result

Fig. 2.9 shows the chip micrograph of the presented active electrode IC, designed and fabricated in a 180nm standard CMOS technology. The performance of different blocks and the entire system are validated experimentally. Fig. 2.10(a) shows the measured voltage gain of the active electrode versus frequency, confirming a mid-band gain of 52.7 dB and a bandwidth of 0.2-400 Hz. Fig. 2.10(b) presents the experimental noise measurement results, showing an

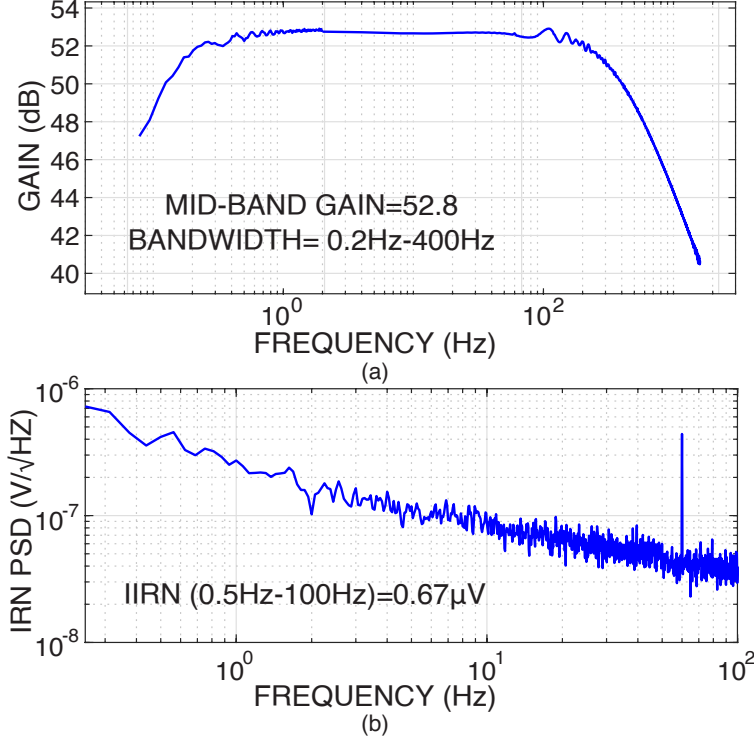


Figure 2.10: Measured (a) gain and bandwidth, and (b) input referred noise of the presented AE.

integrated input referred noise of $0.67 \mu V_{rms}$ for the 0.5-100 Hz range. As shown in Fig. 2.11, we have measured the noise in different values of DC offset. The result shows that the IIRN only experiences noticeable changes for DC offset voltage larger than 0.5 V and stays almost constant within this range.

In the experimental setup, we utilized a Keysight digital multimeter (34465A) that can measure current with a resolution down to the picoampere (pA) level. We modulated the input voltage in a range between 0.8 V to 1 V, incrementing in steps of 20 mV. Throughout these variations, the multimeter registered a current measurement that fell below its 1 pA precision. From this observation, we concluded that our input impedance surpasses $1 T\Omega$ at DC. Furthermore, when we employed a 60 Hz sine input during our trials, we established

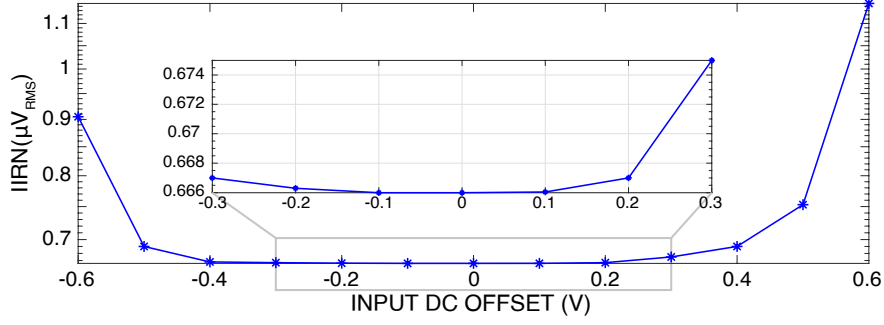


Figure 2.11: Measured integrated IRN versus input DC offset.

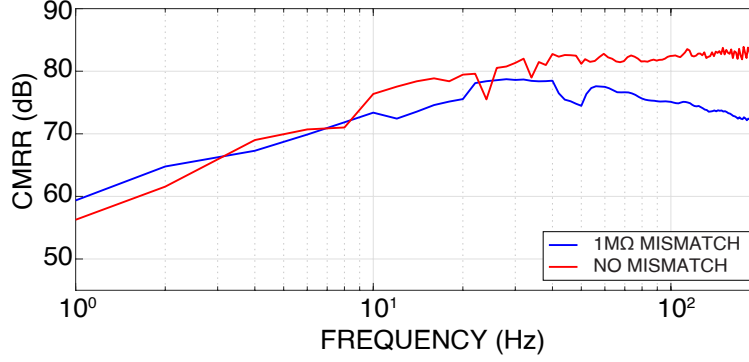


Figure 2.12: Measured AE's CMRR without and with a $1\text{M}\Omega$ Z_{ESI} mismatch showing <5 dB degradation at 60Hz.

that the input impedance was measured at $5.5\text{ G}\Omega$.

The experimental measurement results shown in Fig. 2.12 validate the performance of the proposed design in effective suppression of common mode signals. The plot shows that the structure could achieve a CMRR of 82.2 dB (measured at 60 Hz) when inputs of the two active electrodes are directly connected to the same signal, which represents the situation when there is no mismatch between the interface impedances. In the second (more important) test scenario, a $1\text{ M}\Omega$ resistor was added at the input of one of the AEs to intentionally create a mismatch between the two AEs in terms of electrode impedance, to emulate a realistic situation that could occur for EEG recording with dry electrodes [55]. Our results show that the CMRR is only decreased by less than 5 dB. To put the importance of this result

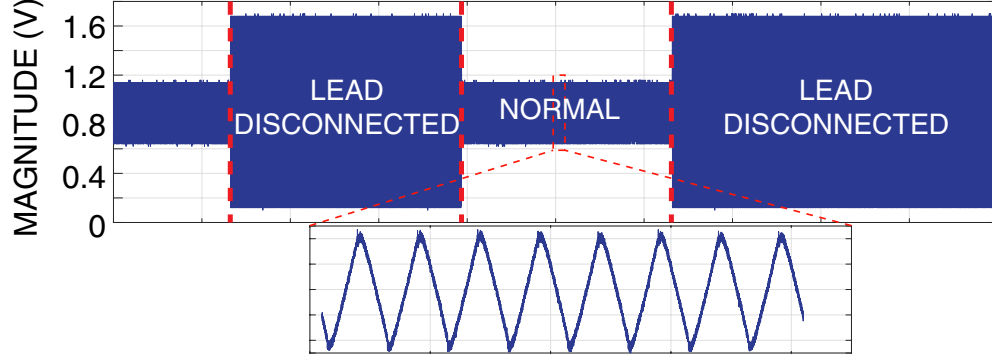


Figure 2.13: Measured output of lead-off detection circuit, showing changes in peak-to-peak magnitude due to Z_{ESI} variations.

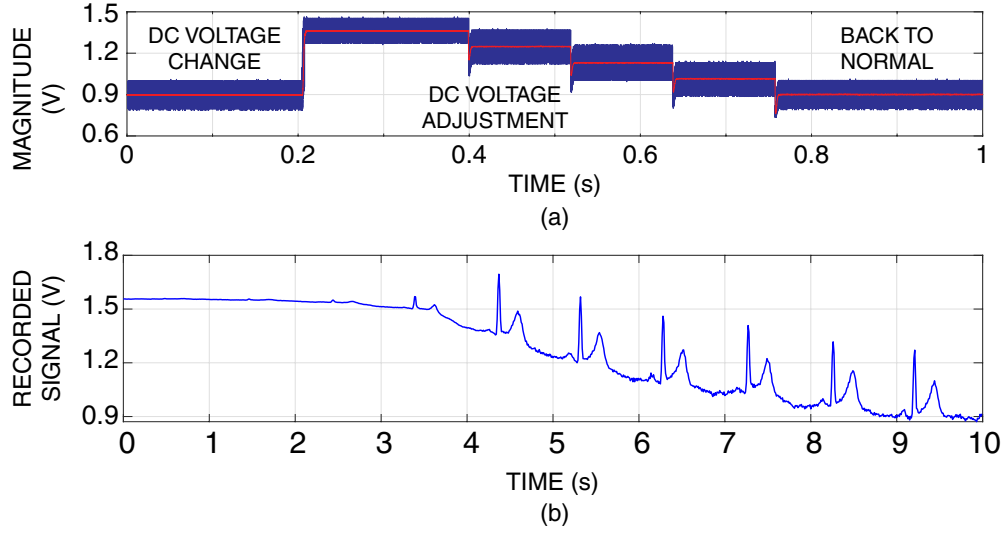


Figure 2.14: (a) Measurement results showing the efficacy of the DC correction loop, (b) and its importance in an in-vivo ECG measurement experiment.

this into perspective, it has been shown in [35] that a 800 k Ω mismatch reduces the CMRR by almost 60 dB. This is achieved mainly due to the proposed recording architecture that benefits from in-AE CMRR double enhancement.

As shown in Fig. 2.12, the CMRR value increases at higher frequencies. The reason is that in this method the added R_{CM} creates a high-pass filter together with the averaging capacitors (i.e., C_{CMS}). From this measurement, it can be observed that CMRRs seem to be even better compared to the case where impedance mismatch is present. The reason is that in

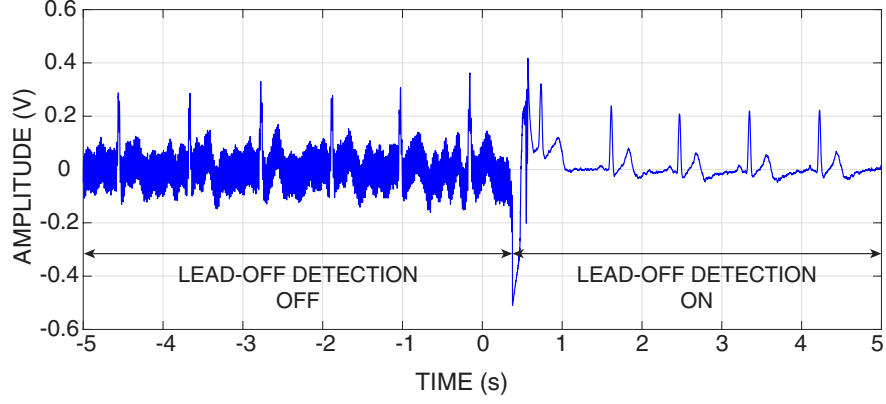


Figure 2.15: In-vivo measurement results showing the effect of an unstable electrode-skin connection on the quality of ECG recording, as well as the efficacy of the lead-off detection circuit in improving CM voltage calculation by excluding the disconnected electrode.

this particular experiment, we intentionally introduced a $1\text{M}\Omega$ resistor to create a mismatch to see how the proposed architecture's CMRR changes under such condition. However, there is an inherent mismatch already present between electrodes, and the addition of this resistor served to compensate for the existing mismatch at lower frequencies for this experiment (it could slightly vary from electrode to electrode). As a result, the CMRR appears to be better when we add the $1\text{M}\Omega$ resistor in this scenario, but this improvement is somewhat random and minor. In a variety of other tests, the effects of introducing this mismatch varied between enhancing and diminishing the CMRR at lower frequencies. Therefore, it is essential to consider the overall performance and the consistency of the results across the entire frequency range of interest. That being said, the overall measured results confirm our expectation that the setup without the additional mismatch resistor exhibits better CMRR, particularly at 60Hz, which is a crucial frequency for wearable applications, due to the strong powerline interference that appears as a CM signal that needs to be removed.

Fig. 2.13 shows the measurement results of the lead-off detection circuit used to dis-

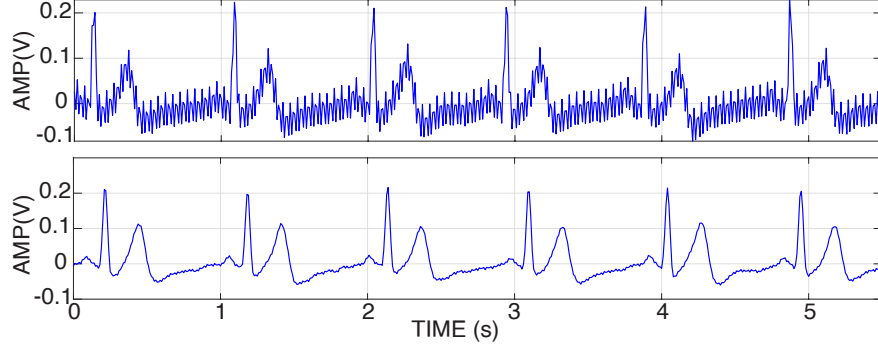


Figure 2.16: ECG measurement results without and with DRL loop.

connect AEs from the CM calculation circuit upon detection of a missing electrode-skin connection for that AE. As shown, the circuit generates a significantly different output peak-to-peak magnitude due to the large change in interface impedance, which relaxes the design requirement for the subsequent ADC.

Fig. 2.14 shows experimental results on the efficacy of the input DC adjustment loop. As shown in Fig 2.14(a), the loop successfully detects and incrementally corrects (through current-pulses' duty cycle adjustment) the intentional DC voltage change, and brings the input DC level back to 0.9 V - ideal for the LN-OTA operation. The averaging window used for DC calculation is programmable. Shorter windows would result in a faster DC correction at the cost of removing very low-frequency signal contents as well. As discussed, while the proposed AE architecture is inherently tolerant to input DC variations up to ± 350 mV, this feature further extends the maximum tolerance to input DC variations that could happen due to artifacts or electrostatic charges to ± 500 mV. Fig. 2.14(b) shows ECG recording measurement results illustrating that the presented circuit is unable to operate properly if the input DC offset is outside its tolerance range. It also shows how the DC adjustment loop corrects the DC level back to the acceptable range. It must be mentioned that for this (and

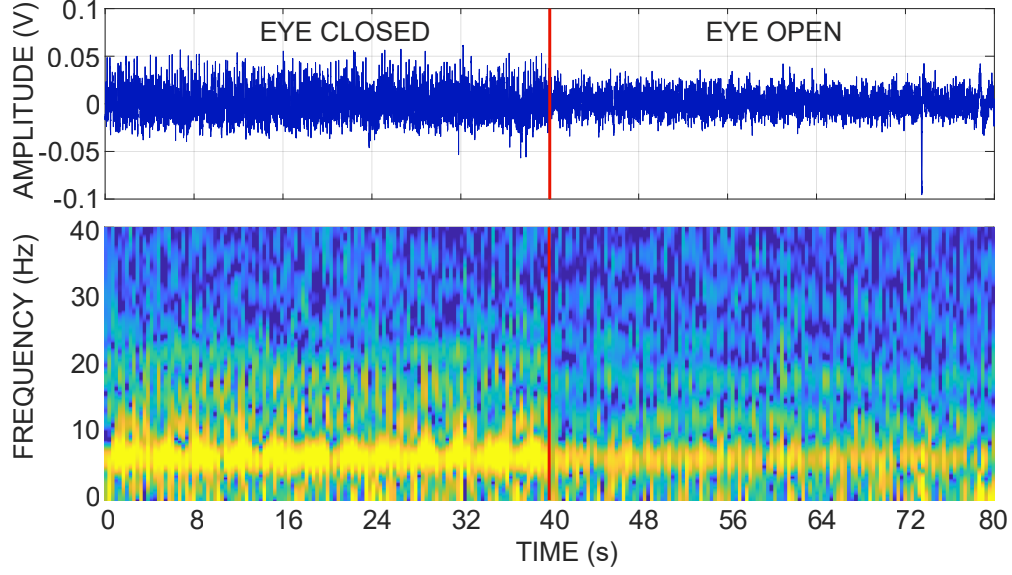


Figure 2.17: In-vivo EEG measurement results (time domain and the corresponding spectrogram) for closed and open eye situations, showing an increase in alpha band activity when the eye is closed.

the next two experiments), we used ECG recording (instead of EEG), mainly due to ECG's repetitive pattern that allows for clear illustration of issues discussed in these figures.

Fig. 2.15 shows the efficacy of the lead-off detection loop in improving the CM calculation and CMRR enhancement. As shown, once the lead-off detection loop is activated, the AE with a loose connection is detected and removed from CM calculations. This results in a short-time transient disturbance in the recording, which is followed by a significant improvement in CM rejection, hence a proportionally higher SNR for the recorded ECG signal. Similarly, Fig. 2.16 shows the ECG measurement result with and without the DRL loop being active, clearly illustrating its effectiveness in eliminating the effect of power-line noise.

Fig. 2.17 shows the experimental measurement result of in-vivo EEG recording using the presented active electrode (connected to a dry electrode). Two AEs were placed on the forehead and the setup was used to record two situations of "eye closed" and "eye open",

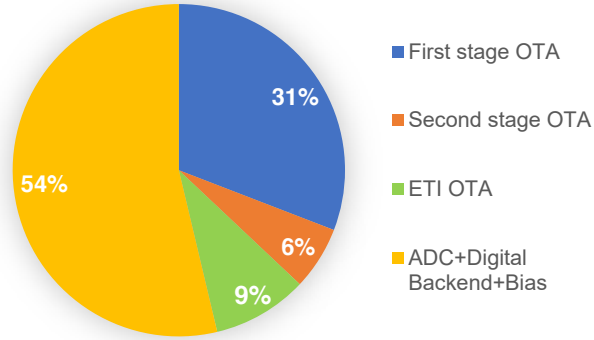


Figure 2.18: Pie chart of the power breakdown of both on-chip and off-chip components in the presented channel.

clearly showing the increased alpha-band activity for the former situation.

Table. 2.1 compares this work with the state-of-the-art active-electrode bio-signal recording microsystems in terms of system-level and circuit-level performance and features. While all recent works report a relatively-high CMRR, only one work reports this performance metric when there is a channel-to-channel mismatch ([35], in which the CMRR degrades by 60dB with 800 k Ω mismatch). Thanks to the proposed architecture, our design is the only work that can achieve an excellent CMRR even in the presence of significant mismatch between different AEs. The table also shows excellent noise performance as well as super-T Ω input impedance for the presented design. Additionally, for the presented design, the power consumption of each AE (including Analog front-end, digitization, and digital interface) adds up to 17.5 μ W, which is the lowest compared to the state of the art. Fig. 2.18 shows the breakdown of power consumption for the presented channel, taking into account both on-chip and off-chip components and the percentage of each block contribution in the total power consumption.

Table 2.1: Comparison with the state of the art AEs

	[47]	[40]	[35]	[56]	[57]	[48]	[36]	This work
Technology	0.18 μ	0.18 μ m	0.18 μ m	0.18 μ m	0.18 μ m	0.18 μ m	0.65 μ m	0.18 μ m
Application	EEG	EEG	EXG	ECG	EEG	EMG/ECG	EXG	EEG
Supply (V)	1.8	1.8	1.8	5	1.2	1.8	1.8	1.8
Power/Ch (W)	19.8 μ	82 μ	104.4 μ	155 μ	43 μ	43.8 μ	340.6 μ	17.5 μ
Voltage Gain (V/V)	3-100	11-101	140-14000	1-2.8-4.5-100	25-1200	55	NR	510
CMRR (dB) @50/60 Hz	82	84	102	70	100	76*	82	82.2
CMRR (dB) with mismatch	NR	NR	42 800k Ω	NR	NR	NR	NR	77.5 1M Ω
IIRN (μ V _{RMS}) (0.5-100Hz)	0.8	1.75	0.65	3.7	1.2	3.52	0.63	0.67
Bandwidth (Hz)	1k	200	200	10k	200	150	250	400
Offset Tolerance (mV)	R-to-R	$\pm$ 250	$\pm$ 350	R-to-R	$\pm$ 300	R-to-R	NR	$\pm$ 350 $\pm$ 500(DC ctrl)
Number of Wires	N	N	1Bus	N	1Bus	4	3	1Bus
Input Impedance	>2G Ω -	1.2G Ω @20Hz	1G Ω @1Hz	400G Ω @0.5Hz	720M Ω @50Hz	160M Ω @50Hz	100M Ω -	>1T Ω 5.5G Ω @DC @60Hz
Input DC control	No	No	No	No	No	No	No	Yes

N/R: Not reported. *:Post-layout simulation

Chapter 3

An Artifact-Resilient Active Electrode with In-Channel Dynamic-Range Boosting for EEG Recording

3.1 Introduction

In the preceding chapter, our focus revolved primarily around addressing two pivotal challenges in the design of Active Electrodes (AE) for dry-contact electrodes: (1) Enhancing the Common-Mode Rejection Ratio (CMRR) and (2) Reducing the quantity of interconnecting wires. In response to these challenges, we introduced an innovative EEG recording system characterized by a distributed configuration. In this chapter, we will discuss additional challenges mainly rooted from the presence of motion artifact when dealing with dry contact electrode and long term brain monitoring applications. Additionally, we have further im-

proved the prior design in terms of CMRR boosting as well as including new features such as auto ranging, high resolution digitization with a noise shaping SAR ADC and in-AE feature extraction and classification (i.e., further explained in the next chapter).

Considering that with the target EEG recording device the aim is to provide a fast, low-cost, and medically-relevant alternative to the existing clinical setups [41, 42], rigid/flexible dry (i.e., gel-free) contact or non-contact electrodes are utilized, which comes at the cost of having a significantly higher and more variable interface impedance due to the less-stable electrode-skin connection. The impedance variations result in fairly-large fluctuations in the signal's magnitude and DC level, commonly known as *motion artifacts* [58, 59]. Since any physical activity of the patient (e.g., talking, chewing, etc.) could cause electrode movements, hence impedance variation, motion artifacts are considered random in nature both in terms of occurrence rate and severity.

As shown in Fig. 3.1(a), conventionally various digital signal processing (DSP) pattern recognition algorithms have been used to extract motion artifacts in recorded bio-signal (e.g., electrocardiography (ECG)) recordings. These techniques primarily rely on pattern recognition algorithms to detect and remove artifacts from the recorded bio-signal. One of the most common approaches used is the independent component analysis (ICA), which is a blind source separation technique that decomposes the bio-signals into statistically independent components. By identifying and discarding components associated with artifacts, ICA effectively suppresses unwanted noise [60]. The next approach is the wavelet-based methods which decompose the bio-signals into multiple frequency bands, enabling the selective re-

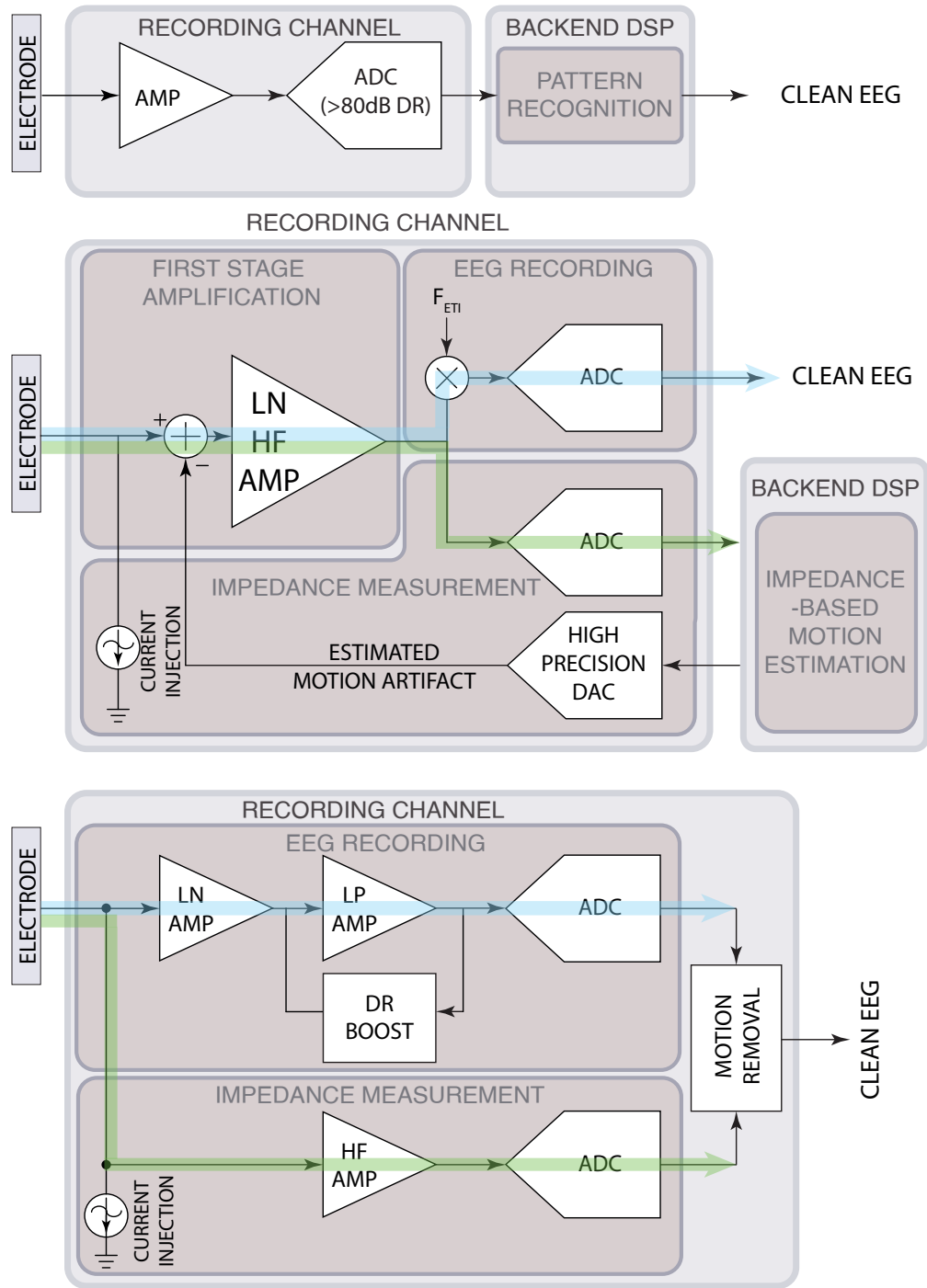


Figure 3.1: Simplified block diagram of conventional methods used for motion artifact removal using (a) pattern recognition and (b) impedance-based artifact estimation. (c) Top-level block diagram of the proposed in-channel DR-Boosting and motion artifact extraction and removal.

removal of artifact-related components [61]. Adaptive filters are the other common approach that are designed to eliminate artifacts by dynamically adjusting their coefficients based on the input signal [62]. However, these DSP-based methods are more suited for ECG signal and face several limitations for removing motion artifacts in EEG signals [37–39]. The main reason is that, unlike ECG signals, EEG signals do not have a distinct, repetitive pattern, making it challenging for conventional DSP algorithms to accurately distinguish between artifacts and actual EEG signals. Additionally, the significant amplitude differences between artifacts (~ 10 mV) and EEG signals (~ 10 - 100 μ V) require high-dynamic-range recording circuits, resulting in power-hungry solutions. Furthermore, DSP techniques can distort or remove underlying EEG activity, be computationally intensive, and introduce latency due to complexity, making them less suitable for portable, low-power EEG systems [63, 64]. Moreover, their performance often relies on proper parameter tuning, which may require expert knowledge or calibration with clean reference data, limiting applicability in real-world scenarios.

Fig. 3.1(b) shows a popular alternative approach, in which high-frequency (out of EEG band) current pulses are injected to the skin and the resulted voltage is recorded to measure the interface impedance, which is used to estimate the real-time magnitude of motion artifacts. The estimated artifact is then subtracted from the amplifier’s input to significantly reduce its dynamic range. To prevent any risk of instability and signal distortion, the overall latency of the feedback loop has to be made strictly small, which comes at the cost of limiting the estimator’s complexity, hence its accuracy [41]. Poor artifact estima-

tion leads to subtraction residues that are larger than the actual EEG signal (i.e., signal drown in noise). Therefore, while the amplifier saturation is avoided, the EEG activity is lost. The estimation accuracy also depends on the resolution and speed of the digital-to-analog converter (DAC) that converts the estimated artifact back to the analog domain to be subtracted from the input signal. Typically, power constraints prevent from employing a high-resolution high-speed DAC (e.g., digital signal processing and 12-bits DACs require $54 \mu\text{W}$ for 3-channel ECG recording [41]). Additionally, measuring the EEG signal and the electrode-tissue impedance through the same path require an OTA that is both low noise and have high bandwidth which results in high power consumption in this structure.

Fig. 3.1(c) shows the proposed approach which has in-channel motion removal. The upper path (signal path) involves a two-stage amplification process. By implementing two sequential amplification stages, the required DR for the ADC is reduced in comparison to the first structure. However, the increased gain from this configuration could potentially lead to saturation at the output of the second amplification stage. To counteract this, a DR boosting circuit has been incorporated within the architecture.

One advantage of this design over the previously discussed approach is the elimination of the need for a high-precision DAC, since the signal has already been amplified. Moreover, the DR boosting mechanism operates independently of any processed data, which alleviates concerns regarding the complexity and latency that may be associated with motion estimation and artifact removal algorithms. The other advantage is that, the EEG signal and the electrode-tissue impedance are captured through distinct pathways. This necessitates the

use of two separate OTAs, each tailored to its specific function. One OTA is optimized for low noise performance, foregoing the need for high bandwidth, while the other prioritizes high bandwidth without the requirement for low noise characteristics. Consequently, both OTAs can be designed to operate with minimal power consumption. This separation and specialization of signal paths allow for efficient and effective design of specific OTA for each path.

3.2 System-Level Architecture

Fig. 3.2 shows the comprehensive top-level system-level architecture of the presented active-electrode IC, optimized for EEG recording. The system is designed to interface directly with the electrode through a DC coupling, ensuring a very high input impedance (Z_{in}), which is essential to avoid signal attenuation, particularly when using dry-contact electrodes that are common in outpatient wearable devices.

The common-mode signal (V_{cm}), is constructed by averaging the input signals from all AEs. This averaging is accomplished through a passive network consisting of C_{cm} capacitors, each of which is linked to the inverting input of the OTA within its respective AE. The opposite terminals of these capacitors converge at a shared node (V_{cm}), which is then connected to a bias voltage via a resistor (located on a distinct board). This V_{cm} voltage is used to drive the reference electrode, enhancing the common-mode rejection (CMR). Additionally, V_{cm} is input into the second stage of amplification, where it is amplified by a gain specific to each AE. This gain is variably set to counteract any imbalances due to mismatches in Z_{in} between AEs, thereby optimizing CM averaging. The gain is adjusted with 8-bit precision

during the device’s calibration mode.

To circumvent saturation caused by motion-induced artifacts, a level-crossing auto-ranging strategy is employed within the second amplification stage. This scheme actively monitors the output, and upon detecting voltage levels crossing predefined thresholds ($\pm 150\text{mV}$), it promptly adjusts the input voltage via a 6-bit voltage DAC and capacitive charge sharing, effectively constraining the dynamic range at the output of the G_{m2} . For extremely large artifacts, a similar level-crossing detection mechanism is utilized at the output of G_{m1} to identify saturation and modulate the closed-loop gain accordingly. Additionally, the amplifiers are followed by a 60Hz notch filter to attenuate the effect of power-line artifact.

In parallel, electrode-tissue impedance (ETI) is measured through a separate path that utilizes a current-mode DAC (IDAC) with an exceptionally high output impedance achieved through triple cascoding, thus preventing any degradation in Z_{in} . The voltage generated from this measurement is amplified and relayed to a switched-capacitor peak-to-peak detection circuit, producing a signal that varies only with changes in ETI. This design significantly reduces the speed requirements for the subsequent ADC. Moreover, a feedback control loop is present to maintain the DC level at the electrode by applying intentional anodic/cathodic mismatches to the IDAC’s output pulses, thereby ensuring the DC level remains at an optimal value. The ETI data serves to estimate and mitigate artifacts within the EEG signal prior to feeding it into the feature extraction unit.

As shown in Fig. 3.2, the output of signal path is connected to a 13-bit noise shaping SAR ADC. The digital output from this ADC is used for reconstruction of the original sig-

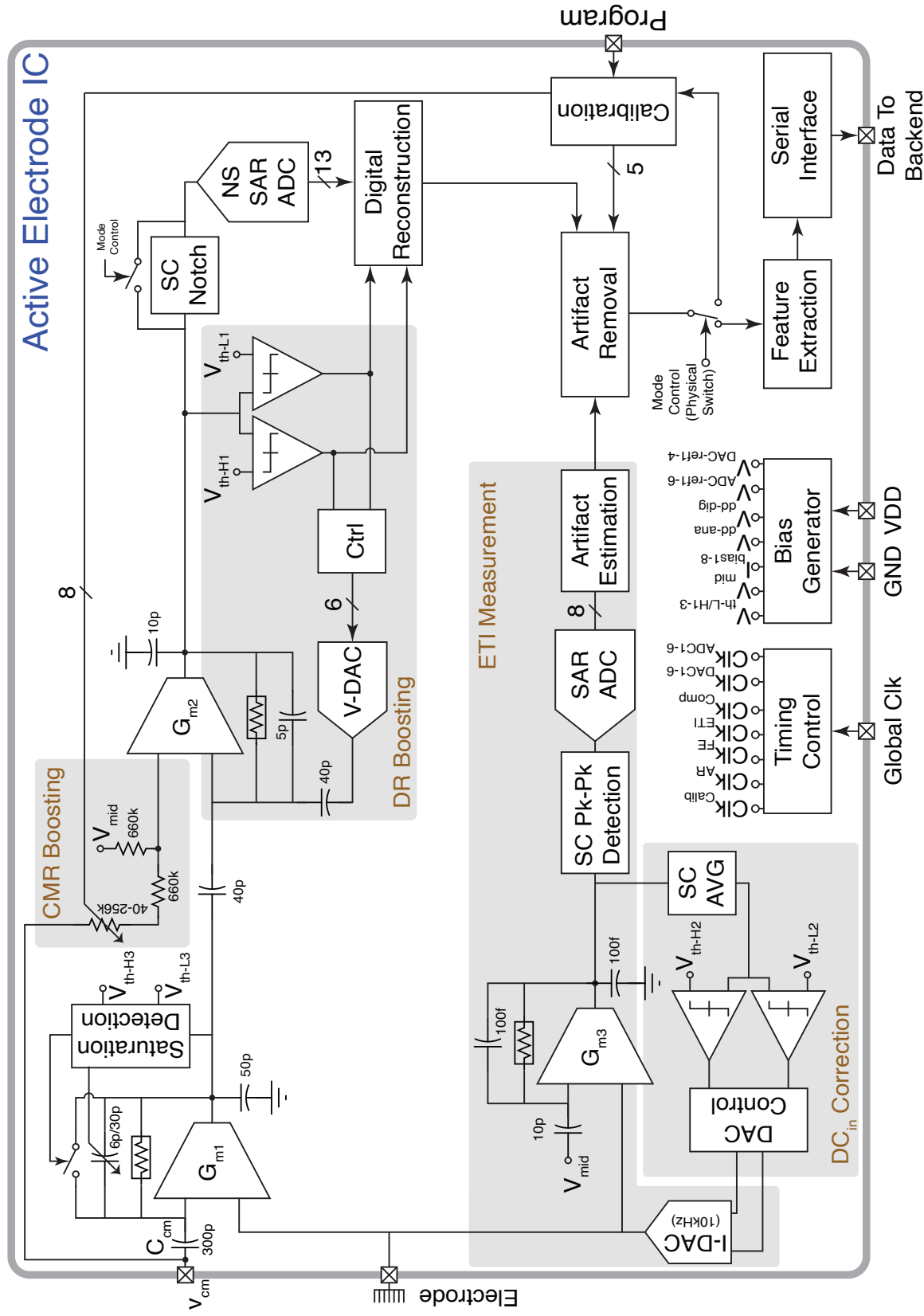


Figure 3.2: Top-Level circuit implementation of the AE IC featuring high DR amplification, quantization, CMR boosting, motion artifact removal, and input DC correction.

nal, where any distortions introduced by the DR boosting stage are removed to restore the signal. Simultaneously, the ETI measurement path feeds its output to a separate 8-bit SAR ADC. The digital data derived from this ADC is used in the elimination of artifacts from the reconstructed signal. By doing so, the system ensures that the EEG signal is swept out of any motion-induced artifacts. As a result, clean signal is used in the feature extraction and serial interface blocks which will be elaborated in chapter 4

To fine-tune this process, the system undergoes a calibration phase, which can be initiated when necessary. During calibration, the ETI signal is manipulated by adjusting its gain and delay, with 5-bit and 8-bit precision respectively. These adjustments aim to maximize the Pearson correlation between the ETI signal and a DC signal. This calibration is critical as it establishes the most accurate parameters for estimating the impact of motion artifacts on the EEG signal. By identifying the settings that yield the highest correlation, the system can more precisely compensate for motion-induced artifacts. Additionally, the division ratio for the CMR boosting block is also determined during this calibration step.

3.3 Circuit-Level Implementation

In this section, we focus on the circuit-level implementation of each of the blocks introduced in the system-level block diagram under EEG recording and ETI measurement paths, the noise-Shaping SAR ADC and motion artifact removal sections.

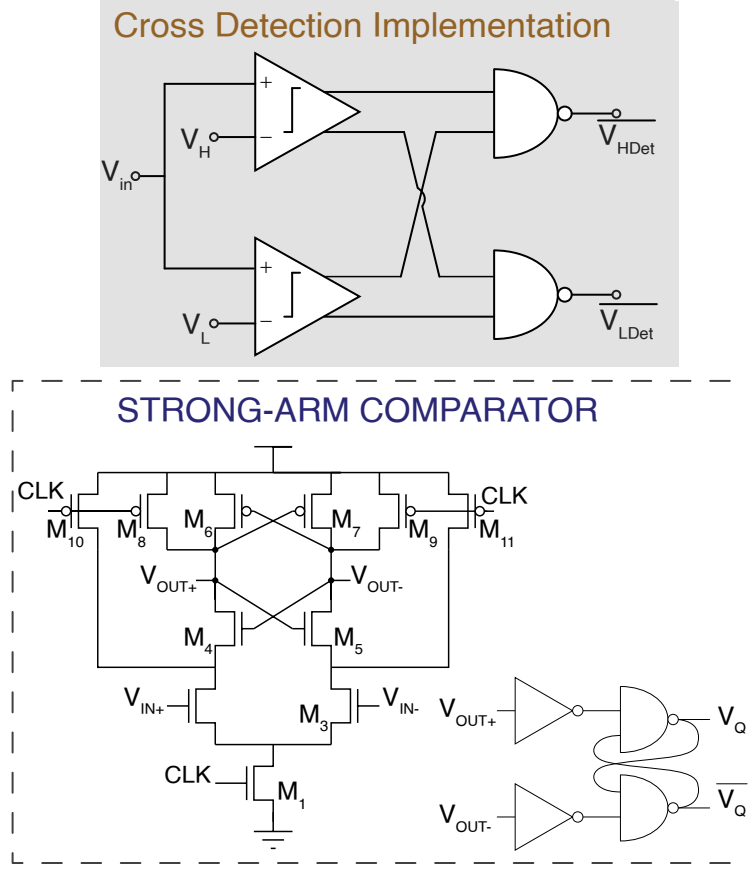


Figure 3.3: (a) Circuit-level implementation of saturation detection and (b) the schematic of the employed strong-arm comparator followed by a latch to store the result of the comparison.

3.3.1 EEG Signal Recording

In this part we focus on the signal recording path from the first stage of amplification stage, its associated saturation detection, second stage of amplification and the associated DR boosting and the 60-Hz notch filter.

3.3.1.1 First Stage of Amplification and Saturation Detection

Amplification in the first stage is achieved through a DC-coupled configuration, utilizing a OTA with the same structure as Fig. 2.7. A notable enhancement in this stage is the in-

troducton of a variable gain feature, designed to address instances where high amplitude input voltages may lead to saturation. To detect such saturation, a dedicated component is employed following the first amplification stage. This saturation detection mechanism is composed of a pair of Strong-arm comparators that are tasked with monitoring for voltage levels that exceed predetermined thresholds. Upon detecting such voltage levels, these comparators trigger a response to dynamically adjust the gain, from an initial 50V/V to 10V/V. In addition to gain reduction, reset signals are also generated to initialize the output of the first stage. Fig. 3.3 details the circuit-level design of this saturation detection system. It showcases the practical implementation of the control logic and the schematic of the employed Strong-arm comparator followed by a latch to keep the comparator output and eliminate the reset phase.

3.3.1.2 Second Stage of Amplification and DR Boosting

As shown in Fig. 3.4, the second stage is a AC-coupled configuration to avoid the amplification of the first stage DC content. The OTA's positive input is connected to a fraction of the common-mode (CM) signal, which aids in CMRR enhancement (details of which will be elaborated in the CMRR boosting section). In scenarios involving motion artifacts, signal amplitudes can escalate beyond a few millivolts, potentially saturating the recording system's output. This issue could be mitigated by reducing the gain of the first stage, though this would degrade the SNR of the entire system. In this structure, we try to maintain the gain at a high level of 50V/V for the first stage, while preventing saturation. The strategy

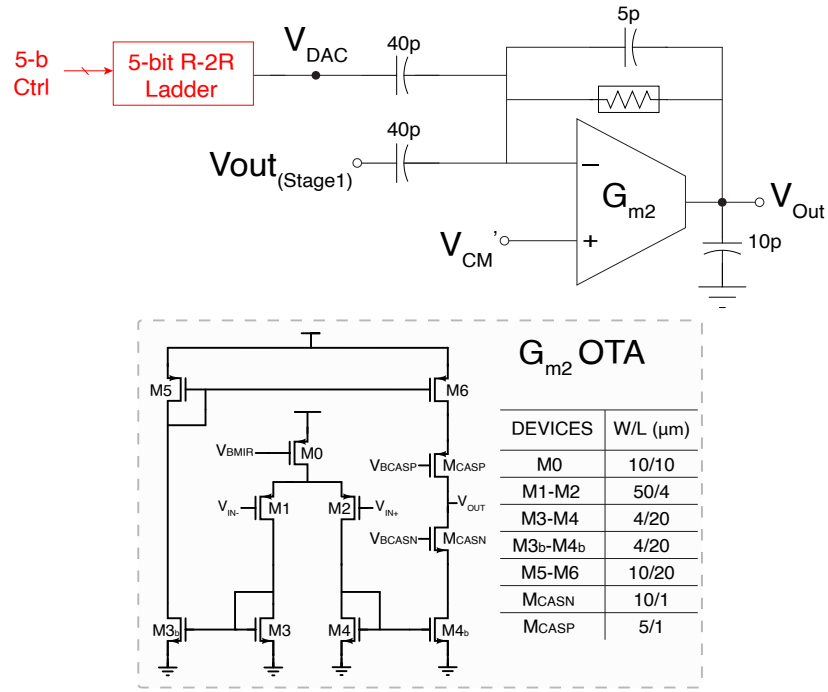


Figure 3.4: Circuit-level implementation of the AC-coupled OTA in the second stage highlighting the required DAC for the implementation of our target DR boosting scheme and the schematic of the employed OTA accompanied by the transistors' sizing table.

involves maintaining the output of the second stage within a predefined range, employing a cross detection block to monitor and identify when the output strays beyond this range. Upon detection, the cross detection block activates a signal that controls a 5-bit R-2R ladder resistive DAC to adjust the signal level at the OTA's input. Therefore, to change the output level, the sudden change in the DAC output voltage is transferred to the output with the OTA gain. The OTA utilizes a negative gain sign for the signal; hence, when the output hits the low/high threshold, the DAC produces a corrective step to increase/decrease the level, ensuring the output is within the desired range.

3.3.1.3 Digital Reconstruction

Within the system architecture, the output from the cross-detection block is combined with the digitized output from the Noise shaping SAR ADC (explained in detail in section 3.3.3) in the digital reconstruction block. This process is designed to accurately reconstruct the true signal, which may potentially surpass the supply voltage. The reconstructed signal is then used in the motion artifact removal stage. During the auto-ranging operation, when the DAC produces a step, the step's amplitude is $VDD/2^6 = 28.125$ mV. This increment/decrement manifests at the output with an amplitude of 225 mV, owing to the 8V/V gain of the second amplification stage. This particular gain was chosen as a power of two, allowing the multiplication process of the DAC digital input to be efficiently realized using a shift register in the digital domain. Therefore, as depicted in Fig. 3.5, the DAC digital input is first shifted by 3 bits to account for the analog gain of 8 in the signal path and then shifted by 7 bits which is the difference of the resolution of the SAR ADC (13) and the feedback DAC (6). In other words the DAC's least significant bit (LSB) is 2^{10} times larger than the ADC's LSB so we implement a total shift of 10 bits. Consequently, the output from the reconstruction block is rendered in a 16-bit format, ensuring that the digital signal precisely represents the actual analog input if there was no auto-ranging procedure which would have saturated the amplifier as it is higher than the VDD value but has been kept within the range thanks to our auto-ranging scheme.

Digital Reconstruction

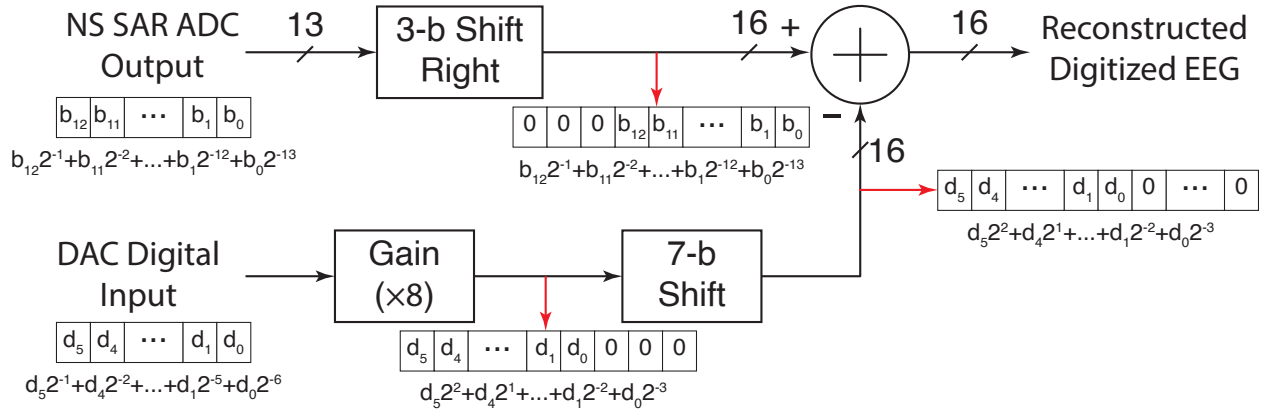
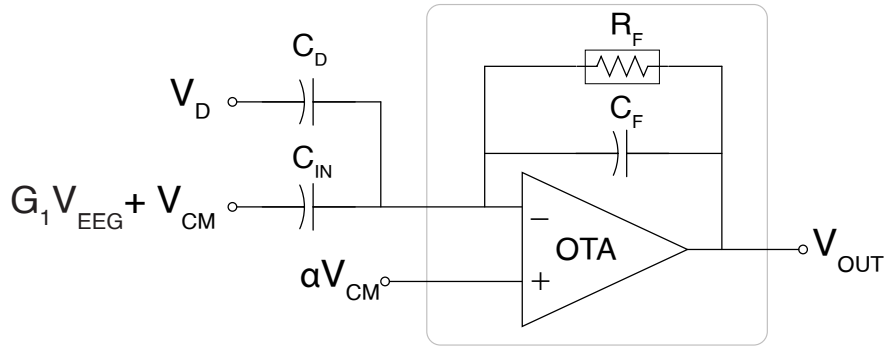
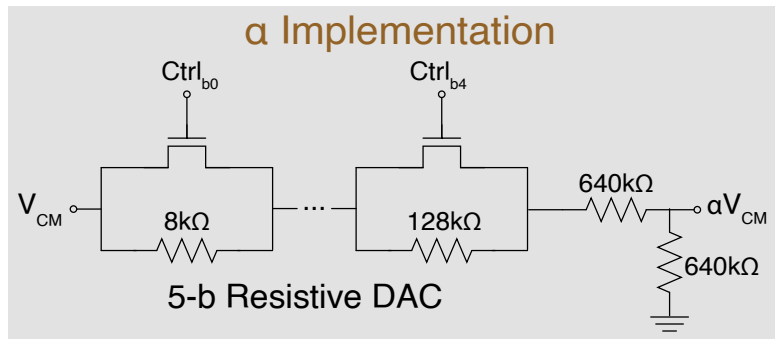


Figure 3.5: Digital implementation of signal reconstruction using the output of the NS SAR ADC and the DAC digital input.



(a)



(b)

Figure 3.6: (a) The circuit-level implementation of the CMRR enhancement scheme and (b) the implementation of the α coefficient.

3.3.1.4 CMRR Enhancement

As we discussed in chapter two, in the previous CMRR enhancement structure we enforce common mode gain to be one in first and second stage. Fig. 3.6(a) shows the second stage of CMRR enhancement in the modified structure. In this structure, the gain of V_{CM} at the output of the first stage is unity but due to the presence of the DR boosting capacitor C_D , the output of the second stage can be calculated as:

$$V_{OUT} = \alpha \left(\frac{C_{in} + C_D}{C_F} + 1 \right) V_{CM} - (G_1 V_{EEG} + V_{CM}) \frac{C_{in}}{C_F} - V_D \frac{C_D}{C_F}. \quad (3.1)$$

where αV_{CM} is the voltage at the non-inverting input of the second stage OTA and G_1 is the gain of first stage. Therefore, in order to remove V_{CM} at the output of the second stage α can be calculated as:

$$\alpha = \frac{C_{in}}{(C_{in} + C_D + C_F)}. \quad (3.2)$$

It is important to consider that due to variations in the electrodes, the common-mode voltage, V_{CM} , may be sensed differently at the input or amplified variably at the output across different electrodes. To compensate for this discrepancy, the coefficient α , rather than being a fixed value, is implemented as an adjustable parameter. This adjustment is facilitated by a 5-bit resistive DAC, as illustrated in Figure 3.6(b). During the calibration phase, the objective is to fine-tune α such that the 60Hz content of the signal is minimized as much as possible.

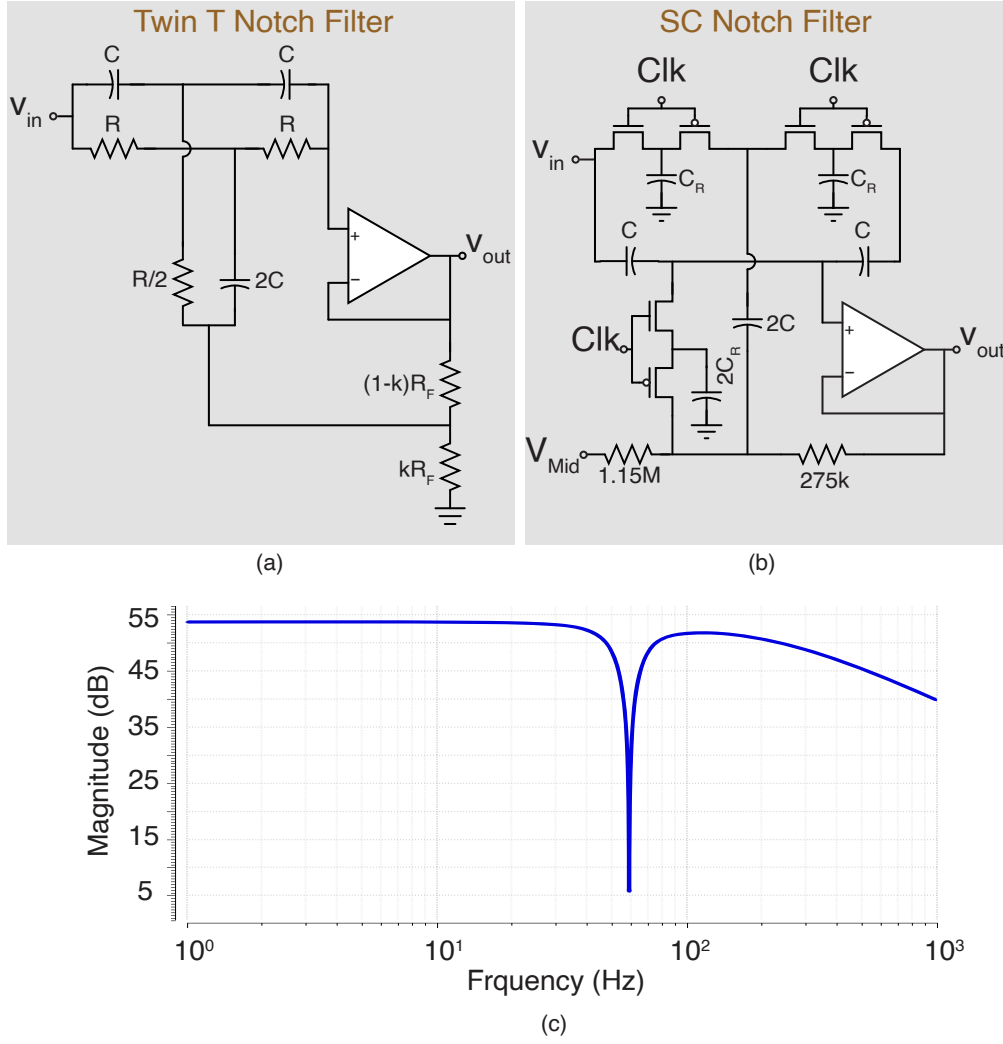


Figure 3.7: (a) The circuit-level implementation of Twin-T notch filter, (b) the proposed switched-capacitor based implementation of the notch filter, and (c) the result from the periodic alternative current (PAC) simulation confirming the 60-Hz attenuation.

3.3.1.5 Notch Filter for 60-Hz Removal

Even with a the CMRR boosting which has been explained, the system cannot reach to 80dB CMRR in some conditions due to the very large effect of power-line artifacts. Therefore, a notch filter is implemented after the second stage to take care of these extreme cases. This filter in the calibration mode will be bypassed to help the calculation of the best control logic of α for CMR boosting block.

Fig. 3.7(a) shows a conventional active twin-t notch filter [65]. In this structure the frequency and the quality factor of the notch filter can be calculated as:

$$f_0 = \frac{1}{2\pi RC} \quad Q = \frac{1}{4(1-k)}. \quad (3.3)$$

As the notch frequency in our design is 60Hz, for a C=15p (in total 60p for all the three capacitors) the resistor should be 177M which is not practical to be implemented on chip due to the area constraints. Considering the high value for the resistor and also the fact that it should be programmable to adjust the values to set the center frequency in presence of any mismatch between the capacitor sizes, the switched-capacitor is a great candidate to implement the resistors in this filter. Our proposed switched-capacitor based twin-t 60Hz notch filter has been shown in Fig. 3.7(b). In this structure, except the voltage divider resistors, others have been implemented with switched-capacitor circuit. As the resistance of a switch capacitor is $1/C.f_{clk}$ so the notch frequency is:

$$f_0 = \frac{f_{CLK}C_R}{2\pi C}. \quad (3.4)$$

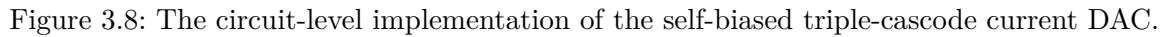
Fig. 3.7(c) illustrates the outcome of a Periodic Alternating Current (PAC) simulation, which confirms the effectiveness of the filtering system at 60 Hz. A pronounced notch is visible at the 60 Hz frequency, indicating a substantial attenuation of the signal at this frequency, which is crucial to reduce the power-line associated artifacts.

3.3.2 ETI Measurement

In this section we focus on the ETI measurement path. In order to measure the motion artifact, it is necessary to first assess the electrode-skin impedance, then translate impedance fluctuations into identifiable motion artifacts. This is achieved by applying a sink-source current to the electrode and monitoring the induced voltage at the electrode interface. Since the frequency of this impedance-related signal is significantly higher than that of the EEG signal, it does not interfere with the EEG recording. The injection of the high-frequency current is implemented by a current-mode DAC with high output impedance to avoid degrading the AE's input impedance. A feedback loop also dynamically adjusts the IDAC's sink and source intervals, ensuring optimal DC levels at the electrode-tissue interface. The voltage derived from the impedance measurement is amplified and fed to a switched-capacitor peak-to-peak detection circuit, yielding a signal that fluctuates solely in response to variations in ETI, which significantly relaxes the operational speed needed for the following ADC.

3.3.2.1 Triple-Cascode Current DAC

Fig. 3.8 shown the schematic of the current-mode DAC employed to sink/source current to the electrode-tissue interface. A 3-bit IDAC is utilized to supply variable current amplitude levels, ensuring compatibility with electrodes of differing impedances. Furthermore, to prevent any degradation of the AE's input impedance, the Current DAC (operating in parallel with the AE's input impedance) employs a triple cascode structure. This design achieves an ultra-high output impedance, ensuring the addition of the ETI measurement circuitry does



3.3.2.2 Electrode-Tissue Interface DC correction

Fig. 3.9(c) presents the voltage input alongside the control pulses controlling the switches. During the initial phase (φ_1 and φ_2), the peaks and valleys of V_{in} are captured in capacitors

C_1 and C_2 , respectively. Subsequently, in the final phase, (φ_0), the average of these voltages is computed and stored in C_{out} . The capacitance of C_{out} is chosen to be several orders of magnitude larger than that of C_1 and C_2 , which ensures the voltage at V_{out} represents the DC level of the input signal V_{in} .

3.3.2.3 Motion Extraction through Peak-to-Peak Detection

The signal generated at the output of the ETI measurement OTA has a 10 kHz frequency, which is orders of magnitudes higher than the frequencies associated with motion artifact signals. Direct connection of this high-frequency signal to the ADC would lead to unnecessary power consumption, as the ADC would be required to handle a signal of much higher frequency than needed for motion artifact analysis.

To address this, the output of the ETI is first processed to determine the peak-to-peak value using a switched-capacitor circuit, followed by an average calculation of these values within the analog domain. This process of peak-to-peak calculation is facilitated by a switched-capacitor based block as demonstrated in Fig. 3.9(b). The operation of this circuit is similar to the averaging block (Fig. 3.9(a)), as it captures the peak and valley of the input voltage (V_{in}) on capacitors C_1 and C_2 . The key distinction is that in the final phase, the voltage difference is stored on C_0 by connecting the C_1 and C_2 with opposite polarities. The frequency response of both circuits is influenced by the ratio of the sampling capacitor to the storage capacitor. To better clarify the concept of the frequency response, we can consider the simplified structure of a passive sample and hold circuit shown in Fig. 3.9(d), where the

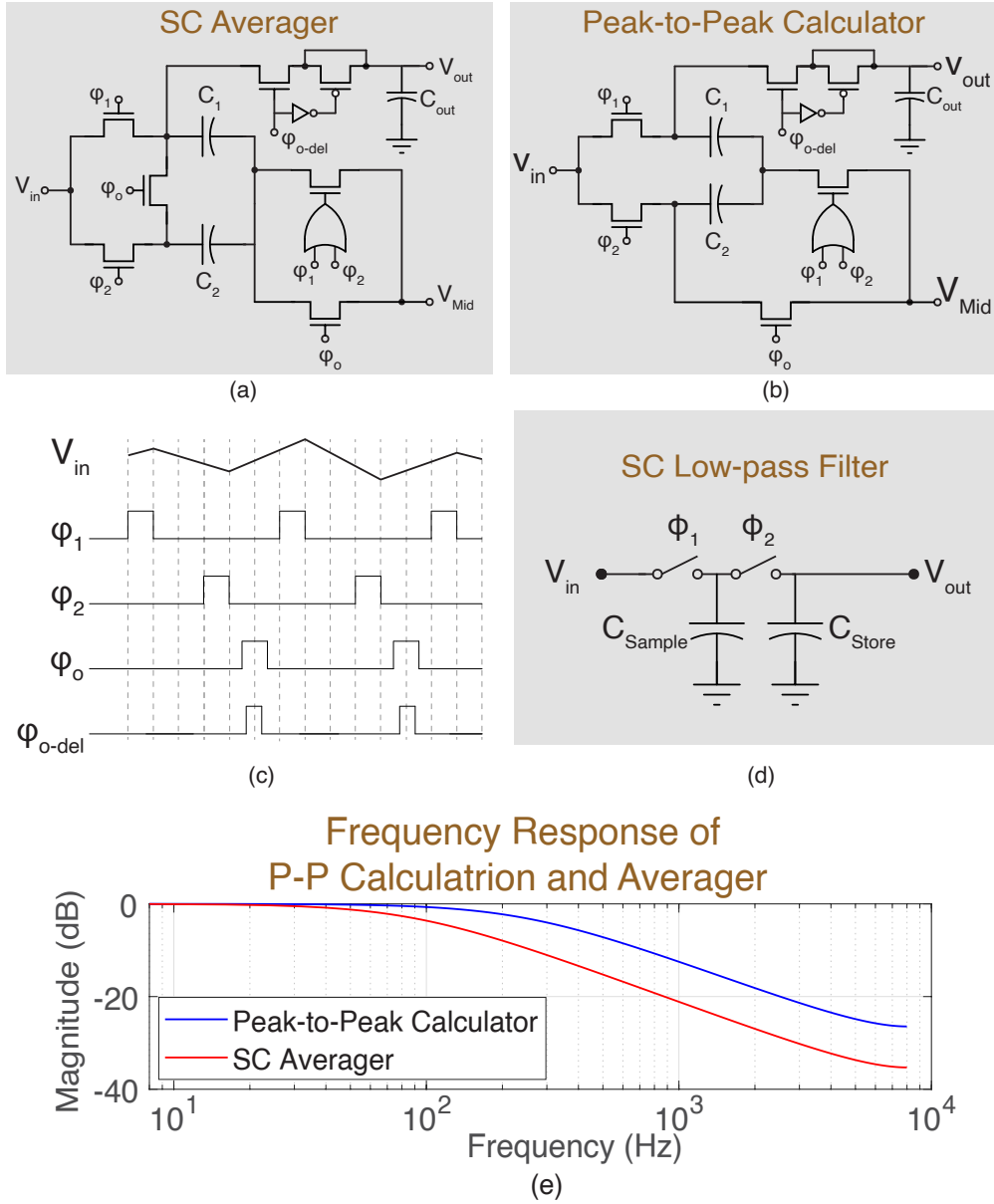


Figure 3.9: (a) Circuit-level implementation of switched-capacitor based average calculator, (a) Circuit-level implementation of switched-capacitor based peak-to-peak calculator, (c) The timing diagram showing the relative timings of the operation phases, (d) the simple structure of a passive sample and hold circuit, and (e) the frequency response of the average and peak-to-peak calculator circuits.

output voltage is calculated as:

$$V_{OUT}[n] = \frac{C_{smp}}{C_{smp} + C_{store}} V_{in}[n] + \frac{C_{store}}{C_{smp} + C_{store}} V_{out}[n-1]. \quad (3.5)$$

In the z domain we can calculate output as :

$$V_{OUT} = \frac{1 - \alpha}{1 + \alpha z^{-1}} V_{in}, \quad (3.6)$$

where α is $C_{store}/(C_{smp} + C_{store})$. Fig. 3.9(e) illustrates the frequency response of two passive sample-and-hold circuits with capacitor sizes corresponding to the values used in the switched-capacitor based DC and peak-to-peak calculation blocks.

3.3.3 Noise Shaping SAR ADC

In this section, we focus on the design and implementation of the noise shaping SAR ADC, a crucial component in our system's design. Despite the utilization of DR boosting and dual-stage amplification, there are extreme scenarios where gain reduction is necessary to prevent saturation, which would require an ADC with at least 13-bit of resolution based on the target minimum input amplitude. Understanding the necessity of a 13-bit resolution for our system, it becomes crucial to select an ADC that can meet this requirement efficiently, especially in terms of power consumption. Charge-redistribution SAR ADCs are typically the go-to choice for applications demanding moderate resolution and bandwidth while being highly conscious of power usage. However, scaling a SAR ADC to achieve a high resolution,

such as the required 13-bit in our case, introduces significant challenges.

As we push for resolutions beyond approximately 10 bits, the precision of SAR ADC's circuit components, particularly the matching of DAC capacitors, starts to limit the overall performance. This mismatch can lead to notable degradation in the converter's efficiency, posing a considerable challenge in maintaining low power consumption while achieving high resolution [66].

To circumvent these limitations, we opted for a hybrid architecture that combines the benefits of both SAR and Delta-Sigma Modulator (DSM) architectures [67]. This hybrid approach allows us to harness the low power consumption characteristic of SAR ADCs, while also attaining the high-resolution capability of DSM architectures through its noise shaping capability. Consequently, our design incorporates a 13-bit noise shaping SAR ADC, effectively balancing the need for high resolution and low power consumption.

3.3.3.1 Structure of the Noise-shaping SAR ADC

Fig. 3.10(a) illustrates a standard 5-bit tri-level single-ended SAR ADC. During the sampling phase, the top plates of all capacitors are connected to V_{CM} , and their bottom plates are linked to V_{IN} to capture the sample (this is known as bottom plate sampling). Subsequently, in the next phase, the bottom plates of the capacitors are connected to V_{CM} . This configuration generates a voltage of $V_{RES} = 2V_{CM} - V_{IN}$ at the negative input of the comparator.

The voltage at V_{RES} is then compared with V_{CM} , and the comparison result is stored in the SAR registers as the most significant bit (MSB). Following this, depending on the

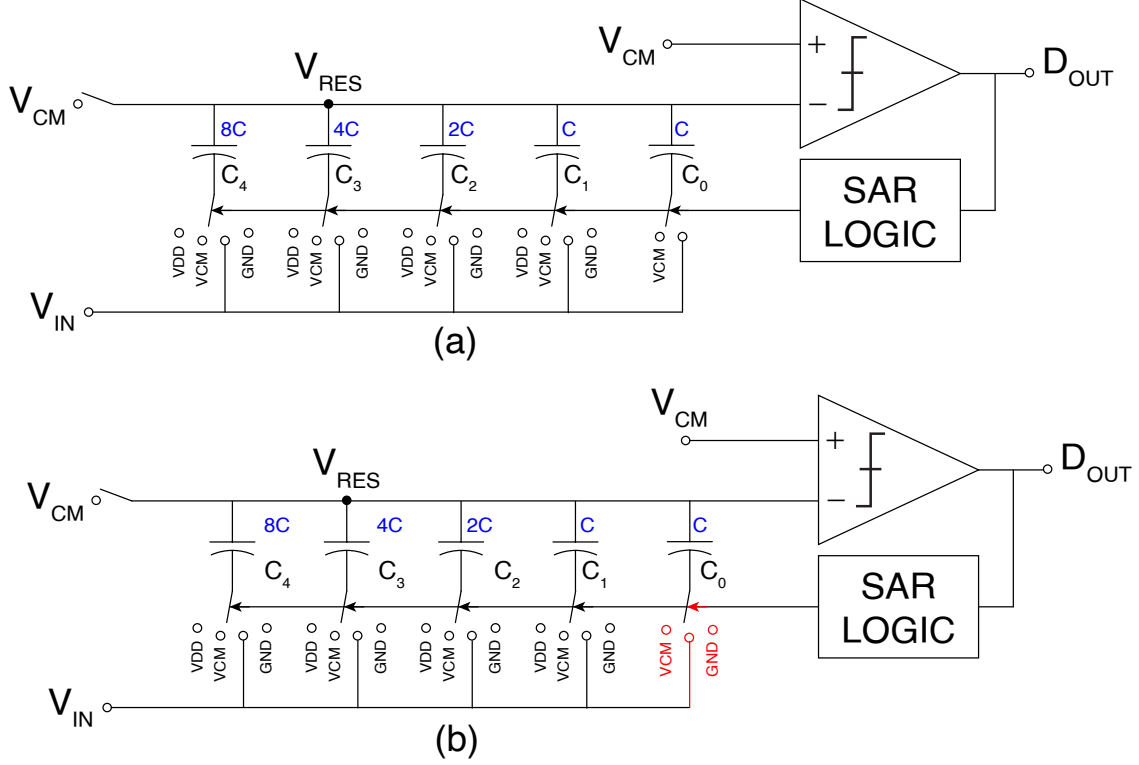


Figure 3.10: Structure of the capacitive DAC switching in (a) conventional SAR ADC and (b) noise-shaping SAR ADC.

outcome of the comparison, the bottom plate of capacitor C_4 is connected either to VDD (the supply voltage) or to the ground. This action either increases or decreases the voltage at V_{RES} for the subsequent bit conversion. Assuming $V_{CM} = VDD/2$, by the conclusion of the 5-bit conversion process, the voltage at V_{RES} will be:

$$V_{RES} = \frac{VDD}{2} - V_{IN} + d_4 \frac{VDD}{2} + d_3 \frac{VDD}{4} + d_2 \frac{VDD}{8} + d_1 \frac{VDD}{16} + \frac{VDD}{32}. \quad (3.7)$$

The fundamental principle of a noise shaping ADC revolves around filtering the difference between the input voltage (V_{IN}), and its quantized output (D_{OUT}). Based on Equation 3.7 V_{RES} is close to $V_{IN} - D_{OUT}$, but it doesn't yet account for the influence of the final

decision on the voltage value. To address this, an additional switch for capacitor C_0 has been integrated, as depicted in Figure 3.10(b). This switch is adjusted in its final position compared to earlier conversions. Specifically, if the last bit b_0 is 0, then C_0 remains connected to V_{CM} ; otherwise, it connects to the ground. Through this mechanism, we achieve:

$$V_{RES} = \frac{VDD}{2} - V_{IN} + d_4 \frac{VDD}{2} + d_3 \frac{VDD}{4} + d_2 \frac{VDD}{8} + d_1 \frac{VDD}{16} + d_0 \frac{VDD}{32}. \quad (3.8)$$

To effectively eliminate quantization noise, the system depicted in Figure 3.10(b) undergoes a modification where the comparator's input, instead of being V_{CM} , becomes the integration of $V_{IN} - D_{OUT}$ plus the V_{CM} . This integration is realized by placing a switched-capacitor integrator between V_{RES} and the comparator, as shown in Fig. 3.11(a). The overall block diagram of the ADC is illustrated in Fig. 3.11(b), and its Noise Transfer Function (NTF) and Signal Transfer Function (STF) are calculated as follows:

$$NTF = 1 - Z^{-1}, \quad STF = 1. \quad (3.9)$$

These adjustments and the introduction of the noise shaping mechanism are key to enhancing the ADC's performance, particularly in terms of reducing quantization noise and improving overall resolution.

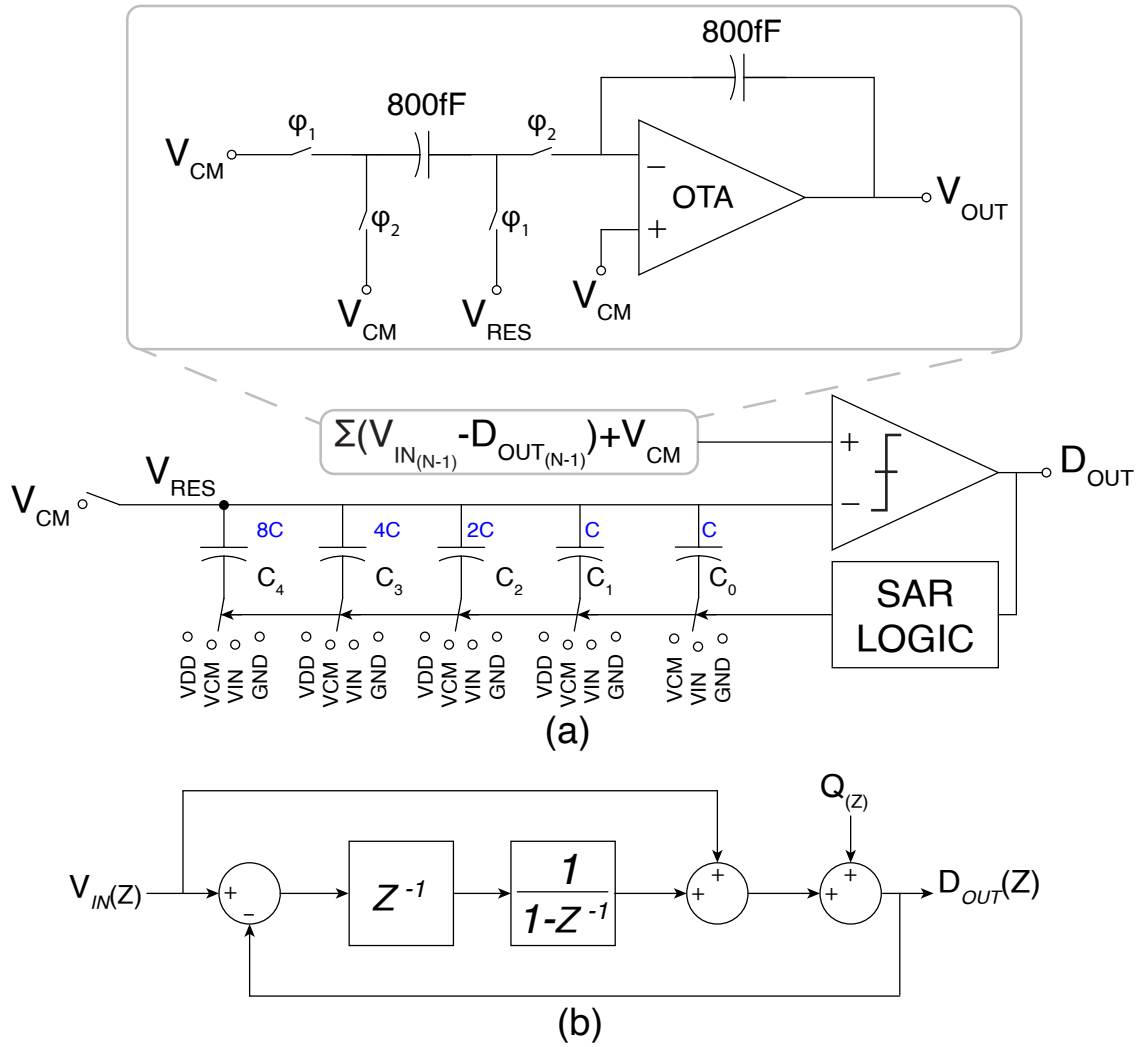


Figure 3.11: (a) Implementation of noise-shaping SAR ADC and (b) block-diagram of noise-shaping SAR ADC.

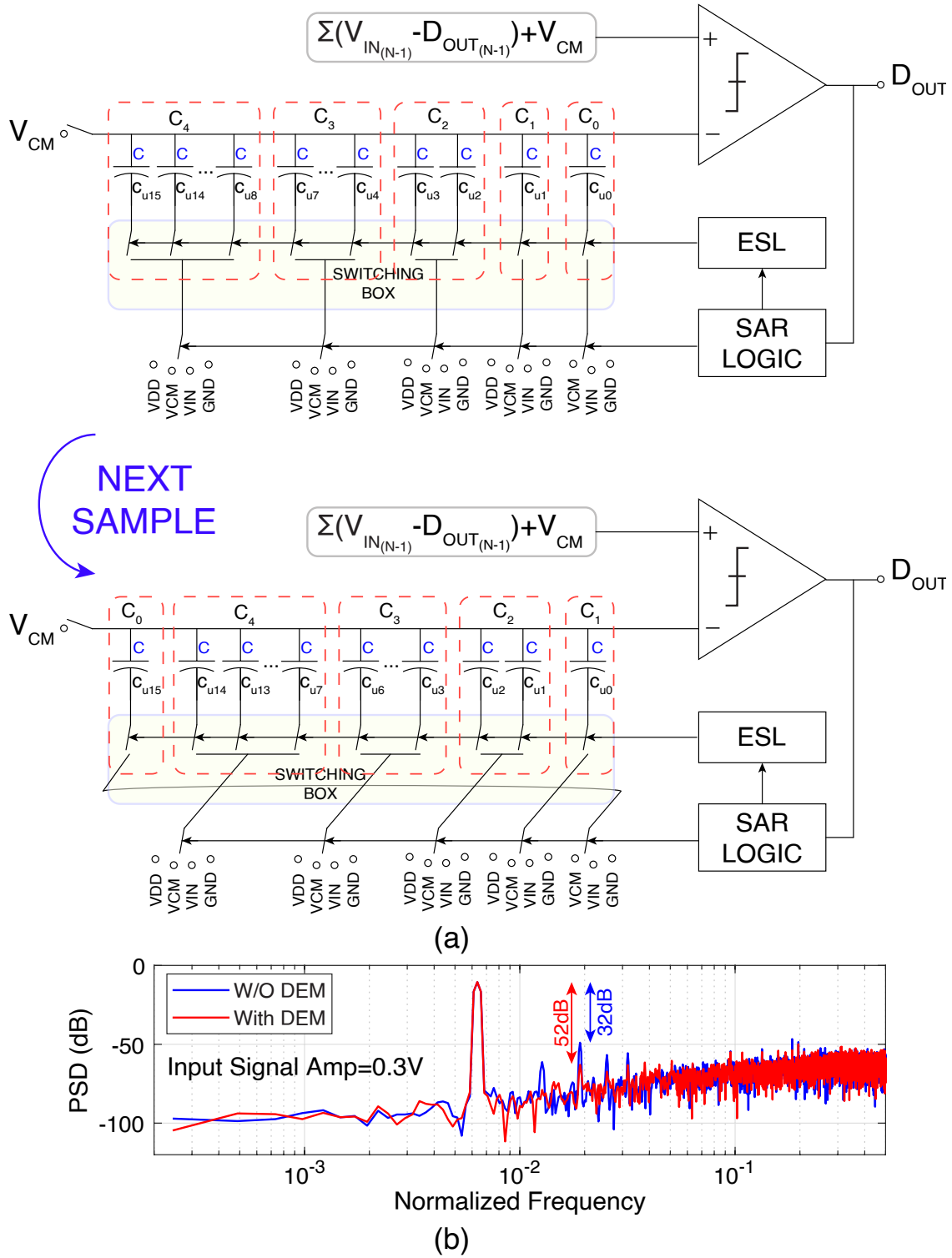


Figure 3.12: (a) The detailed implementation of the dynamic element matching in the noise-shaping SAR ADC highlighting the different arrangement of capacitors for two successive samples and (b) PSD comparison of a noise-shaping SAR ADC with a 1% capacitor mismatch with and without the DEM.

3.3.3.2 Mismatch Error Shaping

In multi-bit DAC noise-shaping ADCs, particularly in delta-sigma architectures, the precision and consistency of the DAC's elements are crucial for maintaining optimal signal-to-noise and distortion ratio (SNDR). Any minor discrepancies within the DAC's components can lead to substantial declines in the ADC's performance. Therefore, achieving precise matching of DAC elements is a critical aspect in the design and fabrication of these ADCs, as it directly influences the SNDR and the overall performance of the system [68].

To mitigate this issue, one approach is the application of digital background calibration. This method involves measuring the discrepancies and recording them in a lookup table (LUT) for correction during the calibration phase. However, the effectiveness of this technique hinges on the accuracy of the initial error measurement, making it somewhat vulnerable to inaccuracies.

An alternative strategy is dynamic element matching (DEM), which aims to average out the mismatch errors over time. Our noise shaping SAR ADC incorporates DEM to enhance its overall performance. As shown in Fig. 3.12(a), in each conversion cycle (i.e., each new sample), the element selection logic (ESL) associates a group of unit capacitors with a specific bit decision. Then, in the subsequent cycle, it rotates this selection to form a new configuration, effectively averaging out mismatch errors. This block is implemented using a Logarithmic Shifter. Fig. 3.12(b) provide the simulation result when the capacitors are subjected to a 1% mismatch, illustrating the efficacy of DEM scheme in enhancing system performance. The results compare the performance of the noise-shaping SAR ADC with and without the DEM

Artifact Removal Calibration Process

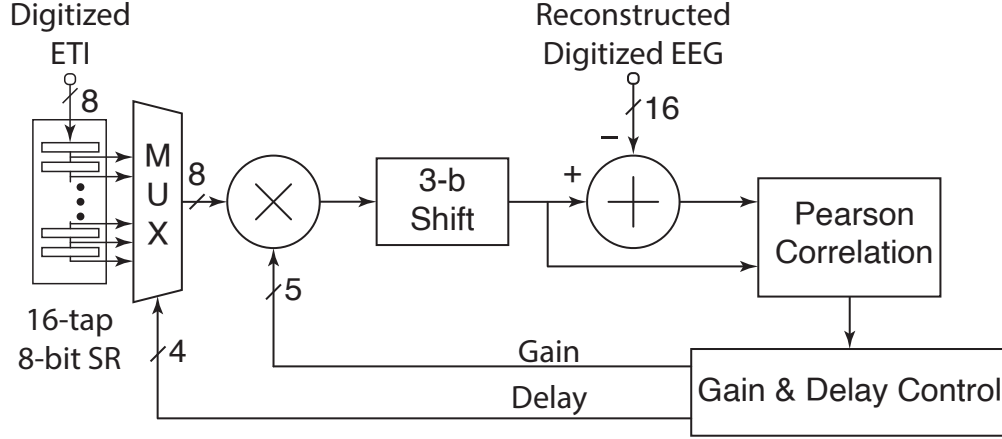


Figure 3.13: Digital implementation of the calibration process for setting the optimal gain and delay to map the extracted motion from ETI measurement to the effect of motion from the signal path.

activated which highlight the superior spurious free dynamic range (SFDR) in the system in the presence of DEM.

3.3.4 Motion Artifact Removal

In this section, we discuss the motion artifact removal stage of our system, a critical step designed to maintain the integrity of the output EEG signal. The methodology involves the subtraction of motion artifacts from the reconstructed EEG signal. This subtraction is performed on the output of the ETI measurement and the reconstructed EEG signal itself. The motion artifact signal, derived from the ETI measurement stage, must undergo specific modifications in gain and delay to accurately replicate the impact of the motion artifact on the signal path, enabling effective and meaningful subtraction. These necessary adjustments to the motion artifact signal are performed during the calibration phase of the system.

As illustrated in Fig. 3.13, the 8-bit ETI signal is initially stored in a 16-tap, 8-bit shift

register bank. The gain and delay control block then determines the appropriate delay for passing the ETI signal to the subsequent stage. This delayed ETI signal undergoes a two-step modification: First, it is multiplied by a 5-bit gain, determined by the control block; and Second, it is subjected to a three-bit shift to transform it into a 16-bit output. The resulting signal, an estimated representation of the motion artifact, is then subtracted from the reconstructed EEG signal.

The objective of this subtraction is to produce a signal with minimal correlation to the ETI signal, which is indicative of the motion artifact. The Pearson Correlation block performs the target task here, calculating the correlation between the result of the subtraction signal and the ETI. The control block actively modifies both the delay and gain settings in an effort to achieve a state where the resultant signal has the least possible correlation with the motion artifact. Furthermore, the control block ensures that the resultant signal does not exceed a 13-bit range, thus confirming that the motion-free EEG signal remains within the supply voltage range.

3.4 Measurement Results

In this section, we focus on the experimental measurement results of the proposed artifact-resilient DR-enhanced active electrode. This presented AE has been fabricated in a 180nm standard CMOS technology and the performance of different blocks and system-level features are validated experimentally. Fig. 3.14 presents the experimental measurement results of the integrated input referred noise (IIRN) and the adjustable gain-bandwidth of the system.

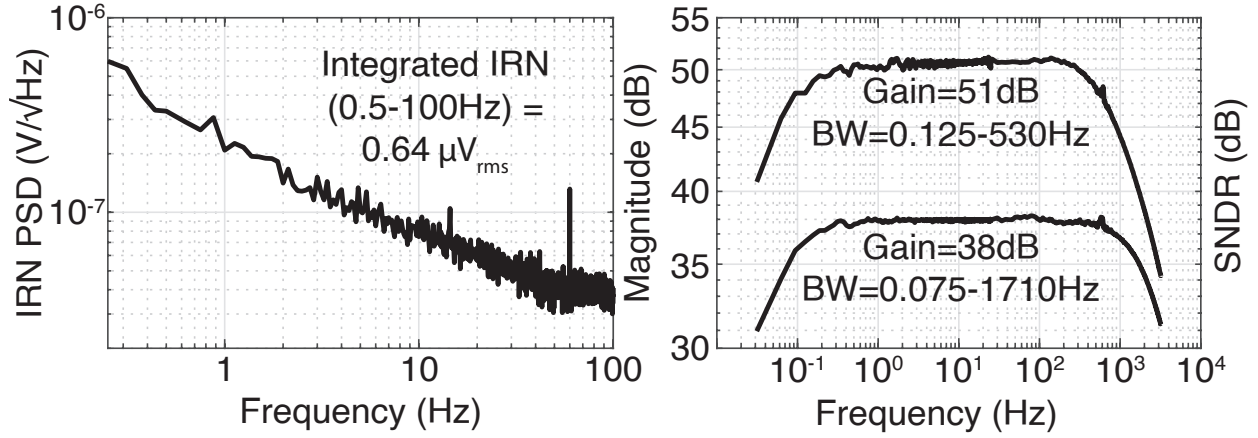


Figure 3.14: Experimental measurement result of the integrated input referred noise and adjustable gain bandwidth of the first amplification stage.

Power spectral density of the noise shows an IIRN of $0.64\mu\text{V}$ over a frequency range from 0.5 Hz to 100 Hz. The overall gain and bandwidth plot with the first stage being adjustable shows that a programmable gain of 51dB over bandwidth of 0.125Hz-530Hz or gain of 38dB over bandwidth of 0.075Hz-1710Hz can be achieved which is adjusted by the saturation detected of the first stage which sets the value of the feedback capacitor.

Fig. 3.15 shows the experimental measurement results of the output signal quality with interference rejection. The plot displays the output signal voltage over a period of 2 seconds, with the 60Hz notch filter being enabled or disabled. With the filter enabled, the output signal exhibits a significant decrease in noise, reflecting the effectiveness of the filter in rejecting the 60Hz interference commonly associated with power-line noise in electrical recordings.

The experimental measurement results of Fig. 3.16 illustrates the CMRR value, in the presence of a $1\text{M}\Omega$ mismatch in the electrode-tissue interface (ETI) of different active electrodes (AEs). The red curve represents the CMRR when CMR boosting calibration is applied, indicating an improvement in the rejection of common mode signals, especially noticeable

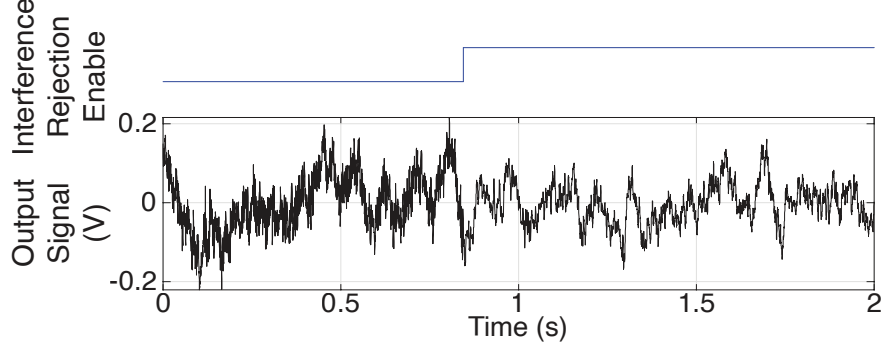


Figure 3.15: Experimental measurement result showing the quality of recording with the 60Hz notch filter disabled and enabled.

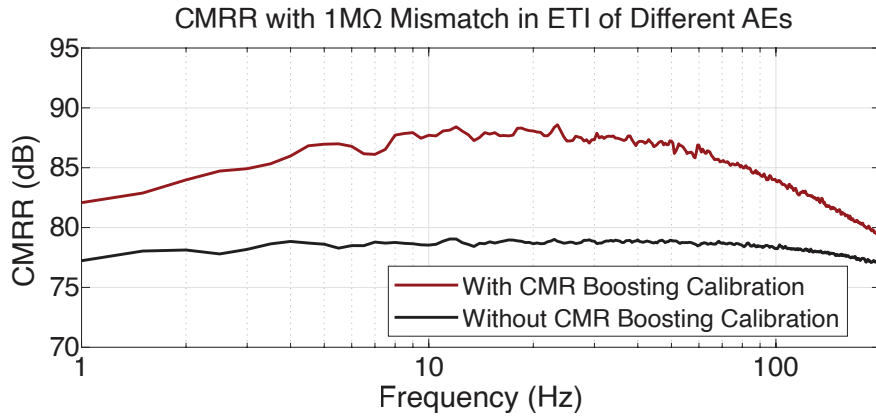


Figure 3.16: Experimental measurement result showing the effect of CMR boosting calibration in improving the CMRR in the presence of AE to AE interface impedance mismatch.

in 10-60Hz range which is the main range of interest due to the effect of power-line interference. The black curve depicts the CMRR without the calibration, serving as a baseline for comparison. The data demonstrate the efficacy of CMR boosting calibration in enhancing the CMRR in the presence of AE to AE interface impedance mismatches.

In the next experimental result, the performance of the DR boosting scheme and motion removal feature are validated using prerecorded EEG signals that is recorded through an electrode which undergoes a series of movements to mimic the effect of motion artifacts. Fig. 3.17(a) shows the effectiveness of dynamic range (DR) boosting in preventing saturation

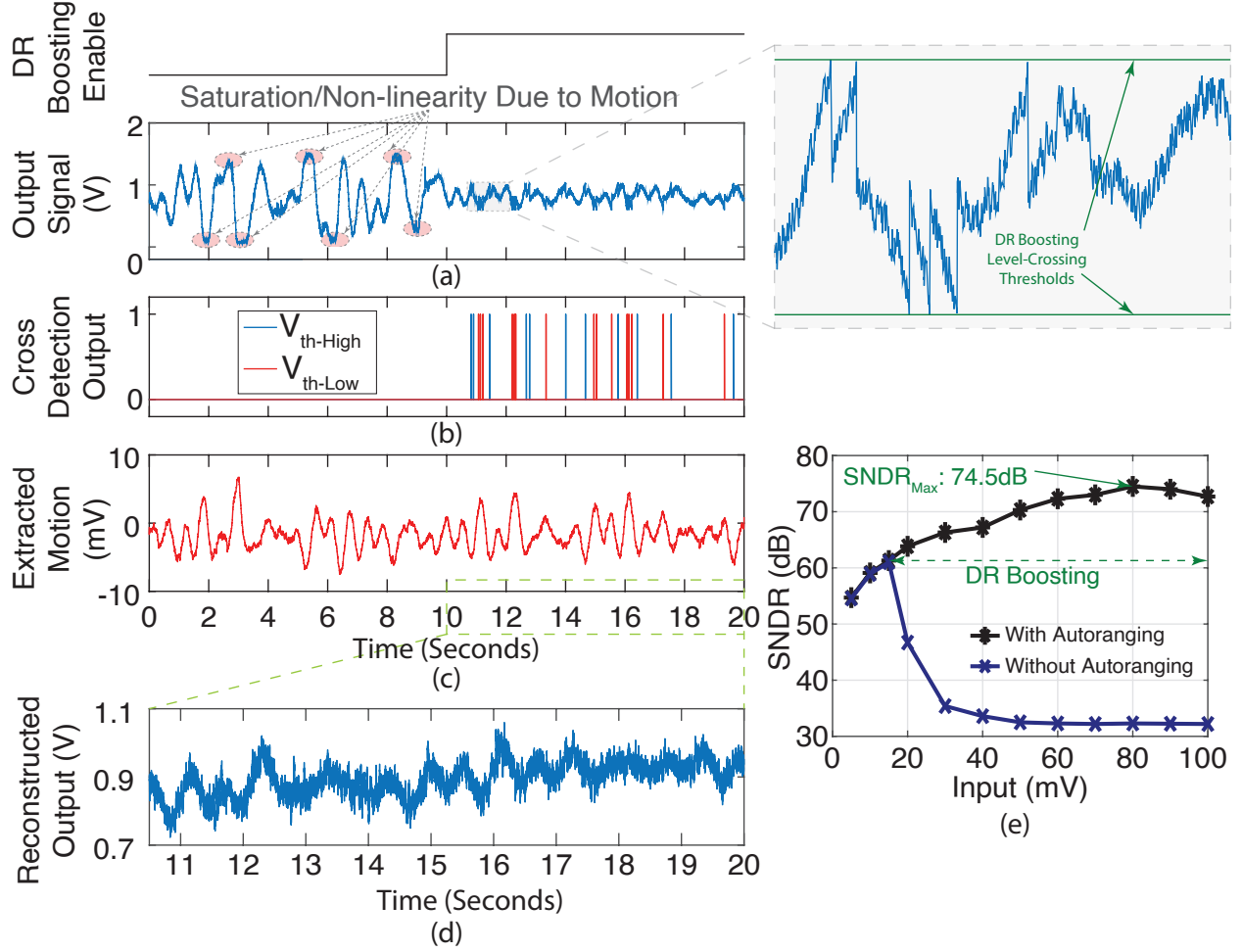


Figure 3.17: Experimental measurement result showing (a) the effectiveness of dynamic range boosting in avoiding saturation or nonlinear operation due to motion artifacts and its zoomed in view highlighting the level crossing threshold and the functionality of the feedback DAC, (b) the output of cross detection that activates the feedback DAC to keep the output voltage in the target range, (c) the extracted motion artifact, (d) the reconstructed signal after motion removal, and (e) experimental measurement result of SNDR with and without the proposed auto-ranging technique.

or nonlinear behavior that is commonly induced by motion artifacts. The zoomed-in view provides a detailed look at the level-crossing thresholds, along with showcasing the operational dynamics of the feedback DAC. Fig. 3.17(b) displays the output of the cross detection mechanism, which is used in activating the feedback DAC. This activation ensures that the output voltage is maintained within a desired operational range, thus avoiding the extremes that could lead to signal distortion. Fig. 3.17(c) presents the extracted motion artifact that has been measured from the from the ETI measurement path. Finally, Fig. 3.17(d) depicts the signal post-motion artifact removal, demonstrating the efficacy of the implemented DR-boosting and motion artifact removal technique.

Fig. 3.17(e) presents an experimental analysis of the Signal-to-Noise and Distortion Ratio (SNDR) as a function of varying input signal amplitudes. It compares the performance of a system with and without the DR-boosting feature enabled, indicating the superiority of recording SNDR in the presence of the proposed DR-boosting. The results shows that with auto-ranging a consistent SNDR performance is maintained across the input amplitude range, culminating in a maximum SNDR of 74.5 dB. This plateau indicates the effectiveness of auto-ranging in sustaining signal quality across a wide range of input signal amplitudes. In contrast, the situation without auto-ranging shows a significant decline in SNDR as the input amplitude increases, illustrating the limitations of the recording front-end at higher input levels where the risk of saturation and non-linearities becomes more pronounced.

Table 3.1 provides the comparison of the presented AE with the state-of-the-art. Our design, fabricated in 180 nm technology, marks a considerable performance in comparison

with the state-of-the-art across several metrics. Power consumption is optimized at 24.87 μW per channel, substantially lower than the power consumption seen in prior works. The CMRR is highly competitive at 89.2 dB, closely approaching the highest reported value, but more importantly, it retains a high CMRR in the presence of electrode-tissue mismatch which is the reality of EEG recording headsets. The input impedance at 50-60Hz achieve the value of $4.3\text{G}\Omega$, offering superior electrode interface quality. A distinguishing feature of our system is the in-amplifier electrode (In-AE) motion artifact removal, which is not reported in other designs and provides a clear advantage in signal clarity. Additionally, the inclusion of on-chip diagnostics represents a notable advancement in self-contained system checks. When compared to existing technologies, our design excels, delivering advancements in power efficiency, noise management, and diagnostic capabilities, making it a leading choice for EEG applications.

Table 3.1: Comparison with Wearable EEG Recording Systems

Specification	JSSC 2014 [69]	TBioCAS 2011 [47]	ISSCC 2019 [40]	TBioCAS 2021 [70]	This Work
Technology (nm)	180	180	65	180	180
Application	EEG	EXG	EEG	EXG	EEG
Channel/Chip	8	8	1	1	1
RecPower/Ch	19.8 μ W	104.4 μ W	340.6 μ W	73.8 μ W	24.87 μ W
CMRR (dB) @50-60Hz	82	102	82	109	89.2
CMRR (dB) (Zin mismatch)	NR	42 (0.8M Ω)	NR	NR	86.9 (1M Ω)
IIRN (μ V _{RMS}) (0.5-100Hz)	0.8	0.65	0.63	0.98	0.64
Bandwidth (Hz)	1kHz	200Hz	250Hz	100Hz	500Hz
Offset Tolerance (mV)	R-to-R	$\pm$ 350	NR	$\pm$ 300	$\pm$ 500
SNDR	NR	NR	84	66.2	80
Number of Wires	N	1Bus	4	NR	6
Input Imp @50-60Hz	>2G Ω	1G Ω	100M Ω	34M Ω	4.3G Ω
Response to Motion Artifact	ETI Recording	ETI Recording	Motion Tolerance	DC Offset Removal	In-AE Removal
On-chip Diagnostic	No	No	No	No	Yes

Chapter 4

Distributed Pulse-Based Feature

Extraction and Multiplier-less

Neuromorphic Boosted Seizure

Classifier

The manifestation of seizure events on EEG signals varies across the patients and more than 10 different types of seizure have been categorized in [71]. As it is shown in Fig. 4.1, when seizure occurred on one of the patients (from CHB-MIT dataset [72]) the amplitude of EEG signals increased while the reduction of amplitude can be observed in EEG data recorded from another patient during the seizure event. It should be noted that even for the same patient, seizure events might appear very different over time, and also from channel to channel

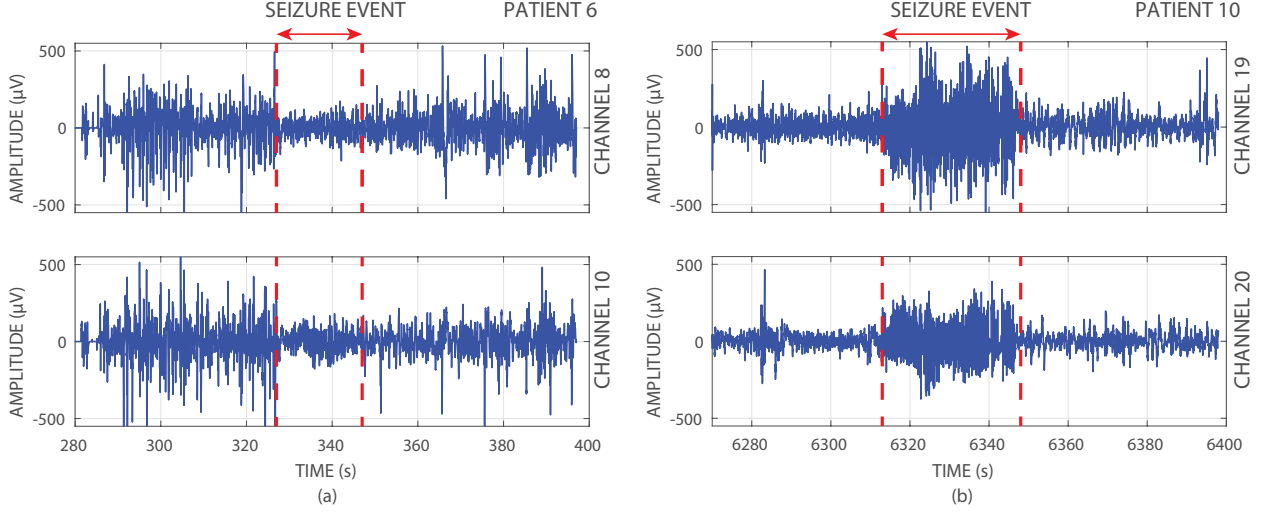


Figure 4.1: Manifestation of seizure event in two different patients with amplitude increase in (a) and amplitude decrease in (b).

(i.e., different levels of EEG signal activity variation before and during seizure in different channels).

Besides the cross-patient, cross-channels, and temporal differences of seizure events, an important challenge in developing seizure detection algorithms is that the scalp EEG signals have very small magnitude (i.e., in the range of $10\text{-}100\mu\text{V}$), which makes the signal prone to any physical or non-physical artifacts such as eye-blinking, head movement, chewing, etc. In addition to affecting the EEG's quality, these artifacts, at least in time domain, have substantial similarity to seizure events, which could lead to detection specificity degradation (i.e., increase in false positive rate). Fig. 4.2 shows a recorded EEG signal during chewing, which illustrates the similarity between a seizure event and an artifact.

The aforementioned challenges has lead to the popularity of the machine learning algorithms for seizure detection application, which offer higher precision than deterministic algorithms, thanks to their data-driven patient-specific nature. Fig. 4.3 shows a conceptual

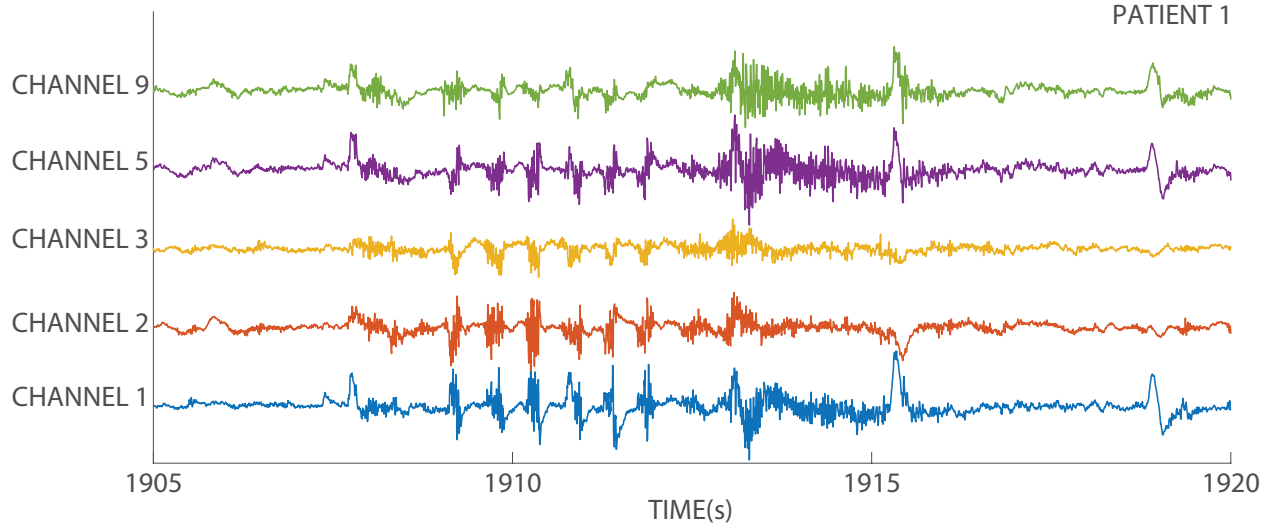


Figure 4.2: EEG recording from 5 different channels during chewing task with similar manifestation as seizure event.

illustration of different stages in a machine learning algorithm in a seizure detection application. The first stage is the signal acquisition block. In an EEG-based seizure detection task, the recorded data includes seizure and non-seizure events and the target is to differentiate them. Similar machine learning algorithms are also used in other types of biomedical application with time series input data, such as ECG-based cardiac arrhythmia detection and EEG-based emotion detection.

Following signal amplification and digitization, the discriminating bio-markers are extracted as the target feature from the raw biomedical data. Different types of features are useful in different application. A few widely-used examples of bio-markers in biomedical applications are spectral energy and phase-locking value in EEG-based application, R-to-R parameter in ECG-based applications and wavelet-based parameters in MRI-based applications. In the classification stage, the data points are categorized in different classes based on the extracted features. The types of classifiers used in these application vary from a simple

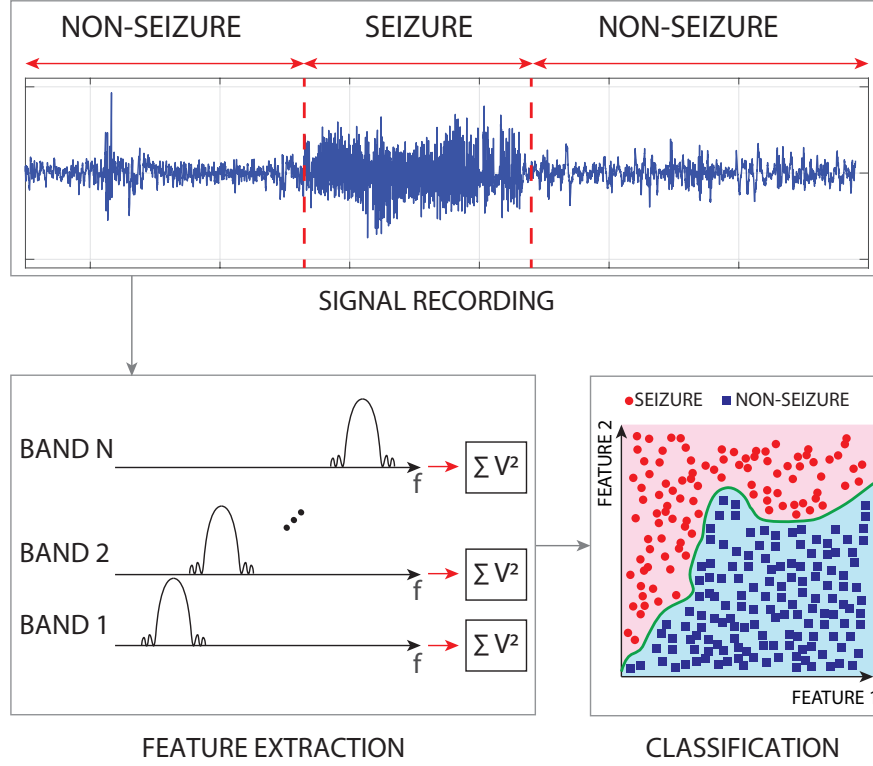


Figure 4.3: Conceptual illustration of different stages in a machine learning algorithm in a seizure detection application.

regression to complex deep neural networks.

4.1 Feature Extraction

The first step of the seizure detection is feature extraction. The most reliable and widely used bio-marker in seizure detection is the power spectral density of the recorded EEG signal in different frequency bands [73–76]. Fig 4.4(a) shows an example of peaks appeared in power spectral density at specific frequencies during a seizure episode while these peaks do not appear in Fig. 4.4(b), which is the FFT of a seizure-free period. This variation in the power spectral density at different bands suggests the possibility of monitoring these features as an

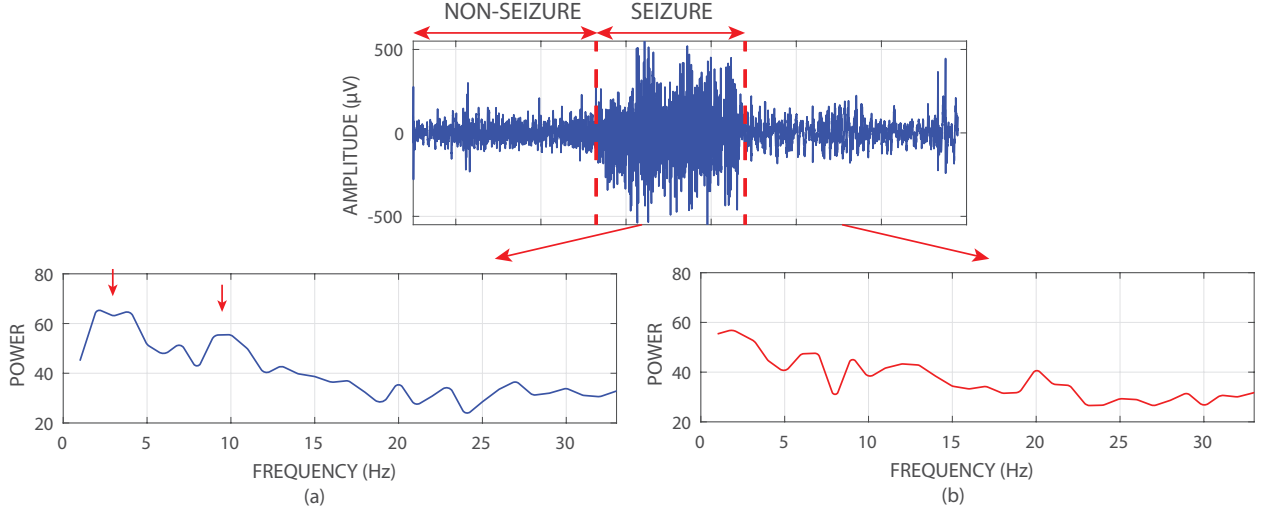


Figure 4.4: (a) Power spectral density of the EEG signal during a seizure event with peaks appeared at specific frequencies and (b) Power spectral density of the EEG signal with no seizure event.

indicator of seizure events.

In order to extract the spectral band energy, the first step is to filter the EEG recording raw data with different band-pass filters and then calculate the power of each band. As a result, the required blocks for feature extraction are the band-pass filter and power calculation block. Fig. 4.5(a) shows the result of filtering the EEG recording, which includes a seizure event at different frequency bands (i.e., delta, theta, alpha and beta) and the calculated power at each band, which shows an increased power during the seizure event in three of the bands but no distinguishable variation in the delta band.

To implement the band-pass filters, finite impulse response (FIR) filters are more desirable in comparison with the infinite impulse response (IIR) filters due to their adjustability without stability concern and constant phase-delay at different frequencies. However, the implementation of FIR filters is challenging in terms of power consumption and area limitations (we need a few of them for each recording channel), especially considering the

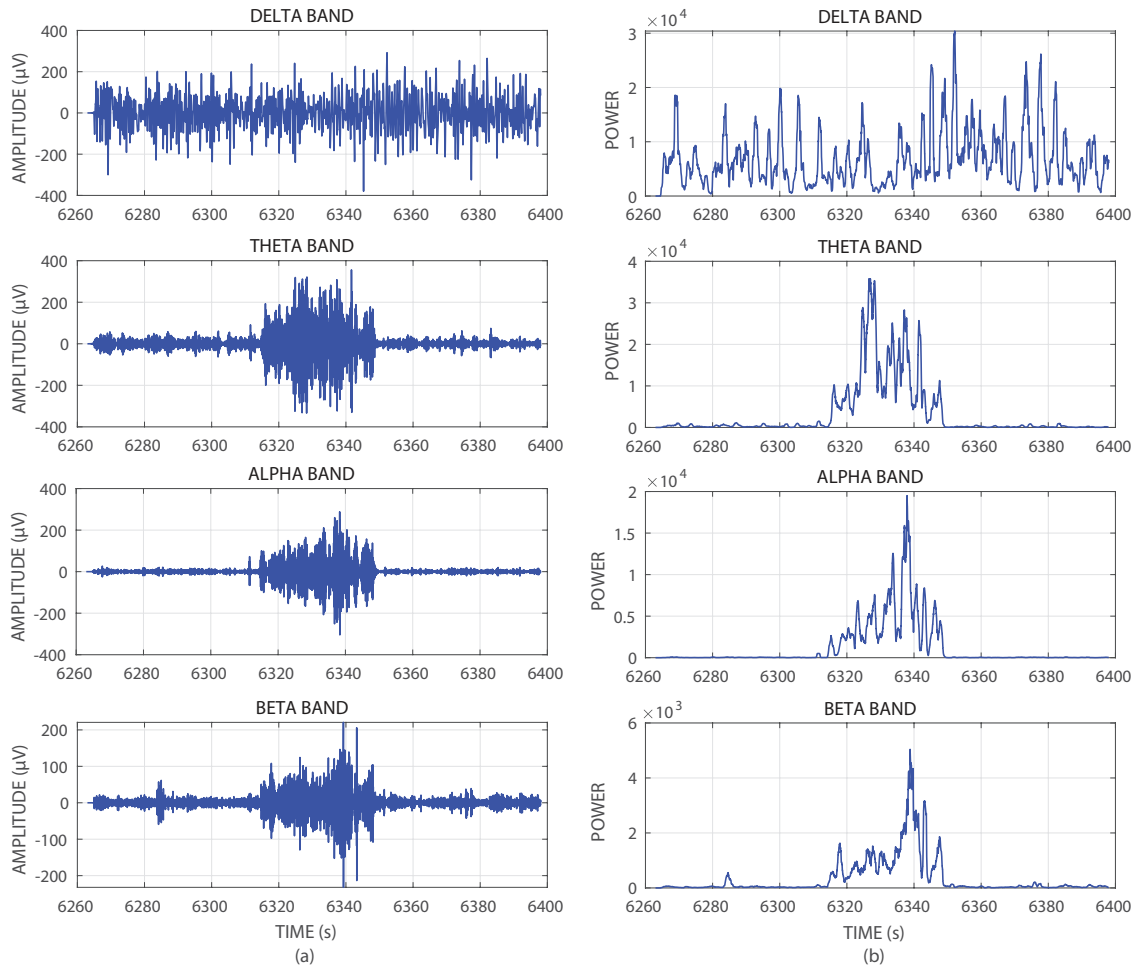


Figure 4.5: (a) Filtered EEG recording at different frequency bands (i.e., delta, theta, alpha and beta) and (b) the calculated power at each band with increased power during the seizure event in three of the bands but no distinguishable variation in the alpha band.

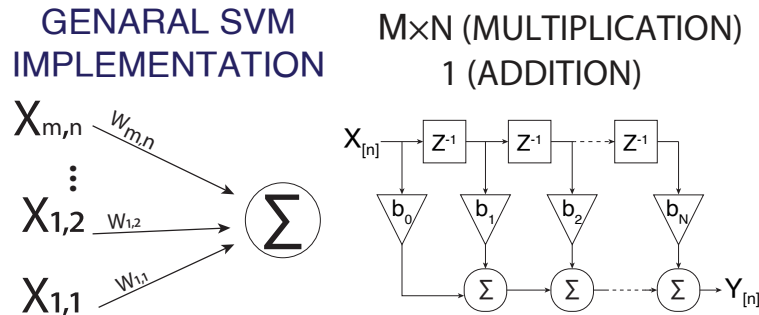


Figure 4.6: Block diagram of a general Nth order FIR filter including N delay taps and N+1 multiplication and N adder blocks.

highly-constrained power/area requirements of wearable devices. A general Nth-order FIR filter includes N delay taps, N+1 multiplier, and N adders (commonly 10-14bits [77, 78]). Therefore, the number of required operations to calculate the result of an Nth order FIR filtered that is applied on a data window with N_S sample is calculated as:

$$\begin{aligned} N_{Multiplication} &= N_S \times (N + 1) \\ N_{Addition} &= N_S \times N. \end{aligned} \tag{4.1}$$

The power consumption for this number of operations can add up to more than $56\mu\text{W}$ for an eight channel ASIC, which is almost in the same order of the whole analog front-end [77].

It should be noted that the computational complexity of a multiplier with N bit input is N times greater than an adder with the same input size. Therefore to decrease the power consumption of the FIR filter and to reach a reasonable power consumption negligible to power consumption of the analog front-end, the goal is to decrease the number of multiplications in the feature extraction algorithm.

As shown in Fig. 4.7, each implemented FIR filter extracts the content of a specific band in the continuous frequency domain. Our proposed approach is to sample the signal in frequency domain at each certain frequency band and calculate the signal power at these representative sampled frequencies instead of the entire band and use that as the indicator of the seizure appearance. The corresponding signal content at each sampled frequency is

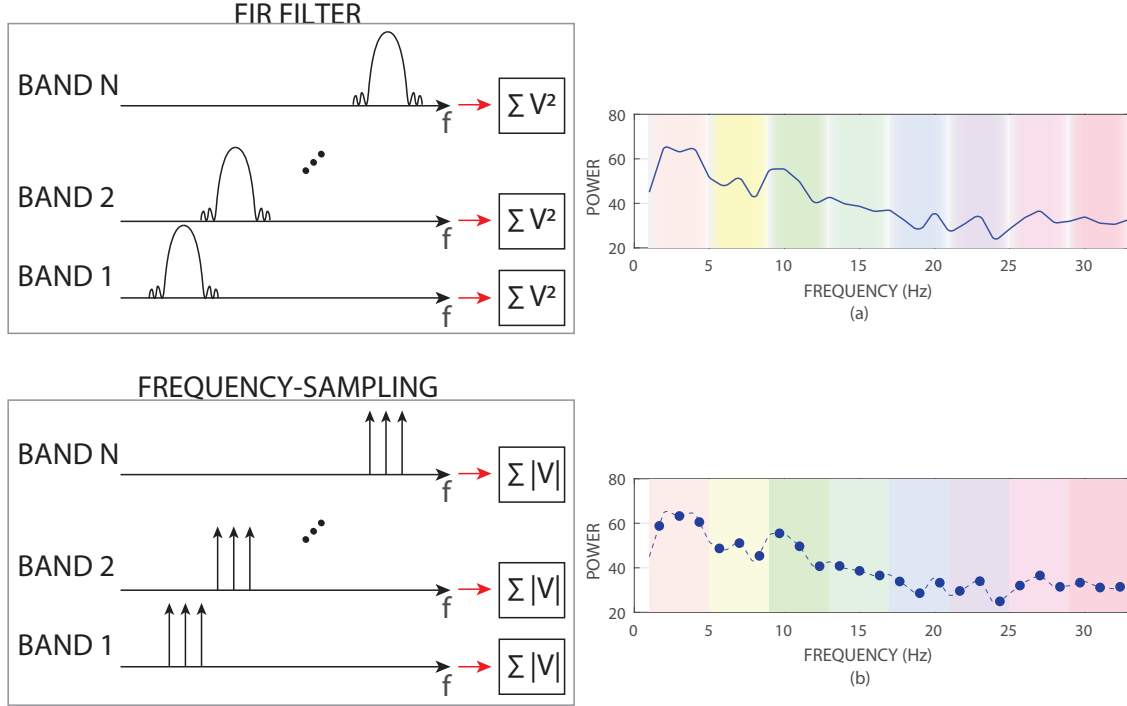


Figure 4.7: Conceptual block diagram of energy-band feature extraction at different frequency bands in (a) conventional scheme using FIR filter followed by a square function and (b) the proposed scheme of sampling at specific frequencies followed by absolute value function.

calculated based on fourier series coefficient equation as

$$f(x) = \sum_{n=1}^{+\infty} \left[a_n \cos \frac{n\pi x}{L} + b_n \sin \frac{n\pi x}{L} \right]$$

$$a_n = \frac{2}{L} \int_0^L f(x) \cos \frac{n\pi x}{L} dx$$

$$b_n = \frac{2}{L} \int_0^L f(x) \sin \frac{n\pi x}{L} dx$$
(4.2)

The signal power at each sampled frequency is calculated as $a_n^2 + b_n^2$. In our proposed algorithm, to avoid the implementation complexity of square function, the power is estimated by the absolute value. Fig. 4.8(a) shows the EEG signal for one of the CHB-MIT database patients, which includes a seizure event from 6313s to 6348s. Fig. 4.8(b) shows the filtered data in frequency band from 6Hz to 9Hz using an FIR filter with order of 1000. Fig. 4.8(c)

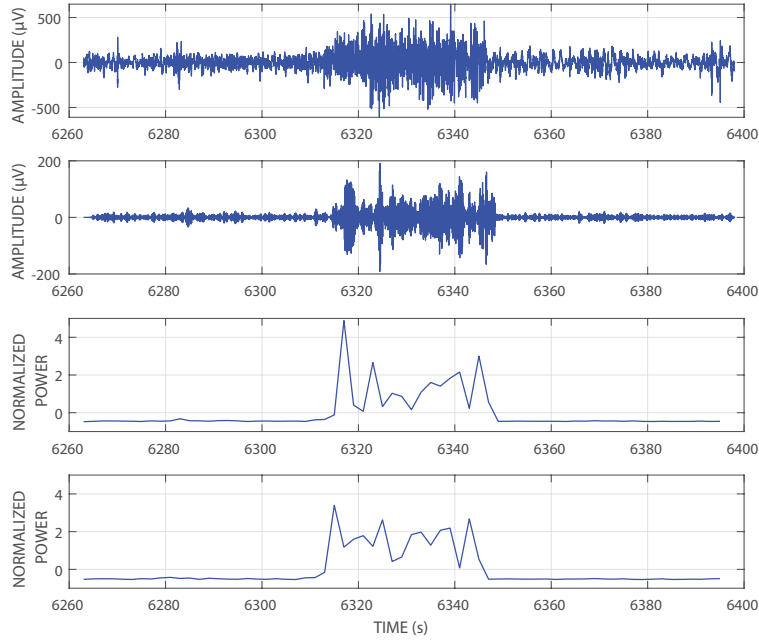


Figure 4.8: (a) EEG signal for patient 10 with a seizure event from 6313s to 6348s, and (b) the filtered data in frequency band from 6Hz to 9Hz using an FIR filter with order of 1000, and (c) the power of the filtered data averaged over time windows with 1s duration and (d) the addition power content of the EEG signal in sampled frequencies of 6Hz to 9Hz with step of 1Hz using the absolute value operator with similar variation in the energy-band content during the seizure event.

shows the power of this filtered data averaged over time windows with 1s duration. Fig. 4.8(d) shows the addition power content of the EEG signal in sampled frequencies of 6Hz to 9Hz with step of 1Hz using the absolute value operator which confirms similar variation in the energy-band content during the seizure event, in the proposed algorithm in comparison with the ideal approach.

The implementation of this algorithm requires the multiplication of the EEG signal by the sine and cosine waveforms with different frequencies (i.e., target sampling frequencies), which requires generation of these waveforms on chip as well as conducting several 12-bit multiplications. To further reduce the required computational resources for our target feature, we substituted the sine and cosine waveforms with a square pulse waveform at the same frequency (Fig. 4.9). In this approach the corresponding signal content at each sampled

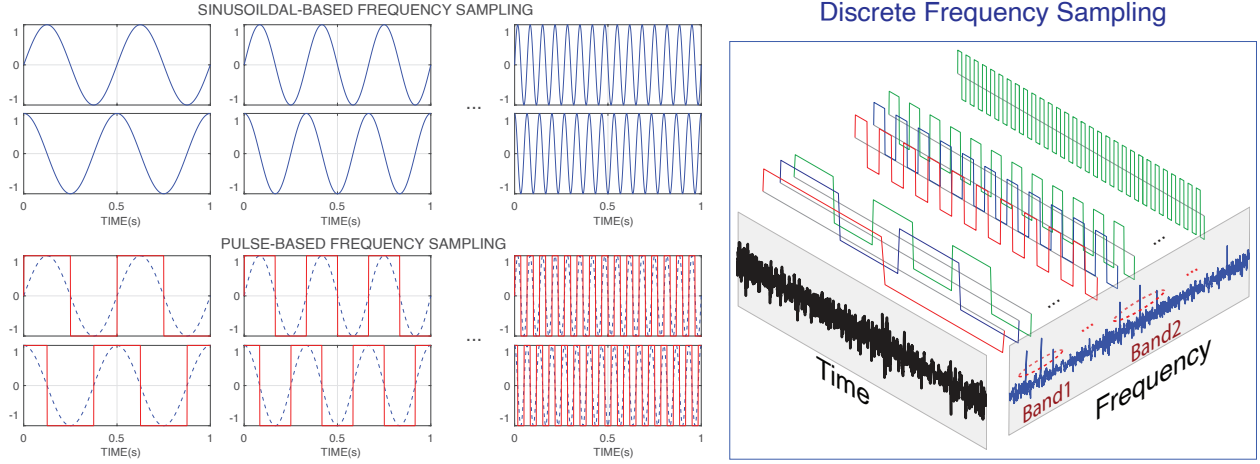


Figure 4.9: Sine and cosine waveforms used in sinusoidal-based frequency sampling at different frequencies and the substituted pulses waveforms used in the proposed pulse-based frequency sampling at different frequencies.

frequency is calculated as

$$\begin{aligned} a_n &= \frac{2}{L} \int_0^L f(x) \text{sign}\left(\cos \frac{n\pi x}{L}\right) dx \\ b_n &= \frac{2}{L} \int_0^L f(x) \text{sign}\left(\sin \frac{n\pi x}{L}\right) dx \end{aligned} \quad (4.3)$$

Fig. 4.10 compares the normalized energy-band feature from the sine-cosine approach and the pulse-based approach, which validates the similarity of the variation in comparison with the normal condition during the seizure event. This figure is a primary validation of the proposed feature in our seizure detection algorithm and further validation is achieved after applying the whole feature extraction algorithm on the target CHB-MIT data base and comparing the results with the state of the art.

The required computational resource for this feature depends on the number of samples in each time window and the target frequency resolution. For example, having three frequencies per band and 256 sample per second will results in 768 operation (addition and subtraction)

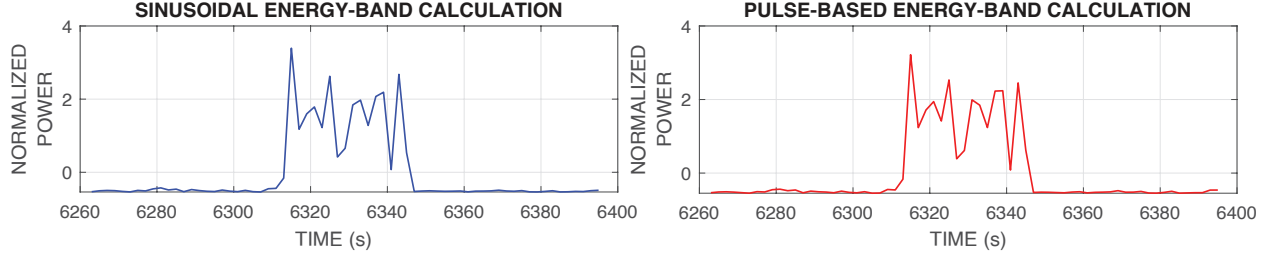


Figure 4.10: Similar increased level of normalized power with power calculation with sinusoidal energy-band calculation versus the proposed pulse-based energy-band calculation.

to calculate the power of each band. As a comparison with the state of the art, the commonly-used filter's order for feature extraction is more than 40 [77, 78], which results in 11520 addition and 11776 multiplication for a time window of 1s with 256 samples per second for each frequency band. Considering that for an N-bit data (e.g., 12 bit in our algorithm) the computational complexity of multiplication is N times higher than addition operation, the overall computational complexity of feature extraction is reduced by a factor of 184 which results in proportional power consumption reduction.

4.2 Classification

The feature extraction output is fed to a classifier, which distinguishes between seizure and non-seizure brain states. The first step to choose the suitable classifier is to define whether the specific classification problem is linear or non-linear. As shown in Fig. 4.11, classifiers that employs linear kernels, are unable to distinguish data points in non-linear distributions (i.e., a multi dimensional hyperplane in the feature space) while this is possible using a non-linear classifier.

The specific problem of seizure detection has shown to be a non-linear problem. An example of the data points distribution for seizure and non-seizure events of a patient is

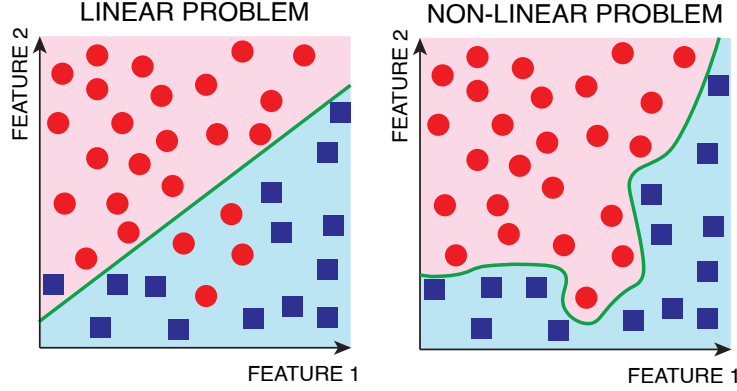


Figure 4.11: Classification tasks with linear and nonlinear distribution of the data points.

shown in Fig. 4.12, where a linear classifier can not be used to distinguish the two states.

Among different ML-based non-linear classifiers, deep-learning algorithms have received a lot of attention due to their overall better performance in different classifications tasks [79]. However, it should be noted that their precision comes at the cost of high computational complexity, thus power consumption. In the specific case of seizure detection application, the comparison of deep learning algorithms and non-linear support vector machine (SVM) algorithms shows that the SVM algorithm can achieve a comparable performance with 384 times reduction in the number of required nonlinear operations and 3557 times reduction in the number of multiplication and accumulator (MAC) operators. It should also be noted that the SVM algorithm is compatible with an unbalanced dataset for training with lower percentage of event data points that is the common condition of seizure detection datasets.

Considering the above advantages, we chose SVM classifier for our seizure detection task. The SVM classifier is a type of supervised machine-learning algorithm compatible with binary classification tasks, with both linear and non-linear kernels. While the non-linear SVMs can achieve a better classification accuracy compared to linear counterparts (in a non-linear

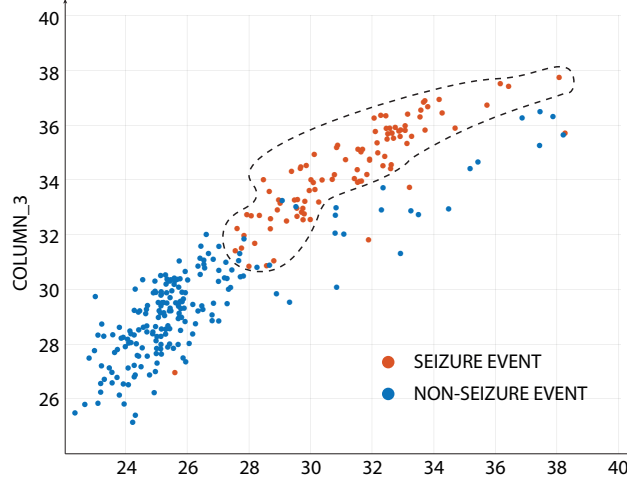


Figure 4.12: Non-linear distribution of seizure and non-seizure events in a seizure detection application.

classification task), they are also significantly more expensive in terms of computational cost. For example as shown in [34], by comparing the energy per classification of linear and non-linear SVM classifiers for an ECG-based cardiac arrhythmia detection, we observe that while the linear classifier consumes only $0.71\mu\text{J}/\text{classification}$, the non-linear polynomial classifier consumes $16160\mu\text{J}/\text{classification}$ and the non-linear radial basis function (RBF) classifier consumes $38090\mu\text{J}/\text{classification}$. It should be noted that in this comparison the linear SVM algorithm can not achieve a comparable accuracy as the classification task is a non-linear problem.

In order to investigate the reason of this large difference in the power consumption of linear and non-linear SVM, we should consider the inference procedure of the SVM algorithm for each given test feature vector ($\vec{x}$), which regardless of the classifier being linear or non-linear performs as,

$$f(X) = \sum \alpha_i K(s\vec{v}_i, \vec{x}) - \beta. \quad (4.4)$$

where $s\vec{v}_i$ is the support vector, $\vec{x}$ is the test vector, α_i is the coefficient, K is the kernel function, and β is the offset value. The support vectors are the vectors in the feature space that define the decision boundaries for the different classes which are defined during the training step. The difference between linear and non-linear SVM comes from the type of kernel ($K(.)$) that is applied to all pairs of each test feature vector ($\vec{x}$) and a support vector (i.e., $(s\vec{v}_i, \vec{x})$ for $i=1:N$). In a linear SVM this kernel is an inner dot product of the support vector and each data point in the feature space. Considering that the inner dot product is a linear operator, superposition can be applied to the summation of this kernel, which means the implementation complexity can reduce from addition of hundreds of inner dot products to a single addition of weighted combination of the input test vector. However, for a non-linear operator like RBF, the super position rule is not applicable and the calculation should be performed for each support vector which results in much higher computational complexity and power consumption.

The simplicity of the implementation of the linear SVM makes it a desirable choice for low power biomedical application. However, the reduced computational complexity in linear SVM comes at the cost of less accuracy for the classification task. For example, as shown in [34], the linear classifier results in almost 18% less sensitivity and 5% increase of the false alarm rate in comparison with its non-linear counterpart in an ECG-based cardiac arrhythmia detection task.

Our proposed structure, in order to benefit from the implementation simplicity of linear SVM while achieving a comparable accuracy with non-linear SVM algorithms, is to apply

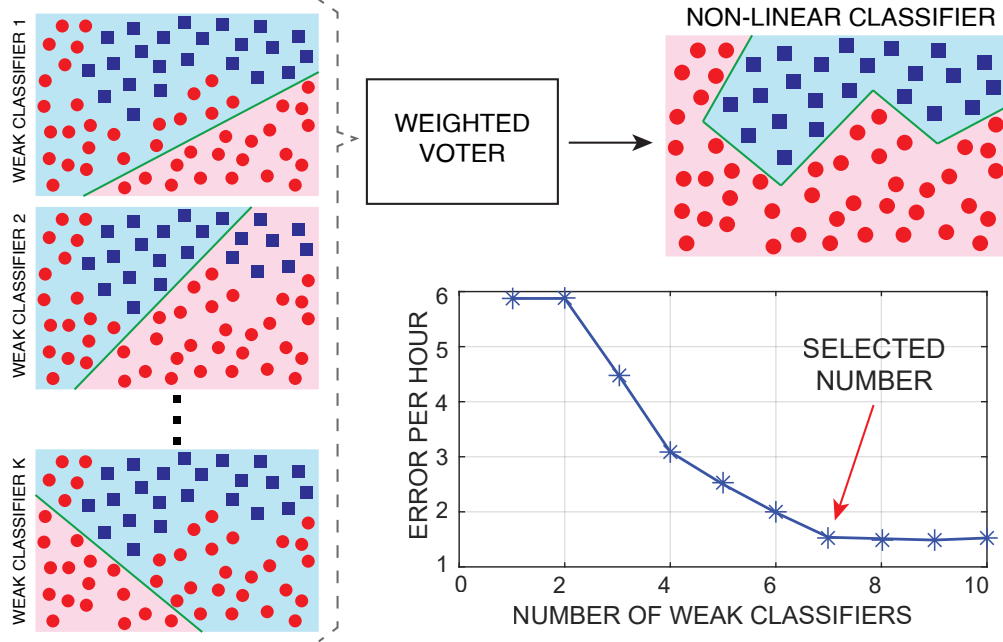


Figure 4.13: Combination of weak linear classifiers acts as a non-linear classifier.

the adaptive boosting technique on the adopted linear SVM algorithm. This technique was proposed by Yoav Freund and Robert Schapire in 1995 as a general concept of combining a set of weak classifiers to operate as a strong classifier [80, 81]. For example, as shown in Fig. 4.13, for a classification task with non-linear distribution of the data points, a non-linear classifier is achieved through combination of several linear classifiers which have individually failed to perform the classification task. Additionally, the simulation results, plotting error per hour against the number of weak classifiers, reveal a plateauing trend in precision after a certain point. Consequently, these observations guide our decision to utilize seven weak classifiers in our model, achieving balance between complexity and performance.

Fig. 4.14 shows the general concept of adaptive boosting which defines each classifier by increasing the weight of the misclassified test vectors using the previous classifiers. This procedure will stop when adding an extra weak classifier would not improve the precision of

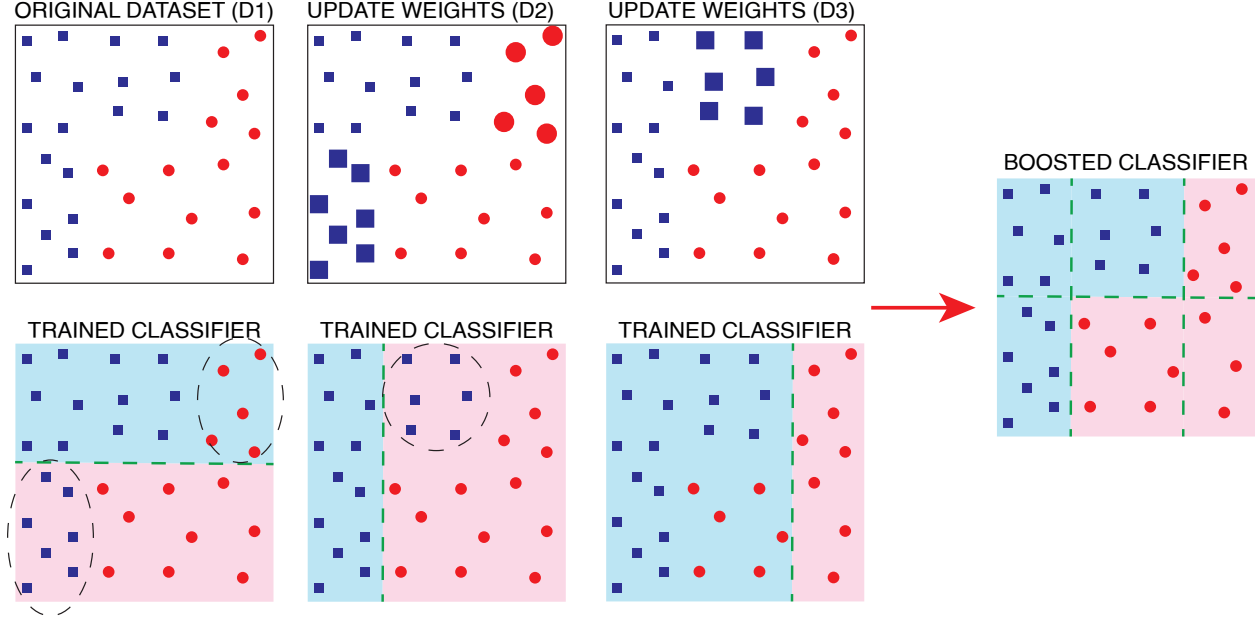


Figure 4.14: Conceptual step by step process of classifier training using adaptive boosting technique by assigning more weights to the mis-classified events in the previous steps.

the whole classifier. The defined weak classifiers are combined with a coefficient to structure the overall strong classifier.

4.2.1 Implementation of the Weak Classifiers

As a result of using adaptive boosting technique and combination of weak classifiers to form a strong non-linear classifier, the classifier structure used in this work is built as a combination of K different linear SVMs. As shown in Fig. 4.15, each feature vector contains $M \times N$ elements associated with the spectral energy of N different frequency bands from M different channels. The mapping function of a linear SVM as a weak classifier to determine

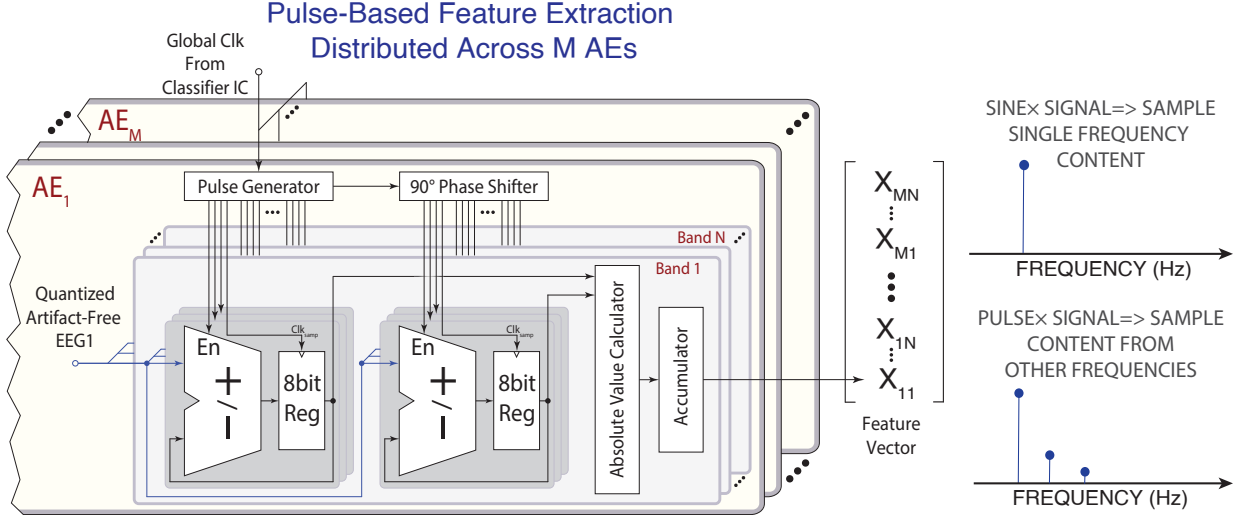


Figure 4.15: feature vector includes the spectral energy of N different frequency bands from M different channels.

the position of each test feature vector is defined as:

$$\begin{aligned}
 f(X) &= \text{Seizure} \text{ if } W^T \cdot X + \beta > 0 \\
 f(X) &= \text{Non-seizure} \text{ if } W^T \cdot X + \beta \leq 0 \\
 W^T &= [W_{1,1}, W_{1,2}, \dots, W_{m,N}] \\
 f(X) &= W_{1,1}X_{1,1} + W_{1,2}X_{1,2} + \dots + W_{M,N}X_{M,N} + \beta
 \end{aligned} \tag{4.5}$$

Therefore, classification of each test feature vector requires $M \times N \times K$ multiplications. This number of operations is still challenging for a resource-limited design. In order to achieve a power-efficient and resource-optimized classifier, we propose a temporally-coded multiplication and accumulation (MAC) to implement the target SVM classifier. The idea behind the proposed temporally-coded MAC implementation is the spike-timing-dependent plasticity of neurons communication which associates the strength of the connection between the neurons

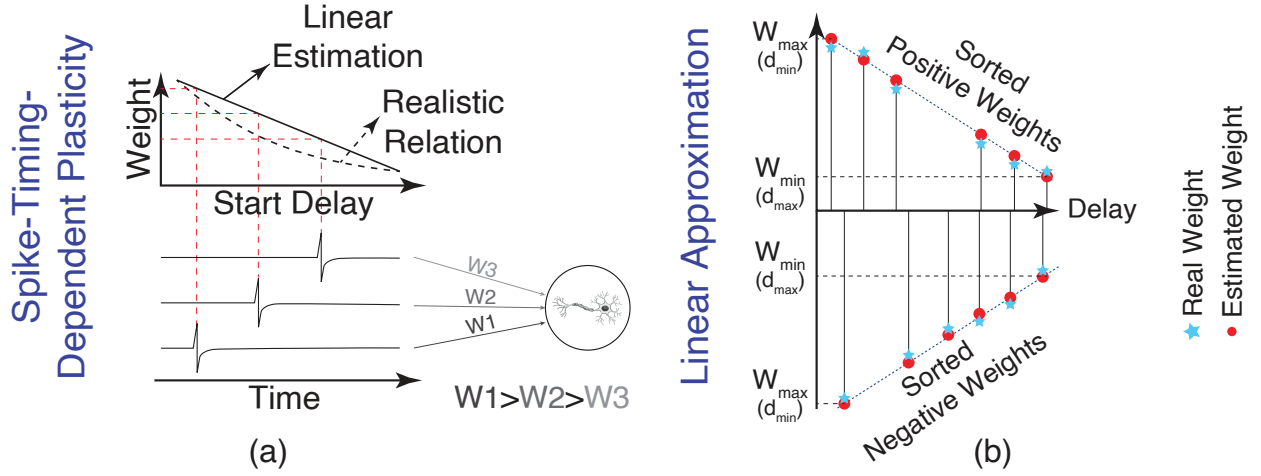


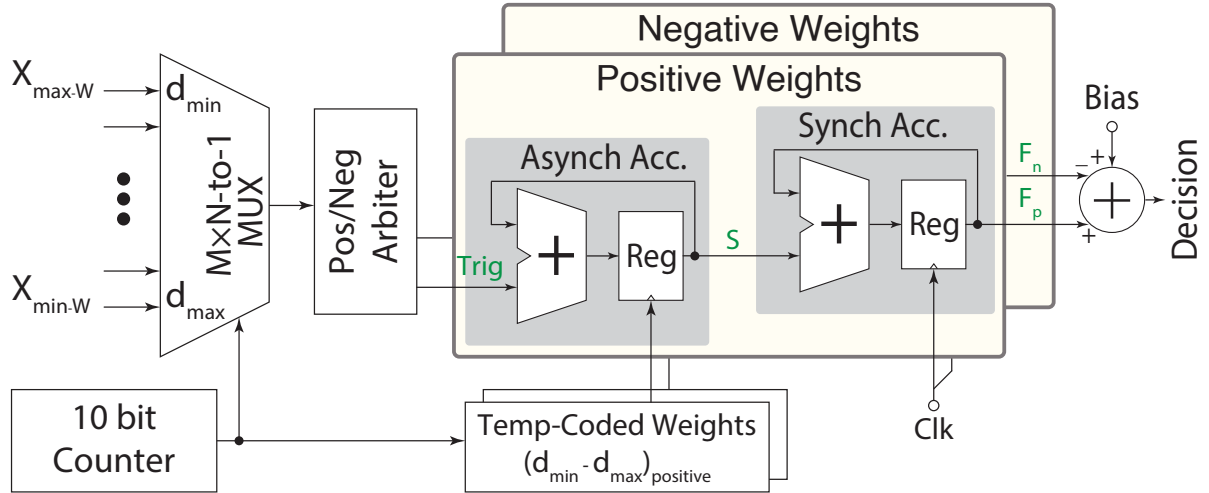
Figure 4.16: (a) The biological basis of our model - the temporally-sensitive response of neurons, simplified to a linear model. (b) A schematic representation of the proposed SVM structure that sorts weights and corresponding features from largest to smallest.

to the time that the spikes from one reaches the other and the spikes that reach the other neuron sooner will have a higher weight. Fig. 4.15 also shows a simplified implementation of the feature extraction block which is explained in details next.

Fig. 4.17 illustrates our approach to an innovative implementation of a neuron-inspired concept, which also showcases our unique solution to the computational demands of a general mapping function. Fig. 4.16(a) demonstrates our adaptation of a fundamental neurobiological principle - the temporal dynamics of neuronal responses to synaptic inputs. In biological neurons, the timing of incoming signals or 'spikes' matters, with neurons being more responsive to the signals arriving sooner and their responsivity diminishing over time. We have incorporated this principle into our model, though we have elected to represent it with a linear relation as opposed to a more complex, yet realistic, nonlinear one for the sake of computational simplicity.

As shown in Fig. 4.16(b), in a general mapping function, the weights are distributed randomly and the implementation requires $N \times M$ multiplication and one addition. Our proposed

Multiplier-Less Weak Classifier



Sample Simulation Results

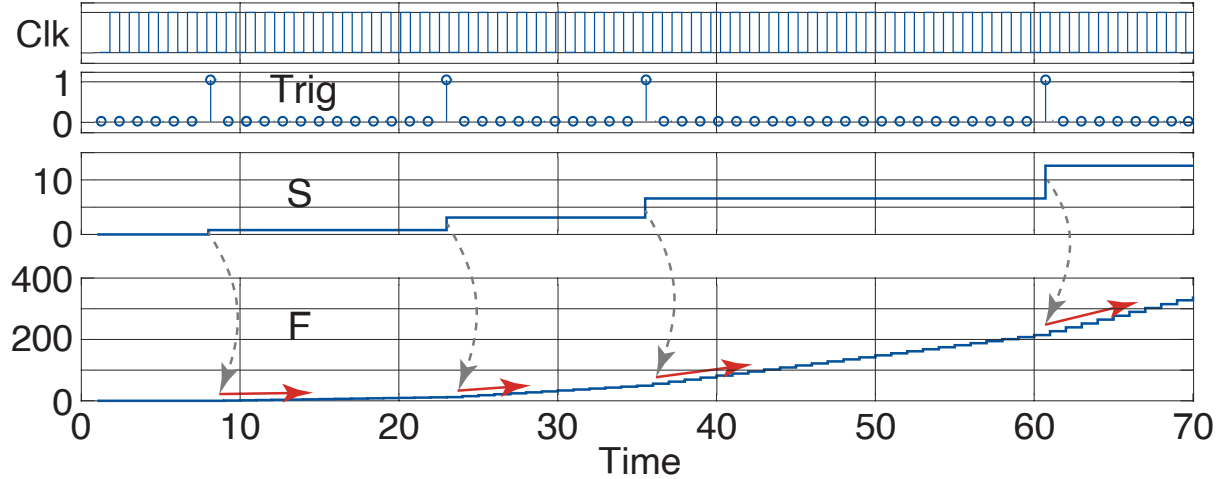


Figure 4.17: Implementation of the dual accumulator architecture with event-based and synchronous operations and an illustrative example of the dual accumulator operation.

structure for a temporally-coded implementation of the SVM is to sort the weights by the size from the largest to the smallest and the elements of the feature vector ($X_{i,j}$) would be sorted based on the places of the associated element of the weight vector ($W_{i,j}$). Therefore, to implement the higher weights, their associated element of the feature vector enters the mapping function sooner.

As shown in Fig. 4.17, in this structure, multiplication process is implemented by consecutive addition operators, while combining all the required multiplications for different elements of the feature vector ($X_{i,j}$) in a single accumulator through updating the accumulator's input. The result of each mapping function is valid after 1024 consecutive clocks and therefore it is possible to implement SVM weight with up to 10bit resolution. The input of the synchronous accumulator is the output of a second asynchronous accumulator, which only updates when a new feature enters according to its weight-associated timing, otherwise it holds the previous value. Therefore, the feature element at the time of t_i is accumulated $1024-t_i$ times, thus multiplied by a factor of $1024-t_i$. Fig. 4.17 also provides an illustrative example of this dual accumulator operation. This example shows that at any given time point t_i , the feature element is accumulated $1024-t_i$ times, effectively equivalent to multiplying the feature element by a factor of $1024-t_i$.

In this implementation, the accuracy of the classification is directly influenced by the precision of the weights. As illustrated in Fig. 4.18, we demonstrate the estimated weights with 5-bit and 10-bit precision. The weight precision in a k -bit setting gives us 2^k-1 discrete levels for weight estimation. As such, with a 5-bit precision, we have 31 distinct levels and

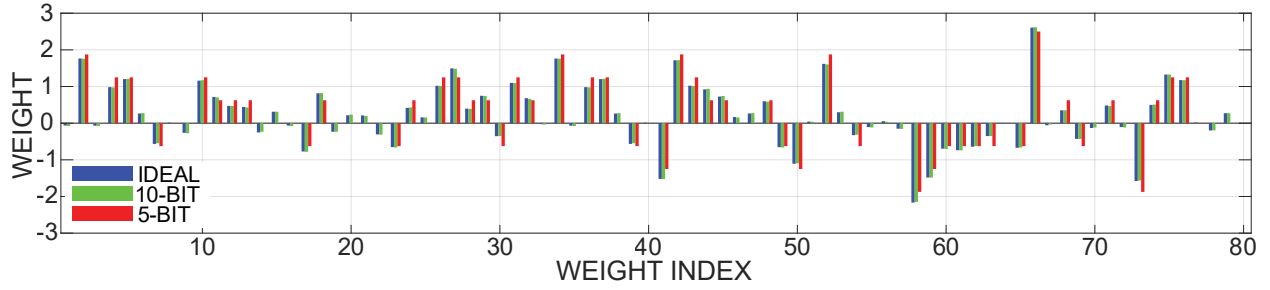


Figure 4.18: Simulation results showing the proximity of the implemented weights to the ideal value for 5-bit and 10-bit digital weights.

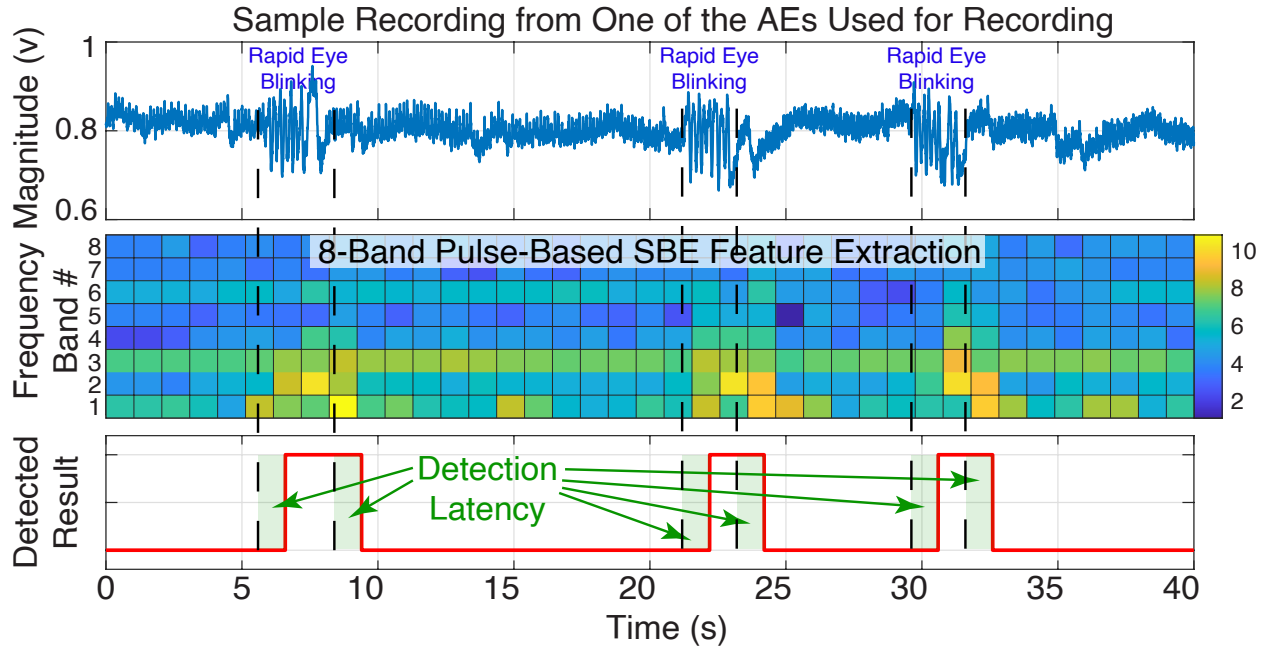


Figure 4.19: Measurement results showing detection of eye blinking event by the trained classifier.

hence all the weights would be estimated within these levels. By increasing the bit precision, we can increase the number of levels for weight estimation, thereby refining the accuracy of weight estimation, and in turn, improving the overall classification accuracy.

Table 4.1: Comparison with State-of-the-Art EEG-Based Seizure Detection Systems

Specification	TBioCAS 2016 [77]	JSSC 2022 [82]	This Work
Tech (nm)	180	40	180
Supply (V)	1	1.1, 0.7	1.8
Feature Extraction	BPF	TCA	Pulse-Based SBE
Classification	NL_SVM	GTCA-SVM	NL-B-SVM
Dataset	MIT	MIT+local	MIT
Number of Patients	24	24	21
Signal Type	EEG	EEG	EEG
Number of Channels	8	16	16
Power/Channel (μ W)	19.5 (Dig)* 10.5 (AFE)*	5.2 (Dig)* 10.3 (AFE)*	1.1 (Dig) 24.87 (HDR AFE+ Artifact Removal))
Active Electrode	No	No	Yes
Sensitivity (Vector)	95.1	97.8	96.4
SRAM	96k	134k	0
FAR/Specificity	0.94/Hour	99.5%	0.41/Hour
Latency (sec)	2	0.74	1

*:Estimated based on reported μ J/classification

4.3 Seizure Detection Results

Fig. 4.19 shows the measurement results of detection eye blinks using the proposed pulse-based energy band calculation algorithm using the multiplier-less implementation for the boosted SVM classifier. In this test the algorithm is first trained with real EEG recording data where the eye-blinking periods are marked manually. Next, the results shows how the increased level of energy band showing the eye-blinking period and how the classifier is able to detect the eye-blinking events.

Additionally, the proposed algorithm (feature extraction and classification) has been applied to 21 patients from CHB-MIT data set. It contains 991 hours EEG recorded signals that includes 136 seizure events. In these calculations the sensitivity is defined as the num-

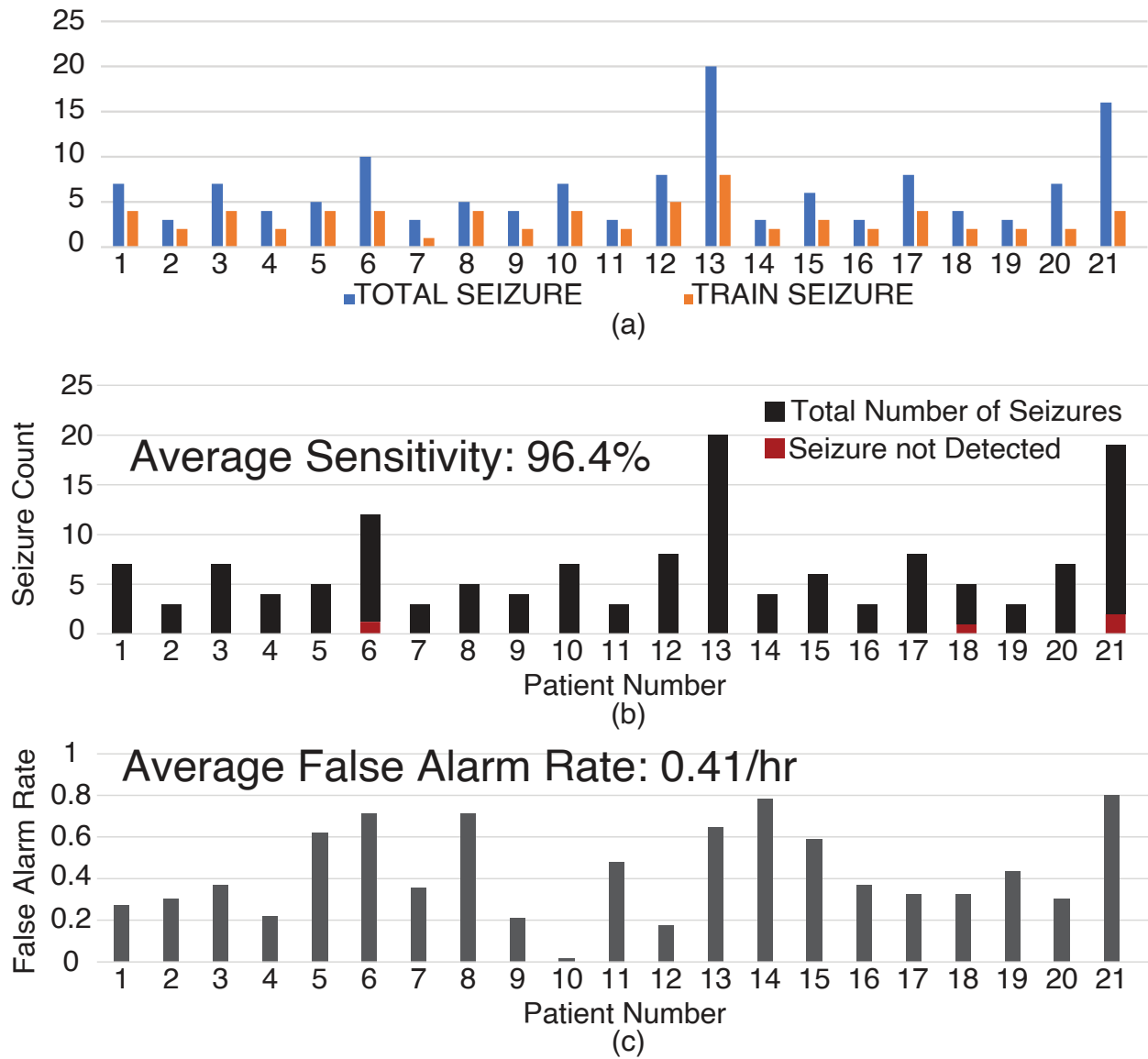


Figure 4.20: (a) The total seizure for each patient and the number of seizures that used to train the classifier. (b) Complete seizure detection for 16 patients and only missed few seizures in 4 patients with average of 94.85%. (c) False alarm rate less than one per hour for most patients with average of 0.49 per hour.

ber of seizure events that has been accurately classified as seizure over the total number of seizure events. The false alarm rate is defined as the average number of non-seizure events that has been mis-classified as a seizure event over a duration of one-hour.

Fig. 4.20(a) shows the total number of seizures for each patient and the number of seizures that were used to train the classifier. As it is shown in Fig. 4.20(b), all seizures have been successfully detected for 16 patients and classifier only missed 7 of the seizures in total in 4 patients. As shown in Fig. 4.20(c), for most of the patients' false alarm rate is less than one per hour which is comparable with the state of the art ([73, 75, 77, 78]). Therefore, using the proposed feature extraction and classification, an average sensitivity of 94.85% and a false alarm rate of 0.49 per hour has been achieved, while being needless of a storage unit, avoiding any non-linear operation, and reducing the computational complexity by two orders of magnitude.

Table 4.1 compares our proposed feature extraction and classification system with the state-of-the-art EEG-based seizure detection systems. This table highlights the superiority of our system in terms of power consumption of the digital block. Also, regarding the analog-front-end, our system is the only one that is compatible with a distributed structure hence allowing the implementation of active electrodes.

4.4 Chip Fabrication and Top-Level System Integration

Fig. 4.21 shows the chip micrograph of the presented IC, designed and fabricated in a 180nm standard CMOS technology. This IC includes analog blocks for (1) EEG signal recording, (2) ETI measurement, (3) Specific ADCs for the signal and ETI path, and (4) Regulator and bias generation, and digital blocks for (1) Decimation filters of the ADCs, (2) Motion artifact removal and feature extraction, and (3) Classifier. The design of the digital blocks was accomplished through the Verilog hardware description language, followed by synthesis with the Design Compiler software. Layout translation was conducted using Innovus, after which the digital blocks were combined with the analog blocks at the top-level integration stage of the IC. As shown in Fig. 4.21, the PCB used for performing the electrical measurement results, hosts 4 different ICs which are used specifically in CMRR measurements as it enables us to (a) have more than one channel to perform averaging to generate the common-mode voltage and (b) evaluate the effect of mismatch between different channels' gain and electrode-tissue interface impedance. Additionally, during the evaluation of feature extraction and classification circuits, one of the ICs is configured as the classifier and the other ones are used as feature extraction units.

Fig. 4.22 provides a comparative analysis of power consumption breakdown between a state-of-the-art design and our current work, measured per channel for various functional components in an EEG system. The left side of the figure details the power distribution in the state-of-the-art system, with the majority of power, being consumed by the analog front-

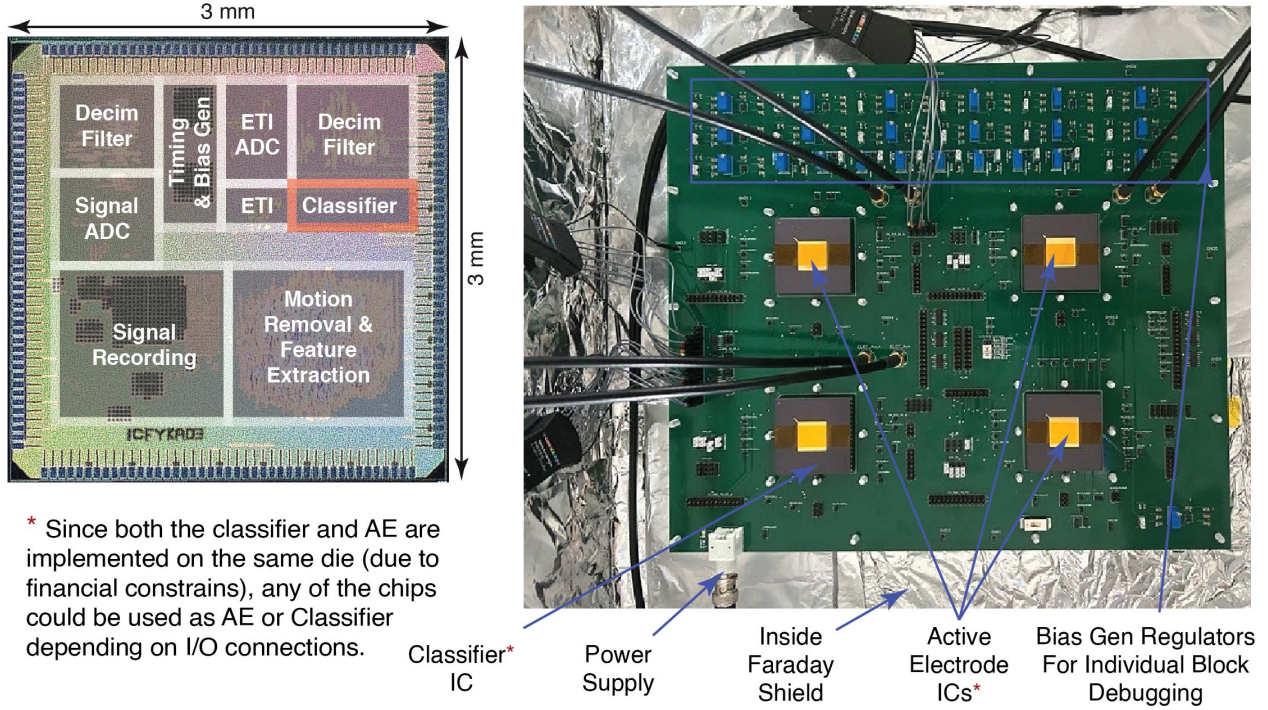


Figure 4.21: Annotated chip micrograph of the fabricated IC and the multi-chip PCB fabricated to test the presented IC.

end. The active electrode to backend communication (AE-to-BE comm) and the classifier are the next in line regarding the percentage of power consumption.

In contrast, our design, shown on the right side of the figure, exhibits a remarkable improvement in energy efficiency. The total power per channel has been substantially reduced to $26 \mu\text{W}$, which is 72.5% improvement. The analog front-end, traditionally a major power consumer, now operates with significantly improved efficiency at $20.71 \mu\text{W}$, a 54% improvement in comparison with the SoTA. Due to the drastic reduction in the required communication data rate, the AE-to-BE comm block, which had the second highest power consumption, now operates at only $0.25 \mu\text{W}$, which is 99.4% improvement. The classifier sees the most dramatic reduction, now requiring just $0.3 \mu\text{W}$, a negligible amount compared to

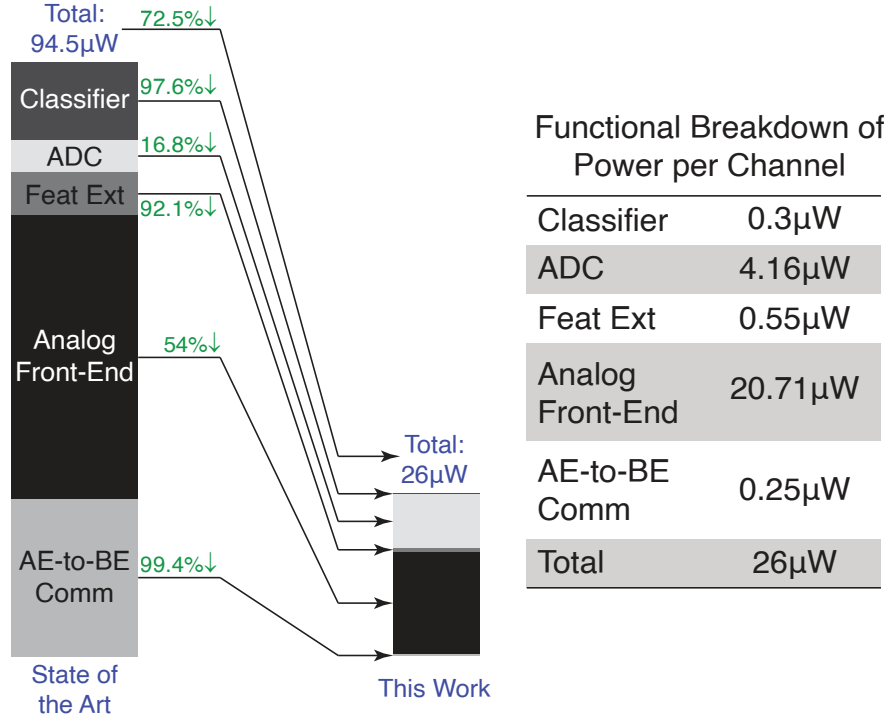


Figure 4.22: Power breakdown and comparison with the state-of-the-art design.

its earlier consumption. The power used by the ADC and feature extraction modules has also been considerably lowered to $4.16 \mu\text{W}$ and $0.55 \mu\text{W}$, respectively.

Fig. 4.23 offers a detailed visual overview of our EEG system’s hardware, highlighting the innovative daisy-chain structure of the active electrodes (AEs) and their seamless integration that contribute to the system’s compact and customizable design. Displayed prominently is an example of the multi-AE mounted system, where each AE is connected to the next, avoiding the need for multiple wires running from each AE back to the central system, thereby significantly reducing the design’s complexity and size. The AE boards, each equipped with connectors on their edges, facilitate this streamlined daisy-chain connectivity.

Additionally, each AE incorporates a manual DIP switch (CVS-01TB, Nidec Components Corporation) that enables the selection of individual AEs for calibration mode. This

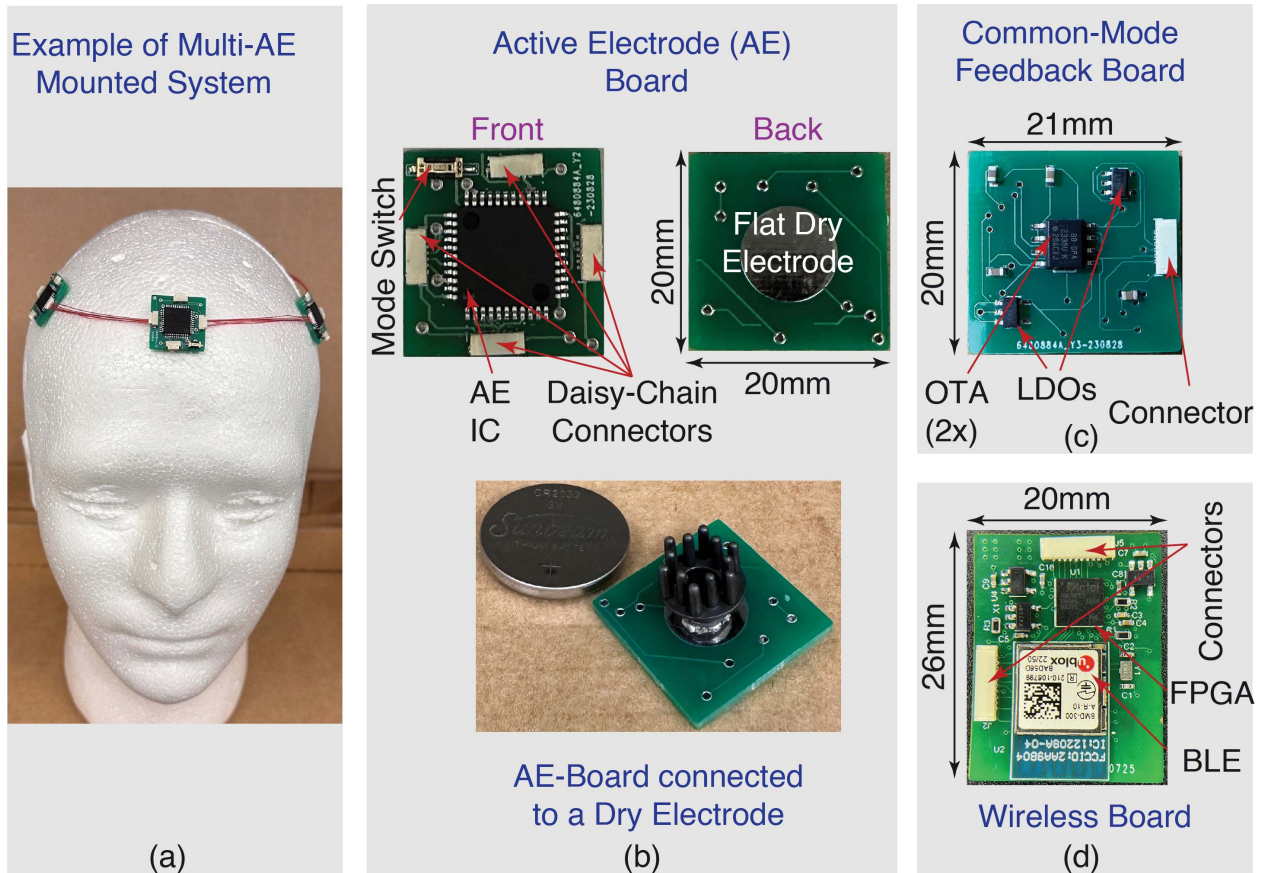


Figure 4.23: Overview of EEG System Hardware. (a) Multi-AE mounted system showcasing streamlined daisy-chain architecture. (b) Active Electrode Board with daisy-chain connectors and calibration mode switch, alongside its connection to a dry electrode. (c) Common-Mode Feedback Board. (d) Wireless Board featuring BLE for data communication.

arrangement results in a six-wire connection between AEs, which transmit essential signals for ground (GND), power supply (VDD), global clock, data, common-mode voltage, and the program signal (being set by the mode control switch). Additionally the front and back views of the Active Electrode Board are shown, highlighting how they interface with through-hair dry electrodes, which has been chosen based on their compact size and simple setup. The common-mode feedback board is also showcased, which is central to generating the common-mode voltage (V_{CM}) through averaging and hosts the Driven Right Leg (DRL) loop and regulators.

Completing the system's overview is the wireless board, tasked with the function of transmitting data wirelessly to a mobile or computer device. This board hosts a low-energy bluetooth controlled by the low power FPGA. This components enable the system for remote monitoring and data analysis, opening avenues for real-time data tracking and patient monitoring without the constraints of wired connections.

Chapter 5

Conclusion, Contributions and Future Work

5.1 Contributions and Relevant Publications

Considerable efforts have been made in the field of EEG recording, with a primary focus on capturing reliable EEG signals while also ensuring user comfort. This has resulted in building devices capable of limited out-patient EEG monitoring. Similarly, for seizure detection, many different types of algorithms have been developed with reasonable accuracy and power efficiency, which allows for their implementation on battery-powered devices.

Despite these progresses, there are still some challenges in this area. The primary obstacle in ambulatory EEG recording lies in effectively identifying and eliminating motion artifacts that occur due to electrode movement during patient activities. These artifacts exhibit considerably higher power levels, resulting in a wide dynamic range and heightened

power demands for the recording equipment. Additionally, achieving a robust common-mode rejection ratio (CMRR) for the entire system remains a challenging task, primarily due to mismatch in voltage gain and electrode-skin impedance among active electrodes.

Another challenge in realizing a high-channel count EEG recording device is the reduction of the number of wires. Current approaches, such as transmitting serialized data on a common bus or employing Frequency Division Multiplexing (FDM), significantly escalate the total power consumption. In the domain of seizure detection, the challenge is to develop a new system architecture that is compatible with active electrodes, consumes reasonable power, and maintains high detection accuracy. Therefore, the target of this study is to develop a fully-flexible, high dynamic range, artifact resilient EEG headset that is compatible with a distributed signal processing scheme.

Toward this target, we introduced the design and experimental characterization of an active electrode (AE) integrated circuit (IC) for wearable ambulatory EEG recording. The innovative architecture includes double common-mode (CM) rejection within each AE, ensuring that the CMRR remains robust despite variations in AE-to-AE gain and interface impedance. The active electrode (AE) offers high input impedance, surpassing $\text{super-T}\Omega$, providing robustness against changes in electrode-skin interface impedance across various recording channels, a crucial aspect for dry-electrode ambulatory systems. It also manages signal quantization and serialization, facilitating a distributed system using a single data bus for communication with the backend module, thus improving scalability. Furthermore, the AE includes features such as detecting unstable electrode-skin connections, dynamically

measuring and adjusting input DC levels, and incorporating a CM feedback loop to further enhance CMRR. This work has resulted in a conference paper and an extended journal paper that are published in 2021 IEEE Biomedical Circuits and Systems Conference (BioCAS) [83] and the IEEE Transactions on Biomedical Circuits and Systems (TBioCAS) [84], respectively.

Then we developed the second generation of our active electrode IC, which further improves the system scalability through the introduction of in-AE seizure detection while significantly reducing overall power consumption. This design features an AE-specific ETI-correlation-based circuit is implemented for motion artifact detection and suppression. An auto-ranging scheme in the analog front-end (AFE) improves dynamic range to avoid saturation or increasing harmonic distortion. An AE-specific-boosted distributed feed-forward common-mode rejection (CMR) enhancement method achieves high CMRR even in the presence of AE-to-AE input impedance (Z_{in}) mismatch. Feature extraction (FE) is performed in each AE, reducing AE-to-BE data communication power. To further reduce the power consumption, an ultra-low-power pulse-based method is employed in each FE. Classification is carried out using a neuromorphic multiplier-less boosted-SVM, which achieves comparable accuracy to a resource-intensive NL-SVM while consuming orders of magnitude less power. The results of this work has been accepted in the 2024 IEEE Custom Integrated Circuits Conference (CICC) and the extended version will be submitted to IEEE Journal of Solid-State Circuits.

5.2 Contributions

The following summarizes a list of accomplished contributions since the start of my PhD (September 2019):

- **A. Dabbaghian**, and H. Kassiri, & Fader, L. (Filer). (2024). Active Digital Electrode With Embedded Motion-Artifact Removal Boosted Common-Mode-Rejection, And Enhanced Dynamic Range For Ambulatory Electroencephalogram . United States Provisional **Patent Application No. 63/611,042**. Filed December 12, 2023.
- **A. Dabbaghian**, and H. Kassiri, “Modular Flexible 80-dB-DR Artifact-Resilient EEG Headset with Distributed Pulse-Based Feature Extraction and Multiplier-less Neuro-morphic Boosted Seizure Classifier,” accepted to appear in *2024 IEEE Custom Integrated Circuits Conference (CICC)*
- **A. Dabbaghian**, Y. El-Haji, M. Ghalamboran and H. Kassiri, “A $0.67\mu\text{V}$ -IIRN super-T Ω -ZIN $17.5\mu\text{W}/\text{Ch}$ Active Electrode with In-Channel Boosted CMRR for Distributed EEG Monitoring,” in *IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)*, vol. 18, no. 1, pp. 3-15, 2024.
- **A. Dabbaghian** and H. Kassiri, “An 8-Channel Ambulatory EEG Recording IC with In-Channel Fully-Analog Real-Time Motion Artifact Extraction and Removal,” in *IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)*, vol. 17, no. 5, pp. 999-1009, 2023.

- **A. Dabbaghian** and H. Kassiri, “An Active Electrode IC with Embedded Analog CMRR Enhancement for Interference- and Gain-Mismatch-Resilient EEG Recording,” in *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, pp. 1-5, 2021.
- **A. Dabbaghian** and H. Kassiri, “An 8-Channel 0.45mm²/Channel EEG Recording IC with ADC-Free Mixed-Signal In-Channel Motion Artifact Detection and Removal,” in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, 2020.
- T. Yousefi, **A. Dabbaghian**, and H. Kassiri, “Motion-Affected Electrode-Tissue Interface Characterization for Ambulatory EEG Recording,” in *2020 42nd Annual International Conference of the IEEE Engineering in Medicine & Biology Society (EMBC)*, pp. 4479-4482, July 2020.
- T. Yousefi, **A. Dabbaghian** and H. Kassiri, “A 3.12 pJ°C² Ultra-Low-Power Direct-ADC Multi-Range Temperature Sensor for IoT Nodes,” in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, 2020.
- T. Yousefi, M.Taghadosi, **A. Dabbaghian**, R. Siu, G.Grau, G.Zoidl and H. Kassiri, “An Energy-Efficient Optically-Enhanced Highly-Linear Implantable Wirelessly-Powered Bidirectional Optogenetic Neuro-Stimulator,” in *IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)*, vol. 14, no. 6, pp. 1274-1286, 2020.
- T. Yousefi, M.Taghadosi, **A. Dabbaghian**, R. Siu, G.Grau, G.Zoidl and H. Kassiri, “A 12.5 mg mm-Scale Inductively-Powered Light-Directivity-Enhanced Highly-

Linear Bidirectional Optogenetic Neuro-Stimulator,” in *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-4, 2020.

5.3 Future Work

As highlighted earlier, one of the advantages of in-channel DR boosting is its insensitivity to the latency associated with motion artifact estimation. This is a great opportunity to implement more intricate algorithms designed to achieve exceptionally precise motion removal. We can explore and implement algorithms of greater complexity, thereby enhancing the overall efficacy of motion artifact mitigation.

One notable avenue for realizing this enhanced performance is the integration of machine learning techniques. Unlike their simpler counterparts, such as correlation-based methods, machine learning algorithms exhibit a remarkable capacity for accuracy and adaptability. Leveraging machine learning in the context of motion artifact removal allows us to tap into advanced models that can recognize patterns and relationships within the data. These models possess the capability to adapt dynamically to the specific characteristics of the input data, resulting in more robust and reliable motion artifact estimation and removal. The utilization of machine learning techniques, therefore, represents a promising path towards achieving superior accuracy and efficiency in motion removal, contributing to the overall quality and reliability of signal processing across a wide spectrum of applications.

The purpose of implementing in-channel feature extraction was to achieve more power efficiency by reducing the required data rate for communication. Moreover, in-channel feature extraction brings an additional benefit. It empowers the capability to introduce a degree of

detection and classification within each individual channel. This becomes particularly valuable in applications such as seizure detection, where data collected from different channels may not carry the same weight or significance in the classifier’s decision-making process. By determining which channels to include in the classifier’s decision and at what precision level, it becomes possible to tailor the system’s power consumption to specific requirements. This control over channel inclusion and precision is beneficial especially in high-channel count scenarios, where power optimization plays a crucial role in system design and operation.

Another modification to build a dynamic system in terms of channel selection and precision control is to add more control to the power and noise level of the analog/mixed signal stages. It is notable to mention that by realizing an in-channel decision maker for required precision, due to the power reduction achieved by data rate reduction, the overall power consumption is dominated by the blocks that burn static power such as analog front-end. One solution is to make such blocks programmable in terms of power consumption and accuracy. For example, by adjusting the current bias of the first and second stage OTAs we can reach to an acceptable noise level while burning lower power. However, this would require further modifications to keep the bandwidth in the desired range. In general, adding more configurability to the system such as the gain of the first stage or the adjustable ADC resolution would help in tailoring the system for any specific application.

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