AN 8-CHANNEL BIDIRECTIONAL NEUROSTIMULATOR IC WITH A HIGHLY-LINEAR HIGH-DYNAMIC-RANGE ADC-DIRECT ARCHITECTURE FOR SIMULTANEOUS RECORDING AND STIMULATION

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ABSTRACT

This thesis presents the design, implementation, and validation of an 8-channel bidirectional neurostimulator IC with a highly-linear high-dynamic-range ADC-direct architecture for simultaneous recording and stimulation. Each channel hosts a novel highly-linear high-dynamic-range recording architecture capable of amplification and quantization of brain's neural signals in the presence of large differential-mode and common-mode stimulation artifacts, as well as a fully-programmable 8-bit current-mode electrical stimulator. The architecture enables the possibility of a patient-specific stimulation therapy required for the next generation of implantable closed-loop neuro-stimulators used for treatment of various neurological disorders. Both system- and circuit-level design, implementation, challenges, and requirements are explained, and a critical comparison with the state-of-the-art is presented.

The proposed design adopts an ADC-direct architecture employing a dual-loop SAR-assisted continuous-time delta-sigma ADC architecture for differential-mode stimulation artifacts and offset removal. Common-mode artifacts are handled using a novel highly-linear Gm-C integrator that is used as the front-end stage of the neural ADC. The presented channel achieves a high input impedance (1.8 GΩ at 1 kHz), 400 mV linear input signal range, 94 dB dynamic range, and consumes 4.6 µW with a signal bandwidth of 5 kHz.

To my parents

for their unconditional love and support

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Introduction

1.1 Motivation and objective

The Electrical stimulation has been established as a proven method for better understanding of brain functions (e.g., memory, sensory, etc.) and dysfunctions (e.g., neurological disorders) through manipulation of neuro-electrical activity. It has been shown to be effective in treatment of several brain disorders such as epilepsy, Parkinson's disease, and chronic pain [1]-[4]. Driven by this, over the past two decades, many implantable neuro-stimulator devices have been reported aiming to provide an alternative treatment option for the patients of these disorders who are refractory to drugs or not deemed candidates for surgery. The early generations of these devices had an open-loop architecture, meaning that they stimulated the brain without any information on the real-time brain state [5], [6]. The more recent devices use a closed-loop architecture, where the stimulation is conducted while the brain neural activity is being continuously monitored.

This architecture allows for real-time adjustment of the stimulation pulse parameters and timing to evaluate and optimize the efficacy of the stimulation [7], [8].

Over the past few decades, and thanks to the advancements in integrated circuit (IC) microfabrication technologies, different types of technologies have been developed to record brain's neuro-electrical signals with various spatial resolution and coverage. This includes electroencephalography (EEG), which records neural signals from the scalp surface, electrocorticography (ECoG) which records from the cortical surface of the brain, and intra-cranial EEG (iEEG) which uses mesh or depth electrodes to record neural signals from different depths in the brain. Among these, EEG is the least invasive method and provides the largest spatial coverage (up to the full brain) with lowest spatial resolution (~>1cm), while iEEG is the most invasive one and sits at the other end of spectrum, offering the highest spatial resolution (~μms) and smallest spatial coverage [9]. Depending on the targeted application, the tolerance to invasiveness, and the spatial resolution requirement, either of these technologies are used. For implantable neuro-stimulators, since both recording and the stimulation are applied to a small region in the brain (e.g., seizure-inducing cells for focal epilepsy), iEEG is the recording method of choice. iEEG signals are divided into local field potentials (LFP) which represent the slow (<500Hz) potential variations (up to 1mV magnitude) of the recording sites, and action potentials (AP) which represent the neural spikes with a magnitude ranging from 20-100 μV and a bandwidth up to 5 kHz (Figure 1.1) . There is valuable information encoded into both these signals making them both necessary to be captured by the recording device.

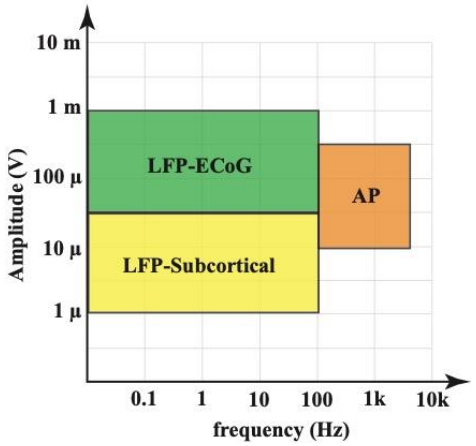

Figure 1.1 Neural signals range [10]

As mentioned, the most important advantage of closed-loop neurostimulators is their ability to conduct stimulation while being aware of the real-time brain activity. For example, in the case of an epileptic patient, it is extremely important (for the treatment success) to inject stimulation pulses to the brain exactly at the onset of a seizure. Given that these seizures are very infrequent (e.g., once a day or a week, depending on the severity of the disease), the device either needs to continuously stimulate the brain at all times (practically frying the brain and demands an un-implantable large battery as energy supply) or only stimulate when a seizure onset is detected. The closed-loop architecture allows for the device to continuously monitor the neural activity and only stimulate when an upcoming seizure is detected.

Ideally, the recording circuit should be used to record brain response to the stimulation before, during, immediately after, and long after the stimulation. This will allow for customizing the stimulation parameters in a patient-specific manner. However, the state-of-the-art technology is only capable of recording the brain signals before and

long after the stimulation. The major issue with conducting recording during and immediately after stimulation is extremely large (>100mV) fluctuations in the signals during stimulation, which are called stimulation artifacts. These artifacts can easily saturate the conventional amplifiers that are designed to amplify small neural signals (<1-2mV). This has made simultaneous recording and stimulation an impossible task for state-of-the-art neural recording electronic circuits, and consequently, has prevented the neuro-stimulation treatment to become a patient-specific therapy.

The main objective of this research is to design, develop, and characterize an integrated circuit that is capable of conducting simultaneous recording and stimulation, while meeting all the other design requirements for a neurostimulation device, including noise, power, area, bandwidth, and scalability.

1.2 Neural Recording Challenges

An implantable neuro-stimulator device could have many recording/stimulations channels (i.e., integrated circuits connected to each electrode for recording or stimulation). In each channel, a low-noise amplifier is the front-end stage connected to an electrode to amplify the signal that is induced on it. The amplifier should always have a differential architecture, as it requires to amplify the difference between the signal sensed at its associated electrode and the signal at a reference electrode that is shared among all channels. The differential recording removes any random interferences and noise that are common among all electrodes and only sends out the neural activity that is unique to each electrode for signal processing.

As mentioned, the neural signals to be amplified (LFP or AP) have a magnitude range of 10µV-1mV and a frequency range of 1Hz-5kHz. In addition to these, various offsets and artifacts could appear on top of these signals, which should be handled by the recording circuit. In the remaining of this section, we will discuss these challenges a bit more in details.

1.2.1 Stimulation Artifacts

Figure 1.2 depicts a simplified generic closed-loop stimulation setup. As shown, neural signals are first amplified, then quantized using an analog to digital converter (ADC). The digitized signals are fed to a backend signal processing unit where the decision for triggering stimulation as well as adjusting stimulation parameters are made and sent to a current-mode digital to analog converter (DAC) to convert the stimulation commands into electrical currents that will be injected into the brain. When stimulation is applied to the brain, a large amount of charges will be injected, causing large voltage fluctuation in the brain. Due to the non-linear and time-variant nature of the brain's neural networks, the magnitude and shape of this artifact could vary significantly and is unpredictable. These artifacts not only affect the signals recorded at the same electrode, but also all the neighboring electrodes, of course, with different levels of severity depending on their proximity to the stimulating electrode. As such, the reference electrode is also affected. Accordingly, these large fluctuations at the input of an amplifier can be classified into two types: (1) fluctuations that are common between the recording and the reference electrodes, known as common-mode (CM) artifacts, and (2) those that are different between the

recording and the reference electrodes, known as differential-mode (DM) artifacts. The value of these artifacts depends on the tissue impedance, stimulator's maximum current, electrode distance relative to the stimulation site, and electrode impedance mismatch [11]. Their typical value for each of DM and CM artifacts is up to 200 mV [12].

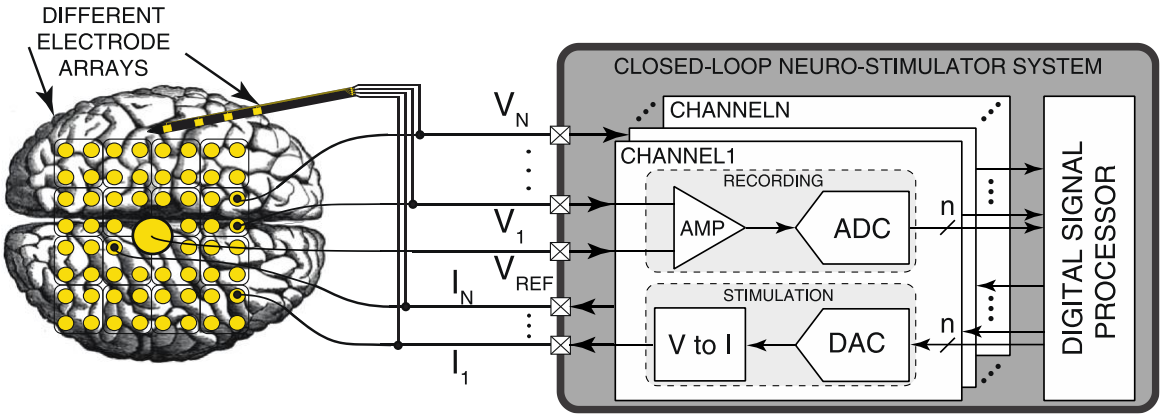

Figure 1.2 Top-level block diagram of a multi-channel closed-loop neurostimulation system.

1.2.2 Electrode DC Offset (EDO)

EDO is generated because of the chemical reactions (oxidation and reduction) between the electrode and the brain tissue [13]. These reactions result in a different DC level at each electrode. Therefore, they cause a DC difference between reference electrode and the recording electrode and in the order is up to ±50 mV [14].

Removing the EDO is done in different ways in neural front-end designs reported in the literature. The most straight-forward method is using AC-coupled amplifiers [15]. Figure 1.3 depicts a conventional AC-coupled neural amplifier. The closed-loop gain of this amplifier is C_1/C_2, and the low-frequency high-pass pole (that sets the minimum input frequency that the amplifier can record) is set by $1/R_2C_2$. C_2 should be chosen much larger

than the parasitic capacitors (typically 100 fF) to limit their effect on the gain and linearity of the amplifier [16]. Therefore, C_1 should be larger than 10 pF to achieve high gain and a high-pass pole of less than 1 Hz. Integrating two of such a large capacitance in each channel increases the channel area beyond the area budget that is acceptable for systems that aim to integrate many (i.e., >1000) channels. The presence of the capacitance at the input also prevents us from using certain noise reduction techniques such as chopper stabilization at the input, as will be discussed later.

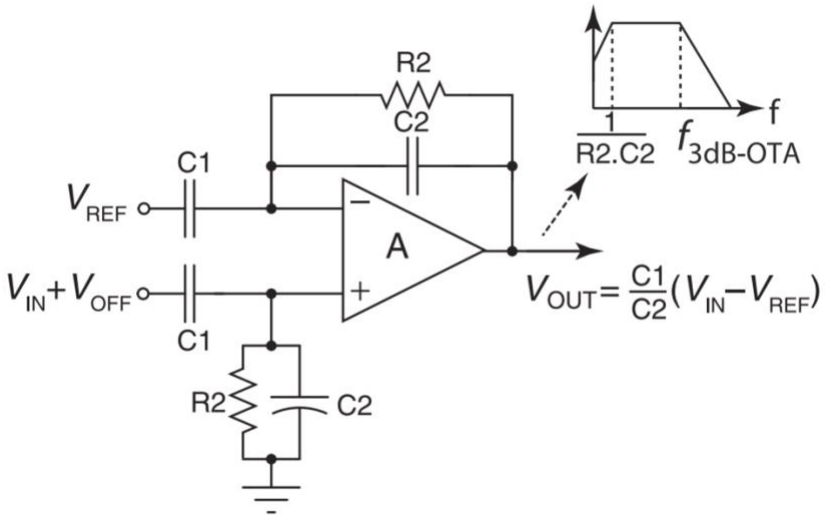

Figure 1.3 Conventional AC-coupled amplifier [15]

To overcome this limitation, DC-coupled amplifiers have been investigated in recent years. The offset in these amplifiers is removed using a mixed-signal path [14]. Figure 1.4 shows a conceptual simplified representation of such circuit. In this architecture, the input is DC-coupled to the electrode, and a low-pass feedback path is used to remove the offset. Digital low-pass filter has a very small low-pass pole, forcing its output to be the summation of the forward-path output's low-frequency content. Then, using a DAC, it

will be translated to analog without area penalty. However, the amount of EDO that could be cancelled using this architecture is very limited and could only be increased to the required level at the cost of increasing the number of taps in the feedback's digital low-pass filter (LPF), which leads to a significant increase in the area (opposing the initial purpose of area minimization) [17].

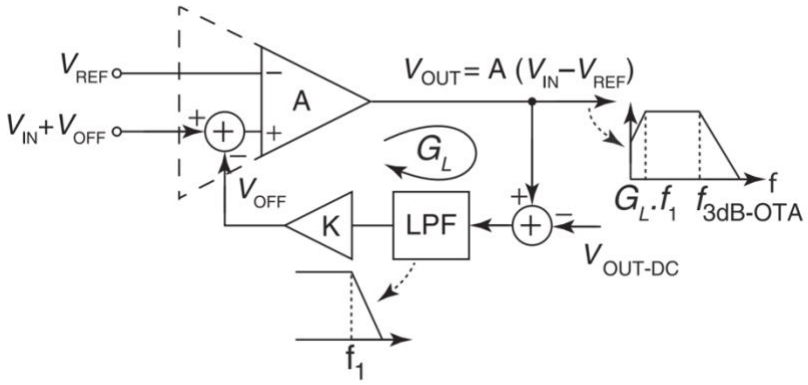

Figure 1.4 Mixed-signal dc-cancellation feedback [14]

1.2.3 Input-referred Noise (IRN)

The electronic recording circuit generates two types of thermal and flicker noise when it operates. When referring the effect of these noise to the input of the amplifier, their overall effect should be less than the smallest signal that we intend to record. Another source of noise at the input of the amplifier comes from the background neural activity in the vicinity of the recording electrode, which is called the background noise. This noise is about 10 μV_{rms} in 5 kHz [11]. The recording circuit should be designed in a way that its noise contribution at the input does not add more than 10% to this number. The total noise of the system is equal to Equation 1.1.

$$n_{Total} = \sqrt{n_{Electrode}^2 + n_{Gm-stage}^2} \quad \textbf{(1.1)}$$

Where n_{Total} is the total noise of the system, $n_{Electrode}$ is the background noise picked-up by neural recording electrodes, and $n_{Gm\text{-}stage}$ is the IRN of the G_m-stage. It should be noted that all the noises are rms values in 5 kHz bandwidth. According to this equation, IRN of the G_m-stage should be limited to 4.5 μV.

In addition to the thermal noise that has a flat spectrum (i.e., constant power at all frequencies), the other noise generated by the recording amplifier is the flicker noise or 1/f noise (i.e., its power spectral density increases as the frequency decreases) [15]. Conventionally, reducing this noise has been done by choosing large input devices. However, the method is not area-efficient [18]. Correlated-double-sampling is another technique that is used, which comes at the cost of it doubles the white noise and inability to remove the flicker noise's high-frequency content [16]. The most popular method for flicker noise cancellation is chopper-stabilization technique, which effectively removes flicker noise as long as the chopping frequency is high enough, and the application nodes have a small time constant [19].

1.2.4 Input Impedance

Increasing the number of channels is neural recording is the new trend leading to better understanding of the brain. However, one of the most important challenges that this will cause is the impedance mismatch between the reference and input electrode. In most of the architectures the reference electrode is shared between all the channels as shown in

Figure 1.5. Therefore, the equivalent capacitance of this channel is by a factor of n larger than the other inputs, where n is the number of channels. This large input mismatch results in common-mode rejection ratio (CMRR) degradation. Total CMRR (TCMRR) is equal to Equation 1.2 [20].

$$\boldsymbol{TCMRR} = \left(\frac{\mathbf{1}}{\boldsymbol{CMRR}} + \left(\frac{\mathbf{1+2}\left(\left|\frac{\boldsymbol{Z_{in}}}{\boldsymbol{Z_e}}\right|\right)\boldsymbol{+n\epsilon}}{\mathbf{2(}\boldsymbol{n\epsilon}\mathbf{-1)}}\right)^{\mathbf{-1}}\right)^{\mathbf{-1}} \quad \textbf{(1.2)}$$

where Z_{IN} and Z_e are the input impedance of the amplifier and the electrode impedance, respectively. ϵ is a multiplier that indicates the impedance difference between the reference and input electrodes (ϵ= 1 when both electrodes are similar).

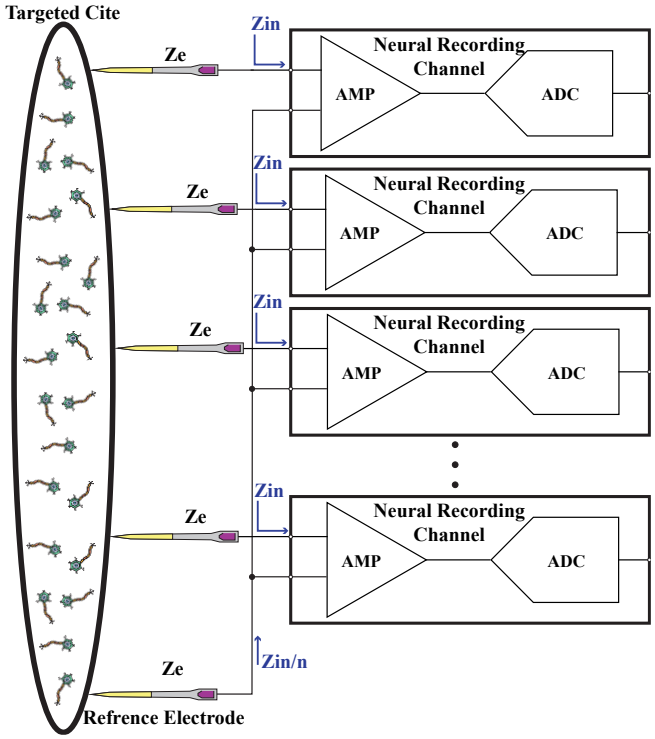

Figure 1.5 Typical multi-channel neural recording setup [20].

The majority of the available electrodes have an impedance ranging from 10 kΩ to 2.5 MΩ [17]. The majority of the neural recording front-ends have used input capacitor leading to low-input impedance [15], [19], [22], [23]. If we assume that the input impedance is 20 MΩ [12] and the electrode has 250 kΩ impedance the Z_{in}/Z_e can be as low as 80 leading to TCMRR of less than 70 dB for more than 1 channel [20]. Therefore, the input impedance not only is important for uniform and perfect amplification of the signal but also it directly affects the system CMRR. Hence, having a large input impedance in all the frequency range is one of the most important challenges in neural recording front-ends.

1.3 State-of-the-art Circuits for Simultaneous Recording and Stimulation

As mentioned, this work aims to enable simultaneous recording and stimulation. As described in section 1.2.1., the CM and DM artifacts generated by stimulation could have a magnitude up to 200 mV, and unlike EDO, cannot be separated from neural signals in the frequency domain [24]. DM artifacts saturate the neural amplifier, and CM artifacts change the amplifier's biasing point, which at the minimum, changes the amplifier's gain, noise performance, etc. if it does not drive the amplifier to the cut-off mode.

Figure 1.6 depicts an example of how a DM artifact affects neural signals. As shown, the DC level of the differential signal at the input of the amplifier changes by up to 200 mV upon arrival of a stimulation pulse (the red trace). To successfully record the signal in the presence of such a large signal's DC level change, the recording circuit is expected to (a) not get saturated because of this, and (b) be able to resume recording neuro-electrical

activity as fast as possible. In this figure, the green trace shows what such an amplifier is supposed to generate as an output. As shown, the circuit should be capable of quickly recovering from the large DC level change and resume recording even in the presence of such a large DC offset at the input. The success of the amplifier in doing so is measured by (1) the signal to noise ratio of the output signal, and (2) how fast it can recover from the DM artifact. Given that the stimulation pulse width is typically in the order of 10s of milliseconds, a recovery time under 1 msec is a commonly-accepted desirable outcome.

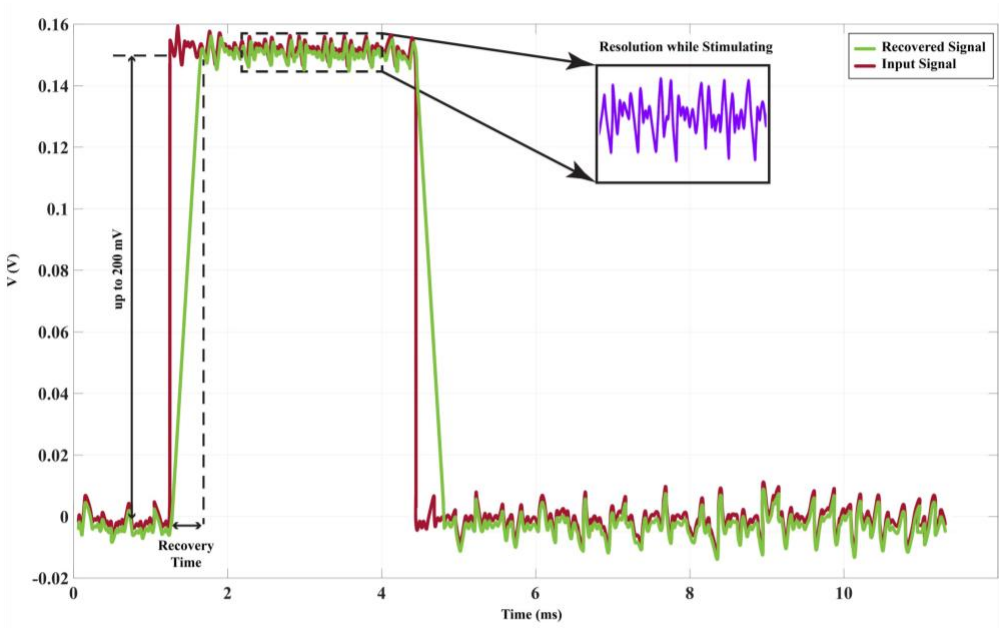

Figure 1.6 Recording channel's output in response to differential artifacts [12]

In order to prevent amplifier's saturation, its voltage gain should be reduced. However, reducing the amplifier's gain increases the ADC's required input-referred noise level, hence, its power consumption. Additionally, the required ADC's DR (i.e., the ratio of the largest to smallest signal that needs to be resolved), is quite high. To tolerate up to

200 mV artifact a DR of ~90dB is required. Designing such an ADC is challenging and increases the power consumption beyond the channel budget [25].

In literature, several methods have been investigated to address this challenge. In [26] blanking amplifier is suggested to prevent saturation. In this method, recording channels will be turned off whenever stimulation is enabled. The drawback of this method is the data loss of very important neural information during and immediately after the stimulation. Additionally, due to very large time constant of the amplifier's input node (mainly because of its extremely high input impedance), once the stimulation is over and the recording circuit turns back on, it takes 10s of milliseconds for the inputs to return to their normal DC level so that the amplifier can resume normal operation. Therefore, even when the stimulation is over, it takes a similar amount of time for the amplifier to be able to record neural signals again.

In [27], the authors have suggested a mixed-signal solution where the stimulation pattern will be predicted using a digital block and then subtracted from the input. The main challenge in this solution is predicting the stimulation pattern. The brain is a complex non-linear system. Therefore, its response is different for different channels making the success of prediction very limited. Generally, all methods based on artifact prediction, at best, can only prevent the amplifier from saturation, and they cannot offer recording during stimulation as the pseudo-random residual error from subtracting the signal from artifact prediction is typically an order of magnitude larger than the signal of interest.

As mentioned, artifacts and neural signals cannot be separated in frequency domain. On the other hand, the amplitude of them are orders of magnitude different. [28] suggested a VCO-based front-end to convert voltage into frequency, where the large DR can be handled in a much more energy efficient manner. Using this front-end the artifacts and neural signals can be separated. Artifacts will be translated to high frequencies and neural signals will be converted to low-frequency signals. Therefore, a low-pass filter can be used to remove the artifacts easily. However, achieving linearity in VCO for such a large input voltage DR is challenging. In the suggested design, a digital non-linearity correction is used to address this issue, but the input range of the design remain limited to artifacts up to ±50 mV. The CM artifacts rejection is also limited to 50 mV.

The most straight-forward solution for increasing the DR is to lower the amplifier gain and increase the ADC resolution. [29] is a good example of this technique. This design is used an amplifier with a gain of 8. The amplifier is chopped leading to low input impedance. Therefore, an impedance-boosting-loop is added to increase the impedance. However, the boosting factor of this loop decreases in higher frequency and the input impedance drops to about 10 MΩ at 5 kHz. To supress CM artifacts, a CM cancellation path is added to the amplifier sensing the CM and keeping constant by subtraction. Using this technique, CM artifact tolerance is 650 mV. Additionally, a 3rd-order (delta-sigma) ΔΣ ADC is used for digitization achieving 15.2 ENOB. The architecture includes about 40 pF capacitor. As mentioned earlier, such a large capacitance prevents the implantable system

from integrating a large number of these channels. Also, the dynamic range (DR) is limited to 81 dB while it has high power consumption comparing with state-of-the-art.

Another method for increasing the DR is using ADC-direct designs. The idea is to merge the amplification and the ADC into one stage to use the power budget of both blocks for achieving the targeted high DR. An example of such architecture is presented in [12] and shown in Figure 1.7. In this design a 2^{nd}-order ΔΣ ADC is used as the front-end with a G_m-C stage as the loop integrator. This architecture includes a 12-bit DAC. When there no artifact present, the DAC output changes by one LSB based on the comparator's decision. When artifacts are applied, the LSB cannot flip the voltage of the integrating capacitor and successive outputs will have the same polarity. After 5 consecutive 1s, the digital autoranging will be enabled to relax the resolution by doubling the step size of the DAC until detecting an opposite polarity at the output of the comparator. This design has reached a 92 dB DR while the power consumption is only 0.9 µW for 500 Hz bandwidth. One of the drawbacks of this design is its low input impedance. In this design summing node of the ΔΣ ADC is realized at the input using capacitors. This forms a switched-capacitor structure with an equivalent impedance that is much lower than what is required by neural front-ends. Besides, this design does not have immunity to CM artifacts, and the amplifier's gain changes depending on the CM artifacts. The other issue is that the chopper frequency is chosen equal to f_{samp}, and the feedback is applied to a node with a large capacitor causing fold-back noise [25].

In this work we will present an ADC-direct neural recording channel that uses a novel G_m-stage capable of handling large CM artifacts up to ±200 mV, and a dual-loop architecture for handling DM artifacts up to ±200 mV. The proposed architecture uses a SAR-assisted ΔΣ ADC to achieve a DR higher than 90 dB while maintaining a high input impedance, low input-referred noise, and low power consumption.

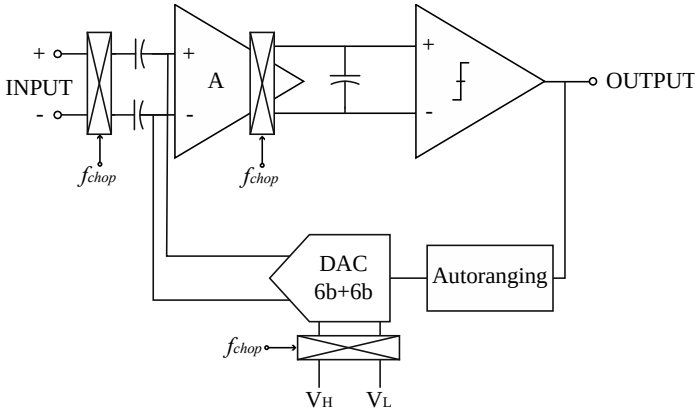

Figure 1.7 ADC-direct front-end [7]

1.4 Thesis Organization

Chapter 2 presents the system-level design of the suggested ADC-direct neural recording channel. It also reports the simulation results of a MATLAB-based model of the design. The focus of this chapter is on the system-level functionality of the proposed architecture.

Chapter 3 presents the circuit level design and implementation of the proposed recording and stimulation channel. In this chapter, design requirements, challenges, and detailed implementation and operation of each circuit block is discussed separately, and its simulation results are reported.

Chapter 4 is the conclusion of the thesis. It also discusses possible future directions for this research work.

Chapter 2

System-Level Design of the Proposed SAR-Assisted ΔΣ Neural ADC

As described in the previous chapter, designing a neural recording channel that can handle simultaneous neural recording and stimulation requires a circuit that can amplify and quantize signals in the range of 10 μV to 100s of millivolts. This translates into a required DR greater than 90 dB, or a quantization resolution of 13-14 bits.

For conventional neural recording channels (i.e., no simultaneous stimulation) where a maximum 10-bit resolution is sufficient, SAR ADCs are typical choice of data converter, mainly due to their inherent energy efficiency. However, their power consumption increases by 4x for every additional bit that is added to the resolution. Therefore, while a 10-bit SAR ADC can be realized with 10s of nW, realizing a 14-bit SAR ADC increases the power by x256, which is way beyond our acceptable channel's power budget, as discussed in the previous chapter. Additionally, achieving a resolution of >10 bits for the capacitive DAC used in SAR ADCs is extremely difficult.

On the other hand, oversampling ΔΣ converters are known for the capability to achieve very high resolutions (e.g., >20 bits) without requiring high precision from their analog and mixed-signal building blocks such as the track-and-hold or the comparator. This is done mainly by reducing the quantization noise using a combination of oversampling and noise shaping [30]. However, since the dynamic power consumption of ΔΣ converters is directly proportional to their oversampling ratio, achieving high resolutions (e.g. 14 bits) comes at a significant power penalty.

Based on the above, in this work, we propose a SAR-assisted ΔΣ ADC as a hybrid solution that leverages the advantages of both architectures. Prior to discussing the circuit-level implementation, in this chapter, the system-level architecture of the proposed recording channel and its principal of operation are explained. The functionality of the suggested architecture is verified using a MATLAB-based model.

Figure 2.1 depicts the proposed top-level block diagram for the presented multi-channel recording system. As shown, an ADC-direct architecture is adopted for the channel where the amplification and quantization take place in the ADC. This allows us to leverage mixed-signal techniques to avoid the amplifier saturation during stimulation. However, it also transfers all the design requirements for the recording front-end (i.e., low input-referred noise, high input impedance, voltage gain, high CMRR, etc.) to the ADC. For the ADC, a continuous-time differential-input ΔΣ modulator with a low-noise high-Z_{in} front-end and a low DR that is sufficient for recording neural signals with up to ~1-2 mV magnitude. It is expected that a large DC offset between the differential inputs, or a large

DM artifact saturates the modulator. Upon detection of such an event, the channel will enter an “artifact recovery” mode, in which a SAR-based feedback loop is employed to estimate the magnitude of the artifact and successively create an intentional opposing imbalance in the front-end gain stage to fully compensate the effect of artifact. Once the recovery is completed, the channel returns to the “recording mode” and the modulator resumes its normal operation. To compensate an offset/artifact with a magnitude of 200 mV with a residue that is smaller than 0.5 mV, the SAR approximation requires about 9 bits of resolution [31]. Using the typically high-frequency clock of the ΔΣ modulator (due to oversampling), this translates into 10s of micro-seconds for the “artifact recovery” mode to be completed. This is negligible and has a minimal impact on the quality of recording, when the input neural signal frequency bandwidth (<5kHz) is considered.

It should be mentioned that in the proposed ΔΣ modulator, the differential mode low-noise front-end is expected to be able to yield a constant amplification gain for neural signals with a large range of common mode (CM) voltage, and only the DM artifacts are to be compensated through the above-described mechanism.

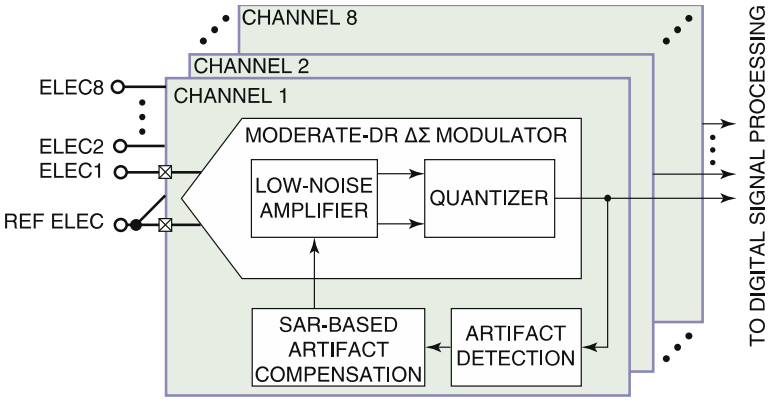

Figure 2.1 The proposed top-level block diagram of the presented multi-channel system.

2.1 Moderate DR ΔΣ Modulator

As mentioned, the modulator is supposed to handle signals during the normal recording mode of the channel, where input magnitude is in the range of 10 µV to 1 mV. Therefore, the required DR is equal to Equation 2.1. It should be noted that artifacts and EDO voltages will be removed before entering the loop. Therefore, the loop resolution is determined by the neural signals.

$$\boldsymbol{Dynamic\ Range = \frac{1\ mV}{10\ \mu V} = 100 = 40\ dB} \quad \textbf{(2.1)}$$

Considering the relatively low DR and to avoid stability complications, a 1st-order modulator is employed. Also, to take advantage of its inherent linearity, a 1-bit coarse quantizer (i.e., a comparator) is used within the modulator. Equation 2.2 shows how the signal to quantization noise ratio (SQNR) of a 1st-order ΔΣ modulator is calculated [30].

$$\boldsymbol{SQNR = \frac{9M^2(OSR)^3}{2\pi^2}} \quad (2.2)$$

where M is the quantizer's resolution and OSR is the oversampling ratio. Based on the equation, for M=1, an OSR of ~40 will be sufficient to achieve the targeted resolution. However, in this equation only quantization noise is considered. Hence, to account for other noise sources, OSR should be increased (e.g., 100) to ensure the SNR requirement is met. Considering the low frequency nature of the input signals (<5 kHz), such an OSR is acceptable in terms of dynamic power consumption.

Figure 2.2 shows a generic system-level block diagram of a 1st-order ΔΣ modulator. In its simplest form of implementation, it requires only an integrator, a coarse 1-bit quantizer, and a 1-bit inherently-linear DAC.

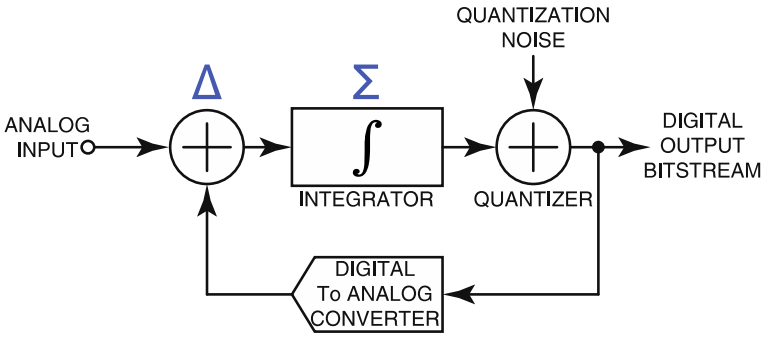

Figure 2.2 System-level block diagram of a 1st-order ΔΣ [30].

ΔΣ modulators are oversampling ADCs achieving very high SNR due to their noise shaping characteristic. Noise shaping can be explained in both time and frequency domain. In time domain, the assumption is that the signal is much slower than the system clock. Hence, the quantization noise of the consecutive samples is equal. The loop realizes a delta between consecutive samples, and therefore it reduces the quantization noise [32].

Figure 2.3 can be used to justify the noise-shaping in frequency-domain. According to this figure the transfer function of the quantization noise is equal to Equation Figure 2.3 Block diagram of ΔΣ modulator in frequency-domain [30].

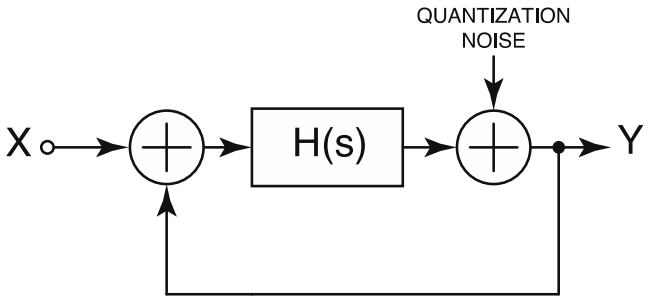

Figure 2.3 Block diagram of ΔΣ modulator in frequency-domain [30].

$$\frac{\boldsymbol{Y(s)}}{\boldsymbol{Q(s)}} = \frac{\mathbf{1}}{\mathbf{1}+\boldsymbol{H(s)}} \tag{2.3}$$

As shown before, H(s) is the integrator therefore Q(s) is equal to Equation 2.4.

$$\frac{Y(s)}{Q(s)} = \frac{s}{s+1} \tag{2.4}$$

Therefore, the spectrum of the quantization noise is shaped. Placing an ADC and a DAC in the feedback loop of the ΔΣ modulator ensures that Y(s) always tracks X(s) and the quantization noise is reduced as long as the loop gain is high enough which is true in low frequencies since H(s) is an integrator [32].

The subtraction (for the negative feedback) and integration could be implemented in many different ways as have been reported in the literature [12], [29]. However, in the proposed channel, since the modulator is directly connected to the electrodes, its first stage needs to be implemented in a way that it meets several requirements simultaneously. As discussed in the previous chapter, the front-end stage needs to yield a high input impedance, low input-referred noise, high CMRR, tolerance to large CM variations, tolerance to large DC offsets between the two inputs, and a descent amount of signal amplification to relax the noise requirements of the subsequent stages. All of the above need to be done while maintaining the area and power consumption at the minimum possible level to enable integration of a large number of these channels on an implantable device.

Figure 2.4 depicts the architecture we have used in this work, which employs a G_m-C integrator along with a current-mode DAC. The key advantage here is that the amplification is performed within the integrator, and more importantly, prior to subtraction. This allows for using various types of differential transconductance stages that can meet the noise, impedance, and CMRR requirements for neural recording. Additionally, the

subtraction and integration are both performed on a passive element at zero additional power cost. Of course, various circuit- and system-level design techniques need to be utilized to make sure that the gm stage is not saturated due to large CM variations, EDO, or stimulation artifacts. The system-level techniques used to handle large differential-mode offsets and artifacts are described in Section 2.3 and the circuit-level ideas for handling CM variations are covered in the next chapter where the integrated circuit implementation of the entire system is described.

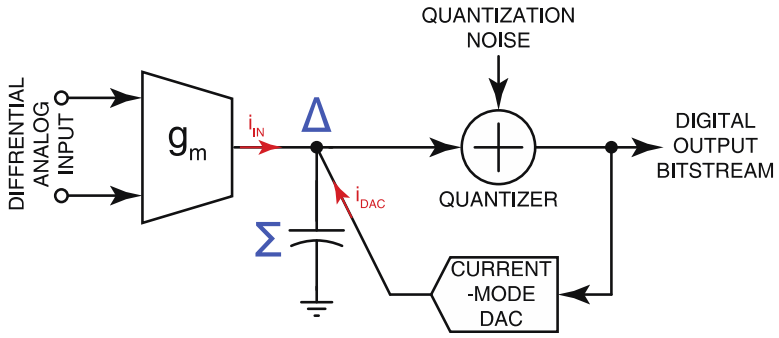

Figure 2.4 Proposed architecture for the high DR recording channel.

2.2 Proposed Channel's Operation in the "Recording Mode"

Figure 2.5 shows the fully differential implementation of the proposed architecture. As shown, the 1-bit quantizer is implemented using a simple voltage comparator, and the 1-bit current-mode DAC is modeled with ideal current sources that can push/pull current into the integrating capacitor, depending on the digital output of the comparator (i.e., 0 or 1). To evaluate the functionality of this circuit and to model how it fails during a stimulation episode, we have modeled all the above blocks in MATLAB. The real circuit implementation will be discussed in the next chapter.

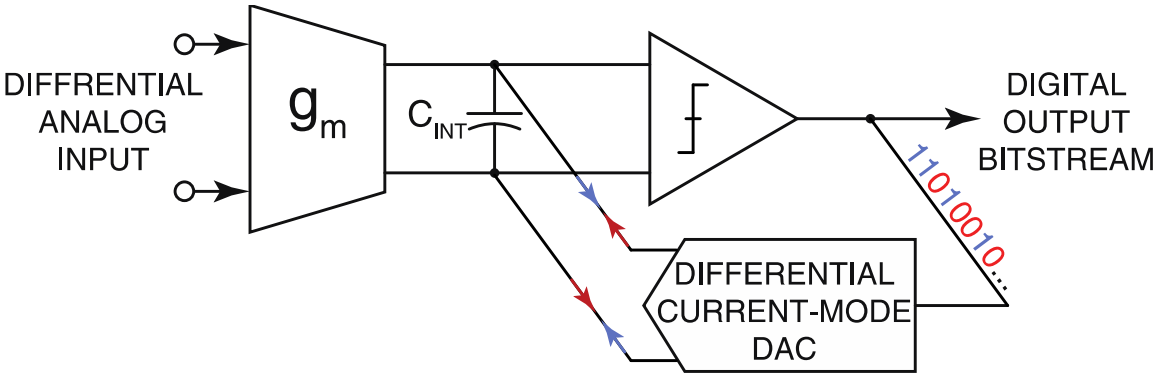

Figure 2.5 Fully differential implementation of the proposed channel.

During the "normal recording" mode, it is assumed that no artifact or offset are present; hence, the input voltages remain in the small-signal range. The G_m-stage continuously translates differential input voltage into a differential current. which will be integrated on the capacitor. At the same time, during each clock cycle, the current DAC injects a pre-determined amount of current with a direction (i.e., push or pull) that depends on the previous output of the comparator. The DAC's current magnitude is slightly greater than the highest possible output current of the G_m-stage, which is associated with the largest input neural signal (e.g., 1 mV). Therefore, it is capable of changing the capacitor polarity, a condition required for the ΔΣ modulator to function correctly. The circuit shown in Figure 2.5 is implemented and simulated in MATLAB for a 1 mV_{pp} 1.3 kHz test input signal. The clock frequency for the comparator is set to 1 MHz to implement an OSR of 100. The output bitstream and a filtered decimated reconstruction of it are presented in Figure 2.6. Figure 2.7 shows PSD of the output bitstream and confirms the 1st-order noise shaping. SQNR of 61.43 dB is achieved that translates into 9.91 ENoB.

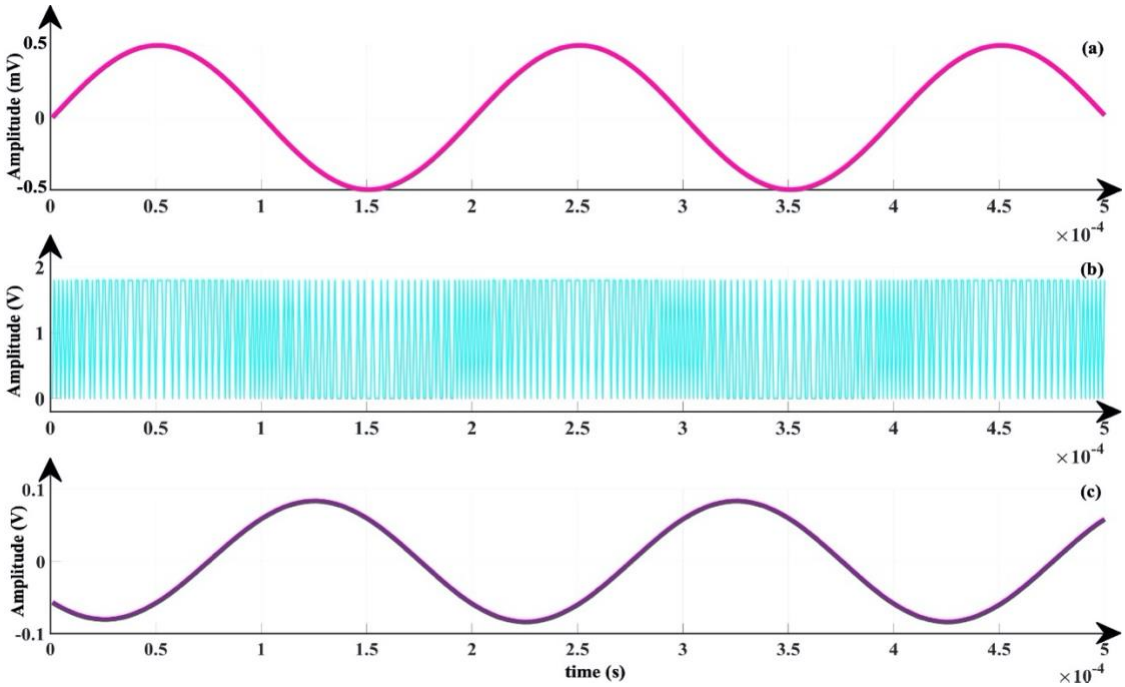

Figure 2.6 (a) The input Signal (b) Output Bitstream (c) Reconstructed Input.

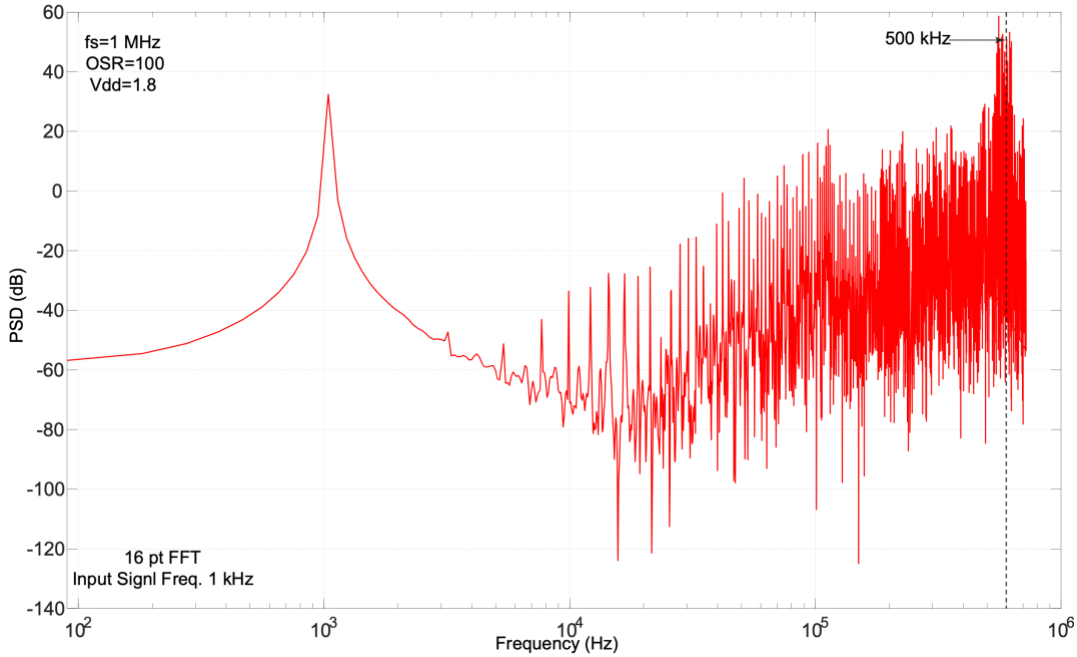

Figure 2.7 Power spectral density plot of the output bitstream showing the signal to noise and noise shaping of the presented ΔΣ modulator.

2.3 Proposed Channel's Operation in the "Artifact Recovery Mode"

In the case of an artifact or DC offset, a large (i.e., > 100mV) differential signal will appear at the input. Such a large signal creates a proportional imbalance in the G_m-stage by changing its biasing condition. As a result, a large positive or negative (depending on the polarity of the input offset/artifact) current will be injected into the integrating capacitor, which is orders of magnitude larger than the current generated by the 1-bit current DAC. In addition, the imbalanced biasing of the G_m-stage will result in a substantial decrease in the circuit's transconductance, causing further disproportion between the input signal and the digital output.

Figure 2.8 shows the second feedback path added to the core recording circuit to address the above-described issues. The main idea here is to monitor the comparator's output to detect bit-stream patterns that indicate the existence of a large differential artifact/offset at the input. Upon detection, the integration capacitor and the 1-bit current DAC are switched out of the circuit, and the G_m-stage, comparator, and a SAR DAC collectively form a SAR ADC that is used to estimate the magnitude of the offset.

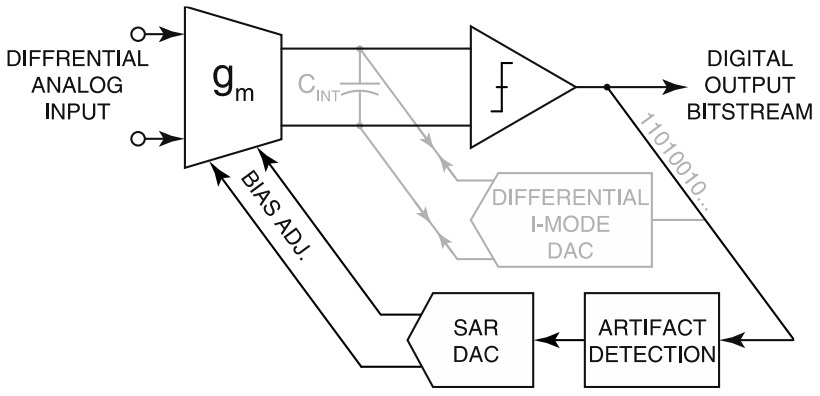

Figure 2.8 The proposed architecture operating in the artifact recovery mode.

The idea here is that based on the comparator's output, the SAR DAC starts a binary search by adjusting the G_m-stage biasing in a successive manner, which means that after every adjustment the new comparator output indicates that if the next adjustment should be continued in the same direction or the opposite one. The magnitude of adjustments is decreased by a factor of x2 at every step (hence, the binary search). Therefore, after N steps, the magnitude of the imbalance is shrunk by a factor of 2^N. For example, the imbalance caused by an offset equal to 256 mV could be theoretically reduced to less than 1 mV after 8 steps. The residual imbalance will be small enough that if the circuit goes back to the normal recording mode, the 1-bit current DACs will be able to handle it.

Based on this, an 11-bit DAC was used to perform the imbalance approximation and compensation. The number of bits is more than the theoretical value to account for ENoB reduction due to the nose and non-idealities. This operation requires 12 clock cycles (e.g., 120 µsec for f_{clk}=100 kHz), which is a very short time compared to the slowly varying neural signals. More importantly, since the source of imbalance is a large differential signal that is created due to an offset (constant) or a stimulation artifact (stimulation frequency is typically <10 Hz), it can be assumed that the imbalance magnitude is constant over the period that the SAR is operating.

Once the imbalance is compensated, SAR control will be disabled, and the 1-bit DACs, and the integration capacitor will be connected while the effect of the large differential voltage is removed, and the system goes back to its normal mode. Figure 2.9 (a) shows an example scenario where the input signal to the presented circuit is a combination

of a 1 mV_{pp} 1.3 kHz sinusoidal representing the neural signal as well as a 150 mV_{pp} square wave representing the large differential artifacts. Figure 2.9 (b) shows the digital output that is reconstructed from the comparator's bitstream. SQNR of this mode is the same as the "normal mode" because the MATLAB model is ideal. It should be noted that the dc level change of the reconstructed signal is caused by the consecutive 1s before the artifact detection and the value does not represent the artifact. In order to extract the artifact voltage, SAR DAC digital output can be used.

An important advantage of the presented circuit is that its SNR can be increased dynamically by increasing the clock frequency (effectively, the OSR), of course at cost of increasing the dynamic power consumption.

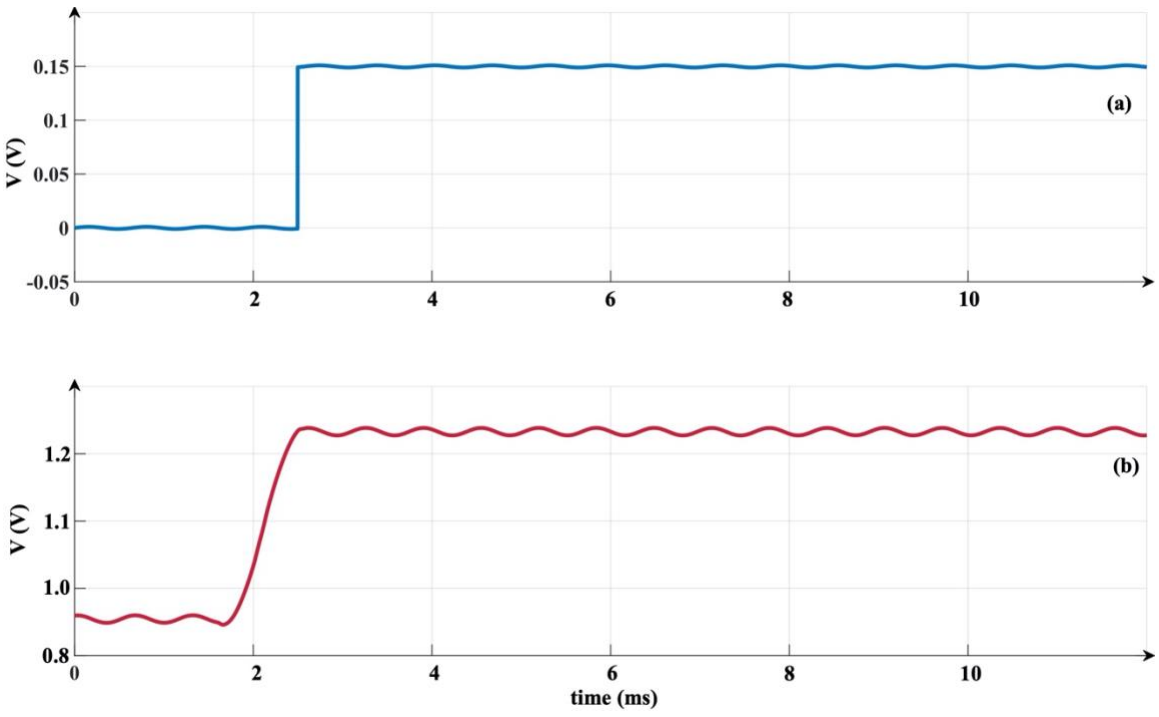

Figure 2.9 System-level simulation results of the presented channel for recording small signals in the presence of a large differential-mode artifact (a) Input signal (b) Reconstructed Signal.

Chapter 3

Circuit-Level Design and Implementation of a 94 dB Dynamic Range Dual-Loop SAR-Assisted Recording and Stimulation Channel

As fully described in the previous chapter, Figure 3.1 depicts the top-level block diagram for the proposed neural recording channel architecture. The MATLAB-based model presented in the last chapter has is used ideal blocks. Hence, performance metrics such as power, non-linearity, and noise were not considered. These nonidealities could significantly affect the performance to the point that they might disrupt the system functionality. In this chapter, the circuit-level design and implementation of each block will be presented and related nonidealities will be discussed.

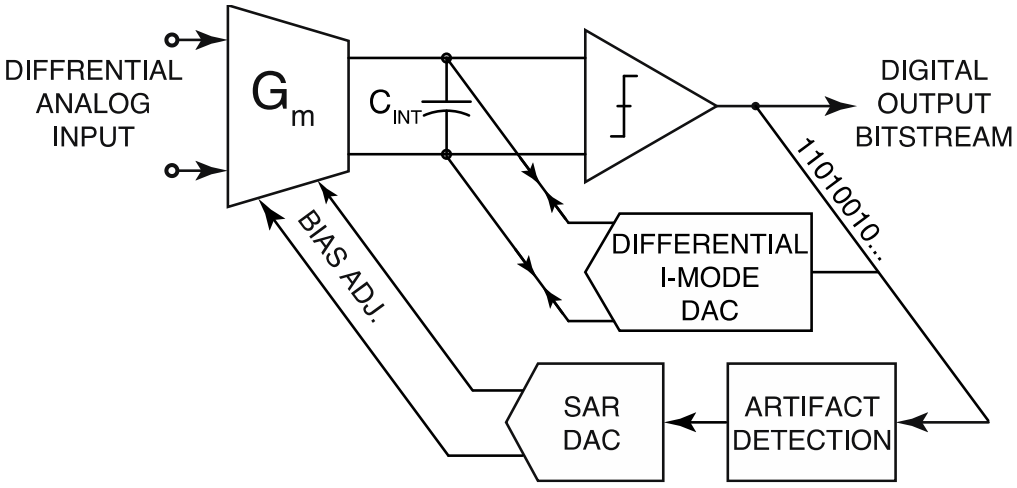

Figure 3.1 Block diagram of the proposed neural recording architecture.

3.1 The Transconductance (G_m) Stage

As mentioned in the previous chapters, since an ADC-direct architecture was adopted in this work, the first stage of the ADC, i.e., the G_m-stage, will be directly connected to the recording electrodes. As such, it must satisfy the design requirements of a neural front-end in terms of IRN, input impedance, immunity to offset and artifacts, and sufficient signal amplification gain.

The IRN of the channel is mainly determined by the noise of the G_m-stage Both thermal (constant over the entire frequency spectrum) and flicker noise (inverse relationship with frequency, also called 1/f noise) sources are present in the frequency range of interest (i.e., DC - 5kHz). Regardless of their type, reducing the noise level has an inverse relationship with power consumption. Hence, the lower limit for the required IRN needs to be determined. The picked-up background noise of neural recording electrodes is

commonly-accepted to be around 10 μV in the bandwidth of interest [33]. The recording circuit should be designed in a way that its noise contribution at the input does not add more than 10% to this number. The total noise of the system is equal to Equation 3.1.

$$\boldsymbol{n_{Total} = \sqrt{n_{Electrode}^2 + n_{Gm-stage}^2}} \quad \textbf{(3.1)}$$

Where n_{Total} is the total noise of the system, $n_{Electrode}$ is the background noise picked-up by neural recording electrodes and $n_{Gm\text{-}stage}$ is the IRN of the G_m-stage. It should be noted that all the noises are rms values in 5 kHz bandwidth. According to this equation, IRN of the G_m-stage should be limited to 4.5 μV.

Reducing thermal noise can be done by careful choice of the transistors' bias point, to ensure the key contributing devices are biased at their minimal noise current density as will be explained later in this chapter. The other type is flicker noise, which is dominant in low frequencies. Flicker noise can be reduced to some extent by increasing transistors size. However, this method has a limited success and more importantly, is not area-efficient, as reducing 20 dB of flicker noise spectral density means increasing the area by a factor of 100 [25]. Such an area-inefficient design is not acceptable and becomes a bottleneck in scaling the number of channels integrated on the implantable chip. The other well-established method is using the chopper-stabilization technique. In this technique, the input signal will be upconverted to a high frequency (i.e., outside of the neural signal spectrum) where flicker noise is several orders of magnitude smaller (due to its 1/f behaviour), in amplifier, and then downconverted to the neural band at the output of the amplifier, as depicted in Figure 3.2. In the presented architecture, this technique is employed.

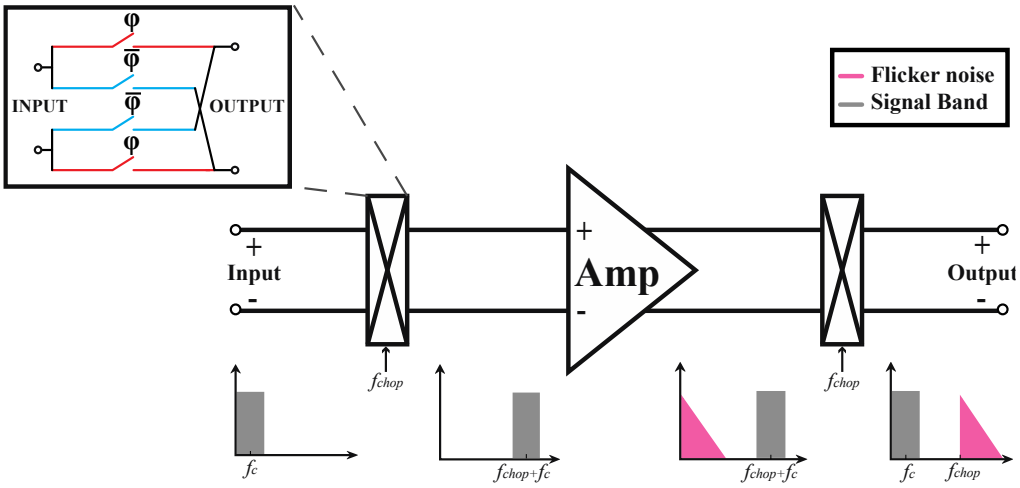

Figure 3.2 Conceptual representation of the chopper stabilization technique.

As shown, chopping is performed using two pairs of cross coupled switches that change the polarity of the differential input to the amplifier at a high frequency called chopping frequency. For half of the chopping frequency cycle the amplifier inputs are coupled to the electrodes in a direct way (φ) and for the other half, in a crossed way ($\bar{\varphi}$). A copy of these switches is repeated at the output to down-convert the chopped signal, also called unchopping. Since these switches are directly connected to the electrode, their effect on input impedance and signal to noise ratio must be considered. If these switches are used in series with an input capacitor as shown in Figure 3.3 (typically used for DC offset decoupling as described in chapter 1), they form a switched capacitor circuit with an equivalent impedance of $1/(f_{chop} .C)$, where f_{chop} is the chopping frequency and C is the input capacitor. This impedance will be the input impedance (Z_{in}) of the neural front-end, which leads to an impractical maximum for the chopping frequency if we need to realize an acceptable Z_{in} (e.g., >100M Ω). This incompatibility with chopper stabilization is indeed

one of the main challenges of AC-coupled amplifiers, which has motivated for a DC-coupled (i.e., capacitor-less) front-end architecture. For the same rationale, direct-ADC architectures that implement the summation node using a capacitive method at the input node (e.g., [12]) will have the same issue with realizing a high input impedance. In order to address this issue, some designs in the literature have employed impedance boosting positive feedback loops [29]. However, these loops increase the power consumption and their boosting factor is not constant in all the input range.

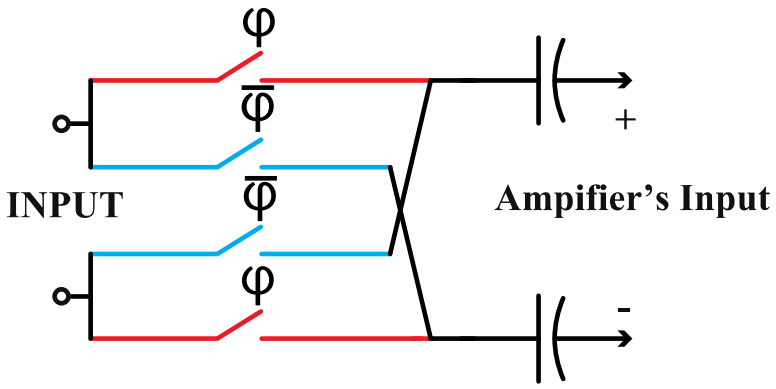

Figure 3.3 Input of an AC-couples amplifier with chopper.

A high capacitance at the chopping nodes of the circuit also increases the time constant of those nodes, hence, limits how high-frequency the chopping could be performed without leaving high-frequency residual fluctuations on the neural signal (called ripples) after unchopping at the output.

None of the above would be an issue of the chopping switches are directly connected to the gate of the input transistors of the G_m-stage, without any other capacitance being present at the input node. Of course, this means that the large DC offset at the input should be removed in a different way than capacitive coupling, and also the summation

point of the ΔΣ ADC cannot be at the input. Both of these are addressed in the proposed channel architecture as will be presented next. The chopping frequency should be chosen by considering noise corner frequency (i.e., the frequency above which, the flicker noise become insignificant compared to the thermal noise), ripple (i.e., the high-frequency residue on the neural signal at the output of the amplifier that is due to the high-frequency switching needed for chopper stabilization), and power consumption [34]. The higher is the chopping frequency, the lower will be the ripple and the noise [34]. However, the dynamic power consumption of the chopper switches will increase, and the input impedance will be reduced.

The other constraint for the G_m-stage is the range of input signal amplitude and common-mode variations that it can handle without getting saturated or perform non-linearly. Both common-mode artifacts, which change the CM of the input signals, and differential-mode artifacts which cause a large differential voltage between the differential inputs, are problematic for the G_m-stage Even if a very small gain is chosen for this stage to avoid output saturation (which comes at cost of increasing the IRN due to next stage noise contributions) these artifacts could easily change the biasing point of the circuit, hence, cause large variations in the transconductance (G_m), which leads to significant nonlinearity in the recorded signal. The other challenge is EDO, which is a large DC offset between the differential inputs and has the same effect as the differential artifacts.

All of the above should be realized with the minimal power consumption and active area to allow for massive on-chip integration (e.g., >1000 channels) of these recording

circuits while meeting the extremely-constrained size and energy budgets of a brain-implantable device.

3.1.1 Highly-linear Artifact Tolerant G_m-Stage Implementation

The first step toward achieving all of the above goals is the best architecture for the G_m. Figure 3.4 shows a rail-to-rail input folded-cascode operational transconductance amplifier (OTA) which is one of the most popular architectures used in the neural recording front-ends. Both NMOS and PMOS differential pairs are used for the input stage as the circuit is supposed to be DC-coupled to the recording electrodes, hence, should be able to amplify input signals with a wide range of DC levels.

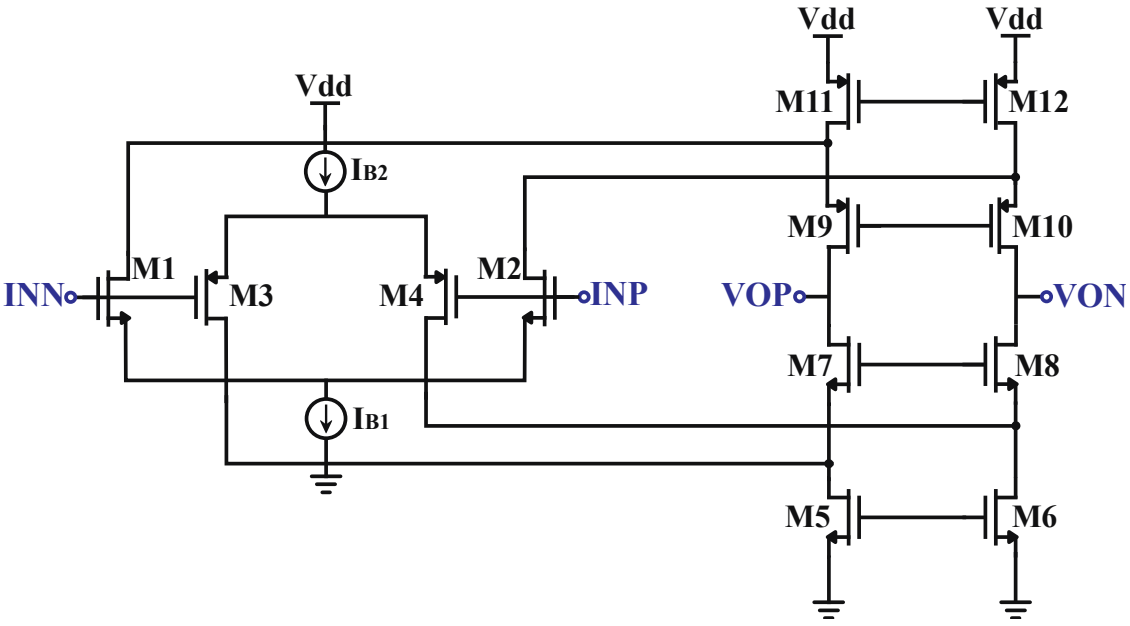

Figure 3.4 Folded-cascode transconductance amplifier.

The inputs are connected to the gate of MOS devices; hence, a high Z_{in} is expected. The isolation of input and output stages in this OTA allows for optimizing the input devices

for noise and output devices for gain. Also, the differential architecture ensures a high CMRR. Nevertheless, in order to determine if the architecture is suitable for simultaneous recording and stimulation, CM and DM artifacts without sacrificing the performance in terms of any of the above metrics should be investigated. Particularly, we will look into how the system-level idea presented in Chapter 2 (i.e., dynamic biasing imbalance adjustment) Folded cascode OTA's G_m depends on the input differential pair and is equal to Equation 3.2.

$$G_m = \frac{2I_{B1}/2}{V_{GS1,2}-V_{Tn}} + \frac{2I_{B2/2}}{V_{GS3,4}-|V_{Tp}|} \quad \textbf{(3.2)}$$

where, I_{B1} and I_{B2} are the tail bias current of NMOS and PMOS pairs respectively, and V_{Tn} and V_{Tp} are the threshold voltage of NMOS and PMOS transistors respectively. Based on this equation, when the common-mode voltage of the inputs increases, the V_{GS} of the NMOS pair resulting in a g_m decrease for these transistors. The same will happen for PMOS transistors in low input CM variations at the input due to stimulation artifacts or electrode-cell chemical interactions. Therefore, both PMOS and NMOS input pairs are required to tolerate the CM artifacts. In this scenario, for higher CM ranges, only the PMOS pair works and in lower CM voltages only the NMOS pair generate the current. In the mid-range both NMOS and PMOS pairs are active and contribute into the overall G_m. Having three different regions of operation (i.e., PMOS only, NMOS only, NMOS-PMOS cooperation), to avoid a nonlinearly amplified output, a careful design is required to ensure the overall G_m does not vary with input CM variations. This is generally done, with an

acceptable level of success, by proper biasing and size adjustments of the NMOS and PMOS pairs (i.e., I_{B1} and I_{B2} as well as W/L of $M_{1\text{-}4}$).

On the other hand, when large a DM artifact (or offset) is present at the amplifier, the mentioned method is not helpful because the V_{GS} of same-type devices (NMOS or PMOS) are different from each other, resulting a large asymmetry in the circuit's biasing. The MOSFETs g_m's sensitivity to this asymmetric biasing mainly depends on how close their $|V_{GS}|$ is from their $|V_{TH}|$. Figure 3.5 shows the $|I_D|$ and g_m of M1 and M3 versus the differential input voltage (i.e., INN-INP) while assuming the input CM is constant and biased at the midrange (i.e., VDD/2).

As shown in this figure, very high or very low $|VIN_{DIFF}|$ values drive the transistor to the triode or off regions, respectively, hence, resulting in reducing the device's small-signal transconductance to zero (i.e., the flat regions). Even before the curves are flatten out, their slope starts to decrease gradually, which indicates the device's g_m degradation. Comparing the two subfigures shows that increasing the transistors' overdrive voltage ($V_{OD}= |V_{GS}|-|V_{TH}|$) will result in widening the linear-g_m region in the center of the plot, hence, decreasing the overall G_m's sensitivity to asymmetric biasing. Of course, this comes at the cost of reducing the transconductance gain, which has the side effect of degrading the IRN as well. Therefore, the input stage was biased as a trade-off between the G_m and linearity.

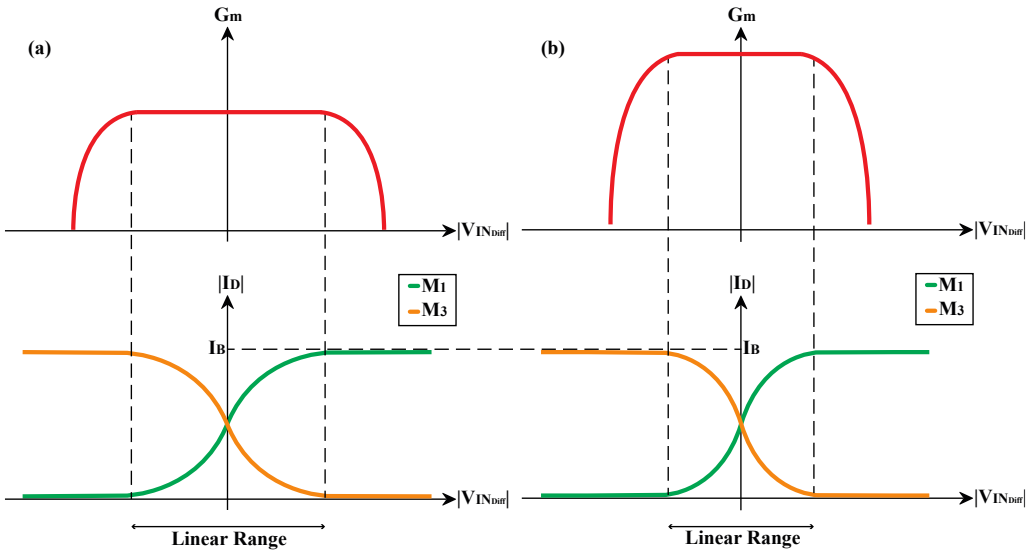

Figure 3.5 I_D and G_m vs. VIN_{Diff} for folded-cascode input transistors. (a) Large V_{OD} is chosen for input transistor. (b) Small V_{OD} is chosen for input transistor.

To minimize the thermal noise, g_m of M5, M6, M11, and M12 should be much smaller than input transistors, meaning that V_{OD} of them should be maximum. Also, it should be considered that these transistors are current sources, and their L should be large enough to yield a large output impedance needed for a relatively constant current. Table 3.1 lists the sizing information for G_m-stage transistors, and Table 3.2 summarizes the amplifier's performance parameters.

Table 3.1:Transistor sizing of the folded-cascode

Transistor	*Width*	*Length*	*Bias Current*
M1, M2	250 nm	16.28 µm	300 nA
M3, M4	250 nm	4.11 µm	300 nA
M5, M6	655 nm	10 µm	600 nA
M7, M8	250 nm	2 µm	300 nA
M9, M10	3.57 µm	4 µm	300 nA
M11, M12	1.69 µm	6 µm	600 nA

In Figure 3.6, the total G_m of the designed folded-cascode is shown. As shown, for a differential input range of [-200mV, 200mV], the G_m varies by 21%, which is unacceptable as it leads to nonlinear amplification of neural signals. As discussed above, reducing this 21% variations can only be done by an extreme increase of transistors V_{OD}, which comes at the cost of making the transconductance gain (G_m) too small to the level that the circuit might attenuate the signal rather that amplifying it. The only way to achieve high linearity while maintaining a high G_m is to increase the total bias current of the input stage, which cannot be done without violating the power budget allocated to a single neural recording channel.

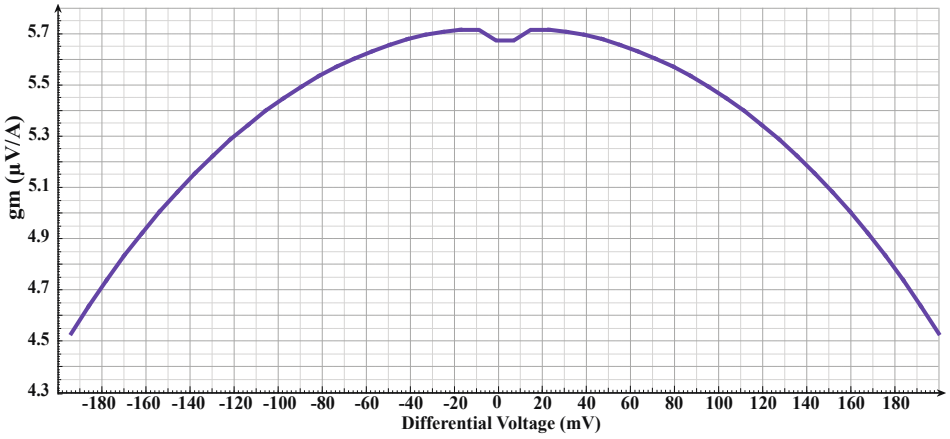

Figure 3.6 G_m of the folded-cascode vs. differential input voltage

Table 3.2:Folded-cascode transconductance amplifier's parameters

Parameters	*G_m Variation (400 mV input range)*	*Power (µW)*	*Thermal Noise level of the G_m (nV/√Hz)*
Value	20 %	3.06	200 @ 30 kHz

This G_m-variation is related to input transistors because those transistors produce the current difference and the second stage does not affect the produced current. Therefore, in order to prevent G_m variation in the presence of unbalanced inputs, a feedback should be applied to the input stage, to increase the total bias current of both NMOS and PMOS pairs. However, this leads to a much higher power consumption when artifacts or offset are presents. Additionally, the virtual ground node voltage was also changing significantly due to the this differential voltage, making it impossible to bring the circuit back to normal.

In this work, we propose a resistor-based recording front-end architecture, shown in Figure 3.7, to address the issue of G_m variations [35]. In this architecture the input currents can be adjusted in a way that keep the total power consumption constant and bring back the G_m to its original value when artifacts are present.

As shown, M1 and M2 are input transistors, connected as source follower voltage buffers to copy input voltages to X and Y. Then the voltage difference will be converted to $I_{in,diff}$. This conversion is done in a purely linear way, thanks to Ohm's law done by R_s ($I_{in,diff}=V_{in,diff}/R_s$). Depending on the differential input polarity, this current is added/subtracted from the DC bias currents (I_{Bp} and I_{Bin} in Figure 3.7) generated by the PMOS current sources (M3,4) and NMOS current sources (M5,6). The bias current in M11 and M12 are set to be exactly equal to the difference between I_{BP} and I_{Bin}. This way, the current passed to the second stage of the OTA is exactly equal to the small-signal current $i_{in,diff}$. This small-signal current then travels through the second stage to the output nodes where it is multiplied by the large output resistance of M13,15 (or M14,16).

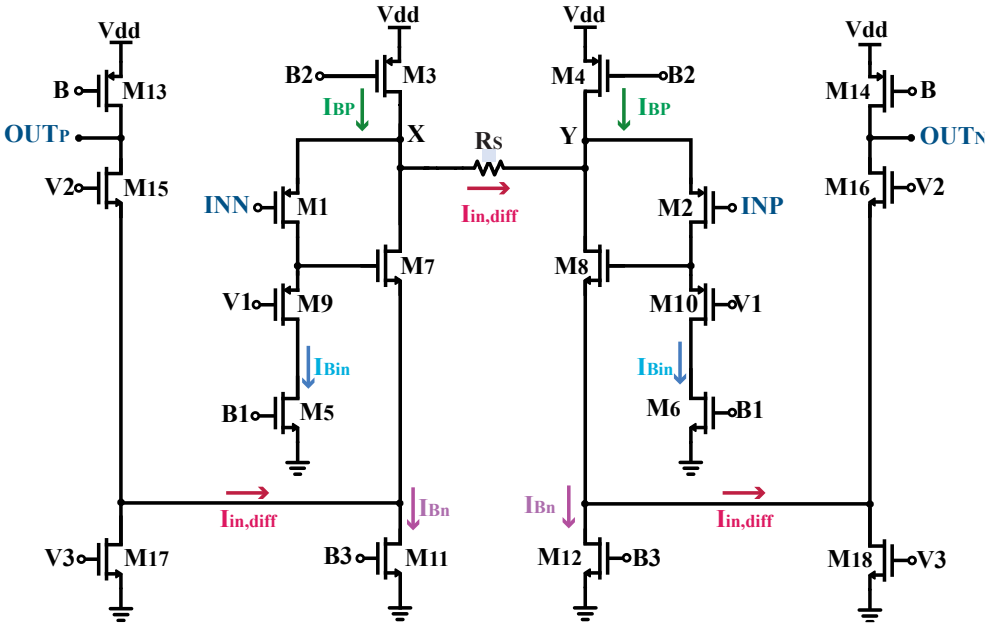

Figure 3.7 The propose resistor-based G_m-stage architecture.

Since voltage to current conversion is done by a resistor the only nonlinearity that can be added is the gain variation of the input buffers. The gain of the source follower voltage buffer is equal to Equation 3.3. According to this equation as long as $g_{m1,2}R_s$ is much larger than 1, the buffers work perfectly and do not introduce any nonlinearity to the G_m. This is one of the advantages of the proposed G_m-stage comparing with folded-cascode. As shown in Equation 3.2, the total G_m of the folded-cascode is the summation of input transistor's g_m. Therefore, any change in their g_m will be translated to a nonlinearity but in Equation 3.4 g_m of transistors is appeared in both the numerator and the denominator, hence the sensitivity to g_m of transistors is reduced.

$$A_V = \frac{g_{m1,2}R_s}{1+g_mR_s} \tag{3.3}$$

$$G_m = \frac{A_V}{R} = \frac{g_{m1,2}R_s}{1+g_mR_s} \times \frac{1}{R_s} \tag{3.4}$$

Choosing the bias of transistors is crucial because it determines the noise, power consumption, and linearity range. Therefore, it will be explained in detail in the next section.

Choosing Bias for G_m-stage Transistors

The IRN of the G_m-stage is equal to Equation 3.5. This equation should be considered for all the transistors biasing.

According to this equation increasing the $g_{m1,2}$ reduces the noise. Additionally, increasing the g_m of them is helpful in terms of linearity according to Equation 3.4.

It should be noted that as chopper will be added to the input parasitic capacitor should be small to keep the input impedance large. Therefore, the sizing should be small.

M3 and M4 are the primary current sources, and their L should be maximum to have a constant current. According to Equation 3.5, the $g_{m3,4}$ should be smaller than inputs. The current of M3 and M4 are larger than M1 and M2 in this circuit leading to larger g_m in order to reduce the current difference between M1,2 and M3,2 I_{Bn} is chosen 2% of I_{BP}. Also, V_{OD} of M3,4 are chosen large.

The same strategy is applied for M11, M12. However, since the current of these transistors are much smaller than the input the noise contribution of them is less significant.

M5,6 and M9,10 have the same current as the input transistors. Therefore, reducing their g_m is done by choosing large V_{OD}.

The noise contribution of the R_s only depends on $g_{m1,2}$ because the value of it determines the G_m of the amplifier.

$$\overline{V_{nt}^2} = 8KT\gamma\left(\frac{1}{g_{m1,2}} + \frac{g_{m3,4}}{g_{m1,2}^2} + \frac{g_{m5,6}}{g_{m1,2}^2} + \frac{g_{m11,12}}{g_{m1,2}^2}\right) + \frac{4KT}{g_{m1,2}^2 R_S} \quad \textbf{(3.5)}$$

The output stage noise contribution is not considered because the voltage gain of the first stage is large (~60). The main criteria in sizing the output stage transistors is to ensure a high output impedance for the OTA.

Figure 3.8 shows the generated current on the resistors for 3 different CM voltages. It should be noted that the linear CM range is smaller than the folded-cascode. However, in this circuit unlike the folded-cascode which had both PMOS and NMOS pairs, only PMOS pair is used.

The G_m drop in this circuited is resulted from the primary current sources. As mentioned, overdrive voltage of M3 and M4 are large to limit their noise contribution. However, with this choice of biasing, the current variation will be increased. When CM level increases, the drain voltage of M3 and M4 will be increased and since the $|V_{GS}|$ is large, their current decreases leading to G_m loss.

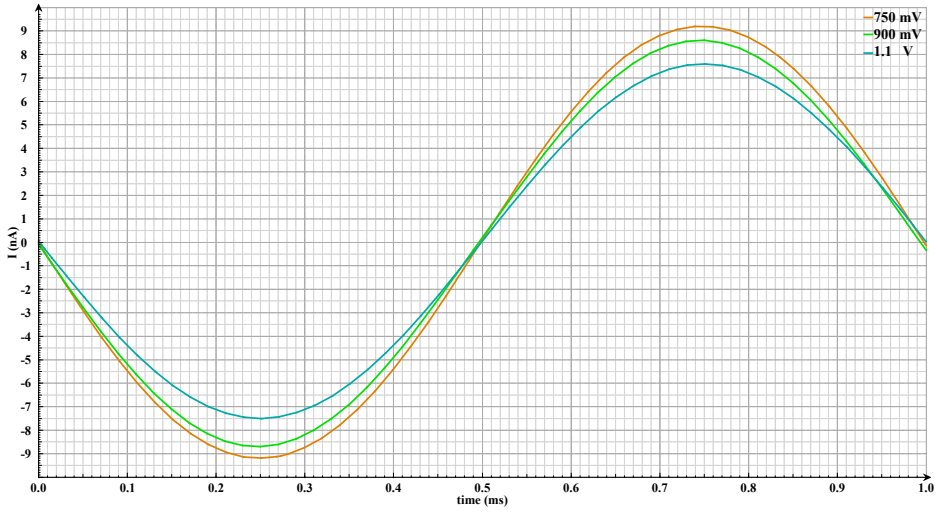

Figure 3.8 I_{INdiff} for different CM levels applied at the input of the proposed channel.

G_m variation for Different CM Values lists G_m variation of the presented G_m-stage for different CM levels. As seen, this variation is smaller than 10% without noise penalty and adding an NMOS pair. It should be noted that the linear CM range of this G_m-stage (300 mV) is smaller than the folded-cascode (400 mV) but this G_m-stage will provide a superior linearity in the case of DM artifact which will be discussed later in this chapter.

Table 3.3 G_m variation for Different CM Values

CM Artifact (mV)	$g_{m\ (\mu A/V)}$
150	7.97
0	8.85
-100	9.37
-200	9.38

Considering all the requirements, Table 3.4 lists the sizing information and current of resistor-based G_m-stage transistor.

Table 3.4:Transistor sizing for the resistor-based G_m-stage

Transistor	*W*	*L*	*I*
M1, M2	64.74 µm	5.0 µm	3.9 µA
M3, M4	37.085 µm	19.995 µm	4 µA
M5, M6	4.245 µm	19.995 µm	2.1 µA
M7, M8	3.665 µm	19.995 µm	1.8 µA
M9, M10	64.74 µm	5.0 µm	3.9 µA
M11, M12	770.0 nm	19.995 µm	100 nA
M13, M14	970 .0 nm	5.0 µm	200 nA
M15, M16	385.0 nm	1.0 µm	200 nA
M17, M18	865.0 nm	5.0 µm	200 nA

It should be noted that the presented the G_m of the presented amplifier varies in case of a DM artifact. The SAR-assisted feedback (described in Chapter 2) needs to be added as will be described in 1.1.3.

3.1.2 G_m-stage Performance

Figure 3.9 shows the gain-bandwidth plot for the proposed highly-linear OTA. The required bandwidth for this stage is 5 kHz. Here, a 3-dB bandwidth of 8.3 kHz is achieved. In order to calculate the bandwidth, the maximum gain is divided by √2 and the frequency for this gain is considered as the bandwidth.

Figure 3.10 shows the IRN of the G_m-stage. The noise corner is about 30 kHz. Therefore, the chopping frequency of 32 kHz is chosen, and a noise level of 55 nV/√ Hz is achieved. This noise level is without chopping. However, only the thermal noise is considered because the chopping frequency is higher than the corner frequency of the circuit and the noise PSD plot will be flat (as described in 1.1). This should be validated in experimental results because it could not be confirmed using simulations due to the switching.

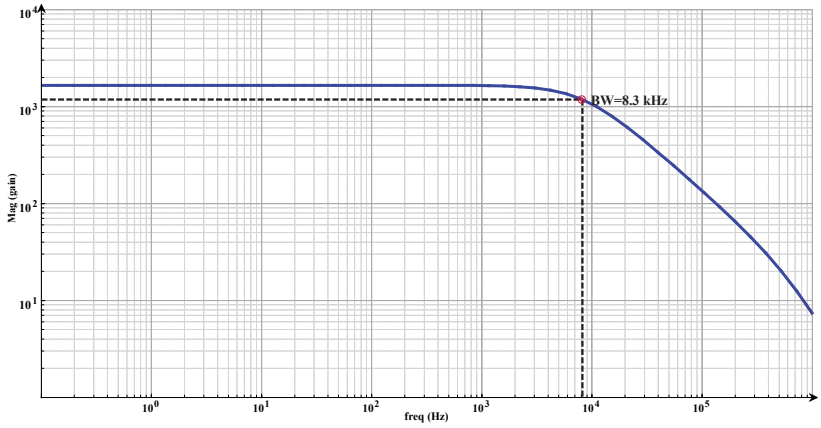

Figure 3.9 Gain-bandwidth plot for the proposed highly-linear OTA

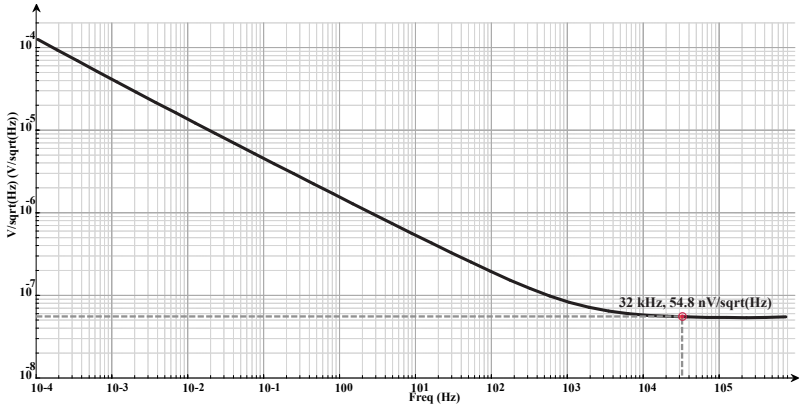

Figure 3.10 Power spectral density of the IRN of the proposed highly-linear OTA

The OTA's continuous power consumption is 15.12 µW, and IRN is 3.88 µV in 5 kHz bandwidth. To further reduce the power consumption, the first stage of the OTA, which is responsible for more than 95% of the total power is power-cycled. As shown in Figure 3.11, three sets of switches are used to turn off the current in the first stages as well as the connection between the first and second stages. The separation of the two stages ensures that the OTA's output stage bias and output impedance remain intact, hence the G_m-C integrator's capacitance will not experience any DC level change. The timing of

these switches needs to precisely set to ensure that the stage isolation is performed before turning off the first stage, in order to prevent any unintended charge injection into the output stage. The power cycling is performed with a 90-10 ratio, in which the OTA is only operational in 10% of the time. Of course, this reduces the average transconductance (G_m) that the OTA delivers to the integrating capacitor, which is acceptable given the high value of the original G_m. In 90% of the time, S1 and S2 are on (turning off M3 and M4), and the rest of switches are off (isolating the two stages from each other), and for 10% of the time the circuit goes back to normal operation (i.e., similar to the schematic in Figure 3.7). As a result of this power cycling scheme, the power consumption is reduced approximately by a factor of 10 (not exactly, mainly because the OTA's second stage is always ON), while the IRN does not increase significantly since the first stage is completely disconnected from the second stage when the current sources are off; hence, any random fluctuations in the first stage is never reaches the output.

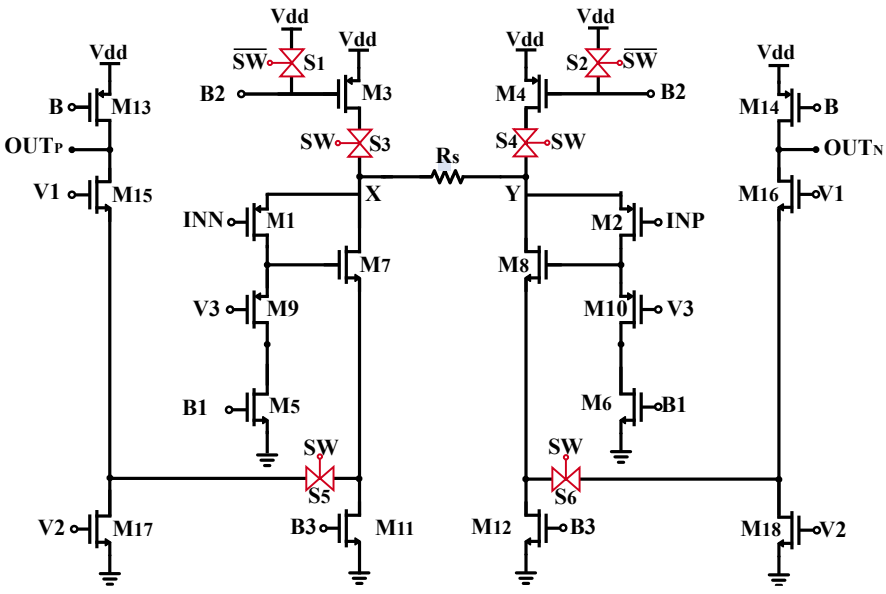

Figure 3.11 The proposed configuration for power-cycling of the presented Gm stage.

Table 3.5 Lists the parameters of the suggested G_m-stage and Table 3.6 lists input impedance of the integrator for different input frequencies.

Table 3.5:G_m-Stage parameters

Parameters	*IRN (V_{rms})*	*Bandwidth (Hz)*	*Power (W)*	*CMRR (dB)*	*G_m Variation*
Value	1.22 µ[a]	5 k	4.6 µ	93.6	<10%[b]

[a] integrated noise in 1 Hz- 500 Hz
[b] for 300 mV input range

Table 3.6 Input Impedance vs. input signal frequency

Frequency (Hz)	*DC*	*10*	*1 k*
Input Impedance (Ω)	7.5 G	7.1 G	1.8 G

As expected from Figure 3.7 and the gain of the amplifier shown in Figure 3.9, the output impedance of this amplifier is very large, and the structure is differential. Therefore, common-mode feedback should be applied to keep the output dc level at $V_{DD}/2$ to avoid DC drifts at the terminals of the integrating capacitor. Figure 3.12 depicts the CMFB circuit. This circuit is biased with only 20 nA. C_C capacitors are added for compensation. In order to get phase margin of 40º, CMFB capacitors (C_C) are chosen 50 fF.

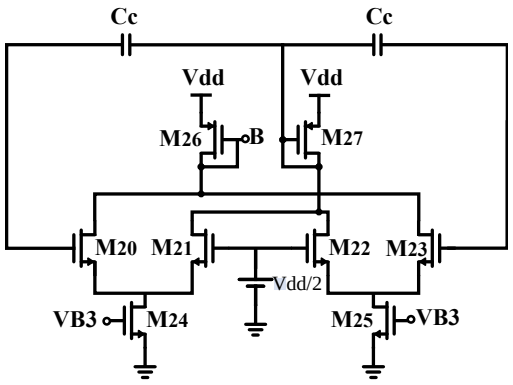

Figure 3.12 CMFB circuit

Table 3.7 lists the sizing information and current bias of the CMFB.

Table 3.7:Sizing information and current biases of CMFB.

Transistors	*Width*	*Length*	*Bias Current*
M26, M27	335 nm	19.995 µm	20 nA
M20, M21, M22, M23	735 nm	19.995 µm	10 nA
M24, M35	515 nm	19.995 µm	20 nA

3.2 Gm-C Integrator Implementation

The designed G_m-stage needs a capacitor to work as the ΔΣ integrator. This capacitor should be sized in a way that the integrating node's time constant is large enough to accumulate a large number of data (comparator's output) that are at the oversampling rate (typically, ~1 µsec). 200 clock cycles (2×OSR) are required for each sample to be digitized. Hence, the time required for keeping 200 samples is 200 µsec (200×1 µsec). If we want to keep 10 consecutive samples, we need 2 msec (200 µsec×10). Therefore, the dominant pole should be smaller than 1 kHz. Hence, considering the R_{out} of the OTA (530 MΩ) a 1 pF capacitor is used. Figure 3.13 shows the gain-bandwidth plot of the integrator illustrating its integrating behaviour at frequencies larger than 300 Hz, and its phase margin, confirming its stability. The stability can also be confirmed using gain margin. This gain can be obtained by finding the magnitude of the transfer function where the phase is 180°. According to Figure 3.13 the gain margin for this circuit is about -20 dB and since it is less than 0, it shows the stability.

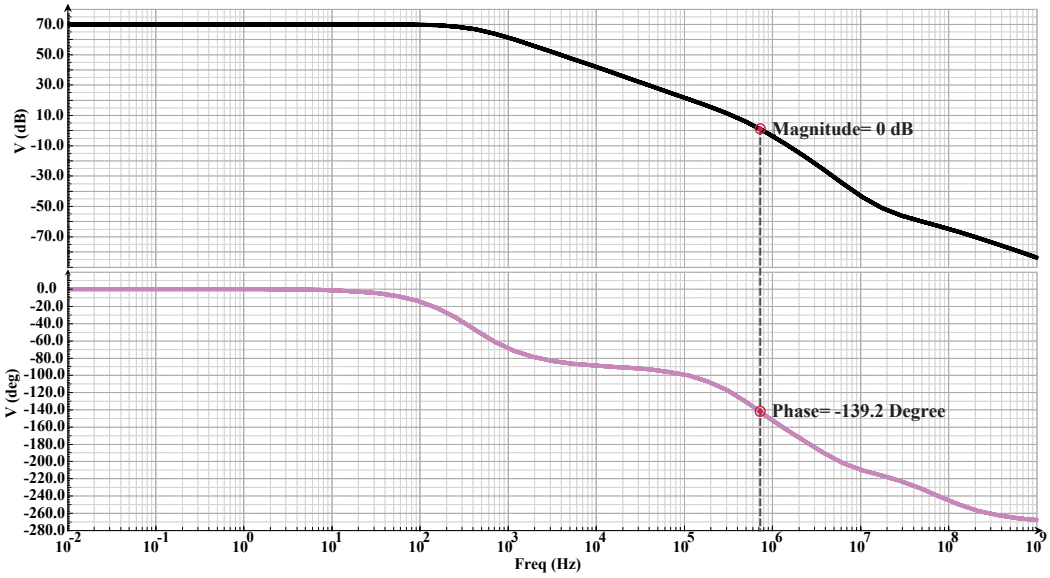

Figure 3.13 The gain-bandwidth plot of the proposed Gm-C integrator.

As mentioned, the chopper should also be added to the integrator to suppress flicker noise. Adding the unchopping switches at the output of the integrator's first stage where there is no capacitor and removing the input capacitors eliminate the possibility of fold-back noise [25]. Figure 3.14 Depicts the full G_m-C integrator schematic, including its CMFB circuit and chopper stabilization switches.

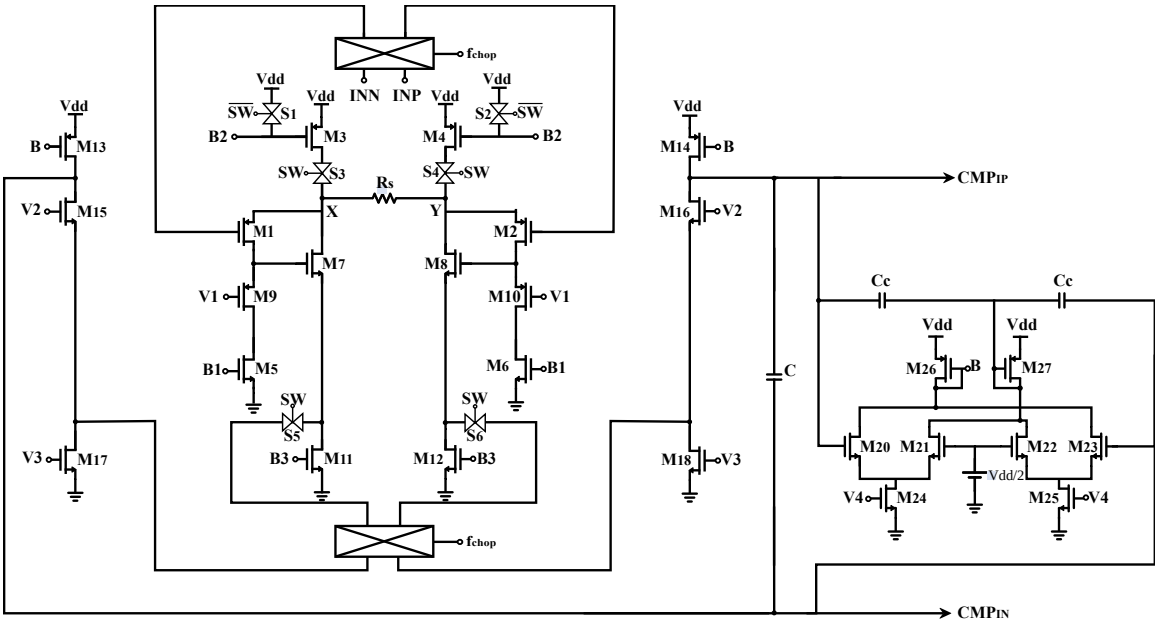

Figure 3.14 Full Gm-C integrator schematic, including its CMFB circuit and chopper stabilization switches.

3.2.1 DM-Artifact Tolerant Gm-C Integrator

As described in details in Chapter 2, the ADC-direct recording channel is designed in a way that in the event of a large DC difference between the two differential inputs (offset or DM artifact), the backend artifact detection module triggers a process that (a) temporarily converts the circuit into a SAR ADC to estimate the amount of DM artifact/offset, and (b) uses the data from the SAR logic to return the biasing of the G_m stage to a balanced situation and cancel the effect of the DM artifact. This requires certain design considerations in the G_m-stage implementation to ensure such an adjustment is done effectively and with minimal additional power cost. To implement the described bias adjustment scheme, first we divided the original M5 and M6 into parallel transistors M5a,

M5b, M6a, and M6b as shown in Figure 3.16. While we expect the DM artifact/offset to cause biasing imbalance, we also assume that there is a maximum to this imbalance. Based on the experimental results reported in the literature, we expect the maximum offset and DM artifact to be limited to ±200 mV. Our simulation results show that this amount of DM artifact could change the biasing of the M5,6 (i.e., 3.9 mA when there is no DM artifact) by ±1.8 mA. In other words, these transistors have a minimum of 2.1 mA and a maximum of 5.7 mA bias current, depending on the DM artifact magnitude and polarity. As such, when each of the M5,6 is converted into two transistors, M5a, 6a are biased with a fixed 2.1 mA as the bias current, and M5b,6b are used as the devices with a variable bias (0-3.6 mA) controlled by the SAR-based feedback. Considering that an increase in one side's bias current needs an identical decrease on the other side, this means that the total bias current of the G_m-stage will remain constant. Therefore, once the SAR-based balancing process is over and the new biasing condition is established, the circuit's overall power consumption is intact.

During the artifact magnitude estimation phase, the SAR DAC replaces M5b and M6b and estimate a differential current for them. S7, S8, S9, and S10 are added to the circuit to replace the M5b and M6b with current-steering SAR DAC outputs. In addition, as described in section 2.3 of the previous chapter, during the estimation phase, the OTA's output is directly connected to the comparator to form a SAR ADC for artifact magnitude estimation. This needs the integrating capacitor to be switched out of the circuit during this phase. This is done using S11, S12, and S13as depicted in Figure 3.15.

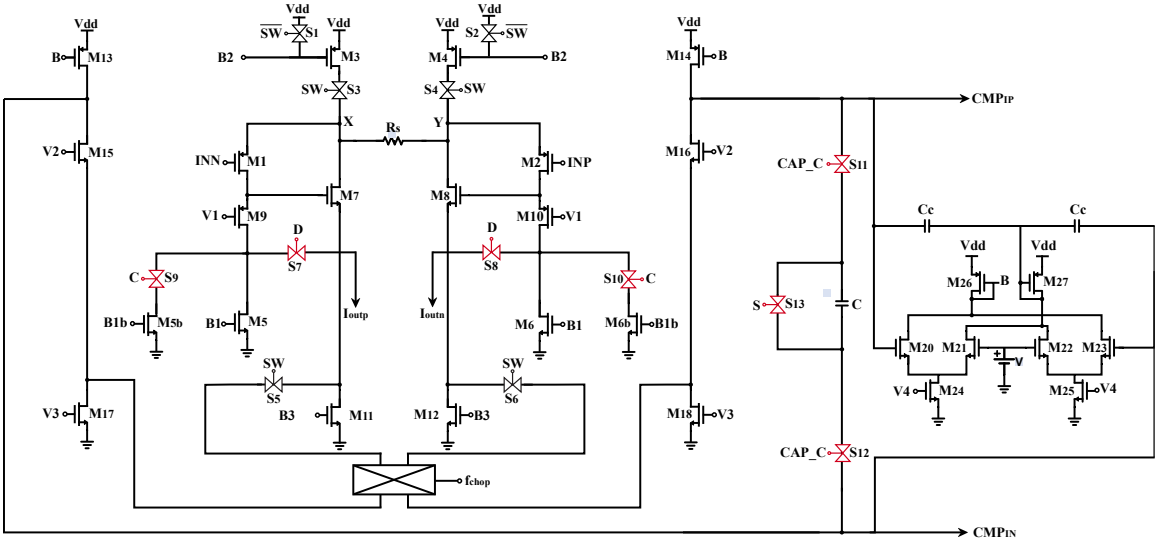

Figure 3.15 The proposed G_m-C integrator with variable bias for handling DM artifacts and offsets.

Figure 3.16 and Figure 3.17 depict the proposed G_m-C integrator during the normal and artifact removal modes of operation, respectively.

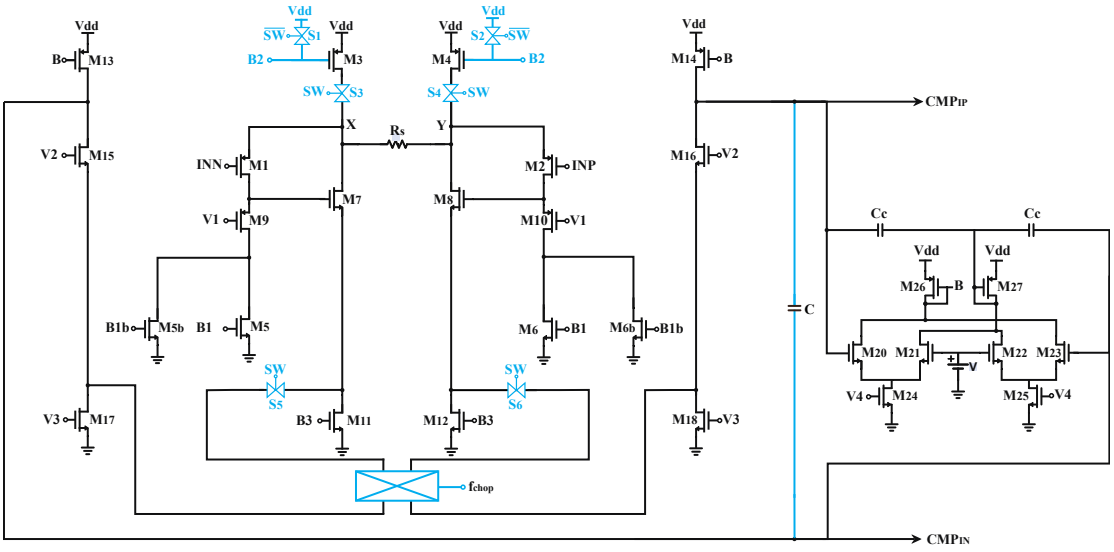

Figure 3.16 G_m-C integrator circuit in the normal mode of operation.

The artifact compensation mode takes 120 µsec (equal to 12 cycles of 100 kHz clock), and during this short period, the power cycling is turned off, leading to a higher power consumption. However, after compensating the artifact, the circuit with the new biasing condition goes back to the normal mode with a power consumption that has not changed. Therefore, the power increase only happens in the beginning and end of stimulation pulses and for a very short period of time. Additionally, it should be considered that electrical stimulation pulses in an implantable device typically have a very infrequent occurrence (e.g., 1-2 times a day in closed-loop stimulators for epilepsy [13]). Therefore, this short-time power increase will have virtually zero impact on the average power consumption of the implant.

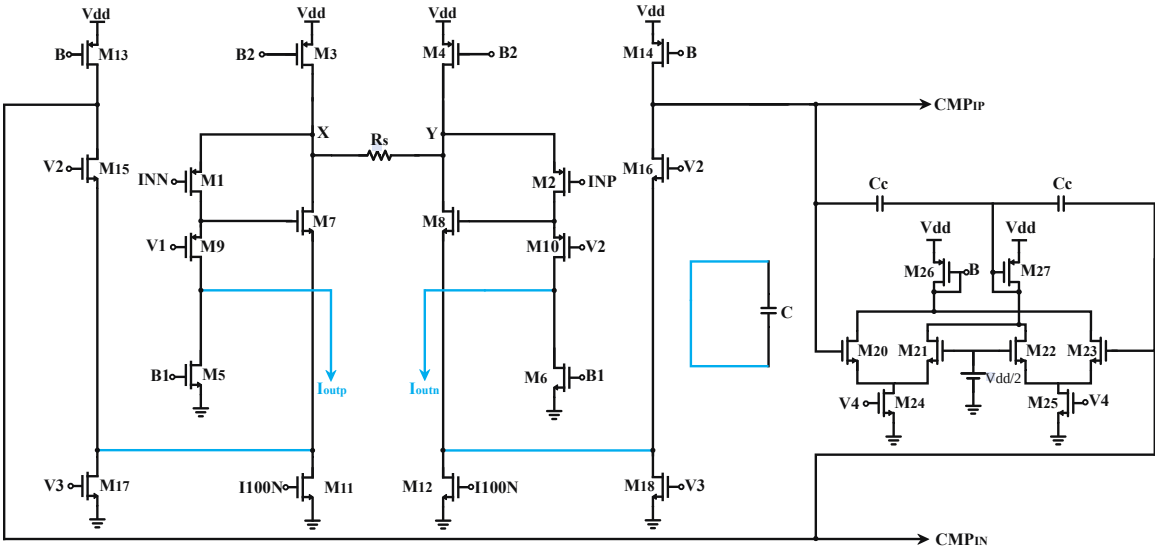

Figure 3.17 G_m-C integrator circuit in artifact removal mode of operation.

When DM artifact is present on top of a large CM artifact, g_m of M1 and M2 is expected to change drastically, which causes significant nonlinearity in the signals

recorded during stimulation. In this situation, the described bias balancing scheme using the SAR DAC helps keeping the G_m constant. As an example, if we assume that INP decreases and INN increases, the DAC predicts a higher current to be required than what M6 is providing in the respective node. This increase in the bias current of M2 will compensate the original increase in its V_{OD} (due to INP decrease) and brings back the M2's g_m ($2I_D/V_{OD}$) to the original value. The efficacy of this method is verified in Cadence simulations, and G_m variation of the transconductance amplifier is shown to be less than 5% for a 200 mV change in the input differential voltage. Figure 3.18 shows different G_m curves of the amplifier, where each of the curve represents the G_m for a different biasing situation.

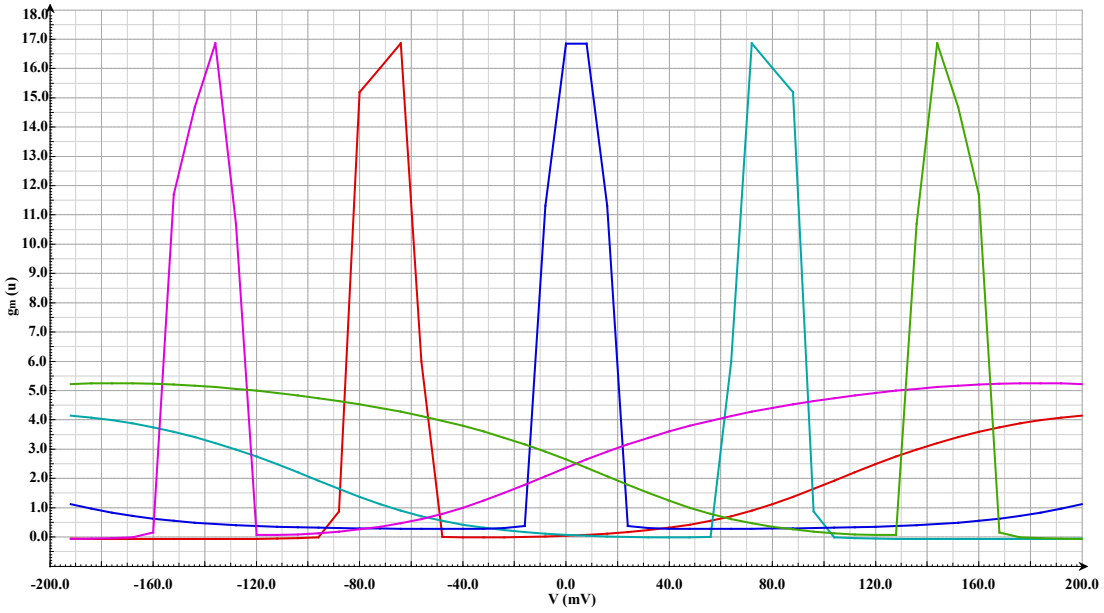

Figure 3.18 G_m of the presented transconductance amplifier with adjusted biasing vs. differential input voltage.

3.3 ΔΣ ADC Implementation

3.3.1 Comparator

A StrongArm comparator is used as the quantizer in ΔΣ ADC. Thanks to its fully dynamic operation (i.e., no static power) the comparator adds minimally to the overall power consumption. To reduce the hysteresis, four reset transistors are used. These transistors reset the output nodes periodically to keep the initial state of the comparator constant for all the inputs. Figure 3.19 shows the comparator. As mentioned, the oversampling ratio of the ΔΣ ADC is 100 and bandwidth is 5 kHz. Therefore, the comparator should be able to operate at 1 MHz. The average power consumption is 1.6 µW and the hysteresis is 20 µV based on the post-layout simulation results.

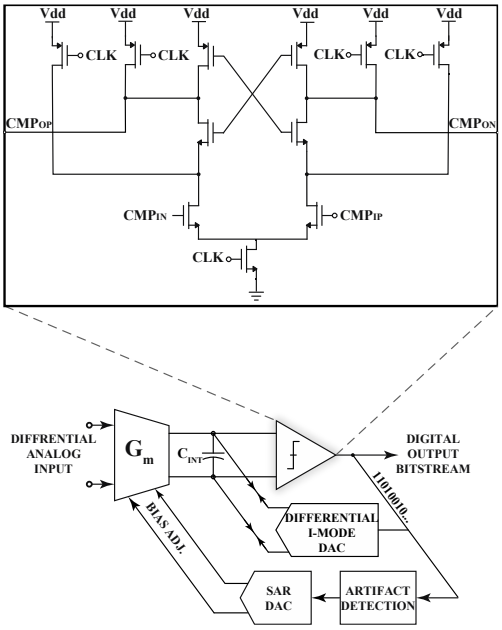

Figure 3.19 The StrongArm comparator used for the 1-bit quantizer in the presented neural ΔΣ ADC.

3.3.2 The 1-Bit Current-Mode DAC

As described its functionality in Chapter 2, the 1-bit current-mode DAC should be designed to push/pull a constant current into the integrating capacitor of the G_m-C filter to form the Δ part of the ΔΣ modulator. A simple push/pull charge pump is used for this block, as shown in Figure 3.20. Thanks to the CMFB used at the output of the G_m-stage, the DC level at the output of the current DAC remains relatively constant and at around mid-rail (i.e., $V_{DD}/2$). which relaxes the output impedance requirement for the charge-pump. It should also be noted that any mismatch between the push and pull currents will translates into an offset error and will not affect the dynamic performance of the ΔΣ ADC.

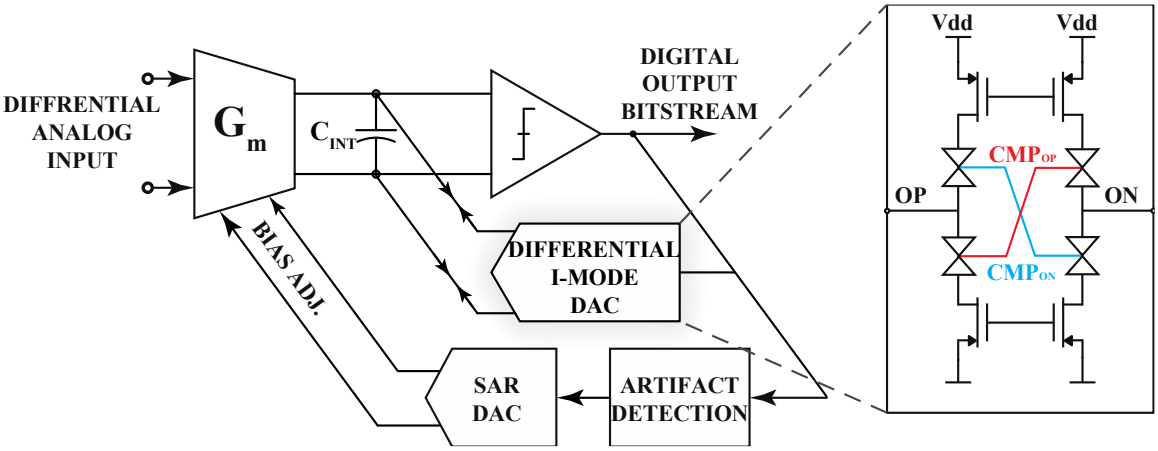

Figure 3.20 Push-pull charge pump 1-bit DAC of the ΔΣ ADC.

3.3.3 SAR DAC

The DAC used for estimation and correction of DM artifacts and offsets in the input G_m-stage is shown in Figure 3.21. As shown, it is a 12-bit current-steering DAC with a SAR architecture. As mentioned, during the artifact compensation mode the outputs of this

DAC replace the bias current provided by M5 and M6. Since the DAC is used only when a large DM artifact is detected, it will be only ON for ~0.1% of the time during the periods when electrical stimulation is performed. Considering the infrequent occurrence rate of electrical stimulation, the ON time of this DAC is even more negligible, despite its critical role in proper operation of the entire recording channel. As a result, it is designed with the main focus being on its speed and accuracy as it is used in the body of the SAR ADC that estimates the magnitude of the DM artifact and needs to produce a precise updated current at every highly-oversampled clock cycle.

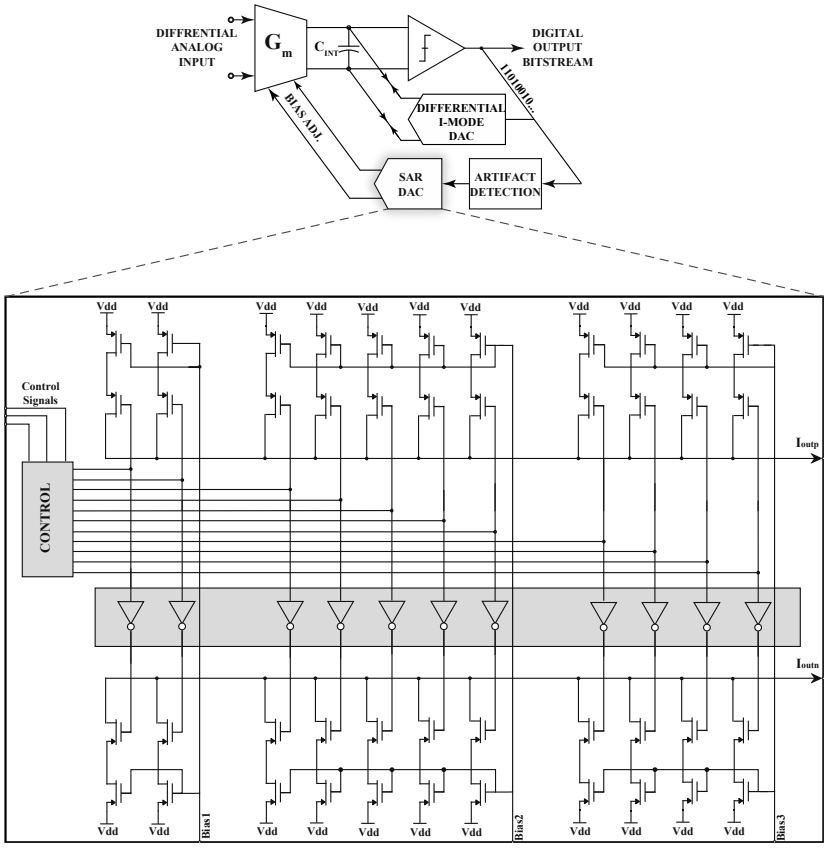

Figure 3.21 The SAR DAC architecture used in artifact removal mode of operation.

3.4 Complete Recording

Figure 3.22 shows an example scenario where the input signal to the presented circuit is a 1 mV_{pp} 1.3 kHz sinusoidal representing the neural signal. The input signal's DC level sits at 0.9 V and there are no CM or DM artifacts present. The output bitstream (i.e., the output of the comparator) and the reconstructed signal (the low-pass filtered version of the output bitstream) are shown.

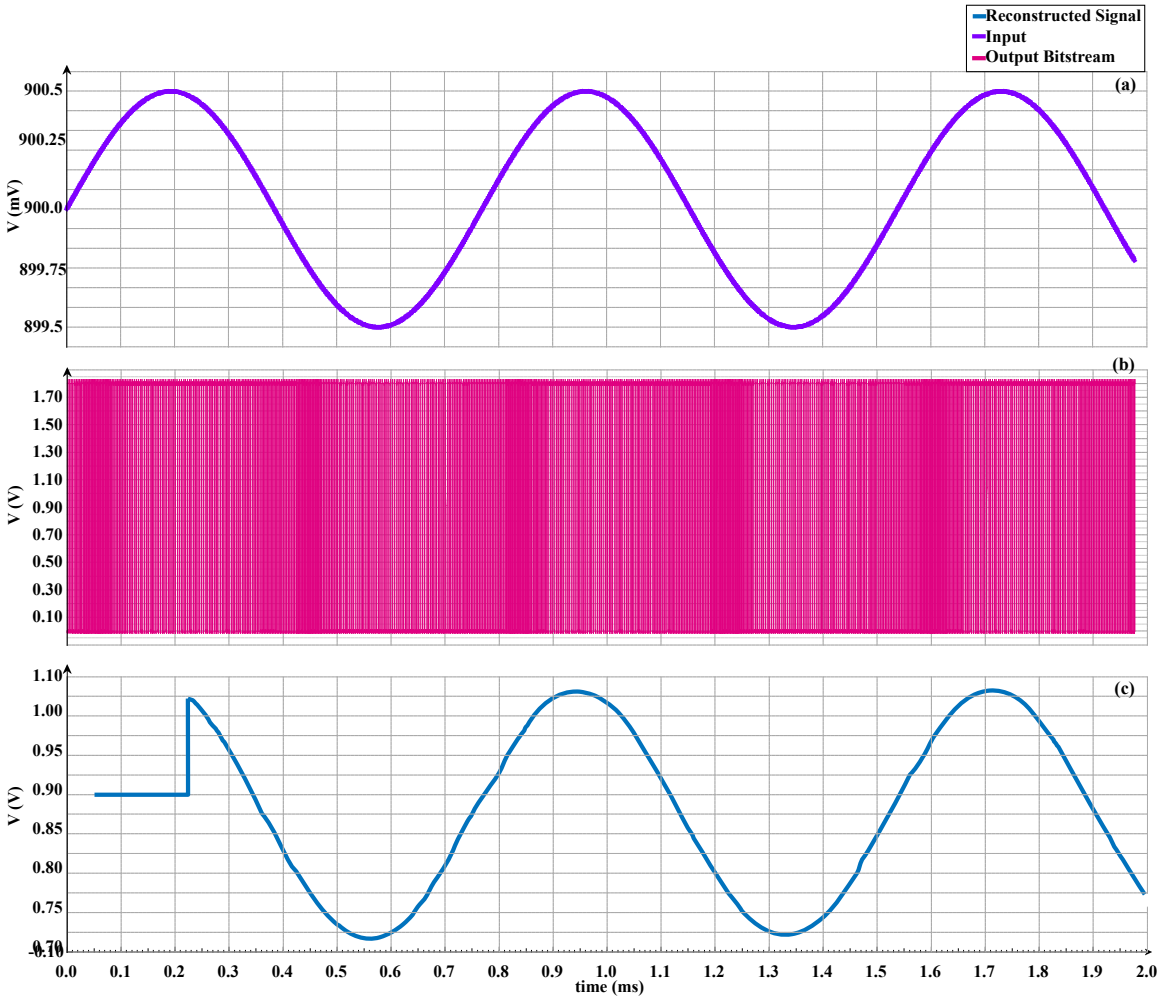

Figure 3.22 Recording channel's performance when the input is a 1 mV_{pp} 1.3 kHz sinusoidal. (a) input signal. (b) output bitstream. (c) reconstructed signal.

The output's spectral view of the bitstream is plotted in Figure 3.23, where the first order noise shaping apparent. The achieved SNR is 59.66 dB, which is equivalent to an effective 9.6 bits. The input signal frequency is chosen 76 Hz in this figure.

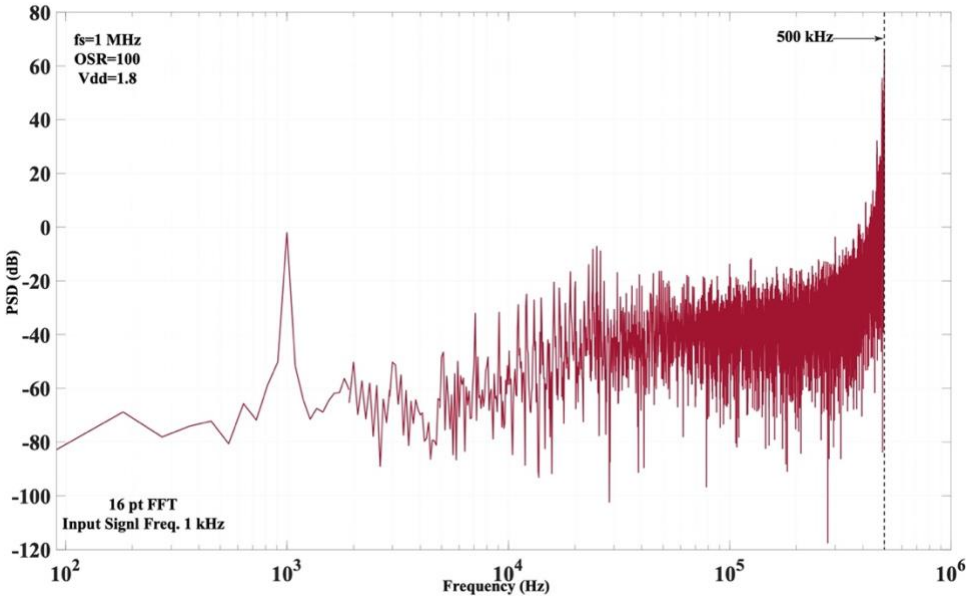

Figure 3.23 Power spectral density plot of the output bitstream showing the noise shaping and the SNR of the presented ΔΣ modulator.

Figure 3.24 shows another example where the input signal to the presented circuit is a combination of a 1 mV_{pp} 1.3 kHz sinusoidal representing the neural signal as well as a 150 mV_{pp} pulse representing the large differential artifacts. The output bitstream and the reconstructed signal are shown. The signal to noise ratio of the recording circuit is 48.02 dB, which is an 11 dB reduction compared to the artifact-less case presented Figure 3.22. This reduction is due to many non-idealities such as residue differential current, gain change because of unbalanced biasing of the G_m, additional noise of the DAC transistor added to the circuit, and chopping the SAR DAC.

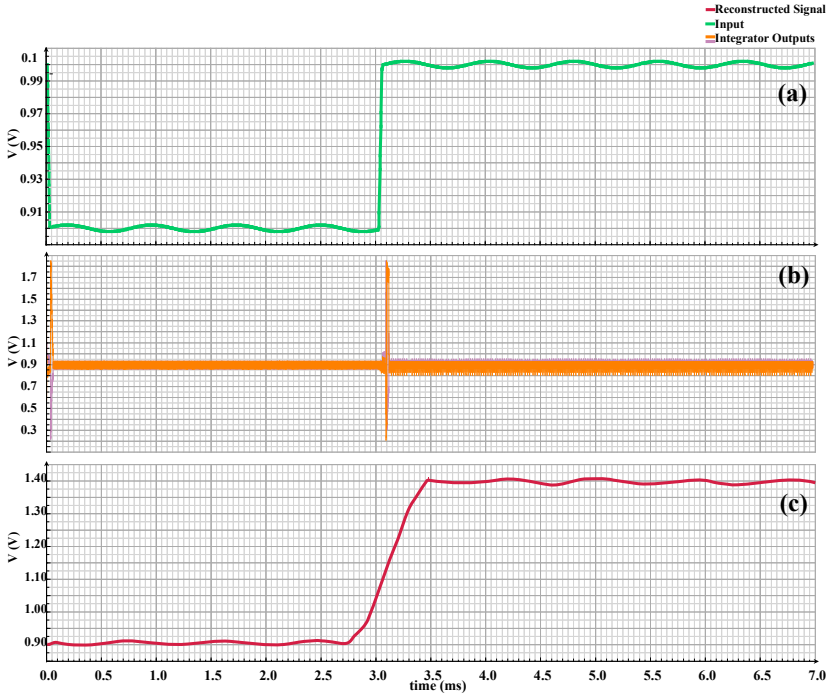

Figure 3.24 Recording channel's performance when the input is a combination of a 1 mVpp 1.3 kHz sinusoidal and a 150mVpp square. a) Input signal. b) Integrator's outputs. c) Reconstructed signal.

It should be noted that 48 dB is SNR is for neural signals, which will be translated to 7.7 ENoB and is enough for digitizing. With the SAR DAC capable of removing artifacts up to 200 mV, the DR of 94 dB is achieved, which means 15.3 ENoB. Also, the linear CM input range of this front-end is 300 mV.

3.5 Current Stimulator

As mentioned in the first chapter, the main goal of this design to enable simultaneous recording and stimulation. We implemented an 8-bit current-mode DAC in each channel to conduct current-mode stimulation. The current-mode stimulators are

generally preferred over the voltage-mode ones because the injected charge transferred to the brain can be controlled precisely. Figure 3.25 depicts the current stimulation circuit, which consists of an 8-bit current DAC, a current mirror output stage, and a control block. The current mirror is used to increase the output impedance and headroom voltage. Besides, it enables biphasic current stimulation. The control block receives the stimulation amplitude, waveform and source/sink and produces control signals for the DAC and output stage switches.

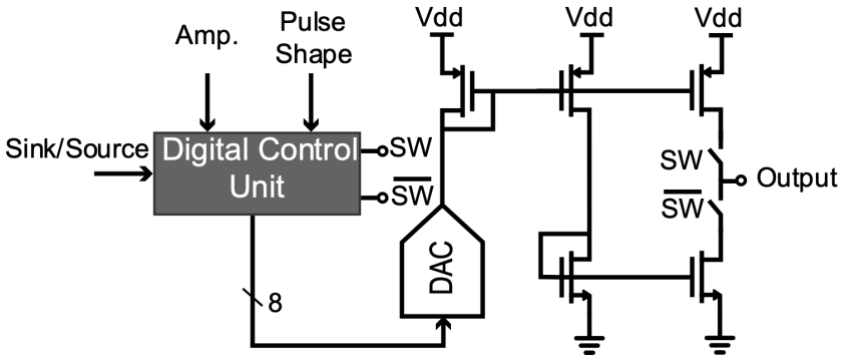

Figure 3.25 Current stimulator's architecture.

3.6 Fabricated Microchip

Figure 3.26 shows the layout of the presented 3×3 mm2 8-channel microchip designed and fabricated in TSMC 180nm CMOS technology. The recording and stimulation channels are highlighted, and their corresponding dimensions are annotated. Finally, in

Table 3.8 the presented work design is compared with the state of the art.

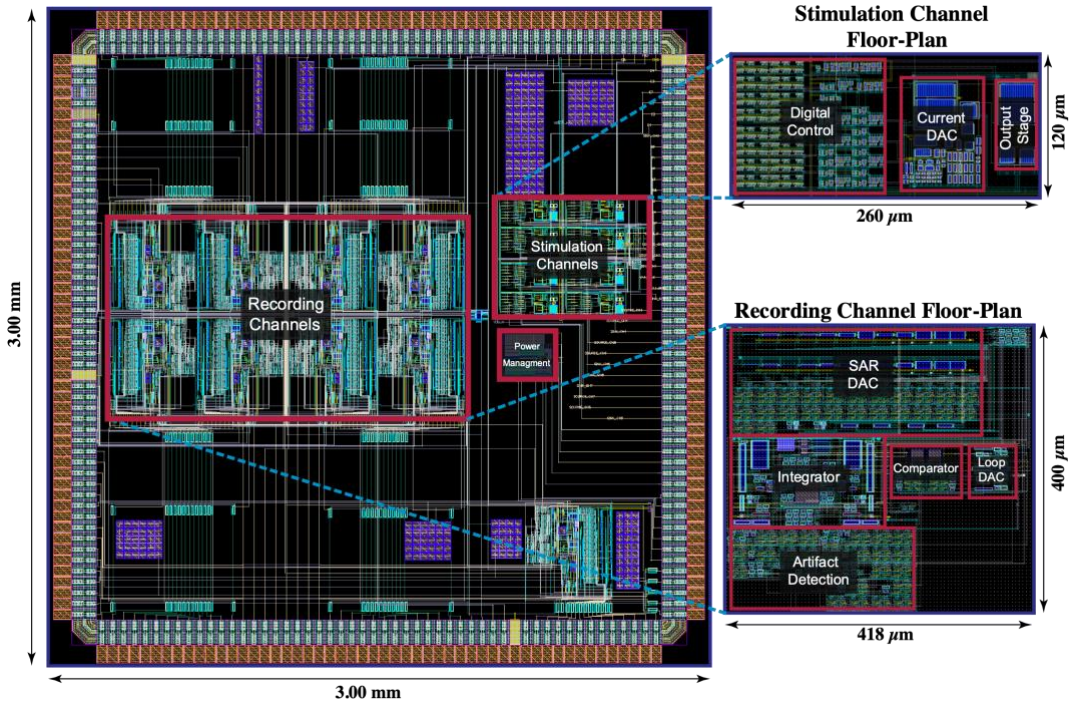

Figure 3.26 Chip-Level Layout of the 8-Channnel Neural Recording and Stimulation.

Table 3.8: Comparison of the proposed design with the State-of-the-art

Parameters	ISSCC20 [38]	ISSCC20 [36]	ISSCC18 [12]	ISSCC18 [29]	JSSCC20 [37]	This Work[a]
Power (µW)	1.48	6.5	0.8	7.3	2.98	4.6
Supply (V)	1.5	1	0.8	1.2	0.5, 2.5	1.8
IRN (μV_{rms}) (IN B.W. (Hz))	1.8 (1-1000)	1.2 (1-200)	0.6 (1-200)	1.8 (1-200)	1.66 (1-1000)	1.22 (1-500)
Input B.W. (Hz)	1 K	10 K	500	5k	1 K	5 K
Max. DM Artifact (mV)	57	300	260	200	110	200
Max. CM Artifact (V)	1.5	-	-	600 m	R-to-R	150 m
Input Impedance (Ω)	>2.2 G @1kHz	Infinite (AC-coupled)	26 M @500Hz	100 M @1KHz	92 M @2kHz	1.8 G @1kHz
Area (mm^2)	0.09	0.078	0.024	0.113	0.0023	0.1
NEF	2.07	-	1.81	-	2.21	1.03

[a] The presented results for this work are from simulations.

Chapter 4

Conclusion and Future Directions

4.1 Conclusion

In this thesis, a novel architecture for simultaneous neural recording and stimulation was presented. Each recording channel consists of an ADC-direct ΔΣ-based front-end circuit equipped with a highly-linear transconductance stage for handling large CM artifacts, and assisted by a SAR-based feedback loop to handle large DM artifacts and offsets. The ΔΣ ADC yields a 94 dB DR (about 15 bits ENOB). The total power consumption per channel is simulated to be 4.6 μW for 5 kHz bandwidth respectively. The channel has an input impedance of higher than 1GΩ, and a CMRR of 93 dB. Chopper stabilization is performed at the DC-coupled inputs to remove flicker noise and the input-referred noise power spectral density is 55 $V^2/\sqrt{Hz}$ at 32 kHz. Each channel is also equipped with a dedicated current-mode electrical stimulator. Current simulators are biphasic, and an 8-bit DAC is used for implementing them.

To further validate the circuits performance, two microchips have been implemented in TSMC 180nm standard CMOS technology. The first chip consists of two recording channels, with the artifact detection block placed off-chip and implemented on an FPGA. This design is fabricated as a 1.1x1.6 mm^2 IC. The second chip consists of an 8-neural recording and stimulation channel, and artifact detection block is implemented on-chip. Both chips are back from fabrication and a PCB test board is designed, fabricated, assembled and programmed to test the chips. Due to the ongoing pandemic, the testing process has been delayed and could not be completed at the time of submitting this thesis for defense.

4.2 Future Directions

4.2.1 System Improvements

4.2.1.1 Increasing Dynamic Range

Although the dynamic range of this system is high, it cannot cover all the input range. In terms of CM artifacts, if the amplitude increases, the gm of the circuit will change. Therefore, the amplifier's gain decreases, and the resolution will be decreased when artifacts are present. Also, the system will be saturated if the amplitude increases more than

200 mV. Therefore, increasing the input dynamic range is one of the main targets of the next generation of this device.

4.2.1.2 Patient-Specific Stimulation

In this design, the focus was on the neural recording channel to make it capable of recording in the presence of stimulation artifacts. However, this does not complete closed-loop stimulation microsystem. In the next design, a signal processing unit will be added to the system to dynamically change the stimulation signal's pattern based on the recorded data. Enabling this would be a significant step toward unsupervised patient-optimized brain stimulation for the long-term treatment of neurological disorders.

4.2.1.3 Activity-Dependent Recording for Energy-Efficient Data Transmission

Power is a critical parameter in implantable devices. With the rapidly-growing demand for high-density brain-interfacing channels for the same power budget, satisfying the power requirement has become increasingly challenging, and it cannot be done with conventional designs, and more features should be added to the SoC. In the next generation, an input-dependent power adaptivity feature will be added to the SoC to reduce the recording power when neural activity is not detected.

The proposed architecture works continuously, and the data rate is 80 kbit/sec. This data rate is acceptable for 8 channels, but if we want to increase the density to 1024 channels, the data rate will be about 80 Mbit/sec, which requires significant power

consumption for transmission. Hence, data compression techniques will be added to the system to reduce the data rate before transmission.

4.2.1.4 Integration of a Wireless Powering Module

The proposed recording and stimulation channels are low-power and low-area. Therefore, they can be used as an implantable device. However, without adding a coil to the chip (on or off-chip) to receive power from outside and transmitting the recording data, it cannot be fully implantable. Using on-chip coils to power the system continuously is very challenging. However, adding it to the chip will be an excellent improvement for the next design.

4.2.2 Further in-vivo and in-vitro Experiments

Due to the time constraints and COVID-19 pandemic, the fabricated chip's experimental results are not completed and not presented in this thesis. The design should be experimentally validated. These measurements include testing the functionality of each block and the performance of the system. Figure 4.1 shows the PCB board which is designed for the testing and it includes both designed chips, the biases and an FPGA for generating the control signals and storing output data. The FPGA is programmed, and all the biases are adjusted. Therefore, testing the fabricated chips will be the first step.

First, the functionality of each block will be tested, then the loop performance will be checked by applying a sinusoidal wave with a 1 mV amplitude and 1 kHz frequency. The SNR of the system will be calculated based on the output bitstream and after that an

artifact will also be added to the input by using a voltage pulse to check the functionally of the artifact recovery mode of operation.

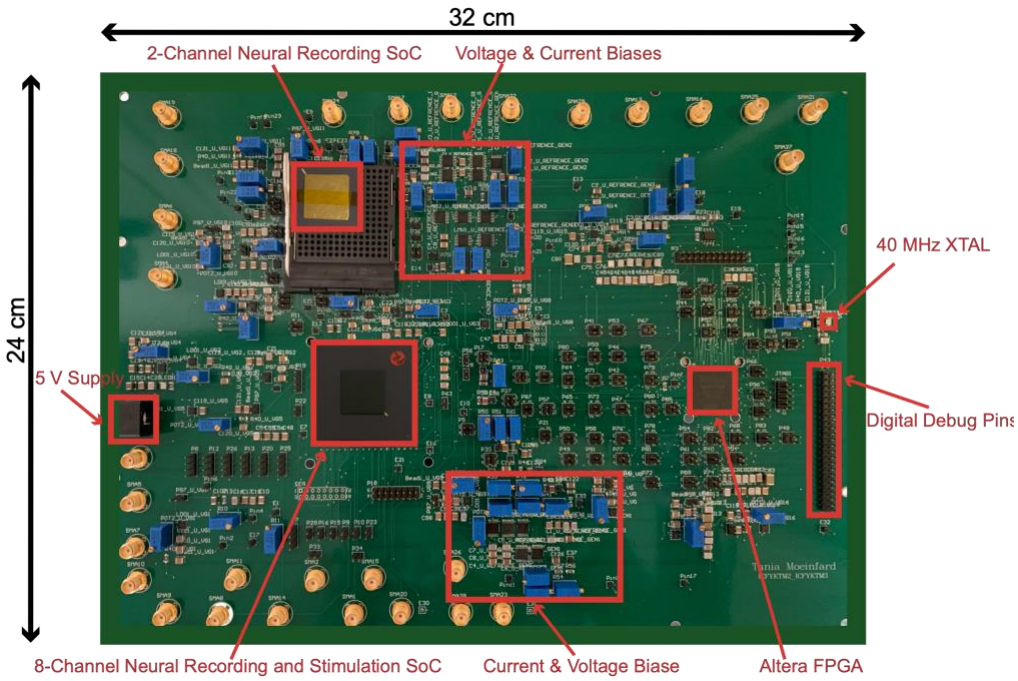

Figure 4.1 Designed board for testing the ICs

In addition to experimental results, in-vivo and in-vitro tests should be added. This microsystem is designed to be implantable, and any biomedical implantable device must be tested in vitro. This measurement will be performed using electrodes dipped in phosphate-buffered saline (PBS). A specific stimulation waveform will be injected into the solution, and pre-recorded human neural recordings will be added. Using this test setup, large artifacts will be sensed at the input of recording channels. The output of the recording channel will be observed in order to measure the achieved SNR of the recording channel. This step will show the effectiveness and reliability of the system.

4.3 Encapsulation and Packaging

Before the in-vivo testing, the safety of the devices should be guaranteed. Therefore, Encapsulation and packaging are necessary steps. Both the device and the brain cells should be protected from each other using a biocompatible encasing. It should be noted that the circuit is consists of standard materials. Therefore, it is compatible with standard encapsulation techniques.

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Appendix A

Board Design

As mentioned, two protypes are fabricated in this project. The first one, includes 2 high-DR neural recording channels and the second one includes 8 high-DR recording channels with an on-chip artifact detection block and 8 neural stimulation channels. Therefore, the board is designed to test both chips.

The fabricated board includes, biasing of the two chips and an FPGA. The FPGA is used to generate the required control signals of the ICs and to decimate the output bitstream of the neural recording channels. The reason for off-chip biasing is that the neural recording channel is designed in a way that its parameters including clock frequency, power consumption and bandwidth can be changed after the fabrication. Therefore, off-chip biasing is used to test the design flexibility as well.

MATLAB Code for the Presented Neural Recording Channel

```
clk=1e6; % clock frequency of the comparator
N=clk;
tstop=(N-1)/(clk);
% tstop=1;
amp=1e-3; %nueral signal amplitude
t=0:1/clk:tstop;
fs=clk;
```

```
cycle=37;
fx=1300; %neural signal amplitude
A=amp;
vp=amp*sin(2*pi*fx*t); %INP of the integrator
vn=amp*sin(2*pi*fx*t+pi); %INN of the integrator
m=tstop*clk+1;
artifact=zeros(1,m);
artifact(1,1/60*m:20/45*m)=50*amp; %adding DM artifact to the input
artifact(1,2/4*m:3/4*m)=190*amp; %adding DM artifact to the input
artifact(1,3/4*m:4/4*m)=150*amp; %adding DM artifact to the input
vp=vp+artifact;
%voltage to current conversion
gn=1.25e-6;
gp=1.25e-6;
ip1=300*1e-9+gn*vp;
ip2=300*1e-9+gn*vn;
in1=300*1e-9-gp*vp;
in2=300*1e-9-gp*vn;
i1=600*1e-9;
i2=600*1e-9;
i3=i1-ip1;
```

```
i4=i2-ip2;

i7=600*1e-9;

i8=600*1e-9;

i5=i7-in1;

i6=i8-in2;

io1=i5-i3;

io2=i6-i4;

x=0;

y=0;

n=0;



$integrating

io=io1-io2;

Rout=1e9;

C_int=1e-12;

Vc=0;

Vfinal(1)=0;

i_step(1)=0;

cp=50e-9;

dac2=4e-6;
```

```
cmp(1)=0;
out=0;
fc(1)=1;
f=1;
b7=0;
b6=0;
b5=0;
b4=0;
b3=0;
b2=0;
b1=0;
b0=0;
stim=0;
q=0;
step=1;

for k=2:step:tstop*clk+1
   n=n+1;
   en(k)=0;
%Activation of the first loop of the desig
if stim==0
```

```
    step=1;
    i_step(k)= io(k)-cp*cmp(k-1);
    Vfinal(k)=Rout*i_step(k);
    Vc(k)=Vfinal(k)+(Vc(k-1)-Vfinal(k))*exp(-1/(clk*(Rout*C_int)));

if Vc(k)>=0
    cmp(k)=1;
    x=x+1;



elseif Vc(k)<0
    cmp(k)=-1;
    y=y+1;
end

if x==16 && n==16
    sgn=1;
    stim=1;
    x=0;
    y=0;
```

```
    n=0;
elseif y==16 && n==16
    sgn=-1;
    stim=1;
    x=0;
    y=0;
    n=0;
elseif n==16
    stim=0;
    x=0;
    y=0;
    n=0;
end
%activation of the second loop of the delsig (SAR DAC)
elseif stim==1
    en(k)=1;
    idac(k-1)=+(b7+b6/2+b5/4+b4/8+b3/16+b2/32+b1/64+b0/128)*dac2;
    i_step(k)= io(k)-sgn*idac(k-1);
    Vfinal(k)=Rout*i_step(k);
    Vc(k)=0;
   %predicting the SAR DAC output current
```

```
vcomp(k)=i_step(k);
    switch n
        case 1
            b7=1;
            if vcomp(k)>0
                cmp(k)=1;
            else
                cmp(k)=-1;
            end
        case 2
            b6=1;
            if vcomp(k)>0
                cmp(k)=1;
                b7=0;
            else
                b7=1;
                cmp(k)=-1;
            end
        case 3
            b5=1;
            if vcomp(k)>0
```

```
        cmp(k)=1;
        b6=0;
    else
        b6=1;
        cmp(k)=-1;
    end
case 4
    b4=1;
    if vcomp(k)>0
        cmp(k)=1;
        b5=0;
    else
        b5=1;
        cmp(k)=-1;
    end
case 5
    b3=1;
    if vcomp(k)>0
        cmp(k)=1;
        b4=0;
    else
```

```
        b4=1;
        cmp(k)=-1;
    end
case 6
    b2=1;
    if vcomp(k)>0
        cmp(k)=1;
        b3=0;
    else
        b3=1;
        cmp(k)=-1;
    end
case 7
    b1=1;
    if vcomp(k)>0
        cmp(k)=1;
        b2=0;
    else
        b2=1;
        cmp(k)=-1;
    end
```

```
case 8
   b0=1;
   if vcomp(k)>0
      cmp(k)=1;
      b1=0;
   else
      b1=1;
      cmp(k)=-1;
   end
case 9

   if vcomp(k)>0
      cmp(k)=1;
      b0=0;
   else
      b0=1;
      cmp(k)=-1;
   end

case 10
   u(k:m)=idac(k-1);
```

```
            io(k:m)=io(k:m)-sgn*u(k:m);
            n=0;
            stim=0;
            b7=0;
            b6=0;
            b5=0;
            b4=0;
            b3=0;
            b2=0;
            b1=0;
            b0=0;
            q=0;
            x=0;
            y=0;
            if vcomp>0
               cmp(k)=1;
            else
               cmp(k)=-1;
            end
        end
end
```

```
end


length_cmp=length(cmp);
for i=1:length_cmp;
   if cmp(i)>0
      cmp(i)=1.8;
   else
      cmp(i)=0;
   end
end


for o=1:m-200
   e=o+200;
   out(o)=mean(cmp(o:e));
end
for o1=1:m-450
   e1=o1+250;
   out(o1)=mean(out(o1:e1));
end
subplot(3,1,1);plot(t,vp)
xlim([0 0.06])
```

```
ylim([0 0.2])
subplot(3,1,2);plot(t,cmp)
xlim([0 0.06])
subplot(3,1,3);plot(t,out)
xlim([0 0.06])
```

Generating Clock Signals

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Create Date:    2:44pm 12/08/2012
// Module Name:    Voltage_DAC_cont
// Target Device:          EP3C10-FBGA256-2
//
//////////////////////////////////////////////////////////////////////////////////
module CLK_GEN(clkIn, CLK_ADC, CHOP1, CHOP2, CLK, CLK_D, RST, TT,
IN_O1, IN_O1D, SHORT);

input               clkIn;
output   reg CLK_ADC = 1 ;
output   reg CHOP1 = 1 ;
output   reg CHOP2 = 1;
```

```
output   reg CLK = 1;

output   reg CLK_D = 1;

output   reg RST = 0;

output   reg TT = 0;

output   reg IN_O1 = 1;

output   reg IN_O1D = 1;

output   reg SHORT = 0;

//Delay Defining parametrs

reg   CLK_ADC_Flag = 0;

reg   CHOP1_Flag = 0;

reg   CHOP2_Flag = 0;

reg   CLK_Flag = 0;

reg   CLK_D_Flag = 0;

reg   RST_Flag = 0;

reg   TT_Flag = 0;

reg   IN_O1_Flag = 0;

reg   IN_O1D_Flag = 0;

reg   SHORT_Flag = 0;

//Frequency Defining parametrs

reg   [11:0] CLK_ADC_Counter = 0;

reg   [11:0]CHOP1_Counter = 0;
```

```
reg   [11:0]CHOP2_Counter = 0;
reg   [11:0]CLK_Counter = 0;
reg   [11:0]CLK_D_Counter = 0;
reg   [11:0]RST_Counter = 0;
reg   [11:0]TT_Counter = 0;
reg   [11:0]IN_O1_Counter = 0;
reg   [11:0]IN_O1D_Counter = 0;
reg   [11:0]SHORT_Counter = 0;
//< Clock Producing
always @ (posedge clkIn)   //CLK_ADC
        begin
                CLK_ADC_Counter <= CLK_ADC_Counter+1;
                if (CLK_ADC_Flag ==0 && CLK_ADC_Counter==116)
                begin
                        CLK_ADC_Flag <=1;
                        CLK_ADC_Counter <=0;
                        CLK_ADC <=0;
                end

                if(CLK_ADC_Flag==1)
                begin
```

```
                if (CLK_ADC_Counter==160)
                begin
                CLK_ADC <=!CLK_ADC;
                CLK_ADC_Counter <= 0;
                end
        end
    end



always @ (posedge clkIn)   //CHOP1
    begin
        CHOP1_Counter <= CHOP1_Counter+1;
        if (CHOP1_Flag ==0 && CHOP1_Counter==340)
        begin
            CHOP1_Flag <=1;
            CHOP1_Counter <=0;
            CHOP1 <=0;
        end

        if(CHOP1_Flag==1)
```

```
        begin
                if (CHOP1_Counter==620)
                begin
                CHOP1 <= !CHOP1;
                end
                if (CHOP1_Counter==1200)
                begin
                CHOP1 <= !CHOP1;
                CHOP1_Counter <= 0;
                end
        end
end
always @ (posedge clkIn)   //CHOP2
begin
        CHOP2_Counter <= CHOP2_Counter+1;
        if (CHOP2_Flag == 0 && CHOP2_Counter == 360)
        begin
                CHOP2_Flag <= 1;
                CHOP2_Counter <= 0;
                CHOP2 <= 0;
        end
```

```
        if(CHOP2_Flag == 1)
        begin
                if (CHOP2_Counter == 580)
                begin
                CHOP2 <= !CHOP2;
                end
                if (CHOP2_Counter == 1200)
                begin
                CHOP2 <= !CHOP2;
                CHOP2_Counter <= 0;
                end
        end
end

always @ (posedge clkIn)   //CLK
begin
        CLK_Counter <= CLK_Counter+1;
        if (CLK_Flag == 0 && CLK_Counter == 4)
        begin
                CLK_Flag <= 1;
```

```
                CLK_Counter <= 0;
                CLK <= 0;
        end

        if(CLK_Flag == 1)
        begin
                if (CLK_Counter == 20)
                begin
                CLK <= !CLK;
                CLK_Counter <= 0;
                end
        end
end
always @ (posedge clkIn)   //CLK_D
begin
        CLK_D_Counter <= CLK_D_Counter+1;
        if (CLK_D_Flag == 0 && CLK_D_Counter == 12)
        begin
                CLK_D_Flag <= 1;
                CLK_D_Counter <= 0;
                CLK_D <= 0;
```

```
                end


                if(CLK_D_Flag == 1)
                begin
                        if (CLK_D_Counter == 20)
                        begin
                        CLK_D <= !CLK_D;
                        CLK_D_Counter <= 0;
                        end
                end
        end


always @ (posedge clkIn) //RST
 begin
 RST_Counter <= RST_Counter+1;
        if (RST_Counter == 1 && RST_Flag == 0)
                begin
                RST <= 0;
                RST_Flag <= 1;
                end
```

```
            else if (RST_Flag==1)
            RST <= 1;
            RST_Counter <= 0;
end


        always @ (posedge clkIn)   //TT
        begin
            TT_Counter <= TT_Counter+1;
            if (TT_Flag == 0 && TT_Counter==40)
            begin
                TT_Flag <=1;
                TT_Counter <=0;
                TT <=1;
            end

            if(TT_Flag==1)
            begin
                if (TT_Counter==380)
                begin
                TT<=1;
```

```
            end
            if (TT_Counter==400)
            begin
            TT<=0;
            TT_Counter<=0;
            end
        end
end


        always @ (posedge clkIn)   //IN_O1
        begin
        IN_O1_Counter <= IN_O1_Counter+1;
        if (IN_O1_Flag ==0 && IN_O1_Counter==60)
        begin
            IN_O1_Flag <=1;
            IN_O1_Counter <=0;
            IN_O1 <=0;
        end
```

```
        if(IN_O1_Flag==1)
        begin
                if (IN_O1_Counter==340)
                begin
                IN_O1<=!IN_O1;
                end
                if (IN_O1_Counter==400)
                begin
                IN_O1<=!IN_O1;
                IN_O1_Counter<=0;
                end
        end
end


        always @ (posedge clkIn)   //IN_O1D
        begin
        IN_O1D_Counter <= IN_O1D_Counter+1;
        if (IN_O1D_Flag ==0 && IN_O1D_Counter==68)
        begin
```

```
                IN_O1D_Flag <=1;
                IN_O1D_Counter <=0;
                IN_O1D <=0;
        end

        if(IN_O1D_Flag==1)
        begin
                if (IN_O1D_Counter==300)
                begin
                IN_O1D<=!IN_O1D;
                end
                if (IN_O1D_Counter==400)
                begin
                IN_O1D <= !IN_O1D;
                IN_O1D_Counter <= 0;
                end
        end
end

        always @ (posedge clkIn)   //SHORT
        begin
```

```
SHORT_Counter<=SHORT_Counter+1;
if (SHORT_Counter==396)
SHORT<=1;
if (SHORT_Counter==400)
begin
SHORT_Counter<=0;
SHORT<=0;
end
end-

endmodule
```

Programming the On-board Biasing DAC

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Create Date:    2:44pm 12/08/2012
// Module Name:    Voltage_DAC
// Target Device:          EP3C10-FBGA256-2
//
//////////////////////////////////////////////////////////////////////////////////

module DAC1 (
```

```
clkIn,
clkDAC,
start,
Data,
din1,
ldac1,
sync1,
din2,
ldac2,
sync2
//idle
);

// Inputs
input clkIn;
input start;  // Start signal
input [17:0] Data;  // Incoming data

// Outputs
output wire din1;
output reg ldac1 =1;
```

```
output reg sync1 =1;
output wire din2;
output reg ldac2 =1;
output reg sync2 =1;
output wire clkDAC;

// Registers
reg [4:0] timer = 5'b00000;
reg [15:0] Dataout;
reg idle;
reg ldac = 0;
reg sync =1;
reg chip0, chip1;

always @ (posedge clkIn)
begin

   case (timer)
      0:
      begin
         idle <= 0;
```

```
        sync <= 0;
        ldac <= 1;
    end
    15:
    begin
        sync <= 1;
        ldac <= 0;
    end
    17:
                                begin
        ldac <= 1;
                                                sync <= 1;
                            end
endcase

if (timer < 17 & ~idle)
    timer <= timer + 1;

if (timer < 15  & ~idle)
    Dataout <= { Dataout[14:0] , Dataout[15]};
```

```
        if (idle && start) //idle
        begin
            // Start operation
            timer <= 0;
            Dataout <= Data[15:0]; // Load the incoming data

            // chip selection
            // This has to be done here, so as sync and idle are not changed between
cycles
            chip0 <= ~Data[17] && ~Data[16];
            chip1 <= ~Data[17] && Data[16];
        end

        if (~idle && ~start)
        begin
            idle <= 1; // when start goes down, go back to idle
            ldac <= 1;
                                    sync <=1;
        end
    end
```

```
    assign din1 = Dataout[15];
    assign din2 = Dataout[15];

    always @ (sync)
    begin
       if (chip0)
          sync1 <= sync;
       if (chip1)
          sync2 <= sync;
    end
    always @ (ldac)
    begin
       if (chip0)
          ldac1 <= ldac;
       if (chip1)
          ldac2 <= ldac;
    end
    assign clkDAC = clkIn &&~sync;

endmodule
```