AN IR-UWB TRANSMITTER IC WITH INTEGRATED LOSSLESS NEURAL DATA COMPRESSION FOR HIGH-CHANNEL-COUNT IMPLANTS

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ABSTRACT

This thesis presents the design, development, and validation of a novel impulse radio ultra-wideband (IR-UWB) transmitter architecture with integrated lossless data compression, targeting high density neural implants. The proposed design incorporates (a) a greatest common divisor (GCD) based compression algorithm that is tailored to the sparse output of a level crossing ADCs (LCADC), (b) an edge combination based UWB transmitter circuit capable of pulse generation for 2-PPM modulation, and (c) programmability to mitigate process, voltage, and temperature (PVT) variations while ensuring spectral compliance. Our results demonstrate the system's capability to perform real time lossless compression, achieving 2 to 7 times (~50% to ~86%) reduction in transmitted bits and up to 17 times (94% reduction if minimal loss is tolerated), leading to significant reductions in transmission energy and enabling scalable channel counts under strict implant power budgets. When combined with the inherent data-rate reduction of LC-ADCs, the overall compression reaches ~259× (corresponding to 99.6% reduction compared to a traditional 10-bit ADC with a 20 kHz sampling rate), enabling proportionally higher channel counts within the same power and bandwidth budget.

The compression algorithm was implemented in System Verilog and synthesized in TSMC 180 nm CMOS, achieving 44.7 μW power consumption and 4114 μm^2 area for the compression block (from synthesis results). The transmitter was realized using programmable current-starved inverter delays, glitch generators, and a unit-cell amplifier, co-designed with a circular patch antenna centered at 4 GHz.

Both the digital controller and the transmitter were fabricated using the TSMC 180nm CMOS process. The digital controller and transmitter were tested with a custom receiver architecture.

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Chapter 1:

Introduction and Motivation

As of 2021, more than 3 billion people worldwide were living with a neurological condition. [1] Neurological disorders such as epilepsy, Parkinson's disease, and Alzheimer's disease not only diminish the quality of life for patients but also place significant emotional and financial burdens on their families and the healthcare system. As the global population ages, the prevalence of these disorders is expected to rise, further emphasizing the urgent need for effective diagnostic and therapeutic technology. Conventional treatment strategies such as medication, surgery, and neuroimaging have provided important tools for disease management, but their effectiveness is often limited by invasiveness, side effects, or insufficient temporal resolution. These limitations highlight the need for advanced neural monitoring technologies that can capture brain activity with higher fidelity and in real time.

High-density neural recording and closed-loop neuromodulation are two complementary technology paths responding to this need. High-channel-count recording enables the study and decoding of distributed neural activity, while closed-loop stimulation uses those measurements to deliver timely, individualized therapy. Even in stimulation-based approaches, accurate monitoring and diagnosis remain essential, as therapy effectiveness critically depends on reliable biomarkers

extracted from neural recordings [2], [3]. This chapter motivates the design choices that allow large-scale data acquisition and telemetry under strict safety and energy constraints.

1.1. Motivation

Over the past several decades, the capacity to measure neural activity has been advancing at an accelerating pace. By increasing the number of neurons simultaneously recorded, larger data sets can be used by neuroscientists to train algorithms to detect irregular brain activity in those who suffer from neurological disorders, restore motor function in individuals with paralysis, and advance our understanding of brain function. It takes 20 to 30 neurons recorded at the same time to decode the movement of a single finger of a human [4], and to scale recording full body movement would require thousands of neurons to be recorded and decoded simultaneously meaning that solutions enabling the scalability of high-density neuron recording is essential. Alike Moore's law, the observation that the number of transistors on a chip doubles approximately every two years, a parallel trend in neuroscience exists. It is referred to as the "Moore's Law of Neural Recording' where the number of neurons that can be simultaneously recorded doubles approximately every 7 years [5].

Scalability is limited by three tightly coupled factors: (i) power per channel (front-ends, digitization, and telemetry), (ii) area/volume available for electrodes and on-implant electronics, and (iii) safe heat dissipation in tissue. Even modest per-channel power (e.g., tens of μW) becomes untenable at 10^3–10^4 channels. Consequently, event-driven acquisition, in-situ compression, and bursty ultra-wideband (UWB) telemetry are attractive because they cut average energy per informative sample while respecting thermal and safety limits such a system is illustrated in Figure

1.1. The contributions presented in this thesis aim to advance the status quo of the Moore's Law of Neural Recording.

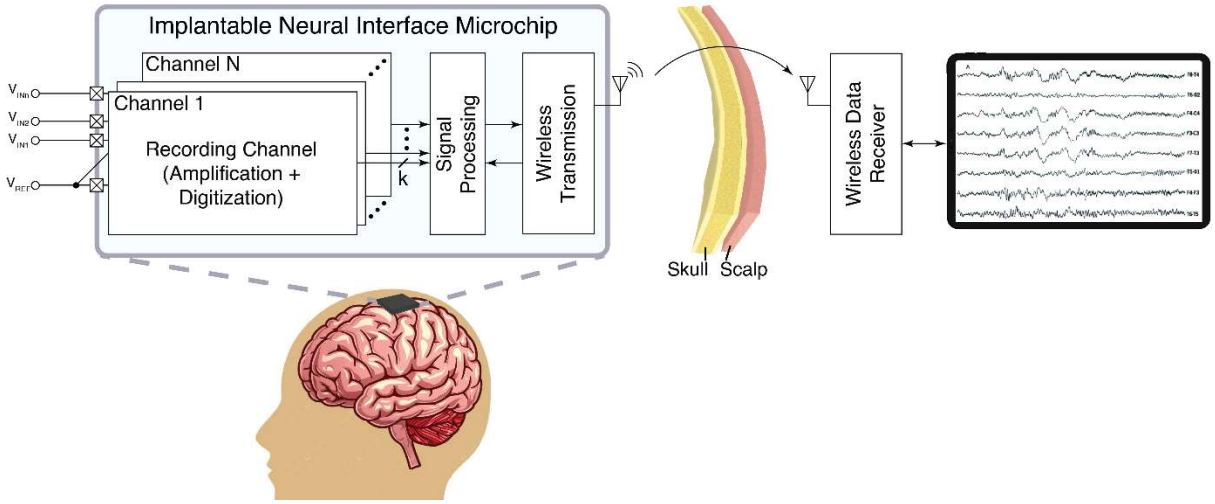


Figure 1.1: Block diagram and conceptual illustration of the proposed neural implant system.

Multiple recording electrodes interface with level-crossing ADCs (LCADCs) and shift registers, whose outputs are serialized and processed by the on-chip lossless compression module. The compressed data is then transmitted via the IR-UWB pulse generation chain (modulator, edge combiner, power amplifier) to an external UWB receiver, where the neural signals are reconstructed for monitoring and analysis.

1.2. Approach and Objectives

1.2.1. Observation: In implantable BCIs, the wireless transmitter is typically the dominant power consumer. Surveying recent neural-interface SoCs and telemetry links consistently show that the transmitter draws most of the system power [6], [7], [8], [9], [10], [11], [12], [13], [14], [15] , far exceeding the front-end [16], [17], [18], [19], [20], [21], [22] and digital processing [20],

[23], [24], [25], [26], [27], [28], [29], [30], [31] blocks. This is because raw neural data streams demand sustained high throughput to preserve both spikes and field potentials.

1.2.2. Approach: Enable channel-count scaling by cutting the energy required to deliver neural data off-implant. We pursue a two-pronged strategy: (1) reduce the number of bits that must be sent, and (2) make each transmitted bit cheaper.

1.2.2.A. Prong 1: Lossless compression with activity-adaptive recording front-end: We design a lossless compressor and windowed serializer that exploit the statistical structure of neural signals (1/f-like spectra for LFP and sparse, bursty spikes), yielding small inter-sample differences for much of the time [32]. The compressor works in concert with an activity-adaptive front-end so that, when neural activity is low, both the produced data volume and the front-end power are reduced; when activity rises, fidelity and throughput scale up. This event-aware approach aligns with recent event-driven neural interfaces [33].

1.2.2.B. Prong 2: Energy-efficient, inherently asynchronous IR-UWB transmission: We employ impulse-radio UWB to emit short, duty-cycled RF pulses only when symbols are present, avoiding the overheads of continuous carriers and high-Q filtering typical of narrowband links. Properly shaped and time-hopped pulses achieve low pJ/bit energy while meeting spectral-mask limits for short-range telemetry [9-10],[34].

1.2.3. Concrete goals:

(i) Demonstrate lossless compression that preserves bit-exact neural data under real-time deadlines while reducing TX payload.

(ii) Realize a programmable IR-UWB transmitter whose activity and output power scale with information content, targeting pJ/bit-class efficiency at Gb/s aggregate throughput within regulatory limits.

(iii) Integrate both prongs to show end-to-end energy savings that translate directly to higher scalable channel counts.

1.3. Design Considerations

1.3.1. Narrowband vs wideband communications

Traditionally, narrowband systems have dominated the communications industry due to its reliability to transmit information over the air across large distances. Narrow band systems produce a continuous sinusoid in the time domain to concentrate the signal power within a small bandwidth and modulates the signal by changing its amplitude, frequency, and phase to communicate different symbols that represent sequences of bits.

In contrast, Impulse Radio Ultra Wide-Band (IR-UWB) systems, spread energy across a large portion of spectrum (typically > 500 MHz) by producing RF pulses rather than continuous sinusoids as illustrated in Figure 1.2. Due to the larger bandwidth, it can transmit at much higher data rates compared to narrowband systems and consumes less average power due to its bursty nature. By spreading its signal power to larger bandwidths, it can reliably communicate at a high data rate at short ranges making it the best fit for intracortical implant radio transmitters.

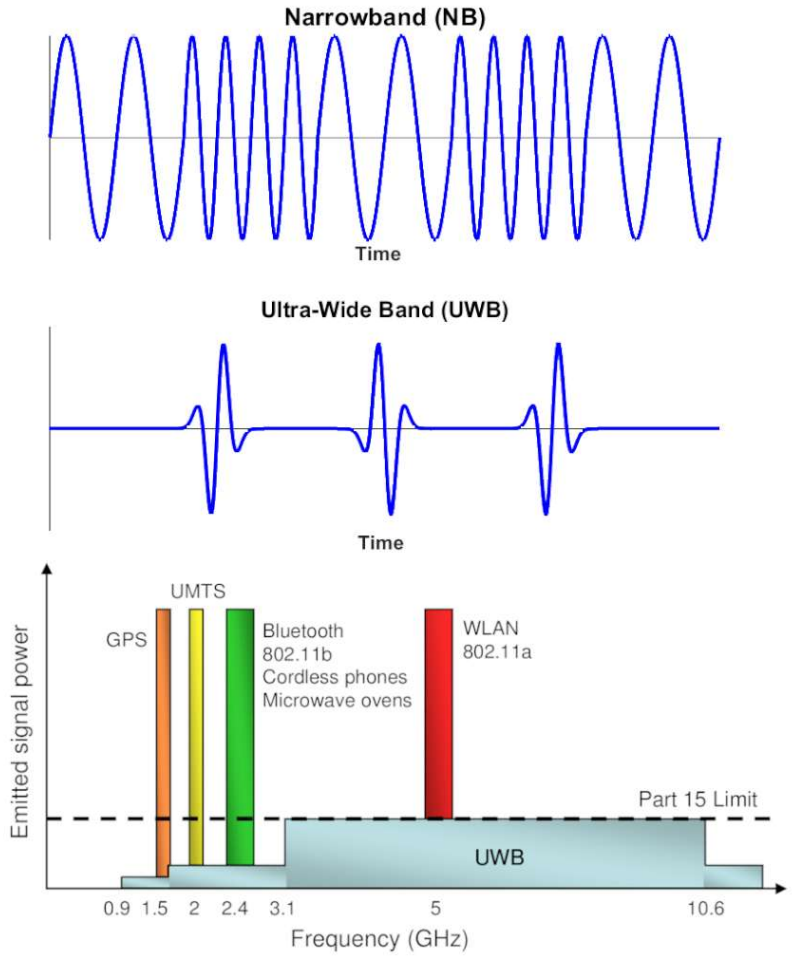


Figure 1.2: Narrow Band vs Ultra Wide Band in Time and Frequency Domain [35]

In 2004, the Federal Communications Commission (FCC) amended its rules to permit new wideband unlicensed devices and authorized the deployment of ultra-wide band technology [36]. It released provisions to limit the effective radiated isotropic power (ERIP) of UWB devices namely to regulate its interference with other existing narrowband technologies such as Global Navigation Satellite System (GNSS), Wi-Fi, Bluetooth, etc.

1.3.2. Application-Level Considerations

At the application level, the design of an intracortical implant with a UWB transmitter must align with the functional needs of neuroscience and clinical practice, ensuring the system delivers meaningful insights while remaining safe and practical for long-term use.

Given the state-of-the art probes now aim to record from more than 1000 channels [37-38] the target capacity is set accordingly to 1000 channels. With each channel sampled at 20-30 kSps and 10-bit resolution, the resulting data rate is approximately 300 Mbps at the minimum. However, to advance beyond current limitations and push the Moore's Law of Neural recording the design will aim to surpass the performance of existing IR-UWB intracortical transmitters, specifically the target data rate will be set to 1.8 Gbps.

The objective of the transmitter will be to communicate the raw intracranial EEG (iEEG), specifically electroencephalography (ECoG) data, over the air for long-term neural data acquisition in real world unconstrained environments. Such capability is particularly relevant for the development and validation of algorithms for seizure detection and long-term neurological monitoring to verify the patient's condition and the effectiveness of stimulation in patients with intractable epilepsy [39 - 41]. The ultimate goal of such a transmitter would be to enable further development of neurological monitoring solutions for many different applications that require the recording, transmission, and analysis of high channel count wireless neural recording solutions.

As the radio transmitter's intended location is to be within a human head, safety regulations must be obeyed. Specific Absorption Rates (SAR) limit the amount of electromagnetic energy is safe for human exposure as electromagnetic radiation absorption causes tissue to increase in temperature. Specifically for systems between 100kHz and 6 GHz, the maximum SAR is 1.6 W/kg

in the head averaged over 1 gram of tissue [42]. If the device is in direct contact with the tissue, then the total output transmit power must be below 1.6 mW.

In practice, SAR compliance is verified in tissue-equivalent media with realistic antenna loading; we therefore co-design pulse width, PRF, and PA drive to satisfy both spectral masks and average EIRP limits while meeting BER. Receiver sensitivity and antenna gains define a link budget that, for sub-10-cm ranges through tissue/air, is compatible with sub-milliwatt average radiated power when UWB pulses are properly shaped and time-hopped. Although within strict regulations and rules, the overarching goal is to enhance the energy efficiency of intracortical transmission, with the system striving to outperform the current state-of-the art efficiency benchmark of 2.3 pJ/bit [9].

1.3.3. System level considerations

System level considerations focus on how different functional blocks, such as signal acquisition, compression, pulse generation, and wireless transmission, integrate to meet performance reliability, and safety requirements in an implant with a UWB transmitter.

1.3.3.a. Architecture

The top-level architecture of the envisaged implant is shown in Figure 1.3. To record and transmit data from >1000 channels working in parallel, serialization of the data must occur so that it can be transmitted over air. To serialize the data, it first needs to be split apart into chunks or “windows” to make large number of channels communicable within a short period of time. After the first window is recorded, the transmitter must finish communicating the data within that window before the end of the next window occurs. The serialization will incorporate shift registers that shift the

bits generated by the channels ADC. After shifting the bits recorded within the window, the shift register will store the data, for processing, compression, and transmission, and continue to shift the next window's set of bits.

After serialization, the data will be compressed to reduce the overall number of bits to send over air, thereby reducing the power required to transmit all the data. It can do this by determining where redundancy exists within the data and aims to compress it without losing any information. This compression algorithm should complete within the time it takes to record a single window and not pose a large power overhead.

After compression, the data needs to be to transmit over air therefore it should modulate the pulse generator circuit to produce the corresponding symbol over air. It does this by triggering the generation of a UWB pulse fed to the antenna.

To handle PVT and load variation, the digital controller exposes programmable knobs (pulse width/shape, amplitude steps in the PA, modulation order, and PRF). Calibration routines sweep these parameters against a known test pattern to ensure spectral compliance and maximize energy per successfully received bit.

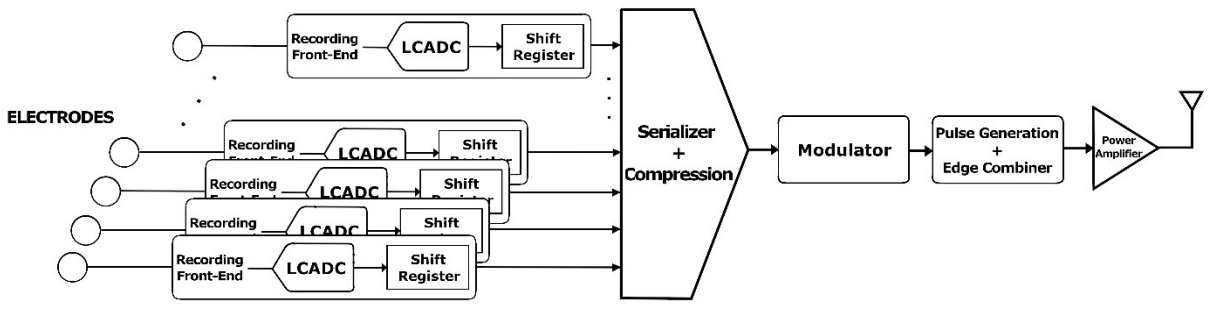


Figure 1.3: Top Level Diagram of Neural Implant with an UWB transmitter.

1.3.3.b. Power Budget and Physical Size

The size of the implant must be limited to reduce the invasiveness of the surgery required to apply the implant to the brain and to assure that it can fit between the cortex and the surrounding layers, resulting in a thickness of 1 to 3 mm. [43] The size of the antenna is heavily dominated by the coils or antennas present to provide wireless power or wireless communication to the device, therefore the size of the implant can vary from 0.24 to 100 mm^2 [44 - 45]. In particular, the antenna used for high-data-rate UWB telemetry plays a critical role, as its geometry determines achievable bandwidth, radiation efficiency, and impedance matching within the lossy tissue environment. These requirements mean that the transmit antenna is often one of the most significant contributors to the overall lateral area of the implant, directly influencing its footprint and integration constraints.

Thermal and safety considerations further constrain allowable size. A larger device can, in principle, spread heat more effectively, but it also increases surgical invasiveness and immune response risk. Conversely, very small implants reduce tissue displacement but demand much higher power efficiency, as less surface area is available for heat dissipation. Because the transmitter is the dominant power consumer, achieving pJ/bit-class efficiency is essential to keep overall temperature rise within medically safe limits.

The target power budget will be based on the amount of power that can reasonably be expected to be delivered to the implant likely through wireless powering. Specifically, Near-Field Inductive Coupling links have proven to have high efficiency [46 - 55] operates within SAR limits, and small. The reported safe power throughput ranges from 19 mW to 82 mW. [56] As the transmitter consumes around 70% of the power budget on average [6 - 10] solutions increasing the energy

efficiency of wireless transmission is necessary to scale channel count further. Given these bounds, a practical total system budget of a few-tens of mW implies transmitter average power in the single-digit mW range at Gb/s rates—i.e., pJ/bit-class operation. This reinforces the need for compression and event-driven telemetry

1.3.3.c. Modulation and Pulse Generation

Selecting the modulation scheme for the neural implant's transmitter requires analyzing existing options and evaluating their impact on the required transmit power. Popular schemes in an IR-UWB architecture include Pulse Amplitude Modulation (PAM), Pulse Position Modulation (PPM), and Phase Shift Keying (PSK) which is shown in Figure 1.4. By changing the amplitude, position, and/or phase of the pulse, the receiver can de-modulate the symbols and recover the transmitted bits in each symbol. The modulation order (N) describes the number of bits transmitted per symbol; a modulation order of N requires that 2^N different levels of (amplitude, phase, or position) be generated at the transmitter and demodulated at the receiver. As the modulation order increases, the data rate increases proportionally. This is a common strategy to increase the throughput of the transmitter but as the modulation order increases the required Signal-to-Noise Ratio (SNR) also increases. A greater SNR at the receiver requires a higher signal power from the transmitter meaning that a balance between modulation order and transmitter power must be established depending on the application of the transmitter.

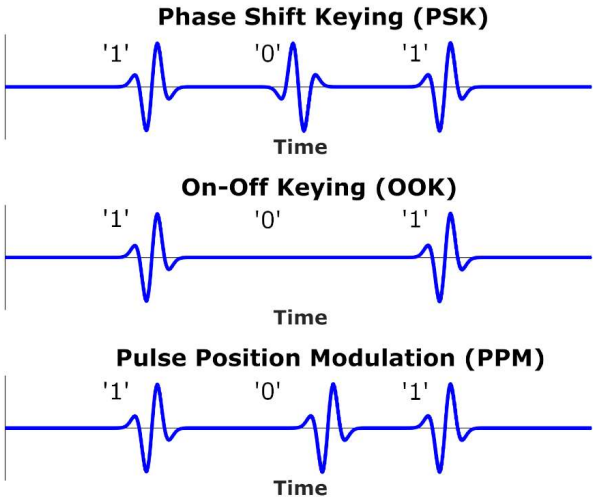


Figure 1.4: An illustration of PSK, OOK, and PPM modulation schemes

Two main architectures are commonly used for pulse generation in IR-UWB transmitters: oscillator and edge combination. The oscillator-based architecture uses an oscillator that can start and stop within a short time, less than 2 ns. The advantage of an oscillator-based architecture is that it can create different frequencies and phases reliably. Edge combination relies on logic gates to combine short pulses together; it can be made entirely of digital circuits to generate the sub pulses and combine them to create an UWB pulse. The advantage of edge combination is that it can produce UWB pulses with very little power but cannot reliably create multiple phases or frequencies. Based on these observations, architectures favoring low-order modulation benefit from using edge combination, where high order modulation architectures would benefit the use of an oscillator for pulse generation.

1.3.3.d. Communication link

The communication link of a neural implant must balance range requirements, the characteristics of the channel, and regulatory constraints. Since the implant operates in a biological tissue the link

must ensure a reliable data transfer over short ranges while minimizing power consumption. Additionally, the system must comply with FCC regulations on ultra-wideband emissions, which set strict limits on transmit power and spectrum. The range can be determining the minimum and maximum path the IR-UWB transmitter would require communicating over. The minimum would be the shortest distance between the biological tissue between the outer layer of the brain and the scalp (about 1.1 cm through tissue). The maximum distance expected transmitting distance will be set to 10 cm through air (plus 1.1 cm through tissue) based on previous works. Finally, to ensure accurate recovery of neural data sent over air the signal needs to have a low bit error rate (BER) and high fidelity. Based on requirements presented in previous works, a BER target of 10^{-6} will be set.

1.3.4. Circuit Level Considerations

To implement the transmitter design, the 180nm TSMC process node will be used due to its availability, cost, and applicability in RF design. In an IR-UWB transmitter, the three functional blocks are a modulator, pulse generator, and power amplifier. Their specifications, requirements, and constraints must be defined to begin the design process. The modulation circuit should be tunable to overcome variations in process, voltage, and temperature (PVT) and to meet the BER requirement. The pulse generator must be able to consistently create an UWB pulse that meets the FCC spectrum requirements and reduces variations in center frequency and bandwidth. The main goal for the pulse generator design will be to produce a reliable UWB pulse whilst using the smallest amount of power per bit. The power amplifier should provide more power to the antenna to overcome path loss and meet the SNR requirements at the receiver. Once the minimum amount of power at the transmitter is determined, voltage and current can be designed for.

We also budget for layout-parasitic-aware tuning (e.g., programmable delay lines and switchable capacitance in the PA/PG) and include hooks for post-silicon calibration to counter PVT and temperature drift

1.4. Previous Works

An analysis of previous works can be made to better understand the impact of the contributions made in this thesis. By examining the status quo for EEG data compression methodologies and IR-UWB transmitters for neural implants, a base line can be established to examine the contributions presented in this thesis.

1.4.1. State of the Art Examples

1.4.1.a. A 49.8 mm^2 Fully integrated, 1.5m Transmission-range high-data-rate IR-uwb transmitter for brain implants

Ding et al. (CICC 2024 [57]) presented a fully integrated IR-UWB transmitter for neural implants that achieved a 49.8 mm^2 and a transmission range of up to 1.5m, surpassing prior works limited to centimeter scale distances. The transmitter employs on-off keying (OOK) with Phase Shift Keying (PSK)-based scrambling to supress discrete spectral tones and comply with FCC regulations. A ring-oscillator-based wideband PLL generates quadrature LO signals, driving a pulse generator that produces 2ns OOK pulses shaped by a programmable delay line for improved spectral efficiency. The design (shown in Figure 1.5) features a switched-capacitor power amplifier (SCPA) in a fully differential configuration, eliminating the need for an off-chip balun. A 14 mm^2 meander dipole antenna was co-designed with the PA, allowing direct impedance matching and

avoiding an external matching network. Fabricated in 65 nm CMOS, the chip delivers around 1.4 dBm output power and supports data rates up to 800 MB/s. Wireless experiments demonstrated reliable operations with BER below 10^{-4}, achieving 500 Mb/s at 100 cm and 375 MB/s at 150 cm. [57] This work represents a state-of-the-art solution, combining compact size, high data rate, and meter-scale transmission range for implantable applications.

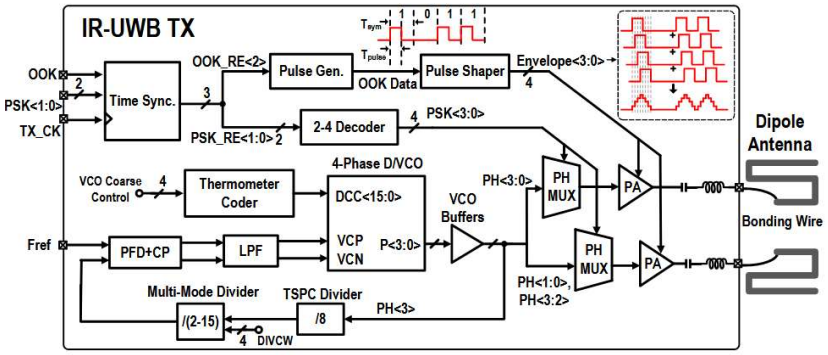


Figure 1.5: Architecture implemented by Ding et al. (CICC 2024) [57]

1.4.1.c. An energy-efficient and high-data-rate IR-UWB transmitter for intracortical neural sensing interfaces

Song et al. (ISSCC 2022 [9]) introduced an energy-efficient IR-UWB transmitter targeting intracortical neural sensing interfaces, achieving a data rate of 1.66 Gb/s with an energy efficiency of 5.8 pJ/bit. The design (shown in Figure 1.6) employs a hybrid impulse modulation scheme that combines Ook with binary phase modulation (BPM), enabling high throughput while maintaining spectral efficiency. A pulse generator with tunable width produces UWB pulses that are shaped to meet regulatory spectral masks. The transmitter architecture integrates an SCPA for efficient energy delivery. Fabricated in 65 nm CMOS, the chip achieves a compact size while supporting Gb/s operation. Wireless measurements verified performance in intracortical implant scenarios, with the hybrid modulation improving both data rate and spectral compliance. [9] Compared to

earlier works, this design emphasizes ultra-high throughput for large-channel-count neural recording systems. Overall, it represents a significant advancement in balancing energy efficiency and transmission speed for implantable UWB telemetry.

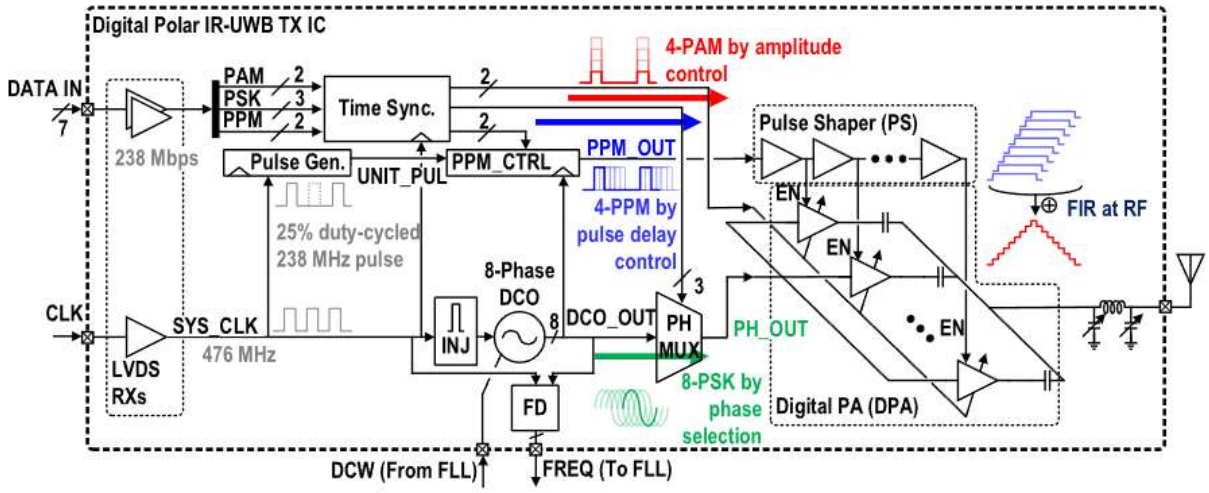


Figure 1.6: Architecture implemented by Song et al. (ISSCC 2022) [9]

1.4.1.b. Event-based spatially zooming interface IC with 10nw/input reconfigurable-inverter fabric and input-adaptive quantization

Xu et al. (ISSCC 2025 [58]) presented an event-based spatially zooming neural interface IC designed to address the scalability and energy bottlenecks of high-density neural implants. The 64-input chip (architecture shown in Figure 1.7) exploits neural spike sparsity across space, time, and amplitude to dynamically switch between lo-power spike detection, high-resolution spike recording, and artifact tolerant modes. A reconfigurable inverter-based front end dissipates only 10 nW per input in detection mode, while adaptive reconfiguration enables continuous-time ADC operation for recording with enhanced effective resolution. Non-uniform sampling and quantization further boost ADC precision and reduce required data rates, enabling compact digital

filtering without analog anti-aliasing. The system integrates wireless telemetry at 915 MHz with an XOR-based transmitter, achieving up to 52 Mb/s at 440uW, scalable down to 0.2 Mb/s at 1.7 µW. Experimental results demonstrated in-vitro spike recording with effective bit resolution up to 14 bits. [58] This work highlights a scalable, event driven approach to neural interfacing, balancing ultra-low power consumption with flexible neural data acquisition.

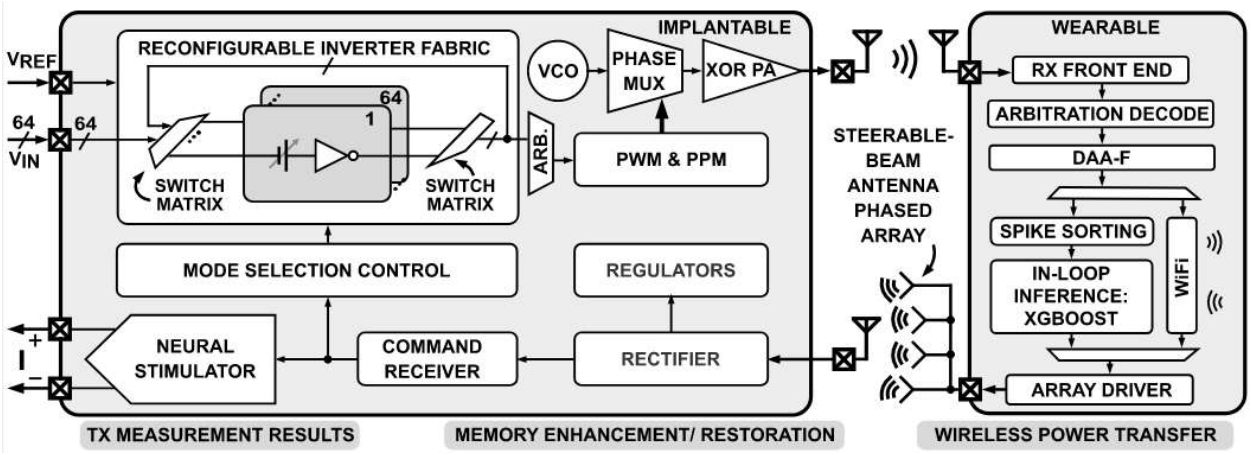


Figure 1.7: Architecture implemented by Xu et al. (ISSCC 2025) [58]

1.4.2. Technical gap and comparison

Recent advancements in IR-UWB transmitters for neural implants increase data rate by increasing the modulation order thereby encoding more bits per symbol transmitted. As this requires a higher SNR at the receiver to maintain a given BER, this solution requires more power transmitted over air. This strategy cannot be scaled indefinitely as the constraints on spectral power density will force either the Pulse Repetition Frequency (PRF) to be reduced or the energy per pulse to be constrained, either will limit the maximum data rate achievable by a traditional IR-UWB transmitter.

For this reason, new methods of encoding neural data into IR-UWB pulses is required to further scale the effective data rate of the neural implant. By conducting recording in an activity-adaptive fashion, i.e., using an LC-ADC at the front-end, an activity adaptive system will be made where significantly lower number of bits are produced and transmitted by an IR-UWB transmitter using a low-order modulation, without reducing the effective data rate. Additionally, we will leverage the sparsity of LC-ADC output bitstream and further compress (lossless) the data by up to 86% before transmission. In such a system, the power consumption will scale based on how "active" the input data is, which is significantly more energy efficient than a conventional ADC. To further increase the energy efficiency of the data compressive IR-UWB transmitter an edge combination-based architecture will be employed due to its superior energy efficiency compared to oscillator-based architectures.

This thesis therefore departs from solely order-raising to an information-aware approach: reduce bits first, then transmit them with minimalist UWB pulses. We quantify the operating region where this yields superior pJ/bit at target BER versus recent Gb/s designs ([10], [15], [18 - 19],[59, p. 21]).

Table 1.1: Comparison table of state-of-the-art IR-UWB transmitter works and Target Performance

Ref.	[58]	[60]	[57]	[10]	[34]	**Target Performance**
Pub.	ISSCC '25	CICC '25	CICC '24	ISSCC '23	ICECS '24	CICC '26 (SUB)
Tech. (nm)	65	65	65	40	28	180
Architecture	Oscillator	Oscillator	Oscillator	E.C.*	E.C.*	E.C.*
Modulation	PWM & PPM	E-PWM & PSK	OOK w Asym. Envelope	D16PPM+PWM +DBPSK	OOK	PPM

BER	$9x10^{-5}$	10^{-3}	10^{-4}	10^{-4}	N/A	10^{-6}
Data Rate (Mbps)	52	1800	100-800	1800	40	> 1800
3-dB BW (MHz)	N/R	1200	2900	2900	2000	500
Center Frequency (GHz)	0.92	8	4.65	4.65		4
Power Consumption (mW)	0.44	28.2	13.2	4.09	0.09	< 10 mW
Energy Consumption (pJ/bit)	8.4	15.7	16.5	2.3	3.8	< 2
Supply (V)	0.7 – 3.3	1	1.2	1.2	1.2	1.8
FoM (pJ/b/m)	N/R	N/R	26.4	N/R	N/R	< 20

* E.C. – Edge Combination.

1.5. Thesis Organization

Chapter 2 introduces the proposed lossless compression scheme and its integration with an activity-adaptive recording front-end. It explains how the algorithm leverages the statistical properties of neural signals to reduce data volume, describes its hardware realization, and evaluates compression performance, energy efficiency, and suitability for high-channel-count implants.

Chapter 3 presents the design and implementation of the impulse-radio ultra-wideband transmitter. It covers circuit architecture, pulse generation and modulation strategies, and power-efficient design techniques, followed by simulation, layout, and measurement results.

Chapter 4 shows the measurement setup and the performance results of the compression algorithm and UWB transmitter. It introduces the receiver architecture used to extract performance metrics and discusses the performance results.

Chapter 5 concludes the thesis by discussing the impact of the contributions presented in the thesis and offers insights into the future works related to this work.

Chapter 2:

GCD-Based Encoding within Input-Adaptive Recording Architecture for Lossless Neural Data Compression

As discussed in previous chapter, data compression is essential in modern wireless communication systems, particularly when transmitting large volumes of data over bandwidth- or energy-constrained channels. These algorithms aim to reduce the size of the transmitted data (e.g., by identifying and removing redundancy), thereby decreasing the number of bits required to represent the information. For ultra-low-power devices such as intracortical brain implants, compression becomes even more critical. Reducing the data's entropy directly translates into lower transmission energy, enabling more efficient and longer-lasting operation.

The compression algorithm must preserve the fidelity of the neural signal while reducing the volume of transmitted data. It should incur minimal power overhead, as energy efficiency is a critical constraint in implantable systems. Low latency is also necessary to maintain real-time neural signal processing and communication. In addition, the implementation should be hardware-efficient, occupying a limited area and computational resources to remain practical for integration in a neural implant. Data compression enables transmission power to adapt to the signal’s level of activity. This is especially useful in cortical recording where long periods of low activity are common. By being input adaptive, the power of the implant can scale proportionally with presence of data meaning that energy usage can be reduced during these long periods of low activity.

Compression and input adaptivity can be applied at various stages sampling/quantization, digital processing, or wireless transmission. Ideally an end-to-end framework is desirable, where resource consumption across all stages adapts to the input signal's activity level. In this chapter, we will first present a recording front-end with inherent input adaptivity, allowing compression during acquisition. We will the introduce our data compression algorithm for further compression of the acquired signals, designed specifically to complement both the front-end and the UWB transmitter.

2.1. Level Crossing ADCs for Neural Recording Front Ends

2.1.1. Motivation

A major research objective in the design of neural recording analog front ends (AFEs) is to improve the energy efficiency of signal digitization. Traditional Nyquist-rate analog-to-digital converters (ADCs) generate samples at fixed intervals, regardless of whether the signal is changing significantly. This results in redundant data during periods of low activity, which is common in physiological signals, and in wasted power for both digitization and subsequent data transmission.

Level-Crossing ADCs (LC-ADCs) have emerged as a promising alternative due to their input-adaptive operation. Instead of sampling periodically, an LC-ADC generates a digital output only when the input signal crosses predefined voltage thresholds separated by the quantization step size, V_{LSB}. In other words, the converter produces samples only when meaningful changes occur in the signal amplitude. This event-driven approach naturally adapts the sampling activity to the signal dynamics, resulting in fewer samples during quiescent periods and higher activity during rapid transitions.

This property has been particularly advantageous in applications such as electrocardiogram (ECG) recording, where long stretches of relatively flat baseline are punctuated by sharp features such.

The inherent sparsity of the ECG waveform makes it well suited to LC-ADC sampling, enabling significant reductions in data rate and power consumption without sacrificing diagnostic quality. Given the similarities in sparsity between ECG and certain neural signals, LC-ADCs are now being actively explored for neural recording applications. Cortical signals, for example, often contain extended low-activity intervals interspersed with bursts of spiking or oscillatory activity. By exploiting this structure, LC-ADCs can provide input-adaptive digitization that not only reduces overall data volume but also lowers the energy cost of acquisition and transmission, making them highly attractive for scalable, ultra-low-power implantable neural prostheses.

2.1.2. Principles of Operation

As shown in Fig. 2.1., it does this by detecting when the input signal crosses predefined quantization levels separated by V_{LSB}. Each crossing triggers the control logic, which updates the reference threshold through a feedback DAC so that the quantization window follows the input. This event-driven mechanism makes the sampling activity proportional to the signal's dynamics: fewer samples are generated during low-frequency or low-amplitude intervals, while rapid transitions are tracked more densely. A key performance parameter is the time granularity (t_{gran}), which represents the loop delay between detecting a crossing and updating the reference. This sets the maximum slope the converter can faithfully record.

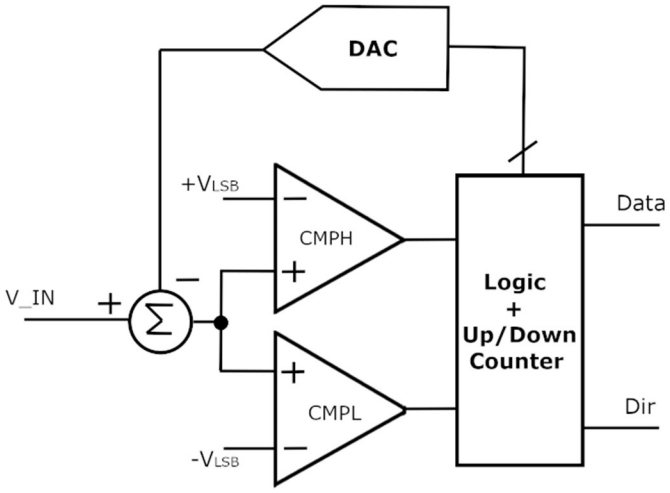


Figure 2.1. Block diagram of a typical LC-ADC

The encoded neural signal is represented using two signals: DATA and DIR. The DATA signal captures when level-crossing occurs, and the DIR signals encodes the respective level-crossing direction. The output can also be represented as UP or DOWN, where the level crossings trigger a pulse on either UP or DOWN depending on the direction as shown in Figure 2.2.

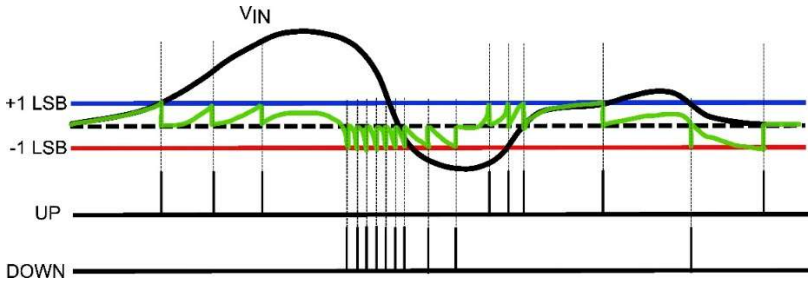


Figure 2.2: LC-ADC signal representation

2.1.3. Problem with Current LC-ADC Data Processing/Transmission

Although the raw asynchronous bitstream produced by the LC-ADC captures signal activity efficiently, it is not typically used directly for processing or transmission. Instead, most systems convert it into a reconstructed synchronous multi-bit binary format by encoding both the direction of each crossing and its timing relative to fixed intervals. This conversion, however, reduces

efficiency: timing information must be explicitly encoded, and the serialized stream can approach the size of conventional Nyquist-rate data. As a result, the very adaptivity that makes LC-ADCs attractive is partly undermined, particularly in ultra-low-power applications where minimizing overhead is critical.

2.2. Sparsity in LC-ADC representation of ECoG Signals

Figure 2.3 illustrates the spectrum for 1-hour ECoG recording for 6 different patients sourced from the SWEC-ETHZ iEEG Database [61]. The intracranial EEG (iEEG) signals between 1 and 100 Hz exhibit a $1/f^3$ spectral distribution, meaning that signal power decreases exponentially as frequency increases. The lower-frequency components, such as delta and theta bands, tend to dominate the signal with relatively high amplitudes, while higher-frequency components like beta and gamma bands have much lower amplitudes. This results in fewer level crossings at higher frequencies. For this reason, it can be said that ECoG data represented by an LCADC are inherently sparse, producing long sequences of zeroes due to the low rate of level crossings in slowly varying neural signals.

In classical signal processing, sparsity is defined as few non-zero coefficients when the signal is represented in a specific domain such as frequency or wavelets also known as “transform sparsity”. This makes it so that the vector representation of the signal (which would be used for signal reconstruction) contains few non-zero coefficients. The sparsity being shown in the LC-ADC representation of ECoG is not this transform-domain based sparsity but sparsity in the time domain. The LC-ADC representation of ECoG data contains long sequences of zeros due to the slow changing neural signal meaning that the signal is sparse in the amount of level crossings present in a window of time.

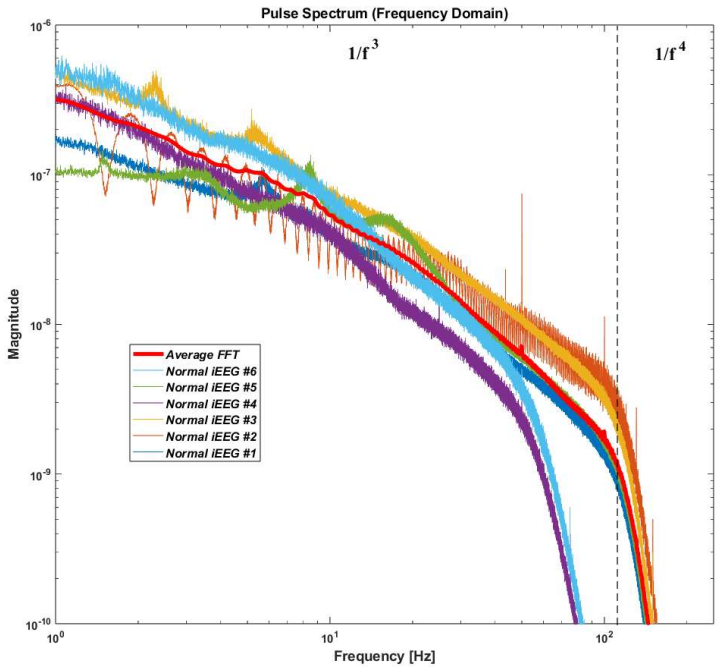


Figure 2.3: Frequency Spectrum of 1 hour of iEEG signals from 6 patients

This sparsity is reflected in the digital representation as long sequences of zeros indicating no level crossing interspersed with samples representing actual events. Figure 2.4 illustrates the distribution between the number of level crossings and the number of no crossing occurrences that happen within a 6-minute ECoG recording (using a t_{gran} of 190 µs) showing that over 97% of the signal produces no level crossing which is very significant because if the transmitter were to transmit each bit and consume power transmitting these long sequences of zeros, over 97% of the energy spent by the transmitter would convey no new information to the receiver and would severely penalize the scalability of a multi-channel LC-ADC based recording front end. While this sparsity preserves important temporal information, it also creates opportunities for data compression, since without compression most of the transmitted bits would contain no new information as it is composed of long sequences of zeroes.

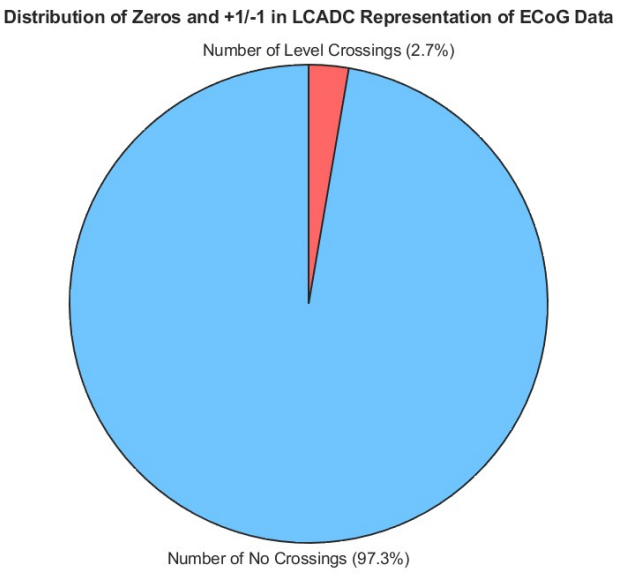


Figure 2.4: Pie Chart exhibiting the level of signal activity within a 6-minute recording of ECoG

In a multi-channel system, each channel generates its own sparse stream of LCADC outputs. When these streams are combined or multiplexed, the overall data volume increases substantially even though much of it consists of redundant zeros. Without compression, the cumulative bandwidth and power requirements grow linearly with the number of channels, posing a major bottleneck for low-power wireless transmission. Therefore, leveraging sparsity across channels through efficient compression becomes essential to maintain energy efficiency and minimize latency in high-density neural recording systems.

2.3. Greatest Common Divisor (GCD)-Based Encoding

In systems with many neural recording channels, transmitting raw data directly can quickly exceed bandwidth and power constraints. A practical solution is to packetize and serialize the data from multiple channels into a unified stream, enabling transmission over a single frequency band. This serialized stream can then be compressed before transmission to reduce both the required

bandwidth and the energy per bit. This process of serializing the data and transmitting it must happen before the next recording window is finished

The LC-ADC outputs data in the form of discrete level changes, encoded as +1 for an upward crossing (an increase by one LSB), -1 for a downward crossing (a decrease by one LSB), and 0 for no change. This results in a ternary signal that can be transmitted with a modulation order of 1.5 bits per symbol. However, due to the sparse nature of neural signals particularly in high-frequency bands where fewer crossings occur, most of the serialized data consists of long sequences of zeros. These sequences represent periods of inactivity and present a clear opportunity for compression.

We propose a Greatest Common Divisor (GCD)-based compression algorithm to address this by encoding the timing between level crossings more compactly. Within each packet, the algorithm calculates the GCD of all zero run lengths, then replaces each run of zeros with a reduced sequence whose length is the original run length divided by the GCD. For example, if a sequence contains 8 consecutive zeros and the GCD is 2, it will be compressed into four zeros, each representing a time step of 2. An entirely inactive packet (comprising only zeros) can be represented by a single zero, as the resulting GCD is the size of the packet. At the receiver end, the original timing is recovered by multiplying the length of each zero sequence by the shared GCD value, as illustrated in Figure 2.5.

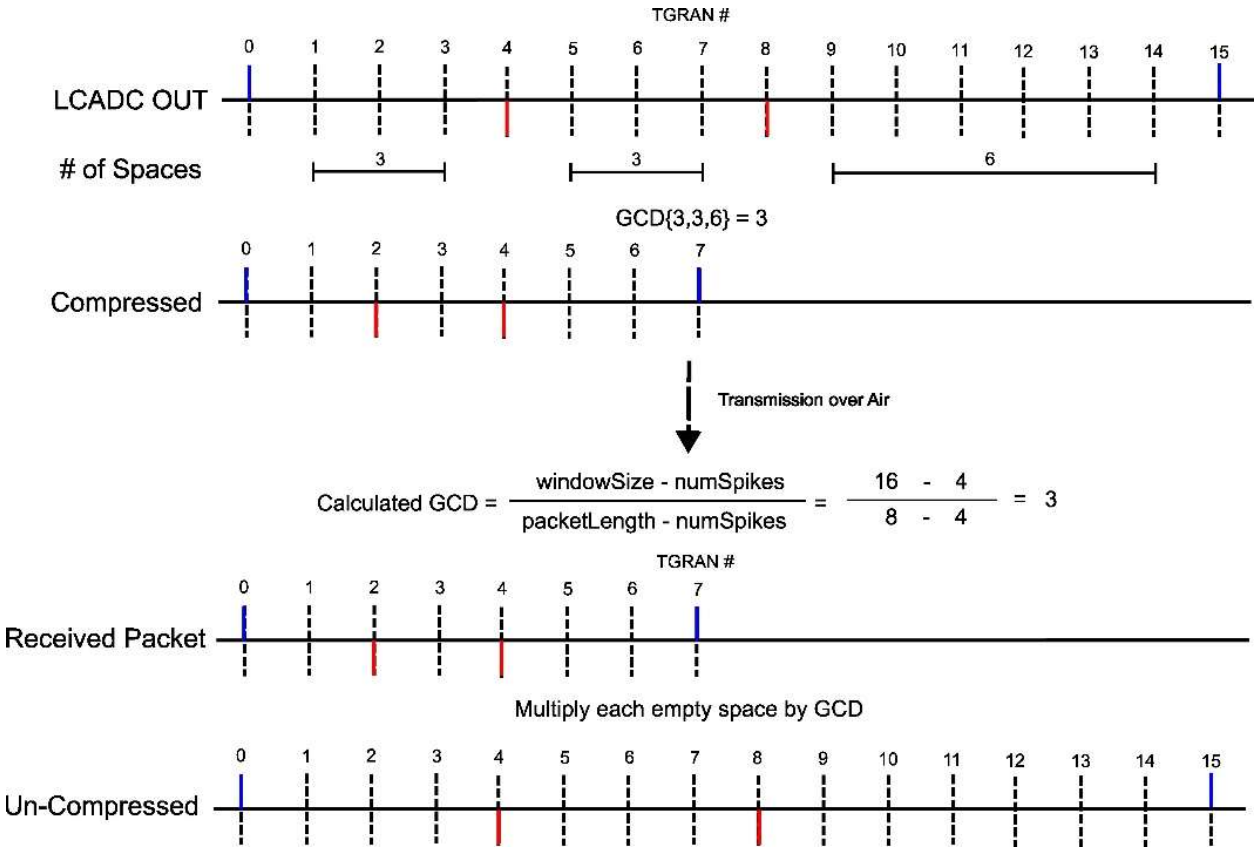


Figure 2.5: GCD Algorithm Compression and Decompression Visualization

This method preserves the temporal structure of the level crossing events while significantly reducing the number of bits transmitted. The algorithm's efficiency improves with higher sparsity and greater packet lengths, and it requires minimal additional computation at the receiver for reconstruction. Importantly, the information required to decompress the packet is embedded within the data being transmitted. The receiver requires the number of spikes present in the packet, the compressed length of the packet, and the original window size. It uses the formula shown in Figure 2.5 to recover the GCD of the packet and uncompress the packet by multiplying each zero between data bits by the GCD which will restore the packet's original width. The functional behavior of the GCD compression algorithm was simulated in MATLAB and it was proven that windowSize of greater than 2 the compression algorithm works for all values between 0 and 2^windowSize values.

This compression algorithm detects redundancy inside of the LC-ADC representation of ECoG data based on the position of data bits within the packet. By moving the position of a data bit up or down the packet the effective calculated GCD can be increased. As shown in Figure 2.6, the GCD compression algorithm cannot compress a packet with {0,1,0,0,0,0,0,0,0,0,0,0,0,0,0,0} but if the '1' is moved with a stride of 1 to the left the GCD algorithm could compress it to {1,0}. This is an interesting phenomenon because when reconstructed at the receiver, the start and end of the recording window will be the same as if the original packet was transmitted. By moving the data bit and not removing it, the voltage at the start and end of the packet is preserved making it so that the change in voltage within that channel comes a TGRAN earlier or later. This version of the algorithm is technically lossy as it introduces errors in reconstruction but due to the small value of the tgran value (typically 190us is used for ECoG data) the error is minimal.

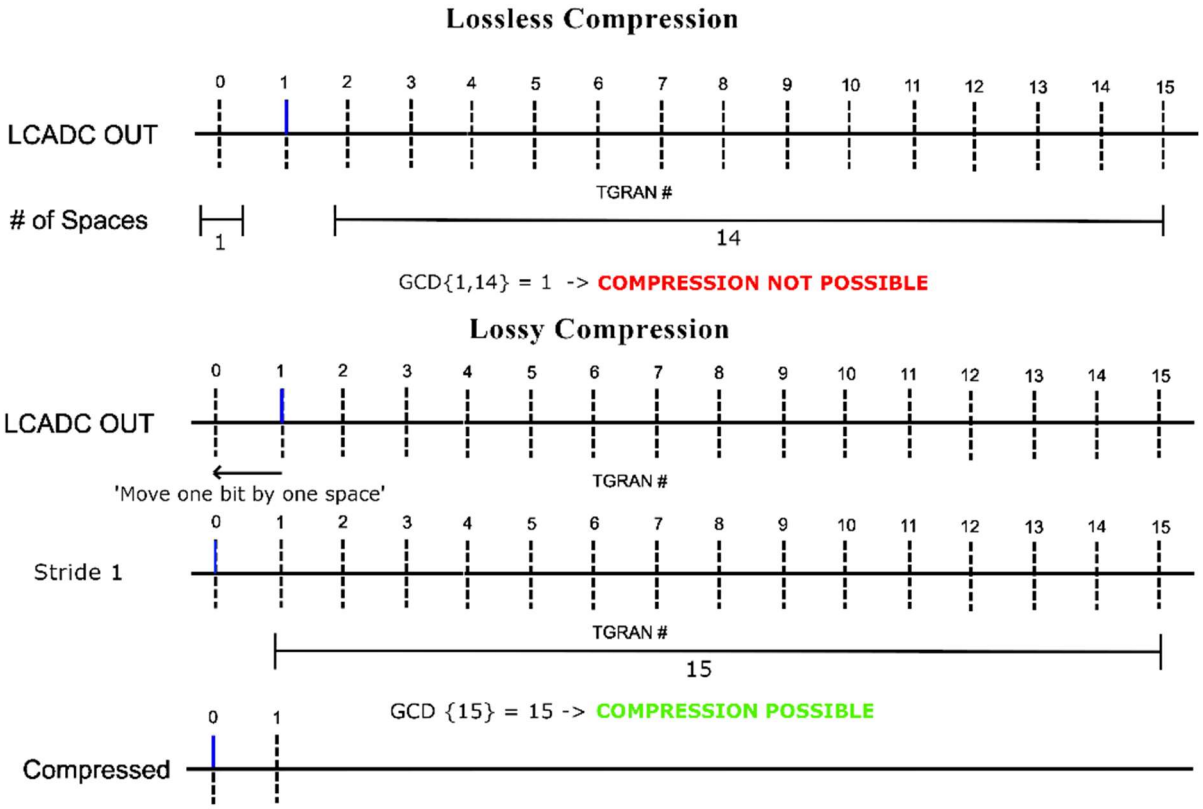


Figure 2.6: Lossless vs Lossy Compression Illustration

To implement this algorithm on-chip, a digital controller can handle the acquisition, compression, and serialization of the LCADC representation of the record ECoG data. Shift registers can acquire the data produced by the LCADC recording front end by shifting a set number of bits. Once full, the shift register can signal a GCD compression block to compress the contents of the shift register. Finally, the serializer can read the output of the GCD compression block and prepare the data to be fed to the transmitter. The GCD compression block can be implemented in two ways: a GCD calculator or a set of logic gates. The GCD calculator can implement the algorithm by recording the zero run lengths within the shift register and calculate the respective GCD from the array of zero length runs. Then it would write the shift registers contents into a separate register while reducing each zero run lengths by the GCD. This implementation requires a high-speed clock to process the calculations and write to registers. Alternatively, the GCD compression block can be implemented with only logic gates. By choosing a discrete set of GCD values that produce 99% of the compression ratio, the GCD compression block can simply detect if the packet matches a set of packets and write the respective compressed packet to the output registers. For example, 70% of the packets recorded are empty; the GCD for an empty packet would be the length of the packet itself. The resulting compressed packet is a single zero. The detector of this packet would be an N-input NAND, the logic gate would output a ‘1’ then the output would write a single zero to the output packet. As seen in Figure 2.8, the most prevalent GCDs (for a packet width of 16) are 15, 5, and 3. These GCDs represent 99% of the packets that can be compressed. Ultimately, the logic gate architecture is clockless therefore introduces very little latency, has an ultra-low power overhead, and can be implemented on-chip integrated into the controller for the transmitter digitally.

2.4. Analysis and results

A MATLAB-based performance analysis was conducted using ECoG data from the SWEC-ETHZ iEEG database, assuming a V_{LSB} of 7.6 μV and a loop delay of 190 μs for the LC-ADC the signals were translated to an LCADC representation. The compression algorithm was also implemented into MATLAB, it calculates the GCD of the packet within any packet length and produces the resulting compressed packet along with other performance metrics such as reconstruction success, relative compression ratio, etc. To analyze the functionality of the algorithm and determine the architecture of the digital implementation of the algorithm on-chip parameters such as window size and set of GCDs to use for lossless/lossy compression.

2.4.1. Recording Window Size or Packet Width

The first analysis sweeps the possible window sizes and calculates the resulting compression ratios. By sweeping the window size, the best resulting compression ratio can be determined and used in the on-chip implementation. As window sizes get smaller, the number of empty packets increases but due to the short recording window the transmitter will have to communicate the recording windows contents often. As window sizes get bigger, the overall compression ratio increases making window sizes, between 10 and 30, favorable. Past a window size of 30, the number of non-empty packets increase diminishing the compression ratio. The relationship between the number of pulses transmitted in a recording window is determined by Equation 2.1.

$$\text{Num. of Pulses per Recording Window} = \frac{\text{N}}{\text{CR} * \text{PRF}} \tag{2.1}$$

The Pulse Repetition Frequency (PRF) is the number of times an UWB pulse is generated per second, N is the size of the recording window, tgran is the minimum loop delay in the LCADC

system, and CR is the compression ratio. Tgran and PRF are metrics that are determined by maximum slope requirements of capturing ECoG data and the capabilities of the UWB transmitter, respectively. The N/CR factor however will be set by analyzing the effect of N on CR and their resulting ratio. By minimizing the N/CR ratio, the optimal value for N can be found to minimize the number of pulses required to be sent over the span of the recording window. By minimizing this value, the PRF and therefore the data rate required to transmit this data can be further reduced by achieving more efficient transmission of multi-channel ECoG data. As shown in Figure 2.7, the analysis revealed that a packet length of 16 bits achieves the optimal trade-off between compression ratio, complexity, and is conveniently a power of two meanings that it will scale well on-chip.

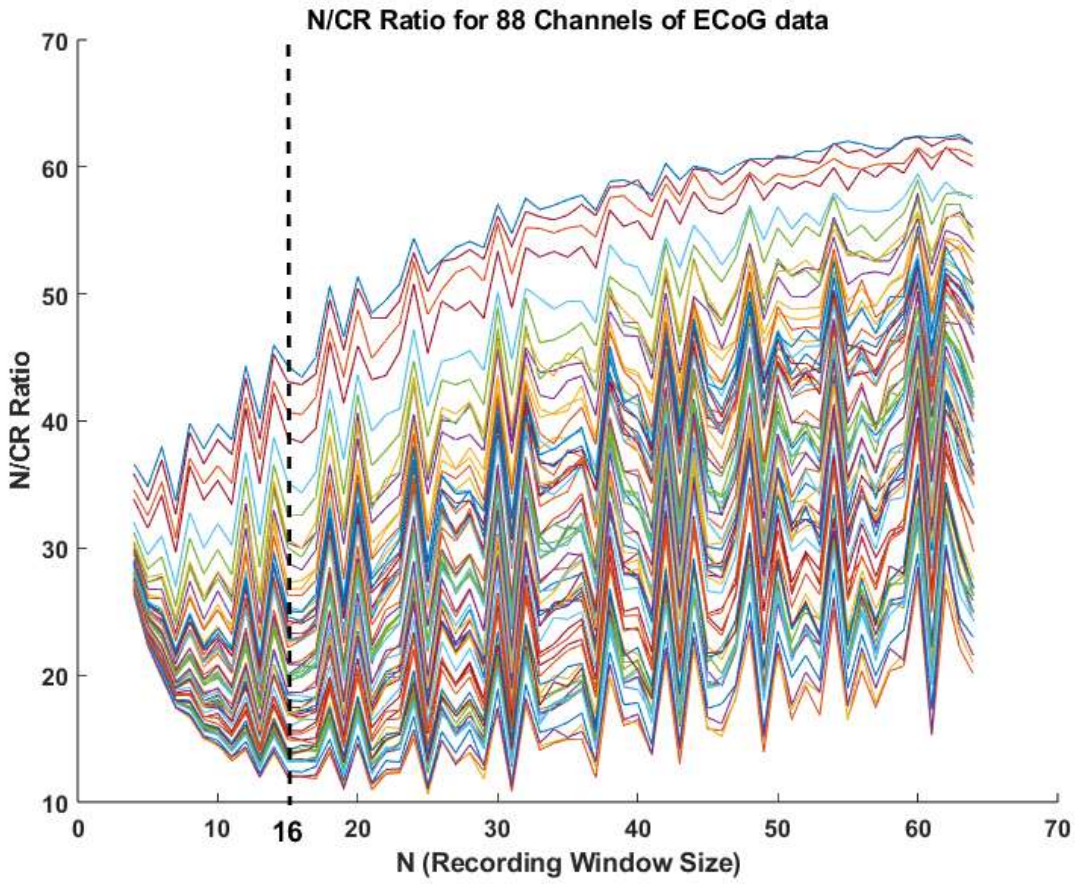


Figure 2.7: GCD algorithm's Compression ratio when window size is swept across 88 channels

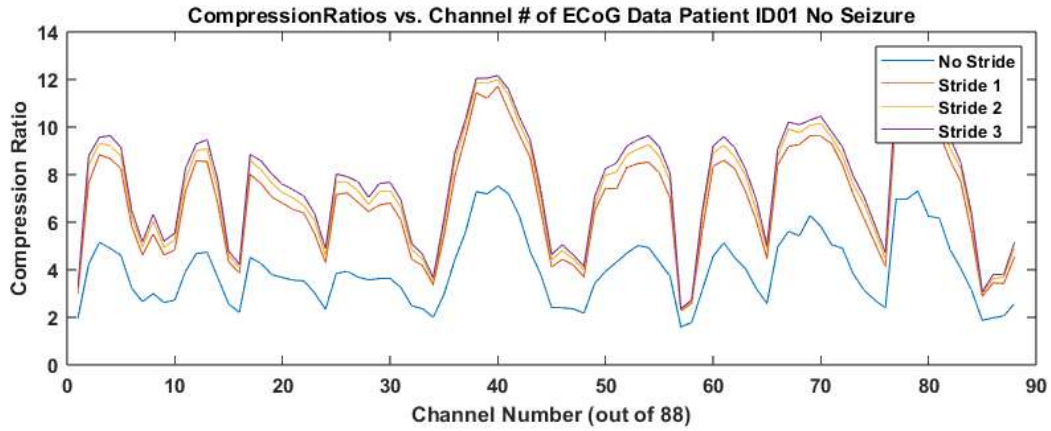
2.4.2. Compression Ratio Performance for Lossless/Lossy Algorithm

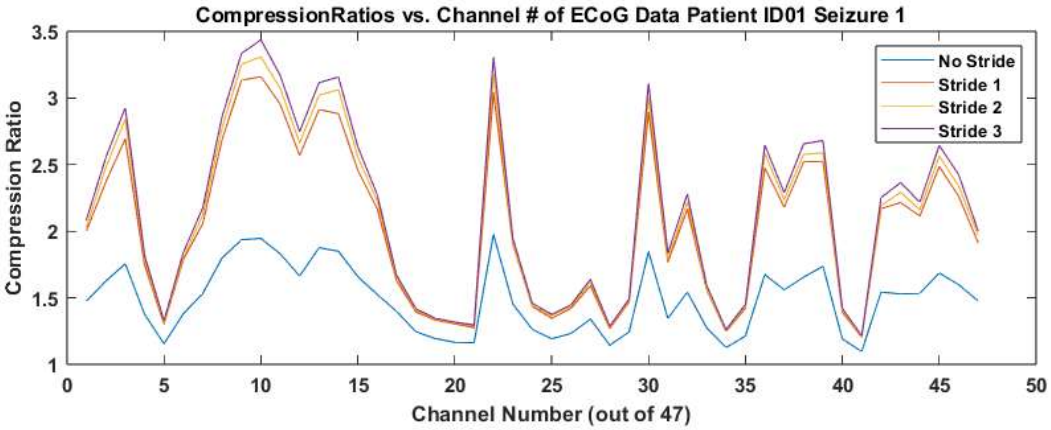
To assess the performance of the algorithm, the lossless and lossy versions of the GCD compression algorithm must be implemented in MATLAB. The analysis first converts the ECoG data from the SWEC-ETHZ iEEG database and creates an LCADC representation of it. This is then packetized into 16 space packet sizes and compressed one packet at a time. The original packets from the LCADC and the compressed packets are then concatenated in an array called ORIG_PACKETS and GCD_PACKETS respectively. The compression ratio (CR) is then calculated by calculating the ratio between the lengths of the two arrays. The CR is calculated across multiple recording channels ranging in levels of neural activity and then across multiple patients experiencing motion artifacts and seizures. As seen in Figure 2.8, the algorithm can compress data ranging from 2 to 7x (depending on channel activity) without losing any data during periods without seizures. When examining the lossy version of the algorithm, the algorithm can compress the data by 4 to 17x smaller than the original size. From the plotted compression ratios, it can also be observed that allowing strides greater than 1 (2 and 3 tested) do not add a significant amount to the overall compression ratio therefore only the no stride and stride 1 version of the algorithm will be implemented on-chip.

2.4.3. Discrete Set of GCDs to Implement On-Chip

To reduce resource costs of implementing a GCD compression block on-chip, a set of GCDs that produce the highest compression ratios can be implemented only. This will allow lower power overhead, be space efficient on silicon, and simplify the design of the compression algorithm block. This analysis takes the packets compressed by the compression algorithm in MATLAB and counts the number of GCDs produced for more than 2,062,500 packets (> 104 minutes) of ECoG

data. As seen in Figure 2.9, packets with GCD of 1 (19% of total packets) are not compressible meaning that all other packets (81% of total packets) were compressed therefore are responsible for the overall function of the compression algorithm. The compression is mostly done by GCD values {3,5,15} therefore to achieve **99%** of the theoretical compression packets that fit under this





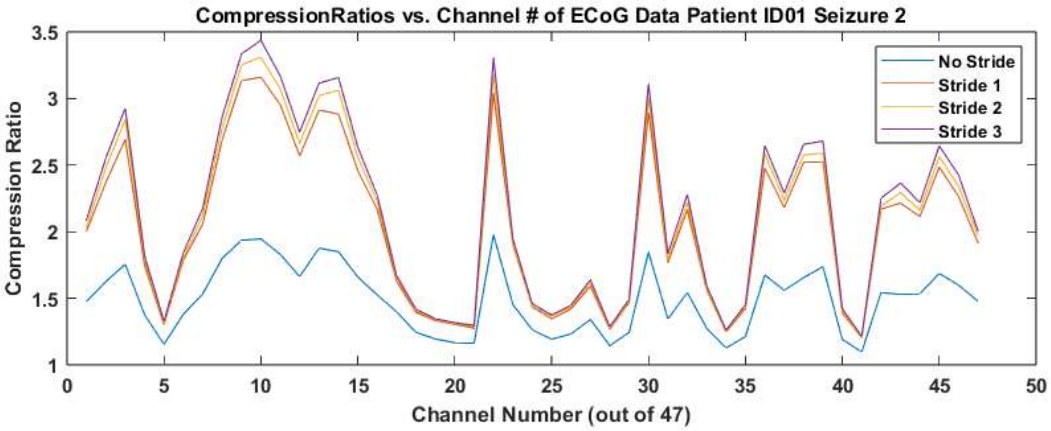


Figure 2.8: Compression Ratios across Channels (Lossy and Lossless) with and without seizures

subset of GCDs will only need to be implemented. The subset of possible GCDs can produce 9 possible packets that would be detected by the compression algorithm block. Additionally, for the lossy version (stride 1), the number of packets required to be detected is 19 but this is a small increase in space and power consumption compared to the two times increase in performance compared to the lossless version. Due to its small size, these packets can be detected entirely using combinatorial circuits. Meaning that the power overhead can be further reduced, this means that a very fast and low-cost implementation of the algorithm can be realized on-chip. The code implementing and testing the lossless and lossy version of the GCD algorithm is shown in Appendix A.1.

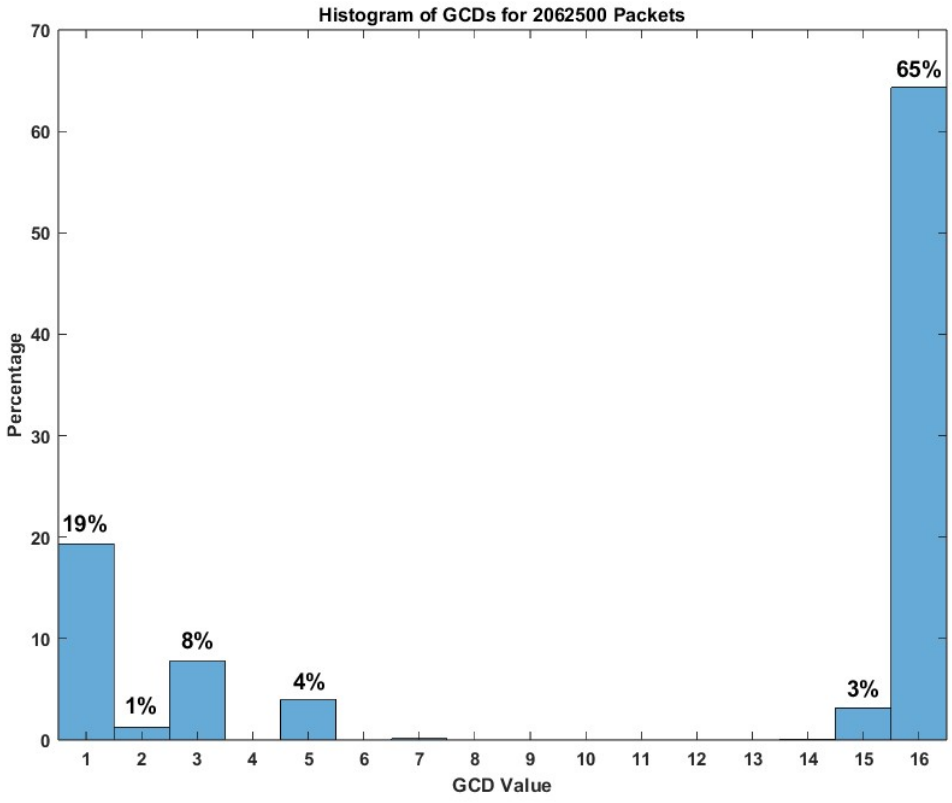


Figure 2.9: Histogram of GCDs calculated over 104 minutes of ECoG data (Lossless Implementation)

2.5. Hardware Implementation

The hardware implementation of the GCD algorithm is a simple set of combinational gates that perform the task of identifying the content of the incoming 16-bit data packet from the LCADC. The two inputs are the DATA_IN and DIR_IN registers that buffer every 16-bit packet and there are three outputs the resulting DATA_OUT, DIR_OUT, and LENGTH that are held in registers. The LENGTH register is used to store the value of the resulting compressed packet. As mentioned in the 2.4.3. Discrete Set of GCDs to Implement On-Chip section, there are 19 packets that need to be detected by the combinational logic block that will map to a unique output result and be stored in the result output registers. If one of the 19 packets are detected at the input, the compressed version of the packet will be set at the output. If it is an uncompressible packet, the input packet will be set at the output register with a LENGTH value equal to the full packet window size. A functional diagram of the GCD compression block is shown in Figure 2.10. The pattern is detected by a set of combinational gates that use the DATA_IN as the input and provide output to DIR_OUT and LENGTH. As the LC-ADC shifts the incoming data bits into the shift register, a digital controller provides clock and control signals to shift and count the data. Once full, the digital controller enables the output value holding registers to clock the results of the combinational GCD compression block and hold the results until the serializer has read the three output registers. Assuming a 7 MHz clock, the combinational GCD compression block will have a 142 ns of time to have the input values propagate to the output of the GCD block and setup time of the output registers.

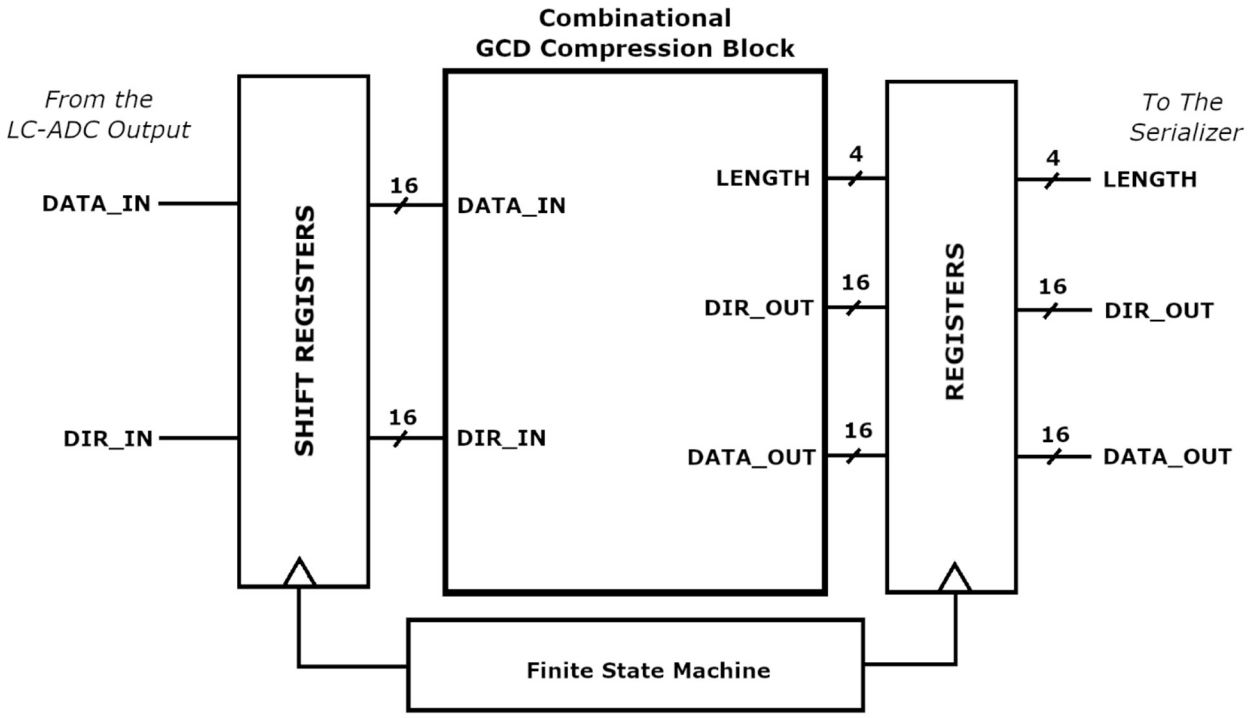


Figure 2.10: Functional Hardware Diagram of the GCD Compression Block

The implementation of GCD compression algorithm was done by writing SystemVerilog code that describes the behavior of the hardware. It was written along with the transmitter controller block to the compression block. As the GCD compression block is primarily composed of gates, the latency is ultra-low meaning that the implementation of the algorithm will be efficient. The SystemVerilog code was then synthesized using Genus to map the SystemVerilog code to the TSMC 180nm Standard Cell Library. Innovus was then used to Place & Route (PnR) the synthesized netlist along with the creation of a clock tree, fillers, power rings, etc. To place on-chip and verify performance, the generated layout was imported into the Cadence IC Design Suite. Pre-silicon performance verification included generating performance metrics from synthesis and validating expected function in Post Layout Simulation (PLS).

2.5.1. Genus Synthesis Performance Metrics

The design was synthesized using Genus to produce a structured netlist that uses the tcb018gbwp7ttc.lib library. The target clock frequency for operation is 7 MHz, this was chosen due to the intended clock sources driving the 7 MHz PRF of the UWB transmitter and the 7 kHz for sampling the output of the LC-ADC. The important metrics to derive from the synthesis reports are total area, total power consumption, and slack time. This highlights the scalability and effectiveness of the compression algorithm block. As seen in Table 2.1, the power consumption is dominated by flip-flop activity totaling to 44.7 µW and the size of the gcd_encoder block is 4,114 μm^2 which is about 375 gates (using NAND2 area to average). The total slack time is shown in Table 2.1, as there are no negative slack time and a large positive slack time meaning that it can be scaled to much higher clock frequencies but for this on-chip implementation 7 MHz will be enough.

Table 2.1: Table of Genus Synthesis Performance Metrics

Cell Area	
4114 μm^2	
Power Consumption	
Registers	37.3 µW
Logic	4.9 µW
Clock	2.57 µW
Leakage	12.7 nW
Total	44.7 µW
Timing (7 MHz Clock)	
Slack (R2R)	141.5 µs

2.5.2. Functional Verification

Functionally, the GCD compression block waits until the DATA_IN and DIR_IN registers shift the recording window number of bits (eg. 16) before it detects the packet and its corresponding GCD. The compression block then raises a VALID flag that tells the serializer that the data in the DATA_OUT, DIR_OUT, and LENGTH register is valid and ready to be read. The length must be reported as depending on the contents of the input registers will change.

In Figure 2.11, the waveforms showing this functionality across three different GCD compression blocks receiving different packets (eg. 0x0040, 0x0020, and 0xFFF8) and the output packets (eg. 0x0004 with a length of 6, 0x0002 with a length of 4, and 0xFFF8 with a length of 16). This functional waveform shows the detection of the compressible packets (0x0040 and 0x0020) and correctly set the compressed packet and reduced length at the output after 16 clock cycles (CLK_TGRAN). Given an uncompressible packet (0xFFF8), the output (DATA_OUT and DIR_OUT) were the same as the input (DATA_IN and DIR_IN) and the LENGTH was set to a value of 16. The SystemVerilog code is simulated using Xcelium. The block was then synthesized with Genus using TSMC 180 nm standard cell library.

To verify the functionality of the block after synthesis, the synthesized netlist was used within the same test bench meaning that if the two sets of waveforms match, then the block is functional on-chip. As seen in Figure 2.12, the results of each test do match with the functional simulation meaning that the synthesis was performed correctly and that the set of digital blocks that were used by the genus synthesizer tool work together to function as intended. The resulting layout of the block is shown in Figure 2.13.

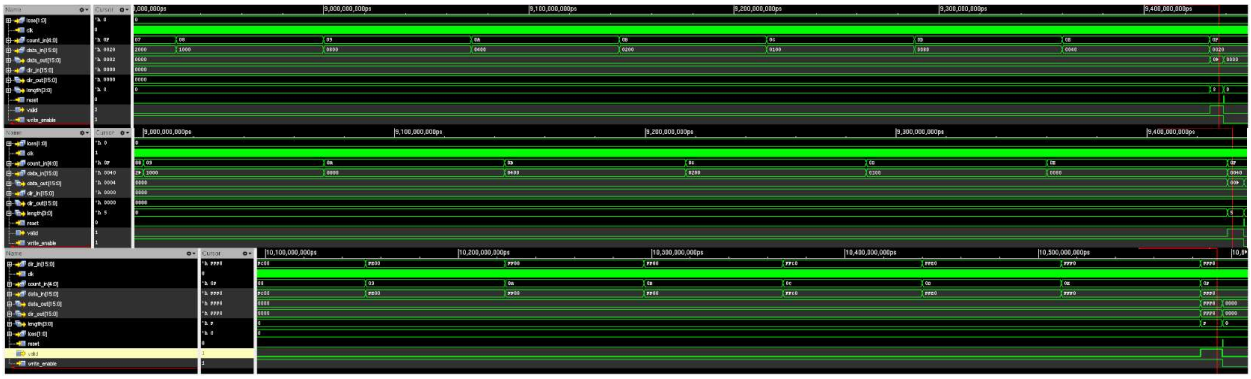


Figure 2.11: Three Functional Simulation of the gcd_encoder block written in SystemVerilog

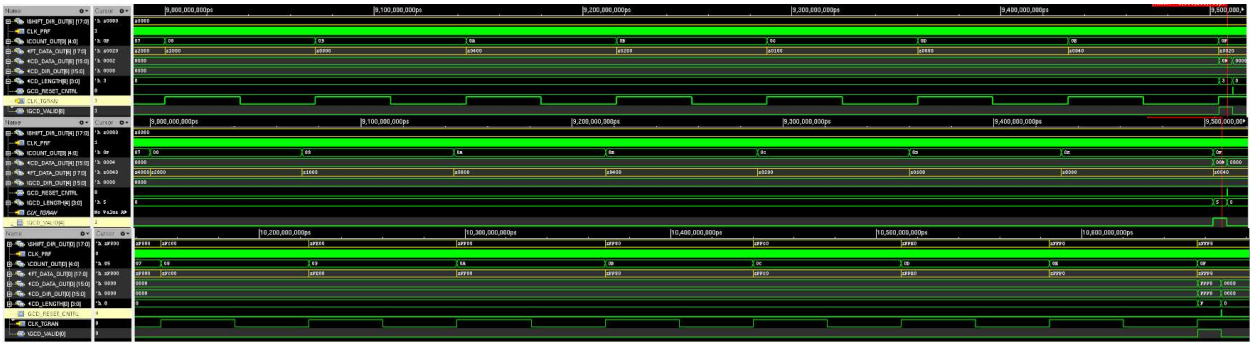


Figure 2.12: Post-Synthesis Simulation of the gcd_encoder block

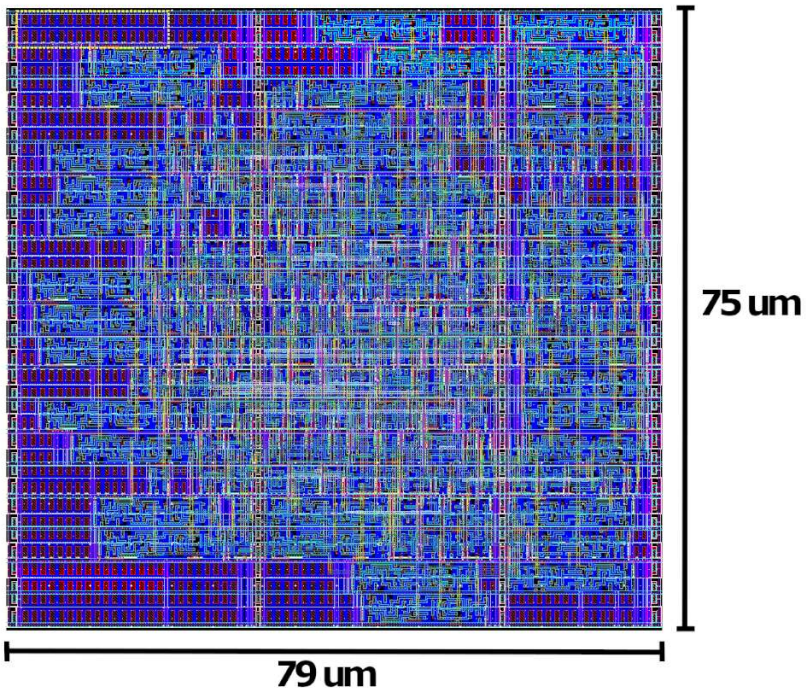


Figure 2.13: Layout of GCD compression block

Chapter 3:

Design and On-Chip Implementation of the UWB Transmitter

IR-UWB first gained significant attention in 2002 when the U.S. FCC authorized its unlicensed use across a wide frequency range. Despite its initial promise, interest in UWB technology declined in the following decade, as competing standards such as Wi-Fi and Bluetooth dominated the market. In recent years, however, IR-UWB has experienced a resurgence, driven by its unique combination of ultra-low power consumption, high data rate capability, and robustness in short-range communication. These features make it an attractive option for modern applications with strict constraints on energy and size, including implantable brain–computer interfaces, Internet of Things (IoT) devices, and short-range radar systems.

3.1. Radio Communications Review

This section establishes the basic vocabulary and trade-offs of digital wireless links—signals, rates, bandwidth, capacity, path loss, antenna constraints, error targets, and energy per bit—to motivate the choice of IR-UWB for short-range, power-limited neural implants.

3.1.1 From Baseband to Passband

In a digital communication system, the data to be transmitted is first represented as a baseband signal. This baseband waveform, often denoted as x(t), contains the digitally modulated symbols but is centered around zero frequency. To send this information wirelessly, the baseband signal is shifted, or upconverted, to a radio-frequency (RF) passband centered at the carrier frequency f_c . The resulting transmitted signal can be written as

$$s(t) = \mathrm{Re}\{x(t)e^{j2\pi f_c t}\} \tag{13.1}$$

where Re{.} denotes the real part.

The information is transmitted in symbols, each of which may represent multiple bits depending on the modulation scheme. If the modulation order is M, then each symbol carries

$$\mathrm{k} = \log_2(\mathrm{M}) \tag{3.2}$$

bits per symbol. With a symbol rate of Rs (symbols per second), the overall bit rate is

$$\mathrm{R_b} = kR_s \tag{3.3}$$

Since spectrum is always a limited resource, a key figure of merit is spectral efficiency, defined as the number of bits transmitted per second per unit of bandwidth:

$$\eta = \frac{R_b}{B} \ (bits/s/Hz) \tag{3.4}$$

where B is the occupied bandwidth of the transmitted signal [62], [63].

These relationships highlight the fundamental trade-offs in digital communication: to achieve higher data rates, one can increase the symbol rate, increase the number of bits per symbol (larger M), or increase the bandwidth. However, each comes with its own cost in terms of power, complexity, and error performance.

3.1.2 Modulation Techniques: From Conventional Carriers to IR-UWB Pulses

Modulation is the process of mapping digital bits onto changes in a radio-frequency (RF) carrier so that the information can propagate wirelessly. In amplitude-shift keying (ASK) and quadrature amplitude modulation (QAM), the amplitude of the carrier (and phase in the case of QAM) encodes different symbols. Phase-shift keying (PSK) instead uses discrete phase states of the carrier to represent information, with common examples including binary PSK (BPSK) and quadrature PSK (QPSK). Frequency-shift keying (FSK) conveys information by switching the carrier between distinct tone frequencies. These are all digital modulation schemes and should be contrasted with legacy analog techniques such as amplitude modulation (AM), frequency modulation (FM), and phase modulation (PM), which vary the carrier continuously rather than mapping discrete symbol states.

IR-UWB departs from continuous sinusoidal carriers by transmitting very short pulses (hundreds of picoseconds to a few nanoseconds). Each pulse occupies a very wide bandwidth in the frequency domain—hence “ultra-wideband.” Symbols are commonly encoded by shifting the temporal

position of the pulse (pulse-position modulation, PPM) or by flipping its polarity (binary pulse modulation, BPM) [64], [65]. These pulse schemes enable simple receiver architectures that detect pulse presence, timing, or polarity rather than tracking precise carrier phase or multiple amplitude levels. The result is especially attractive for short-range, low-power links such as neural implants: ultrashort pulses allow aggressive duty-cycling (transmitter and analog front-end are active only briefly), reducing average energy per bit while still supporting high aggregate data rates due to the large, occupied bandwidth [66].

Because modulation choices affect how much spectrum we occupy and how fast symbols change, we relate bandwidth next to symbol rate and pulse duration.

3.1.3 Bandwidth, Symbol Rate, and Pulse Duration

The occupied bandwidth B of a signal is typically measured between the −3 dB points (or using a 99%-power definition). With Nyquist pulse shaping, the occupied bandwidth scales with symbol rate Rs and the excess-bandwidth factor α (roll-off):

$$B \geq (1 + a)R_s \tag{3.5}$$

For IR-UWB, sub-nanosecond pulses correspond to gigahertz-scale bandwidths, enabling high data rates without resorting to very high modulation orders. Conversely, in narrowband systems a small B forces either lower Rs or higher bits per symbol (larger M), which typically increases required signal-to-noise ratio and circuit complexity [63],[66].

Bandwidth alone does not determine how much information can be carried; noise and received power also matter, summarized next by Shannon–Hartley.

3.1.4. Capacity, SNR, and E_b/N_0

The Shannon–Hartley theorem upper-bounds the reliable data rate C (capacity) of a band-limited channel: $\mathrm{C} = \mathrm{B}\ \log_2(1 + \mathrm{SNR})$

Here SNR is the signal-to-noise ratio over the receiver bandwidth B. Relating SNR to energy per bit Eb and noise spectral density N0 gives:

$$\mathrm{SNR} = \frac{P_r}{N_0 B} = \frac{E_b R_b}{N_0 B} = \frac{E_b}{N_0} \tag{3.6}$$

Thus, for a fixed Eb/N0 trying to push very high spectral efficiency η (e.g., by using large M in a narrow B) demands proportionally higher SNR, usually increasing linearity, clocking, and power requirements. IR-UWB instead leverages large B to raise C without extreme η, supporting simpler, lower-power receivers [63].

3.1.5. Link Budget: Free Space and Tissue

The SNR we can achieve depends on how much power actually arrives at the receiver, which is governed by the link budget. In free space, the received power P_r depends on the transmit power P_t, antenna gains G_t and G_r, wavelength λ, and distance d (Friis relation):

$$P_r = P_t G_t G_r \left(\frac{\lambda}{4\pi d}\right)^2 \tag{3.7}$$

The corresponding free-space path loss (FSPL) in decibels is:

$$FSPL_{dB} = 20 \log_{10}\left(\frac{4\pi d}{\lambda}\right) \tag{3.8}$$

For implants, propagation is not free space: biological tissues add frequency-dependent absorption and interface reflections at skull, dura, skin, and air. A practical link budget in dBm is:

$$P_r(dBm) = P_t + G_t + G_r - FSPL - L_{tissue} - L_{misc} \tag{3.9}$$

where L_{tissue} aggregates tissue losses and L_{misc} includes mismatch, packaging, and other parasitics. For very short ranges (e.g., implant to head-mounted receiver), these losses can be offset by modest P_t and appropriate antennas, especially at higher f_c where antennas are smaller [63],[67]. Antenna size and efficiency are themselves constrained by wavelength, linking device form factor to center frequency.

3.1.6. Center Frequency, Wavelength, and Antenna Size

The wavelength is $\lambda = c / f_c$. Resonant antennas typically scale with λ (e.g., $\lambda/2$ dipole). Electrically small antennas ($ka \ll 1$, with $k = 2\pi/\lambda$ and the minimum circumscribing radius) suffer fundamental efficiency and bandwidth limits (Chu–Harrington), approximately worsening with ka^2 [68]. Consequently, higher center frequency reduces antenna size, which is desirable in implants, at the expense of increased tissue attenuation.

$$\lambda = \frac{c}{f_c}, \quad k = \frac{2\pi}{\lambda}, \quad ka \ll 1 \tag{3.10}$$

3.1.7. BER Targets and Design Use

Acceptable BER depends on application and coding. Uncoded consumer links commonly target $10^{-3} - 10^{-5}$, while medical sensing and neural recording often target 10^{-6} or lower (possibly after forward-error correction). Given a BER target, standard references provide the corresponding required E_b/N_0 for the chosen modulation and receiver structure; combining that

with the link budget yields transmitter power, antenna, and margin choices appropriate to the implant scenario [63].

3.1.8. Energy per Bit, Duty Cycling, and IR-UWB

Average power and energy per bit are related by:

$$E_b = \frac{P_{avg}}{R_b} \tag{3.11}$$

IR-UWB transmitters exploit a low duty cycle δ: RF and analog circuits are active only during brief pulse intervals. At short implant-to-receiver distances, this pulsed operation meaningfully reduces analog on-time and clocking demands, lowering Eb while respecting specific absorption rate (SAR) limits. Combined with the large available B, UWB achieves high throughput at modest complexity and SNR [66].

3.1.9. Synthesis: Why IR-UWB over Narrowband Far-Field

For high-density neural implants, the link is short-range and power-limited; antennas must be millimeter-scale; aggregate data rates are high; and error rates must be tightly controlled. IR-UWB aligns with these constraints: (1) It uses large bandwidth to raise data rate without extreme spectral efficiency, avoiding the high SNR and linearity burden of very high-order narrowband modulation (Sec. 3.1.4). (2) Pulsed operation minimizes analog/RF duty cycle, reducing average power and energy per bit (Sec. 3.1.8). (3) Higher f_c enables smaller antennas compatible with implant form factors (Sec. 3.1.6), and the short-range path keeps link losses manageable (Sec. 3.1.5).

By contrast, narrowband far-field links must achieve comparable throughput in small B, which pushes spectral efficiency, raises required SNR and circuit complexity, and struggles with practical

antenna sizes at sub-GHz [41, p. 999], [69], [70], [71]. Considering range, bandwidth, center frequency, BER targets, antenna constraints, and energy per bit together, IR-UWB provides a more favorable operating point for implantable brain–computer interface transmitters [63], [66], [68]

3.2. Wireless communication in brain implants

For cranial implants, the device must be sufficiently small and conformal to avoid mechanical stress or damage to surrounding bone and soft tissues. Reported adult calvarial (skull vault) thickness averages between 6–8 mm, depending on anatomical region (e.g., frontal ≈ 8 mm, parietal ≈ 7 mm), which sets the dimensional envelope for implants designed to fit within or beneath the skull [72 – 73].

In addition to mechanical safety, thermal safety is a critical consideration. Power dissipated by the implant generates heat that can raise local tissue temperature. International standards for active implantable medical devices (e.g., ISO 14708) recommend that the temperature rise at the tissue–device interface should not exceed 2 °C under worst-case conditions [74]. This guideline is consistent with broader safety frameworks (e.g., FDA), which generally consider tissue temperatures up to 39–40 °C as tolerable, provided the incremental heating from the device remains within the 2 °C margin [75 - 77].

Across all wireless BCIs, it can be consistently observed that most of the power consumption comes from the wireless communication back-end of the implant [34], [77 - 78]`. Optimizing the energy efficiency of the transmitter will have the largest impact on the overall system energy efficiency and therefore it’s scalability to greater recording channels.

The communication requirements of cranial implants differ fundamentally from those of conventional wireless systems. Standards such as Bluetooth, Wi-Fi, or cellular networks are optimized for long-range links and multi-user coexistence. They operate over relatively narrow bandwidths (tens of MHz) to conserve spectrum and rely on elaborate packet structures and control fields, which introduce overhead regardless of whether useful data is present. These design choices improve reliability across tens to hundreds of meters but come at the cost of higher protocol complexity and energy per bit.

By contrast, neural implants only need to bridge a short link (implant to nearby receiver) while streaming data from hundreds of channels in real time. In this scenario, spectrum scarcity is less critical than energy and area efficiency. Ultra-wideband signaling takes advantage of gigahertz-scale bandwidth to transmit large volumes of data at low spectral efficiency, thereby avoiding the high-order modulation and strict SNR requirements of narrowband schemes. Equally important, its pulse-based nature enables aggressive duty-cycling of the RF front-end, reducing both dynamic power consumption and silicon area.

For these reasons, IR-UWB emerges as the most suitable transmitter architecture for cranial implants: it matches the short-range link budget, minimizes energy per bit, scales gracefully with channel count, and can be realized efficiently in mature CMOS technologies such as 180-nm.

3.3. IR-UWB Transmitter Design

3.3.1. IR-UWB Regulations

To mitigate interference with already existing narrowband communication systems, regulations and standards must be set. The Federal Communications Commission (FCC) and the Canadian Ratio-Television and Telecommunications Commission (CRTC) are two governing bodies in the United States and Canada, respectively, that sets the wireless communication standards to prevent the overlap of frequency bands that would interfere with neighboring communication systems [79]. These standards are enforced by setting the maximum Power Spectral Density (PSD) within the allocated frequency bands, specifying the maximum allowable output power radiated by the antenna, and defining the bandwidth size. In practice, the FCC specifies a spectral mask for ultra-wideband devices that limits emissions to −41.3 dBm/MHz across the UWB range, while also capping the maximum radiated output power at 0 dBm [80].

The allowable PSD according to the FCC standards (Part 15 Subpart F) and CRTC (RSS-220) is plotted in Figure 3.1. The maximum allowable radiated power is 0 dBm in a 50 MHz bandwidth and the bandwidth standard is set by only allowing a fractional bandwidth greater than 20% or an absolute bandwidth greater than 500 MHz. Equivalent frameworks exist internationally, such as ETSI EN 302 065 in Europe and MIC guidelines in Japan, with similar but not identical PSD masks and frequency allocations [81 - 82]. These regulatory limits directly influence transmitter design by constraining pulse amplitude, pulse repetition frequency, and spectral shaping, ensuring coexistence with Wi-Fi, Bluetooth, and other incumbent systems.

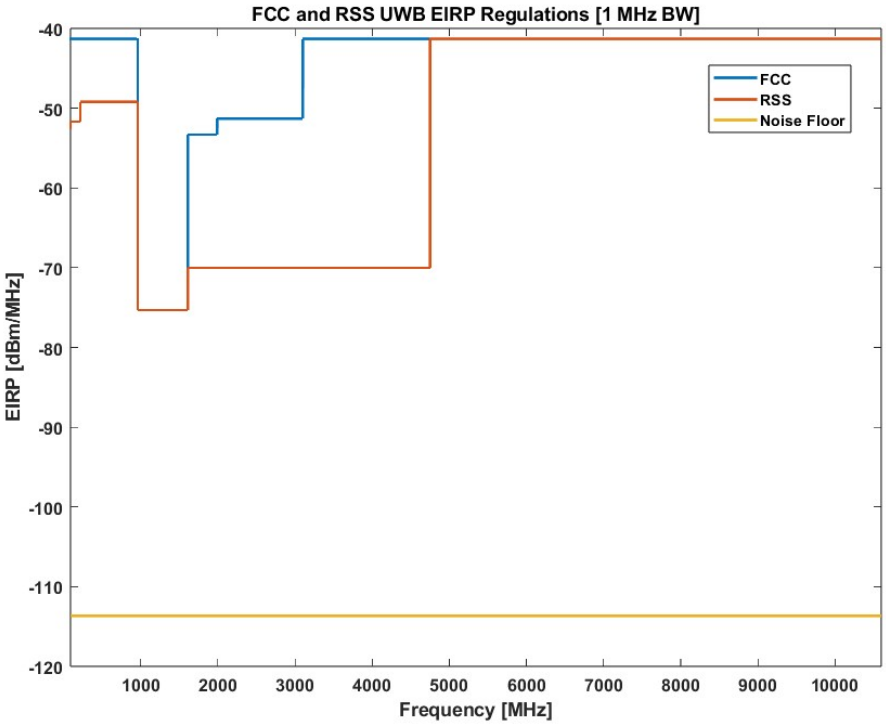


Figure 3.1: EIRP Regulations for IR-UWB devices from FCC and RSS Standards

3.3.2. The UWB Pulse

As the IR-UWB communication systems uses RF pulses to transmit data, the pulses need to be characterized as to better understand the requirements of the transmitters architecture. As the pulse width is equal to the inverse of the pulse's bandwidth, the minimum bandwidth of 500 MHz correlates to a maximum pulse width of 2 ns. In practice, narrower pulses (e.g., sub-nanosecond) would correspond to multi-gigahertz bandwidths and allow even higher data rates, but at the cost of more challenging circuit design and potentially increased attenuation through tissue [66].

The center frequency is chosen to be 4 GHz to minimize path loss while balancing tissue penetration and antenna size constraints, as it offers better propagation characteristics than higher-frequency brands. Frequencies much lower than this (e.g., sub-GHz) would improve penetration

but require physically larger antennas unsuitable for cranial implants [83]. Additionally, this frequency selection ensure compliance with the FCC spectral mask. The 3.1–10.6 GHz UWB band defined by the FCC provides flexibility in center frequency choice, but 4 GHz is a common compromise between efficiency and safety [80].

For a 4 GHz center frequency and a pulse width of 2 ns, the sub pulses would have 0.25 ns periods each, with 8 sub pulses total for the 2 ns UWB pulse to be formed. An example of this pulse can be seen in Figure 3.2. This sub-pulse structure also eases implementation of pulse-position or pulse-polarity modulation, since timing resolution on the order of hundreds of picoseconds is sufficient for symbol encoding in neural implant applications.

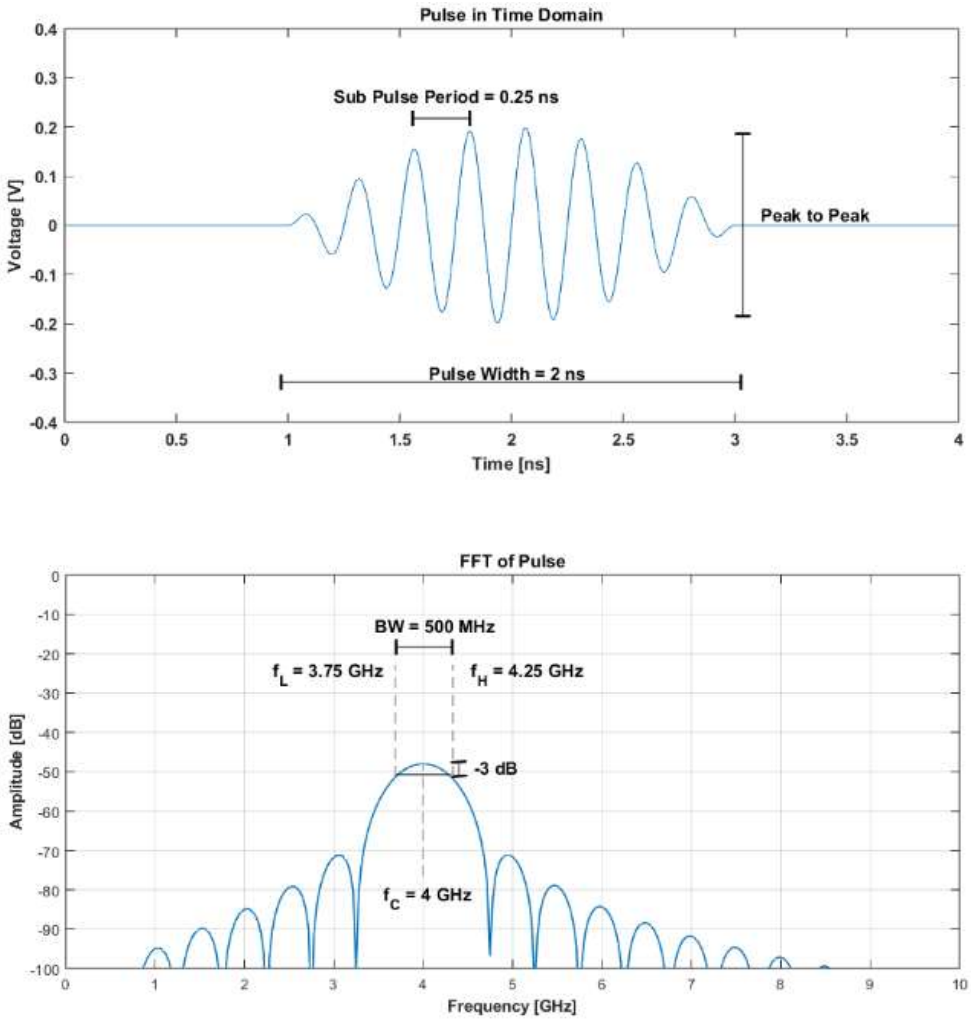


Figure 3.2: A 4 GHz (center frequency) UWB pulse with a bandwidth of 500 MHz

3.3.3. Transmitter architectures

In recent years, two main architectures have emerged for IR-UWB transmitters: up-conversion and edge-combination [84]. An up-conversion architecture uses an oscillator that is turned on/off to create a short UWB pulse. The main benefit of using an oscillator is that many different phases can be generated meaning it can create high-order modulation schemes but is less energy efficient, than the edge-combination architecture due to the presence of an oscillator that is either always ON or needs to turn ON and OFF quickly which can be very inefficient [66]. Furthermore, the

integration of wideband oscillators and mixers typically requires analog-intensive design, increasing chip area and limiting scalability in low-cost CMOS nodes [85].

The edge-combination architecture has no oscillator and primarily uses digital blocks. It creates a pulse by using a delay line to create multiple delayed copies of an edge that triggers multiple sub-pulse generators or delays an input sub-pulse and combines these sub-pulses to create a UWB pulse [86]. This architecture benefits from the high energy efficiency of digital blocks but is unable to accurately create multiple phases or frequencies therefore it is best implemented when low-order modulation schemes are required [87]. Another advantage of this approach is that it naturally produces short, well-defined pulses with minimal carrier leakage, reducing spectral sidelobes and simplifying compliance with FCC/CRTC emission masks [88].

Ultimately, the edge-combination architecture was chosen due to its high energy efficiency, low-complexity, and its compatibility with low-order modulation schemes. As the RFE is based on an LCADC, the data has three symbols (+1, -1, and 0) which can be implemented using a simple modulation scheme such as PPM [89]. This design choice also aligns with the primary goal of neural implants, where the dominant challenge is minimizing energy per bit and silicon area, rather than supporting high-order constellations or long-range links.

3.3.4. Receiver architectures

Although the design of an IR-UWB receiver is out of scope, it is important to understand how they work to better understand its relationship with the transmitter. The goal of the receiver is to demodulate the incoming RF signal and detect the UWB pulses and de-modulate the symbol into its respective digital value. The two main architectures used are: coherent and non-coherent receivers [90].

Coherent receivers use a template pulse or sinusoidal that relies on the precise synchronization of the RF signals and template's phase. To synchronize the template's phase with the RF signal, the channel must remain consistent and known meaning that the transmitter-receiver link must be set and remained unchanged. The benefit of this architecture is its high sensitivity, robustness to multipath, and supports high-order modulation but suffers from higher power consumption, complexity, and requires precise synchronization [91]. Coherent schemes often employ techniques such as rake receivers to exploit multipath diversity, which can significantly improve performance but at the cost of even greater computational and energy overhead [92].

As for non-coherent receivers, the architecture uses the incoming RF signal only to detect the presence of pulses, it does this by either squaring and/or using an envelope detector to detect the amount of energy present in the RF signal. If a pulse is present, a greater amount of energy will be in the signal which can be compared to a base line of the noise within the channel. This method is less complicated and consumes less energy than coherent architectures but can't demodulate complex modulation schemes [93]. Energy-detection receivers, in particular, are attractive for biomedical applications because they eliminate the need for carrier tracking, tolerate channel variations, and can be implemented almost entirely with low-power digital logic [94].

Both architectures are suitable for the current implementation of the designed UWB transmitter but due to the low-order modulation scheme implemented at the transmitter, a non-coherent receiver can be implemented adjacent to the transmitter. This pairing of edge-combination transmitters with non-coherent energy-detection receivers has been widely proposed in short-range biomedical telemetry, where minimizing energy per bit and silicon area outweighs the benefits of supporting high spectral efficiency [95].

3.4. Transmitter Design Requirements

In this section, we define the key performance requirements and constraints that shape the design of IR-UWB transmitter system for high-density neural implants. Typical intracranial-to-scalp links span only a few centimeters, but attenuation through bone and tissue can exceed 20–30 dB depending on frequency, which directly impacts link budget planning [96]. A target range and path loss must be established to figure out the required receiver sensitivity and required transmitter output power. The performance requirements will define the required pulse repetition frequency (PRF) and other constraints such as pulse width, number of sub pulses, and maximum allowable delay.

In practice, PRF determines both the achievable data rate and the average power consumption, since higher PRF increases throughput but also raises the transmitter's duty cycle [97]. Pulse width and sub-pulse structure, on the other hand, influence spectral occupancy, compliance with FCC/CRTC emission masks, and timing resolution at the receiver [80]. Finally, delay constraints are dictated by both circuit timing margins and the need to avoid inter-symbol interference, which becomes critical in multipath environments typical of in-body channels [98].

3.4.1. Path loss and range

To establish an accurate path loss model, the required Signal to Noise Ratio (SNR) for the respective modulation scheme must be established. By simulating an Additive-White Gaussian Noise (AWGN) channel, sweeping through SNR values, and the respective Bit Error Rate (BER) can be calculated as shown in Figure 3.3. For a BER value of less than 10^{-6} an SNR of 22 dB is required at the receiver [67]. This value is consistent with published performance curves for binary

pulse-position or binary phase-shift modulation in AWGN channels, and it provides a conservative margin for biomedical applications where link reliability is critical [66].

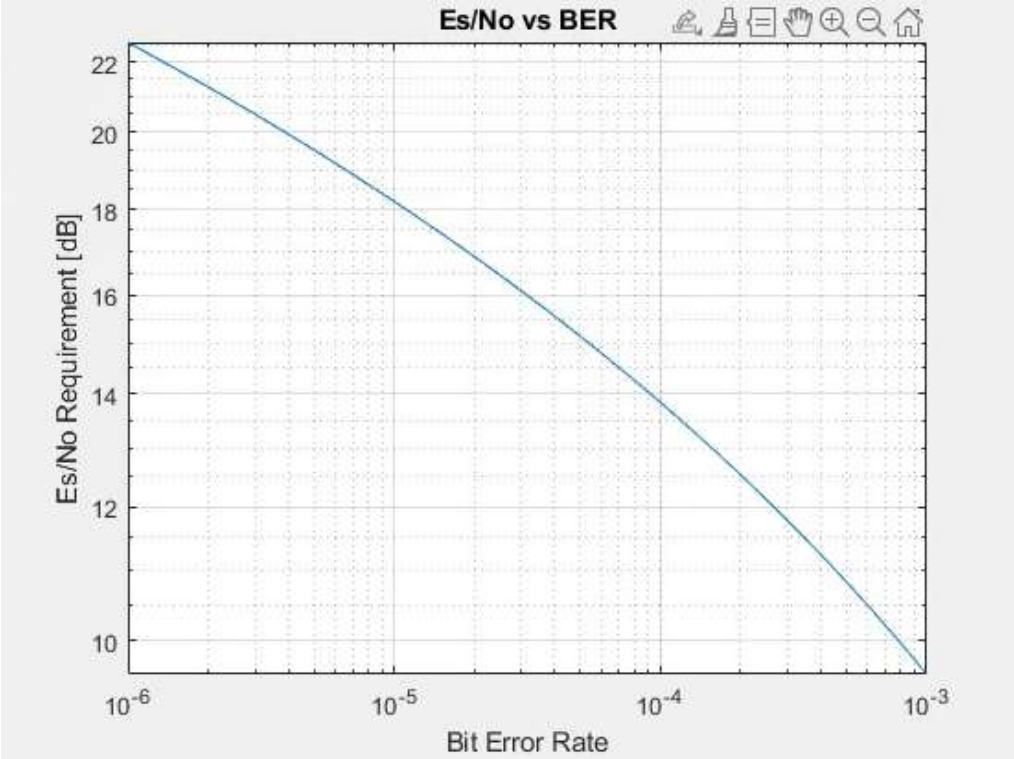


Figure 3.3: SNR Required for a given BER for PPM Modulation in AWGN channel

The normalized noise floor is characterized by using the thermal noise floor equation for a temperature of 38.5 °C (average temperature in a human head).

$$N_0 = 10\log(kTB) + 30 = -174\ dBm/MHz \tag{3.12}$$

Here, k is Boltzmann's constant, T is absolute temperature, and B is the system bandwidth. The +30 term converts watts to dBm. The −174 dBm/MHz baseline is a widely accepted reference noise density at room temperature, with a small correction applied for body temperature [62].

To calculate the minimum receiver sensitivity, the noise floor power must be added to the required SNR (22 dB) and expected noise figure of the receiver (e.g., 2 dB).

$$P_{RXmin} = N_0 + 10\log(BW) + NF + \frac{E_S}{N_0} = -63\ dBm \tag{3.13}$$

This represents the weakest signal level that can be decoded with acceptable BER under the assumed modulation and receiver design. Assuming maximum cable losses of 4 dB, antenna gain of 3 dB, 10 cm of air medium, and 1 cm of tissue layer. The path loss in air was calculated to 24 dB and the path loss of the tissue layer to 2.4 dB. The minimum required transmitter output power is therefore,

$$P_{TXmin} = P_{RXmin} + Air_{Pathloss} + Tissue_{Pathloss} + 2L_{cable} - 2Gain_{Ant} = -35\ dBm \tag{3.14}$$

which corresponds to about 0.32 μW average radiated power. This link budget is summarized in Figure 3.4. This extremely low power requirement highlights the feasibility of IR-UWB transmitters for cranial implants, where energy budgets are tight and thermal safety constraints limit average dissipation.

3.4.2. Protocol and pulse repetition frequency

As mentioned in Chapter 2, the compression algorithm heavily reduces the PRF requirement of the transmitter enabling larger pulse amplitudes therefore more reliable reception at the receiver and less power consumed at the transmitter. Here, PRF (pulse-repetition frequency) denotes the average number of transmitted pulses per second; for PPM with one pulse per symbol, PRF ≈ symbol rate. Lower PRF at fixed data volume allows higher per-pulse energy while keeping average power and PSD within regulatory masks.

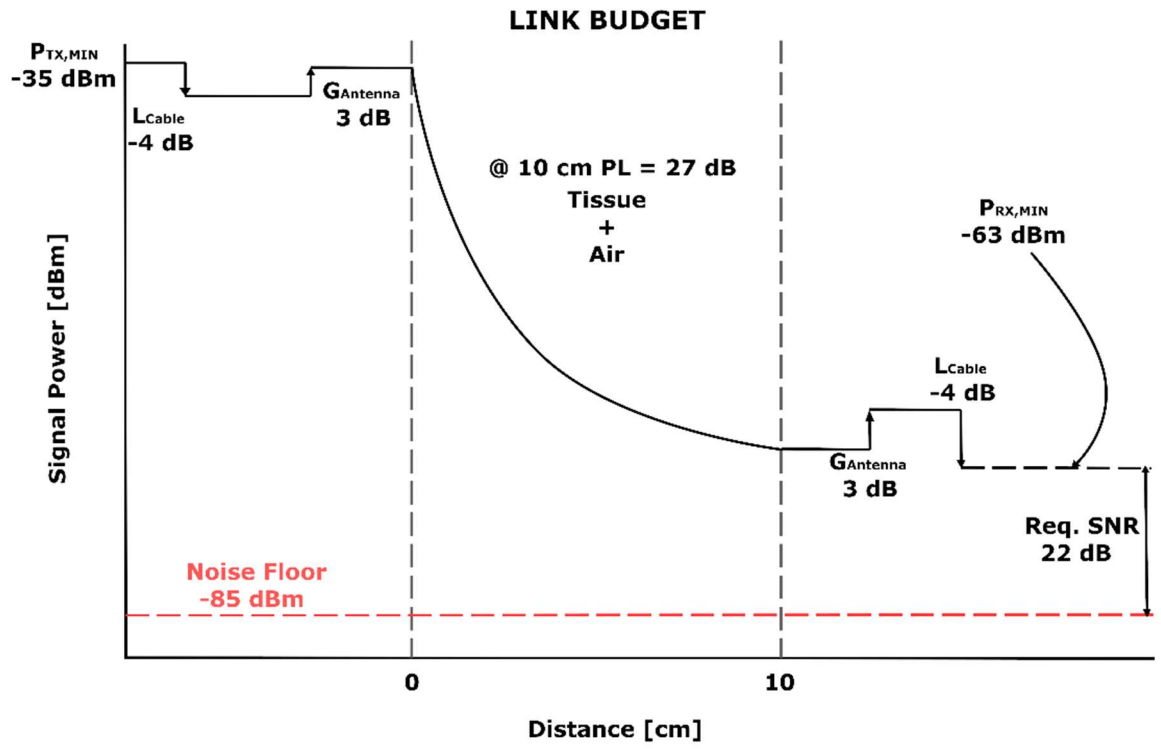


Figure 3.4: Link Budget of the proposed IR-UWB Transmitter – Receiver Link

The goal of the transmitter would be to transmit 1000 recording channels' data. This channel count is an illustrative scalability target (not a fixed requirement); all calculations scale linearly with the number of channels and can be re-parameterized for other counts (e.g., 128, 256, 512). Assuming a T_{GRAN} of 190 us and a 16 TGRAN window, and a PPM modulation scheme, 16000 symbols would have to be sent within a 3.04 ms time frame so that the next time frame can be recorded and prepared for transmission.

Without compression, the transmitter would have to work at a frequency of 5 MHz.

$$PRF_{woCompression} = \frac{Num.\,of\ Symbols}{Recording\ Time} = 5\ MHz \tag{3.15}$$

In practice, the achievable PRF is limited by (i) technology timing (minimum delay cell, edge slew, clock/data jitter), (ii) spectral-mask compliance (−41.3 dBm/MHz FCC/UWB PSD), and (iii) allowable duty cycle $\delta = PRF \times \tau_{pulse} \ll 1$ to keep average power and temperature rise within safety limits.

With lossless compression, which reduces the number of symbols by 4.18 times on average, the new PRF would have to be 1.2 MHz. Because average transmit power satisfies $P_{avg} \approx E_{pulse} \times PRF$, lowering PRF by compression permits either (a) reduced P_{avg} for the same link margin or (b) increased pulse amplitude/energy for improved robustness at the same P_{avg} . Both options improve energy/bit and receiver reliability over short in-body links.

To test the transmitter with and without the compression, the target PRF should be set to 5 MHz. This worst-case PRF exercises the timing and spectral-mask limits; the 1.2 MHz operating point then demonstrates the energy/performance gains enabled by compression under identical frame timing. The protocol should be enabling the receiver to differentiate between each packet which could be done either through creating delays between each packet or setting a specific start/stop sequence that is recognized by the receiver as the start/stop of each channels data. In addition, a short preamble and channel/length fields (with CRC) minimize ambiguity and allow the receiver to re-synchronize across frames without continuous carrier tracking, which is consistent with non-coherent, energy-detection receivers used in low-power UWB. Packetization overhead should be budgeted explicitly, as it slightly increases required PRF (or frame time) if per-channel headers are used; a frame-level header amortized across channels typically minimizes this overhead.

3.5. Transmitter architecture

The transmitter architecture is chosen based off an edge-combination scheme. It will create multiple sub-pulses that are combined to create the final UWB pulse. This approach avoids the need for a wideband oscillator and mixer chain, relying instead on digital delay and edge generation to produce short, spectrally wide pulses with high energy efficiency. As the chosen modulation scheme is PPM, the modulator will only impact the timing of the UWB pulse being sent and not it's shape. In this architecture, the pulse generator path defines the waveform envelope, while the PPM block controls when in time the composite UWB pulse appears, cleanly separating pulse-shaping from symbol encoding. This separation simplifies circuit design and ensures that modulation does not distort the pulse spectrum, which is critical for compliance with FCC/CRTC emission masks.

The architecture employed can be seen in Figure 3.5. At the top level, it can be viewed as a chain that transforms input data into precisely timed RF pulses: the PPM modulator encodes timing, the edge-combination delay line expands each event into multiple aligned sub-pulses, and these are then summed and amplified before being radiated by the UWB antenna. This organization supports scalability (by adjusting the number of sub-pulses or delay stages) and robustness (by distributing energy across a broad spectrum), making it well-suited to the short-range, low-power communication required in neural implants.

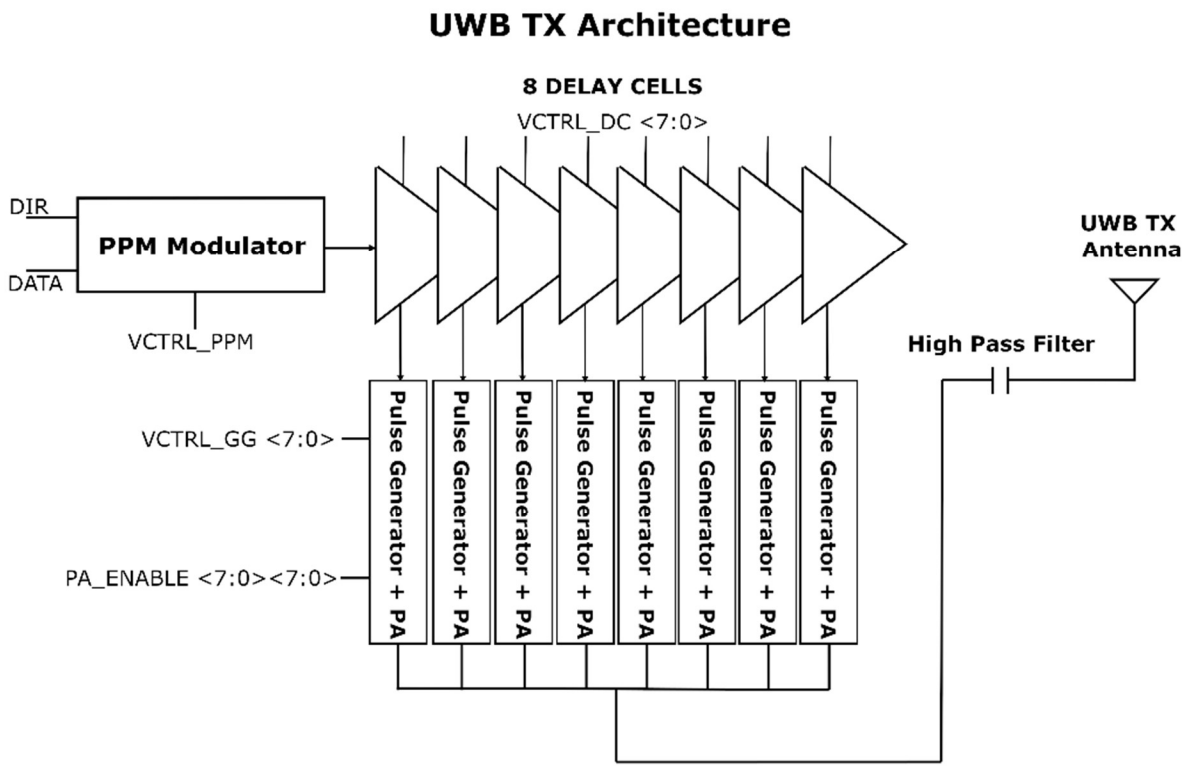


Figure 3.5: UWB TX Architecture Block Diagram

3.5.1. Delay Cell

The delay cell is comprised of a current-starved inverter that is controlled by two current mirrors biased by a single voltage as seen in Figure 3.4. This architecture was chosen due to its precise control over the OUT delay. It creates this delay by letting a precise amount of current fill the input capacitance of the inverter at the output of the delay cell. As current-starved inverters have a weak drive capability the slope is heavily influenced by the input capacitance seen at the output of the current-starved inverter. A tail PMOS transistor has been placed to gate the current flowing into the delay cell circuit. The purpose of this was to reduce the leakage current of the circuit to improve the power consumption of all other circuits using this delay cell (PPM modulator, Delay Line, and Pulse Generator). The individual sizing of the transistors within the Delay Cell are shown in Table

3.1. As seen in Figure 3.6, this delay cell architecture can reliably create delays ranging from the minimum delay created by a minimum sized inverter in TSMC 180nm to 120 ns

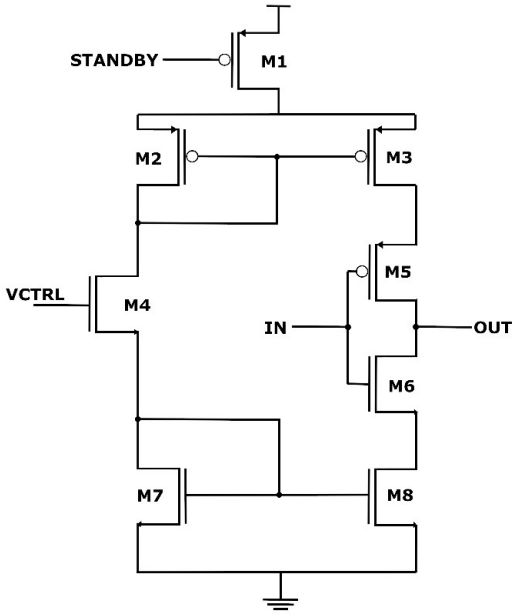


Figure 3.6: Delay Cell Architecture

Table 3.1: Transistor sizes used for the Delay Cell circuit

Transistor	**Size W/L [µm]**
M1	0.72/0.18
M2	1/0.18
M3	4/0.18
M4	0.36/0.18
M5	2.16/0.18
M6	1.08/0.18
M7	0.5/0.18
M8	2/0.18

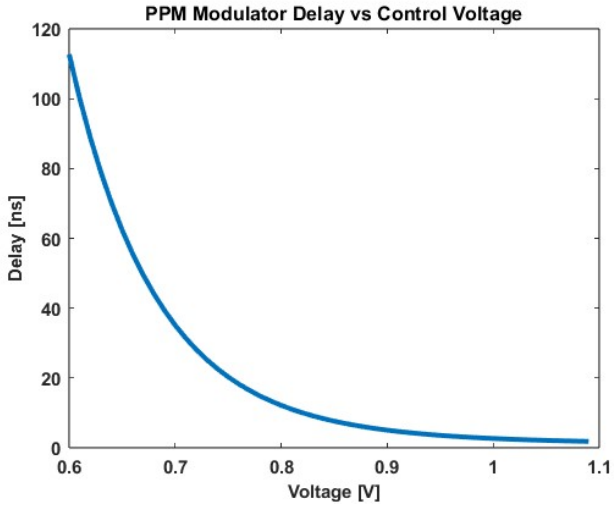


Figure 3.7: PPM Modulator Effective Delay Vs VCTRL voltage plot

3.5.2. PPM Modulator

The PPM modulator is shown in Figure 3.6. It functions by either delaying the input rising edge or letting it through. It does this by multiplexing between two paths one allows the edge to propagate, and the other is connected to a delay cell that delays the leading edge. This simple structure enables symbol encoding purely through timing rather than amplitude or phase, which reduces complexity and is well-suited for low-power neural implant transmitters.

The delay line is composed of a current-starved inverter that is controlled by a voltage biased current mirror. This configuration provides a tunable propagation delay by modulating the drive current of the inverter, allowing fine-grained control of pulse position. Voltage biasing (using V_{CTRL}) was selected because it permits fast switching between different delay values and makes it possible to extend the design to M-ary PPM schemes. Supporting M-ary PPM not only increases spectral efficiency but also enables experimental evaluation of receiver performance limits under higher-order modulation.

For this implementation, the transistor sizing for the delay cell is the same as shown in Table 3.1 and the transistors in the inverter are minimum-sized devices. This minimizes parasitic capacitances, reduces area, and lowers static power consumption, at the cost of increased sensitivity to process variation, which is an acceptable trade-off in this application given the low duty cycle of operation. As shown in Figure 3.9, the PPM modulator achieves a variety of delays based on the value of V_{CTRL} (0.6 – 1.1 V) for the PPM '1' bit but regardless of V_{CTRL} the minimum delay is achieved for PPM '0'.

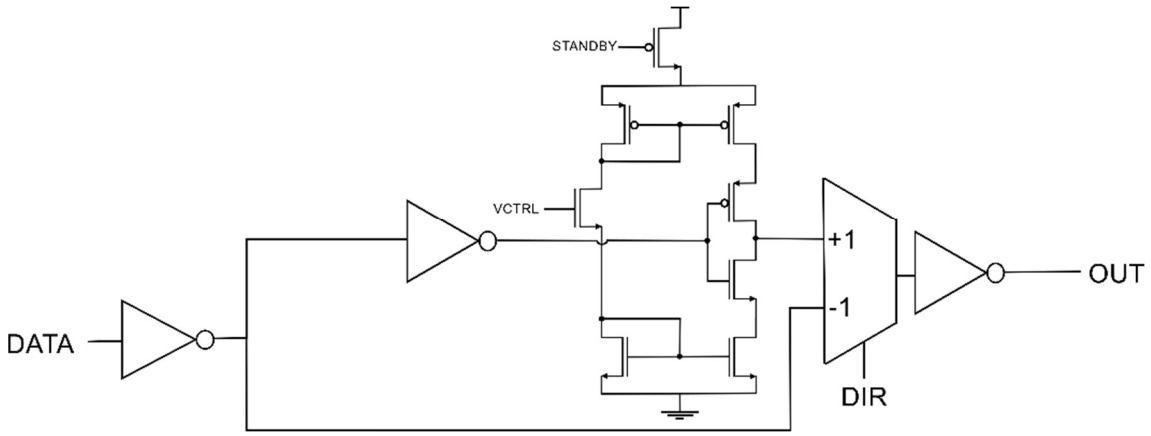


Figure 3.8: The PPM Modulator Architecture

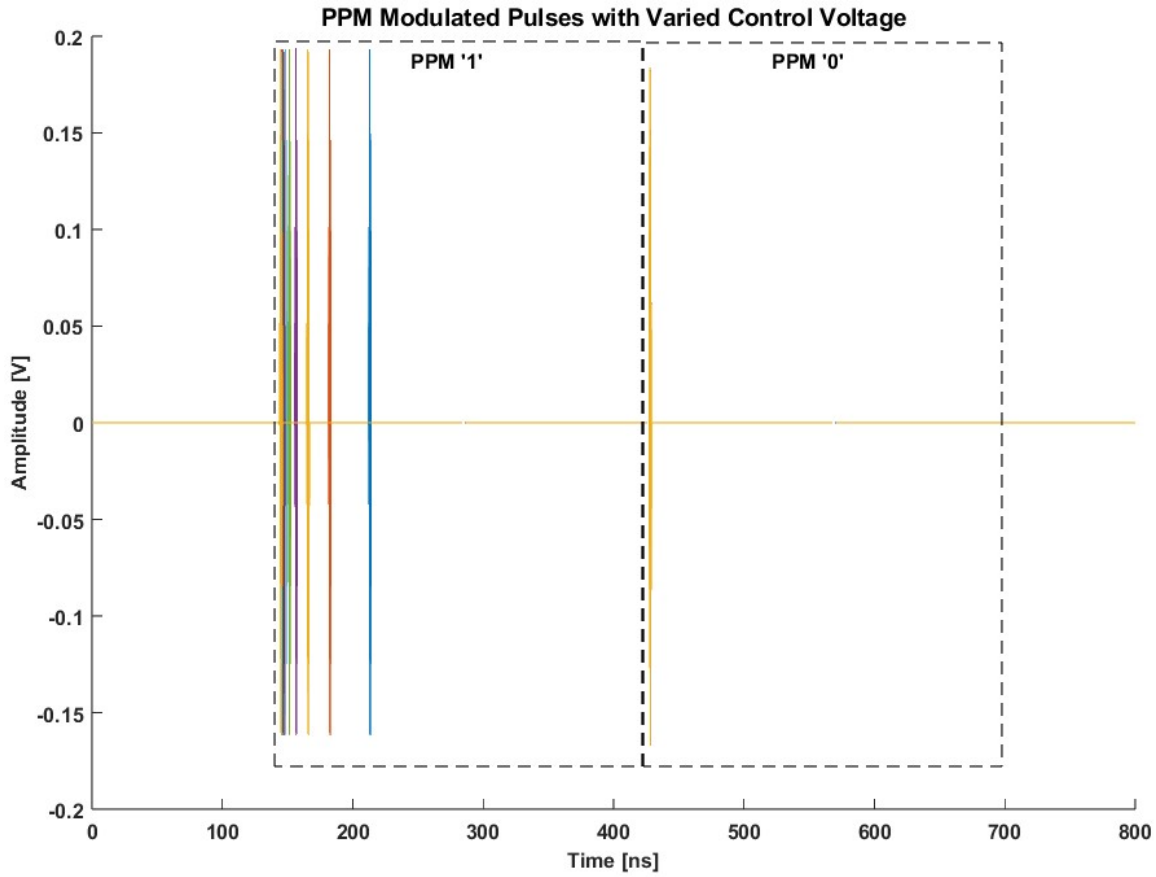


Figure 3.9: PPM Modulated Pulses for a range of VCTRL for both bit PPM ’1’ and PPM ‘0’

3.5.3. Delay Line

The delay line uses the output rising edge of the PPM modulator as a trigger to generate an UWB pulse. This edge is propagated through 8 delay cells that drive 8 separate pulse generator and power amplifiers. These sub-pulses are then combined to make the UWB pulse.

The delay line is simply composed of current starved inverters that are controlled by voltage biased current mirrors. his approach was chosen because current-starved inverters provide fine control over propagation delay by modulating the current available to the inverter transistors [1].

Such tunability is critical for accurate pulse shaping and for ensuring that the sub-pulses align correctly to form a stable UWB waveform.

The delay cell (sized the same as shown in Table 3.1 and Figure 3.4) is then connected to a minimum sized inverter to drive the consecutive delay cell. This was done to make the triggering edge leading to the pulse generator consistent across all delay cells and compensate for the weak driving capability of current starved inverters. The architecture of the delay cell used within the delay line is shown in Figure 3.10.

Each delay cell will have their own voltage biasing to prevent PVT variations from affecting the biasing and to ensure a reliable delay between each sub-pulse. Although this approach requires additional biasing pins connected to the outside of the chip, it provides programmability and flexibility. This not only ensures robust operation under varying conditions but also allows post-silicon tuning, which is valuable for experimental characterization and for testing alternative pulse structures in future revisions.

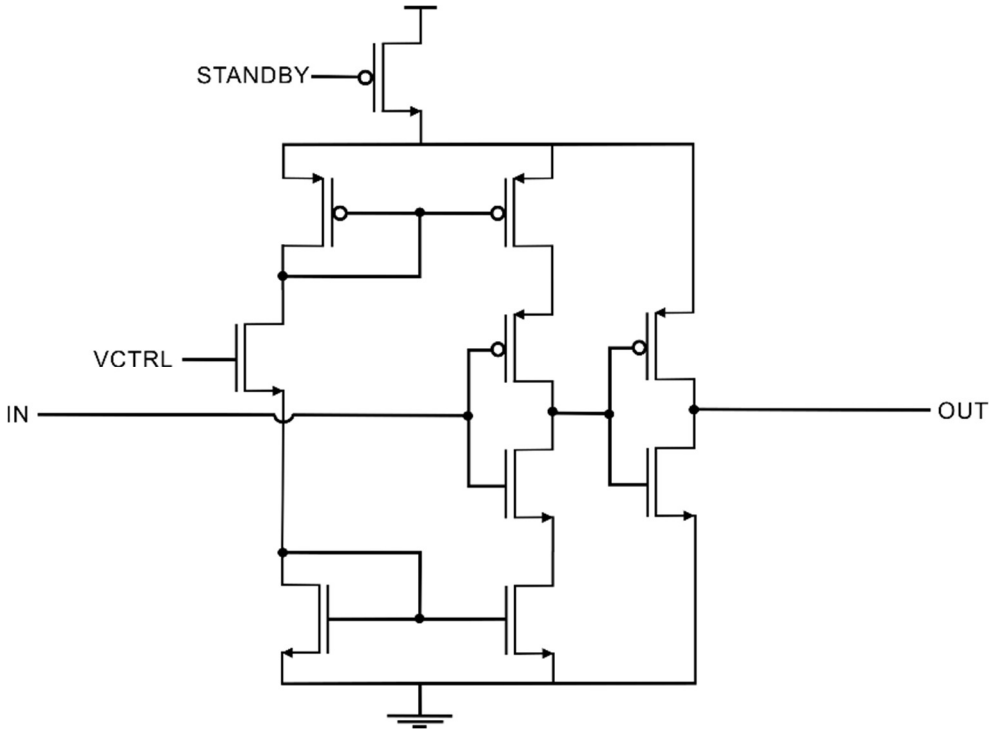


Figure 3.10: Delay Cell for Delay Line Architecture

3.5.4. Pulse generator

The pulse generator uses the delayed rising edges from the delay cells and creates a small pulse with a pulse width corresponding to the period of the required center frequency of the UWB pulse. It uses a glitch generator architecture which is comprised of a delay cell and a logic CMOS AND gate.

The delay cell (sized the same as shown in Table 3.1 and Figure 3.4) creates a falling output edge from a rising input edge with a controllable delay between the two edges. The delay is created by a current starved inverter and controlled by the voltage biasing the current mirror. This choice allows fine-tuning of the generated pulse width, which directly determines the effective bandwidth

of the transmitted UWB signal. By adjusting the bias voltage, the designer can calibrate the pulse width to achieve compliance with spectral masks such as the FCC UWB emission limits.

The AND gate would generate a short pulse when AND'ing the two signals. This method is simple and energy efficient, as it relies on standard digital CMOS logic rather than analog shaping circuits, making it highly compatible with deep submicron processes used for system-on-chip integration. The full architecture of the pulse generator is shown in Figure 3.7 and the simulation results from varying the V_{CTRL} (1.1 V to 1.75 V using 50mV steps) is shown in Figure 3.8. The higher the V V_{CTRL} CTRL voltage is the more current can flow through the delay cell, giving a lower delay, which produces a smaller pulse width.

The pulse width is therefore programmable and enables the transmitter to transmit at a wide range of center frequencies and bandwidths. In practice, this programmability provides two key advantages: (i) the ability to optimize link performance under different propagation conditions (e.g., tissue depth, receiver distance), and (ii) the flexibility to test multiple center frequencies and bandwidths in experimental settings without redesigning the hardware. Moreover, the inclusion of the *standby* control further reduces static power consumption by disabling the glitch generator when no pulses are needed, aligning with the ultra-low-power goals of neural implants.

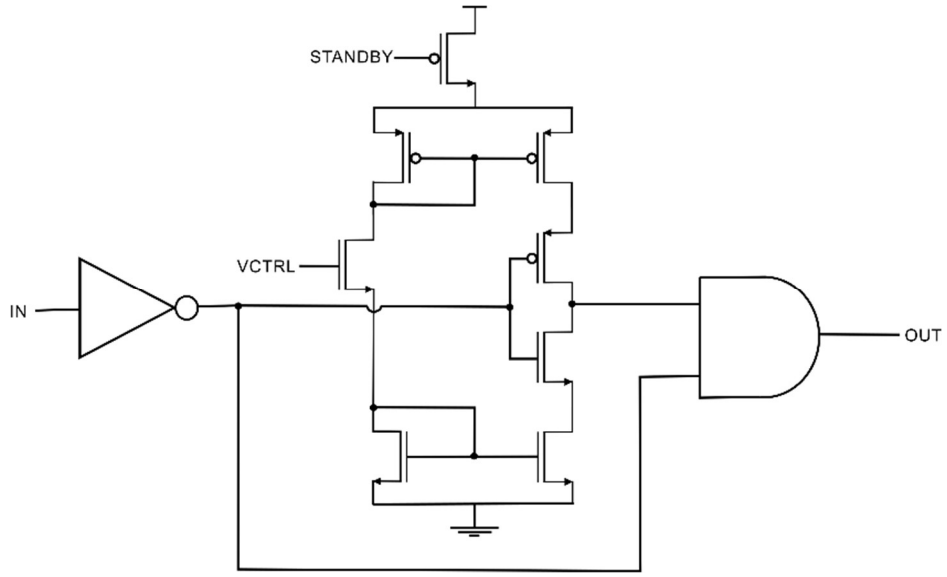


Figure 3.7: Pulse Generator Architecture

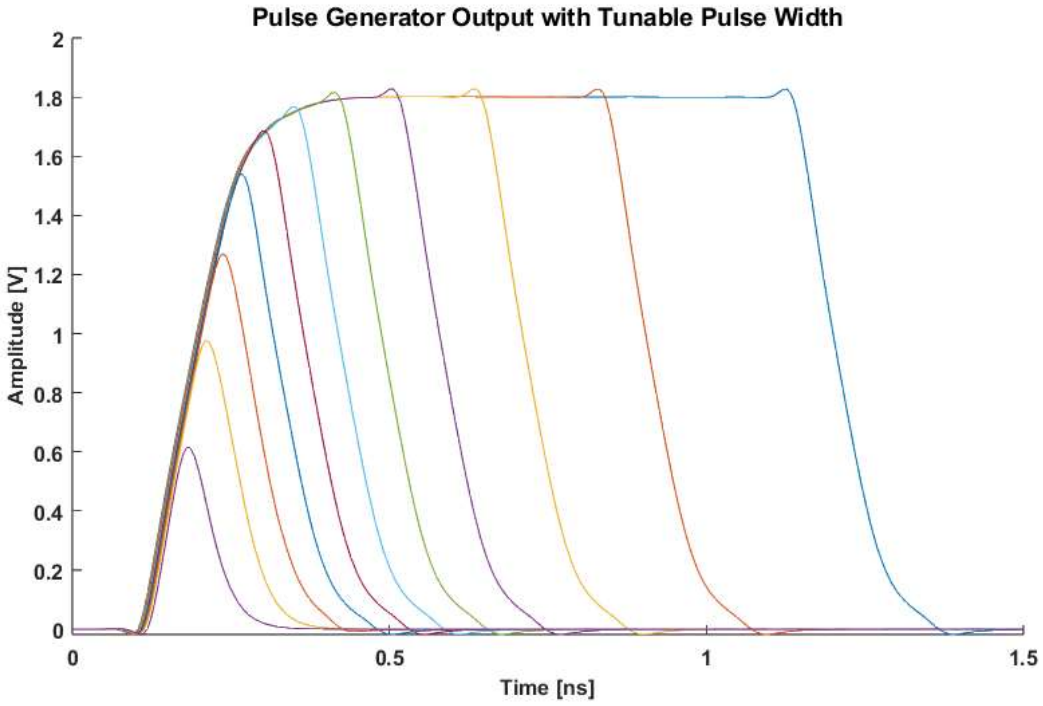


Figure 3.8: Simulation results of Pulse Generator showing OUT signal whilst varying VCTRL

3.5.5. Power Amplifier (PA)

The power amplifier is responsible for amplifying the power sent into the antenna and aims to shape the UWB pulse. It is composed of 8-unit power amplifiers that effectively amplify the sub-pulse by turning on a series of NMOS/PMOS transistors to pull the output signal high and then low. The full power amplifier architecture is shown in Figure 3.9. Each unit PA is composed of a tri-state buffer that can drive the output to VDD, VSS, and High-Z. The High-Z mode is particularly important, as it allows the unused unit PAs to be disabled, preventing static current draw and improving energy efficiency. The unit PA architecture is shown in Figure 3.10.

These transistors turn ON/OFF in parallel allowing more current through each transistor and is programmable by taking the unit PA out of the High-Z mode where both the NMOS and PMOS are turned OFF. The final inverting stage PMOS and NMOS are sized 2.16 μm/0.18 μm and 1.08 μm/ 0.18 μm, respectively. This parallelization provides fine-grained programmability of the output drive strength: by enabling more unit PAs, the effective output current and thus the transmitted pulse amplitude can be increased. Conversely, disabling units reduces the drive strength and conserves energy. This enables adaptive trade-offs between link margin and power consumption depending on operating conditions (e.g., implant depth, receiver distance, or channel quality).

Additionally, the tri-state buffer design ensures that the PA has fast switching speed while avoiding shoot-through current, which is essential for preserving the sharp edges of the UWB pulse. Maintaining pulse fidelity directly impacts the spectral mask compliance and the efficiency of energy detection at the receiver. Finally, because the unit PAs operate as digitally controlled blocks,

the architecture scales well with CMOS technology, simplifying layout and integration with the rest of the transmitter.

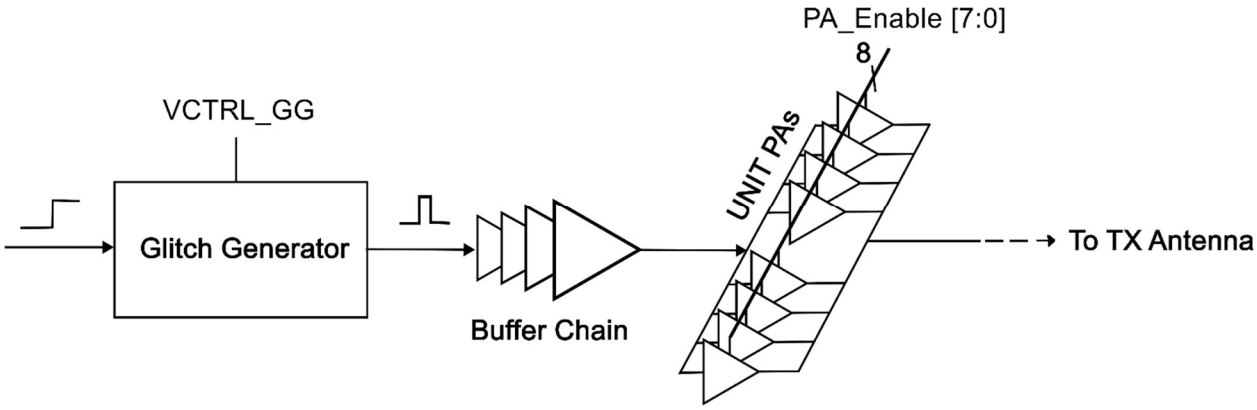


Figure 3.9: Architecture of the Power Amplifier

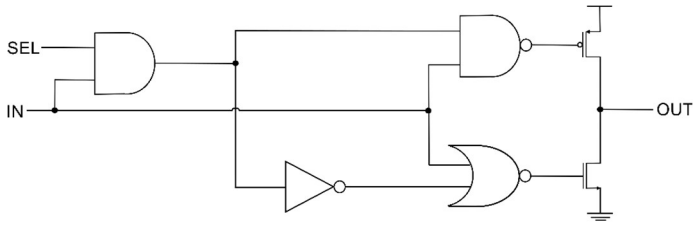


Figure 3.10: Architecture of the Unit Power Amplifier

3.5.6. Filter and Antenna Design

The final stage of the UWB transmitter is the filter and antenna. The filter is meant to differentiate the generated the UWB pulse which further shapes the pulse seen by the antenna. By differentiating the UWB pulse, the pulse is transformed from switching between low/high logic levels to between a negative and positive amplitude. This removes low-frequency components within the original signal that jeopardize the signals spectral compliance with FCC requirements.

A 5^{th} and 3^{rd} order Chebyshev LC bandpass filter was simulated to supress unwanted low-frequency components, but a clear issue arises with adding inductors into the path of the RF signal. As the LC bandpass filter contains LC tanks that resonate at a chosen frequency, the energy within

the inductor and capacitor oscillates causing large ringing in the output of the signal. This is to be expected as the UWB pulse being fed into the filter acts like an impulse and this produces the filters impulse response which is a ringing chirp signal. This effect extends the width of the pulse to more than 100 ns (original pulse width of 2ns) which proportionally shrinks the bandwidth of the signal below 500 MHz which severely reduces the bandwidth of the channel (reducing overall data rate) and produces a signal that isn't FCC compliant. Instead, a single capacitor was chosen to act as a high pass filter (HPF). This solution achieves the desirable differentiation and DC blocking functionality without the ringing.

The antenna was designed using High Frequency Structural Simulation (HFSS) software. The goal of the design was to create UWB patch antennas that achieve the highest efficiency and lowest signal losses at the desired center frequency (4 GHz) and bandwidth (500 MHz). The antenna will use an FR4 substrate (dielectric constant of 4.4 and a thickness of 1.6 mm) so that it can be fabricated using standard Printed Circuit Board (PCB) manufacturers.

In total, three geometries were simulated for the conductor and ground plane of the UWB patch antenna: the circular patch antenna and a semi-circular patch antenna as seen in Figure 3.11. By doing a frequency domain analysis, the Voltage Standing Wave Ratio (VSWR) and the S11 parameter (reflection coefficient) can be extracted. The VSWR shows the mismatch between the antenna and the feedline indicating whether the geometry of the antenna and feedline are appropriate, a VSWR of 1 means that there is no mismatch between the feedline and antenna. The S11 parameter shows the reflection of signal power at the port of the antenna which can be used to analyze which frequencies does the antenna resonate at and therefore propagate through the air wirelessly.

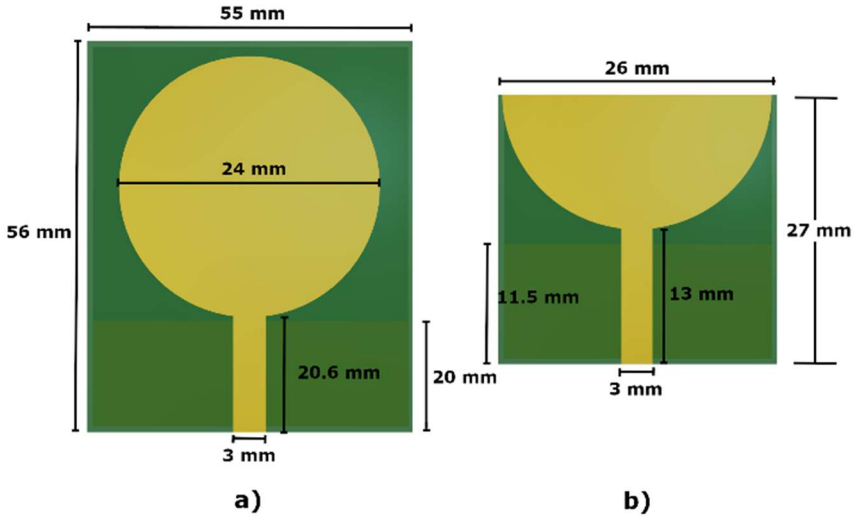


Figure 3.11: Circular and Semi-Circular Patch Antennas Dimensions

As seen in Appendix A.3, the results of the analysis indicate that the Semi-Circular Patch Antenna is the best candidate due to its performance with a S11 of – 16.72 dB and a VSWR of 1.34 at 4 GHz. The antenna of choice will use an SMA connector to connect to the PCB housing the custom chip.

3.6. PVT Variations and PLS Simulation Results

As all CMOS technologies are susceptible to variations in Process, Voltage, and Temperature (PVT) a thorough investigation must be conducted to determine how the performance of the design changes with these variations. The overarching strategy used to compensate for PVT variations were through programmability. By adding externally adjustable voltage references for the delay cells in the PPM modulator and pulse generators the shape of the pulse can be adjusted.

PVT variations affect the propagation delay of logic gates and the threshold voltage which directly influence the timing accuracy and amplitude of the generated UWB pulses. These changes can manifest as pulse-width distortion, jitter, or a shift in center frequency, ultimately degrading system

performance if left uncompensated. Programmable biasing enables fine-tuning of the circuit response post-fabrication, ensuring that the pulse width and timing remain within specification across different operating conditions. As seen in Figure 3.12, the required PPM modulator of up to 50 ns can be achieved meaning a large range of delays can be achieved regardless of variation in process. The intended center frequency is 4 GHz meaning that a delay of 150 ps must be achieved across all corners (shown in Figure 3.13).

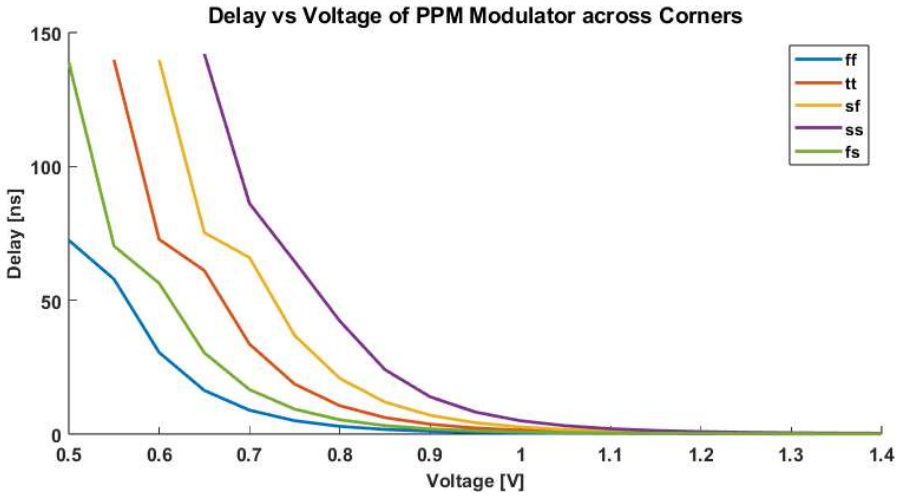


Figure 3.12: Delay Vs Control Voltage of PPM Modulator across Corners

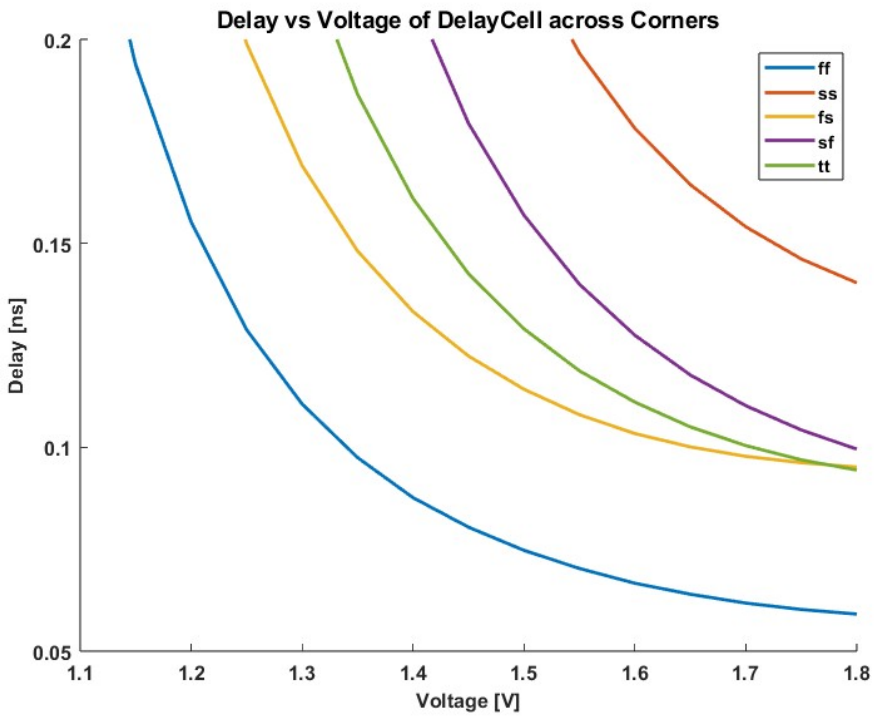


Figure 3.13: Delay Vs Control Voltage of Delay Cell in Pulse Generator across Corners

Finally, after creating the layout for the transmitter and extracting parasitics using Calibre. A post layout simulation of the UWB pulse can be seen in Figure 3.14.

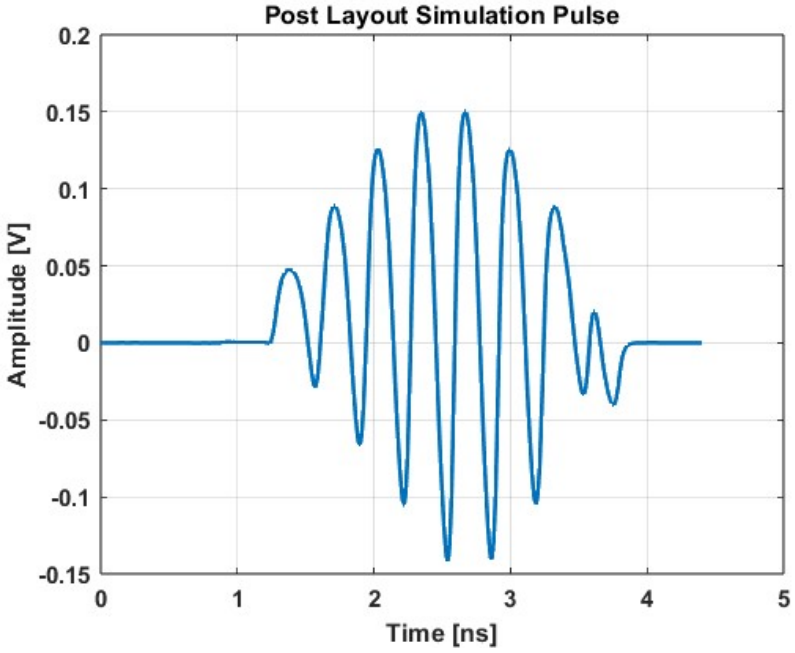


Figure 3.14: A UWB pulse generated using post layout simulation

3.7. Digital Controller

To test the UWB transmitter a digital controller must be present to feed control signals and data to be transmitted over air. The digital controller must be able to control blocks multiple blocks within the transmitter such as the Unit PAs and the delay cells state. It can do this by implementing a register file that physically connects to the UWB transmitter. This register file will be able to load data from off the chip and use it to set registers connected to the UWB transmitter's control points. Additionally, the digital controller will function as a pseudo RFE plus a digital signal processor. As seen in Figure 3.14, the shift registers, serializer, and data compression block will be implemented within the same digital controller.

The LC-ADC based recording front-end will read data incoming off-chip to simulate the level crossings produced by the LC-ADC. A total of 8 channels will be implemented on-chip and will take DATA and DIR signals from off chip. These signals will be shifted into shift registers within the digital controller and will be compressed using the compression block described in Chapter 2. The digital controller will facilitate the data acquisition by clocking in data at a clock frequency proportional to the expected T_{GRAN} of 190 us (5.2 kHz) and to then to create a signal that will be fed directly to the UWB transmitter that has a clock frequency proportional to the expected required PRF of 7 MHz. To communicate the start and end of each packet a programmable sequence of bits will be sent out as the start/stop symbol.

This digital system will be implemented in SystemVerilog and Xcelium will be used to verify functionality. Once verified, genus will be used to synthesize the digital controller using a netlist comprised of standard digital cell library for the TSMC 180 nm technology. Post-Synthesis

simulations were then performed to validate the synthesized netlist by replacing the top-level module used in the functional test bench and comparing the waveforms.

A report on the area, power, and slack is shown in Table 3.2. To test the design, a start and stop bit of 3'b111 for DATA and 3'b101. The values of {16'h0000, 16'h0000, 16'h0000, 16'h0800, 16'h0200, 16'h2000, 16'h0400, 16'h3FFF} in DATA and {16'h000, 16'h000, 16'h000, 16'h000, 16'h000, 16'h000, 16'h000, 16'h000} in DIR were loaded into the LCADC registers, compressed, and then serialized to transmit. As shown in Figure 3.15, the resulting values of the TX_DATA and TX_DIR were {1'b0,1'b0,1'b0,16'h0800,6'h04,16'h2000,4'h4,16'h3FFF} and {1'b0, 1'b0, 1'b0, 16'h0000, 6'h00, 16'h0000, 4'h0, 16'h0000}, respectively. After PnR, analysis of the performance results such as power consumption, slack, and area was recorded to validate functionality and fit within the on-chip implementation. After post-PnR validation, the digital controller was imported into the Cadence IC Design suite to be integrated into the on-chip implementation along with the UWB transmitter. The full layout of the digital controller is shown in Figure 3.16.

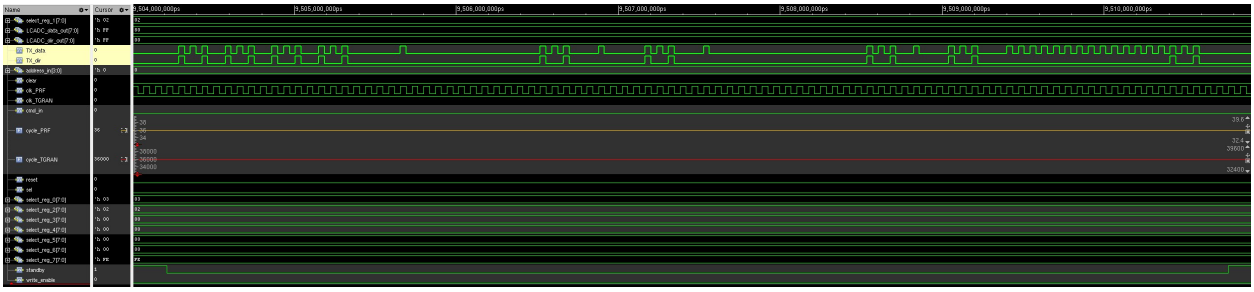


Figure 3.15: Post-Synthesis Simulation of Digital Controller

Table 3.2: A report on the Digital Controller implemented On-Chip

Cell Area	
99472 μm^2	
Power Consumption	
Registers	0.59 µW
Logic	0.12 µW
Clock	0.27 µW
Leakage	27.4 nW
Total	0.74 µW
Timing (7 MHz Clock)	
Slack (R2R)	141.9 µs

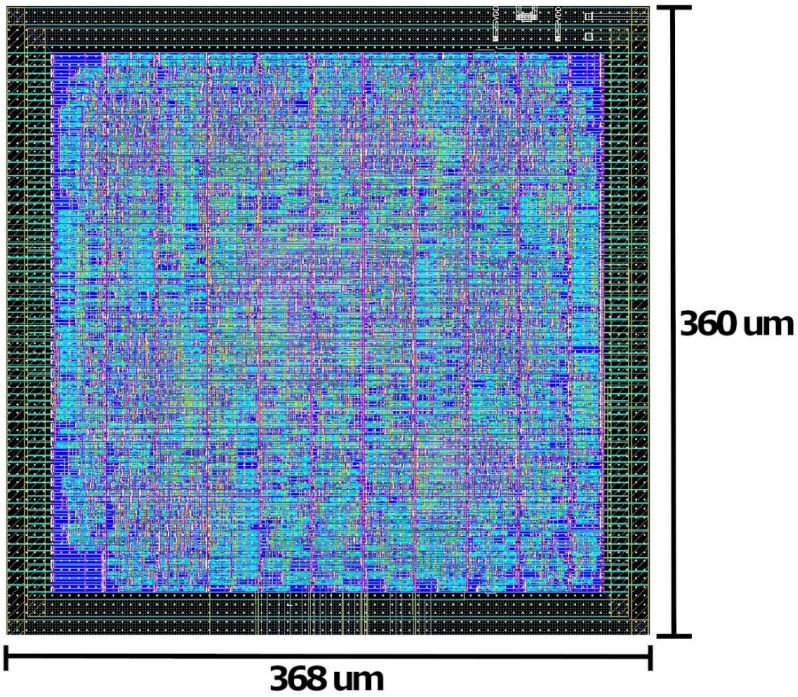


Figure 3.16: Layout of the Digital Controller

3.8. On-Chip Implementation

This transmitter and digital controller architectures were implemented on chip using the TSMC 180nm process. Between the digital controller and the UWB transmitter, a multiplexer was added to add testability to the design so that data could be fed directly to the transmitter for testing purposes. The final architecture of the circuits implemented on chip can be seen in Figure 3.17.

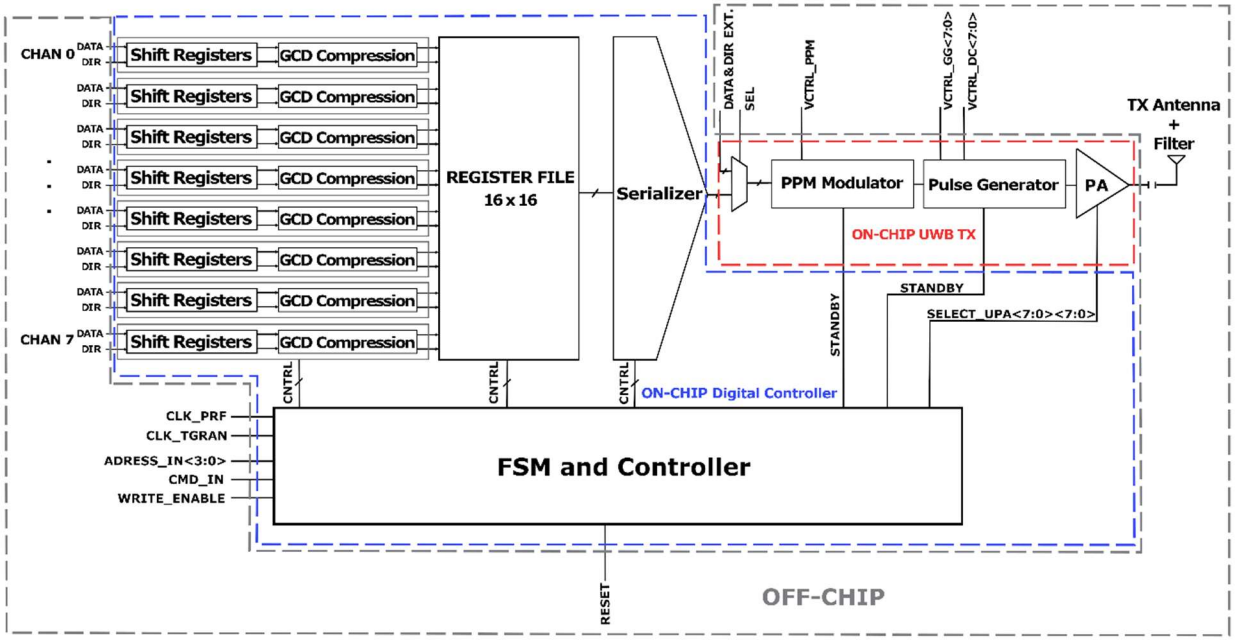


Figure 3.17: The Final Architecture of Circuits implemented On-Chip

After validating the schematic simulation of the IR-UWB transmitter architecture the layout of all individual blocks was performed. A major challenge that was identified during post-layout simulation (PLS) was skewed delays between pulses due to the geometry used in layout. As each block were tightly placed together a goal was to make sure that the parasitic capacitances between the interconnects did not dominate the delay experienced at each node.

For this reason, extra care was taken into making sure that the interconnecting wires between delay sensitive blocks such as the delay cells connecting to the pulse generators were kept equal. This would ensure that the capacitances seen along the pulse generators were made to be as similar as

possible ensuring equal timing between the generation of the sub-pulses and their propagation to the output node. The delay cells are controllable meaning that the delay between each delay cell in the delay line and the pulse widths were adjustable but the propagation delay between the pulse generator and the output must be kept the same. The layout was done within a 2 x 3 mm area as was assigned to by CMC Microsystems along with LCADC channels and other test circuitry.

The digital back-end controller was also implemented on-chip along with the transmitter to control different features of the transmitter such as the programmable unit power amplifiers, modulator, and the standby feature can be controlled on-chip. The digital controller was placed close to the transmitter to reduce the signal paths to the transmitter to achieve a predictable performance. Bypass capacitors were also added to the power ring surrounding the digital controller to stabilize the 1.8V VDD. The full layout of the chip is shown in Figure 3.18.

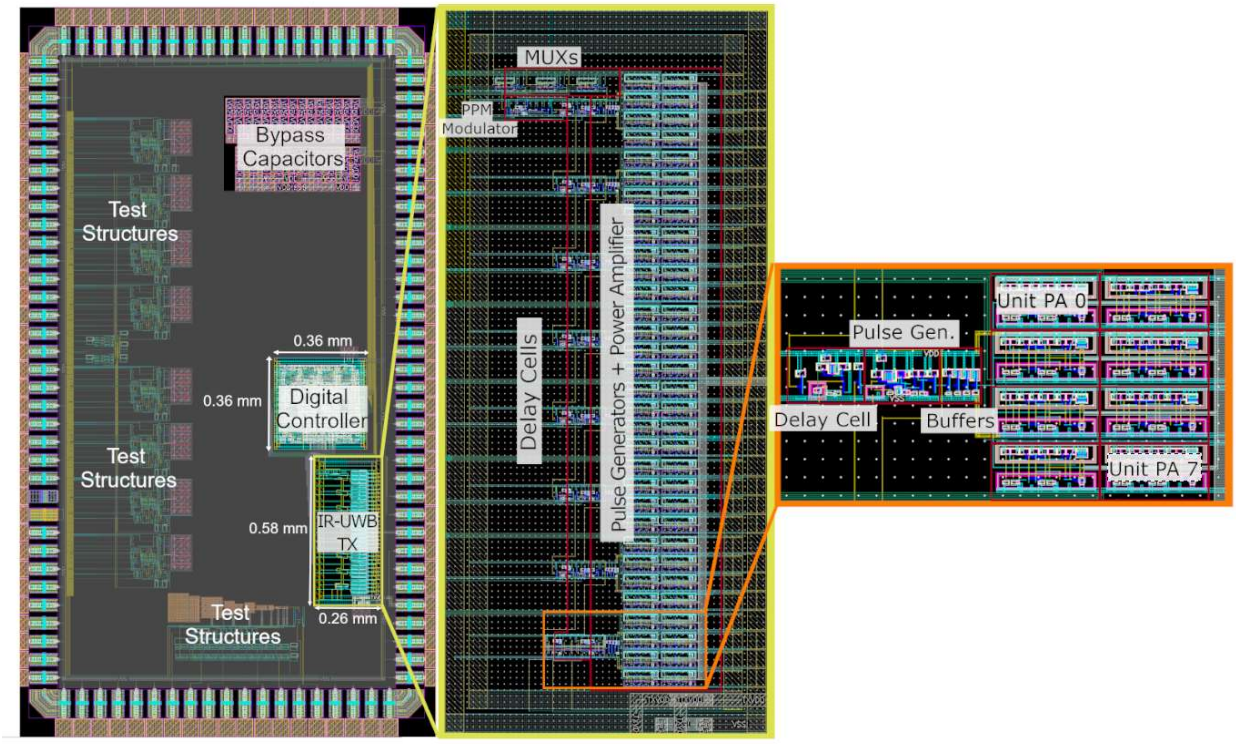


Figure 3.18: Full Chip Layout showing Digital Controller and UWB Transmitter

Chapter 4:

Testing, Validation, and Discussion

After fabrication, the custom UWB transmitter and digital controller will be tested, validated, and compared to state-of-the-art systems. To test the system-level performance of the transmitter a UWB receiver is required to extract performance metrics such as data rate, BER, and energy efficiency. For this reason, a receiver was designed using commercial components and validated using a commercial UWB transmitter to test the uplink. In this chapter, a description of measurement plans, test benches, and measurements results will be presented to be able to accurately report its performance.

4.1. Receiver Architecture

As the UWB transmitter is programmable and configurable, the demodulation at the receiver must remain flexible to properly test the throughput and efficiency of the transmitter. Given this demand, the receiver is comprised of an antenna, a bandpass filter, and a low-noise amplifier (LNA). The LNA feeds its output to a real-time oscilloscope with a 33 GHz bandwidth (DPO70000SX). As the incoming symbols use a PPM modulation, the signal can be demodulated using digital signal processing (DSP) algorithms to determine the position of the pulse relative to its symbol window.

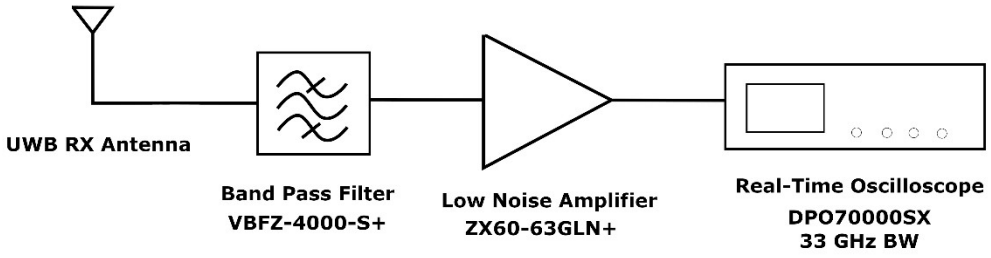


Figure 4.1: Receiver Top-Level Architecture

To assure proper matching between the transmitter and receiver antenna, the receiver antenna is chosen to be identical to the transmitter antenna (semi-circular patch antenna) this will ensure a reliable matching. The RF bandpass filter (BPF) requires a center frequency of 4 GHz and a minimum bandwidth of 500 MHz. The LNA must operate within the intended frequency range of the transmitter (4 GHz center frequency with a minimum 500 MHz BW). Ultimately, the VBFZ-4000-S+ commercial 4 GHz RF bandpass filter by Mini-Circuits [99] and the ZX60-63GLN+ RF LNA by Mini-Circuits [100] was chosen.

To isolate the transmitters performance, the receiver chain was characterized to be able to accurately identify the transmitter output power, SNR, etc. Specifically, the insertion loss of the BPF and the gain and NF of the LNA must be identified. By using Vector Network Analyzer (PNA-X), the S-Parameters and Noise Figure were measured and reported for both the LNA (shown in Figure 4.2) and BPF (shown in Figure 4.3). At 4 GHz, the LNA was shown to be 22.6 dB, the NF of the LNA is 2.4, and the insertion loss of the BPF is 1.16 dB.

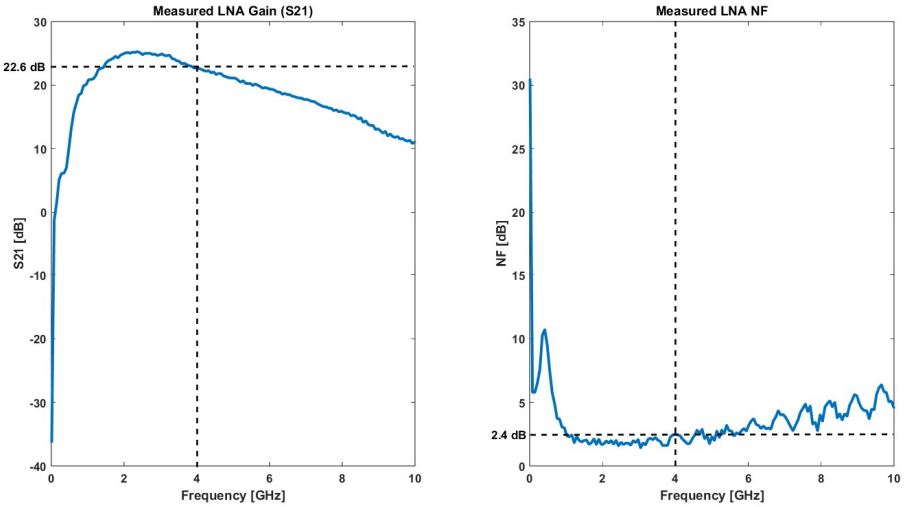


Figure 4.2: Measured Gain and NF of the LNA (ZX60-63GLN+)

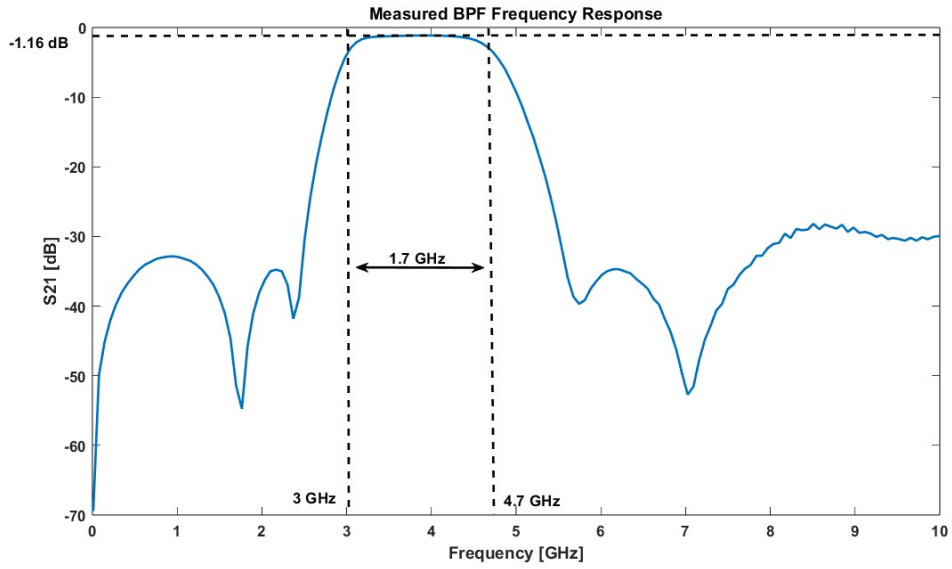


Figure 4.3: Measured Frequency Response of the BPF (VBFZ-4000-S+)

4.2. Testing and Validation

The testing of the custom UWB transmitter will be split into three phases: (1) testing a commercial transmitter with a commercial receiver and antenna, (2) testing a commercial transmitter with a commercial receiver and a custom antenna, and (3) testing the custom-designed transmitter IC with a commercial receiver and a custom antenna. These three phases will require individual custom PCBs.

4.2.1. Commercial Integrated Tx with a Commercial Rx and Antenna

The first phase was used to validate the function and expected performance of the bandpass filter, LNA, and real-time oscilloscope. It uses a commercial UWB antenna such as the FXUWB10.01.0100C UWB antenna by Taoglas [101]. By transmitting UWB pulses, the receiver architecture should be able to capture the transmitted UWB pulse and display it for measurements

on the oscilloscope. For this purpose, the DWM1000 IR-UWB transmitter was chosen as it uses a commercial transmitter that produces IR-UWB pulses centered at 4 GHz with a minimum bandwidth of 500 MHz and comes with an integrated UWB transmitter antenna. It is a commercial IR-UWB transmitter with programmable BW, center frequency, and data rate. The first PCB was designed to house the DWM1000 module and breakout its connections so that it can be interfaced with an Arduino Mega board (shown in Figure 4.4 and Figure 4.5).

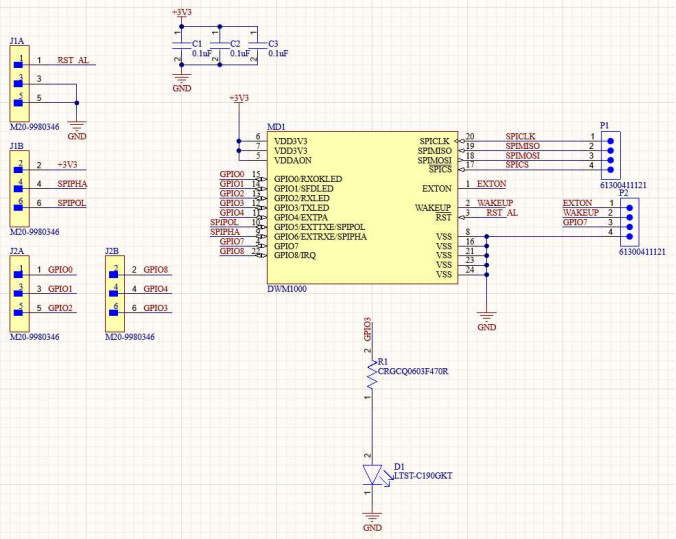


Figure 4.4: Schematic of DWM1000 PCB

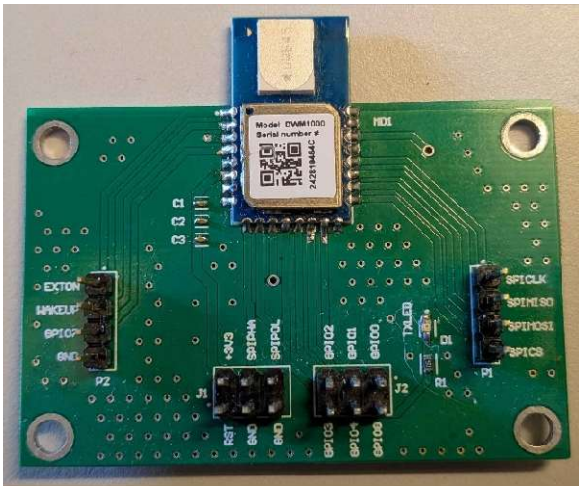


Figure 4.5: Picture of the PCB housing the DWM1000 UWB TX module

Once assembled, the transmitter was set into a Continuous Wave Mode (CWM) that produces a continuous stream of UWB pulses to test if a waveform can be captured properly on the oscilloscope (shown in Figure 4.6 in Time Domain and Figure 4.7 in Frequency Domain).

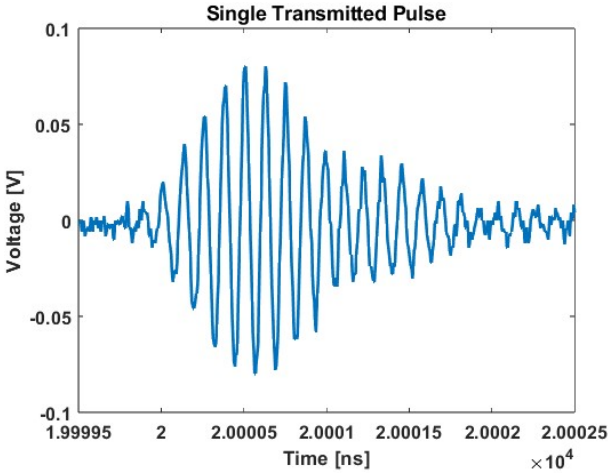


Figure 4.6: DWM1000 transmitted UWB pulses in Time Domain captured by the DPO70000SX oscilloscope.

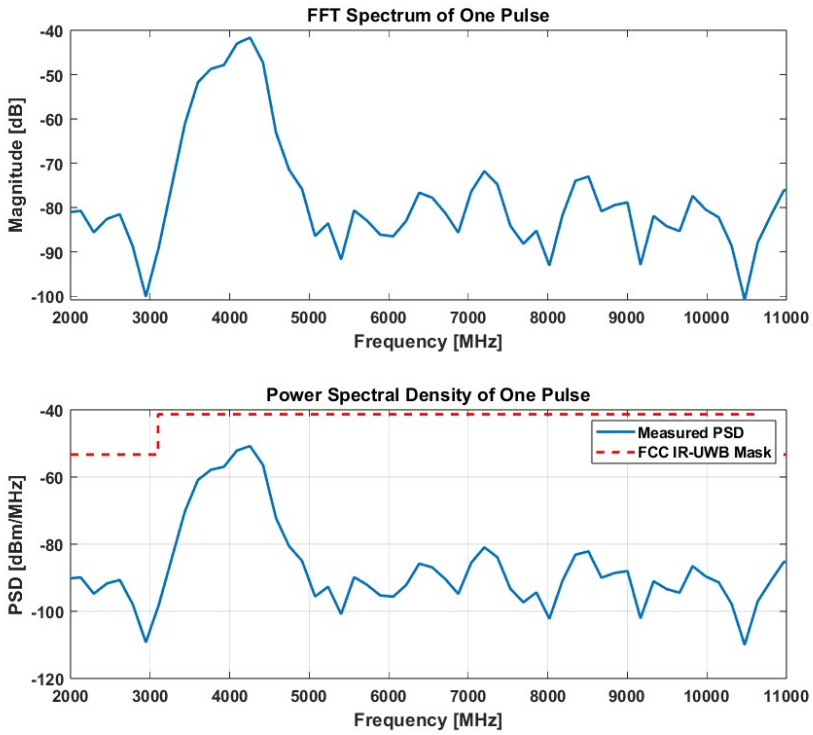


Figure 4.7: DWM1000 transmitted UWB pulses in Frequency Domain captured by the DPO70000SX oscilloscope.

Using the first PCB, the expected and measured path loss can be compared and analyzed. By using the VNA, the gain between the TX and RX antenna can be measured. The path loss was measured at three distances (5 cm, 10 cm, and 20 cm) the path loss measured is shown in Figure 4.8 (-17 dB, -24 dB, and -30.5 at 4 GHz respectively).

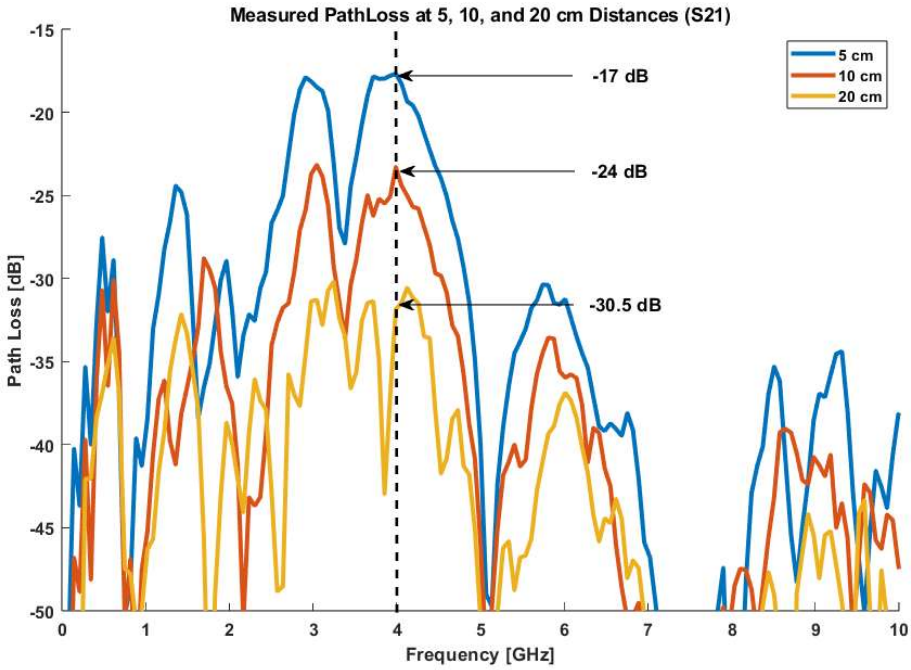


Figure 4.8: The path loss measured at 5, 10, and 20 cm distance of the custom circular antenna

4.2.2. Commercial Transmitter with a Commercial Receiver and Custom Antenna

As the DWM1000 module packages the DW1000 UWB transmitter and an integrated UWB antenna, a second PCB was designed to verify the functionality of the custom antennas, which will be later used with our custom-designed transmitters, and to validate the procedure used to directly measure the transmitter's output on the oscilloscope. This test will be useful as it will validate the shape of the pulse before it is fed to the antenna and radiated into free space. The PCB contains a series of biasing circuits, an external XTAL to provide the transmitter with a clock, voltage regulators (3.3V and 1.8V), bypass capacitors, and communication pins. The schematic is shown in Figure 4.9 and the assembled view shown in Figure 4.10. It was fabricated by JLCPCB using a

custom PCB stack-up to control the impedance of the transmitters RF output to the balun and the output of the balun to the SMA connector. The semi-circular patch antenna was tested to validate the TX antenna and full commercial RX chain. An Arduino was used to communicate with the transmitter over an SPI link and registers such as TX_POWER (power control), TX_BUFFER (transmission data buffer), etc. were modified to test the transmitters performance metrics.

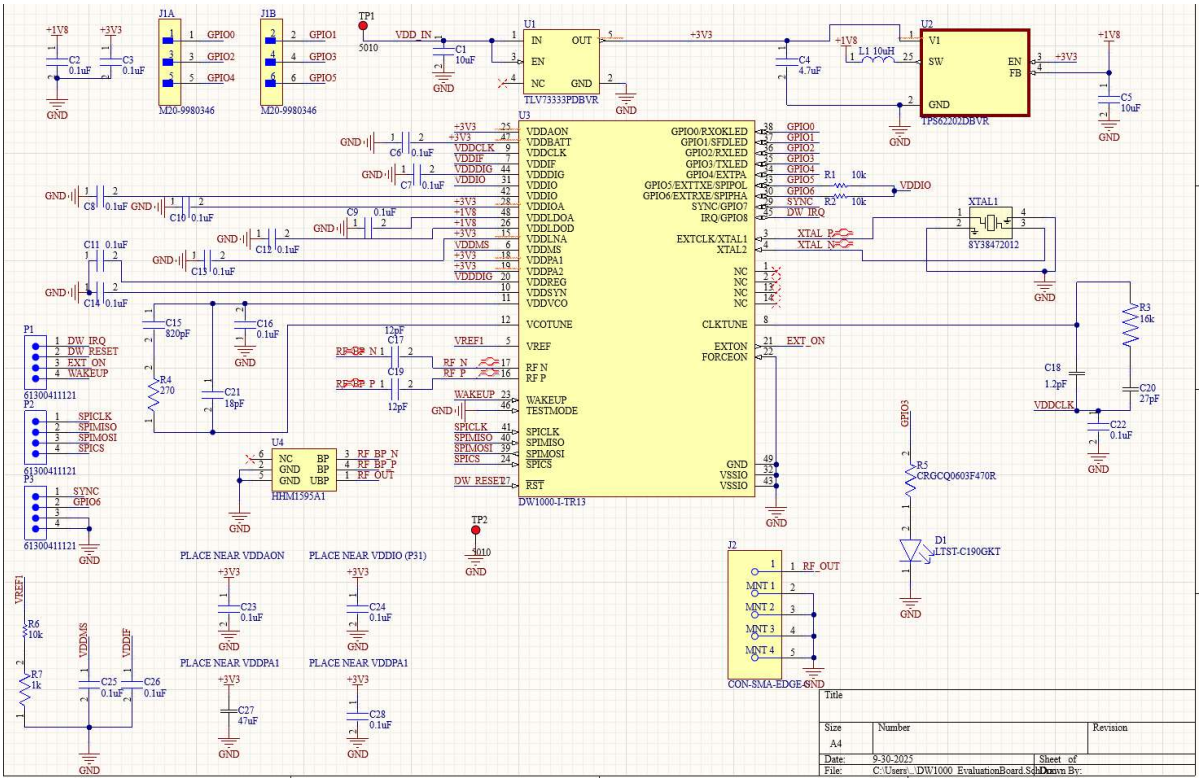


Figure 4.9: Schematic of the DW1000 Evaluation PCB

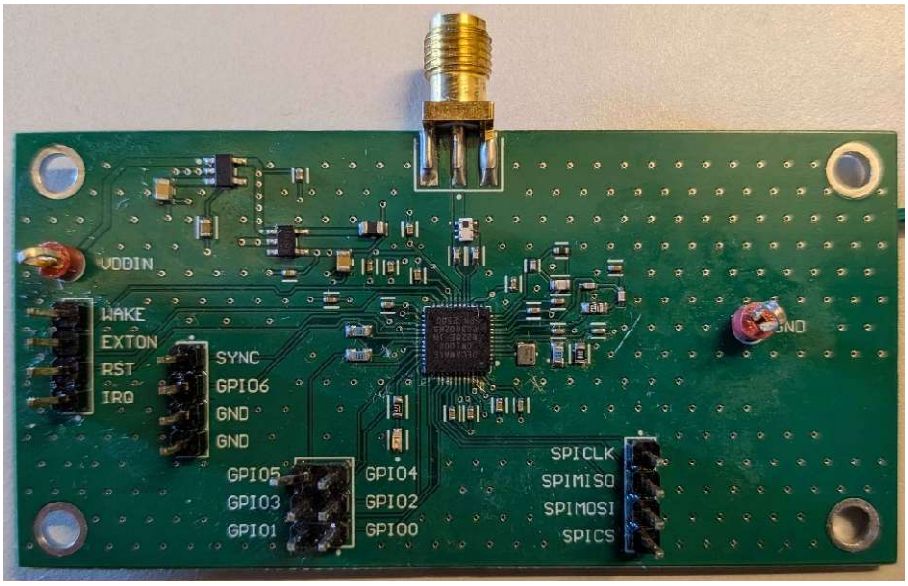


Figure 4.10: 3D view of the DW1000 Evaluation PCB

Once assembled, the transmitter was directly plugged into the real-time oscilloscope and the UWB pulse was recorded both in the Time Domain (shown in Figure 4.11) and in the Frequency Domain (shown in Figure 4.12). As shown, the PSD of the transmitted pulse are centered at 4 GHz and complies with the FCC spectral mask. Additionally, as the output of the transmitter can be directly measured a comparison can be made between the transmitted and received signal power. The transmitted signal power was measured to be 156 µW (-8 dBm) and the received power was measured to be 100 µW (-10 dBm) at a distance of 10 cm, including a path loss of -24 dB and a gain of 22 dB, the resulting loss of power is 2 dB which validates the received power being 2 dB lower than the transmitted meaning that the outline model is accurate and can be used to extract the performance metrics of the custom UWB transmitter.

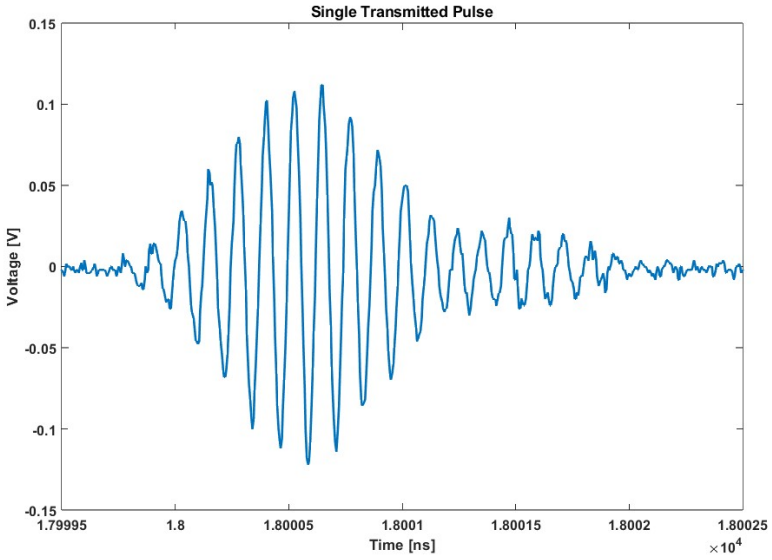


Figure 4.11: UWB pulse recorded in the Time Domain directly at the output of the DW1000 Evaluation PCB

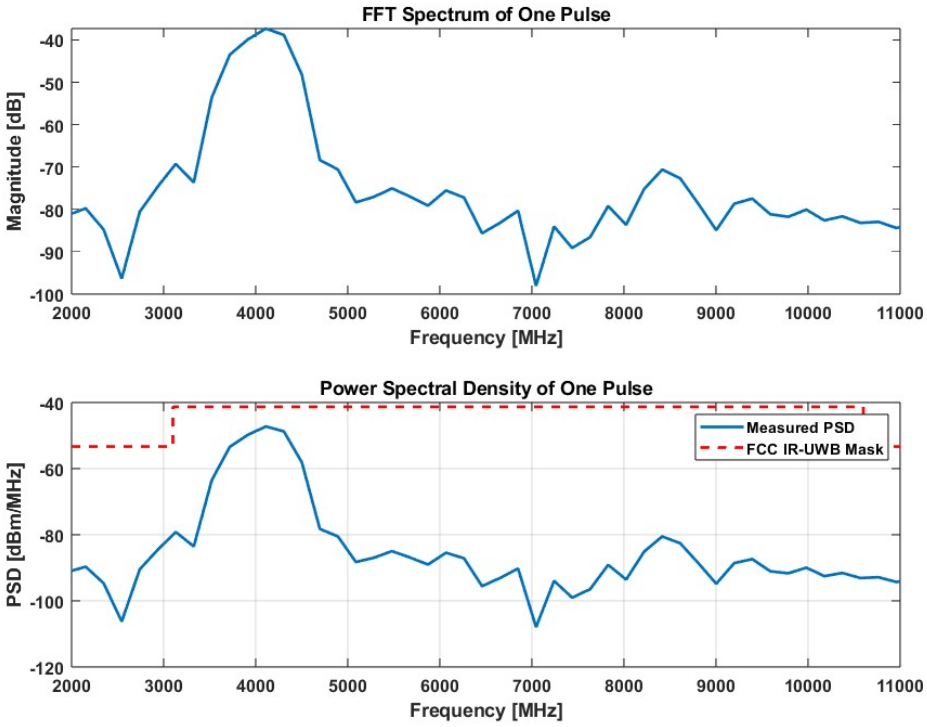


Figure 4.12: UWB pulse recorded in the Frequency Domain and PSD directly at the output of the DW1000 Transmitter

4.2.3. Custom Designed Transmitter IC with Custom Antenna and Commercial Receiver

The third PCB houses our custom-designed IR-UWB transmitter IC. Firstly, as a on-chip UWB TX antenna is out of scope for this design, we opted for an off-chip antenna and filter. This was done to have control over the filters components values and provide further testability to the overall design. It contains a 9 dual channel 12-bit DACs (MCP47CMB22) that were used for the voltage biasing required to drive the VCTRL_PPM (PPM modulator voltage control), VCTRL_GG (Pulse Generator voltage control), and VCTRL_DC (Delay Cell Voltage Control). These DACs use an I2C protocol meaning that they can be programmed using the on-board FPGA. The iCE40LP1K-QN84 Lattice FPGA was chosen as the ideal candidate to control the UWB TX IC due to the number of I/Os present (required to interact with the on-chip digital controller) and its compatibility with 1.8V CMOS logic.

The FPGA uses an external clock generator IC to provide a 25 MHz clock (ASE-25.000MHZ-LC-T) to the FPGA's global input pin. Additionally, Lattice offers FPGA development software such as iCECube2 to synthesize System Verilog code into a .bin file which will be uploaded to a SPI flash (IS25LP040E-JNLE) located on the PCB. A series of tunable low-drop out voltage regulators were placed on the board to supply the 3.3V required for SPI communication, 1.8V for the on-chip transmitter, digital controller, and the FPGA VCCIO, and 1.2V for the core logic circuits of the FPGA. A schematic of the final PCB testbench is shown in Appendix A.2 and a 3D view can be seen in Figure 4.13.

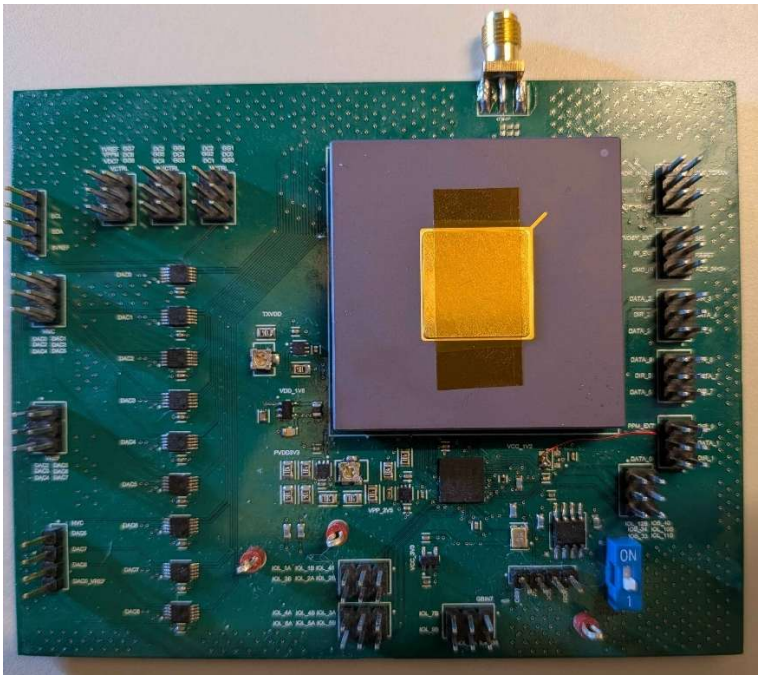


Figure 4.13: 3D view of the custom UWB TX IC PCB

Once assembled, the PCB's function was validated by testing the voltage regulators under load. The DACs One-Time Programmable memory was programmed to contain different DAC addressing so that a single I2C bus could address all 19 DACs. The DACs output was also measured to make sure that the functionality is as expected. A clock generator circuit is then tested by probing its output pin and verify the waveform of the clock. An open-source software called AsProgrammer was used to upload the to the FPGAs FLASH memory. By reading its device ID, erasing, programming, and reading the contents of the FLASH the functionality of the SPI FLASH was verified.

Once programmed, the FPGA boots-up during power-on and read the configuration from the SPI FLASH to configure itself and toggle the CDONE FPGA pin high to show that the configuration

was successful. THE FPGA will be used to drive the control signals and LCADC DATA and DIR signals for the 8 recording channels present within the on-chip digital controller, provide external triggers to the on-chip UWB transmitter, and communicate with the DACs over an I2C bus. Once the functionality of the PCB was fully validated, the testing of the custom UWB transmitter IC could begin.

The first course of action to make sure that the UWB TX IC is working is to test the throughput of the pulse used to trigger an UWB pulse to be generated through the 8 delay cells on board. This was done by setting the MUX connected to the input of the transmitter to propagate external triggers into the transmitter and consequently generate an UWB pulse. The final delay cell within the chain of delay cells is connected to a buffer that passes the trigger pulse through the chip and out the DELAYLINEOUT pin of the transmitter IC. If identical but delayed version of the pulse is measured using an oscilloscope, then this would prove that the ESD diodes of the IO pads are functioning and that the main UWB transmitter is receiving power through it's VDD pin (TXVDD). Next, the on-chip digital controller will be validated by setting the SELECT_PA registers to enable the unit PAs of one single pulse generator.

Once set, the DAC that biases that pulse generators VCTRL_DC and VCTRL_GG will be set to the expected voltage and the output of the transmitter will be recorded. If successful, a single pulse should be recorded with a pulse width of a couple of nanoseconds. After testing each pulse generators functionality, the VCTRL_PPM biasing will be swept to see the delay between the external trigger and the output of the transmitter leading edge. By sweeping the VCTRL_PPM voltage, the delay will be recorded to show that a series of different PPM delays can be achieved.

At this stage, the basic functionality of the transmitter is validated, therefore the functionality of the digital controller can then be tested. The digital controller will be tested by providing signals similar to the testing of the digital controller shown in Chapter 3.7: Digital Controller. By setting the control registers and feeding the same LCADC DATA and DIR signals, a series of pulses at the output of the transmitter should be shown. A basic test can be done by enabling the digital controller to read from the LCADC channels and see if the start/stop pulses are seen at the output of the transmitter. If these pulses are shown on the oscilloscope, then the communication between the FPGA to the digital controller, communication between the digital controller and the on-chip UWB transmitter, and the PPM modulator function can be validated. Finally, the full LCADC waveforms can be fed to test the compression block, a control register to switch between no compression, lossy compression, and lossless compression can be set to verify functionality. Once validated, the next phase of testing will be to extract performance metrics of the on-chip IR-UWB transmitter.

4.3. Measurement Results

To compare the custom UWB transmitter to state-of-the-art implementations, a series of performance metrics must be established. In this section, all the measurements typically reported in state-of-the-art UWB transmitter papers will be presented. These metrics include overall waveform shape and spectral compliance, output power and energy efficiency, programmability, data rate and BER performance, timing metrics, and power consumption.

4.3.1. Output Waveform and Pulse Shape

To verify the function of the pulse generator, the output waveform will be recorded and analyzed to determine its similarity to the ideal UWB pulse generated at the transmitter. Once recorded, the center frequency, bandwidth, and pulse width can be measured. The output waveform was measured using the receiver architecture shown in Chapter 4.1. The maximum output power of the pulse is -32.3 dBm, the pulse shows a center frequency of 3.3 GHz, and a -10 dB bandwidth of 1.3 GHz confirming the successful generation of an UWB pulse. By comparing the simulated and measured pulse shown in Figure 4.14, it can be observed that the general shape is present, but the center frequency is lower than anticipated. This is most likely due to the antenna characteristics filtering the higher frequency component of the pulse.

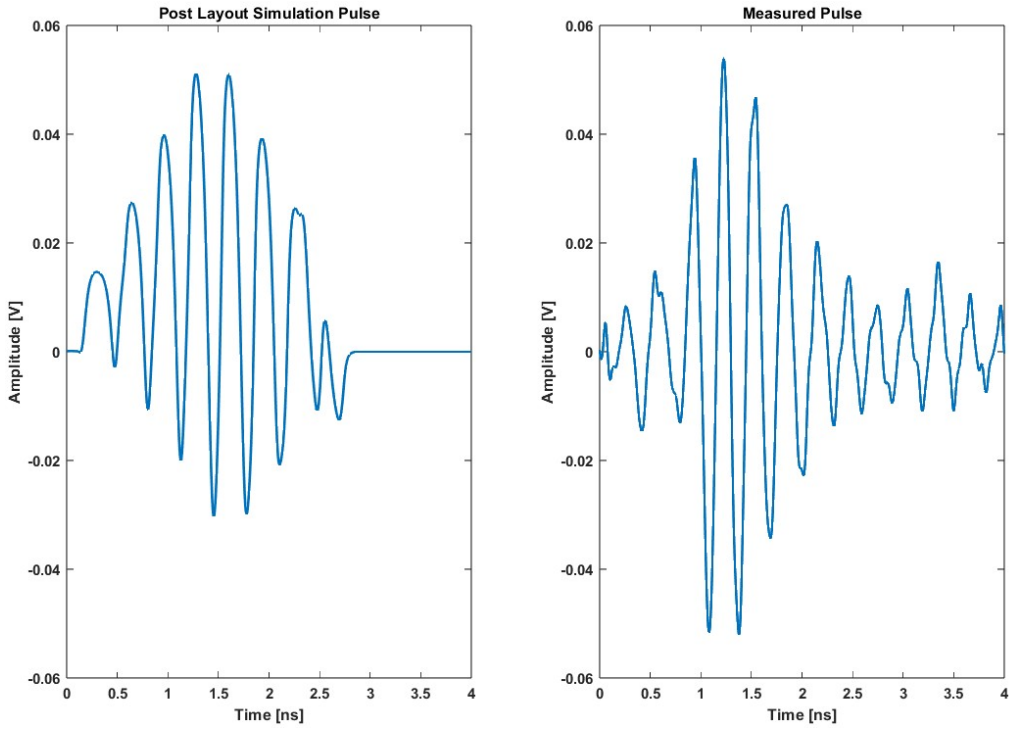


Figure 4.14: Examples of UWB Pulses Generated by the custom UWB Transmitter

4.3.2. Spectral Mask Compliance

As IR-UWB transmitter must comply with spectral standards set by the FCC and CRTC, the power spectral density (PSD) and output power must be reported. To summarize the requirements, the UWB pulse must have a -10 dB BW larger than 500 MHz, comply with the spectral mask shown in Figure 3.1. As seen in Figure 4.15, the output power is weaker than expected which is caused by sub-optimal impedance matching, but the UWB pulse is compliant of the FCC guidelines.

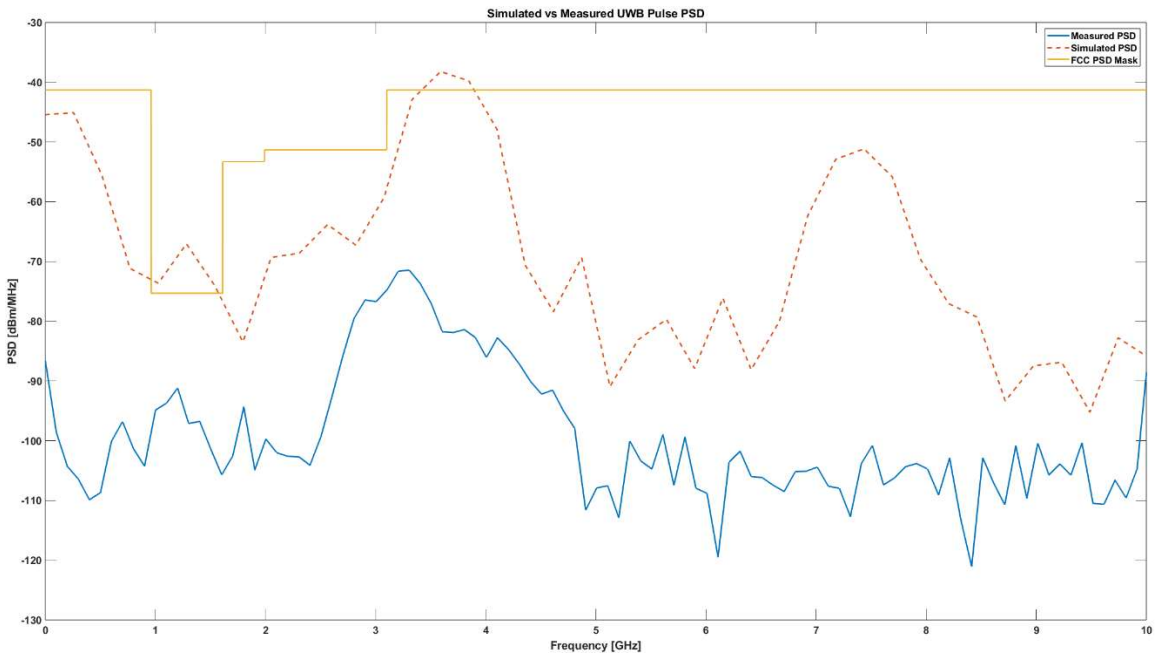


Figure 4.15: PSD of the Simulated and Measured UWB Pulse with the FCC Spectral Mask

4.3.3. Modulation

As seen in Figure 4.16, the PPM modulation implemented on-chip successfully created a stream of bits that can be demodulated at the receiver. As the receiver architecture is used to purely

sample the signal, the demodulation took place in MATLAB using a script that would assess the position of each pulse within the signal. By tuning the VCTRL_PPM voltage, a delay of 5 ns can be set for the PPM modulator to delay the UWB pulse to represent a ‘0’ bit. A PRF of 20 MHz was used to confirm the performance of the modulation scheme. The PRF was then set to the maximum before distortion between the pulses occurred which will show the base data rate, BER, and distance.

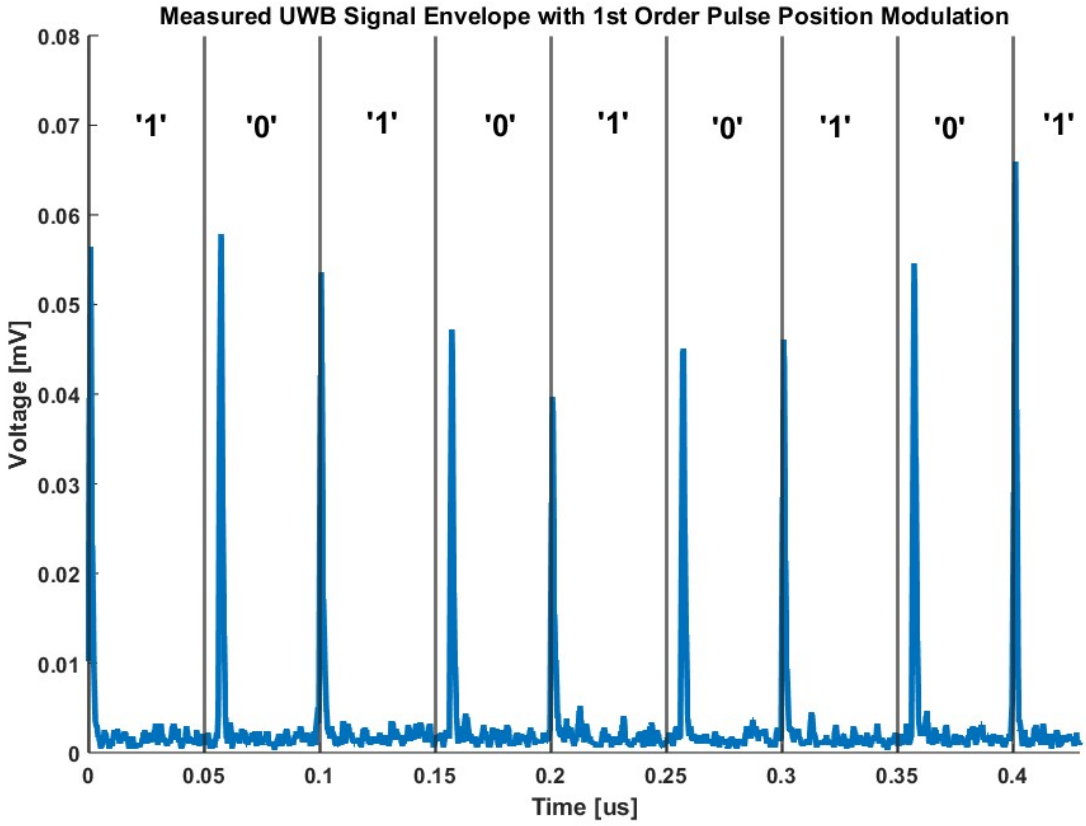


Figure 4.16: PPM Modulated UWB Pulse Train

4.3.4. Data Rate (BER, PRF, and Range)

As the data rate scales based on the modulation order, PRF, and ranges it must be tested whilst sweeping each parameter. First, the data rate and BER will be recorded by directly sending the

transmitter a digital bit stream on the DATA and DIR lines to see how the SNR at the receiver changes based on different distances. At 5 cm, the maximum base data rate was shown to be 40 Mbit/s with a BER of 3.3×10^{-5}. At 10 cm, the base data rate for a BER of 10^-3 was calculated for a data rate of 20 Mbit/s. This shows that the transmitter can achieve high base data rates at low distances ideal for neural transmitters. Given the base PRF of 40 MHz and CR values ranging from 2 – 9× (for lossless) and 2 – 14× (lossy), and the use of an LC-ADC recording front end (reduces the required data rate from 8 kb/s for a Nyquist ADC to 0.9 kb/s for an LCADC) which is an 8× improvement.

$$Data\ Rate = PRF * CR_{GCD} * CR_{LCADC} \tag{4.1}$$

The results of the compression algorithm can then be applied to determine the effective data rate of the transmitter when transmitting neural data using Equation 4.1 which results in an effective data rate of 1.4 Gbit/s using lossless compression and 3.4 Gbit/s for lossy compression.

4.3.5. Power Consumption and Area

Finally, the power consumption of the transmitter can be analyzed to determine the energy efficiency of the transmitter. At 40 MHz PRF, the power consumption of the transmitter was 0.3177 mW. This represents an energy efficiency of 8 pJ/bit when the base data rate is used. By including the compression of data achieved by the LC-ADC based recording front-end and the GCD compression the effective energy efficiency is 0.21 pJ/bit. Additionally, during periods of inactivity, the transmitter will be placed into standby mode where no UWB pulses are produced. The power consumption during the standby mode was measured to be 0.0248 mW. For the digital controller, the average power consumption was measured to be 0.4185 mW. These values are within the specifications outlined and

4.4. Comparison and Discussion

As performance will be presented, it could then be compared with the state-of-the-art UWB transmitters, and a discussion can be made to support its contributions and their value. The target performance metric to improve would be the energy per bit value. As the compression algorithm aims to reduce the size of the data required to be transmitted, the energy per bit is reduced proportionately and therefore requires less energy to transmit neural data. A mix of techniques were used to reduce this value, within the proposed neural implant architecture, such as the use of a level-crossing ADC in contrast to a traditional uniform sampling ADC, a compression algorithm further reducing the number of bits required to be transmitted, and the power consumption of the pulse generation itself needs to be reported to definitively report the effective energy per bit. A comparison between the reported metrics of the custom UWB transmitter and the state-of-the-art metrics can be seen in Table 4.1.

Table 4.1: A comparison of the measured performance metrics of this work and state-of-the-art works

Ref.	[58]	[60]	[57]	[10]	[34]	**This Work**
Pub.	ISSCC ‘25	CICC ‘25	CICC ‘24	ISSCC ‘23	ICECS ‘24	CICC ’26 (SUB)
Tech. (nm)	65	65	65	40	28	180
Architecture	Oscillator	Oscillator	Oscillator	E.C.	E.C.	E.C.
Modulation	PWM & PPM	E-PWM & PSK	OOK w Asym. Envelope	D16PPM+PWM +DBPSK	OOK	PPM
BER	$9x10^{-5}$	10^{-3}	10^{-4}	10^{-4}	N/A	$3.3x10^{-5}$
Data Rate (MHz)	52	1800	100-800	1800	40	40
3-dB BW (MHz)		1200	2900	2900	2000	1300

Center Frequency (GHz)	0.92	8	4.65	4.65		3.3
Power Consumption (mW)	0.44	28.2	13.2	4.09	0.09	0.73
Energy Consumption (pJ/bit)	8.4	15.7	16.5	2.3	3.8	17.85
Supply (V)	0.7 – 3.3	1	1.2	1.2	1.2	1.8
FoM (pJ/b/m)	N/R	N/R	26.4	N/R	N/R	357

Chapter 5:

Conclusions and Future Works

5.1. Conclusions

This thesis presented the design, on-chip implementation, and validation of a lossless data-compressive impulse radio ultra-wideband transmitter targeted for high density neural recording applications. Motivated by the growing demand for larger numbers of recording channels in neural interfaces and the dominance of wireless transmitter in implant power budgets, the works addressed the dual challenge of reducing the number of transmitted bits and making each transmitted bit more energy efficient.

A GCD-based lossless compression algorithm was introduced, leveraging the inherent sparsity in the LCADC representation of neural data. MATLAB evaluation using real ECoG recordings demonstrated a 2 to 7 times reduction in data size for lossless compression, with up to 17 times reduction in size in a lossy stride-based variant. This compression was achieved with minimal

hardware overhead and preserved neurological events. The algorithm was implemented on-chip in SystemVerilog synthesized and placed-and-routed in TSMC 180 nm technology, achieving a compact 4114 um^2 area and consuming only 44.7 μW at 7 MHz.

The digital backend controller was designed to integrate compression, serialization, and protocol management for the transmitter. It supported programmable operation, including adaptive packet sizing, standby control, and selectable compression modes. Post-layout simulation confirmed reliable operation with sub-uW power and small silicon footprint, ensuring scalability for high channel counts.

At the circuit level, a custom IR-UWB transmitter-based edge-combination pulse generation was developed. The designed employed programmable current-starved inverter delay cells, glitch generators, and edge combiners to realize sub-nanosecond pulses suitable for 2-PPM modulation. A programmable power amplifier architecture and a co-designed semi-circular patch antenna ensured compliance with FCC/CRTC emission masks while maintain link robustness. Programmable biasing was incorporated to mitigate PVT variations and allow post-fabrication tuning.

System-level simulation and experimental validation demonstrated that the integration of compression with IR-UWB transmission significantly reduced the pulse repetition frequency (PRF) requirement, lowering average power consumption while improving energy efficiency per bit.

5.2. Statement on Contribution

The proposed compression algorithm development, its behavioral and system level implementation in MATLAB was done by the author.

The digital controller implementation from SystemVerilog coding to physical layout and steps related to chip sign off are performed by the author.

The IR-UWB transmitter schematic level simulations for all blocks were designed and validated by the author.

The IR-UWB transmitter physical layout and PEX simulations was performed by the author.

The error-free layout of the chip and bond pads was implemented by the author with help from the research team.

All circuit designs, implementations, verifications and tests presented in this thesis are done by the author.

5.3. Future Directions

The proposed design shows a great potential for high density neural implants. Although, it does have room for improvement to be fully adopted and commercialized in the future. In the following sections are some of the major improvements and issues that can be investigated are discussed.

5.3.1. GCD Compression for Error Detection/Correction

As discussed in Chapter 2, the GCD algorithm works by reducing the zero-run lengths within the LCADC representation of neural data by the greatest common denominator. This means that the GCD values recovered at the receiver to decompress the data need to be integer values. If they are not, this means that there is an error that occurred when demodulating the data. In this way, the GCD algorithm at the receiver could work to detect if an error occurred by examining whether the resulting GCD value of the received packet is a whole number. If it is not, then an error within the packet is detected and the receiver can report the accuracy of the received signal based on this method. Additionally, an error correction method could be developed that compliments the error detection. This idea could be further investigated and tested to examine its effect on the BER of the communication link. It could also be implemented on a custom IR-UWB receiver IC.

5.3.2. Implementation of a Custom IR-UWB Receiver IC

As the receiver used to test the transmitter is made from commercial components and uses digital signal processing to demodulate the data, a custom IR-UWB receiver IC can be implemented to reduce the latency introduced by using DSP to demodulate and implement custom RF circuits that consume less power and are more energy efficient. The receiver could also contain a digital controller that performs the decompression of the GCD compressed neural data transmitted over air. The implementation of this receiver would compliment the presented IR-UWB transmitter by providing an end-to-end solution for high density neural recording.

5.3.3. Multi-Band IR-UWB Transmitter IC

The current implementation of the IR-UWB transmitter uses a single frequency band (centered at 4 GHz with a 500 MHz BW). By implementing a digital control over the pulse generators center frequency and BW, a multi-band IR-UWB transmitter can made to increase the throughput of the communication channel. This could increase the number of recording channels data that can be transmitted at the same time and could therefore support a greater number of recording channels.

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Appendix A.1. GCD Compression MATLAB Code

```
%iEEG_GCD Packetizing (AsyncProtocolv4)
%iEEG LCADCout spike distribution analysis
%LCADC iEEG represents 325.5208s of data
close all
duration_sec = 3600;
for stride = 0:1:1
    compression_ratios_all = [];
    for window = 16:8:16
        disp(["Window: " num2str(window)]);
        compression_ratios = [];

        %LCADC Settings
        TGRAN = 190e-6;

        %max_windows = floor(length(comp_comb)/window); %Cap on # of windows as to keep each distribution with the same number of samples for equality in histogram
        max_windows = 1000;

        % window = (time_window/duration_sec)*data_length; %Number of samples per window
        for channel = 1:1:88
            comp_up_out_all = EEG_out.comp_up_out;
            comp_down_out_all = EEG_out.comp_down_out;
            comp_up_out = comp_up_out_all(channel,:);
            comp_down_out = comp_down_out_all(channel,:);
            comp_comb = comp_up_out - comp_down_out;
```

```
data_length = length(comp_comb);
i = 1; %Track current index of comp_up_out
count = 0; %Count variable for histogram tracking
pulse_steps = 0;
packet_count = 0;
success = 0;

modif_packet = [];
orig_packet = [];
GCD_packet = [];
renorm_packet = [];
gcds = [];

while(count<max_windows) %While loop to go through all windows within sample
   if (i+window-1>length(comp_comb))
      break
   end
   data_packet = comp_comb(i:i+window-1); %Contents of individual data packets

   [data_packet_o,gcd,out,out_unc,success] =
gcd_compress_uncompress(data_packet,stride);

   if success == 1
      success = success + 1;
      %disp([count "/10000: Success!"])
   else
      disp("AAAAAAAAAAAAAAAAH");
```

```
        end
        orig_packet = [orig_packet data_packet];
        modif_packet = [modif_packet out_unc];
        GCD_packet = [GCD_packet out];
        renorm_packet = [renorm_packet data_packet_o];
        i = i+window; %Increment index by window size
        count = count + 1;
    end

    compression_ratios = [compression_ratios length(orig_packet)/length(GCD_packet)];
    %compression_ratios_all = [compression_ratios_all; compression_ratios];
%       figure;
%       histogram(gcds,'BinMethod','integers');
%       title(["Channel Num: " num2str(channel)]);
    % figure(1);
    % subplot(3,1,1)
    % stem(norm_packet);
    % title("LCADC Output");
    % subplot(3,1,2)
    % stem(GCD_packet);
    % title(["GCD Reduction - Window Size: " window]);
    % subplot(3,1,3)
    % stem(renorm_packet);
    % title("Reconstruction");

    % pause(0.5);
```

```
        end
        hold on
        plot(compression_ratios);
        title(["Compression Ratio [input length/reduced length] Window: " num2str(window)]);
        ylabel("Compression Ratio")
        xlabel("Channel #")
        drawnow
    end
    hold off
end

function [in,gcd,out,out_unc,success]= gcd_compress_uncompress(in,stride)
    [val idx] = find(in ~= 0);
    dist_test = findDistances(in);
    gcd_test = findGCD(dist_test);
    max_i = 0;
    %stride = 2;
    if length(idx) ~= 0 && gcd_test<length(in)-1
        gcds = [];
        in_test = in;
        success = 0;
        for j = 1:1:length(idx)
            in_test = in;
            i = idx(j);
            dir = 1;
            s = 1;
```

```
        val = in_test(i);
        for x = 1:1:stride*2
            in_test = in;
            if (i+(s*dir) >= stride && i+(s*dir) <= length(in)) && in_test(i+(s*dir)) == 0
                in_test(i) = 0;
                if in_test(i+(s*dir)) == 0
                    in_test(i+(s*dir)) = val;
                end
                dist = findDistances(in_test);
                gcd = findGCD(dist);
                gcds = [gcds; gcd i s dir];

                if s == stride %Problem is that s does not get incremented to stride it goes back
down
                    dir = -1;
                    s = 1;
                elseif s < stride
                    s = s + 1;
                end
            end
        end
    end
    if ~isempty(gcds)
        [~,max_i] = max(gcds(:,1));
        if gcds(max_i,1) ~= 1
            val = in(gcds(max_i,2));
            in(gcds(max_i,2)) = 0;
```

```
            in(gcds(max_i,2)+(gcds(max_i,3)*gcds(max_i,4))) = val;
        end
    end
    dist = findDistances(in);
    gcd = findGCD(dist);
    out = compressGCD(gcd,in);
    out_unc = uncompressGCD(gcd,out);
    if out_unc == in
        success = 1;
    end
  else
    dist = findDistances(in);
    gcd = findGCD(dist);
    out = compressGCD(gcd,in);
    out_unc = uncompressGCD(gcd,out);
    if out_unc == in
        success = 1;
    end
  end
end

function distances = findDistances(array)
  % Find the positions of -1 and 1 in the array
  positions = find(array == -1 | array == 1);

  % Calculate the distances between each adjacent position
```

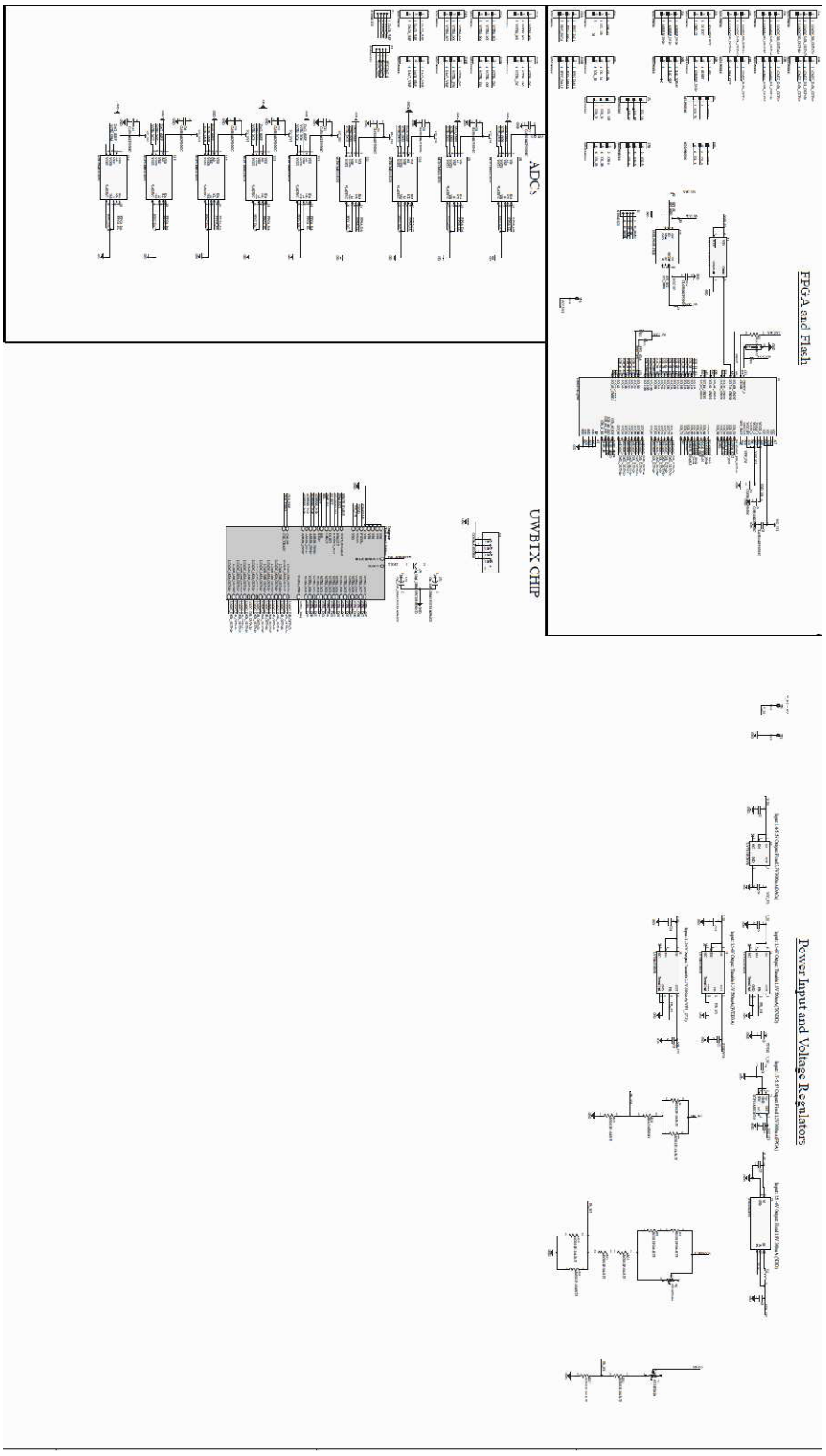
```
    distances = diff([0 positions length(array)]);
    distances = [distances(1:length(distances)-1)-1 distances(length(distances))];
end

function gcd_value = findGCD(array)
    % Remove all elements equal to 999
    array(array == 999) = [];
    if isempty(array)
        gcd_value = NaN; % If the array is empty after removing 999s, return NaN
    else
        gcd_value = array(1);
        for i = 1:length(array)
            gcd_value = gcd(gcd_value, array(i));
        end
    end
end

function array_out = compressGCD(gcd,array)
    array_out = [];
    if gcd == 1
        array_out = array;
    else
        i = 1;
        while i<=length(array)
            if array(i) == 0
                array_out = [array_out 0];
```

```
            i = i + gcd;
        else
            array_out = [array_out array(i)];
            i = i + 1;
        end
    end
end
function array_out = uncompressGCD(gcd,array)
    array_out = [];
    if gcd == 1
        array_out = array;
    else
        for i = 1:1:length(array)
            if array(i) == 0
                array_out = [array_out zeros(1,gcd)];
            else
                array_out = [array_out array(i)];
            end
        end
    end
end
```

Appendix A.2. UWB TX Test PCB Schematic



Appendix A.3. Measured S11 Parameter of UWB Antennas