CMOS CAPACITIVE SENSOR FOR CELLULAR AND MOLECULAR MONITORING

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Abstract

This thesis focuses on the design and implementation of complementary metal-oxide-semiconductor (CMOS) based capacitive sensors for life science applications. The use of CMOS capacitive sensors has shown to be effective in a variety of applications, including chemical solvent monitoring, cellular monitoring, and DNA analysis. Despite significant advances, major challenges still exist with the current CMOS capacitive biosensing technologies including extending the dynamic range of detection, diminishing the sensitivity to remnants, and rapid high-throughput monitoring.

In the second chapter, a fully integrated capacitive sensor with a wide input dynamic range (IDR) and a digital output is proposed. The design concepts and constraints, functionality, characterization, and experimental results with chemical solvents are also demonstrated in this chapter. With this novel topology, a significant increase in the IDR has been achieved which is discussed in the same chapter. Furthermore, in this chapter, we have proposed a novel calibration-free capacitive sensing technique. The proposed technique allows for uncovering the sudden changes due to the remnants as well as gradual changes due to target molecules and cells. The input dynamic range of the system is 400fF based on the post-layout simulation results. the measured resolution of the sensor is equal to 416 aF with up to 1.27 pF input offset adjustment range using the programmable bank of capacitors with a resolution of 10 fF.

In the third chapter, we present a fully integrated capacitive sensor array for life science applications. This sensing device consists of an array of 16 × 16 interdigitated electrodes (IDEs) integrated with a charge-based readout and multiplexing circuitries on the same chip.

This sensing device has a wide IDR of about 100 fF and a resolution of 150 aF, and the capability of temporal, spatial, and dielectric sensing. It makes it possible to develop a low-cost, calibration-free sensing platform for life science applications. In this chapter, the functionality and applicability of the proposed sensing device have been demonstrated and discussed by introducing various chemical solvents including ethanol, methanol, and pure water. The simulation and experimental results achieved in this work have taken us one step closer to a fully automated calibration-free capacitive sensing platform for high-throughput monitoring in life science applications.

In the fourth chapter, the applicability of the proposed CMOS capacitive sensor for monitoring dried DNA mass has been demonstrated with experimental results. These experiments enabled us to measure the linear effect of five different concentrations with a resolution of 45 ng/µl DNA mass in ultra-pure water. With this novel application of the CMOS capacitive sensor, we can monitor the dried DNA for DNA storage monitoring purposes. Based on the results, the detection range of sub-pico mol has been achieved which is compatible with the concentrations of DNA used in DNA memory technologies.

In the fifth chapter, a rapid and accurate assessment of oral cells using our CMOS capacitive sensor chips has been demonstrated. This kind of diagnostics allows for the early detection and control of periodontal and gum diseases. the experimental and simulation results demonstrate the functionality and applicability of the proposed sensor for monitoring oral cells in a small volume of 1 µl saliva samples. These results reveal that the hydrophilic adhesion of oral cells on the chip alters the capacitance of IDEs. The presented results in this chapter set a new stage for the emergence of sensing platforms for testing oral samples.

Dedication

To my wife

for her unconditional love and patience

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C	capacitance
CCC	capacitance-to-current converter
CCO	current controlled oscillator
CFC	capacitance-to-frequency converter
CMOS	complementary metal-oxide-semiconductor
C_{OFFSET}	offset capacitance
C_{SOL}	the capacitance of the sample solution
C_{PL}	capacitance of the passivation layer
C_{DL}	double-layer capacitance
CVC	capacitance-to-voltage converter
ECBCM	enhanced charge-based capacitance measurement
ECR	electrode capacitive ratio
GUI	graphical user interface
IDE	interdigitated electrode
IDR	input dynamic range
L	length
MCU	microcontroller
MOSFET	metal oxide semiconductor field effect transistor
NMOS	n-type metal oxide semiconductor
PMOS	p-type metal oxide semiconductor
POC	point-of-care
R_{SOL}	resistance of sample solution
SPI	serial peripheral interface
V_{DD}	source voltage positive polarity
V_{SS}	source voltage negative polarity
V_{TH}	MOSFET threshold voltage
V_B	bias voltage
W	width
Δ	the conductivity of sample solution
ΔC **OR** DC	the change in the target sensing capacitance due to the solution or target molecules
ΔC	the time-varying capacitance due to remnants
E_R	relative permittivity
K	dielectric constant
Λ	channel length modulation parameter

Chapter 1. Introduction

This thesis focuses on the design and implementation of complementary metal-oxide-semiconductor (CMOS) based capacitive sensors for life science applications. These sensors have attracted the attention of researchers for a variety of applications, including chemical solvent monitoring [1], [2], cellular monitoring [3]–[5], and DNA analysis [6]–[10]. This chapter presents the motivation, objective, and challenges associated with CMOS capacitive sensors and briefly discusses our proposed solutions to these challenges.

1.1 Motivation and the Main Objective

CMOS process has convincingly demonstrated competitive advantages for developing low-cost, high-precision, high-throughput biosensing platforms, with the possibility of rapid launching into the market for cellular and molecular applications [3], [5], [11]–[17], [18]. For instance, a landmark DNA sequencing platform featuring millions of Ion-Selective Field Effect Transistors (ISFETs) has recently been commercialized for genetic analysis [19]. Similarly, CMOS-based biosensors consisting of an array of interdigitated electrodes (IDEs) have attracted the attention of researchers for other life science applications such as in-vitro drug tests [3], [4], [17], DNA storage [20], [21], and point-of-care (PoC) diagnostics [22], [23]. In this thesis, our main objective is to tackle some of the existing CMOS capacitive sensors' drawbacks and develop a high-throughput platform.

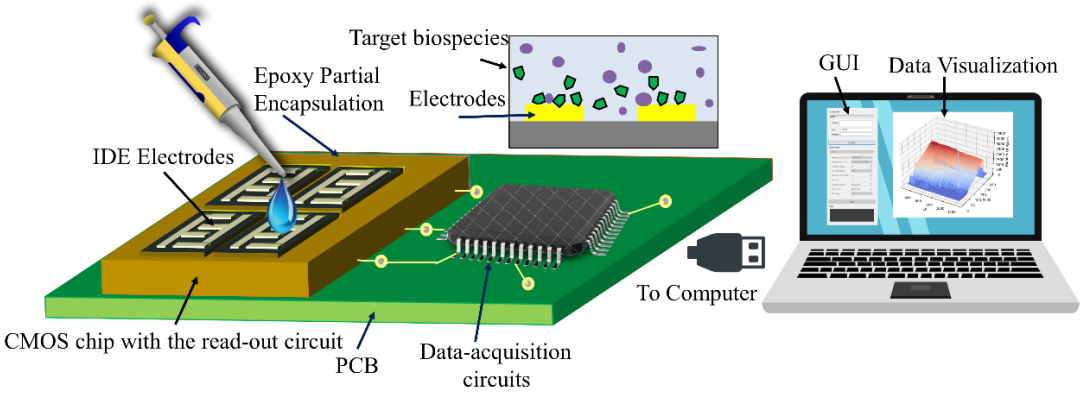


Figure 1.1: The schematic of a capacitive sensing system composed of the CMOS chip with the IDEs on the topmost metal layer, which is partially encapsulated with epoxy for the protection of pads from liquid samples on a PCB with a microcontroller for control signals and data acquisition. The captured data is sent to a custom-made GUI via USB and visualized in the GUI.

As shown in Figure 1.1, such a sensing platform consists of an array of IDEs connected to a capacitive interface circuit on the same chip, a microfluidic encapsulation, a data acquisition system, and a graphical user interface (GUI). Despite significant advances, major challenges still exist with the current MOS capacitive biosensing technologies. These challenges include but are not limited to extending the detection dynamic range, decreasing the sensitivity to remnants, and rapid high-throughput monitoring. Tackling these problems has been the main motivation for this work. Other challenges include lowering the power consumption as well as reducing the noise for higher resolution. Although decrease in power consumption is desirable, it has not been considered among main challenges in this thesis due to not being limited to battery power in this application and rather having a source of power through connections to the PC.

1.2 State-of-the-art CMOS Biosensors

CMOS biosensors have successfully been used for biosensing purposes using different measurement techniques including optical [24]–[27], magnetic [16], [28], electrochemical

[14], [29]–[34], ion-selective field effect transistors (ISFET)-based [35] and capacitive [4], [3], [36] as seen in Table 1.1.

Optical microscopy is considered a gold standard technique for clinical and research purposes. As reported in [24], CMOS-based optical biosensors consist of a single [26] or an array of photodiodes [24], [27], obviating the need for bulky microscopes. Despite significant size reduction and increase in throughput (e.g. 16 by 16 pixels/2.56 mm2 in [26]), a critical structural problem of on-chip light source for excitation of labels (e.g. fluorescent labels [37]) remains unmet in CMOS-based optical biosensors. Furthermore, these CMOS optical biosensors require specific light bandwidth that can be achieved by developing optical filters on the top of the CMOS chip, as reported in [26], [27]. To date, CMOS optical sensors (Table 1.1) have been used for many applications, including breast and prostate cancer cell detection [24], [25] as well as the detection of cholesterol levels in serum [26].

In addition to optical sensors, magnetic sensors can detect magnetically labeled target molecules or cells and thus can be used as a detection tool in cellular and molecular analysis. For instance, a CMOS hall magnetic sensor can be effectively used to detect functionalized beads with antibodies. The magnetic beads are surrounded by antibodies. These beads are used as a label to amplify the magnetic signal. For instance, in [28], a CMOS magnetic sensor is used to detect breast cancer cells. In another effort [16], antibodies, labeled with magnetic beads have been employed for the selective detection of antigens, in this case, food pathogens. Labeling used in optical and magnetic sensors is a costly and time-consuming process. It can also affect the natural living environment of bio-particles [3].

On the other hand, the electrochemical sensing techniques are considered as real-time and label-free approaches that can reveal the biochemical changes at the electrode-solution interface [5], [38]–[40]. Electrochemical techniques are highly compatible with standard CMOS technology, wherein the topmost metal layer of CMOS can be used to host electrodes

without the need for further post-processing or external components. Electrochemical measurement technique is an umbrella term for potentiometry [33], [41], impedimetric [2], [5], [38], [40], [42], [43], amperometry [14], [31], [33], conductometry [44], [45], and capacitance measurement [3], [8], [10], [13], [15], [17], [46]–[52] sensing. In the electrochemical techniques, voltammetry [53], [54] is based on measuring ohmic changes in the biosensor due to the presence of analytes with a sweep of voltage as an excitation signal. The induced current is measured, and an IV plot is generated. This technique has been used in [29] for neurotransmitter detection, as shown in Table 1.1. Similarly, amperometry measures the output current for a DC voltage excitation. These techniques have been used in [31], [33], [14], and [55] for glucose detection, analysis of chemical solutions, detection of neurochemicals, and bacterial counting, respectively, as shown in Table 1.1. In another type of electrochemical technique, the so-called potentiometric technique, the presence of ions in the proximity of the sensing electrodes creates a voltage that can be measured over time. In [41], this technique has been used to screen foodborne bacteria rapidly. Successful applications for these techniques typically include reactions during which the concentration of ions changes. Additionally, impedimetric, conductometric, and capacitive measurements that involve the measurement of resistive and capacitive changes during the experiment are other types of electrochemical sensing techniques. They become specifically more important when there is no significant ion exchange due to the nature of reactions such as cell attachment or antigen-antibody binding. [2], [5], [40], [56]. [4], [36], [57], and [43] are some examples of capacitive sensors used for real-time measurement of cell proliferation, detection of single bacterial cells, cancer, and stem cell monitoring.

Among the electrochemical sensing techniques, capacitive sensors implement direct measurement of the capacitance without the need for indirectly extracting the capacitance

from the measured impedance. This, in turn, can bring simplicity to the read-out circuitry compared to impedance measurement techniques. Table 1.1 lists some proposed CMOS biosensors in the literature based on the type, application, electrode array size, type of electrodes, and the implemented CMOS technology. Among various CMOS biosensing techniques, this thesis focuses on CMOS Capacitive sensors.

Table 1.1: Various CMOS biosensors

Sensing Principle	Detecting Target	Array #	CMOS Process	Sensing Pixel	Detection Concentration	Ref
OP[1]	Breast and prostate cancer cells	32×32	0.18 µm	pD[15]	Normal– 300 times diluted blood samples	[24], [25]
OP	Test reports with Qdot8 only	-	65 nm	PD	10 fM -48 zM of quantum dots	[27]
OP	Cholesterol	16×16	0.35 µm	PD	1.2 mM- 29µM	[26]
MG[2]	Breast cancer cells	2	0.18 µm	MC[16]	3ng/mL – 100 pg/mL	[28]
MG	Mouse IgG	21	65 nm	Mc	200 cells/ µL	[16]
ISFET	DNA strands	1.2 million	0.35 µm	ISFET[9]	N/A	[35]
IM[3] and CV[4]	Dopamine	32 and 28	0.18 µm	Pt[10]-MEA[17]	200 – 500 µM	[29]
IM	Zika virus oligonucleotides	16×20	0.18 µm	Au[11]-MEA	1 µL - 1mM	[58]
AM[5]	H2O2	1	0.35 µm	Pt-MEA	100 µL – 1mM	[31]
AM	Dopamine and glutamate	2	0.13 µm	C–nT[12]	N/A	[14]
AM	Microbeads with the same size as bacteria	1024×1024	0.6 µm	Au[13]-MEA	N/A	[55]
AM/PO[6]	Acetonitrile solvent, TBAPF6 and ferrocene	2	0.35 µm	Ti-Au	All pH range	[33]
PO	Escherichia coli	512×128	65 nm	ISFET	100 cfu/mL[18]	[41]
CA[7]	Human ovarian cancer cells	4×4	0.35 µm	IDE[14]	100 – 1000 cells/µL	[4]
CA	Staphylococcus epidermidis	16×16	0.25 µm	IDE	7 – 100 cells/µL	[36]
CA	Human lung carcinoma cell	8×8	0.35 µm	IDE	100 -200 kcells/mL	[57]

1 Optical, 2 Magnetic, 3 Impedimetric, 4 cyclic voltammetry, 5 Amperometry, 6 Potentiometric, 7 Capacitive, 8 Quantum dots (QDs) are tiny semiconductor particles nanometers in size, having unique optical and electronic properties. They are a central topic in nanotechnology. When the semiconducting quantum dots are illuminated by UV light, the transition of an electron from the valence band to the conductance band accrues. The excited electron can drop back into the valence band, releasing its energy by the emission of light, 9 Ion sensitive field-effect transistor, 10 The current sensing electrodes have been post-processed by Platinum, 11 The current sensing electrodes have been post-processed by Gold, 12 The current sensing electrodes has been post-processed by Carbon Nanotube, 13 The current sensing electrodes has been post-processed by titanium – Gold Alloy, 14 IDEs passivated with silicon oxide,15 Photodiode, 16 Micro Coil, 17 Microelectrode Array, 18 colony-forming unit per milliliter.

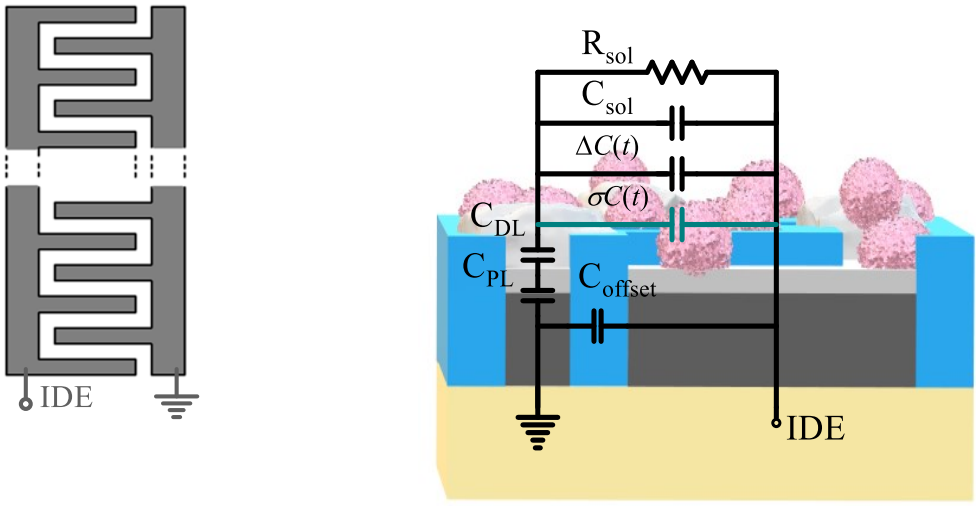
1.3 CMOS Capacitive Sensors

Capacitive sensors have widely been used for cell or DNA detection applications, via recording capacitance change on an interdigitated electrode (IDE), as reported in the literature [4], [10], [17], [51], [59]–[62]. An IDE is shown in Figure 1.2 (a). In the IDEs, the attachment of biological or chemical materials to the surface of electrodes typically changes the capacitance value in the equivalent circuit model of the electrode-electrolyte interface. The electrode-electrolyte interface hosts double-layer capacitance [63], [64] that can change because of molecular adsorption onto the electrode interface [3], [4], [15], [62], [65].

1.3.1 Capacitance Sensing Electrodes

The use of IDE (Figure 1.2) for capacitive sensing purposes has widely been reported in the literature [4], [7], [9], [17], [47], [49], [59]–[61], [66], [67]. Figure 1.2 (b) shows a cross-section of an IDE in the presence of a sample and the equivalent circuit model of this interface. $\sigma C(t)$ represents the change in the target sensing capacitance for the measurement due to the solution or target molecules. Rsol represents the sample solution's resistivity. Similar equivalent electric models are given in [17], [62], [65], [68], [69]; however, $\Delta C(t)$ which is the time-varying capacitance due to remnants has been considered in our work for the first time. The equivalent capacitance of the passivation layer and the double layer capacitance are represented by CPL. In the case of a low-conductive analyte, Rsol can be neglected; thus, the equivalent capacitance of the IDE, CIDE, will be equal to Coffset || 2CPL+Cs(t) where Coffset is the total parasitic capacitance of the IDE with the underlying CMOS layers and $Cs(t)= \sigma C(t) + Csol + \Delta C(t)$. If CPL >> Cs(t), on the right-hand side, Cp+Cs(t)+Cp will be equal to Cs(t) which can result in the highest possible sensitivity. Etching the native insulating layers that cover the electrodes in the standard CMOS process

has been considered in some papers as a way to increase CPL and thus boost the sensitivity [3], [4], [70]. On the other hand, the reason to keep this layer is to protect the sample from direct contact with the metal surface of the electrode that might be toxic to bioparticles [13], [68]. In this thesis, both types of electrodes have been implemented to benefit from the high sensitivity of the non-passivated IDEs and the stability of results in the non-passivated electrodes.



(A) (B)

Figure 1.2: (a) IDE, top view, (b) Cross section of the IDE with the sample and the equivalent electric model.

1.3.2 Challenges and the state-of-the-art

IDEs implemented on a CMOS chip come with an offset capacitance. The offset capacitance is the addition of Cstanding and Cstray, shown in Figure 1.3 [15], [46], [52], [62]. This is a static offset that exists due to the topology of the electrodes and is sometimes called the static offset.

Another type of offset is due to the accumulation of the remnants on the electrodes at the time of the experiment. This type of offset is shown with ΔC(t) in Figure 1.3 (b) and is a result of sedimentation and accumulation of non-target molecules called “remnants”.

Despite exclusive benefits of CMOS capacitive sensors proposed for life science applications, including high precision, low cost, and size, these sensors suffer from multiple drawbacks [67] due to these offset capacitances. One major drawback is the low IDR which stems from output saturation when the value of offset is much higher compared to the sensing capacitance. To simply quantify this, we define electrode capacitive ratio (ECR) as $\alpha c = 100 \times dC/C0$, where dC is the sensing capacitance, and C0 stands for the offset shares of the electrode-analyte interface. Canceling the effect of C0 can significantly help increase ECR. For instance, in [17] a capacitive bacteria detection sensor is reported with a 61 aF/bacteria sensing and 2 fF offset capacitance (αc=3.05%). The authors proposed using the differential output to cancel the effect of C0 by differentiating two sensor readings, in the presence and absence of the sample. They reported a 55 fF dynamic range for their topology. In [4], the authors reported the use of several reference electrodes, implemented outside of the active sensing area to prevent electrodes' contact with the solution. To increase ECR, they implemented differential output values by subtracting the output recorded from the sensing electrodes with and without contacting the sample solution at the software level within a 1 fF IDR.

Accumulation of chemical/biological remnants on the electrodes can significantly increase C0 in real-time resulting in a further drop in ECR during the experiment [3], [4], [70], [71]. For instance, the presence of unwanted remnants was reported in [70] which was mostly composed of cells that had undergone apoptosis (cell death). The authors report that their bacteria growth monitoring sensor was saturated because of these remnants resulting in a drop in the maximum detectable bacteria concentration. In [71], it is pointed out to the presence of protein residuals on the electrodes after cells are detached. This was found to play the role of an unwanted insulating layer that lowered the sensitivity during cell growth. Furthermore, these remnants are hardly removable without damaging the tiny electrodes and

are currently the main obstacle preventing the CMOS sensors from being reused for multiple tests. For instance, Figure 1.3 (a) shows a 3D microscope image of our chip after being washed multiple times following the water droplet test. The image demonstrates the solidified remnants after evaporation of the sample (see section 2.5.4) for more details.

In the presence of a reference capacitance to take the benefit of higher resolution, another major drawback is the effect of mismatches in the IDEs as well as in the pixel read-out circuitry [3], [4], [17], [24], [72], [73]. The mismatch can impose an offset on the output that can lead to diminished IDR. In [74], [75], current mirrors with digitally programmable gain are used as a calibration tool for mismatch compensation. In [50], [76], the use of floating-gate transistors with a combination of impact-ionized channel hot electron injection and Fowler–Nordheim tunneling mechanisms is suggested for mismatch compensation and output offset cancelation.

In another effort, in [4], it is shown that a capacitance-to-frequency (CFC) conversion scheme can provide a higher dynamic range than a capacitance-to-voltage (CVC). This is because the change of frequency can reach multiple times of magnitude higher compared to the change in voltage which is limited by the rail-to-rail swing room. Based on this principle, a capacitance-to-frequency interface circuit using a five-stage ring oscillator loaded with five IDEs for bacteria detection is proposed in [68] to reach a higher IDR.

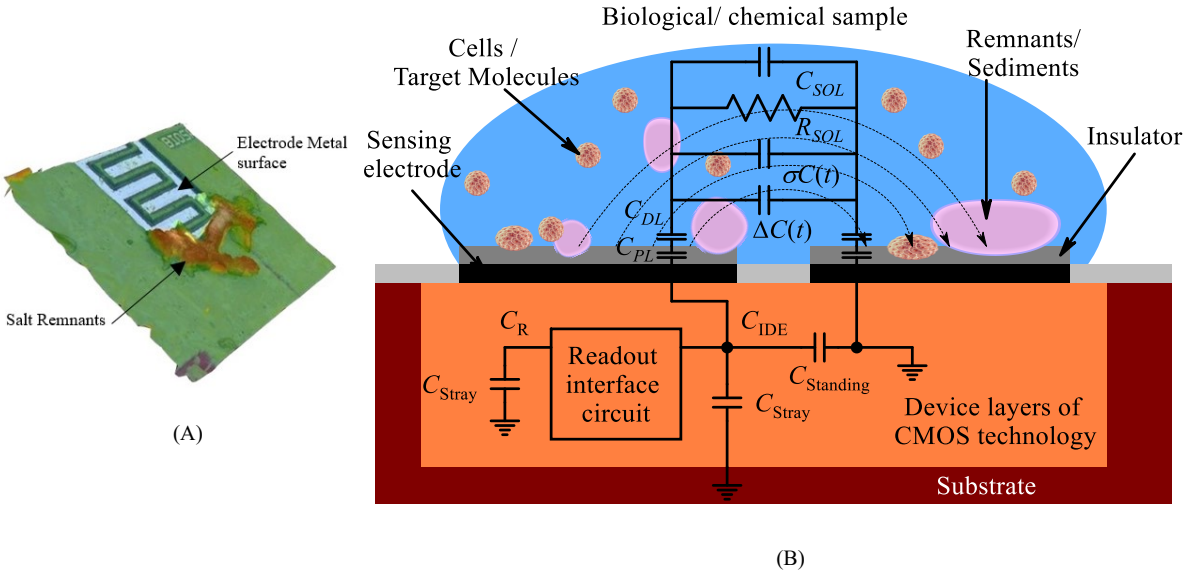


Figure 1.3: IDEs: (a) 3D microscope image of the IDE in the proposed capacitive sensor in this chapter (using VHX – 5000 - Keyence microscope) (b) Cross-section accompanied by the electric equivalent circuit model of the IDE electrodes and the analyte.

In a nutshell, while differential methods can provide higher ECR, calibration schemes are necessary for mismatch compensation and input offset cancelation. It is also important to have a mechanism to cancel the extra offset capacitance due to sedimentation. On one side, differential capacitance circuit topologies present themselves as necessary components of high-IDR CMOS capacitive chemical and biological sensors. On another side, capacitance-to-frequency has become a more popular conversion scheme for higher dynamic range benefits.

1.3.3 Proposed Solutions in this Thesis

1.3.3.1 Linearity of the Capacitive Sensor

We have shown that using an integrating capacitor to integrate the current, which has been shown in the three generations discussed in Section 2.2.2 is the main factor in introducing saturation and decreasing the nonlinearity of the CBCM circuit. We have

proposed a novel enhanced CBCM (ECBCM) circuitry that provides a significant linearity increase, as discussed in detail in Chapter 2.

1.3.3.2 Input Dynamic Range (IDR)

In this thesis, in addition to an increase in the linearity through proposing the ECBCM block in a wider range of input, we have proposed a new topology to integrate a current-controlled oscillator (CCO) into the ECBCM block. This way, the conversion of capacitance to voltage has been avoided. Instead, the differential current from the ECBCM block has been directly converted to frequency. This topology has been explained in detail in Chapter 2, together with the chip fabrication and measurement results based on this topology.

1.3.3.3 An array of Capacitive Sensing Electrodes

In this thesis, we have proposed and demonstrated an array topology without adding any switching element on the measurement nodes. We have shown the functionality of this topology where multiplexing takes place on the CBCM clock signals. In Chapter 3, the details about this topology, fabricated chip and the experimental results have been demonstrated.

1.3.3.4 Variation of Offset Capacitance

CMOS capacitive sensors that are used in life science applications are exposed to aqueous samples in the presence of bioparticles or other non-target remnants [67], [70]. The presence of remnants can change the sensor reading and can easily saturate the sensor depending on their size. Different calibration techniques discussed in Section 2.2.2.2, are only effective for pre-experiment calibration. In this thesis, a calibration-free sensing

paradigm has been proposed that uses a digitally programmable bank of capacitors on the reference side of the ECBCM circuit, that can reveal the operating point changes during the experiment because of the deposition of non-target molecules. The detail of this technique is highlighted in Chapter 2.

1.3.3.5 New Cellular and Molecular Applications

The quantification of DNA in the dry phase and the detection of oral cells are introduced in this thesis as two new applications for CMOS capacitive sensors.

1.3.3.5.1 DNA Quantification in the Dry Mode for DNA Storage Monitoring

The reported applications of DNA detection using CMOS capacitive sensors, such as the ones in Table 2.1, are limited to the detection of DNA hybridization in an aqueous solution. In the reported works, the hybridization of a specific strand of DNA molecule that covers the area of the electrode, with a target molecule results in a change in capacitance.

In data storage devices, where DNA molecules are used as the medium of storage, using the hybridization technique for quantifying the amount of DNA is less feasible since the DNA is stored in a dry phase. To that end, quantification of DNA in the range of nanograms in the dry mode is crucial to evaluate the data storage accuracy. For the first time, we have shown the applicability of our device for the quantification of DNA in dry mode. Chapter 4 discusses the details of the DNA detection that can pave the way toward future data storage devices using DNA, offering multiple times higher storage capacity per same mass compared to the semiconductor-based storage devices.

1.3.3.5.2 Screening Oral Cells for Periodontal Point-of-care (PoC) Purposes

Many research papers have addressed using CMOS capacitive sensors for cell monitoring, as shown in Table 2.1. In these works, cells have been cultured on the CMOS sensor and the live cells that proliferated and attached to the surface of the electrodes have been detected. However, for oral cells screening in the saliva sample, culturing is impractical since oral cells have been inactivated after entering the mouth cavity. In Chapter 5, we have shown the applicability of the proposed CMOS capacitive sensor for the screening of oral cells in saliva samples without culturing them which can set a new stage for developing PoC diagnostics tools for periodontal diseases.

1.3.3.6 Design Metrics

The capacitive sensor in this thesis is intended to be a general-purpose device without being limited to a specific application. For cell monitoring and DNA detection applications a resolution in the range of sub-femto farad is necessary from the literature. In addition, the presence of remnants has shown to increase the capacitance of the IDE to the level of tens of femtofarads. Measurement speed and power consumption are not major limiting factors in the design mainly due to slow dynamic of the biological reactions and non-stringent power budget due to continuous connectivity to power sources such as USB ports.

1.3.4 Organization of the Thesis

In Chapter 1, the main objective of this research, the state-of-art capacitive interface circuits, and the challenges were covered. In Chapter 2, we address the challenge of developing a high IDR and resolution interface circuit and demonstrate its advantages for chemical solvent monitoring. The proposed circuitries, simulation, and experimental results

of this chapter have been published in IEEE Transactions on Biomedical Circuits and Systems (TBioCAS) journal in a paper titled “Wide IDR fully integrated capacitive sensor for life science applications” [77] and in IEEE Transactions on Instrument and Measurement (TIM) journal entitled “Calibration-free CMOS capacitive sensor for life science applications” [78]. Chapter 3 addresses the challenges of developing high throughput capacitive sensor arrays for life science applications. This chapter has been submitted as a paper titled “A high dynamic range 16×16 capacitive sensor array for life science applications” to IEEE Transactions on Biomedical Circuits and Systems (TBioCAS) journal [77]. In Chapter 4, we demonstrate and discuss the applicability of the proposed circuitries for DNA storage purposes. The focus of this chapter is on DNA quantification in dry mode using the proposed CMOS capacitive sensor. The details of this chapter were published as a paper titled “CMOS capacitive dry DNA storage monitoring: design, implementation and experimental results” in IEEE Sensors Journal [79]. Chapter 5 puts forward the advantages of the proposed circuitries for cellular monitoring. This chapter is published in Bioengineering journal in the form of a paper entitled “Oral cells-on-chip: design, modeling and experimental results” [80] and for the first time addresses the challenge of monitoring oral cells on a CMOS chip. Chapter 6 is dedicated to concluding remarks and future work.

Chapter 2: Wide-Input Dynamic Range and Calibration-free CMOS Capacitive Sensor

This chapter demonstrates a new circuit and system with a high IDR targeting multipurpose detection in life science applications. In addition, thanks to the proposed circuit topology, a new measurement technique is proposed that can be used for the detection of large capacitance changes due to remnants as well as small capacitance changes due to target molecules without the need for calibrating the sensor. The proposed circuitries and the achieved simulation and experimental results of this chapter have been published in IEEE Transactions on Biomedical Circuits and Systems (TBioCAS) journal in a paper titled "Wide IDR fully integrated capacitive sensor for life science applications" [77] and in IEEE Transactions on Instrument and Measurement (TIM) journal entitled "Calibration-free CMOS capacitive sensor for life science applications" [78].

2.1 Abstract

In this chapter, a wide-IDR fully integrated capacitive sensor is proposed. The design concepts and constraints, functionality, characterization, and experimental results with chemical solvents are demonstrated. This circuit is composed of a new CBCM block which has a feedback circuit at its output that extends the linearity of the CBCM block, here

designated as ECBCM. Furthermore, a topology is proposed in which the output current of the ECBCM is directly converted to a frequency in a CCO, with a maximum frequency of 300 MHz without converting it to voltage. In this topology, the integrating capacitor has been eliminated and the integration of ECBCM output current takes place in the digital domain using the CCO and a counter. With this novel topology, an IDR of about seven times higher compared to the previous second-generation CBCM circuits and about three times higher compared to the CBCM with cascode current mirrors has been achieved. A counter-serializer generates the digital output of the sensor. In addition to the ECBCM block and the capacitance-to-digital conversion, in this chapter, we have proposed a novel calibration-free capacitive sensing technique. This technique relies on the implementation of a programmable bank of capacitors on the reference side of the ECBCM block for the first time. This programable bank of capacitors is crucial for sweeping the value of the reference capacitance which allows for the creation of time-resolved three-dimensional (3D) specific patterns for the measurement of capacitance variations of the sample-electrode interface. The main advantage of this technique is the revelation of huge capacitance change due to remnants in the sample. CMOS capacitive sensors in life science applications are typically reported to suffer from significant capacitance changes caused by remnants and sediments during the experiment within several biological and chemical reactions. The proposed technique allows for uncovering the sudden changes due to the remnants as well as gradual changes due to target molecules and cells.

The circuit has been implemented and fabricated under AMS 0.35 µm technology and has two independent circuits with one IDE connected to each. The input dynamic rage of the system is at least 400fF based on the post layout simulation results. The measured resolution of the sensor is equal to 416 aF with up to 1.27 pF input offset adjustment range (IOAR) using the programmable bank of capacitors with a resolution of 10 fF. Having a

measurement speed of 15 µs, this sensor is among the fast CMOS capacitive sensors in the literature. In this chapter, the sensors' functionality and applicability to life science applications have been demonstrated through the experimental results µL for monitoring 2 evaporating droplets of chemical solvents. By using samples of solvents with different conductivity and relative permittivity, a wide range of capacitance and resistance variations in the sample-IDE interface electric equivalent model has been created. We tested the sensor using three different chemical solvents. The four different categories of curves that constitute the specific patterns of the chemicals showed a match with the post-layout simulation results. The generated specific pattern is valid for the chemicals with a conductivity of up to 5 mS/cm.

Based on the results, our proposed device addresses the challenge of detecting small capacitance changes despite large parasitic elements caused by the ions in the solution or by remnants deposited on the electrode. This chapter has been prepared regarding two of our published papers in IEEE Transactions on Biomedical Circuits and Systems (TBioCAS) [77] and IEEE Transactions on Instrumentation and Measurement (TIM) [78] journals.

2.2 Introduction

2.2.1 Capacitive Circuit Topologies for Life Science Applications

This section puts forward the recent advances of CMOS capacitive interface circuits in three categories, capacitance-to-voltage converters (CVC), capacitance-to-frequency converters (CFC), and capacitance-to-current converters (CCC).

2.2.1.1 Capacitance-to-Voltage Converters (CVC)

Charge-sharing circuits and charge-sensitive amplifiers are the two main circuit topologies that convert capacitance to voltage. In [81] and [82], a circuit based on a charge-sharing technique is shown for tracking breast cancer cell proliferation. Figure 2.1 (a) illustrates the circuit topology. In the reset phase, the capacitances of nodes N1 and N2, CN1 and CN1, are charged to the supply voltages, Vdd and Vss, respectively. In the evaluation phase, the charge is redistributed between the capacitances of the nodes N1 and N2. The output voltage is a function of the capacitance of the sensing electrode, CS, as well as other parasitic capacitances, as shown in 2-1.

$$V_{Out} = \frac{(\mathrm{C_{N1}} + C_S).V_{dd} + \mathrm{C_{N2}}.V_{ss}}{\mathrm{C_{N1}} + \mathrm{C_{N2}} + C_S} \quad 2\text{-}1$$

Some practical considerations for the implementation of this circuit are to minimize the parasitic capacitances at N1 and N2 nodes such as the capacitance between the electrode and the substrate.

Figure 2.1 (b) illustrates a typical charge-sensitive amplifier (CSA) circuit used in [83]. When Φ transitions to the high state, the reset switch on the integrator is closed, and the Op-Amp charges the sensing capacitor, CS. When Φ falls, the feedback capacitor, Cfb, integrates a charge proportional to the difference between the sensing and reference capacitors. The output of this charge-sensitive circuit is given in 2-2. An analog-to-digital converter (ADC) with appropriate resolution converts this voltage to a digital output.

$$V_{out} = \left(\frac{C_S - C_R}{C_{fb}}\right) V_A \quad 2\text{-}2$$

where VA denotes the amplitude of Φ and CR is the reference capacitor. Charge-sensitive amplifier circuits are sensitive to parasitic capacitances unless used in a differential topology to measure the differential capacitance [84]. In [85], a differential topology has been implemented which uses a combination of three capacitors as a reference. A

configurable on-chip reference capacitor has also been used in [86] where the reference capacitance can be configured in the range of 250 fF to 15 pF in steps of 250 fF. These circuits have typically small footprints but require precise timing signals. One drawback of this category is the limitation of the output to a fraction of Vdd, which limits the dynamic range. Another issue is that the parasitic capacitances at the measurement nodes can decrease the sensitivity.

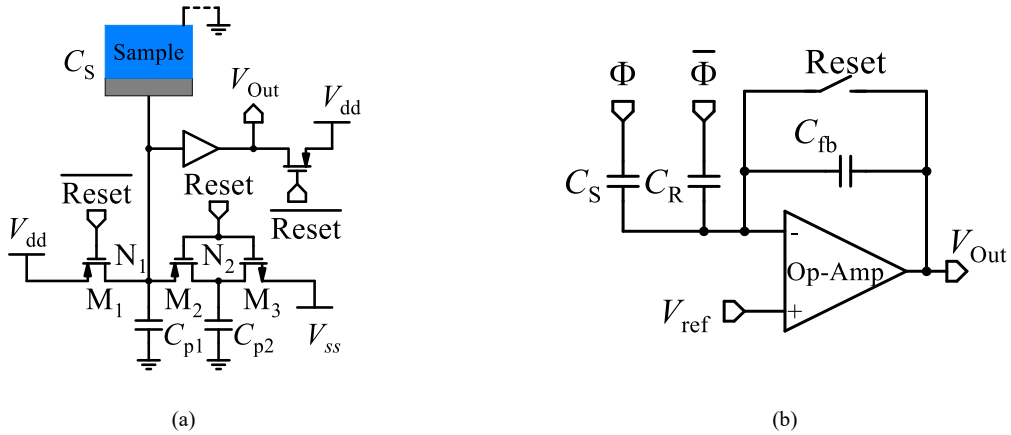


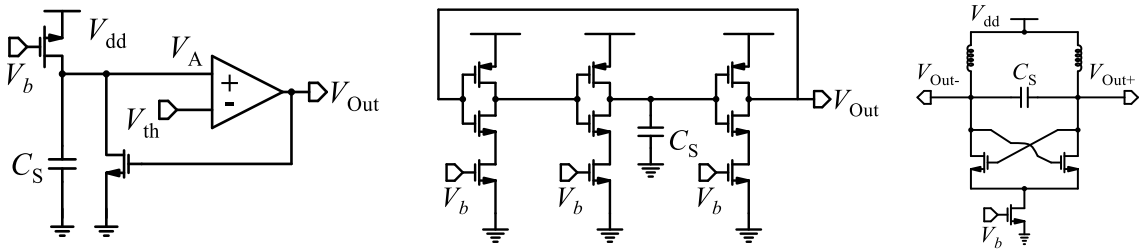
Figure 2.1: (a) Charge sharing circuit used in [81], (b) Charge sensitive amplifier circuit [83].

2.2.1.2 Capacitance-to-Frequency Converters (CFC)

Figure 2.2 (a) demonstrates a circuit in which a P-type device connected to a bias voltage, Vb, creates a constant current to charge the sensing capacitor, CS. A comparator compares the voltage of CS with a threshold voltage, Vth. The output voltage of the comparator is initially zero. When VA reaches the threshold voltage, the output of the comparator flips to high, resulting in CS being discharged by the switch controlled by the output signal of the comparator. This topology, the so-called relaxation oscillator, is utilized in [87], [88] for label-free sensing of neurotransmitter dopamine as well as labeled magnetic-based detection of microbeads. It is shown that the output frequency is a function of the sensing capacitor value in 2-3.

$$f = \left(\frac{C_S . V_{th}}{I_B} + \tau_d\right)^{-1} \quad 2\text{-}3$$

where τ_d is the delay caused by the comparator. A similar circuit has been implemented in [8] using switches for reversing the direction of a single reference current and the creation of two symmetric threshold voltages for a comparator working with a single threshold voltage. As a result, a squared waveform is generated with a frequency inversely proportional to the sensing capacitance.



(a) (b) (c)

Figure 2.2: Schematic of (a) comparator-based relaxation oscillator used in [88], (b) Ring oscillator-based CFC [4] (c) LC-tank oscillator-based CFC [89].

As seen in equation 2-3, the delay term can cause nonlinearity if the period of the output signal is in the same range of τ_d. Besides, comparator-based relaxation oscillators need accurate current references and comparators.

In [4], [59], [68], [90]–[92], a ring oscillator-based capacitance measurement circuit has been utilized for the measurement of the sensing capacitors as a varying load, Figure 2.2 (b). The effect of change in the value of sensing capacitance is the change in the frequency of the oscillator. The bottleneck of the ring oscillators is the high sensitivity of the output frequency to temperature, process variations, supply voltage, and a nonlinear relation of the output frequency with the load capacitance [90].

In [89], [93], the sensing capacitors are inserted in an LC tank of an oscillator. The change in the value of the sensing capacitance leads to a frequency shift in the output of the oscillator. A typical implementation is illustrated in Figure 2.2 (c). LC oscillator's frequency before exposure, f_0 , alters by Δf after the change in sensing capacitance due to the presence

of samples. The relative frequency shift ($\frac{\Delta f}{f_0}$) of the LC tank is proportional to the capacitance change over the initial capacitance ($\frac{\Delta C}{C_0}$), 2-4, as shown in [94].

$$1+\frac{\Delta f}{f_0}=\frac{1}{\sqrt{1+\frac{\Delta C_S}{C_0}}} \qquad 2\text{-}4$$

where C0 is the equivalent capacitance consisting of the sensing capacitor, CS, and parasitic capacitances. Another approach is given in [89] where a phase-locked loop (PLL) circuit is used to fix the frequency shift to a nominal operating frequency. The DC tuning voltage of the PLL loop is shown to be proportional to the change in capacitance value. The required inductors are in the range of nH that can occupy a significantly large area on the die.

2.2.1.3 Capacitance-to-Current Converters (CCC)

The circuit proposed for this conversion is charge-based capacitance measurement (CBCM). The technique inherently measures the differential capacitance and thus can reach high accuracy by canceling the parasitic capacitances [95]. The core of this circuit topology is depicted in the dotted-line block in Figure 2.3.

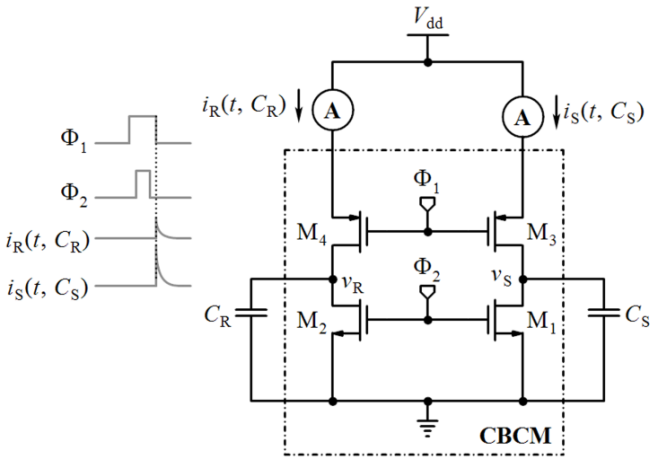


Figure 2.3: CBCM circuit

Two identical branches, composed of NMOS (M1 and M2) and PMOS devices (M3 and M4) provide the charge and discharge paths for the sensing, CS, and the reference capacitor CR. Two non-overlapping clock pulses, Φ1 and Φ2, provide the necessary switching signals. When Φ1 and Φ2 are low, the capacitors, CS and CR, are charged via pull-up switches (M3 and M4) up to, Vdd. Whenever these clock pulses transition to high, the capacitors are discharged via pull-down switches (M1 and M2). The "average" of differential current of the two branches is(t, CS) and iR(t, CR), over one period of Φ1 and Φ2 is linearly proportional to the difference of the sensing and reference capacitances, (CS - CR) as given in 2-5.

$$average(i_S(t) - i_R(t)) = (V_{dd}).(C_S - C_R) \quad 2\text{-}5$$

To use this topology in cellular and molecular detection applications, CS node is connected to an IDE that can be exposed to samples. On the other hand, CR is designed in different versions ranging from floating nodes or a dummy IDE to internal capacitors. The common point about all the variations is that the reference side is insensitive to samples.

Averaging is essential in this technique to maintain the linear relation of differential current to differential capacitance. Therefore, the integrator is an essential building block in the CBCM. A wide range of research uses integrating capacitor for this purpose [3], [15], [38], [40], [50], [52], [60], [61], [96]–[98]. In [66], to increase the sensitivity, current amplification has been added to this circuitry. The high sensitivity of CBCM is demonstrated in [66].

Table 2.1: Summary of various circuit topology and measurement techniques discussed in this section

Ref.	Application	Tech (µm)	Method	D/ND	Output type	Array #	Resolution	Sensitivity	IDR	Area (mm^2)	V_{dd} (V)	Power
[36]	Single bacterial	0.25	CVC by ChS (ChR)	ND	A	16×16	450 aF	55 mV/fF	0.45 fF-57 fF	0.1 (DA)	2.5	29 µW
[81]	Cell proliferation	0.5	CVC by ChS (ChR)	ND	A	28	0.1 fF	-	25 fF	2.25 (DA), 0.16 (EA)	3	-
[83]	Localization	0.35	CVC by CSA	D	D	320×320	21 aF	345 mV/fF	-	-	3.3	-

Ref.	Application	Tech (μm)	Method	D/ND	Output type	Array #	Resolution	Sensitivity	IDR	Area (mm^2)	V_{dd} (V)	Power
	of bioparticles		(ChR), external ADC									
[99]	Cancer	0.18	SC+ SAR	ND	D	9	4.5 fF	-	16.137 pF	0.06 (AA), 8.76 (EA)	0.9 - 1	2.1 μW
[87]	Neurotransmitter dopamine	0.35	CFC by Rel.O	ND	D	5×5	-	21 kHz/fF @ 4.9 MHz @ 123 fF	12 fF-700 fF	-	-	-
[8]	DNA	0.5	CFC by Rel.O	D	D	8×16	-	23 Hz/pF @ 7.5 kHz @ 330 pF	330 pF- 10 nF	28.8 (DA)	5	-
[92]	Cell volume growth	0.13	CFC by RO	D	D	3×4	10 aF	235 mV/fF	+/- 100 fF	2.25 (DA), 1 (AA)	-	-
[4]	Cell proliferation	0.35	CFC by RO	ND	D	4×4	14.4 aF	590 kHz/fF	1 fF	9 (DA), 0.0144 (EA)	3.3	8 mW
[59]	Single cell	0.35	CFC by RO	D	D	1	14 aF	570 kHz/fF @ 1.37 GHz @ 500 fF	-	4 (DA)	-	-
[88]	Cells and biomolecules	0.35	CFC by RO	ND	D	8×8	2.5 fF	223 kHz/fF @ 5.2 MHz @ 23 fF	-	-	-	-
[68]	Bacteria	0.25	CFC by RO	ND	D	1	10 fF	11 kHz/fF @ 254 MHz @ 17.5 fF	-	0.05 (AA), 0.0506 (EA)	2.5	29 mW
[100]	Nano- and micro-particles	0.18	CVC by CBCM	ND	D	3×3	1 fF	10 fF/mV (or 0.1 mV/fF)	-	1.8 (DA)	1.2 to 1.3	-
[15]	Cell	0.5	CVC by CBCM	D	A	6×6	15 aF	200 mV/fF	±25 fF	3	3	165 μW
[70]	Bacteria growth	0.18	CBCM+ΣΔ ADC	ND	D	3	110 aF	250 mV/fF	7 fF	2 (DA)	1.8	-
[57]	Cell growth	0.35	CBCM, ΣΔ ADC	D	D	8×8	10 aF	350 mV/fF	10 fF	9 (DA)	-	-
[2]	-	90 nm	CBCM, ADC	ND	D	256×256	10 aF	-	1 fF	2,525,253 (DA), (Radius of NE=90 nm)	1.2	15 mW
[101]	DNA hybridization	0.35	TW, SC, ADC	ND	D	16×8	1 pF	-	10 pF-10nF	10 (DA)	-	-

CVC: Capacitance-to-voltage converter, ChS: Charge sharing, ChR: Charge redistribution method, CSA: Charge sensitive amplifier, ADC: Analog-to-digital converter, SC: Switched capacitor technique, SAR: Successive approximation register ADC, CFC: Capacitance-to-frequency converter, Rel.O: Relaxation oscillator, RO: Ring oscillator, CBCM: Charge based capacitance measurement, TW: Triangular waveforms analysis, ND: None-differential, D: Differential, DA: Die area, EA: Electrode(s) area, AA: Active area, Vdd: Supply voltage, NE: nanoelectrodes, D: Digital, A: Analog

However, the limitation of voltage swing of the amplifier from zero to Vdd restricts the sensor's output and thus input dynamic range (IDR). Section 2.2.2 thoroughly reviews CBCM-based circuit topologies.

2.2.1.4 Comparison of the Circuit Topologies

Table 2.1 compares the state-of-the-art read-out circuitry for capacitive sensors based on sensitivity, IDR, resolution, power consumption, and array size. The sensitivity of the sensors in the category of capacitance-to-voltage or -current converters reaches a maximum of 350 mv/fF for a CBCM-based technique presented in [57]. The maximum sensitivity of 590 kHz/fF has been reported for the implementation of ring oscillator-based CFC reported in [4]. In terms of IDR, the implementation proposed in [92], using a ring oscillator-based capacitance-to-frequency conversion, has reached 200 fF. The CBCM-based technique reported in [2] demonstrates a significantly high resolution of 6.7 aF. As the table shows, the power consumption varies significantly among the designs from a few μW to a few mW depending on the circuit topology. Power consumption up to a few tens of mW therefore has been considered an accepted range with no significant impact on the performance of the sensor. Besides, the largest size of array implementation has reached 320 × 320 due to the small footprint of the circuit with a differential charge-sensitive approach reported in [83].

In general, techniques based on CBCM and CFS using oscillators present high resolution in the range of some tens of aF and are among the most popular approaches used for LoC applications due to their high dynamic range, low complexity, and smaller on-chip footprint [18].

2.2.2 Core-CBCM Capacitive Circuit Topologies

An overview of capacitive interface circuits based on CBCM method is presented in this section.

2.2.2.1 First-generation core-CBCM Circuitry

In an approach reported in [66], the CBCM currents, iS and iR shown in Figure 2.4 (a), are first amplified utilizing two current mirrors with equal gains of AI as depicted in Figure 2.4 (b). When Φ1 is low and CS is charged rapidly, the amplified currents are equal to i'S = AI.iS and i'R = AI.iR. After amplification, the currents i'S and i'R are averaged using two individual integrating capacitors, Cint+ and Cint-. The voltages of the integrating capacitors, VO+ and VO- are amplified by employing a differential amplifier. In this approach, the common mode offset voltage, which might vary due to remnants in the sample, can result in the saturation of the differential amplifier. Despite the high resolution of about 10 aF, a low dynamic range of 1fF has been reported [66]. An extended version of the circuit has been used in [102] where typical current mirrors have been replaced with the current-voltage mirrors shown in Figure 2.4 (c). (M6, M7) and (M12, M13) are the typical current mirrors while the four-transistor pairs (M5, M8, M9, and M10) and (M11, M14, M15, and M16) are implemented as voltage mirrors. (M9, M10) and (M15, M16) pairs create a virtual short between the CBCM and output nodes of the current mirrors to decrease the nonlinearity due to the dependency of the output current on drain-source voltage. To understand the virtual short, we should observe that Vsg10=0 and (Vsg16=0), thus M10 and M16 are literally off. The current path for M9 and M15 is through M10 and M16, respectively. Therefore, M9 and M15 will also be turned off dictating their Vsg voltage to be zero and thus creating the virtual short. An increase in the sensitivity from 28.7 mV/fF to 47.73 mV/fF has been

reported with higher linearity achieved from voltage mirroring pairs compared to the typical current mirror circuit. However, the cost of adding these voltage mirroring pairs is diminishing dynamic range due to more limited output voltage swings [102].

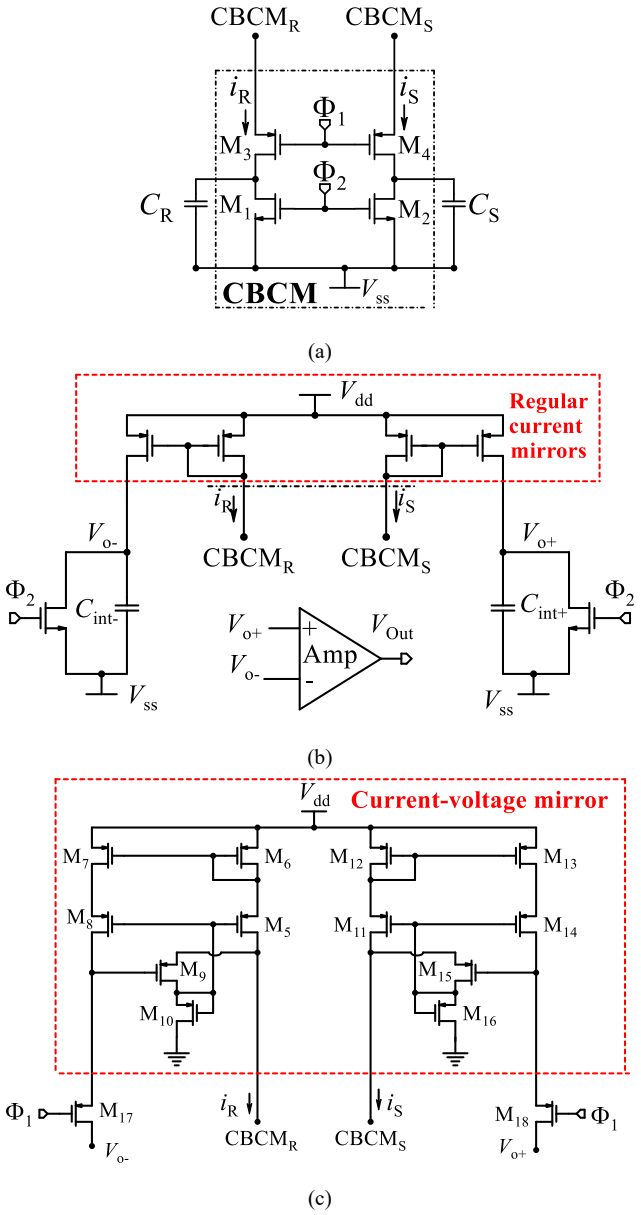


Figure 2.4: (a) Core-CBCM circuit, (b) a CVC topology where CBCM currents are amplified in regular current mirrors and integrated individually on two integrating capacitors creating VO+ and VO- voltages. The output is generated in a differential amplifier with VO+ and VO- as inputs, (c) the typical current mirrors have been replaced by current-voltage mirror topology.

Another alternative circuit has been proposed in [103] and is shown in Figure 2.5. V_{ref1} and V_{ref2} are used instead of Vdd and Vss, where $V_{\mathrm{ref1}} > V_{\mathrm{ref2}}$. In the evaluation phase, S1 is closed and both CS and CR are charged to $V_{\mathrm{ref1}} - V_{\mathrm{ref2}}$. In the integration phase, S2 is

closed and i+ and i- are integrated with two Cint capacitors while both CS and CR are discharged to $V_{\mathrm{ref1}} - V_{\mathrm{cm}}$ where Vcm = (Vdd+Vss)/2. The output voltage is a differential voltage on the load capacitors, CL, as expressed in 2-6.

$$V_{Out} = \frac{\Delta C\left(V_{ref1} - V_{cm}\right)A_{amp}}{C_{int}\left(1 - A_{amp}\right)} \qquad 2\text{-}6$$

where Cint is the value of integrating capacitor, A_{amp} stands for the gain of the differential amplifier, ΔC denotes the input differential capacitance between CS and CR, and V_{ref1} is an arbitrary reference voltage. The use of the same circuit along with a ΣΔ ADC and wireless tags has been reported in [104] as a wireless biosensor. The circuit has been repeated to create a 4 × 4 array of sensors. In the array structure, the integrating capacitors and the Op-Amp are shared among all 16 blocks. The selection of blocks has been implemented using N-type and P-type array-clock controllers. The main disadvantage reported for this topology is its low sensitivity of 3 mV/fF and consequently its low resolution of 10 fF.

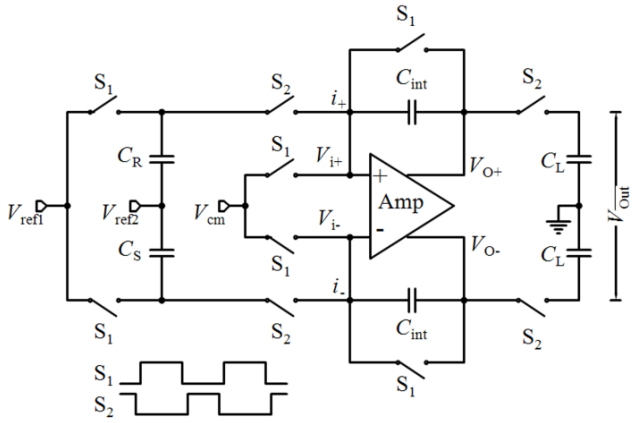


Figure 2.5 A switching capacitive interface circuit proposed in [103].

2.2.2.2 Second-generation Core-CBCM Circuitry with Differential Current

The second generation of core-CBCM circuits include a differential current mirror that can generate the difference between the current of the sensing side and the reference side. In this section these circuits have been explained in detail.

2.2.2.2.1 Charge-based Capacitance-to-Voltage Converter (CVC) Using Differential Current

Figure 2.6 demonstrates the implementation of the circuitry proposed in [105]. This circuit differentiates the CBCM currents, i'S and i'R , by adding M9-M10 N-type devices. This circuit mitigates the dynamic range's limitation caused by common mode offset voltage in the CBCM first-generation circuits by differentiating the amplified currents.

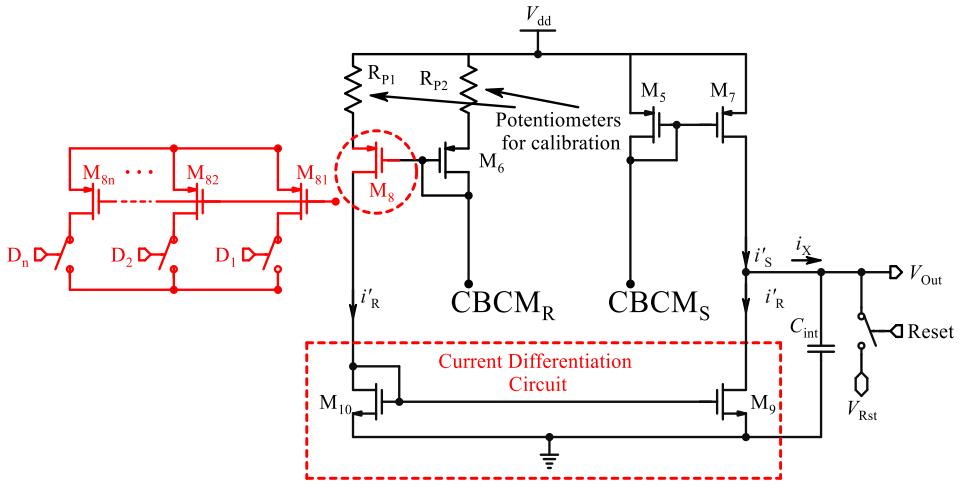


Figure 2.6: A second-generation CBCM circuit with a current mirror composed of M10 and M9 for differentiating the current before integration for increasing the dynamic range. Potentiometers as well as a current mirror with programable gain have been used for calibration.

In the second generation, the mismatch of the devices on the sensing and the reference branch has been reported to be the main source of error in the readings. To alleviate that problem, a calibration mechanism has been proposed using two potentiometers, RP1 and RP2 (see Figure 2.6) to manually adjust the gain of the current mirror composed of (M6, M8) at the time of characterization. In addition, since only a coarse adjustment can be

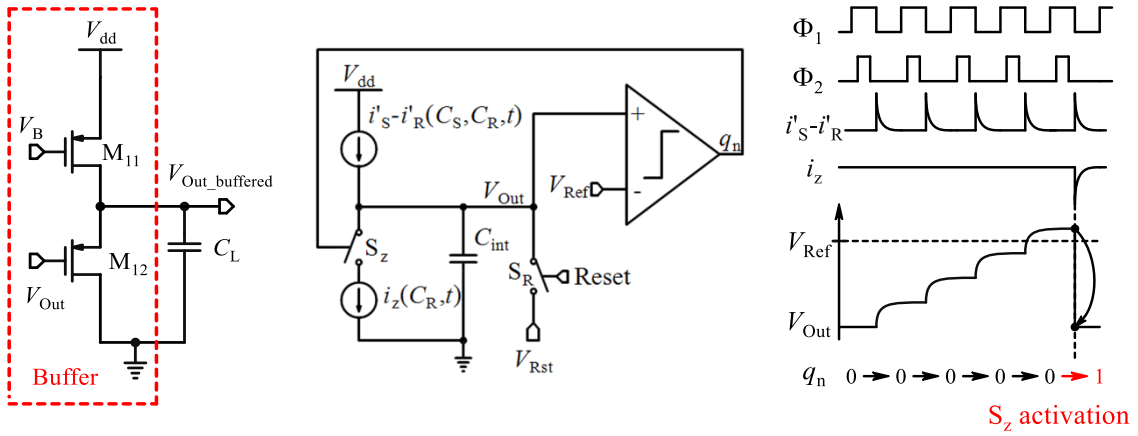
performed in RP1 or RP2, M8 has been implemented as a connection of multiple transistors in parallel, connected to switches that can be digitally turned on or off. In this implementation, the gain of the current mirror that is on the reference side of the CBCM can be digitally adjusted before putting the sample. The aspect ratio of W/L of M8 has been increased in a binary fashion as shown in 2-7.

$$\left(\frac{W}{L}\right)_6 = 2^1\left(\frac{W}{L}\right)_{81} = 2^2\left(\frac{W}{L}\right)_{82} = \cdots = 2^n\left(\frac{W}{L}\right)_{8n} \qquad 2\text{-}7$$

A sensitivity of about 250 mV/fF in 0.18 µm technology and 1.8 V power supply voltage and an increased IDR of about 2.7 fF with a resolution of about 10 aF have been reported for this circuit. In the early chips published in [46], [52], [105], the output of the chip was an analog voltage and external ADCs were required to convert the voltage to a digital output. To cancel the effect of parasitic elements of the PAD and I/O Pin, in [98], a source follower buffer has been added consisting of M11 and M12 to the output of the circuit shown in Figure 2.6, (see Figure 2.7 (a)). The buffer also makes it possible to drive a larger capacitor, CL, for further high-frequency noise filtering. This circuit has been used for the detection of Salmonella and E. coli bacteria.

2.2.2.2.2 Charge-based Analog-to-Digital Converter (ADC) Using Differential Current

An on-chip ΣΔ modulator with low complexity has been adapted to the circuit in [61] to generate digital output that is shown in Figure 2.7 (b). In Figure 2.7 (c), a conceptual model of operation for this ADC is illustrated. The digital output is 0 in every clock pulse if the accumulated voltage on the integrating capacitor is lower than a reference voltage, Vref. The output becomes 1 as soon as VOut >= Vref . This condition triggers SZ switch that discharges the integrating capacitor. Considering a predefined number of bits for the output, higher capacitance results in more 1s in the output which translates to a higher output value.



(a) (b) (c)

Figure 2.7 (a) Source follower output buffer, (b) simple model of the ΣΔ modulator, (c) applied clock pulses, differential current, ΣΔ current, output voltage, and the bitstream of the sensor.

The proposed circuit has been examined in [46], [61], [65] by using polyelectrolyte solutions, chemical solvents with known dielectric constants, and bacteria for growth monitoring in [70], [105]. In [98] (M5 and M7) and (M6 and M8) pairs have been biased in the subthreshold region instead of the saturation region. The objective was to benefit from the increased gm, which is exponential in the subthreshold region in contrast to quadratic in the saturation region. In addition, this could mean the operation of the sensor in the ultra-low-power region. A simple circuit with one current mirror was fabricated to test this idea. However, the transistors in the subthreshold region are higher nonlinear which in turn resulted in significantly limited IDR.

2.2.2.3 Third-generation Core-CBCM Circuitry

The third generation of core-CBCM circuits include differential output and on-chip analog to digital converters that has been explained in this section.

2.2.2.3.1 Two-stage Current Mirror-based Circuitry

Single-ended structures suffer from limited dynamic range. An idea has been proposed in [50], [62] to use two copies of the differential current, namely, i'S - i'R as well as i'R - i'S, to create a differential rail-to-rail output voltage. This circuit not only mitigates the common mode noise but also doubles the IDR compared to a single-ended output (see Figure 2.8 (a)). In this circuit, in an ideal case, Cint+=Cint-=Cint, and both currents Δi+=iS-iR, and Δi-=iR-iS are amplified with current mirrors with equal gains. The differential output voltages (VOut±) are given in 2-8 [62].

$$V_{Out\pm} = \pm \frac{A_I . \Delta C . (V_{dd} - V_{ss} - |V_{thp}|) . f_S}{C_{int} . f_{int}} + V_{off\pm} + V_{cm} \qquad 2\text{-}8$$

where Vdd and Vss are dual supply voltages, and Vcm represents the common-mode voltage at the output nodes. Voff± denotes the offset voltage after integration of Δi+ and Δi-. Integration is performed during a single period of Φ1 and Φ2. Equation 2-9, describes the differential output [62].

$$\Delta V_{\mathrm{OUT}} = \frac{2 . A_I . \Delta C . (V_{dd} - V_{ss} - |V_{thp}|) . f_S}{C_{int} . f_{int}} + \Delta V_{off} \qquad 2\text{-}9$$

The equation is straightforward if ΔVoff =Voff+-Voff-=0, which only happens under ideal conditions. In practice, the output has some offset voltage due to the mismatches between the sensing and the reference sides of the circuit.

In [15], [62], to alleviate the offset voltage and reach a higher dynamic range, floating gate transistors for the M7 and M12 in the current subtractors are utilized in the current mirrors. Furthermore, a combination of electron injection and tunneling has been reported as extra calibration techniques. The gate of the transistor must be isolated via a high-quality insulator (SiO2) to provide a reliable charge storage node.

In [106], simple current mirrors are replaced by cascade current mirrors shown in Figure 2.8 (b). The motivation has been to achieve higher linearity in the output of current mirrors.

The sensitivity of this sensor is increased to 1.42 V/fF. Despite showing a significantly high resolution, the output voltage swing restriction due to cascade current mirrors limits the IDR to about 0.3 fF.

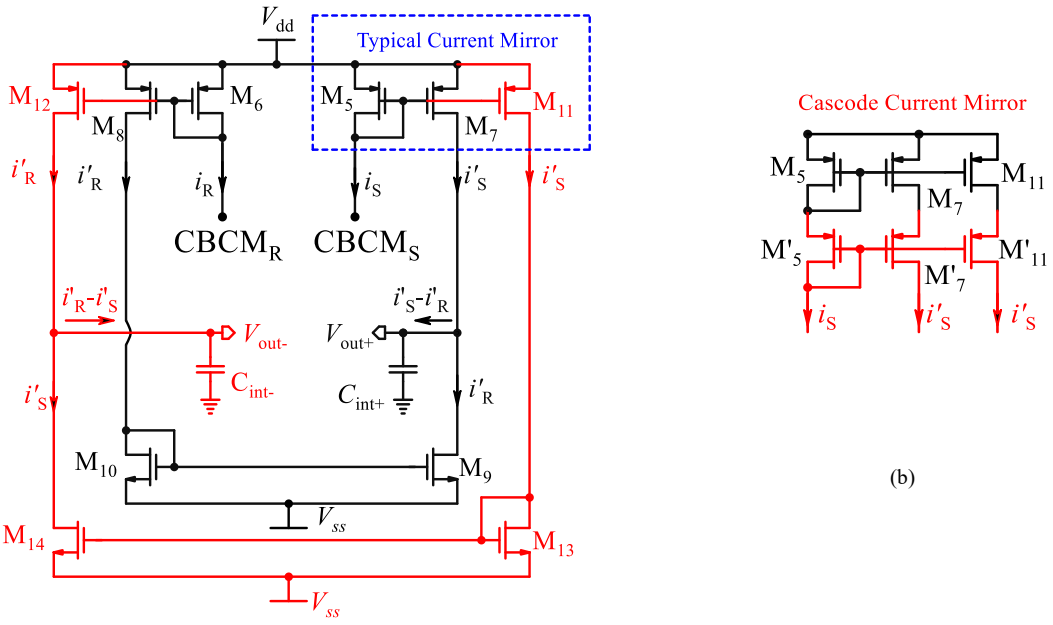
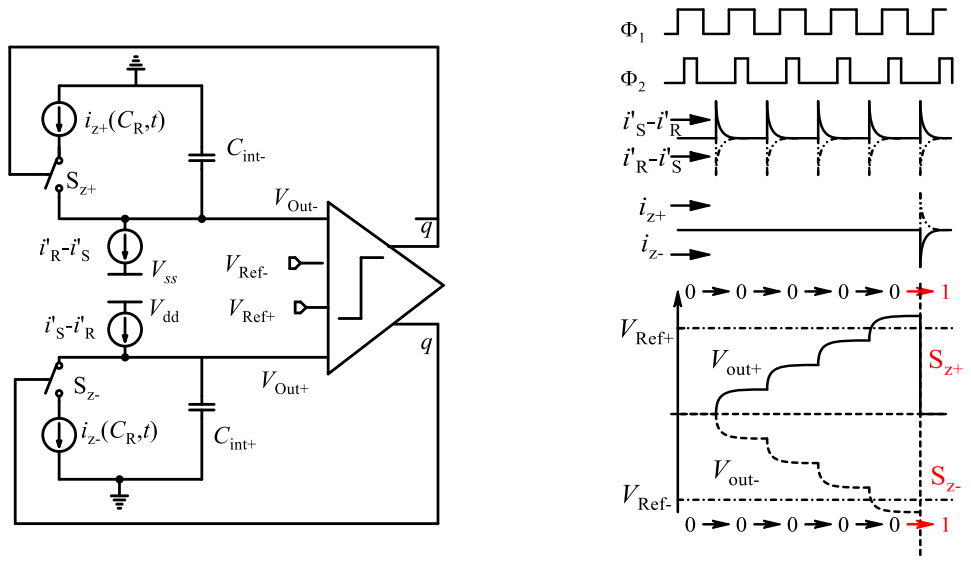


Figure 2.8: (a) Third-generation CBCM capacitive sensor, (b) cascode current mirrors replaced in [106] for higher linearity.

2.2.2.3.2 Differential Charge-based ADC

In [75], an extended version of the ΣΔ modulator in [61] is proposed to be implemented on a chip and provide a digital output (see Figure 2.9 (a)). If VOut+-VOut- > VRef+-VRef-, the comparator will close Sz+ and Sz- switches. As a result, iz- will be subtracted from the positive differential current i'S- i'R and iz+ will be added to the negative differential current.



(a) (b)

Figure 2.9 (a) A ΣΔ modulator adapted to a fully differential core-CBCM capacitive sensor, (b) the related signal diagrams.

Figure 2.9 (b) illustrates the generated signals. Similar to the ΣΔ modulator in [61], the ADC reading was considered in a predefined n number of clocks that resulted in an n-bit output. This sensor has been characterized using chemical solvents [75], adopting 10 bits for the digital output. A sensitivity of about 350 mV/fF and a dynamic range of 10 fF in 0.35 µm CMOS technology has been reported for this circuit.

2.2.2.4 Core-CBCM Capacitance-to-Frequency Conversion (CFC)

A combination of CBCM and CFC circuitries enables a high-resolution and high-IDR differential input circuitry and is proposed in [107]. The circuit proposed in [108] is shown in Figure 2.10. Since the output of CFC circuitry is frequency rather than voltage, higher bandwidth is possible to be achieved. In this circuit, two integrating capacitors are used to convert the output currents into the output voltage. The output voltage is compared to Vref and passed to a delay gate, D. As soon as the output of the delay gate is transitioned to high, the integrating capacitors are discharged. The output frequency is shown to be a function of

the capacitance that is being evaluated. To achieve a high resolution, small integrating capacitors are required while for a large dynamic range, larger integrating capacitors are needed. In this scheme, first, the CBCM current is converted to voltage, and then the voltage is converted to frequency. Thus, the voltage swing limitation still exists, and a small IDR of a few femto Farads has been reported.

Another circuit is proposed in [48] that uses a combination of an integrator, and a Schmitt trigger which is illustrated in Figure 2.11. In this topology, currents from the sensing and the reference sides of the CBCM circuit are separately mirrored and integrated into both charging and discharging cycles creating a triangular signal. The Schmitt trigger block is used to convert the triangular signal to a square wave signal and a counter is used to create a digital output. The difference is calculated in the software based on the digital outputs of the two sides. The main challenge within both topologies is to achieve a high resolution since the differentiation takes place at the output stage instead of using a CBCM differential current.

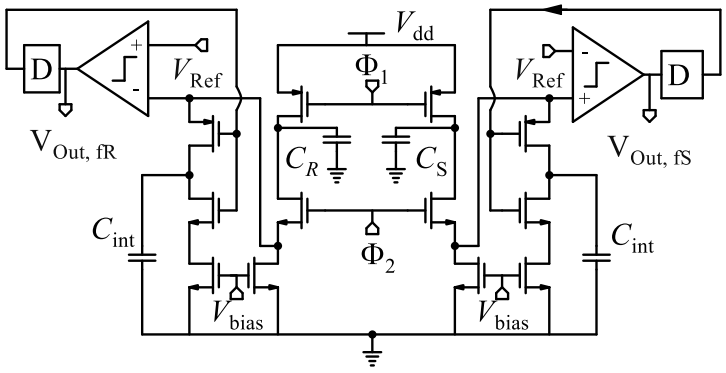


Figure 2.10: A combination of the CBCM method and conversion to a frequency.

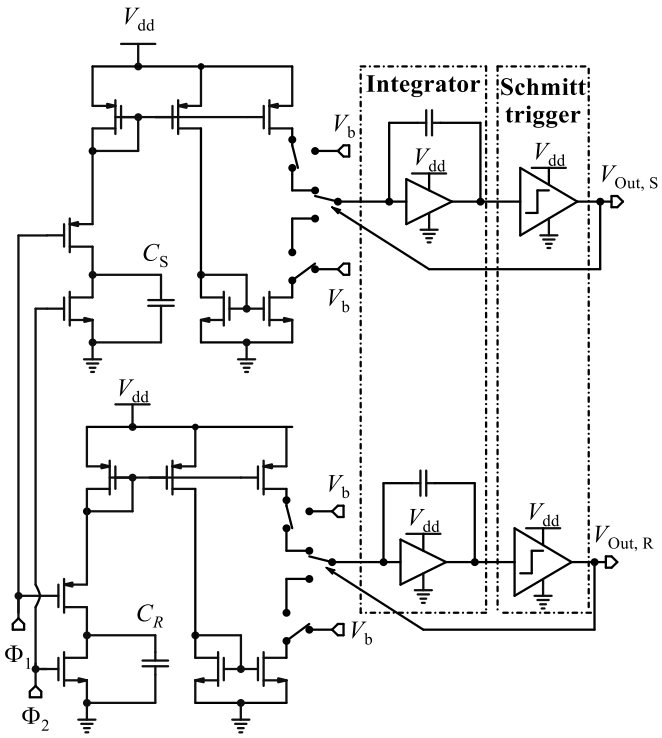


Figure 2.11: circuit topology proposed in [48]

2.2.2.5 CBCM-based Array Implementations

In [3], [75], [100], [15], [62], an array of capacitors is implemented as shown in Figure 2.12 (a). In this implementation, the CBCM block has been repeated for every cell, as depicted in Figure 2.12 (a), in a column, and each cell has been connected to a shared current mirror circuitry using PMOS switches to enable the cell (via Enn , n=0,1,2,3 signal). Each one of the command lines En0, En1, and En2 can activate one row to do the measurement. Each column has independent integrating circuitry for current-to-voltage conversion and ΣΔ ADC. One drawback in this topology is the addition of parasitic capacitances of the Enn switches to the common node of the current mirror. As a result, the nonlinearity can increase if the array size grows.

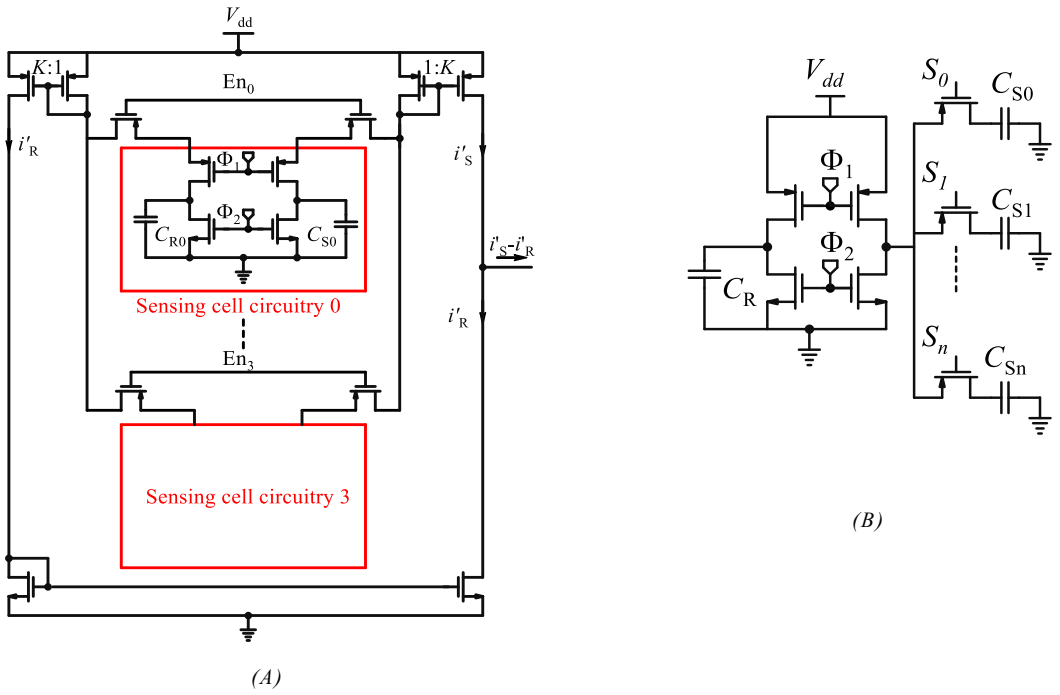


Figure 2.12 A 3×3 sensor array configuration with the capability of simultaneous evaluation of three different capacitances.

In another CBCM-based array design, as shown in Figure 2.12 (b), an array of 8 × 8 electrodes has been implemented by adding switches in the path of current to fulfill the multiplexing of the electrodes [74]. The bottleneck of this technique is the addition of parasitic capacitances of many switches that can hinder the implementation of a large array. In Chapter 3, a novel CBCM array chip has been proposed that supports a large array size using a single shared reference for all the electrodes.

2.3 The Proposed Circuits and System

A schematic of the proposed system is illustrated in Figure 2.13. The building blocks of our proposed system-on-chip include a CBCM circuit, a calibration circuitry consisting of an array of switched capacitors, a feedback circuit, a current-controlled 300 MHz oscillator, a counter-serializer, and the IDEs realized on the topmost metal layer. The output of the chip is connected to a microcontroller through which the data is transmitted to a

customized GUI. In this section, we demonstrate the details of the design of each block and discuss the characteristics of the proposed system.

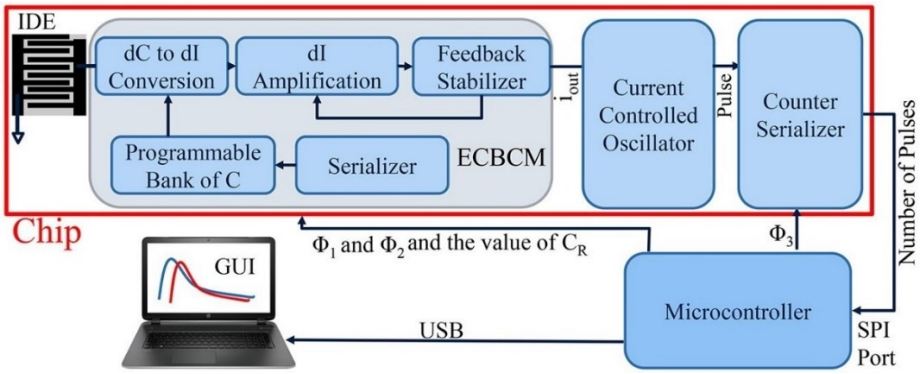


Figure 2.13: The system-level block diagram of the proposed capacitive sensor

2.3.1 IDE-sample Interface Model

The proposed capacitive sensor has been implemented in AMS 0.35 µm CMOS technology. This sensor consists of two almost identical interface circuits connected to two IDEs. To increase the sensitivity, the passivation layer on the electrodes is etched using PAD masks. As a result, an aluminum oxide layer forms naturally on top of the aluminum electrodes when they are exposed to air and acts as a passivation layer. Figure 1.3 (b) illustrates a cross-section schematic and the equivalent circuit model of the electrode when it is exposed to the sample. The electric equivalent model is similar to the one shown in [17], [68]; however, the effect of remnants, modeled by ΔC(t), is considered in this thesis for the first time. CPL represents the capacitance formed by the Al2O3 passivation layer, in series with the double-layer capacitance, CDL. Rsol models the resistivity of the solution, in parallel with the capacitance of the solution material, Csol. The presence of bioparticles in the proximity of the electrodes, or attachment to the surface can change the structure, and as a result, alter the capacitance which is shown with σC(t) in this model. The relative permittivity, εr, of the passivation layer composed of Al2O3 is equal to 9 while it is 80 for a typical water-based ionic buffer sample medium solution. The thickness of the Al2O3

layer that is naturally formed on the electrode reaches a few tens of nanometers while the thickness of double-layer capacitance is around 1 nm [109]. Considering the thickness and the relative permittivity values, CPL is much smaller compared to CDL. Thus, the total capacitance of the series structure of CPL and CDL is close to the value of CPL. The presence of CPL is therefore crucial for eliminating the effect of CDL as one of the components of the overall offset capacitance for increased ECR.

2.3.2 Enhanced CBCM Interface Circuit (ECBCM)

In Figure 2.14, the second-generation CBCM topology is demonstrated in gray. The purpose of this circuit is to transduce the differential input capacitance (dC = CIDE - CR) to the differential current. An integrating capacitor, Cint, is conventionally utilized to convert the differential current to the output voltage as shown in gray dotted lines as discussed in 2.2.2. In equation 2-5), we showed that the transfer function of ($\overline{\iota_{out}}$/dC) where ($\overline{\iota_{out}}$) is the average of output current of the CBCM block is linear. However, with Cint as a load, the drain-source voltage of N2 (VD), varies following the charge and discharge of Cint, while the drain-source voltage of N1 (VC) remains fixed for a given CR. In the circuit shown in grey, I1, and i'R also depend on the drain-source voltage due to the channel length modulation effect. As a result, I1, which is required to be equal to i'R, can significantly deviate because λ, the channel-length modulation parameter, is non-zero. The use of long-channel devices for N1 and N2 can to some extent suppress the adverse effect of λ but cannot completely solve this systematic deviation [110]. Cascode current mirrors are also known and have been considered to alleviate the adverse effect of channel length modulation by utilizing an additional stage to shield the current mirrors from being affected by the variation of the load voltage [111]. Despite the improvement, cascode topology still has restrictions

due to the limited voltage headroom. The use of current-voltage mirrors in [102], as discussed in Section 2.2.2.1, and cascode current mirrors in [106], as discussed in Section 2.2.2.3, increase the linearity at the cost of a lower dynamic range.

The focus of this chapter has been on showing the effectiveness of the novel feedback loop for CBCM circuits that reduces the above-mentioned tracking error for a wide range of input differential capacitance values. The proposed ECBCM topology has a feedback path composed of N2, N3, and the Op-Amp, shown in Figure 2.14, that forces VD to track VC regardless of the value of CIDE. Simulation results in Figure 2.15 (a) show the deviation of VD from VC for different CIDE values in typical CBCM with Cint. Figure 2.15 (b) demonstrates that in the ECBCM topology, the drain-source voltage of N2 successfully tracks the drain-source voltage of N1. The result is that I1 will be equal to i'R, regardless of the value of CIDE. Equations 2-10 and 2-11 show the transfer function of the ECBCM circuit.

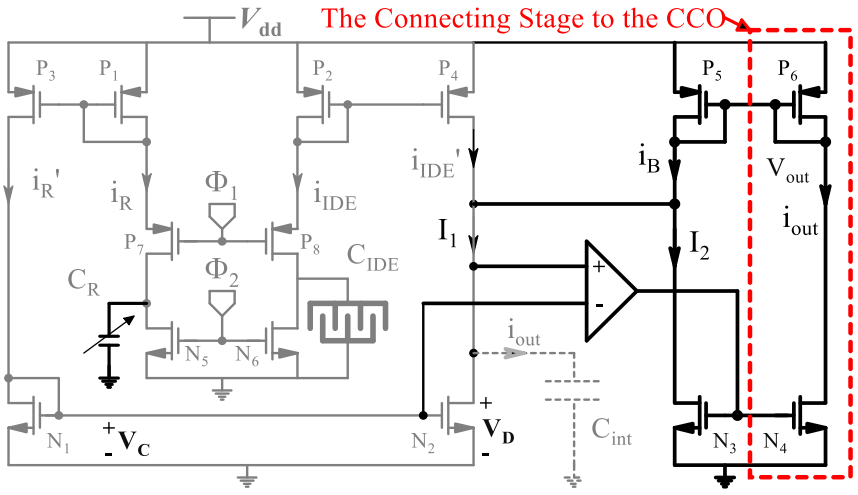


Figure 2.14: (A) Proposed circuit: The CBCM CVC is shown in grey with an integrating capacitor for current-to-voltage conversion depicted in dotted lines. The proposed feedback path consists of the N2, N3, and Op-Amp blocks shown in black that along with the CBCM circuitry form the ECBCM topology. the opAmp is used from the TSMC 0.18 µm CMOS Standard Cells Library - tsmc-cl018g_sc-x_2004q3v1 [112] without any change.

$$i_{out} = \frac{W_{N_4}}{W_{N_3}} \frac{L_{N_3}}{L_{N_4}} \frac{1 + \lambda V_{out}}{1 + \lambda V_D} \left(k \times (i_{IDE} - i_R) + i_B\right) \quad 2\text{-}10$$

$$i_B = \frac{k'}{2} \frac{W_{P_5}}{L_{P_5}} (V_{dd} - V_D - V_{TP})^2 \times \left(1 + \lambda(V_{dd} - V_D)\right) \quad 2\text{-}11$$

where k denotes the gain of current mirrors composed of P1-P3 and P2-P4, VTP is the threshold voltage of the P-channel MOSFET device. W and L stand for the width and length of devices, respectively. Vdd is the supply voltage, and iB, given in 2-11, denotes the offset current from P5. The equation is not linear, due to the terms $1 + \lambda V_{out} / 1 + \lambda V_D$ and iB. To alleviate the nonlinearity, long channel transistors are used for the realization of N3 and N4 at the final stage (see Table 2.2 for sizing) which helps to fulfill $\lambda V_{out} \ll 1$ and $\lambda V_D \ll 1$ conditions. Thus, the nonlinear term $1 + \lambda V_{out} / 1 + \lambda V_D$ can be approximated as unity. To decrease the effect of iB, W/L of P5 is minimized. Thus, $k \times (i_{IDE} - i_R) \gg i_B$, and equation 2-10 can reduce to a linear equation given in 2-12. It is noteworthy to mention that, in 2-10, the channel-length modulation effect of P3 and P4 are not considered for simplicity.

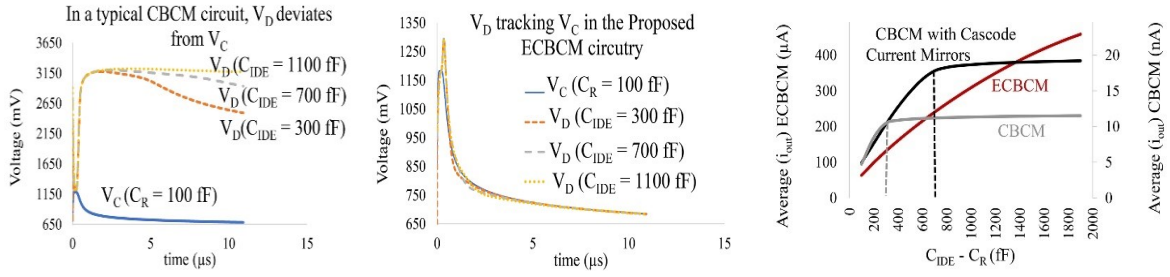


Figure 2.15: Performance of proposed circuit using ECBCM versus CBCM (a) VC (solid) and VD (dashed) for different values of CIDE when the output is connected to an integrating capacitor, (b) The same simulation for the ECBCM with the feedback loop, (c) The transfer function of the proposed ECBCM, the CBCM with adding cascode current mirrors similar to cascode topology used in [111], and CBCM circuit.

$$i_{out} = \frac{W_{N_4}}{W_{N_3}} \frac{L_{N_3}}{L_{N_4}} \times k \times (i_{IDE} - i_R) \quad 2\text{-}12$$

Besides, P5 is added to the topology for adding a bias current which is proportional to the value of reference capacitance as a baseline. This helps when the CCO has nonlinear behavior for very small currents (the CCO used in this circuit shows nonlinearity for currents of less than 1 µA). Figure 2.15 (c) demonstrates the transfer function of the proposed

ECBCM and the CBCM with Cint circuits with and without cascode current mirror topologies. We have considered the dynamic range of each circuit to be the maximum input differential capacitance variation for which the transfer function ($\overline{\iota_{out}}$/ dC) maintains above 98% linearity with respect to linear regression, (for the linearity of the proposed ECBCM circuit see Section 2.4.5). From Figure 2.15 (c), the IDR is about 200 fF (from 100 fF to about 300 fF) for the CBCM circuitry, about 600 fF (from 100 fF to 700 fF) for the CBCM with cascode current mirrors, and about 1800 fF (from 100 fF to 1900 fF) for the ECBCM. These numbers might slightly vary for different sizing (for the sizing in this chapter refer to Table 2.2) but in general, reflect the effectiveness of the proposed feedback loop.

Table 2.2: Device sizing

DEVICE	W/L (µM)	EQ[1]	DEVICE	W/L (µM)	EQ
P_1, P_2	0.5 / 4	(3)	N_1, N_2	20 / 0.35	(2)
P_3, P_4	40 / 0.35	(3)	N_3	8 / 10	(3)
P_5	0.4 / 0.5	(2)	N_4	4 / 10	(3)
P_6	6.8 / 0.35	(2)	N_5, N_6	0.4/10	(-)
P_7, P_8	0.4 / 10	(4)	N_7	3 / 0.35	
P_9, P_{10}, P_{12}, P_{13}	3.4 / 0.35	(-)[2]	N_8 ,, N_9	2.2 0.35	(-)
P_{11}, P_{14}	34 / 0.35	(-)	C_{O1}, C_{O2}, C_{O3}	50 FF	(-)

[1] Eq: the equation that the sizing is calculated from 2 (-): Obtained empirically.

2.3.3 Digitally Programmable Bank of Capacitors

The reference capacitance, CR, is implemented using a bank of on-chip capacitors in a topology shown in Figure 2.16. This topology allows the implementation of a digitally programmable capacitor. It consists of seven NMOS switches, S1 to S7 in series with seven capacitors, C1 to C7 where Cn = 2×Cn-1. Considering the ON/OFF state of each switch, the equivalent capacitance value can be obtained as $C_R(n) = C_1 \times (S_1 + 2 \times S_2 + \cdots + 2^{n-1} \times S_n)$ where S_i is equal to 1 if the switch of the ith branch is ON and is 0

otherwise. The primary role of the bank of capacitors on the reference side is to provide a wide range of capacitance to cancel the total offset capacitance, including ΔC of remnants to maximize ECR during the experiment. This topology makes the necessary calibration possible with a wide input offset adjustment range (IOAR). C1 is chosen to be 10 fF in this implementation, thus, CR of up to 1.27 pF with a step of 10 fF change (42 dB) can be programmed. The effect of all parasitic capacitances of the NMOS switches on each path is compensated by adjusting the size of the CPOLY cap of that path in the post-layout simulations.

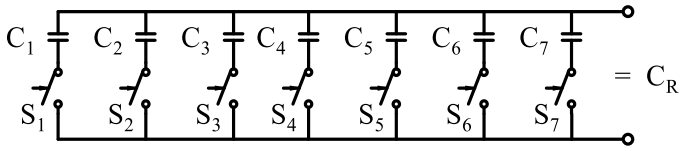


Figure 2.16: Digitally programable bank of capacitors ranging from 10 fF to 1.27 pF with a 10 fF resolution.

2.3.4 Differential Current-to-Digital Conversion

The output current of ECBCM (iout in Figure 2.14) feeds a current-controlled relaxation oscillator similar to the one proposed in [113]. The topology is shown in Figure 2.17 (a). The W/L ratio of transistors (see Table 2.2 for sizing) in this oscillator has been modified to increase the IDR of the CCO to around 280 μA where its oscillation frequency can reach 300 MHz. CO1, CO2, and CO3, in series with the SO1, SO2, and SO3 switches are added to the topology to create a programmable oscillation frequency for test purposes. The path, consisting of P6 and N4 is added to connect ECBCM to the CCO. To generate the digital output from the oscillation frequency, a counter is implemented. A serializer is designed and implemented that loads the counter's value in every measurement cycle and outputs the value during the next cycle (see Figure 2.17 (b) for the counter and the serializer topology, Figure 2.17 (c) for the circuit that creates the timing signals, and Figure 2.17 (d) for the

timing diagram). When Φ1 becomes low, CR and CIDE are charged. Thus, the number of pulses must be counted while Φ1 is low. The NOR gate at the input of the counter satisfies this condition. The serializer outputs the number that was loaded in the previous cycle with the clock pulse of Φ3. In each cycle, the generated number is loaded in parallel into the serializer as soon as Φ2 becomes high. The reset signal of the counter is inverted Φ2 to keep the counter value at zero during the time that capacitors are being discharged. The implemented counter-serializer has 12 bits (see section 2.4.1); however, only 3 bits are shown in Figure 2.17 (b) for simplicity. The frequency of Φ3 must be chosen high enough to output all 12 bits when Φ1 is low.

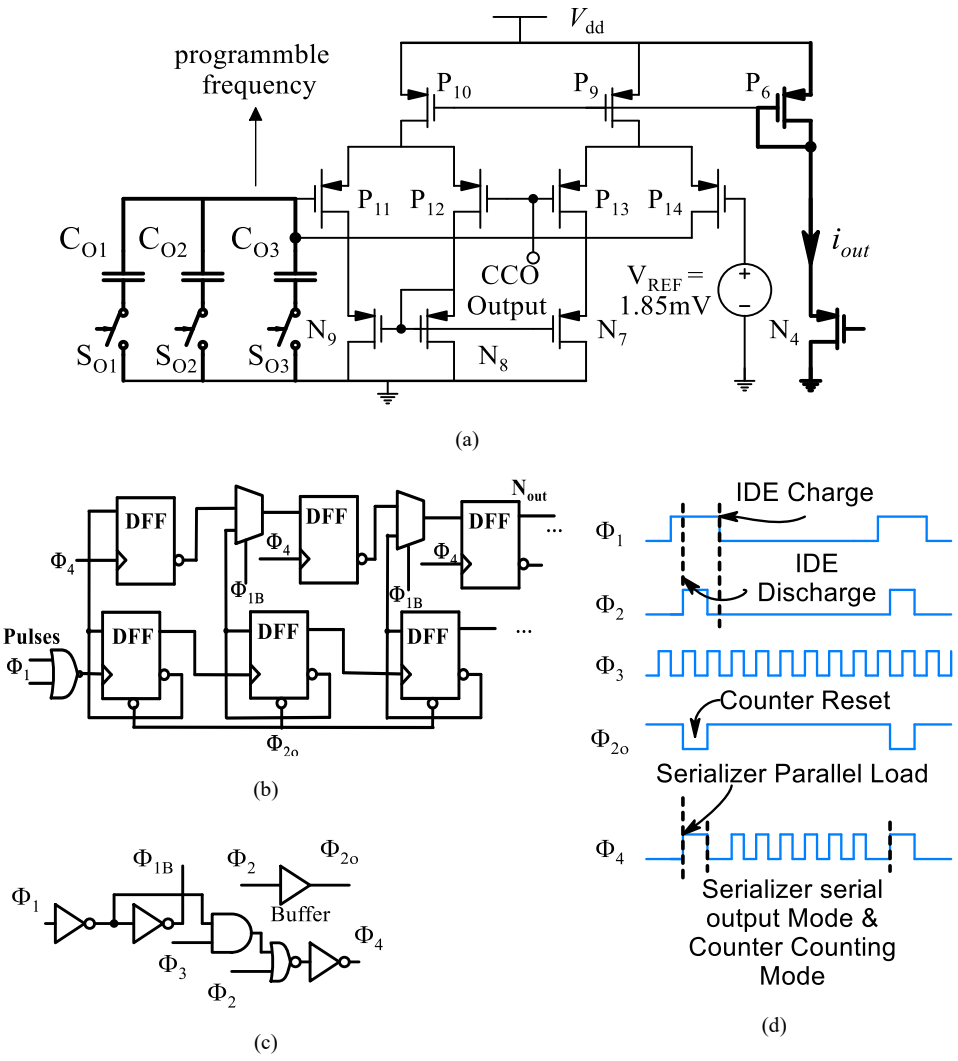


Figure 2.17: Implemented circuit topologies: (a) The linear CCO using a relaxation oscillator topology introduced in [113], (b) Counter-serializer topology (DFFs are digital flip-flops), (c) The circuit generating the timing signals, (d) Counter-serializer timing diagram.

2.3.5 Maximum Measurement Speed Using ECBCM

Figure 2.18 shows the reference (P1, P7, and N5) and the sensing (P2, P8, and N6) branches of ECBCM circuitry during Φ1 and Φ2 at a low level (evaluation phase). At the onset of the evaluation phase, P7 and P8 turn on in saturation and stay in saturation as long as VCR < |VTP7| and VIDE < |VTP8|, respectively, where VCR is the voltage drop on CR and VIDE stands for the voltage drop on the IDEs. When P7 and P8 are in saturation P1-P7 and P2-P8 pairs constitute current sources. The current value is a function of W/L of these pairs, as given in 2-13, where μp and Cox are the mobility of holes and gate oxide capacitance in a P-channel MOSFET. We call this phase the "constant current" phase.

$$i_{R,cte} = i_{IDE,cte} = \frac{\mu_p C_{ox}}{2} \frac{W_{P_7}}{L_{P_7}} \frac{W_{P_1}}{L_{P_1}} \left(\frac{V_{dd} - (|V_{TP1}| + |V_{TP7}|)}{\sqrt{\frac{W_{P_7}}{L_{P_7}}} + \sqrt{\frac{W_{P_1}}{L_{P_1}}}} \right)^2 \quad 2\text{-}13$$

When VCR > |VTP7|, P7 enters the triode region. The same happens to P8 when VIDE > |VTP8|. In this phase, P7 and P8 act like resistances, shown as R, with the value given in 2-14. We call this phase the "RC" phase. As CR and CIDE are charged, the current in the path decays, and the voltage drop on the diode connected P1 and P2 decreases. Therefore, V rises, and the value of R reduces according to 2-14. VIDE in the constant current mode region is given in 2-15.

$$R = \frac{1}{\frac{k'}{2} \frac{W_{P_7}}{L_{P_7}} (V - |V_{TP7}|)} \quad 2\text{-}14$$

$$V_{IDE} = R_{sol} \times i_{IDE,cte} \left(1 - e^{-\frac{t}{R_{sol} \times (C_{sol} + dC + C_{re})}} \right) + \frac{i_{IDE,cte}}{C_{PL}} t \quad 2\text{-}15$$

The sensitivity of the interface circuit to dC is zero in the constant current mode since iR,cte = iIDE,cte. Therefore, the minimum time for proper measurement should include the RC phase. The time, t1, when the circuit is in constant current phase can be calculated from2-14 2-16 by putting VIDE = |VTP7|. The equation for calculating t1 is given in 2-17.

$$R_{sol} \times i_{IDE,cte} \times \left(1 - e^{-\frac{t_1}{R_{sol} \times C_{sol}}}\right) = |V_{TP7}| - \frac{i_{IDE,cte}}{C_{PL}} t_1 \qquad 2\text{-}17$$

Since 4 × RC is required for the settlement, the minimum time for proper measurement will be Tmin = t1 + 4 × RC. Since R varies, we approximated Tmin to α × t1 for simplicity where α >1, and its value can be obtained either empirically or using simulation. The maximum frequency of CBCM non-overlapping clocks, Φ1 and Φ2, will therefore be Fmax= 1 / (Tmin + Tdischarge +Tnon-overlap) where Tnon-overlap is the time overhead for creating the non-overlapping signals, and Tdischarge stands for the discharge time. Since, in our interface circuit, the evaluation of the capacitance completes in one cycle, Fmax represents the maximum measurement speed.

It is noteworthy to mention that, based on the above discussion, minimizing the length of P7 and P8 for a given width, results in a faster response. Table 2.2 shows that we have not used minimum length for these devices. This suggests that the topology has the potential to achieve even faster speed if it is needed. There are some considerations that we would like to mention about the sizing of P7 and P8. First, P7 and P8 are critical devices in terms of device noise in this topology. The main reason is that noise of these devices is amplified by the current mirror gain composed of P1-P3 and P2-P4 pairs. Thermal noise of MOSFET devices is related to gm, $\overline{I_n^2} = 4KT\gamma g_m$, (transconductance g_m is inversely related to the L, $g_m = \mu C_{ox} \frac{W}{L} \left(V_{gs} - V_{TH}\right)$. Fliker noise has also an inverse relation with L, ($\overline{V_f^2} = \frac{K_f}{C_{ox}WL} . \frac{1}{f^{\alpha}}$) [110]. Since with a value larger than the minimum length, an acceptable speed has been reached, we have chosen a longer L for lowering the noise. Additionally, from the

mismatch perspective, larger devices suffer less from mismatch which is another benefit we wanted to consider in this circuit dedicated to high-accuracy sensing. Moreover, from the application point of view, shorter lengths of P7 and P8 allow significantly higher transient currents at the onset of the transition of Φ1 from high to low. Since the application of this sensor is life science, sudden changes in the excitation voltage or current, with significant magnitude might result in biological stress [56], [114]. Another consideration is the error due to the charge injection mismatch in the CBCM topology requiring that the size of devices be minimized. Based on quantitative analysis in [115], the total error caused by charge injection mismatch for PMOS device sizes of W=10 µm and L=0.6 µm is less than 4% when the capacitance under test is less than 1 fF. The error decreases to less than 3% for larger capacitances under tests of >20 fF. The 4% error in the capacitance reading can typically be acceptable for quantitively analyzing the surface changes in most of the life science applications. Besides, the variable reference capacitance that has been implemented on the reference side can be used for compensating mismatches (see Section 2.4.9).

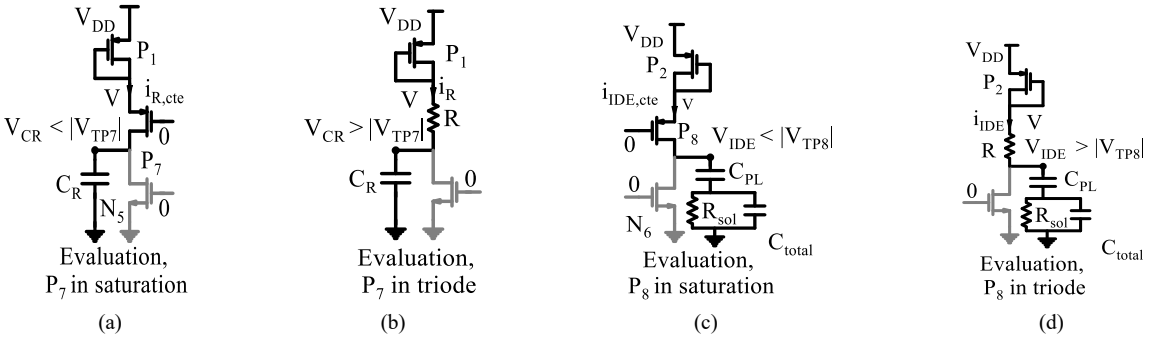


Figure 2.18: Modes of operation of the CBCM reference and sensing branches during the evaluation phase, necessary to obtain the maximum measurement speed: (a) Reference evaluation in saturation mode, (b) Reference evaluation in the triode region, (c) Sensing side evaluation phase in the saturation region, (d) Sensing side evaluation phase in the triode region.

2.3.6 Input-output Transfer Function of the System

The transfer function of the analog-to-digital conversion (number of pulses versus $\overline{i_{out}}$) is obtained by post-layout simulations and is given in Figure 2.19. The transfer function of

the linear region is fitted to the curve N= 11.227 $\overline{i_{out}}$ + 135.7. This linear regression yields R2 = 99%. As a result, the input-output transfer function of the system is described by 2-10 and the transfer function of the CCO.

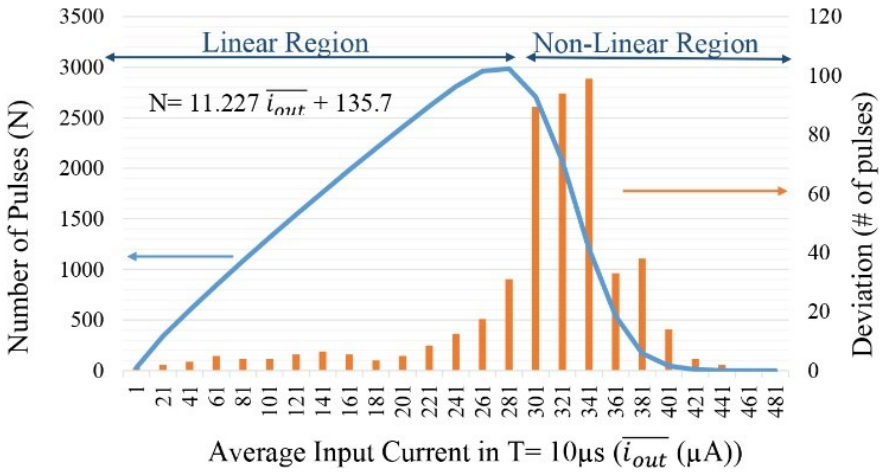


Figure 2.19: Left vertical axis: transfer function of the analog-to-digital converter block based on an evaluation time of 10 µs using post-layout simulation results. Right vertical axis: maximum error in the number of pulses due to device and supply voltage noise during the same time frame.

2.3.7 Maximum Sensitivity Analysis

As seen in Figure 2.19, the oscillation increases linearly until 280 µA and then non-linearly decreases until it stops at around 420 µA which is called the "oscillation threshold" in this thesis. The sensitivity of the system is a function of the sensitivity of the ECBCM block and the frequency of the oscillator, given in 2-18.

$$S = 11.227 \left(\frac{\overline{i_{out}}}{dC}\right) \qquad 2\text{-}18$$

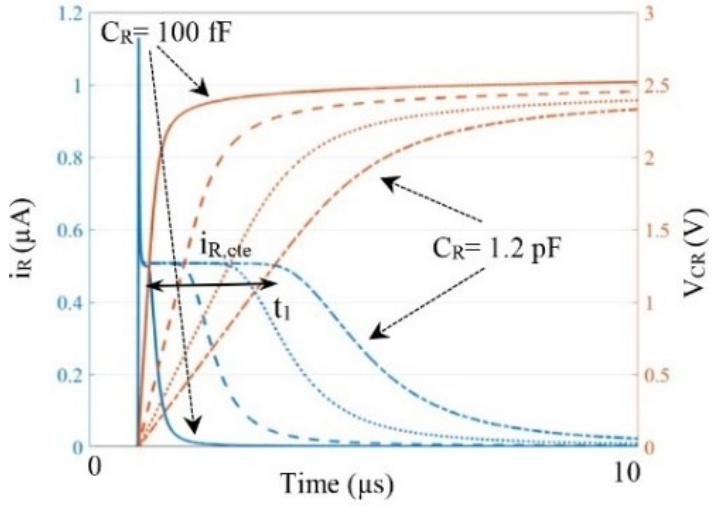
where $\overline{i_{out}}$ is the average of the output current of the ECBCM circuit.

2.4 Results

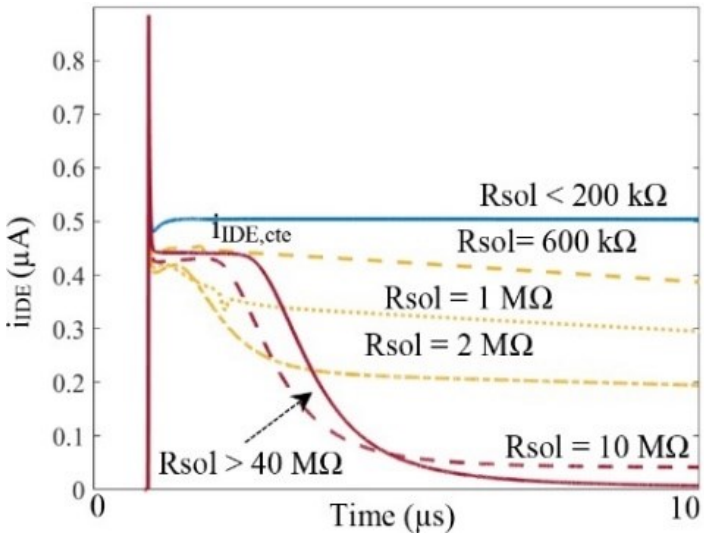
In this section, we present the simulation and experimental results using the microliter droplets of three different chemical solvents.

2.4.1 Measurement Speed

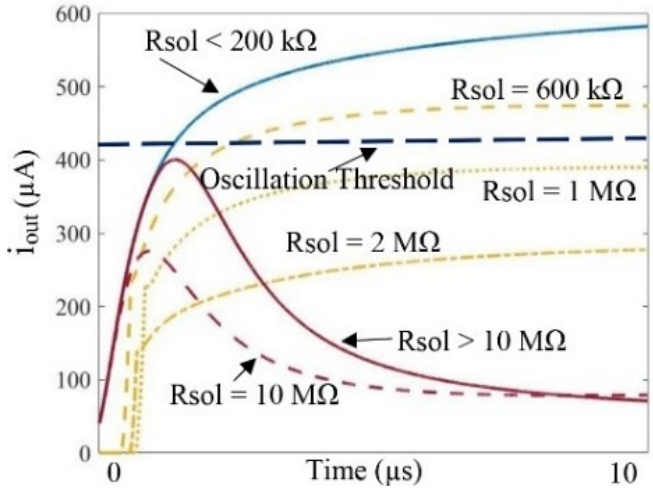
Simulation results in Figure 2.20 (a) show that t1 for the maximum possible capacitance on the reference side, 1.27 pF, is about 4 µs. Therefore, we chose α to be 2.5, which results in Tmin = 10 µs. Moreover, Treset is 3 µs for the reset phase, and an extra 2 µs is also defined to create the non-overlapping signals. Thus, the optimal period for the Φ1 and Φ2 signals will be 15 µs. (frequency = 66.7 kHz). Also, from Figure 2.19, the maximum number of pulses can reach 3000 during 10 µs. Therefore, a 12-bit counter is utilized for generating digital output.



(a)



(b)



(c)

Figure 2.20: Waveform trends of the reference, sensing, and output of ECBCM circuit with respect to different solution conductivities: (a) Charging current curve (Left) and the voltage (right) on the reference side for different values of CR, (b) Charging current curves on the sensing side for different values of parallel resistance, (c) Output current waveforms for fixed values of capacitances and variable Rsols.

2.4.2 The Effect of the Solution Conductivity on the Output of ECBCM

Figure 2.20 (b) demonstrates the simulation results for the sensing side current where the electric equivalent model, discussed in Section.2.3.1, is considered for the IDE-sample interface. It illustrates iIDE waveforms for a fixed value of CR, and Ctotal= Csol+σC+ΔC, and Coffset while Rsol varies. For Rsol < 200 kΩ (high-conductivity solution), the constant current phase becomes larger than the evaluation period and as a result, the sensitivity to dC

becomes zero (curve in blue). On the other hand, when Rsol rises (low-conductivity solution), CPL in series with the Ctotal capacitance becomes dominant and the current waveform trends (shown in red) become like the pure capacitive behavior seen for the reference side (see Figure 2.20 (a)). The region in between is the medium range of resistance (curves in yellow). Figure 2.20 (c) shows the simulation results for the output current of ECBCM block, iout. From 2-12, iout is a function of iR and iIDE. The waveform for the high-conductivity solution is shown in blue. The pattern for the medium conductivity solution is shown in yellow. As the figure shows, for medium- to high-conductivity solutions, part of the curve lies under the oscillation threshold whereas for low- to medium-conductivity, the whole curve is under the oscillation threshold. Also, low conductivity curves, shown in red, stand under the oscillation threshold. Thus, we see two different output patterns that are discussed in Section 2.4.9.

2.4.3 Sensitivity Considering the Effect of Solution Conductivity

The $\overline{\iota_{out}}/dC$ curves are illustrated in Figure 2.21 for different values of Rsol. The highest sensitivity happens for Rsol >100 MΩ shown in red and is 0.22 μA/fF. This value translates to a sensitivity of 2.46 pulses per fF change in capacitance from 2-18. Therefore, the resolution will be 416 aF. The slope of the curve reduces as Rsol drops. Around Rsol = 200 kΩ, the sensitivity becomes zero. The minimum value of Rsol is a design parameter for P1-P7 and P2-P8 sizing. By increasing the W/L ratio of P1 and P2, the value of constant current will increase, which will reduce t1 and, consequently, makes it possible to measure capacitance variations for Rsol $<$ 200 kΩ (equal to 0.05 S/m concerning our electrode dimensions, see Section 2.4.10.1).

2.4.4 Oscillator Noise

The bars in Figure 2.19 demonstrate the deviation in the number of pulses due to device and voltage supply noise for various input current values. The deviation is insignificant in the linear oscillation region, but they become considerably higher when the input current exceeds 280 µA. The experimental results, shown in section 2.5.4, are obtained based on sweeping the bank of capacitors in the full range, as a result, $\overline{i_{out}}$ at some point exceeds 280 µA. This especially

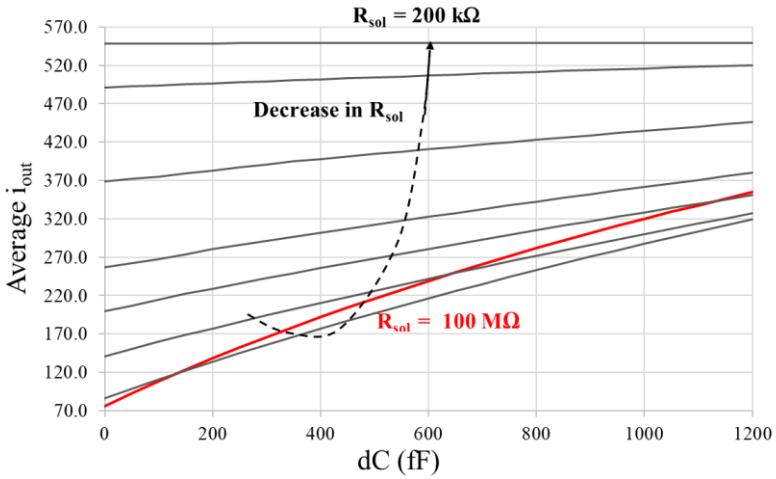


Figure 2.21: Sensitivity analysis for different values of Rsol.

happens when the reference side has a much smaller capacitance than the sensing side. The same happens when Rsol is in the range of low to medium allowing a high transition current to be passed on the sensing side. If the measurement takes place in the linear region of oscillation by adjusting the value of the bank of capacitors to a proper value, the average oscillation noise will be insignificant. The sensor, therefore, can achieve its highest resolution in the linear region since noise is minimum there.

2.4.5 Nonlinearity Analysis

The transfer function of the ECBCM enters a nonlinear region for significantly high input (CIDE-CR). Overall, P4 entering the triode region and Op-Amp entering saturation can be two reasons for the nonlinearity. Figure 2.22 demonstrates the degree of nonlinearity in different given IDRs. The linearity of above 98% is preserved for a change in the differential input capacitance of 2 pF.

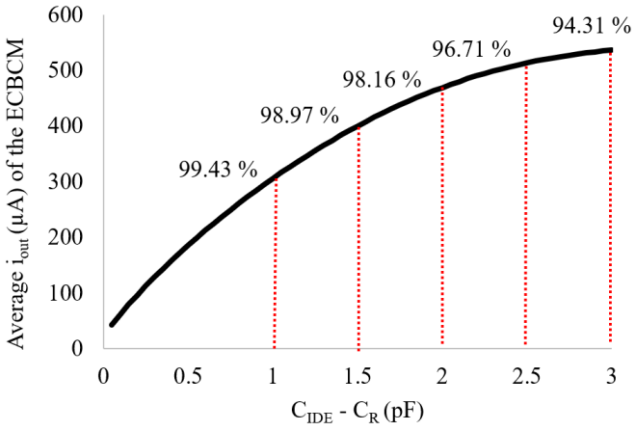


Figure 2.22: Linearity of the ECBCM block for different given IDRs.

2.4.6 Randomness Analysis

2.4.6.1 Monte Carlo Analysis for Mismatch Evaluation

The randomness effect of fabrication on the transfer function of the ECBCM block is illustrated in Figure 2.23. 200 runs are performed to obtain iout in the ECBCM block for the CIDE-CR=1 pF, for which the linearity of the transfer function is above 99%. Based on the simulations, the typical current is 284.3 µA and the standard deviation due to mismatch is 12.52 µA. 113 runs fall under average ± standard deviation which is about 60% of the chips.

The effect of mismatch on the oscillator, shown in the blue histogram, is near optimum where 148 runs fall under the typical condition.

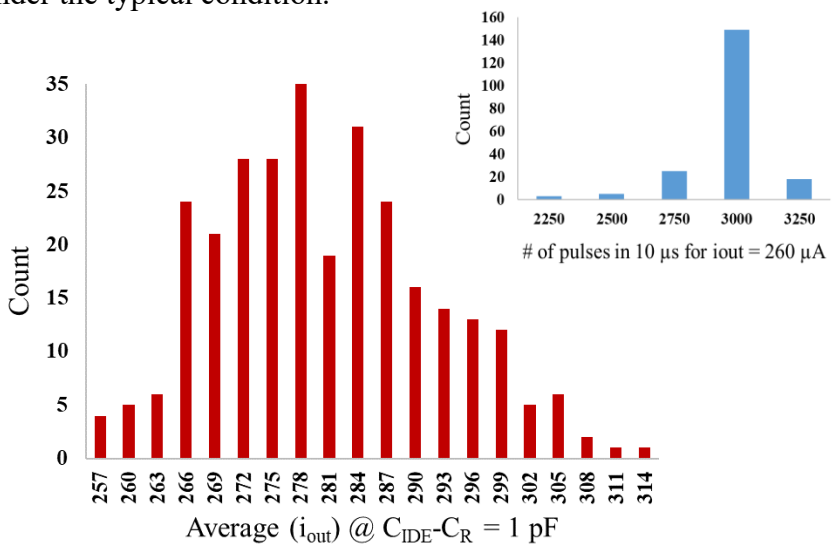


Figure 2.23: Monte Carlo simulation results including 200 points. For CIDE-CR=1 pF where the linearity of the transfer function is still more than 99%, $\overline{i_{out}}$ varies between 256.7 µA and 314.4 µA with an average equal to 284.3 µA and a standard deviation of 12.52 µA. The effect of mismatch on the maximum oscillation frequency is given with the histogram in blue. The oscillator is significantly more resilient to mismatch as 148 runs show no variation from the nominal value.

2.4.6.2 Corner Analysis

The summary of simulation results of fast and slow process variation and temperature corners for the ECBCM block are shown in Table 2.3.

Table 2.3: Summary of Corner simulations

Process Corners	Temperature Corners (^{O}C)	$\overline{i_{out}}$ for C_{IDE}-C_R = 1 pF (µA)	# of pulses in 10 µs for $\overline{i_{out}}$=260 µA
Fast	0	375.6	3928
	27	355.1	
	100	351.7	
Slow	0	202.8	2106
	27	200	
	100	195.8	

2.4.7 Discussion on the Effect of Randomness on Sensitivity

According to the mismatch analysis, in the worst-case scenario, $\overline{i_{out}}$ can vary by about ±10% (as shown in Figure 2.23, $\overline{i_{out}}$ can vary from 256.7 µA to 314.4 µA because of mismatch). The effect of mismatch on the maximum oscillation frequency is given with the histogram in blue. The oscillator is significantly more resilient to mismatch as 148 runs show no variation from the nominal value. Thus, the overall change in the sensitivity can be approximated to vary by ±10% which translates to ±0.24 pulses/fF. The worst-case scenario of the change due to the corners is from high temperature with the slow corner (195.8 µA, 2106 pulses) to low temperature and fast corner (375.6 µA, 3928 pulses). This constitutes about ± 31% variation in the $\overline{i_{out}}$ and about ±30% variation in the maximum frequency of oscillation. As a result, the whole variation due to the corners is expected to be ±61% which translates to ±1.46 pulses/fF.

2.4.8 The Effect of the Sweep of CR on iout Curves in Fully Capacitive Mode

The peak and average of the needle-shaped current waveform of the reference side, iR, increases when CR is swept from its minimum to its maximum value. From 2-12, iout is a function of CR as well as CIDE. Thus, for a given iIDE, an increase in iR decreases the differential current (iIDE – iR) resulting in a negative slope curve of iout with respect to CR as illustrated in simulation results in Figure 2.24. In Figure 2.24, three different values are assumed for $\Delta C(t)$. $\Delta C(t)$=200 fF represents a small amount of remnant. $\Delta C(t)$=700 fF denotes medium residuals and $\Delta C(t)$=1200 fF mimics a sample that creates a high amount of sedimentation. Figure 2.24 demonstrates that the average current entering the oscillator

linearly drops when CR grows for a given CIDE. It is noteworthy to mention that the bank of capacitors can create CRMin < CR < CRMAX with a step change of CRSTEP. The linearity of the ECBCM circuit with the transfer function given in 2-12 for CR < CIDE < CR + CRSTEP is crucial for the linearity of the sensor and its whole dynamic range. In other words, the resolution of the bank of capacitors should be such that the read-out circuit remains linear when the change of measurand capacitance is between two consecutive values of the reference capacitance. On another side, the minimum detectable differential capacitance, (CIDE - CR) determines the applicability of the sensor for different bio/chemical applications. In our design, ECBCM circuit's output remains linear based on the post-layout simulations shown in Figure 2.24 for the programmable bank of capacitors that can create capacitance values between 10 fF to1.27 pF with a step change of 10. Therefore, the maximum "offset capacitance", ΔCMax, is 1.27 pF which can be compensated in our design.

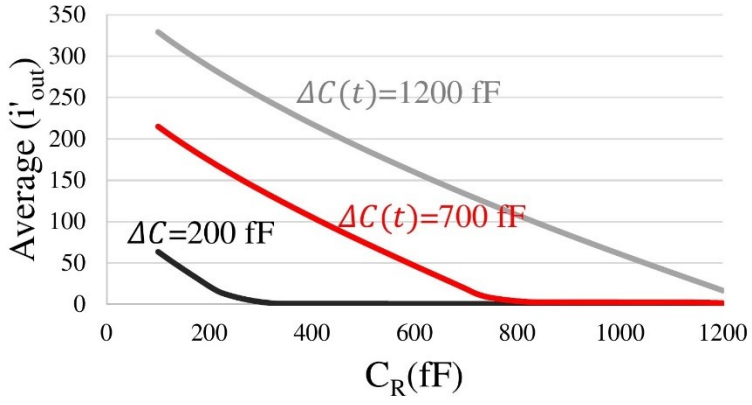


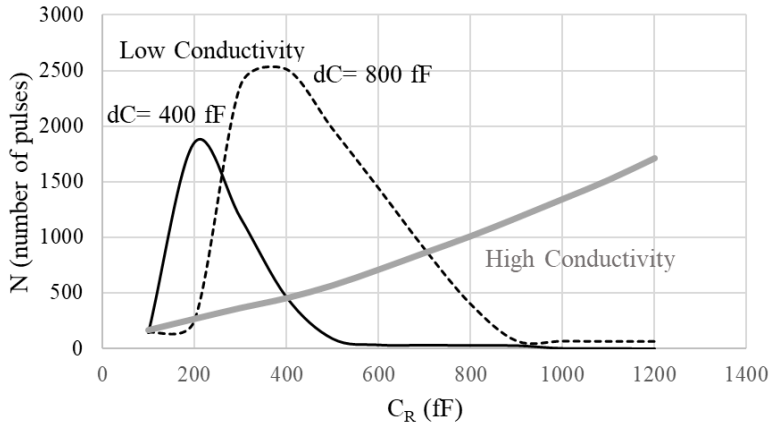
Figure 2.24: CR sweep curves for the average of i'out (the output current of the ECBCM block) for various amounts of remnants (ΔC(t)).

2.4.9 Patterns of Sensor Output Curves and the Calibration Scheme

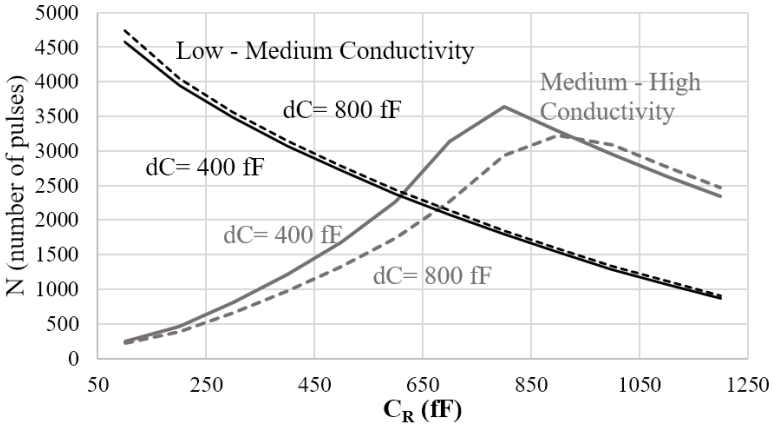
As shown in 2.4.8 , by reading the output of the circuit at each reference value, a 2D curve with the value of reference capacitance at the x-axis can be created. This curve can also reveal the conductivity of the solution medium and the value of total capacitance.

Considering the solution conductivity, inversely related to Rsol, and concerning the oscillation threshold as discussed in Section 2.4.4, four different types of curves are created. When the conductivity of the solution is high, the output curve becomes a straight line as shown in gray in Figure 2.25 (a). This pattern corresponds to the type of curves demonstrated in blue in Figure 2.20 (c). The reason for the creation of this pattern is that during the CR sweep, for each step increase, the iout curves slightly shift to the right, leaving a larger area under the oscillation threshold. This in turn means a greater number of pulses at the output. On the contrary, with a low-conductivity solution, where the capacitive behavior is dominant, curve patterns are like the ones shown in black in Figure 2.25 (a). From Figure 2.25 (a), the change in dC results in a shift in the point where the peak happens (horizontal axis value). Besides, when the conductivity of the solution is medium to high, the curves will be like the ones shown in gray in Figure 2.25 (b). The reason is that iout waveforms, shown in dotted yellow lines in Figure 2.20 (c), shift down as a result of an increase in the CR. Two curves with dC = 400 and 800 fF are shown that the CR value in which the curve peaks is shifted. Finally, when the value of conductivity is low to medium, the output waveforms become like the curves shown in black in Figure 2.25 (b) since only a portion of the iout waveform stays under the oscillating threshold. In this mode, an increase in CR shifts the whole curve down as demonstrated for dCs ranging from 400 fF to 800 fF. These curves, therefore, can serve as a measurement scheme, as explained. Another measurement scheme can be considered by using the curves obtained from the sweep method (see Figure 2.25 (a) and (b)) to choose a fixed value of reference capacitance. For various applications, such as biological cell culture, this is more suitable since the sensor tracks the changes in cell attachment on the surface of the chip. Therefore, one can cancel the effect of offset capacitance at the beginning of the sensing procedure and throughout the experiment. The scheme for finding the value of reference capacitance through calibration procedure takes

all the four regions discussed above into account and includes the following steps. 1- Obtain the output curve by sweeping the CR; 2- Detect the CR for which the output curve peaks; 3- Fix the CR to the detected value; 4- Monitor the changes in the number of pulses with the fixed CR.



(A)



(B)

Figure 2.25: Simulation results showing the output patterns of the sensor with respect to different measurement capacitance and solution conductivities: (a) High-conductivity solution (Rsol < 200 kΩ) in gray and low-conductivity solution (Rsol > 10 MΩ) in black, (b) Output trend for low to medium conductivity (1 MΩ < Rsol < 10 MΩ) in black and, medium to high conductivity (200 kΩ < Rsol < 1 MΩ) in gray.

Thus, scanning CR can be repeated multiple times during the experiment to observe any change in the value of ΔC because of remnants or Rsol due to a possible change in ions' concentration.

2.4.10 Fabrication and Measurement Test Bench

2.4.10.1 Chip and the printed circuit board (PCB)

Table 2.2 reveals the sizing of the devices and the corresponding equation numbers for obtaining the size. A die micrograph of the chip is demonstrated in Figure 2.26. This chip occupies 2 mm × 1 mm. We have implemented two IDEs, 220 μm × 110 μm with 10 fingers, electrode width, and pitch of 10 μm, with two identical interface circuits. After receiving the chips, all chips have been partially encapsulated using hysol epoxy resin to cover the pads and bond wires (Figure 2.27 (b) and (c)).

To practically utilize the chip, a dedicated test bench including both hardware (see Figure 2.27 (a)) and software (see Figure 2.28) has been developed. The chip requires two sets of supply voltages for digital and analog parts and a reference voltage. The supply voltages are fed through Texas instruments low dropout voltage regulators TPS75901KTTR with adjusting the output to 3.3 V. Considering that we have separated the left and right circuits, four voltage regulators in total were used. The CCO requires a 1.85 V reference that has been supplied through the NCP705MTADJTCG adjustable output regulator from ON Semiconductor. Required clocking signals were generated using an Arduino DUE board, and the serial peripheral interface (SPI) port of the board was used to capture the digital output data. Detailed technical information about the test bench can be seen in Appendix II.

2.4.10.2 GUI Development

The use of a test bench without a GUI is not very practical and user-friendly. As a result, a GUI has been implemented in Python, enabling the users to configure their required set of

experiments as well as perform data visualization. Figure 2.28 illustrates a snapshot of the GUI. Users can select to capture data from right, left, or both channels and also choose to obtain curves when the reference bank of capacitor's values are swept in the whole range or measured at a single point by determining the reference point value. Furthermore, by determining the number of samples, multiple measurements will be performed at a single reference point that can be averaged for better noise immunity. Users can set the GUI to obtain as many curves as desired or set the time-based measurement settings for the time interval of data acquisition and the experiment time.

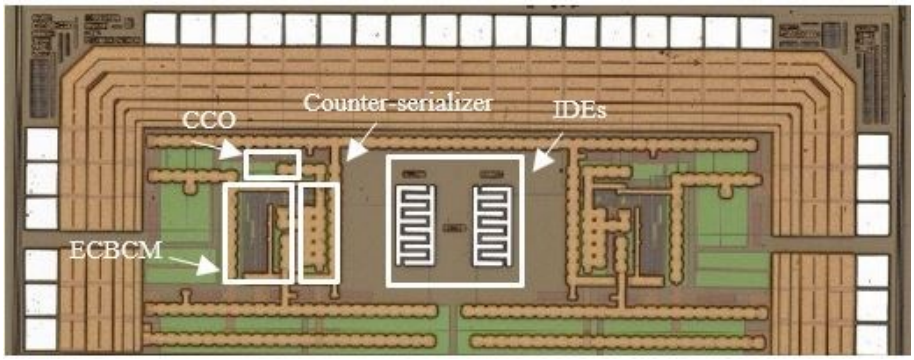


Figure 2.26: Die micrograph

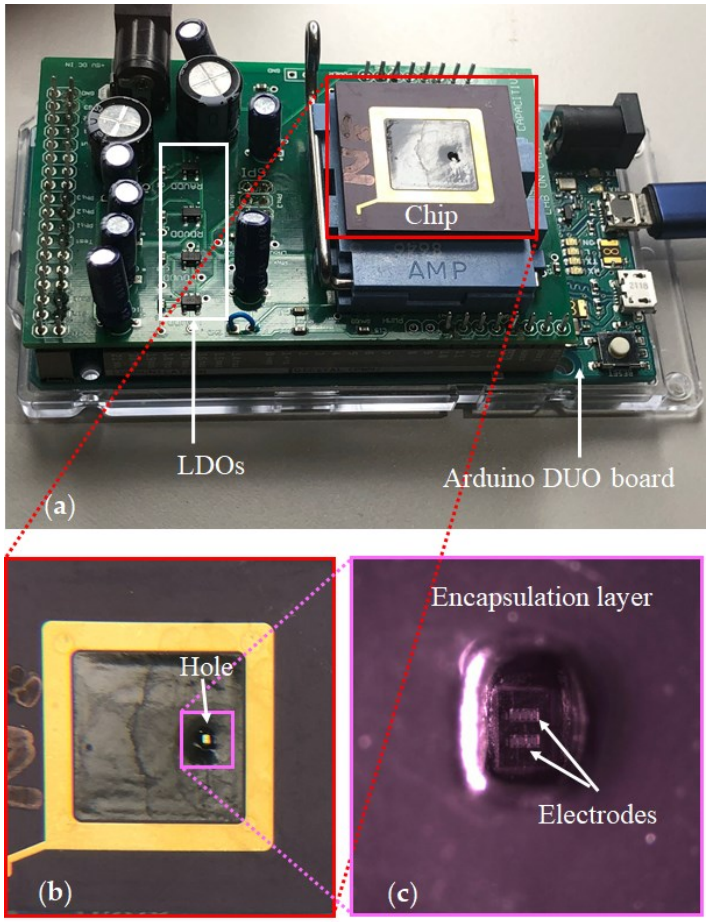


Figure 2.27: (a) An Arduino DUE microcontroller board together with a custom-made electronic board holding the chip, (b) The chip, (c) The microscopic image of the two electrodes and the surrounding encapsulation layer with a hole for the non-passivated sensing electrodes

The visualized data is a 3D curve with the chip's output (number of pulses) on the z-axis, the values of the reference capacitance on the x-axis, and time on the y-axis that has been explained in detail in Section 2.5.3. The GUI also extracts the value of capacitance from the captured data, explained in detail in Section 4.4. Snapshots of the visualized 3D data for both the right and left channels are shown in Figure 2.29 (a) and (b), respectively.

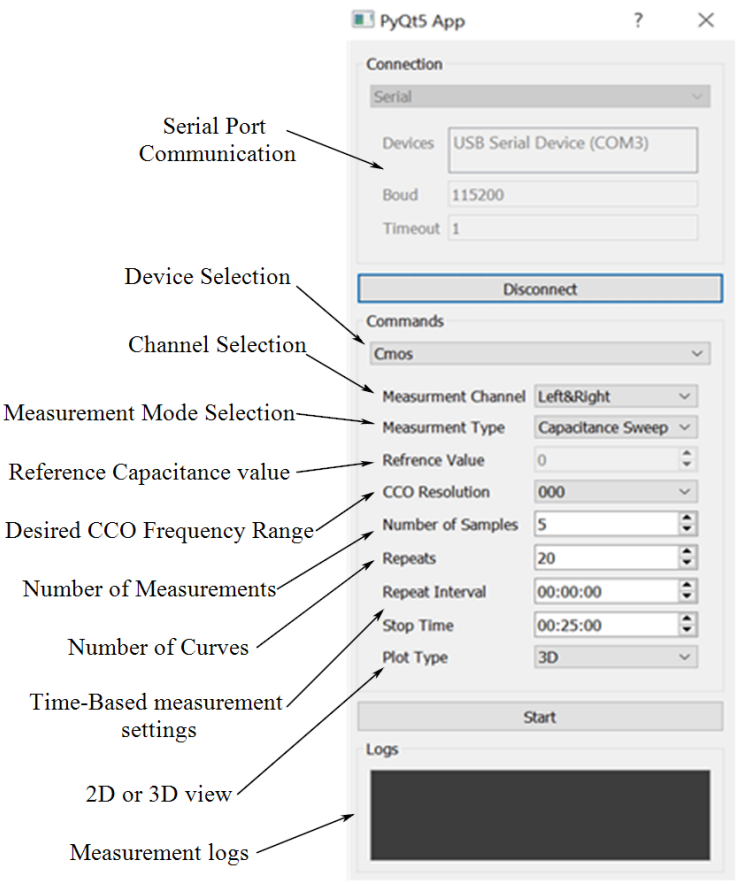
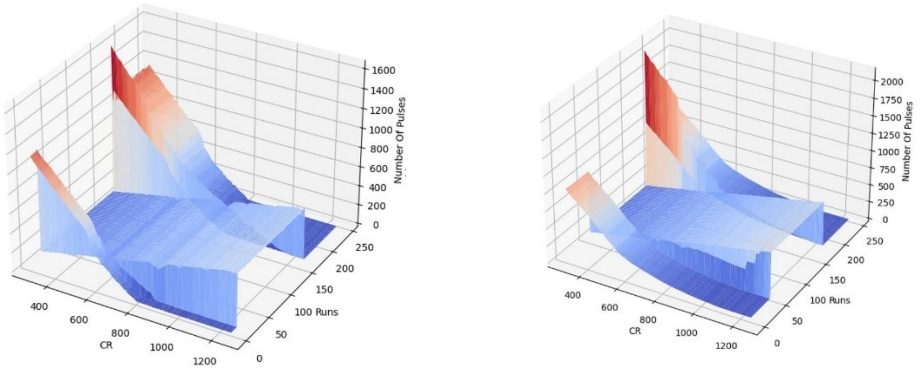


Figure 2.28: A snapshot of the GUI.



(**A**) (**B**)

Figure 2.29: The visualized data captured by the GUI in real-time: (a) for the left IDE, (b) for the right IDE.

The real-time visualization and signal processing capability that the GUI provides enables monitoring of the experiment and detection of the time that the sample has been introduced as well as the time that the sample evaporates, as discussed in detail in Chapter 4 and 5. Figure 2.30 illustrates the flowchart of the operation of the GUI that communicates with the microcontroller (Arduino DUE board).

After a serial communication channel has been established between the GUI and the microcontroller unit (MCU), the GUI converts the user input settings to four different types of commands, namely the number of samples, and the value of the reference capacitance, and the channel of interest. If writing the commands were successful, the GUI initiates the measurement command. After receiving this command, the MCU transmits the measurement data through the SPI port to the GUI.

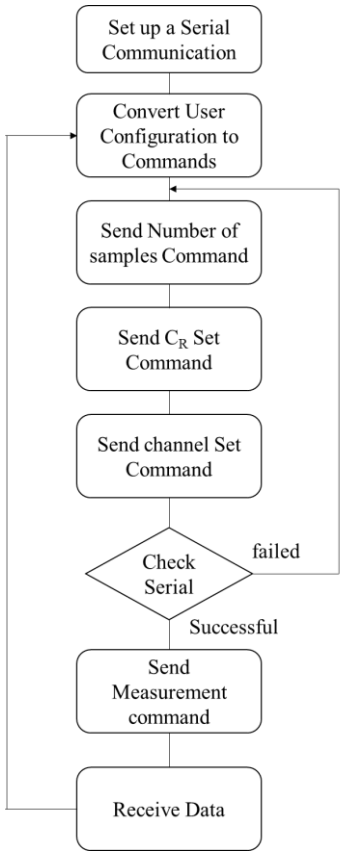


Figure 2.30: The flowchart of the GUI data acquisition from the Microcontroller: After a serial connection is set up between the GUI and the microcontroller, the user can input all the settings shown in Figure 2.28. The GUI generates three commands based on the user settings and sends them to the microcontroller. Then, the serial port is checked again before establishing the measurement command on the serial port. Next, the data is received from the chip and read from the microcontroller's SPI port buffer.

2.4.11 Consistency Test of the Fabricated Chips and the Repeatability

In total, five chips have been fabricated using the AMS 0.35 µm technology. All the chips have passed the functionality test. The output curves in a scan mode without any

sample on the chips are obtained. All the obtained curves showed the pattern expected for a capacitive model with infinite resistance due to the absence of the solution (Figure 2.25 (a) for low conductivity patterns). Figure 2.31 demonstrates the distribution of the peak of the curves for all 10 runs. Each characterization has been repeated 10 times to test the repeatability of the set-up. The difference between the number of pulses is only 1 at the peak because of overall noise.

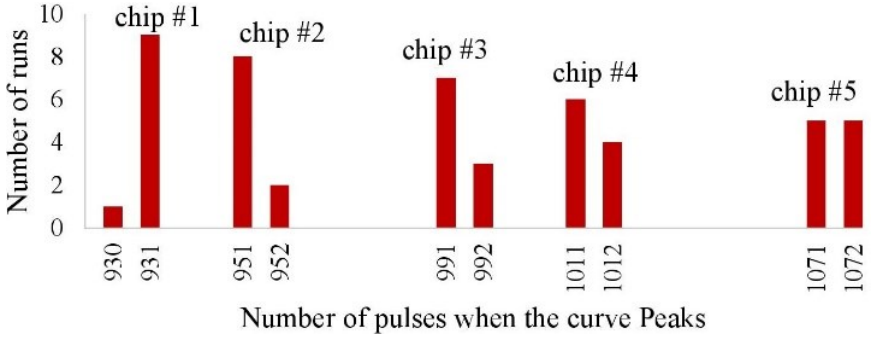


Figure 2.31: The summary of chip characterization shows a variation among the 5 received chips. Each characterization has been repeated 10 times to see the repeatability of the experiments. The difference between the number of pulses is only 1 which is a result of noise.

2.5 Calibration-free Capacitance Measurement Technique

The effect of environmental factors, systematic errors, parasitic effects, and experiment-time offset change caused by the remnants of biological and chemical samples are among the main challenges of CMOS biosensors that can diminish the accuracy of obtained results [69]. Calibration helps to decrease the inaccuracy in the assessment of the desired sensing parameter. In the multimodal sensor, reported in [12], a current digital-to-analog converter (DAC) calibration unit is embedded in the stimulation units to compensate the effect of parasitic capacitance on the output. In [4], a CFC sensor is reported that utilizes a calibration curve obtained by a distance measurement platform to model the capacitance variations and readout calibration. In the so-called sensors, calibration circuitry has significantly increased the footprint and the complexity of measurement.

In CBCM methods non-idealities like the mismatches between the sensing and the reference channels and the deposition of biological and chemical remnants on electrodes can limit the dynamic range of the measurement by creating a large input offset. Digitally programmable current mirrors [69], [70], [74], potentiometers [69], and floating-gate transistors [15], [76] are some of the in-circuit trimming elements reported for the compensation of mismatch and offset in CBCM circuits and discussed in 2.2.2. While the offset resulting from mismatch is time-invariant and can be adjusted with calibration, sediments from biological and chemical samples can generate a significant offset during the experiment time [17], [116]. Thus, a coarse calibration of the offset capacitance based on the conditions before the exposure of the electrodes to the analyte might not cancel such an instantaneous experiment-time offset change.

We address this issue by proposing the sweeping of the value of variable reference capacitors at periodical time slots to uncover the instantaneous and gradual capacitance changes in a wide range during the experiment without calibrating the sensor. The generated 2D curves, when plotted with respect to time, form an informative 3D graph which is hypothesized to be a signature that specific ptterns the capacitive properties of the biological and chemical samples at the interface with electrodes as well as discloses the sedimentation of non-target molecules such as dead cells, etc.

2.5.1 Offset Cancellation-related Works

With reference to Figure 1.3 (a), where CStray represents the parasitic capacitance between the electrode and the underlying interconnect layers or substrate, CStanding stands for the parasitic capacitance in between the fingers of IDEs, four compensation schemes have been introduced to cancel the effect of parasitic and offset capacitances for CBCM circuits until recently.

In the first scheme, CSc1, implemented in [15], the node of the reference capacitor is left unconnected to the electrodes making the capacitance at the reference node equal to $C_R = C_{\text{Stray}}$. The disadvantage of this technique is that the standing capacitance, CStanding will not be compensated, and the IDR of the circuit will be restricted by the offset introduced by CStanding. The main reason for employing this scheme is to create smaller pixels in arrays.

The second scheme, CSc2, [66], in which the sensing IDE is replicated on the reference side, is an approach to compensate the standing capacitance. In this case, the reference electrode is either insensitive to or not in touch with the analyte. In an ideal case, where the two sides of the circuit completely match, the capacitance at the reference node will be $C_{\text{R}} = C_{\text{Stray}} + C_{\text{Standing}}$. This technique aims at compensating the time-invariant offset capacitance more precisely. However, in practice, inevitable mismatch in the devices results in compensation error. Compared to the first scheme, this technique can provide higher IDR at the expense of larger pixel sizes.

In the third scheme, CSc3, like in [69], [70], [74], the reference side has tunable current mirrors and potentiometers. In this scheme, the offset capacitances, $C_{\text{Stray}} + C_{\text{Standing}}$, can be compensated by the reference capacitor as well as the mismatch can be compensated by adjusting the gain of the current mirror on the reference side. The adjustment can replicate the effect of electrode mismatch. In this case, CR can be formulated as $C_{\text{R}} = C_{\text{Stray}} + C_{\text{Standing}} + C_{\text{os}}$, where Cos is the equivalent value of reference capacitance after proportional adjustment. The advantage of this technique is that the time-invariant offset capacitance can be compensated more precisely. However, this technique requires configuring the optimum gain of the digitally programable current mirror before each experiment and per each pixel which makes it a cumbersome technique, especially for a chip with a large array of electrodes.

In the fourth scheme, CSc4, which is employed in [9], offset capacitances are compensated without replicating the sensing structure. In this technique, an offsetting capacitor (Cos), has been implemented by interlayer dielectric capacitances and has been added to the reference node. Thus, CR can be expressed as $C_{\mathrm{R}} = C_{\mathrm{Stray}} + C_{\mathrm{os}}$. This technique is the closest to our work; however, due to a fixed value of the reference capacitor, large offset capacitance during the experiment because of sedimentation and remnant cannot be compensated. This in turn limits the IDR of the sensor.

2.5.2 Capacitive Signature

Assuming ΔC(t), a capacitance change resulting from remnants (see Section 2.3.1), stays constant over a period between t1 and t2 and t2-t1> TΦ, a reference capacitance CR can be used to cancel the effect of ΔC. Assuming the offset capacitance of an IDE, CIDE, is canceled with ΔCMin (part (1) of Figure 2.32(a)) in the first period T, iout in the ECBCM circuit will only be proportional to the change in σC(t). During the experiment, the presence of remnants on the IDE can cause extra offset capacitance, such as ΔC1 and ΔC2 as shown in parts (2) and (3) of Figure 2.32 (a). As a result, a fixed CR cannot secure the cancellation of ΔC(t) at all times of the experiment. If any of the calibration schemes described in Section 2.5.1 were used, the value of CR would be kept at ΔCMin and iout could easily reach the saturation region or leave lowered headroom for the measurement of the target sensing capacitances σC(t).

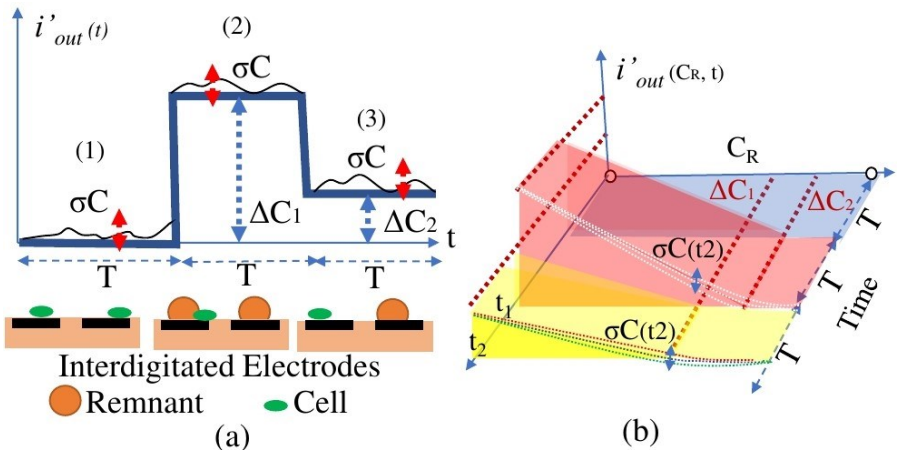


Figure 2.32: Illustrations of CBCM's output current with respect to change as a result of remnants and cells: (a) 2D, and (b) 3D signals.

This problem has been addressed by proposing a variable CR and sweeping it in its full dynamic range, ΔCMin < CR < ΔCMax, where ΔCMin and ΔCMax are the lowest and the highest capacitances that can be achieved with the implemented bank of capacitors. Sweeping the CR allows the detection of sudden and gradual capacitance changes caused by the remnants above the electrodes ΔC(t) and the attachment of target molecules σC(t). In Figure 2.32 (b), iout as a function of (CIDE-CR) and time is illustrated as a 3D representation. In analogy to Figure 2.32 (a), each plate represents a baseline regarding the value of ΔC(t). Thus, Figure 2.32 (b) is an extension of Figure 2.32 (a) with the addition of C_R axis. With consecutive acquisition of 2D curves, 3D representation of the entire time of the experiment is achieved that can uncover both ΔC(t) and σC(t) for the whole time of the experiment. This constitutes a calibration-free technique in monitoring a wide range of capacitance changes in a solution including abrupt changes due to remnants, ΔC(t), as well as gradual changes due to the interaction of target molecules with the electrode, σC(t).

2.5.3 Time-resolved 3D Signature

The output of the chip is a digital number (number of pulses) that is proportional to the input differential capacitance. Consecutive acquisition of the chip output with respect to the

full-range sweep of CR has been used as a tool for time-resolved monitoring of the samples. For this purpose, the so-called “output versus CR” 2D curves are combined with time. The result forms a 3D signature of the changes during the entire experiment period. Thus, the generated 3D specific pttern has 3 axes including CR, time, and the output of the chip (number of pulses). The experimental results demonstrated in Section 2.5.4.5 are generated utilizing this technique.

2.5.4 Experimental Results with Chemical Solvents

To observe all four types of output curves as proof for the high-dynamic range of the sensor, we conducted the test using 2 μL droplets of three different chemical solvents with known relative permittivity and conductivity, (see Table 2.4) and put them on the chip using a micropipette. In addition to that, we needed a sample with a fast dynamic so that our sensor’s response time could be examined.

2.5.4.1 Steady-state Results

Figure 2.33 shows the obtained curves for the filtered water, methanol, and propanol droplets and compares them with the simulation results. The curve in solid blue illustrates the filtered water in a steady state. Filtered water, as seen in Table 2.4 is highly conductive due to its high ionic impurities. As a result, the expected pattern of a straight line is obtained. The curve in dashed blue corresponds to the simulation result using the model given in section 2.3.1 with Rsol and Csol corresponding to the filtered water from Table 2.4. Curves in gray are for methanol with relative permittivity of 30 and conductivity of 0.3 mS/cm (equal to 24.8 fF and 350 kΩ) which puts the solution in the medium to the high conductivity range. Therefore, the expected pattern is like the type shown in gray in Figure 2.25 (b).

Propanol on the other hand falls under the category of low to medium conductivity with a pattern like the curves shown in black in Figure 2.25 (b) and depicted in red in Figure 2.33. In all the above curves, the simulation results based on the known conductivity and permittivity of solutions agree with the experimental data.

Table 2.4: The chemical properties of the chemical solvents used.

Chemical	ε_r	C_{sol} (fF)	δ (mS/cm)	R_{sol} kΩ
Water	80.2	66.5 fF	15	7
Methanol	30	24.8 fF	0.3	350
Propanol	20.1	16.7 fF	0.1	1000

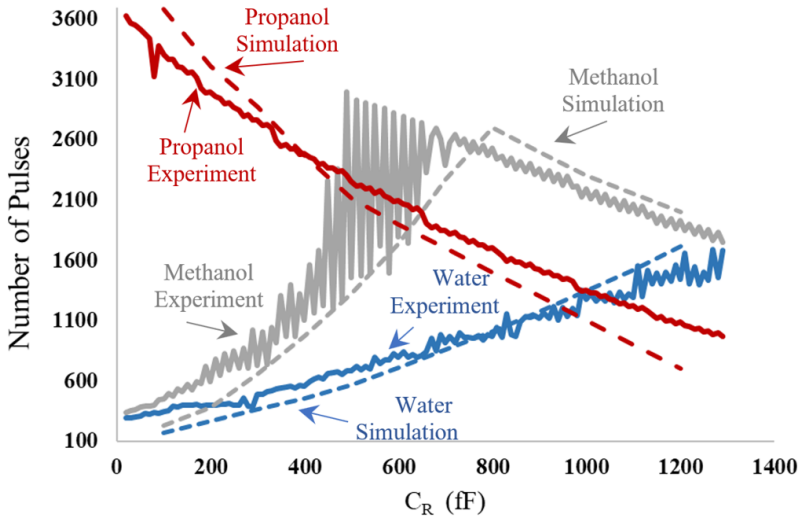


Figure 2.33: Experimental results and the simulation curves for the steady state of the droplet test using filtered water (Blue) Methanol (Gray), and Propanol (Red).

2.5.4.2 Fully Capacitive Experiment

Another experiment validates the dynamic range of dC change in the fully capacitive mode. Before testing the chip with droplets, the output curve was obtained for both left and right-side IDEs as shown in Figure 2.34. Since there is no sample on the IDE, the curve corresponds to the very high R and the capacitance change is dominant. Another curve is obtained after the complete evaporation of the filtered water droplet and the solidification of salty remnants, (see Figure 2.35 (a) for a 3D microscopic image of the remnants in two different runs of the experiment). The drift in the curves of the left IDE on which major

remnants have been deposited reveals a 470 fF capacitance change by calibrating the CR to 400 fF (200 pulses) that results in the highest sensitivity (see Section. 2.3.7).

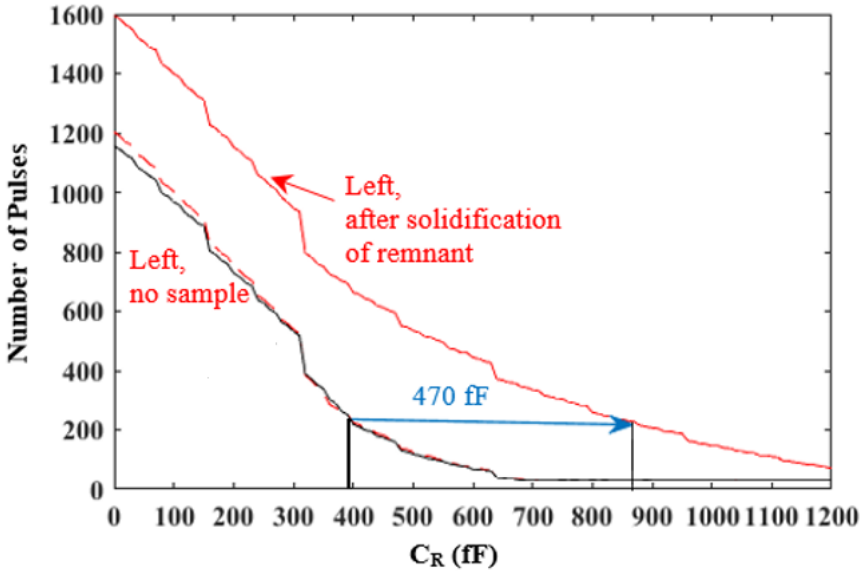
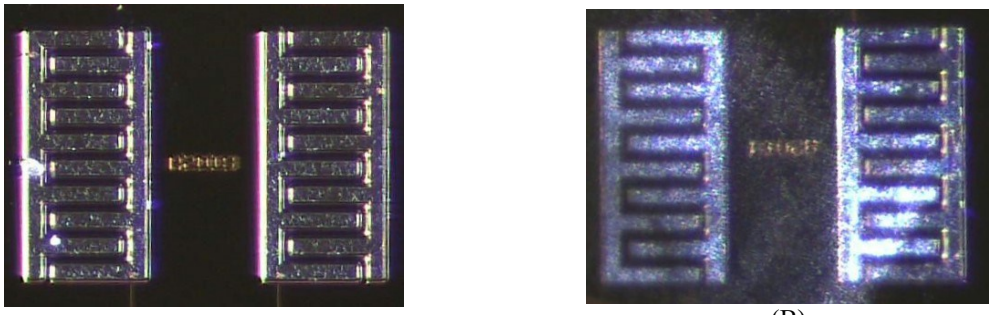


Figure 2.34: The proposed sensor's output at the onset of introducing the filtered water droplet and after complete evaporation and solidification of salty remnants.



(A) (B)

Figure 2.35: (a) Microscopic image of the electrodes before being exposed to any sample, (b) The electrodes after filtered water droplet evaporation test. This figure shows a layer of deposited material on the electrode mainly composed of salt.

2.5.4.3 Time-resolved Water Experiment with Transition Curves

Figure 2.16 illustrates the main patterns observed in the filtered water experiment. We have hypothesized that these curves are generated because of a change in the equivalent electric model of the interface during the evaporation of filtered water. "A" represents the no-sample situation and "B" captured shortly after introducing the filtered water complies

with the low conductivity and low-to-medium conductivity, respectively (see Figure 2.25). As the droplet settles on the electrode, the conductivity of filtered water, because of the presence of ions, dominates the capacitance in the parallel equivalent circuit model (see Figure 1.3 (b)) and creates curve "C" that follows the medium-to-high conductivity pattern shown in Figure 2.25. Simulation results show that after adding the conductivity of the solution to the model iIDE curve will not necessarily remain needle-shaped. Instead, the shape can vary depending on the sample's conductivity. As a result, the waveform shape of $i_{IDE} - i_R$ that forms i'out also depends on the conductivity of the sample, shown in Figure 2.20. Meanwhile, I_{max}, the upper bound of the CCO (see Section 2.4.4) introduces a truncation line for i'out curves. Any input current above IMAX will not result in oscillation. Solution conductivity for our sensing system can be categorized as "low", "low to medium", "medium to high" and "high", (see Table 2.5), conductivity solutions that are briefly explained here. When the conductivity of the solution is low or low to medium, the capacitive behaviour is dominant and i'out patterns are not truncated with the IMAX. On the other hand, when the conductivity of the solution is medium to high, the curves expand upwards where a portion of curves are truncated, as shown in Figure 2.37.

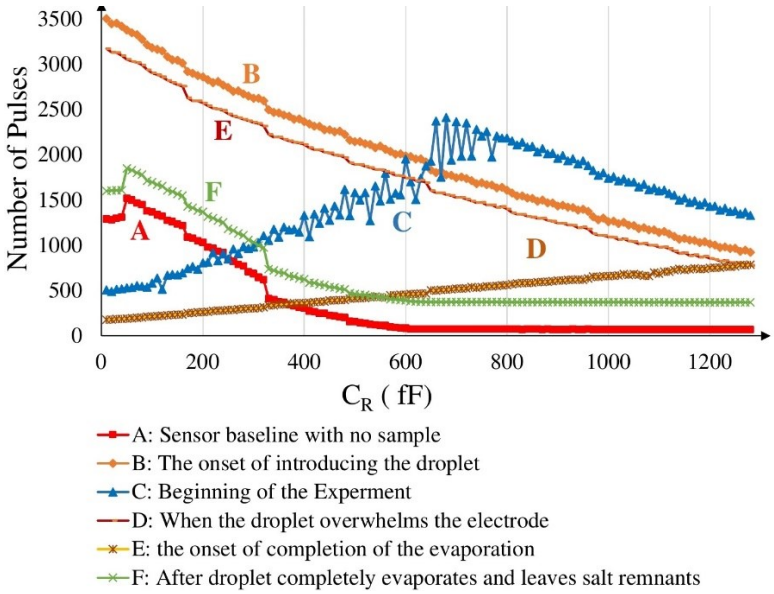


Figure 2.36: All four types of curves observed for evaporating droplet experiment with filtered water.

Table 2.5: Sample solution and affected design parameters

Design Parameter	Range			
R_{sol}	R_{sol} < 200 kΩ High Conductivity	200 kΩ <R_{sol} < 1 MΩ Medium to High Conductivity	1 MΩ <R_{sol} < 10 MΩ Low to Medium Conductivity	10 MΩ <R_{sol} Low Conductivity
C_{sol}	500 aF to 1.27 pF			
I_{MAX}	280 µA			
C_R	10 fF to 1.27 pF with a step of 10 fF			

In this mode, the curves shift down because of an increase in the CR. When the conductivity of the solution is high, all the curves are truncated by IMAX, (see Figure 2.38). The reason is that during the CR sweep, for each step increase, the i'out curves slightly shift to the right, leaving a larger area under the oscillation threshold. This means a greater number of pulses at the output as CR increases. In Figure 2.36, "F" is the curve that shows the output of the sensor after the complete evaporation of the droplet. Comparing Figure 2.35 (a) to Figure 2.35 (b), there is a significant amount of salt remnants on the electrode and the difference in the amplitude of "A" and "F" corresponds to the capacitance increase due to this remnant in the dry phase.

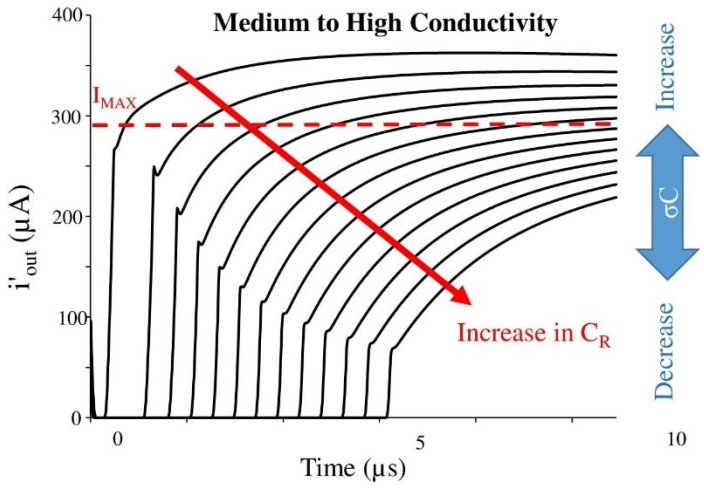


Figure 2.37: i'out curves in a medium to high conductivity solution for different CR values and the IMAX truncation line.

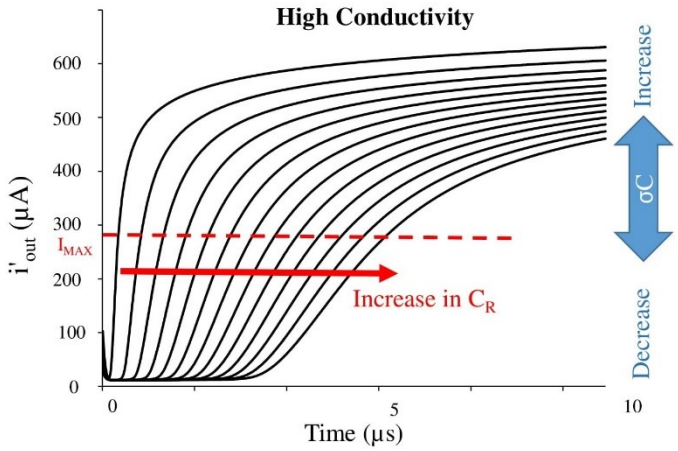


Figure 2.38: i'out curves in a high conductivity solution for different CR values and the IMAX truncation line.

2.5.4.4 Measurement Speed Test

To evaluate the measurement speed of the sensor, we repeated the filtered water droplet test by keeping track of the time and repeating the full CR sweep. The full-range CR sweep creates 128 reference capacitance values from 10 fF to 1.27 pF with a step of 10 fF. Each measurement completes in 15 µs, which in total takes 2 ms for a complete sweep and to obtain the curve. Our GUI receives the data after every sweep for real-time visualization. This data transfer from the MCU to GUI added overhead of about 1 s for serial communication. Our system was able to show the curve every second which proves the expected speed discussed in Section 2.4.1. For the application where real-time visualization is not required, the data can be buffered at the MCU to avoid serial communication overhead time. Table 2.6 compares this work to the previous state-of-the-art sensors. This work brings about the possibility of a wider IDR of multiple times higher compared to relative works while maintaining an acceptable sub-femto Farad measurement resolution for life science applications. It also offers the advantage of a significant input offset dynamic range adjustment for offset cancellation. Furthermore, because of the high measurement speed, our sensor is suitable for applications with rapidly changing dynamics. On the other hand,

the ECBCM-based chip consumes higher power than the typical CBCM which can be considered as the cost of this topology.

2.5.4.5 3D Specific pattern of Chemical Solvents

To test the capability of our sensor in generating 3D specific patterns of samples, 2 µL droplets of three different chemical solvents, with different conductivities and resistivities are introduced to the on-chip IDEs and the 3D specific pattern is captured in the time frame of 5 seconds before putting the sample until complete evaporation of the droplets at the room temperature. Complete evaporation of the samples allows the formation of salty crystals and sedimentation on the electrodes that in turn allows us to see the effect of attached material in addition to monitoring the liquid phase. Figure 2.39 illustrates the 3D specific pattern created for a 2 µL droplet of propanol (dielectric constant (ε_r)=20.1, conductivity (δ)=0.1 mS/cm). The baseline represents the total offset capacitance of the electrode without the effect of the sample on it. At the onset of introducing the sample, a significant capacitance change is observed which shows the equivalent capacitance due to the sample which has not yet contacted the electrodes. During the experiment, a gradual increase in capacitance is recorded. At time=90 s, a sudden increase in the capacitance is captured which can be due to a solid salt particle passing on top of the electrode. The pattern in this specific pattern is aligned with what is discussed in Section 2.4.9. The signature shows that the capacitance of the droplet slightly increases during the experiment and then falls at the onset of complete evaporation close to the baseline when there was no sample. It also shows that rapid changes can be detected such as the bump-shaped pattern captured around 90 s after the start of the experiment. A mathematical model for the impedance of an evaporating droplet, given in [56], suggests that the increase in capacitance happens as a result of the evaporation of the droplet. In this model, a parallel combination of geometrical capacitance, Cgeo, and double-

layer capacitance, Cdl, forms a total capacitance that might increase during evaporation because of the increase in double-layer capacitance.

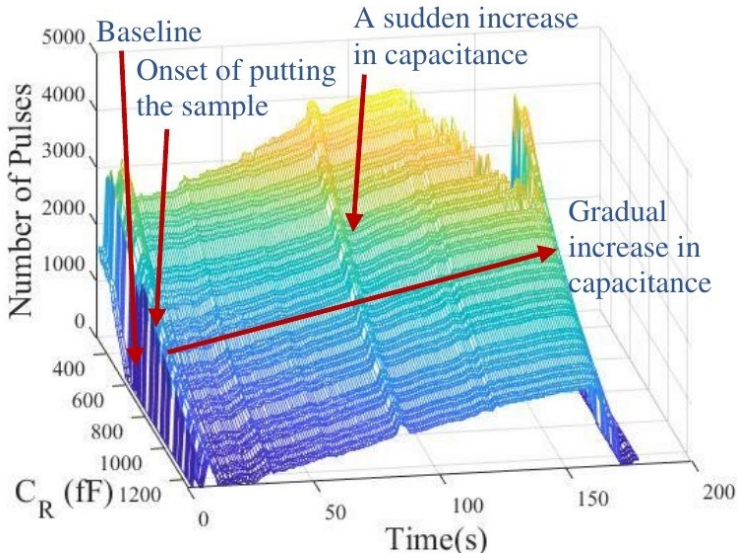


Figure 2.39: 3D signature for evaporating droplet experiment with a 2µL of propanol.

Another test is performed using a droplet of methanol which has a higher dielectric property and slightly higher conductivity (ε_r=30, δ=0.3 mS/cm). The result is shown in Figure 2.40. The specific pattern starts with a baseline and demonstrates the same sudden increase of capacitance as seen in Figure 2.36. The difference is in the value of output which is higher for methanol compared to propanol due to its higher dielectric property. At about time=100 s, the curves change their pattern and show higher capacitance until the end of the experiment when the droplet completely dries. When the sample dries, the curves do not return to the baseline, unlike the propanol test. This part is a result of the significant sedimentation of salty crystals that existed in the initial sample. The third experiment has been performed using filtered water (ε_r= 80.2, δ=15 mS/cm) and the results are demonstrated in Figure 2.41. In comparison to what is observed in the propanol and methanol specific patterns, the test using filtered water demonstrates a similar baseline with different patterns of curves. These patterns have roots in the discussed maximum input current limit I_{max} above which the CCO stops oscillating.

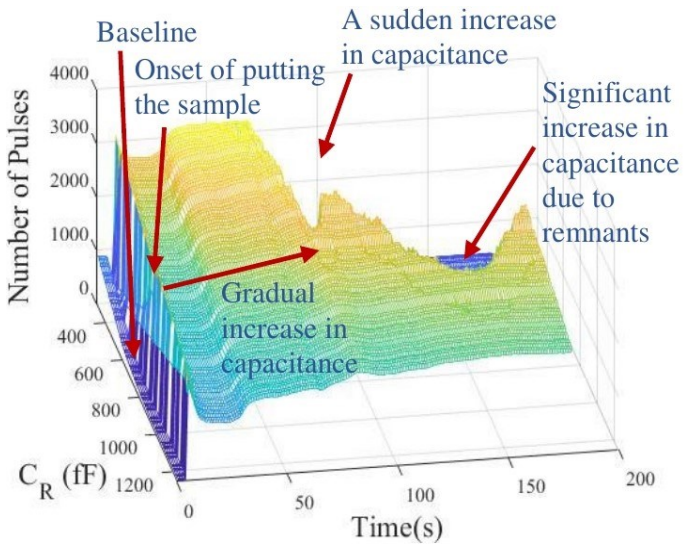


Figure 2.40: 3D signature for evaporating droplet experiment with a 2 µL of methanol.

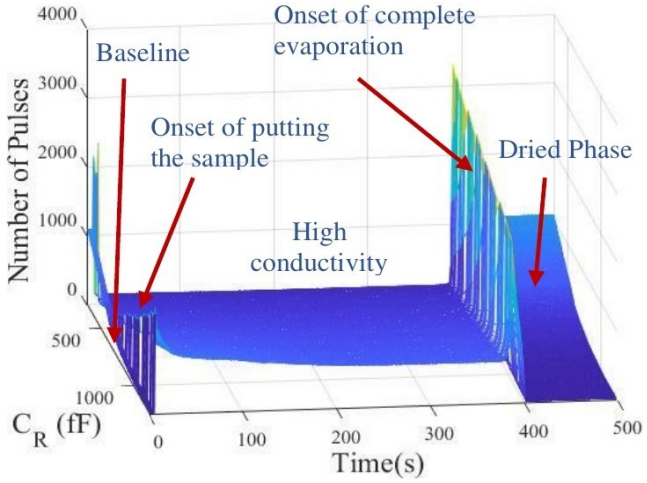


Figure 2.41: 3D signature for evaporating droplet experiment with a 2 µL of filtered water.

2.6 Chapter Summary

A novel capacitance sensor based on a hybrid topology of ECBCM circuit and oscillator was introduced. The proposed ECBCM circuit offers the advantage of a wider IDR of about 400 fF based on post-layout simulation results for a given reference capacitance value. The minimum detectable change in the differential capacitance of 416 aF was achieved which is typically enough for the detection of a wide range of cells and molecules. The sensor is among the fastest in the literature with only a 15 µs measurement time. In addition, by replacing the reference IDE with a programmable bank of on-chip capacitors and sweeping

the value of reference capacitance in its full dynamic range, the novel calibration-free 3D time-resolved specific pattern was created. The experimental results with a 2 μL droplet of chemicals showed an agreement with the simulation results. Furthermore, they revealed that the abrupt and gradual change of capacitance due to sample-electrode interactions can be captured in the 3D time-resolved specific pattern. The proposed capacitive sensing method can, therefore, be employed to measure small capacitive changes in a liquid condition with various sources of large offset capacitances as well as detect the remnants in the dried condition.

Table 2.6: Comparison of this work with the state-of-the-art

Ref	Circuit Topology	Electrode Dimension	IDR	Input Offset Dynamic Range	Measurement Time	Resolution	Passivation Layer	Digital Output	Supply Voltage (V) Technology (µm)	Power Consumption	Calibration technique	The elements/ models/ methods used for calibration
[3]	DC2DV–IDE on CBCM + ∑Δ	50 µm × 50 µm IDE	6 fF	A[5] 6 fF	50 ms	10 aF	Natural CMOS	8-bit	3.3 / 0.35	700 µW	In Hardware	Current mirrors with programmable gain
[4]	C2F–IDE	30 µm × 30 µm IDE	1 fF	NA[6]	1.5 s	14.4 aF	Natural CMOS	12-bit Digital	3.3 / 0.35	8 mW	In Software	Calibration curve (f-C) obtained by distance measurement platform
[17]	C2V[3]–IDE	14 µm × 16 µm IDE	57 fF	NA	20 µs	450 aF	Al_2O_3	NO / (Voltage)	3.3 / 0.35	29 µW	In-circuit trimming	Reference voltage and large on-chip capacitance
[70]	DC2DV – IDE on CBCM + ∑Δ	1000 µm × 200 µm	7 fF	A 7 fF	10 ms	110 aF	Natural CMOS	6-bit	1.8 / 0.18	126µW	In Hardware	Current mirrors with programmable gain
[68]	C2F[1]–IDE	200 µm × 230 µm IDE	10 pF	NA	20 min	10 fF	Al_2O_3	NO / (output of Oscillator)	0.3-2.5 / 0.25	29 mW	In Software	Comparison with a no sample baseline
[15]	DC2DV[2] – IDE on CBCM	30 µm × 30 µm IDE	±25 fF	NA	1 ms	15 aF	Natural CMOS	NO / (Voltage)	3 / 0.5	165 µW	In-circuit trimming	impact-ionized channel hot electron injection
[117]	C2F–IDE	N/A	350 pF	NA	Max 750 µs	85 fF	N/A	16 bits Digital	±0.9 / 0.18	162 µW	In hardware	Switch Capacitor
[118]	C2V	40 µm × 40 µm	N/A	NA	1.1 s @ 1kHz	N/A	Au	NO / (Voltage)	3.3 V	85 mW	In Software	Comparison with a no sample baseline
[119]	C2V–IDE	Off-chip IDE	27 pF	NA	30 µs	10 fF	Si_3N_4	NO / (Voltage)	1.8 / 0.18	11.772 mW	In Software	Comparison with a no sample baseline
[90]	DC2V–IDE	Customized coplanar device	1.5 pF	NA	100 ms	800 aF	-	NO / (Voltage)	-	Not Reported	In-circuit trimming	Variable capacitor/ Calibration curve (*f-C*)
This Work	DCDC2F[4]–IDE	220 µm × 110 µm IDE	> 400 fF	A 1.27 pF	15 µs	416 aF	Al_2O_3	12-bit Digital	3.3 / 0.35	29.91 mW	N/A	Calibration Free

[1] C2F: Capacitance-to-frequency, [2] DC2DV: Differential Capacitance-to-Differential Voltage, [3] C2V: Capacitance-to-Voltage, [4] DC2DC2F: Differential Capacitance -to-Differential-Current -to-Frequency, [5] Adjustable, [6] Not Adjustable

Chapter 3: A High Dynamic Range 16×16 Capacitive Sensor Array

This chapter proposes a circuit and system for high throughput monitoring based on the proposed high IDR and calibration-free sensor in Chapter 2. A new array topology for the CBCM family of circuits has been proposed that allows the electrodes to use a shared bus to connect to a single read-out circuit. The content of this chapter has been submitted as a paper with the same title to IEEE Transactions on Biomedical Circuits and Systems (TBioCAS) journal.

3.1 Abstract

We present a fully integrated CMOS capacitive sensor array for life science applications. This sensing device consists of an array of 16 × 16 IDEs integrated with a charge-based readout and multiplexing circuitries on the same chip. This chip was implemented in 0.35 µm AMS CMOS process. This sensing device has a wide IDR of about 100 fF and a resolution of 150 aF, and the capability of temporal, spatial, and dielectric sensing. It makes it possible to develop a low-cost, calibration-free sensing platform for life science applications. In this chapter, we demonstrate and discuss the functionality and applicability of the proposed sensing device by introducing various chemical solvents

including ethanol, methanol, and pure water. The simulation and experimental results achieved in this work have taken us one step closer to a fully automated calibration-free capacitive sensing platform for high-throughput drug development and other purposes.

3.2 Introduction

CMOS capacitive sensors have opened up new horizons for the development of integrated platforms for various applications such as DNA hybridization detection [9], drug toxicity tests [3], bacteria growth monitoring [17], virus detection [120], and detecting different cancer cells like breast cancer [81], and ovarian cancer cells [4], [121] as well as chemical solvent monitoring [75]. In these CMOS sensors, an array of electrodes is implemented on the same chip together with the interface circuit offering practical advantages such as low complexity, label-free, and high precision sensing [122]. These features have paved the way for the monolithic integration of large arrays of sensors on a single chip for high-throughput measurements. A schematic of such a system with an off-chip data acquisition and a GUI is shown in Figure 3.1.

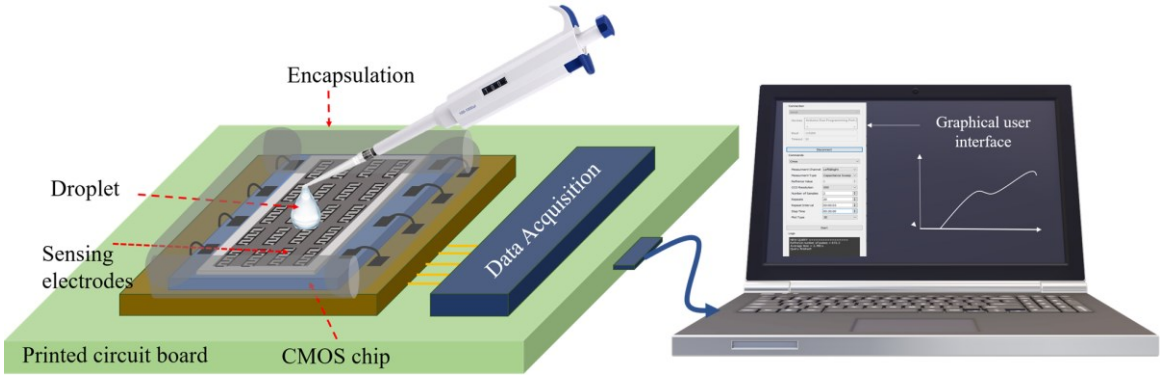


Figure 3.1: A platform including an array of capacitive sensors and an interface circuit on the same CMOS chip encapsulated for introducing biological and chemical samples, as well as a data acquisition system and GUI.

As seen in Table 3.1, in life science applications, several custom-made capacitive sensor arrays have been developed to measure from auto Farad (aF)- [3], [4], [17], [62], [74], [123],

[124] to femto Farad (fF)- [81] change in the sensing capacitance. For instance, Prakash et al. [81] reported a voltage-mode circuit using charge sharing principle for the development of an array of 28 sensors, each pixel of which consists of 8 MOSFET Transistors (MTs) but the resolution of this sensor is limited to a femto Farad range (5 fF). In [17] a 16×16 capacitive sensor array has been proposed whose pixels include 7 MTs one of which is used as a switch for selecting the pixel. They achieved a higher IDR of 57 fF and a better resolution in the range of atto Farad (about 450 aF) by using a similar principle but with one less MT in each pixel. In [4], [123], [124] a 4 × 4 array, each pixel with 9 MTs for implementing a ring oscillator, a switch, and a buffer has been demonstrated. Row/column decoders automatically activate each pixel by an on-chip control logic and the output of each ring oscillator passes through a digital buffer into a multiplexer connected to a counter. This sensor reads the capacitance changes with a resolution of 14.4 aF but with a limited IDR of 12 fF. For the calibration of this sensor, a distance measurement platform was used for modeling the capacitance changes and obtaining a calibration curve. Among the sensors using CBCM technique, an array of 6 × 6 sensors is reported in [62] each pixel of which is composed of the core of CBCM circuitry including 4 transistors as the switches. A column-parallel architecture based on a shielded current routing bus has been designed to eliminate the need for individual pixel calibration and improve immunity to noise and junction leakage. Moreover, they used floating-gate transistors for offset cancellation. A row-wise selection and a column-wise readout addressing scheme have been employed in this architecture. As mentioned in Table 3.1, this sensor can provide a resolution of 15 aF but with a limited IDR of 10 fF because it works in the voltage mode, and its output voltage is restricted by the supply voltage. In addition, our team has previously reported an array of 8 × 8 core-CBCM sensors [3], [46], [74] with only two transistors in each pixel. In this sensor, a sigma-delta modulator is adapted to CBCM technique which includes adjustable current

mirrors for mitigating the offset of the sensor. This sensor can achieve a resolution of 10 aF but in the limited IDR of 10 fF which is due to the voltage conversion employed in the middle of the readout process of the signal. Furthermore, in the array structure of this sensor, a transmission gate was inserted into the current path of each IDE to connect/disconnect it to/from the readout circuit. Considering that the CBCM sensors work based on charging and discharging of the capacitance of the electrode, this technique can introduce unwanted resistor-capacitor (RC) parasitic effects directly to the current path.

As shown in Table 3.1, several researchers have tried to achieve a high-density matrix of electrodes for high spatial resolution with a reasonable IDR. On the one hand, there is a compromise between IDR and resolution. Thus, these metrics are usually defined according to the desired application, such as cell growth monitoring which needs a high resolution [3], [46], [62], [74]. On the other hand, to achieve a high-density array, the measurement circuit should occupy a small silicon area. To this end, as shown in Table 3.1, researchers have developed various circuit topologies to minimize the circuit footprint that has to be placed under the electrodes. Obviously, the number of MTs and the employed technology can affect this issue.

Table 3.1: Comparison of different array-based capacitive sensors.

CMOS (µm)	MT[1] #	Array size	Res.[2] (aF)	IDR (fF)	Cal.[4] method	Application	Ref.
0.5	8	28	5000	NA[3]	DA[5]	CGM[8]	[5]
0.25	7	16 × 16	450	57	NA	BD[9]	[3]
0.35	9	4 × 4	14.4	12	DA	CCD[10]	[6,12,13]
0.5	4	6 × 6	15	10	ICM[6]	CG	[10]
0.35	2	8 × 8	10	10	ICM	CG/ DT[11]	[2,11]
0.35	2	16 × 16	160	100	CF[7]	DA[12]	This work

[1]MOSFET Transistor (the required multiplexing switches inside a single cell), [2]Resolution, [3]Not Available, [4]Calibration, [5]Data analysis, [6]In-circuit trimming, [7]Calibration-free, [8]Cell growth monitoring, [9]Bacteria detection, [10]Cancer cell detection, [11]Drug test, [12]Droplet analysis.

Moreover, capacitive sensors are considered non-selective sensing devices. Thus, the presence of any other non-targeted cells or molecules may change the capacitance. Therefore, in addition to the change of sensing capacitance (CS) due to the attachment of sensing cells [3], [81] or absorption of molecules [9] on the surface of these sensors, there are other non-ideal sources of capacitive changes that can be time-variant. These include the detachment and levitation of dead cells, deposition of non-targeted molecules on the surface, the evaporation of culture medium, variation of temperature, or the variation of pH resulting in so-called non-targeted capacitance changes (ΔC(t)). Therefore, the measurement of CS, in the presence of time-variant ΔC(t) requires a high-IDR capacitive sensor with proper calibration to cancel the parasitic capacitances. So, the sensing capacitance of an IDE which is mostly reported for biosensors can be expressed by equation 3-1.

$$C_{IDE} = C_{\mathrm{C}} + \Delta C(t) + \sigma C(t) \qquad 3\text{-}1$$

where σC(t) denotes time-variant target sensing capacitance change, and CC stands for all the offset and parasitic capacitances inside the chip.

As aforementioned and summarized in Table 3.1, various techniques have been used to mitigate the effects of parasitic and offset capacitances of the sensors including data analysis [81], [125] using a calibration curve as well as different types of in-circuit trimming techniques [2], [3], [62], [74] such as connecting identical electrodes along with replicated circuits to both reference and sensing nodes [66], or employing potentiometers and adjustable current mirrors [66], [69], [70], [74], or adding an offsetting capacitor to the reference node [62]. Despite great advances in developing capacitive sensors, less attention has been paid to developing high-precision calibration procedures to cancel the effect of ΔC(t) to increase IDR.

We proposed a calibration-free and wide-IDR capacitive sensor using a current-mode technique based on ECBCM technique that can address the removal of unpredictable time-

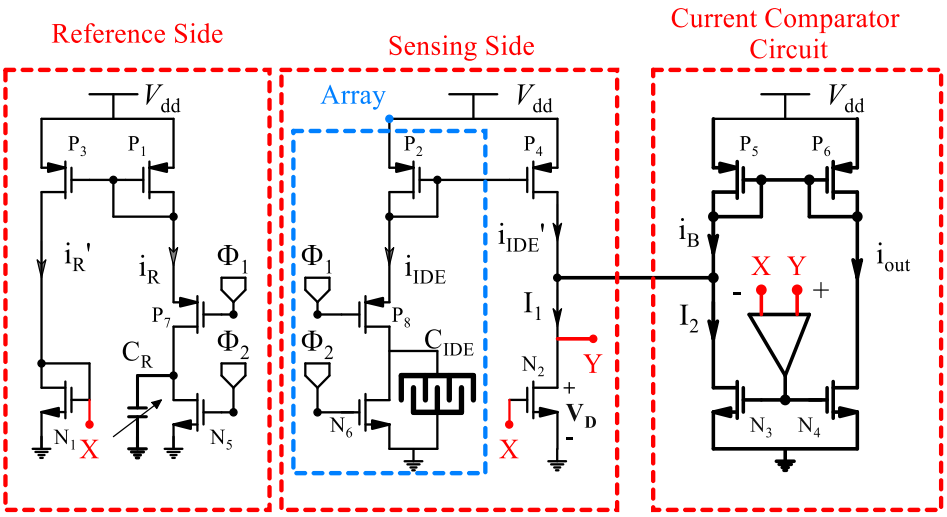
variant offset [62], [77], [78] in Chapter 2. To go further in this approach, we modified the circuitry associated with the calibration structure and ECBCM to achieve a higher resolution in this chapter. Herein, we propose a novel 16 × 16 capacitive sensor array with the advantage of being calibration-free on each single sensing electrode which can provide a wide IDR of 100 fF and a resolution of 150 aF. The obtained IDR and resolution in this capacitive sensor array can be suitable for some applications like on-chip analyses of chemical solvents and droplets. Furthermore, in this work, we propose a novel multiplexing scheme so that no extra MT switch is used for the IDEs and each pixel uses only the two transistors of the core CBCM structure (P8, and N6 in Figure 3.2 (a)).

3.3 Proposed Array-based Capacitive Sensor

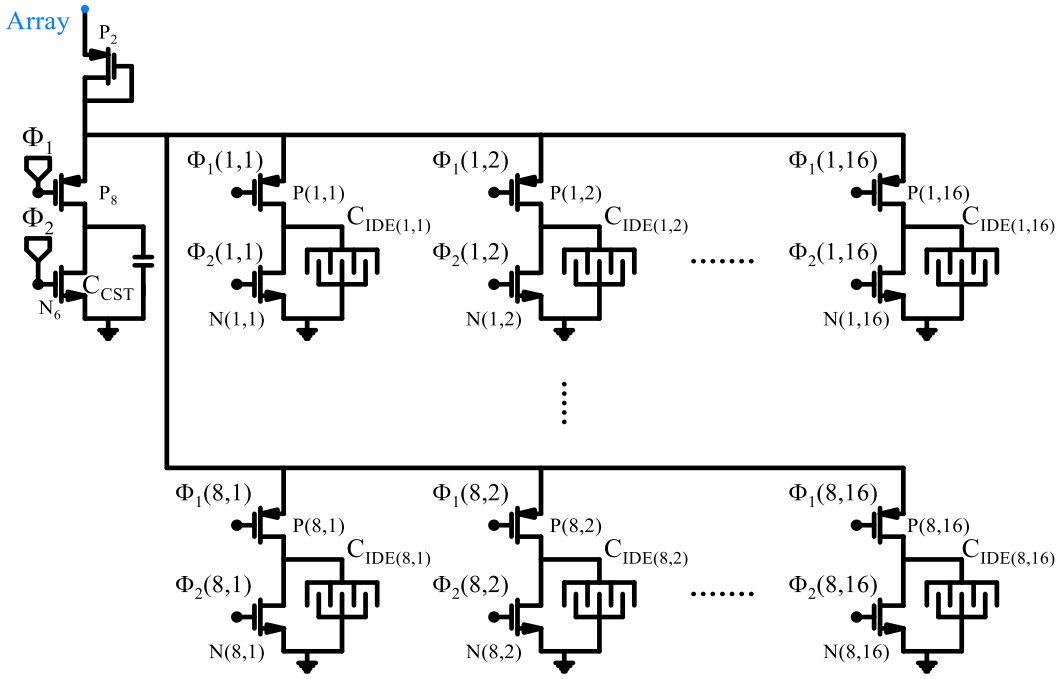
In this section, the proposed multiplexing circuitry is introduced, and the optimized ECBCM circuitry, oscillator, and bank of capacitors are discussed.

3.3.1 ECBCM Circuitry for the Array Chip

The ECBCM-Array circuit, including the ECBCM circuit and the proposed array, is shown in Figure 3.2 (a) and (b). The ECBCM circuit depicted in Figure 3.2 (a) is modified to support an array of electrodes instead of a single electrode. In Chapter 2, it has been proved that $i_{IDE} - i_R$ and $i'_{IDE} - i'_R$ are proportional to $C_{IDE} - C_R$ in CBCM technique.



(a)



(b)

Figure 3.2: (a) The ECBCM circuit topology, (b) The proposed array topology.

By increasing the gain of the feedback stabilization circuit in the ECBCM, this block acts as an intermediate block that compares the currents from the reference side and the sensing side of the circuits. The dropped voltage on node X, (VX) is a function of i_R' as seen in equation 3-2 and the voltage on node Y (VY) can be obtained from equation 3-3.

$$V_X = \sqrt{\frac{2 \times L \times i'_R}{k' W}} + V_{TN} \quad 3\text{-}2$$

$$i'_{IDE} - i'_R = \frac{k'}{2}\frac{W'}{L'}(A_v(V_Y - V_X) - V_{TN})^2 \times (1 + \lambda V_Y) \quad 3\text{-}3$$

where L and W are the length and width of N1, and V_{TN} denotes the threshold voltage of N1. A_v is the open-loop gain of the Op-Amp, L' and W' are the length and width of N3. λ is the channel length modulation parameter and $k' = \mu C_{ox}$ where μ and C_{ox} stand for mobility and gate-oxide capacitance per unit area, respectively. According to equation 3-3, an increase in $i'_{IDE} - i'_R$ causes V_Y to rise, resulting in a boost in the I_2 current (see Figure 3.2 (a)). The gain of i_{out}/I_2 has been designed to be significantly high by increasing the aspect ratio (width/length) of N4 over N3. Equations 3-2 and 3-3 describe the output current of the ECBCM circuit. Equation 3-4 defines the sensitivity of the device as the change in the average of the output current over one period of Φ1 and Φ2 for a given reference capacitance. In this design, we have tried to increase the sensitivity by, first, decreasing the value of the bias current, iB, and second, increasing the gain of iout over differential capacitances.

$$S = \frac{dAverage(i_{out})}{dC_s}|_{at\ C_R} \quad 3\text{-}4$$

In Section 3.4.1, the waveforms of this block and the dependency of i_{out} to $C_{IDE} - C_R$ (dC) are illustrated and the linearity and sensitivity of the ECBCM-Array circuit have been investigated using post-layout simulation results.

3.3.2 Proposed Multiplexing Topology for a Large Array

Figure 3.2 (b) illustrates the schematic of the proposed circuit composed of an array of electrodes. In this topology, a group of IDEs, 16 × 8 in this work, are multiplexed and connected to only one ECBCM circuit. In this multiplexing scheme, the P(i,j) and N(i,j),

where i and j represent row and column, respectively, are the only in-pixel devices. The gates of each pair of P(i,j)-N(i,j) transistors are connected to a network of multiplexed clock signals, namely □□□i,j), and □□□i,j) shown in Figure 3.3. This digital circuitry includes 3-bit and 2-bit multiplexers with A, B, C, D, E, F, and G as the control signals with G being the most significant bit in this 7-bit number. The timing signals resulting in □□□i,j), and □□□i,j) signals generated in the multiplexing circuit for rows i=j=1, i=2, j=1, and i=8, j=16 are shown in Figure 3.4, as three examples of how the multiplexing circuitry works. In this scheme, all the PMOS switches that are connected to the IDEs and provide a charging path are off except for the one whose IDE is being evaluated, called Active IDE. As an example, as shown in Figure 3.4 (b) when the input of the multiplexers, GFEDCBA is 0000001, P(2,1) and N(2,1) receive the Φ1 and Φ2 signals while the PMOS devices of the rest of the IDEs (P(i,j) for i ={1,…8}f, j={1,2,…16}) are all off. It is noteworthy to mention that the IDEs are charged at the falling edge of □□□i,j) and discharged at the rising edge of □□□i,j). The clock pulse signals of the reference side that are fed to P7 and N5 (see Figure 3.2 (a)) are not multiplexed as the reference is shared for all the IDEs. Figure 3.2 (b) also shows that in this multiplexing scheme, all other non-active IDEs are connected to the ground through the NMOS device. This is a great advantage in the electrochemical tests that creates a large counter electrode and makes the voltage of the solution uniformly close to zero. The electrodes in this work are IDEs implemented on the topmost metal layer with 2 fingers and dimensions of 35 μm by 30 μm.

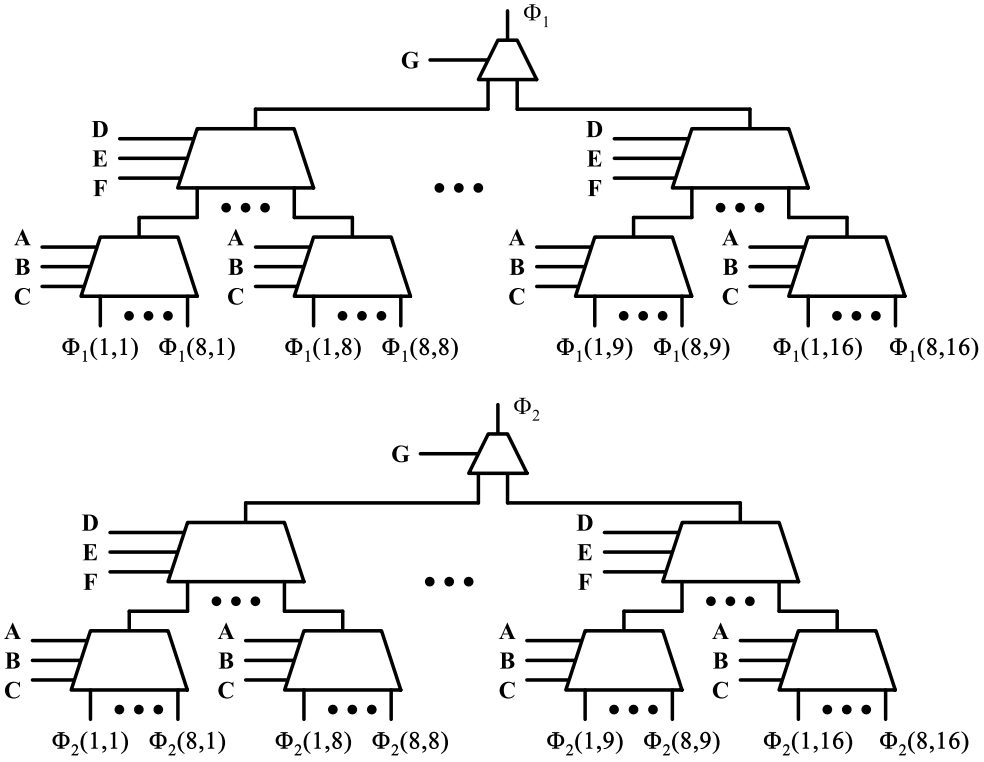


Figure 3.3: The multiplexing circuitry

3.3.3 Oscillator Circuit

The circuit topology of the oscillator, shown in Figure 3.5, is based on the charge and discharge cycles of a timing capacitor, CT, up to a reference voltage [113]. The part of the circuit shown in red illustrates the parts that we have changed compared to the CCO circuit of the non-array chip discussed in Chapter 2. The circuit depicted in gray is for tuning switches that can be considered for changing the frequency of the oscillation frequency. The circuit in blue illustrates the output stage of the current mirror circuitry from the ECBCM block. The size of MB1 and MB2 is crucial as they play the role of current mirrors in mirroring the output current of the ECBCM-Array into the CCO.

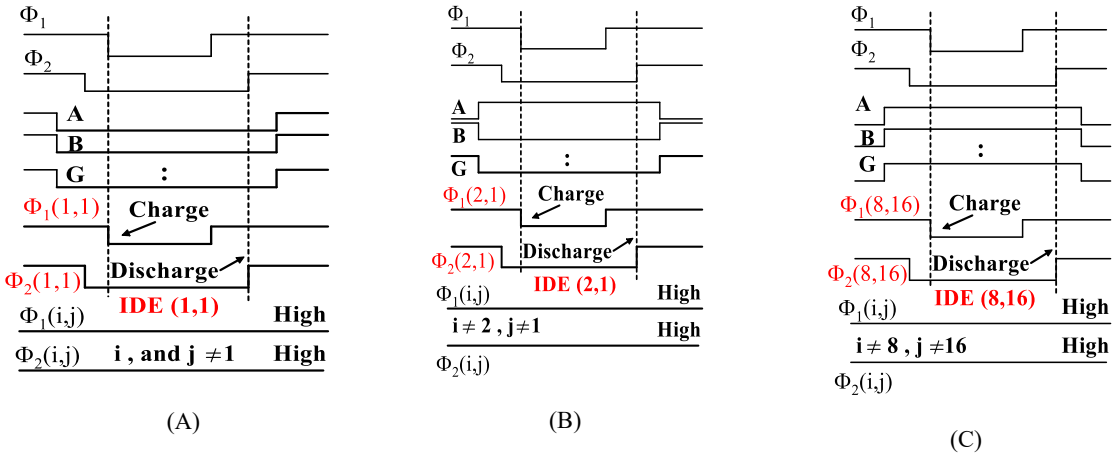


Figure 3.4: Timing diagram of the multiplexed clock pulses: (a) when all multiplexing signals are zero, IDE (1,1) becomes active IDE and receives the □□ and □□ clock pulses. PMOS and NMOS devices of all other IDEs are high, making the IDE connected to the ground through the NMOS device, (b) When A becomes high, IDE (2,1) is active, (c) IDE (8, 16) is active when all multiplexing signals are high.

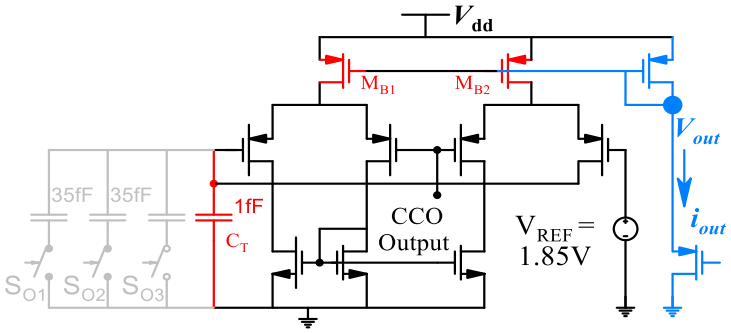


Figure 3.5: The CCO circuit topology. The gray parts are eliminated in the CCO of the array chip. The parts of the circuit shown in red illustrate the parts that we have changed and optimized compared to the original circuit. The circuit shown in gray depicts the switches that can be considered for tuning the oscillation frequency. The circuit in blue shows the output stage of the current mirror circuitry from the ECBCM block.

In addition, the value of the timing capacitance, CT, has an inverse relation with the frequency of oscillation. Smaller capacitance causes a decreased time constant that results in faster charge/discharge cycles and consequently higher oscillation frequency.

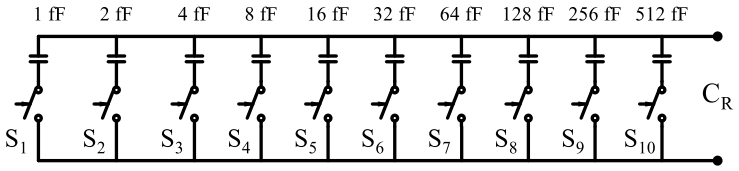


Figure 3.6: Circuit topology for the bank of capacitors of ECBCM-Array.

3.3.4 The Bank of Capacitors for Offset Capacitance Cancellation

With the proposed calibration-free measurement technique in Chapter 2, a smaller change in the programmable bank of capacitors results in a higher resolution in the scanning mode. While the ECBCM circuit provides a high dynamic range, the bank of capacitors enables sweeping the value of the reference capacitor to cancel unwanted offsets, such as the offset of remnants during the experiment. The sweeping step of 1 fF with 10 bits up to 1024 fF has been made possible with the programable bank of capacitors shown in Figure 3.6.

3.3.5 Generation of the Digital Output of the Chip

The digital output of the chip is generated in an on-chip 12-bit counter-serializer that counts the number of pulses received from the oscillator with no change as discussed in chapter 2. The same Φ_1 and Φ_2 signals are used to cycle through the counter and the serializer. In this chip, there are two outputs that work in parallel, and each is connected to 8 × 16 electrodes. In this topology increasing the number of electrodes will result in decreased speed since the interface circuitry is shared. To avoid that problem the number of outputs must be increased if the array size must be increased.

3.4 Simulation Results

In this section, the simulation results of the circuit for testing the multiplexing scheme and the performance of different blocks are demonstrated and the effects of different corners and temperatures are discussed.

3.4.1 ECBCM-Array Block's Dynamic Range and Sensitivity

Figure 3.7 illustrates the waveforms of the ECBCM block shown in Figure 3.2 (a) which is obtained by post-layout simulation. As seen in the figure, once i'_{IDE} becomes higher than i'_R, the value of I_2 increases. Since i_{out} mirrors I_2 with a large gain, their waveforms are alike with a difference in amplitude. In the circuit of the reference side, i'_R is the current passing through C_R amplified by the P_1 and P_2 pair. From the circuit of the sensing side, i'_{IDE} is the current passing through C_{IDE} amplified by the P_2 and P_4 pair. Since i_{out} is transitioning from low to high based on the comparison of the i'_{IDE} and i'_R, $(i'_{IDE} - i'_R)$, it can be said that the transitioning is based on the $(C_{IDE} - C_R)$.

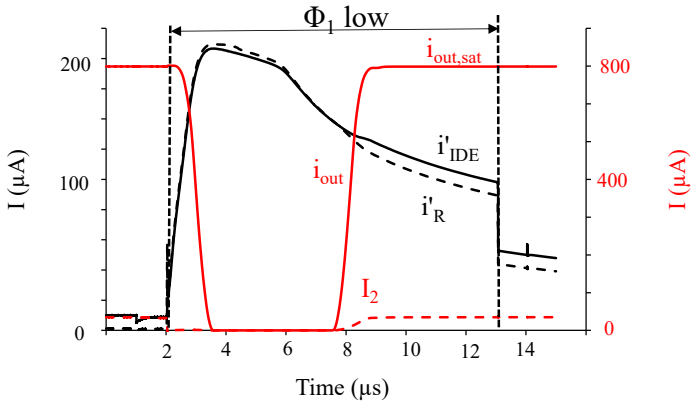


Figure 3.7: post-layout simulation results for ECBCM-Array circuit. The circuit works like a comparator of two currents, i'_{IDE} , and i'_R. The output is i_{out} that transitions in two states of zero and $i_{out,sat}$.

Figure 3.8 shows the post-layout simulation results for the transfer function of the ECBCM-Array block in different input ranges and the corresponding root mean squared parameter for the linearity. In this simulation, all the bits of the bank of capacitors are zero. Thus, the reference capacitance is equal to its offset value, shown to be close to 260 fF. The variation of sensing capacitance is the dC value, depicted in the figure, plus the offset capacitance of the array network, which is estimated to be about 260 fF as well. As seen in this figure, the linearity of the block can be considered an acceptable amount of R2 = 0.9886

with an IDR of 100 fF. The linearity of the curve increases for the smaller range of IDR. For instance, in the IDR of 80 fF, the linearity of the curve becomes R2 = 0.9927.

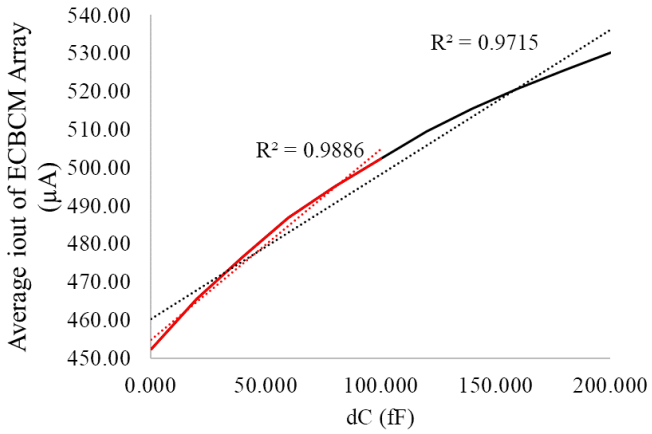


Figure 3.8: The linearity of the transfer function is R2 = 0.9886 in the dynamic range of 100 fF while it decreases to R2 = 0.9715 in a larger dC of 200 fF.

Figure 3.9 illustrates the change in the average of i_{out} for each 0.5 fF of differential input capacitance variation in the range of 2 fF within the IDR of the sensor. The simulation conditions for the bank of capacitors are the same as the conditions in Figure 3.8. The sensitivity of the block based on this post-layout simulation result is 0.59 µA/fF.

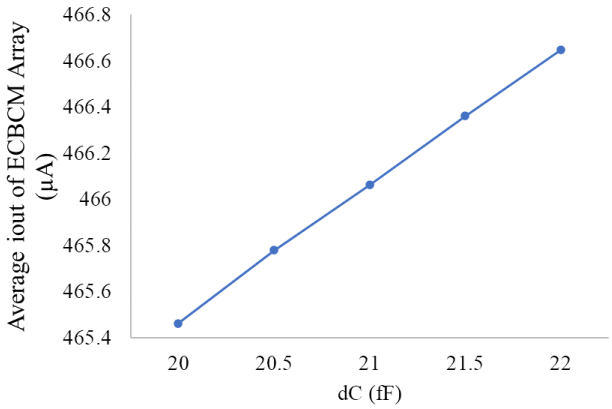


Figure 3.9: The change in the average of i_{out} for each 0.5 fF of differential input capacitance change in the range of 2 fF within the range of the sensor's dynamic range.

3.4.2 The Resolution of the Sensor

Figure 3.10 shows the post-layout simulation results of the ECBCM-Array circuit. This figure shows that the output current curve, i_{out}, shifts to left by about 95 ns for a unit dC increase. The oscillation frequency when $i_{out} = i_{out,sat}$ is about 75 MHz in the typical corner and temperature (25°C) conditions. Thus, the curve for 1 fF higher dC results in 7.125 more pulses when □□ is low (evaluation period, see Figure 3.7). Therefore, the resolution of the sensor is roughly equal to 150 aF. This can be changed in different process corners and temperatures. The simulation results in different corners and temperature conditions are given in Sections 3.4.6 and 3.4.7.

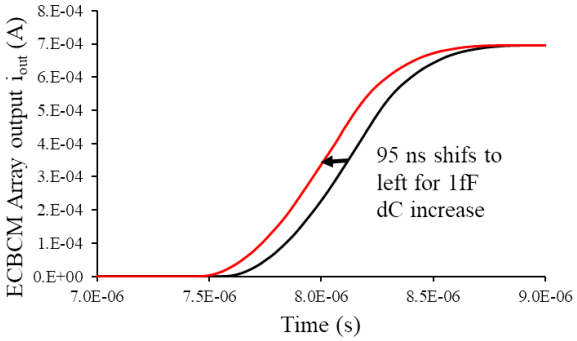


Figure 3.10: The amount of shift to left in the output of the ECBCM-Array circuit as a result of a unit increase in the differential input capacitance.

3.4.3 Current-controlled Oscillator (CCO) and Back of Capacitors

Figure 3.11 shows the characteristic curve of the oscillator. The linearly increasing part of the curve which is the IDR of the CCO is about 1000 µA. In this range, the oscillation frequency can reach about 90 MHz.

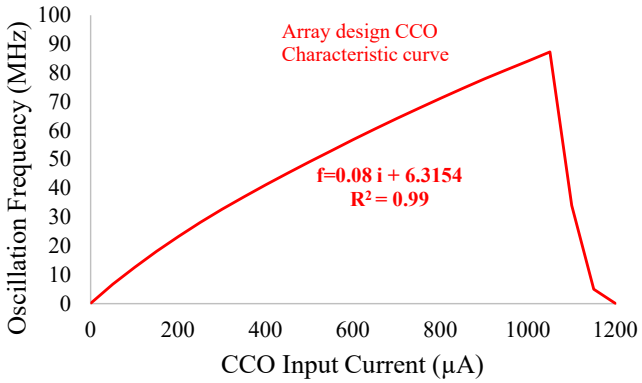


Figure 3.11: The characteristic curve of the oscillator. The linearly increasing part of the curve denotes the IDR of the CCO and is about 1000 µA where the oscillation frequency can reach about 90 MHz.

3.4.4 Bank of Capacitors

The post-layout simulation results show the offset value of the bank as well as the capacitance values that can be generated with a 10-bit-binary input (Figure 3.12). The offset capacitance for the bank of capacitors is about 260 fF. Thus, the reference capacitance value when all the switches are off is equal to this offset capacitance.

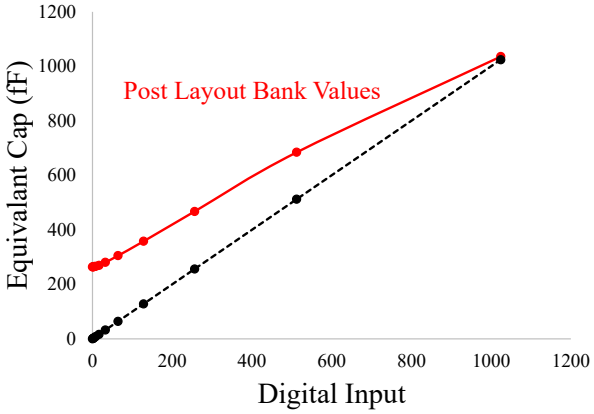
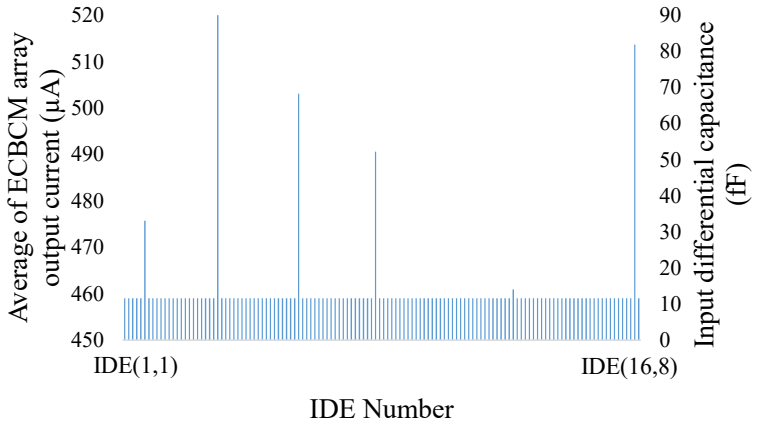


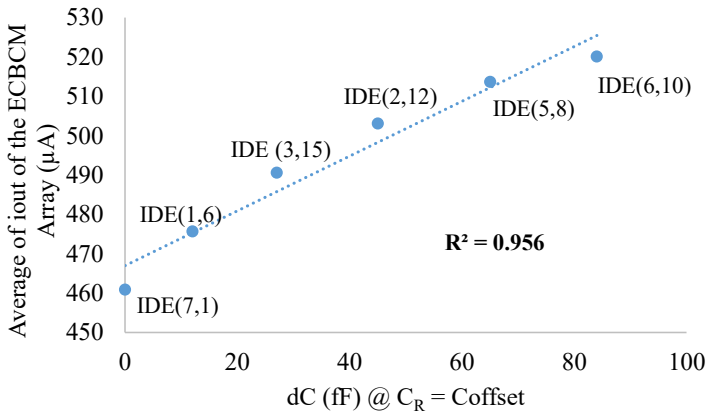
Figure 3.12: The comparison between the nominal value of the bank of capacitors and the post-layout values.

3.4.5 Multiplexing Circuitry

To show the functionality of the multiplexing scheme, we have performed post-layout simulations by selecting IDEs that are connected to capacitances within the IDR of the system from different regions of the implemented array. This simulation is to test the effect of the routing in the array on the readings of the sensor. The results are shown in Figure 3.13 (a) and (b). In Figure 3.13 (a), the average of iout is shown on the left axis and the differential capacitance that has been connected to an IDE, numbered as mentioned on the x-axis, is shown on the right axis. In Figure 3.13 (b), the IDEs are sorted based on the value of the capacitance that is connected to them. For instance, IDE (7,1) is connected to a capacitance of 260 fF which is equal to the offset capacitance of the bank of capacitors, and IDE (6,10) is connected to a 260 fF + 83 fF.



(A)



(B)

Figure 3.13: Post-layout simulation results for the functionality of the array. IDEs that are connected to capacitances within the IDR of the system are selected from different regions of the implemented array. The value connected to these IDEs is equal to the offset capacitance of the reference side plus the value of dC shown in the figure: (a) Bar graph, (b) Average output current with respect to dC value.

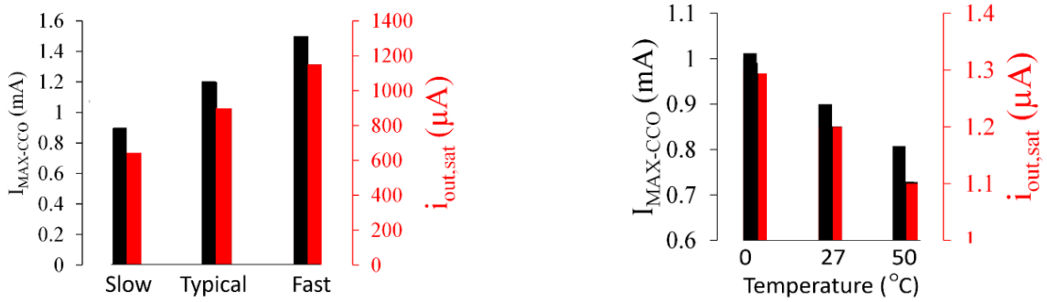
Results show a linear increase for different IDEs with a root mean squared index of R2 = 0.956. This result shows that the multiplexing scheme can successfully evaluate one capacitance change connected to the target IDE in the array and can successfully turn off other IDEs with the insignificant effect of the array routings or other IDEs.

3.4.6 Corner Analysis

Since the counter-serializer is a digital block, whose functionality cannot be significantly altered by process variations, the ECBCM-Array and the CCO blocks' variations within different process corners are investigated. Based on the simulation results shown in Figure 3.14 (a), the IDR of the CCO shown as $I_{MAX\text{-}CCO}$ varies from 900 µA at the slow corner to 1.2 mA at the typical corner and about 1.5 mA at the fast corner. On another side, the variation in the saturated output current of ECBCM-Array block, $i_{out,sat}$, varies from around 650 µA to around 1.15 mA in the range of slow corner to fast corner.

3.4.7 The Effect of Temperature Variation

The effect of temperature on the ECBCM-Array and the CCO blocks is investigated through post-layout simulations. Figure 3.14 (b) demonstrates the increase in the effect of temperature on IMAX-CCO and iout,sat. By increasing the temperature from 0°C to 50°C, oscillator's IDR decreases from 1 mA to 800 µA, and iout,sat reduces from 1.3 mA to 1.1 mA. By increasing the temperature, the maximum output current decreases resulting in a uniform decline in the output value.



(A) (B)

Figure 3.14: Post-layout simulation results: (a) for different corners: Maximum current causing the oscillation at different corners based on post-layout simulation: At the slow corner, the oscillation stops at 900 µA. At the typical corner, the oscillation stops at 1.2 mA, and at the fast corner, the oscillation stops at about 1.5 mA, (b) for different temperatures: Maximum current causing the oscillation at different temperatures based on post-layout simulation: At 0°C the oscillation stops at 1 mA, at 27°C the oscillation stops at 900 µA, and at 50°C, the oscillation stops at about 800 µA.

This means that for the same dC, an increase in temperature can result in uniformly smaller values for the output.

3.5 The Fabricated Chip and the Test Bench

In this section, we demonstrate and explain the fabricated chip and the test bench.

3.5.1 The Fabricated Chip

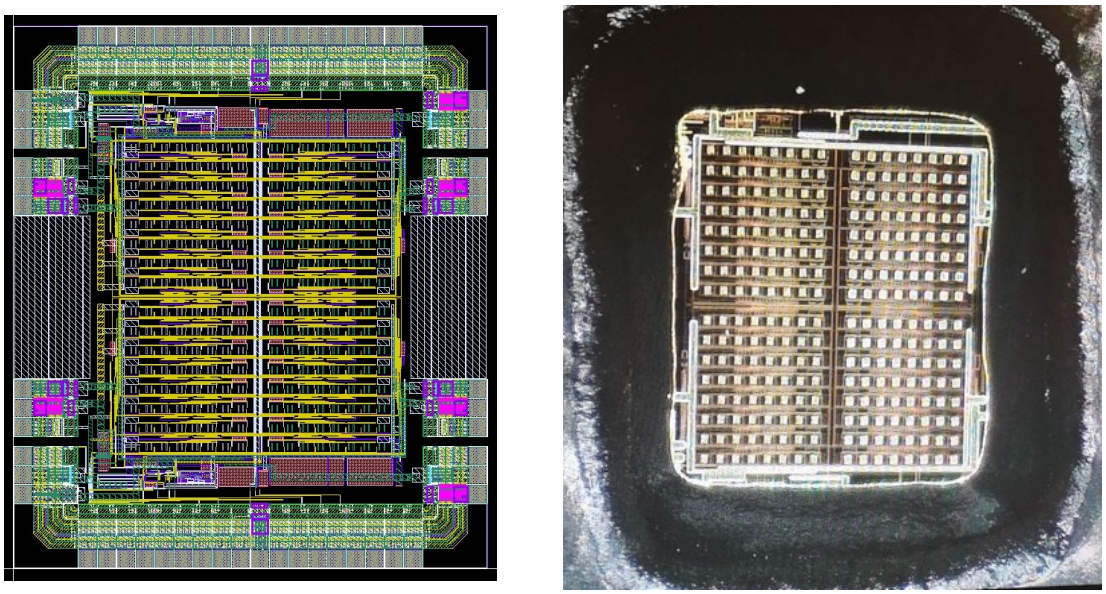
The chip was implemented in AMS 0.35 µm CMOS technology. In the layout, an 8×16 array was implemented to one block of ECBCM with the CCO and the 12-bit counter-serializer. To increase the number of electrodes, this layout was repeated in the opposite direction to build a 16×16 array of electrodes. Therefore, the whole chip is composed of two independent compartments each with independent outputs. Also, the IDEs have been implemented as both passivated (with silicon oxide) and non-passivated (bare aluminum electrode) in both compartments. As a result, each compartment has 8 × 8 passivated and 8 × 8 non-passivated arrays of electrodes. The layout is shown in Figure 3.15 (a) and the partially encapsulated chip is illustrated in Figure 3.15 (b).

3.5.2 Test Bench printed circuit board (PCB)

The chip is in a commercial CPGA85 ceramic package on a PCB dedicated to providing the necessary clock signals as well as data acquisition shown in Figure 3.16. There are five different voltage regulators and one multiplexer on this board. Four voltage regulators are of the type of TLV75533PDBVR, which is a 500-mA, high-PSRR, low-IQ, low-dropout voltage regulator with 5 V enable voltage, SOT-23 package, and -40 to 125°C operating temperature range. Each of these four regulators was used to power analog and digital voltages to 3.3 V, two for the right side and two for the left side. TLV713185PDBVT, which is a 500-mA, high-PSRR, low-IQ, low-dropout voltage regulator with 5 V enable voltage, SOT-23 package, and -40 to 125°C operating temperature range was utilized for the required 1.85 V reference voltage for the oscillator's VREF pin. All LDOs’ enable pins were tied to the input voltage. TMUX1247DCKR, a precision analog multiplexer with 30-ohm ON

resistance and rail-to-rail capability was also used. Decoupling capacitors were employed for all the components' input power and output power supplies to reduce the noise.

The PCB was connected to an Arduino DUE board that creates the clock signals and performs the data acquisition using an SPI port. The MCU was configured as a master and the chip was a slave where data transmits from the chip to the MCU with a shared clock bus, Φ3. Details about the test bench are given in Appendix III.



(A) (B)

Figure 3.15: (a) Die layout, (b) Microscopic image of the partially encapsulated chip.

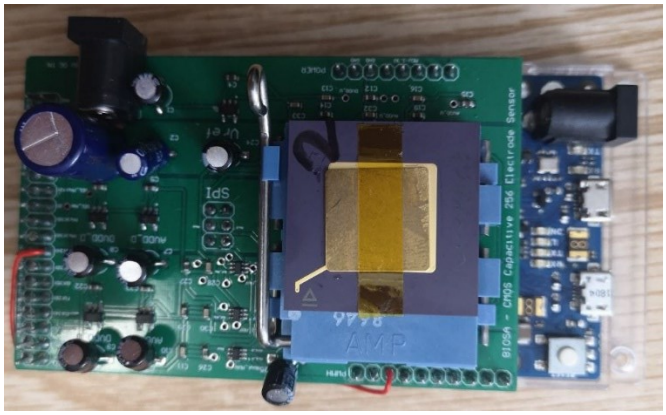


Figure 3.16: The designed test bench.

3.6 Measurement Results

In this section, after showing the characterization results without any samples in Section 3.6.1, we will demonstrate the experimental results using different liquid samples in Sections 3.6.2 to 3.6.5.

3.6.1 Characterization Results with no Sample

We obtained the characterization curves without any samples. The curves were acquired by recording the output of the chip as the reference capacitor was swept in its full range for every pixel. The resulting decreasing patterns are shown in Figure 3.17. In these curves, an increase in CR results in a gradual drop in the output of the chip creating a linear decreasing pattern. The pattern is the same for both passivated and non-passivated electrodes with a slightly higher value of the output which indicates a higher capacitance due to the passivation layer capacitance. Regarding IDE (1,7), a transmission gate is implemented in series with the IDE which connects and disconnects the IDE to the sensing circuit. Figure 3.17 also demonstrates the measurement results for the closed transmission gate that shows a large shift to the right compared to the IDEs without a transmission gate which indicates the effect of parasitic capacitances of the transmission gate.

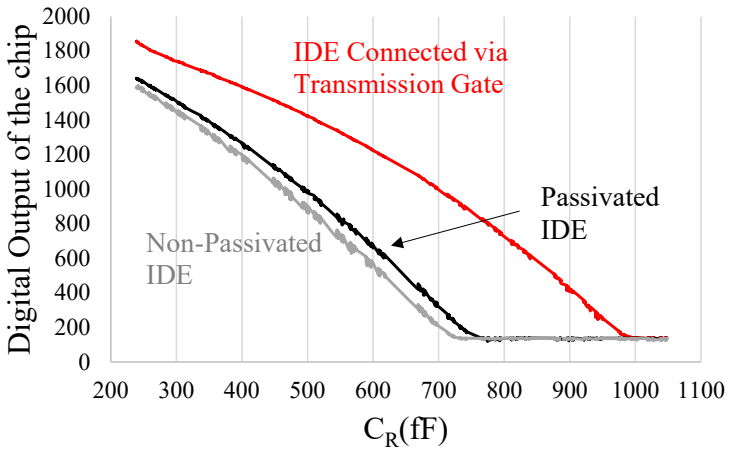


Figure 3.17: The output of the chip with the decreasing pattern with respect to the rise in the value of the reference capacitance.

3.6.2 Pixelated Results for Monitoring Droplets

To demonstrate the ability of the sensor to differentiate between the liquids with different dielectric values and to determine the position of the droplet, different droplets with various volumes were put manually by a precise micropipette on the surface of the electrodes of the partially encapsulated chip. It is expected to see different outputs for the electrodes covered and uncovered by the sample. We scanned all 256 electrodes once before and once after putting the droplet. Each full-page scanning takes about 7 minutes. In this experiment, the top of the sensing area was covered by a lid to provide enough time for scanning the whole area by decreasing the evaporation time of the droplet and avoiding the effects of light penetration on the measurement. As a result, it is possible to map the droplet footprint with the sensor readings with an acceptable accuracy to match the image with the sensor data. by considering the presence and absence of the sample as the sensed and baseline values, respectively, the metric for the measurement of the capacitance change can be the difference between these two values. After obtaining this index for all the pixels, a map was generated that is shown in each part of Figure 3.18 beside each droplet snapshot. Figure 3.18 (a) to (f) are obtained for 0.3 µL of pure water, 0.5 µL of 10% ethanol in pure

water, 0.5 µL of 30% ethanol in pure water, 0.5 µL of 50% ethanol in pure water, 0.5 µL of 10% methanol in pure water, and 0.5 µL of 30% methanol in pure water, respectively. As seen in these figures, all the maps indicate that the pixels under the droplet show a higher differential index than the ones that are not covered.

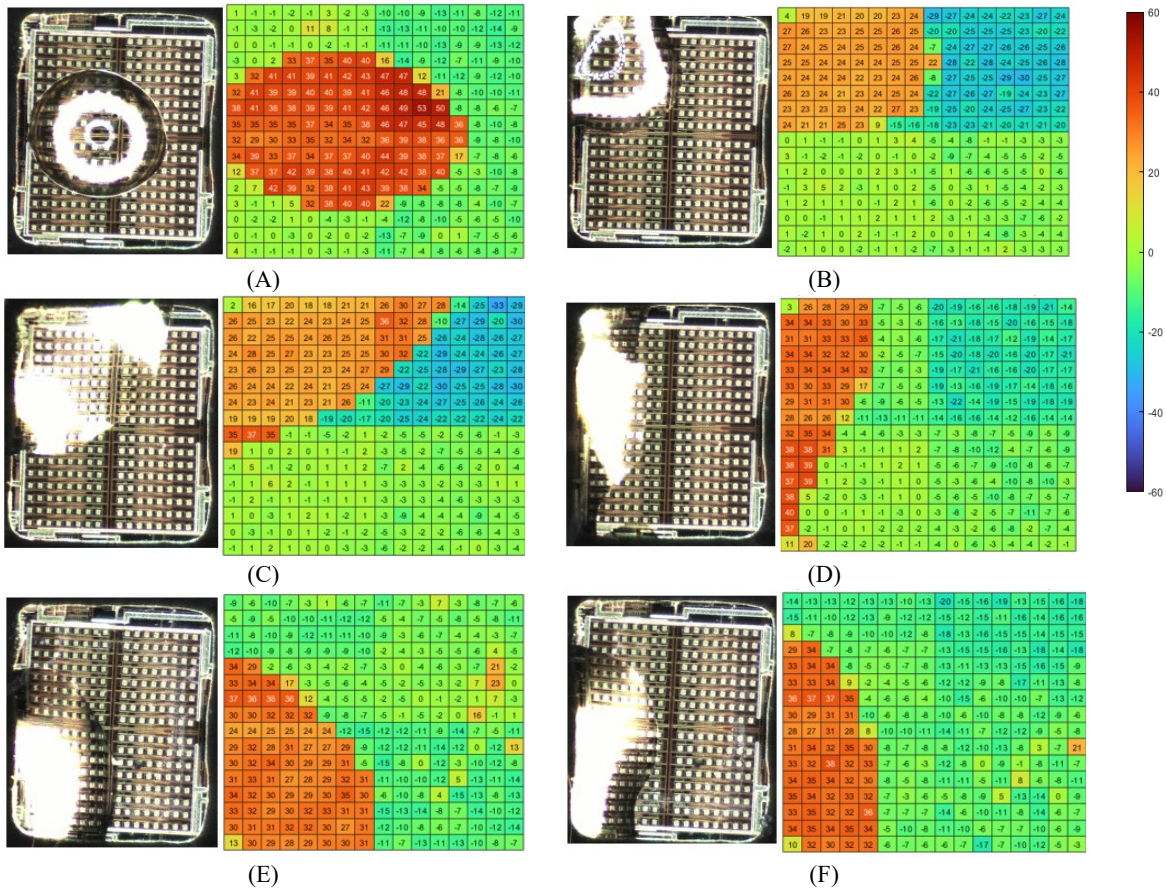


Figure 3.18: The microscopic images of the chip during the droplet test (on the left side) and the differential values of the output with respect to the baseline (on the right side) for: (a) 0.3 µL of pure water, (b) 0.5 µL of 10% ethanol in pure water, (c) 0.5 µL of 30% ethanol in pure water, (d) 0.5 µL of 50% ethanol in pure water, (e) 0.5 µL of 10% methanol in pure water, (f) 0.5 µL of 30% methanol in pure water.

3.6.3 Sensitivity of the Sensor to Different Dielectric Constants

To test the sensitivity of the sensor, the chamber was filled with different samples with different dielectric properties, and the top of the sensing area was covered by a paper lid to avoid light penetration and slow the evaporation speed of the liquid. Water, ethanol, and methanol with dielectric constants of 78.2, 24.55, and 32.7 at room temperature (25°C) were

employed for this test. Then, we scanned all the pixels and all reference electrodes for each pixel (which usually takes about 7 minutes).

The differential output with respect to the baseline was measured for all pixels when the chamber is covered with pure water, methanol, and ethanol. Figure 3.19 shows the average of the differential output with respect to the baseline for all pixels in this test. As depicted in Figure 3.19, the chip is sensitive to solutions with different dielectric constants as all three liquids have been distinguished. The error bars are obtained from three times repetitions of the experiment.

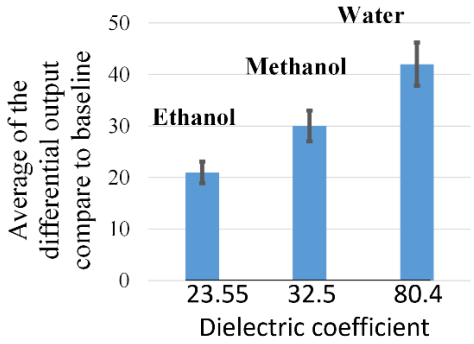
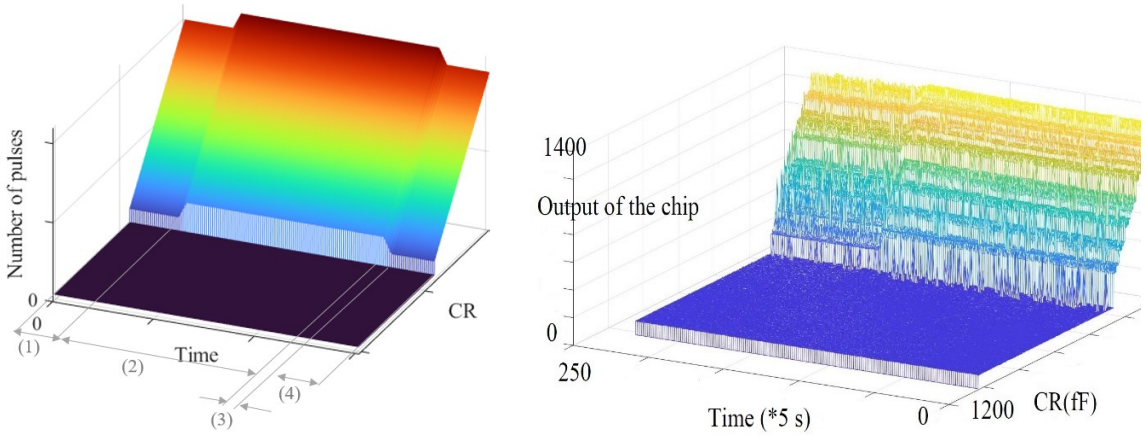


Figure 3.19: The average of the differential outputs with respect to the baseline measured for all pixels when the chamber was filled with water, ethanol, and methanol (k is the dielectric constant). Error bars are obtained from 3 times repetitions of the experiments

3.6.4 Time-resolved Results with Water Droplets on a Single Electrode

With the focus on the data acquisition of a single electrode, a 3D profile can be generated. The information that this 3D time-resolved pattern contains is the profile of the variations in the capacitance of an IDE whose status changes from fully covered by the droplet to completely dried. Figure 3.20 (a) illustrates the conceptual view of this type of 3D profile. This transition has been captured and shown in Figure 3.20 (b) for a water droplet showing the capacitance transitions from high to low. The gradual decrease in capacitance value indicates the evaporation of the water droplet on the IDE. The difference in the capacitance value is about 50 pulses which can be translated to about 5 fF of change in the

capacitance since from the post-layout simulations, we know that each pulse is about 0.15 fF. To decrease the effect of high-frequency noise, we have applied a moving average filter of size 11 to the data in MATLAB.



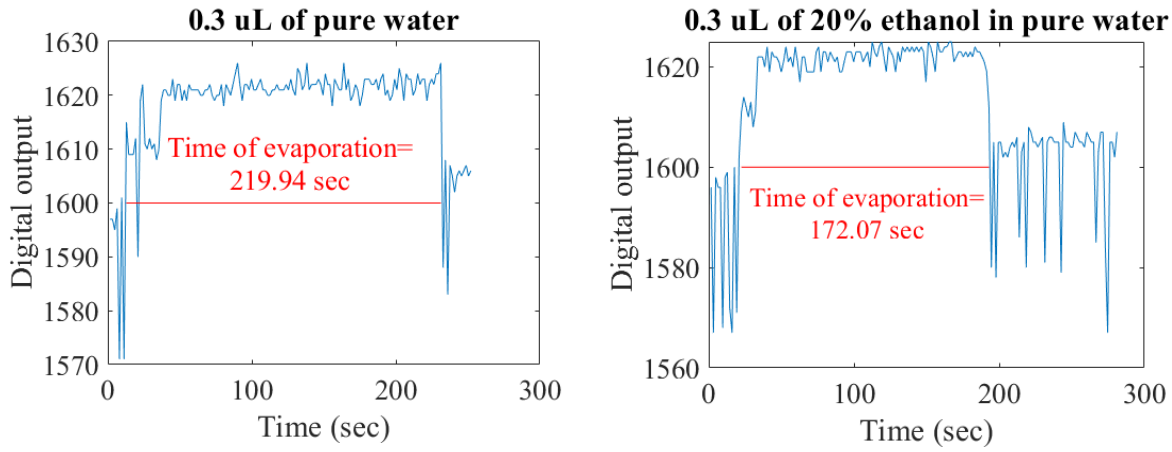
(A) (B)

Figure 3.20: (a) Conceptual view of the 3D profile obtained from a single electrode showing the capacitance decrease during the evaporation of water droplets. The regions are: (1) baseline, (2) presence of the droplet on the electrode, (3) transition from droplet to complete evaporation, (4) complete evaporation, (b) An experimentally measured 3D specific pttern obtained for a single IDE that shows capacitance decrease during the evaporation of water droplet.

3.6.5 Time of Evaporation of Different Samples

This sensor is also able to measure the evaporation time of different samples by using one of the electrodes. To do this, we obtained a 3D curve for one of the electrodes in the array. This 3D curve was obtained for IDE (8,8) by repeating the measurements and sweeping all the values of the reference capacitors in each repeat. The sensing area was not covered with any lid. To avoid the capillary effects of the walls and assure the desired electrode is in contact with the liquid, the droplets were put on the center of the sensing surface without touching the chamber walls. A precise pipette was employed to introduce the sample to the array. Figure 3.21 (a) and (b) show the curves of the digital output of the chip versus time for 0.3 µL of pure water and 20% ethanol in pure water, respectively. As

seen in these figures, the evaporation times obtained for these liquids are 219.94, and 172.07 seconds. The addition of ethanol to pure water decreases the evaporation time of the droplet.



(A) (B)

Figure 3.21: The digital output versus time for the first CR for the electrode in row 8 and column 8 exposed by 0.3 µL of (a) pure water, (b) 20% ethanol.

3.7 Chapter Summary

In this chapter, we proposed a 16 × 16 CMOS capacitive sensor array with a novel multiplexing scheme based on a wide-IDR current-mode structure using an ECBCM block, a CCO, and a counter. The simulation and experimental results have demonstrated the ability of the sensor to differentiate between the dielectric constants of different liquids, determine the location of the droplet on the sensing area, and measure the evaporation time of the droplet on the chip surface. Using microfluidic devices can help to mitigate the errors due to the manual introduction of the sample to the sensor. In addition, denser arrays of electrodes that can cover all parts of the sensing area can increase the accuracy of the system. Moreover, due to the evaporation speed of the droplet and the limited speed of this circuit, the 3D profiles obtained by several repetitions of the sweeping of the reference capacitors can be achieved for only one of the electrodes. A readout circuit with a higher speed can enable us to obtain such 3D profiles for all electrodes. Furthermore, increasing the number

of reference capacitors can help to improve the accuracy of the sensor. It is also worth mentioning that, in this work, since the readout circuit was under the electrodes, the sensor was sensitive to light. But using the microscope light to take the images was inevitable. Also, the environmental temperature was not controlled. Thus, the effects of the lights and temperature should be considered to achieve a more practical design. Research to solve these issues is already underway. However, the results so far have been very promising, and this approach could conceivably lead to droplet-on-chip analyses.

Chapter 4: Dry DNA Monitoring for DNA Data Storage Devices

We have shown, for the first time, the detection of DNA nano-mass in the dry phase using the CMOS capacitive sensor without the need for DNA hybridization for future DNA data storage technologies. The details of this chapter were published as a paper entitled "CMOS capacitive dry DNA storage monitoring: design, implementation and experimental results" in IEEE Sensors Journal [79].

4.1 Abstract

This chapter proposes the applicability of the CMOS capacitive sensor in monitoring the dried DNA mass for emerging DNA memory technologies. The concept of DNA-based data storage has shown to be a promising solution with an ultra-high data density storage capability of gigabytes per nanogram mass of DNA. There are several drawbacks to achieving ubiquitous technology and existing research has mostly addressed the translation of digital data to synthesized nucleotides, the physical storage of DNA, and reading out the data via sequencing, as well as computational processes. The successful detection of down to 45 ng /μL mass of dried DNA has been shown with the experimental results that consist of five runs for five different concentrations. Based on the results, the detection range of sub-pico Mol has been achieved which is compatible with the concentrations of DNA used in DNA memory technologies.

4.2 Introduction

There has been an astonishing growth in the data created, captured, copied, and consumed worldwide from 2×1012 gigabytes in 2010 to 79×1012 gigabytes in 2020 which is predicted to reach 175×1012 gigabytes by 2025 [126]. Current technologies such as solid-state drives (SSDs), optical storage devices, magnetic disk drives, and cloud-based storage systems are less likely to meet the need to store the expeditiously growing global data soon. Another concern is the lifetime of the available storage devices. In the quest to find durable and reliable high-capacity memories, DNA has been identified as a compact, durable, and recoverable medium for data storage with the capability of storing several gigabytes in one gram mass for decades. [21]. Figure 4.1 demonstrates the end-to-end workflow of a DNA-based data storage system. In the first step, the digital binary data composed of "0" and "1" is encoded into the sequence of four DNA bases of Adenine (A), Thymine (T), Guanine (G), and Cytosine (C). The second step is called DNA synthesis in which DNA sequences are written into actual DNA molecules known as information DNAs (iDNAs). In the third step, called DNA storage and random access, DNA molecules are physically organized into a library. The capability of random access makes it possible to selectively get access to only the desired part of the written information. In the fourth step, the stored DNA oligonucleotides are read through DNA sequencing. Finally, the initial binary codes can be obtained by decoding the DNA sequences to digital data [127], [128]. There are still many challenges limiting the use of DNA-based data storage systems [129], [130] one of which is monitoring the storage of the synthesized DNA strands on physically isolated and addressable pools which is the focus of this chapter. Improper DNA storage may cause a high risk of contamination as well as DNA loss and consequently end in the loss of information. A breakthrough reported in [131] utilizes digital microfluidics (DMF)-based

high-density DNA storage library to isolate DNA spots on a glass cartridge. To fulfill random access in this system, a dehydration/rehydration procedure was proposed by which DNA spots can be moved, deposited, and dehydrated on the cartridge in separate pools and then retrieved through a rehydration process using a droplet of water. Since physically isolated DNA spots can share the same addresses (primers), more bases of DNA will be available to store the translated data resulting in higher storage capacity per same DNA mass. The data recovery, especially after long-term storage, might be affected by various factors such as dwell times, temperature, humidity, contaminations, and the remnants of the DNA samples which can result in data loss. Thus, the bottleneck of this innovative approach is the requirement of bulky bench-top devices and a time-consuming procedure to indirectly detect the DNA mass in both wet and dry states and measure it from the concentration of the retrieved DNA sample.

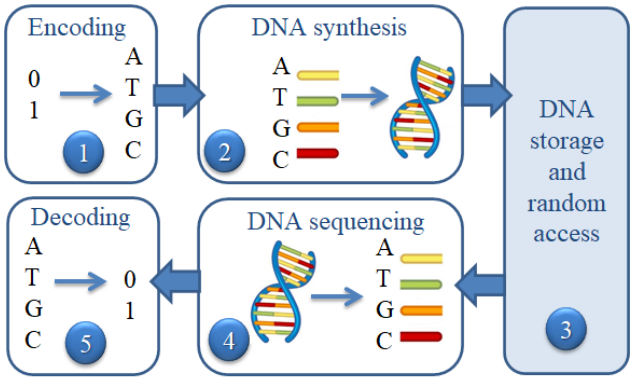


Figure 4.1: The end-to-end workflow of a DNA-based data storage system: (1) Encoding, (2) DNA synthesis, (3) DNA storage and random access, (4) DNA sequencing, (5) Decoding

Automatic sensors integrated by using CMOS technology can be promising candidates to reduce the size and cost of DNA storage systems. CMOS capacitive sensors are among these sensors. To the best of our knowledge, most of the CMOS capacitive sensors designed for DNA analyses are reported for DNA hybridization detection and DNA sequencing with no attention to developing sensors to be incorporated with DNA storage systems to monitor

negatively charged iDNA mass. We demonstrate for the first time, the utilization of the proposed CMOS capacitive sensor in Chapter 2 for immobilization-free monitoring of nano mass of DNA molecules and detecting the dehydration/rehydration events as well as approximating the amount of the DNA mass in the dried phase. This chapter is dedicated to this new application to quantify the retrieved DNA from the dehydration/rehydration procedure of such DNA storage systems. The experiments show the applicability of this sensor for monitoring the DNA sample in the drying phase.

This chapter is organized as follows. Section 4.2.1 gives an overview of the related works on CMOS DNA sensors, especially capacitive sensors, as well as core-CBCM capacitive sensors. The mathematical modeling of DNA on the electrodes is described in Section 4.2.2. Section 4.3 is dedicated to experimental results.

4.2.1 CMOS-based DNA Sensors for DNA Detection

Various label-based and label-free CMOS sensors have been reported in the literature such as optical [132], magnetic [133], and electrochemical [134], [135] for the detection of DNA. The detection of DNA has mostly relied on DNA hybridization when the DNA strands hybridize with a recognition element covering the electrode surface in a post-processing procedure. Various materials can be fabricated as the top surface material through CMOS and post-CMOS processes among which gold (Au) is widely used in DNA hybridization detection devices to improve the immobilization of DNA probes which provides reliable bonding to organic molecules containing amine groups and thiols [101], [103], [136]–[138]. The approach of interest in the attachment-based sensors is the interface capacitance measurement which can be conducted using simpler and faster readout circuits than impedance sensors. In [9], a core-CBCM circuit has been employed to measure the capacitance variations due to DNA hybridization of Alkanethiol-modified single-stranded

DNAs (ssDNAs) with 25-mer length as probe molecules which were immobilized on the electrodes by covalent S–Au bonds. Some works have used silicon dioxide (SiO2)-coated Aluminum (Al) layers for DNA analyses. In [139], 20 μm × 20 μm-sized IDEs with an aluminum layer (metal 3) of a two-polysilicon-four-metal (2P4M) 0.35 μm CMOS process covered by the inter-metal SiO2 thin film are utilized for DNA hybridization detection. In this chapter, the main purpose is to detect the DNA on the surface using an immobilization-free capacitance measurement method and by employing aluminum electrodes using the sensor explained in Chapter 2.

4.2.2 Mathematical Modeling of the On-chip IDEs

In this section, we propose a mathematical model for the capacitance of the on-chip IDEs with considering the existing parasitic and fringe capacitances when implemented on the topmost metal layer of a CMOS chip for DNA detection. We have used pad masks to etch the native protection layer, typically composed of 1 μm silicon oxide and silicon nitride layer on top of topmost metal layer in this CMOS technologies [140]. As a result, aluminum is exposed to air resulting in the formation of a very thin layer of aluminum oxide. Figure 4.2 (a) illustrates a cross-section schematic of the implemented IDE electrode in the dried phase (the aqueous solution has been evaporated and DNA remnants have been deposited). The cross-section schematic and the parasitic capacitances have been shown based on the information on the datasheet of the 0.35 μm 50 V CMOS Process Parameters [140] as well as the implemented geometry of our electrodes. The dimensions and the geometry of the electrodes are shown in Figure 4.2 (d). The width and the gap are both 12 μm and the IDE has 5 fingers. The IDE has been implemented on the topmost metal layer of the AMS 0.35 process technology [140] and the material is aluminum, based on the datasheet. The insulation layer between the metal and device layers is silicon oxide. As a result of etching

the protection layer, the electrodes are at a lower elevation compared to the adjacent protection layer, as shown in the schematic. Three distinct parasitic capacitances are shown that are created in this topology. Coffset-sub is formed between the electrodes and the underlying layers (in our layout, we have not implemented any circuit under the electrode, thus this capacitance is between the electrode and the substrate). Coffset-fringe stands for the offset capacitance due to the fringe electric fields underneath the electrodes through the underlying layers. Coffset-dir denotes the offset capacitance because of the direct electric field between the electrodes while Csens is the fringe capacitance due to the fringe electric field formed on top of the chip. Among these capacitances, only Csens can be affected when the electrodes are exposed to analyte samples. In the following sections, the mathematical model of the electrode is given before the experiment when there was no DNA remnant on the electrodes as well as after the complete evaporation of the sample.

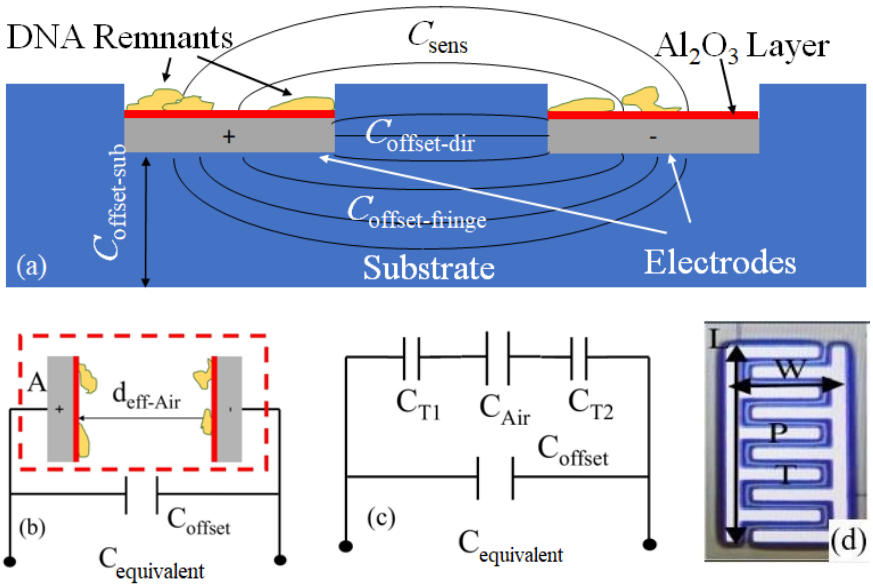


Figure 4.2: (a) Cross-section schematic of the implemented IDE electrode, (b) Equivalent capacitance model, (c) Equivalent electric model, (d) microscopic image of the implemented electrode and length(L) = 220µm, width (W)=110 µm, finger width(T)=12 µm, and pitch(P)=12 µm.

4.2.2.1 Before Exposure to DNA Samples

The value of Coffset-sub can be obtained from the CMOS technology datasheets where the per area parasitic capacitance value between different layers of the technology is reported. It is typically a function of the area of the implemented electrode, A, as well as its perimeter, PR as shown in 4-1 [140].

$$C_{offset-sub} = \alpha_1 \times A + \alpha_2 \times PR \quad 4\text{-}1$$

where α_1 and α_2 are process-dependent. Coffset-dir capacitance is a function of the side area of the electrodes that coincide with each other, and the electrode pitch, P, which is given in 4-2.

$$C_{offset-dir} = \varepsilon_0 \frac{\varepsilon_{Sio_2} \times P_{coinside} \times E_{th}}{P} \quad 4\text{-}2$$

where ε_0 is the vacuum permittivity, $\varepsilon_{\mathrm{Sio_2}}$ denotes the relative permittivity of silicon oxide as the dielectric between the electrodes, P_{coinside} stands for the perimeter of the electrodes that coincide with each other, E_{TH} represents the thickness of the electrodes and P is the pitch of the electrodes. Considering the symmetry in the implementation of the IDEs, it can be approximated that Coffset-fringe is $\varepsilon_{\mathrm{Sio_2}}$ times larger than Csens as expressed in 4-3.

$$C_{offset-fringe} = \varepsilon_{Sio_2} \times C_{sens} \quad 4\text{-}3$$

The overall offset capacitance, Coffset is the additional Coffset-sub, Coffset-dir, and Coffset-fringe given in 4-4.

$$C_{offset} = C_{offset-sub} + C_{offset-dir} + C_{offset-fringe} \quad 4\text{-}4$$

Figure 4.2 (b) illustrates an equivalent capacitance model of the electrodes shown in Figure 4.2 (a) where A is the area of electrodes and deff-Air is an effective equivalent direct distance for the fringe distance. The strips shown in red represent the oxide layer created on the metal because of its exposure to air with an exaggerated thickness. The thickness of the

aluminum oxide, which is formed naturally by being exposed to air, can reach less than 10 nm [141] and as a result, $C_{\mathrm{Al_2O_3}}$ is significant. The equivalent model depicted in Figure 4.2 (c) represents a simplified electric model with three capacitors in series, one with the air as its dielectric and the others representing the capacitances of the aluminum oxide layer affected by the presence of the DNA. The equivalent capacitance without the presence of DNA is given by 4-5.

$$C_{equivalent} = \varepsilon_0 \frac{\varepsilon_{PL} \times \varepsilon_{Air} \times A}{\varepsilon_{PL} \times d_{eff-Air} + \varepsilon_{Air} \times (2d_{PL})} + C_{offset} \quad 4\text{-}5$$

where $\varepsilon_{\mathrm{PL}}$ stands for the relative permittivity of the aluminum oxide passivation layer, $\varepsilon_{\mathrm{Air}}$ is the relative permittivity of air, and d_{PL} represents the thickness of the passivation layer.

4.2.3 After Exposure to DNA Samples

Figure 4.2 (b) demonstrates the equivalent capacitance model when the sample has been completely evaporated and DNA remnants have been deposited on the electrodes. DNA remnants play the role of a third dielectric in the equivalent capacitance model. The percentage of the area of the electrode that is covered by DNA, referred to as confluence, confn=A1/A (where A1 is the surface area covered by DNA remnants and A is the total surface area of the electrodes), determines the amount of change in the capacitance. Figure 4.2 (c) illustrates the equivalent electric circuit model for the dried phase of DNA where deposition of DNA affects the capacitances of the passivation layer shown as CT1 and CT2. Equations 4-6 and 4-7 describe CTn and Cequivalent, respectively.

$$C_{Tn} = \varepsilon_0 \times A\left(\frac{\varepsilon_{PL} \times \varepsilon_{DNA} \times conf_n}{\varepsilon_{PL} \times d_{eff-DNA} + \varepsilon_{DNA} \times d_{PL}} + \frac{\varepsilon_{PL}\,(1-conf_n)}{d_{PL}}\right), \quad n = 1, 2 \quad 4\text{-}6$$

$$C_{equivalent} = C_{offset} + (C_{T1} \,||\, C_{Air} \,||\, C_{T2}) \quad 4\text{-}7$$

where $\varepsilon_{\mathrm{DNA}}$ stands for the relative permittivity of the dried DNA, and $d_{\mathrm{eff-DNA}}$ represents the average thickness of the sedimented DNA. Equation 4-6 shows that the value of capacitance of the passivation layer depends on the percentage of the coverage of DNA on the electrodes, $conf_n$. From 4-7, equivalent capacitance is equal to the combination of C_{T1}, C_{T2}, and C_{Air} in series plus C_{offset}. As a result, an increase in the measured $C_{\mathrm{equivalent}}$ will be representative of an increase in C_{Tn} and, therefore, the amount of DNA in the aqueous sample.

4.3 Experimental Results

4.3.1 Model Validation and Sensor Characteristics

To validate the proposed model, we have used the parameters given in Table 4.1 to calculate Coffset-sub and Coffset-dir of the electrode to be 77.135 fF and 2.53 fF, respectively, using equations 4-1 and 4-2. The measured capacitance when there is no sample on the electrodes, CIDE, is equal to Coffset + Csens. From 4-3, $C_{\mathrm{offset-fringe}} = \varepsilon_{\mathrm{Sio_2}} \times C_{\mathrm{sens}}$. Using the technique described in Section 4.4 , we have performed multiple measurements on all our chips to obtain CIDE as shown in Table 4.1. These values have been used to calculate the average of deff-air to be 16.5 μm which is higher than the pitch of the IDEs, 12 μm, and thus is a meaningful result. To obtain the level of noise and uncertainty, we repeated the CIDE measurement five times without putting any sample on the chip. The result is shown in Table 4.1. The average is 106.24 fF while the standard deviation, which is the resolution of the sensor is 0.5 fF.

Table 4.1: Dimensions of the implemented IDE and process parameters and CIDE Measured Value when there is no sample on the electrodes

Parameter	Value	Parameter	Value	Chip Number	C_{IDE} (fF)
A	7056 μm^2	ε_{Sio2}	3.9	1	106.8
PR	1200 μm	ε_{Air}	1	2	105.7
$P_{coinside}$	878 μm	ε_{AL2O3}	9.1	3	106.3
Space	12 μm	ε_{SiN}	7.9	4	105.9
α_1 = CM4FOX	0.006 fF/μm^2	d_{AL2O3}	5 nm	5	106.5
α_2 = CM4FOXF	0.029 fF/μm	$d_{SiO2\text{-}SiN}$	1 μm + 1 μm	Average	106.24
ε_0	8.8542 × 10^{-3} fF/μm	TH_E=*MET4Thickness*	1 μm	Standard deviation	0.5

4.3.2 DNA Sample Preparation and Experiment Protocols

Single-stranded DNA (ssDNA) salmon testes samples were purchased from Sigma-Aldrich (Product Number: D7656). In the first step, the main sample with the concentration of 10.0 ± 1.0 mg/mL DNA in molecular level water was diluted into five different concentrations of 45 ng/μL, 80 ng/μL, 117 ng/μL, 222 ng/μL, 287 ng/μL. Based on the manufacturer's information, the DNA strands anneal at room temperature and form double-stranded DNA (dsDNA). All the tests were performed at room temperature and the obtained dsDNA fragments were employed for the investigations using two independent protocols:

Protocol I: Firstly, a 1 μL droplet of the sample was pipetted on the sensor chamber using a 0.1-2.5 μL micropipette and was allowed to dry. After the complete evaporation, 1 μL of molecular-level water was placed on the sensor to wash the previous DNA sample. The water droplet was allowed to remain there for 30 seconds and then was removed without any pipetting or brushing process. This test was performed for all the concentrations with three repeats each. The results showed variation and insignificant repeatability. Then, we improved the accuracy of the test with some modifications: a 0.7 μL droplet of DNA sample was put on the sensor to remain there until complete evaporation. Next, adding 1.5 μL of molecular level water, pipetting it on the sensor at least 10 times and brushing were used for the complete removal of the DNA sample.

Protocol II: The possibility of sensing the accumulation of DNA for continuously added droplets of DNA has been investigated. A 0.7 µL droplet of 117 ng/µL was put on the sensor to evaporate. The second droplet was then added to the first sample without any washing process to increase the DNA concentration on the sensor. Five droplets were added to the sensor surface in a similar pattern and the results were analyzed.

4.4 DNA Measurement Results

Through the GUI, we performed a complete sweep of the reference capacitance, CR for each measuring cycle. The obtained curves illustrate the number of pulses with respect to the value of CR during the whole experiment. Depending on the wetness of the surface, different patterns were generated during the experiments discussed in Chapter 2. The GUI demonstrates the curves in a time-based manner resulting in the generation of a 3D time-resolved illustration of the experiment. These 3D curves are shown in Figure 4.4 (a) and (b) for the DNA sample and water, respectively. As seen in these figures, the two 3D patterns are considerably different for water and DNA. Figure 4.4 (c) illustrates a microscopic image of electrodes after a DNA experiment where DNA remnants are formed after the complete evaporation of sample water. Figure 4.4 (d) shows a microscopic image of electrodes after a water experiment. As expected, there are no remnants after evaporation of pure water. Precise extraction of the value of capacitance from the 3D curve relies on the circuit's working principle at the equilibrium point, where capacitance on the sensing side, CS is equal to capacitance on the reference side, CR. Under this condition, the output of the chip (number of pulses) will maintain the same value regardless of the absolute value of CS and CR. To benefit from this, an on-chip poly capacitance with a nominal value of 400 fF has been connected in parallel with the IDE through a transmission gate connected to the IDE

(see Figure 4.3). This topology plays a role in the precise capacitance measurement with the steps summarized below.

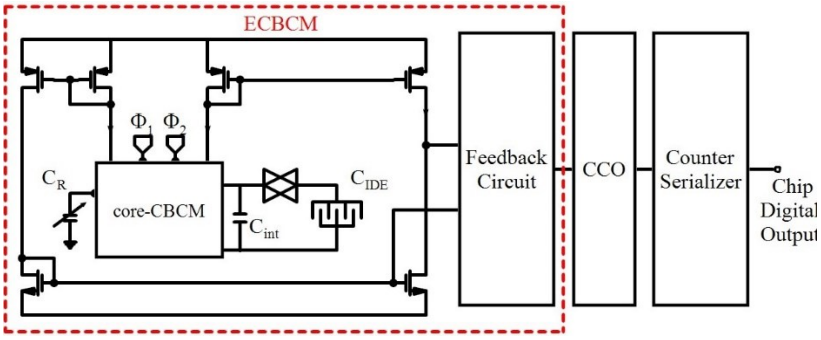


Figure 4.3: The transmission gate implemented in the ECBCM block

Switch off the transmission gate and obtain the output curve versus the value of sweeping reference capacitance (number of pulses versus CR);

Calculate the output of the chip for CR=400 fF;

Turn on the switch and obtain the number of pulses versus CR curve;

For the calculated output at stage (2), calculate the amount of shift to right. The shifted value is $C_{\text{equivalent}}$ ($C_{\text{equivalent}}$ represents the offset capacitance of the IDE as well as the capacitance change due to the alternation in the capacitance of the sample and the IDE interface).

Figure 4.5 provides a visual demonstration of this algorithm. This algorithm has been used to extract the capacitance value from the 3D curves for all of the experiments of this work. The extracted values from each of the 3D curves shown in Figure 4.4 (a) and (b) are demonstrated in Figure 4.5 (e) for DNA samples and water samples. This figure illustrates the key measurement technique that has been proposed and utilized for the DNA dry mass measurement in this work. Four distinguished phases can be seen. Phase A is before the deposition of the sample on the chip. Thus, the extracted capacitance in this phase acts as a baseline of the sensor at the beginning of the measurement. B illustrates the phase where the droplet is present. The presence of the water-based solution with a high dielectric constant

of about 80 results in a very high saturated capacitance. To distinguish between this saturated value and the sensor measurement values, we have shown the capacitance of phase B with zero. Phase C represents the transition from wet to dry as the droplet starts to complete its evaporation. Phase D is when the evaporation has been completed and the surface is void from moisture and as a result, the reading of the sensor goes back to the baseline.

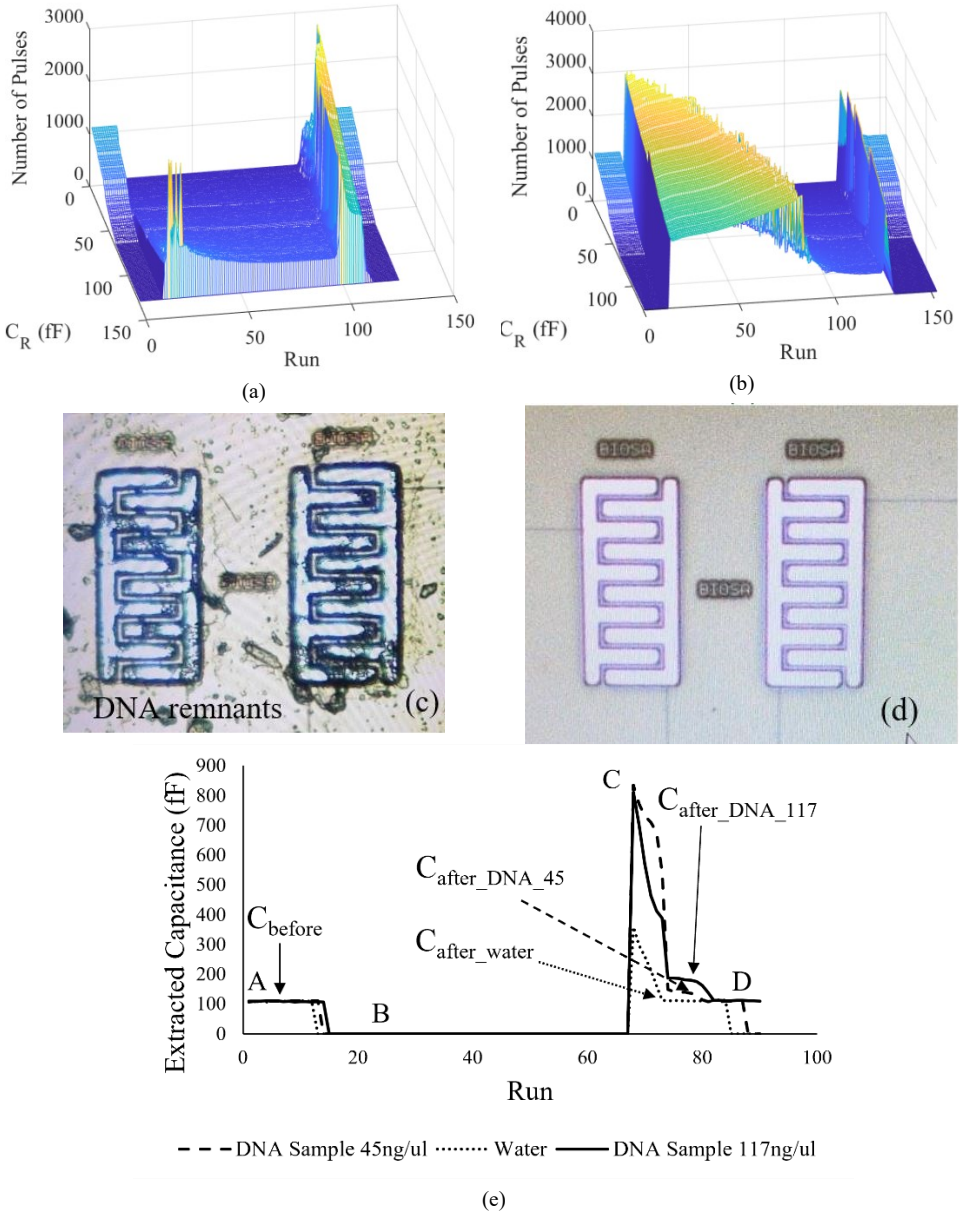


Figure 4.4: (a) The 3D output from the GUI for DNA droplet with a concentration of 45 ng/µL from introduction to complete evaporation, (b) The 3D output from the GUI for water droplet from introduction to complete evaporation, (c) Microscopic image of electrodes after a DNA experiment, (d) Microscopic image of electrodes after water experiment, (e) The extracted capacitance from the 3D curve based on the algorithm explained in Section IV.C for

DNA droplet of 45 ng/µL, DNA droplet of 117 ng/µL and water. From the extracted capacitance, the wet, dry, and transition phases are distinguished as B, C, and D, respectively. Points at the onset of the complete dry phase have been chosen for comparison with the baseline, shown as A.

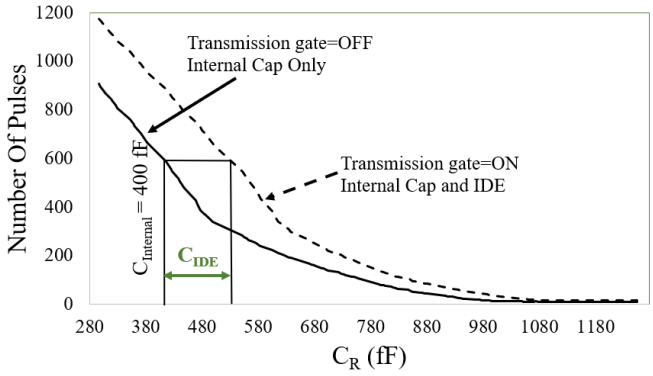


Figure 4.5: Visual representation of measuring C_{IDE}.

The average value of the extracted capacitance in the baseline (A), shown in Figure 4.4 (e), has been considered as Cbefore, and the capacitance at the onset of complete evaporation of sample solution, as shown Figure 4.4 (e) in phase C, has been considered as Cafter. The difference between the Cafter and Cbefore has been considered an indicator of the value of the deposited DNA mass. The experiments have been done using two different protocols, explained in Section 4.3.2 as Protocol I and Protocol II, to test the device and show the applicability of the CMOS capacitive sensor for dry DNA mass detection. The main difference between the protocols is the addition of a washing step and a water droplet test between each DNA sample measurement in Protocol I. The water droplet test has been considered as a reference for comparison. Figure 4.6 shows the difference in the change of capacitance after and before DNA samples, (Cafter – Cbefore), with that of water when employing Protocol, I for different concentrations. Each of the five different concentrations has been repeated five times. All experiments demonstrate an increase because of the accumulated DNA in the dry phase and the back-to-baseline trend. The pattern of change shows an increase in the measured differential capacitance for higher DNA concentrations. A slight error from the ideal linear trend for concentrations 117 ng/µL, and 222 ng/µL can be observed for practical reasons that have been discussed in Section 4.4.1.

The extracted capacitance results for Protocol II have been shown in Figure 4.7. A consistent and meaningful trend in the change of capacitance was not observed using this protocol for practical reasons that have been discussed in Section 4.4.1. In summary, all experiments using Protocol I showed a meaningful increase in capacitance because of the deposition of DNA on the electrodes compared to water tests with values above the minimum detectable capacitance change of 0.5 fF. This showed that DNA remnant increased CIDE proportional to the amount of remaining DNA mass. In addition, after each time washing, the capacitance returns close to the baseline value that shows the removability of remnants during the washing procedure.

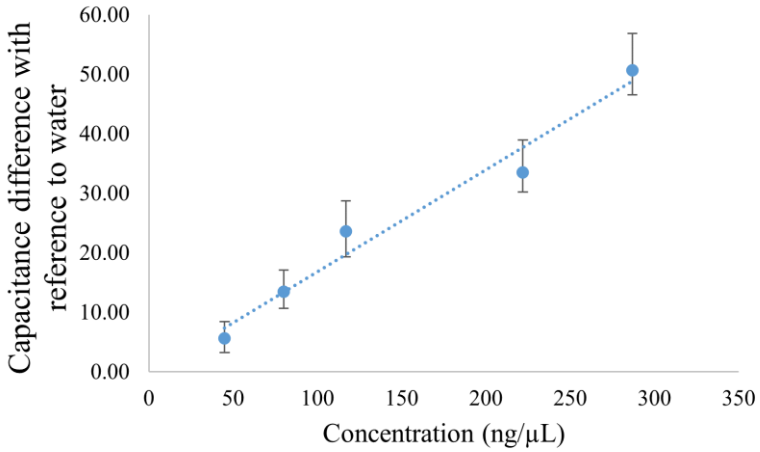


Figure 4.6: The transfer function obtained based on the difference in the change of capacitance after and before DNA samples, ($C_{after} - C_{before}$), with that of water when employing Protocol I with different concentrations.

4.4.1 Practical Considerations

In Figure 4.6, we can see variations from the linear pattern and some overlapping error bars. Multiple factors in the experimental procedure can be reasons for such discrepancies. First, the volume of the sample that has been manually put on the chip via a micropipette can slightly vary for different runs for both DNA and water samples. This in turn can alter the final amount of DNA sedimented on the electrodes. We can address this issue in the

future using proper microfluidic technology to precisely direct the sample toward the sensing site. The evaporation can also be considered as an error factor; however, in this technique, we monitor the capacitance over a range of time, so that the capacitance will be measured before full evaporation using the 3D profiles shown in Figure 4.4 (a)-(b). Another source of error can be due to the protocol of introducing the sample (see Protocols I-II, Section IV.D). In this work, Protocol I demonstrated a better performance because the washing of the surface of electrodes using pure water prevents the accumulation of errors caused by remnants. Temperature can also slightly change the output of the sensor, as discussed in Section 2.4.6.2. Figure 4.8 illustrates another simulation result for the ECBCM at three different equilibrium points when the capacitance on the sensing and the reference side are 10 fF, 300 fF, and 700 fF. As shown in the curve the output of the first stage decreases by 5.6% due to a temperature change from 0°C to 60°C.

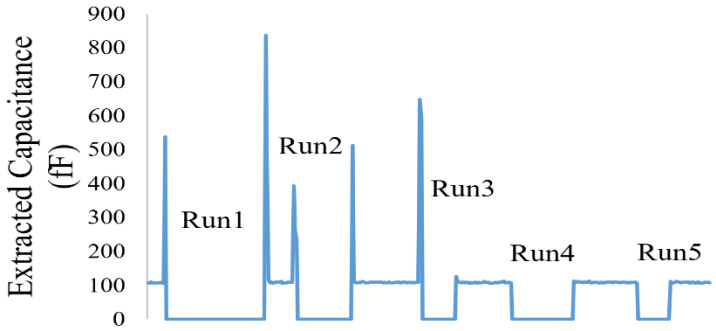


Figure 4.7: The extracted capacitance for the five continuous runs. The patterns reveal inconsistency in the shapes.

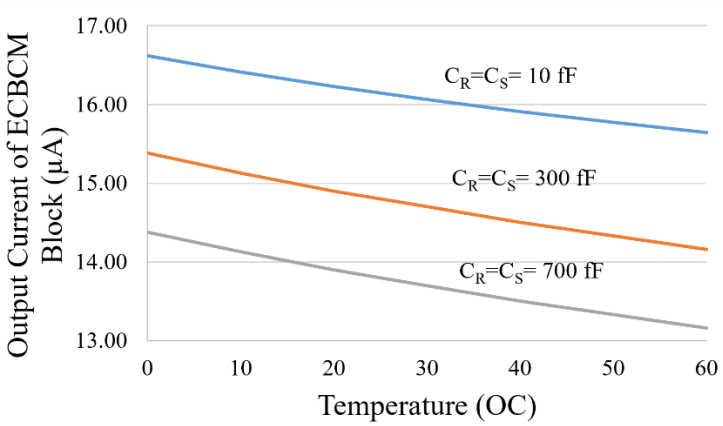


Figure 4.8: Simulation results for the temperature sensitivity of the ECBCM (the analog) block of the sensor. The digital blocks including CCO and the counter-serializer do not show any sensitivity.

4.4.2 Comparison with the State-of-the-art Sensors

Table 4.2 gives a comparison of our work with the state-of-the-art sensors in the literature. Our sensor shows the capability of detecting DNA in the dry phase which is crucial for DNA measurement in future integrated DNA data storage systems. In addition, no surface-functioning material is used to absorb DNA strands. Besides, a sub-microgram mass of DNA can be detected. The sensitivity and the resolution of the sensor for the detection of a minimum of 45 ng/µL have been verified. In addition, the results show that the sensor is sensitive to DNA remnants with acceptable repeatability. As seen in Table 4.2, the main difference between our sensor and other CMOS-based DNA sensors is that the proposed sensor can measure DNA mass without the need for immobilization or surface modification in the dry phase whereas the other DNA sensors, that have used CMOS sensors, are based on DNA hybridization and need probe immobilization, even [136] which is reported for mass detection in dry steady states. To the best of our knowledge, this is the first immobilization-free CMOS capacitive sensor that is reported for detecting DNA mass in the dried sample. There are several drawbacks to immobilization including higher complexity, more cost, and shorter lifespan due to the presence of active biological material

on the sensor. On the other side, to detect each type of DNA, a specific type of immobilization material must be used that can be a limiting factor for versatility and the use of the device in general-purpose memory applications with different types of DNA used as a storage material. In addition to that, the wide dynamic range of our device paves the way for an extended range of measurements for higher concentrations. The concentration range of 45 – 287 ng/μL has been tested here as a typically reported range of concentration for the existing DNA storage memories.

4.5 Summary

This chapter demonstrated the applicability of the sensor explained in Chapter 2 for monitoring dried DNA mass for DNA-based data storage systems. Among the different blocks of such systems, monitoring for the dry DNA storage part was the focus of this chapter. The proposed sensor has paved the way for high-precision, direct, and rapid monitoring of the DNA mass dried on the storage pools. Furthermore, integrating the required sensor along with other signal processing circuits on a single chip is a step toward the miniaturization of the interface circuits required for emerging DNA memories. The sensor works without the need for surface functionalization material and the sensitivity to detect a minimum of 45 ng dried DNA was verified and shown by experimental results.

Table 4.2: Comparison of different CMOS-based label-free DNA sensing devices

Sensing parameter	Surface material	Imm.	Probe concentration	Target DNA (bases)	Target DNA concentration	Pixel size	Tech. (µm)	Power	DR	Chip area (mm^2)	Sensitivity (resolution)	Ref.
Impedance	Au	Yes	7×10^6 per electrode	30	1 ng/µL	90 µm × 90 µm	0.35	84.8 mW @ 3.3 V	97 dB (BW=10 Hz)	2 × 2	330 pA @ BW=10 Hz (10 nS)	[142]
Surface stress/ Mass (in dry phase)	Au (Cantilever)	Yes	NA	19, 20	1 pM-10 nM	L/W/H= 150/ 40/ 3.26 µm	0.35 (CMOS-MEMS)	1 mW @ 3 V	<0.6 Ω	30.4	2 kHz/Ω	[136]
Capacitance	Au (IDE)	Yes	NA	25	NA	200 µm × 200 µm	0.5	NA @ 5 V	330 pF-10 nF	28.8	23 Hz/pF @ 7.5 kHz @ 330 pF	[8]
Capacitance	Au	Yes	NA	20	100 µM-1 M	4 µm × 4 µm	1.2	NA	10 - 1000 fF	0.5 × 1	NA	[103]
Capacitance and the charge-transfer resistance	Au	Yes	50 µM	18	1 µM	170 µm × 80 µm	0.35	NA	5 pF to 10 nF	10	NA	[101]
Capacitance	Au (IDE)	Yes	NA	21	100 pM-1 µM	L=350 µm, S= 20 µm	0.35	2.34 mW @ 3.3 V	94.6% @ 1 µA, 1 kHz	4 × 5	1.69 pulse/ pF	[138]
Capacitance	Al/SiO_2 (IDE)	Yes	10 µM	20	1 fM-10 fM	20 µm × 20 µm	0.35 (2P4M)	NA	NA	NA	NA	[139]
Capacitance	Al/SiO_2 (IDE)	Yes	10 µM	19, 20	10 aM-0.1 nM	30 µm × 30 µm	0.35 (2p4M)	NA	NA	NA	NA	[134]
Capacitance (in dry phase)	Al/Al_2O_3 (IDE)	No	NA	NA	100 – 400 ng/µL (= 0.1 µM – 0.64 µM)	110 µm × 220 µm	0.35	29.91 mW @ 3.3V	>400 fF	1 × 2	2 pulse / fF	This work

Imm.: Immobilization, Tech.: Technology, IDR: Dynamic range, Res.: Resolution, NA: Not available, L: Length, W: Width, H: Height, IDE: interdigitated electrode, BW: Bandwidth

Chapter 5: Detection of Oral Cells in Saliva Samples

In this chapter, we address the detection of oral cells including neutrophils and epithelial cells using the CMOS capacitive sensor. The detection of these cells in a non-culture environment has been shown for the first time. The contents of this chapter have been published in Bioengineering journal with the title of "Oral cells-on-chip: design, modeling and experimental results" [80].

5.1 Abstract

Recent advances in periodontal studies have attracted the attention of researchers to the relation between oral cells and gum diseases. A rapid and accurate assessment of these cells using integrated circuits and sensing technologies such as CMOS chips allows for the early detection and control of these diseases. This chapter presents the CMOS capacitive sensor proposed in Chapter 2 as an alternative hand-held device for current bench-top instruments for the analysis of salivatory cells such as oral neutrophils. The experimental and simulation results demonstrate the functionality and applicability of the proposed sensor for monitoring oral cells in a small volume of 1 μL saliva samples. These results reveal that the hydrophilic adhesion of oral cells on the chip alters the capacitance of IDEs. The presented results in this chapter set a new stage for the emergence of sensing platforms for testing oral samples.

5.2 Introduction

Recent periodontal research studies have found a correlation between gum diseases and other conditions such as diabetes, osteoporosis, and human immunodeficiency virus (HIV) [125], [143], [144]. For instance, it is well documented that patients with severe osteoporosis will likely experience periodontal breakdown [145]. There are also reports regarding the increased populations of periodontal-related bacteria in patients with HIV [146], [147]. Moreover, there is a high risk of heart disease in people with unhealthy gums which is a result of bacterial infection in the bloodstream [148], [149]. Also, recent studies show a link between salivatory oral cells such as Oral Polymorphonuclear Neutrophils (oPMNs) and gum diseases [150]–[152]. Indeed, the quantification and analysis of oral cells can improve our understanding of the cellular activities in saliva and might deliver a clear picture of oral health. For example, it has been verified that the number of oPMNs in patients with periodontitis is 4 times higher in comparison to healthy individuals [153]. The presence of an excessive number of oPMNs might have a negative impact on the oral tissue's integrity [154]. As a result of periodontitis and chronic activation of oral neutrophils, there might be damage to the periodontal connective tissue which leads to the loss of attachment, alveolar bone, and tooth loss [155].

Another example is a link between the epithelial cells derived from oral cavities and oral health. As per recent studies, epithelial cells contain biomarkers for oral diseases such as oral cancer [20,21]. These research findings further show the importance of oral cell analysis using advanced sensing technologies to improve our understanding of the role of salivary cells in the gum and other inflammatory diseases [156], [157].

Until now, there has been no already-established sensing platform for analyzing oral cellular activities. Researchers employ standard methods such as fluorescence microscopic

and flow cytometry [158]. These methods need specialized equipment with tens of thousands of dollars, a costly service contract, and trained staff to operate them. Therefore, their use is restricted to well-funded laboratories [159].

Capacitive sensors are one of the popular CMOS biosensors reported to be advantageous for studying growth and other cellular activities [3]. In these applications, the cells are firmly attached to the surface through integrin-containing multi-protein structures [160]. But, there are some challenges related to studying oral cells and doing research on them [161].

Unlike other cells, oral cells have very low culture ability, thus, they have less affinity to the surface even if they are in a culture medium [162]–[164]. Although researchers have made some efforts to culture oral cells in the saliva medium or other similar mediums, it has not been quite successful [161]. In many experiments for culturing neutrophils, the cells have undergone apoptosis and died after less than an hour and their morphology has changed [161]. In most tests on periodontal diseases, normal saline was used to take samples and study saliva cells without culturing them. Oral cells should be studied in the most similar material to saliva in order to be alive during the experiments [165]. These cells cannot be cultured in an in-vitro environment because they have a concise life span [166]. It is worth mentioning that since oral neutrophils have been activated during their migration from blood circulation to the oral cavity, they cannot be divided anymore. So, they are in the last stage of their life cycle, and their nucleus cannot do cytokines as well [166], [167]. There are different types of CD markers on the surface of neutrophil cells that might be responsible for cell attachment. According to the literature, the essential CD markers accountable for cell attachment are Mac-1 (CD 11b and CD18) [163], [166]. These CD markers may increase the affinity of cells to the hydrophilic surface of the silicon oxide or aluminum

oxide above the CMOS chip. This chapter addresses the challenge of monitoring the hydrophilic adhesion using the CMOS capacitive sensing platform.

5.2.1 Related Works

To date, many papers have reported the advantages of CMOS capacitive sensors for monitoring the growth or proliferation of different types of cells. Some state-of-the-art sensors are compared in Table 5.1. Indeed, the reported capacitive sensors have benefited from high resolution and sensitivity. However, they have had low dynamic range, thus suffering from parasitic capacitances created due to the debris and other remnants above the capacitive sensor. In this chapter, we employ the CMOS capacitive sensor proposed in Chapter 2 for oral cell monitoring for the first time with different oral cell types in the sample. The experimental results agree with the proposed equivalent circuit and Multiphysics simulation results as discussed in Section 5.2.3. Furthermore, the sensing electrodes in this chapter and other reported papers include metal or metal oxides demonstrating hydrophilic properties suitable for measuring the hydrophilic materials such as oral neutrophils attached to the electrodes [168].

Table 5.1: Comparison of the capacitive sensors reported for cellular applications

CMOS technology	Type of cell	Electrode material	Resolution	IDR[1] (fF)	Reference
0.5 µm	hBC[2]	Al/1pass[5]	0.1 fF	25	[81]
0.35 µm	hOC[3]	$Al/SiO_2/Si_3N_4$	14.4 aF	12	[123], [124]
0.25 µm	*S.epidermidis*	Al/Al_2O_3	10 fF	NA	[68]
0.25 µm	*S.epidermidis*	Al/Al_2O_3	450 aF	57	[17]
0.18 µm	*E.Coli*	Al/wPass[6]	10 aF	7	[70]
0.35 µm	hLC[4]	Al/PEM[7]	10 aF	6	[3]
90 nm	hBC	AuCu	10 aF	1	[2]
0.35 µm	Oral cells	Al/A_2O_3	416 aF	400	This work

IDR1: Input dynamic range, hBC2: Human breast cancer cell, hOC3: Human ovarian cancer cell, hLC4: Human lung carcinoma cell, Al/1pass5: Al electrode with one passivation layer, Al/wPass6: Passivated Al IDE with a window in between the fingers, PEM7: Polyelectrolyte Multilayer

5.2.2 Oral Samples-on-chip

The addition of oral neutrophil samples on the chip mimics the three distinct states, (1) when there is no sample on the electrode, (2) when the sample droplet exists on the electrode, (3) after the evaporation of the droplet as shown in Figure 5.1 (a), (c), and (e), respectively. An equivalent capacitive model corresponding to each state is shown in Figure 5.1 (b), (d), and (f), respectively. The electric equivalent model for the state with no sample has been discussed in Section 4.2.2.1 in Chapter 4. As seen in the electric equivalent model given in Figure 5.1 (d), due to the high conductivity of the sample solution that contains ions, a resistive path forms between the electrodes, Rsol. In addition, a double-layer capacitance forms in the interface of the electrodes and the sample. The overall effect is saturating the sensor readings and showing the pattern for the highly conductive solution discussed in Chapter 2. Figure 5.1 (e) demonstrates the phase in which the sample has evaporated while some moisture remains on the surface and the cells are deposited. In this phase, cell remnants play the role of a third dielectric in the equivalent capacitance of the passivation layer. Since the sample solution has evaporated, the value of resistance, Rsol, is negligible. The amount of change in the total capacitance of the electrodes in the presence of cells compared to the capacitance of the electrodes with no sample is related to the percentage of the area of the electrode that is covered by cells, referred to as confluence and discussed in detail in 4.2.3.

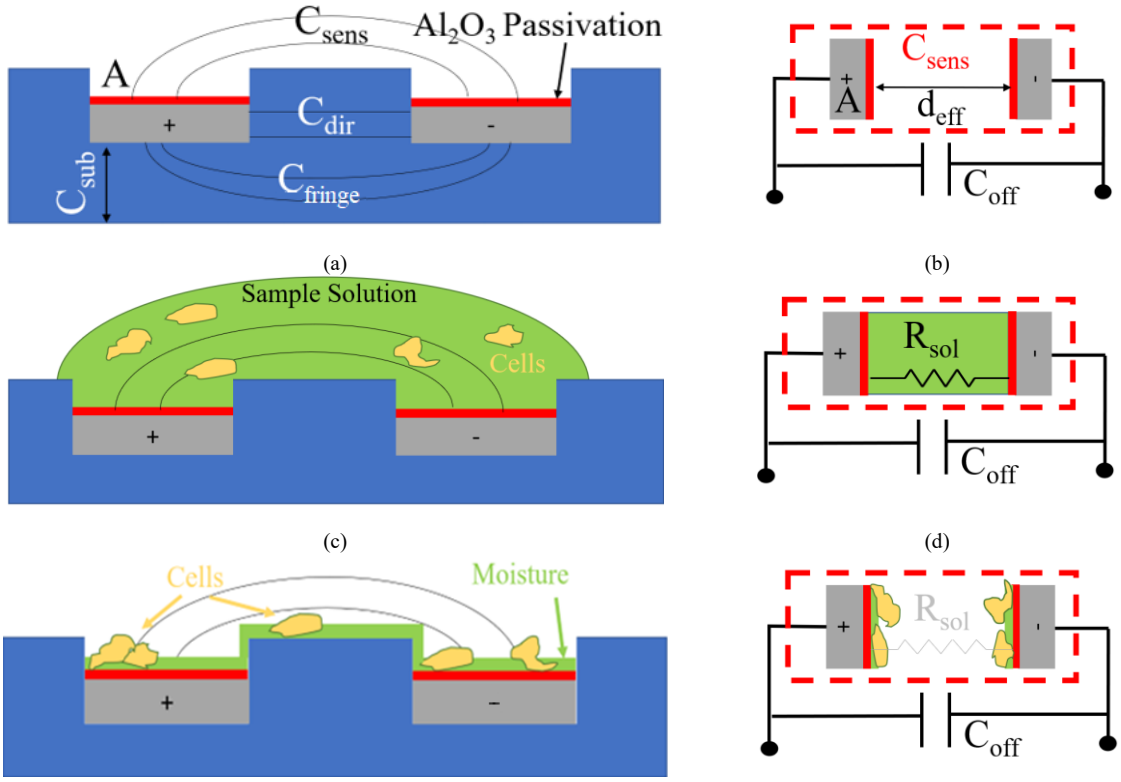
At the beginning of our experiments, to have a baseline, we perform a full reading of the sensor without introducing the sample. The readings reveal the Cdir+Cfring+Csub+Csens. Immediately after introducing the sample, the readings become saturated due to the presence of the water droplet. After the water droplet evaporates, the model enters the third state with moist cell remnants. In this state, the sensor readings reflect the amount of change in the Csens due to the presence of wet oral cells on the electrodes. The experiment results are explained in detail in Section 5.3.7.

5.2.3 COMSOL Simulation

In this section, the capacitive response of the electrodes is simulated for two modes: (1) In dry mode; and (2) when electrodes are exposed to cells in the water. In the wet mode, we also study the effect of the thick and thin layers of liquid. These simulations cover all three phases.

5.2.3.1 Dry Mode

A COMSOL Multiphysics simulation was carried out to model the CMOS capacitive sensor's static electrical response in the dry mode and when the sensor is subjected to a specific cell concentration. For this purpose, the sensor was modeled in the electrostatic module of COMSOL following the size and physical boundary conditions maintained in the fabricated sensor. In this module, the following formulas, 5-1 and 5-2, are solved numerically, which determine the sensor's electrical potential for measuring the capacitance.



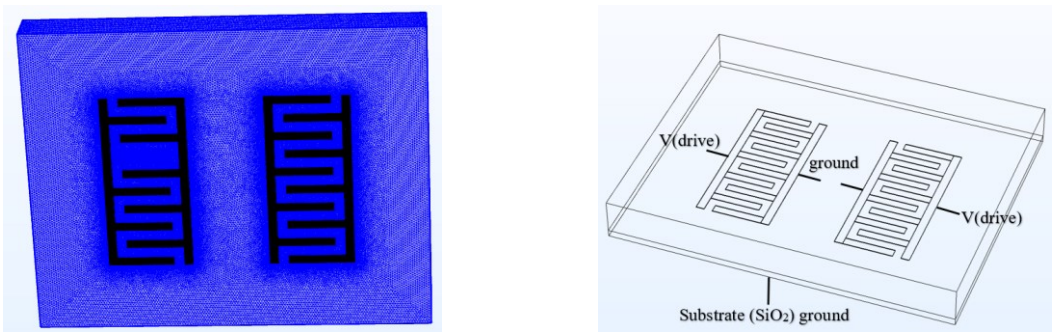
(e) (f)

Figure 5.1: (a) Cross-section schematic of the implemented IDE electrode without sample, (b) Equivalent capacitance model without sample, (c) Cross-section schematic of the IDE electrode with the sample before the evaporation of the sample solution, (d) Equivalent capacitance model the sample before the evaporation of the sample solution, (e) Cross-section schematic of the IDE electrode with the sample after the evaporation of the sample solution, (f) Equivalent capacitance model the sample after the evaporation of the sample solution.

$$E = -\nabla V \quad 5\text{-}1$$

$$\nabla.(\varepsilon_0 \varepsilon_r) = \rho_v \quad 5\text{-}2$$

where E is the electric field; ε_0 denotes the vacuum permittivity; ε_r is the relative permittivity; ρ stands for the electric charge density, and V is the electric voltage. To perform the simulation, the sensor was designed in the CAD module of COMSOL and then meshed to perform numerical simulation. A mesh analysis was performed to avoid the meshing effect on the result; consequently, the extra-fine mesh was utilized. The relative permittivity was used as the dielectric model. A schematic of the boundary conditions and the meshed structure is demonstrated in Figure 5.2.

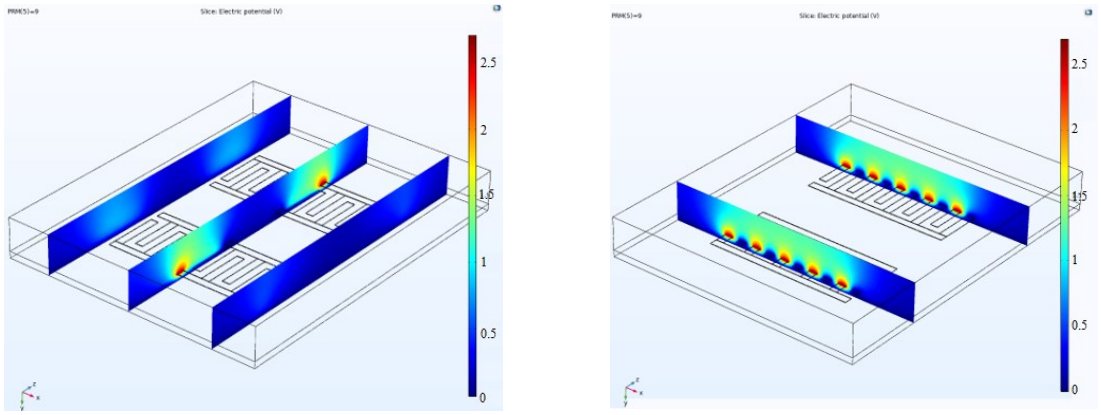


(a) (b)

Figure 5.2: (a,b) Boundary conditions and meshing structure of simulated sensor in COMSOL software.

Figure 5.3 demonstrates the electrical potential contours of the CMOS capacitive sensor when it is subjected to 2.7 V bias. The sensor was meshed with an extremely fine approximation to yield the best convergence. The sensor surrounding material is a thin layer of SiO2 identical to the CMOS fabrication materials. The simulation considers the capacitance due to the thin layer of SiO2 as the native material between the layers and the

P-type silicon substrate of the sensor which is electrically grounded. According to the simulation results, the equivalent capacitance for the sensor in dry mode is around 117.415 fF. The capacitance is calculated by assuming that the sensor is surrounded by air.



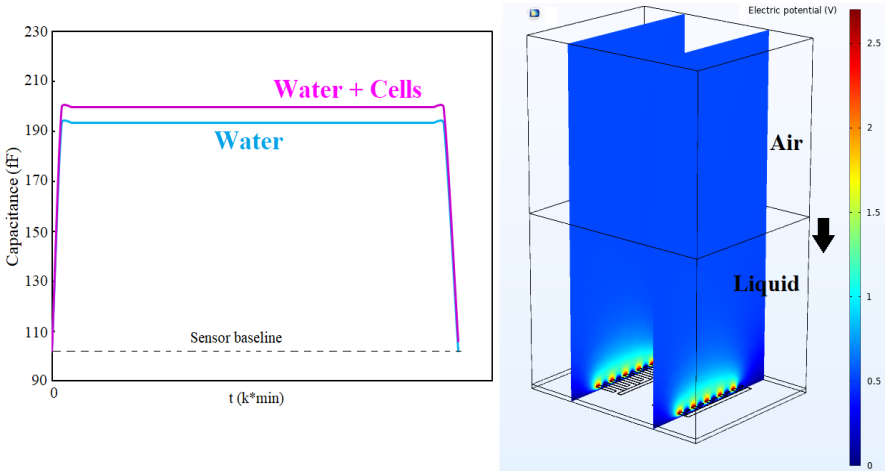
(a) (b)

Figure 5.3. (a, b) The electrical potential counters of the sensor for a bias voltage of 2.7 Volts. The substrate is grounded.

5.2.4 Exposing the Electrodes to Cellular Sample

According to experimental evidence, the capacitance upsurges when exposed to a liquid volume. After complete evaporation of liquid on top of the sensor, the response gets back to baseline considering the presence of cells. This also occurs when the medium encompasses cells or other components. Due to a change in the medium's dielectric, the sensor response changes, and the cycle of rise-fall of capacitance would be different from the previous cycle with a different dielectric. To prove this observation and validate it, COMSOL Multiphysics was employed to simulate the cycle. Following experiments, in modeling, we filled the top of the sensor with a thick liquid layer (here water) below the air layer as can be seen in Figure 5.4. Afterward, we changed the thickness of the water layer from 400 µm to 5 µm atop the sensor. This gradual decrease of the water layer thickness resembles the evaporation of the droplet. At the same time, the capacitance of each step was recorded. As seen in Figure 5.4, the sensor initially gets saturated, and then after the complete evaporation of the droplet,

it returns to its baseline. However, we expect different levels in the return cycle due to the existence of remnants of cells on top.



(a) (b)

Figure 5.4. (a, b) COMSOL simulation showing the saturation of the sensor in liquids and returning to baseline.

As shown in Figure 5.4, the electric potential on top of the sensor is decaying with the distance from the sensor surface. If the sensor environment is filled with a liquid (with a specific dielectric constant), the sensor response reaches a saturation level and constant level. When the liquid is evaporating, the cells' concentration becomes more visible to the sensor by increasing the dielectric constant. Therefore, we can sense the mass of cells on the sensor surface. COMSOL simulation validates this idea that, with the capacitive sensor, we can measure the concentration of biological entities in the droplet by measuring the capacitance change during the sedimentation of cells on the sensor in a loop shown in Figure 5.4 and experiments.

5.3 Results

In this section, the biological and chemical protocols are described. Then, the experimental results are demonstrated and discussed.

5.3.1 Measurement Setup

Figure 5.5 illustrates the test bench prepared for the real-time data acquisition using the GUI and capturing images before and after cell experiments by employing the high-resolution reflective camera. Imaging the surface has been challenging for many reflective microscopes due to the partial encapsulation of the chip. We were able to utilize the reflective high-resolution camera of the prob station, TS200-SE. A micropipette was used to manually put 1 µL of oral cell samples on the chip.

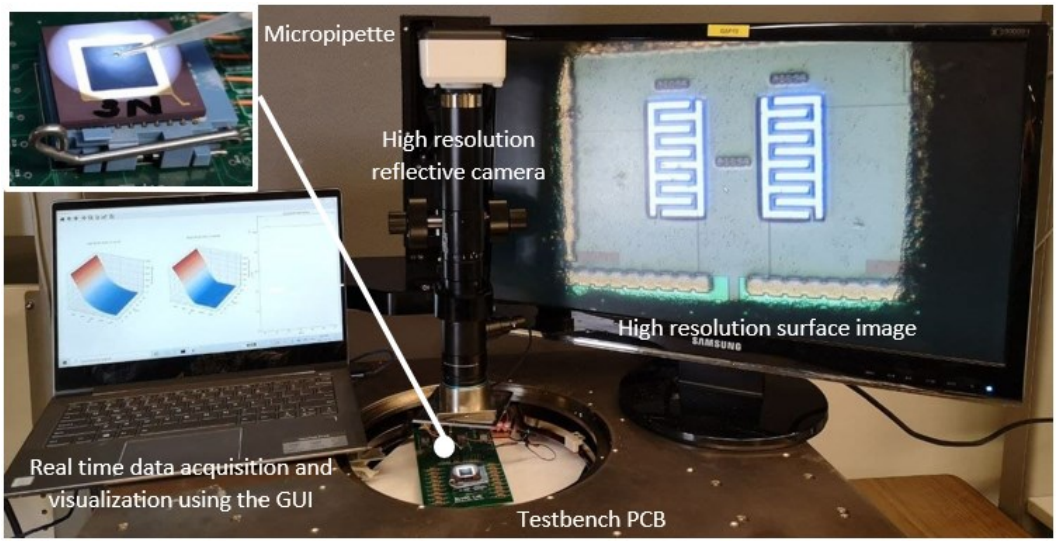


Figure 5.5. The prepared test bench for real-time data acquisition using the GUI and capturing images before and after cell experiments using the high-resolution reflective camera.

5.3.2 Biological and Chemical Protocol

After introducing the employed materials and instruments in Section 5.3.3, the cleaning procedure is explained in Section 5.3.4. Then, the sample preparation protocol and control measurement techniques are described in Sections 5.3.5 and 5.3.6, respectively.

5.3.3 Materials and Instruments

In this work, various materials were used. These materials are 50 polypropylene conical tubes (Baxter, Toronto, ON, Canada); Sterile cell strainer: 40 μm nylon mesh (Millipore, USA); 11 μm nylon filters (Millipore, USA); 1.5 mL Eppendorf tubes (Fisher science, Canada); 0.9 % irrigation-grade sodium chloride solution (Baxter, Toronto, ON, Canada). We also employed several instruments, including an incubator (Heracell 150i, Thermo Fisher Scientific); Lab Centrifuge (Sorvall ST 8, Thermo Scientific); He-mocytometer (BLAUBRAND® Neubauer Millipore Sigma); Inverted and phase contrast Microscope (isherbrandTM Inverted Infinity, Phase contrast 10x and 20x, light splitter (100% or 20/80%), Fishers Scientific).

5.3.4 Cleaning Procedure

Although the goal in the field of CMOS-based biosensors is mass-production and designing single-use devices, it is important to wash and reuse them while they are still in the research stage. Because their cost is high when fabricated in limited quantity despite their cost-effectiveness in batch production [123]. To test the functionality of the device, we gradually increase the cell concentration in each step to observe the differences between the device's response to an increased number of cells. But to have a precise measurement, it is crucial first to clean the surface and reuse it for the subsequent trial. We tried drop-casting and dipping in washing materials such as acetone, isopropanol alcohol (IPA), and ethanol; however, this method did not completely clean the surface. Therefore, we applied mechanical force to remove the cell residuals. Using a micrometric brush and droplets of Ethanol or IPA approximately solved the problem, and the surface was cleared of biological remnants.

5.3.5 Sample Preparation

To prepare neutrophil samples, participants were advised to not to consume anything with water being an exception for 30 minutes before sample collection, rinse the oral cavity with 10 mL of tap water for 15 seconds, and discharge the rinsed fluid. The participants were asked to wait for 2 minutes before rinsing the oral cavity with 10 mL of a 0.9 percent w/v saltwater solution (normal saline) measured using 15 mL falcon tubes and then eject the sample into 50 mL falcon tubes. After one wash, there was a 2-minute wait time, and the same process was repeated five times. Then, the final sample was filtered gently via 40 □m filters to isolate the cells from the debris larger than 40 µm sizes. The tubes were centrifuged at 4°C for 5 minutes with 2600 RPM and the supernatant was discarded until 1 mL of the sample remained in the falcon tube. Then, 1 mL of ultrapure water was added to the falcon tube and mixed with the cells. The related ethical approval for this research, including the human participants, has been provided by York University.

5.3.6 Control Measurement Technique

Hemocytometry cell counting technique was used to control the measurement results. At this step, the sample was thoroughly mixed. The hemocytometer was washed and cleaned with 70% (v/v) ethanol and allowed to dry. The coverslip was washed with 70% ethanol, allowed to dry, and placed in the hemocytometer counting chamber. A pipette has been used to mix 10 µl of cells and 90 µl of Trypan Blue in 1.5 mL Eppendorf. Then, 10 µl of cell suspension was added to Trypan Blue under the coverslip on a hemocytometer. After 2 minutes, the cells were counted. We estimated that the number of neutrophil cells in each 10 µL of saliva sample was about 7. The number of epithelial cells was around 13 in each

microliter of the saliva sample. Figure 5.6 shows the microscopic images of the hemocytometer showing neutrophil and epithelial cells.

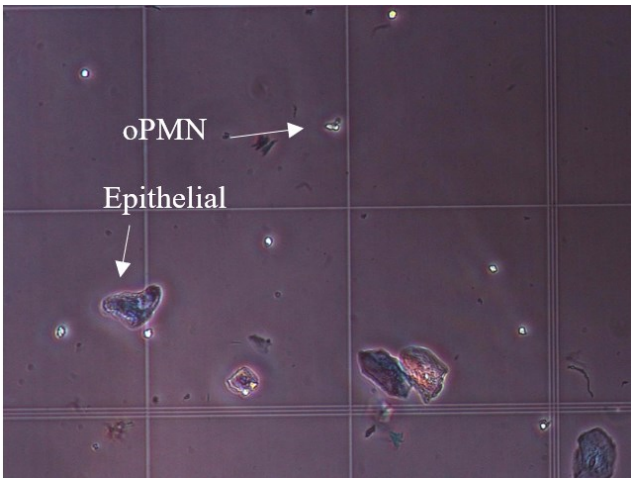


Figure 5.6. The microscopic images of the hemocytometer showing neutrophil and epithelial cells.

5.3.7 Oral Cell-surface interaction results

In this section, the capacitance measurement results are demonstrated in two phases: (1) wet phase and (2) dry phase.

5.3.7.1 Capacitance Measurement in the Wet Phase

In the beginning, the baseline of each electrode, which is a result of the inherent offset capacitance of the IDE, has been evaluated by obtaining the chip's output without introducing the samples. The output of the chip was obtained for the whole range of values of the bank of capacitors to have a reference point at all possible reference capacitance values. 1 μL of oral samples were placed on the electrodes. The presence of water on the non-passivated chips could increase the capacitance to a saturation level even for the highest value of reference capacitance. As a result, the data obtained before introducing the sample and before water evaporation was considered to determine the cell coverage on the

electrodes in the wet mode. The details of the extracted capacitance and the three phases are shown in Figure 5.7.

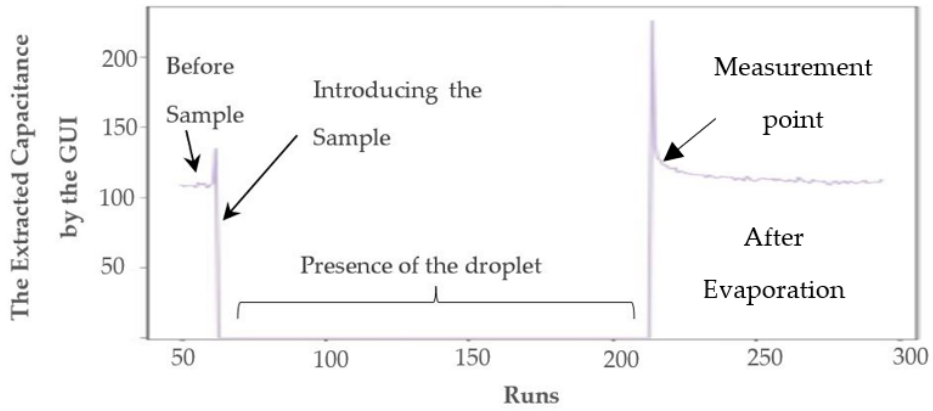


Figure 5.7: The extracted capacitance variations versus time.

Figure 5.8 (a) illustrates the microscopic image of the surface of the electrodes before the deposition of samples. The deposition of cells, including epithelial and neutrophil cells (shown in Figure 5.8 (b)) on the electrodes depends upon the hydrodynamic of the evaporation and the tendency of the cells to attach to the surface. Figure 5.8 (b) shows the microscopic images after the first trial. We put 1 µL of oral sample on the chip and waited until the preliminary water evaporation occurred to eliminate the effect of resistive path (see zero value, Figure 5.7) due to the high volume of ionic water. In Figure 5.8 (b), two different types of cells are recognized in the microscopic images. The smaller spherical cells are neutrophils, and the larger cells with nuclei are epithelial cells. Figure 5.8 (c) to (e) demonstrate the surface after the second, third, and fourth trials, putting 1 µL of oral sample on the chip and after partial evaporation. It is noteworthy, that the onset of evaporation is where the capacitance sharply drops, as shown in Figure 5.7. However, this is not the condition that the cells are completely dried.

Figure 5.9 demonstrates the magnitude of capacitance changes after each run with respect to the baseline before the first run (CAfterRun#-CBeforeRun1). The results have been obtained by performing the capacitance extraction procedure explained in Section 4.3.

By comparing the values of differential capacitance (CAfterRun#- CBeforeRun1) and the images shown in Figure 5.8, there is a correlation between the amount of cells that cover the electrode surface and the change in the capacitance. After the first run, there is some coverage of cells on both electrodes, with higher coverage on the left side electrode. The capacitance changes after the first run are about 26 fF and 9 fF for the left electrode and the right one, respectively. After the second run, There is more coverage of cells on the right side, and the capacitance change is approximately 32 fF for the left side and 43 fF for the right side.

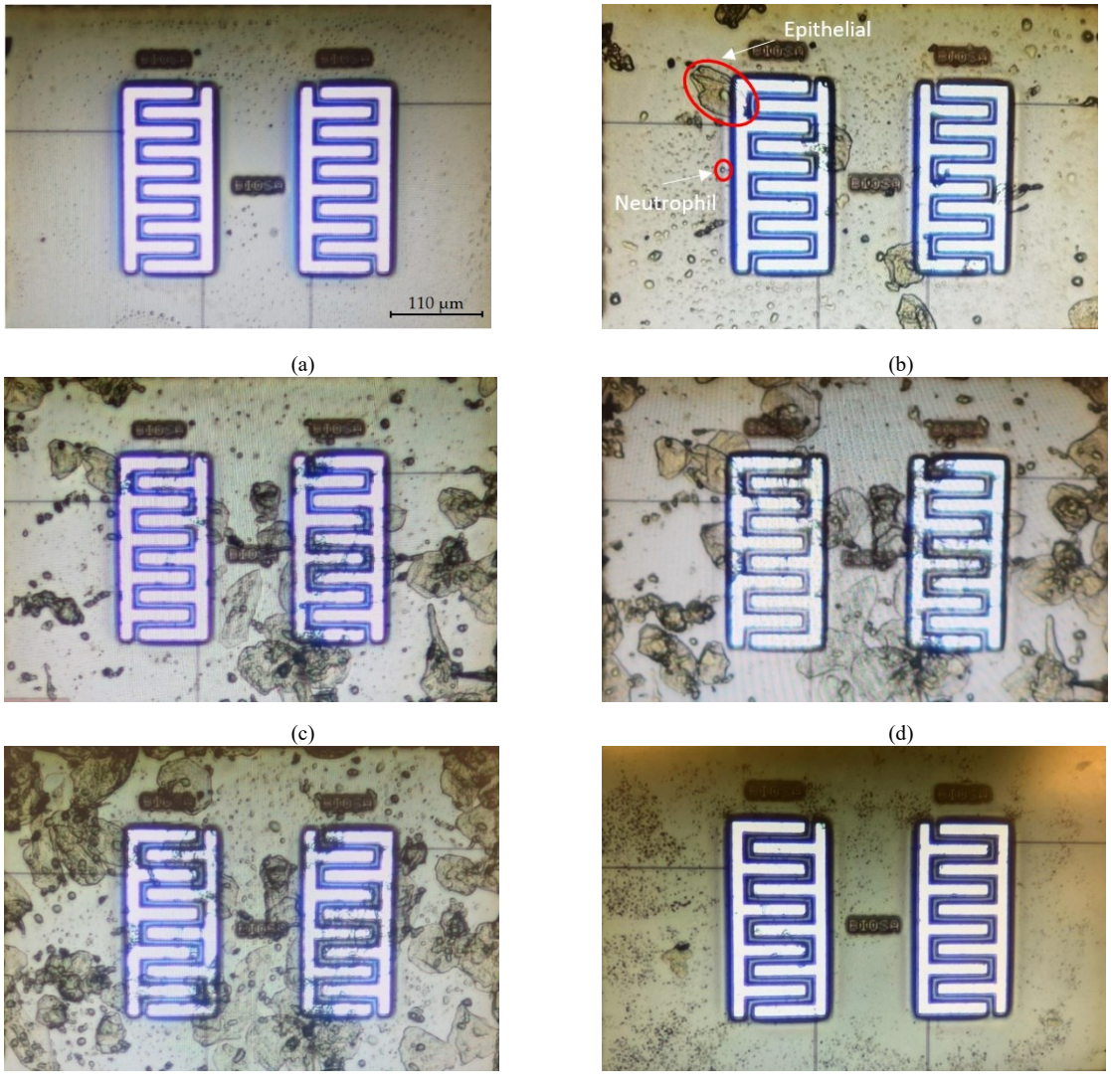


Figure 5.8. The microscopic image of the surface of the chip for the first experiment: (a) before putting samples, (b) after the first sample, (c) after the second sample, (d) after the third sample, (e) after the fourth sample, (f) after washing (The size of the electrodes is 220 µm × 110 µm which shows the scale of the images).

After the third run, cells deposited on the left side have increased as the capacitance change also shows a higher value for the left electrode after the third run, 57fF on the left compared 53fF on the right. After the fourth run, small amount of cells has covered both electrodes and the sensor readings are 61fF and 55fF for left and right respectively. This could be due to effect of the ions that were left on the electrodes. Figure 5.8 (f) illustrates the microscopic image of the chip after washing, and it shows that the cells have been successfully removed with the procedure explained in Section 5.3.4.

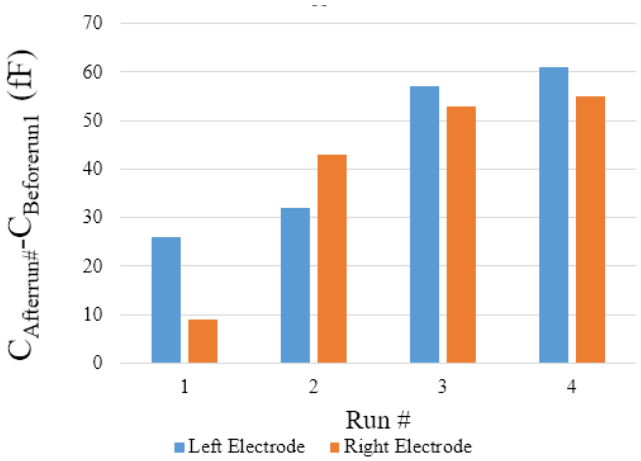


Figure 5.9. The difference between the capacitance after each run and the capacitance before the first run (fF) for four consecutive runs of the first experiment for the two electrodes.

5.3.8 Capacitance Measurement in the Dry Phase

In the second experiment, the output of the sensor was monitored until the surface was completely dried, and the output capacitance reached a steady-state value. In the first step, the sensor surface was cleaned with the procedure explained in Section 5.3.4 as shown in Figure 5.10 (a). Then, a new prepared sample was introduced to the sensor. The outputs were measured consecutively during two runs without any washing steps in between. Figure 5.10 (b) and (c) show the microscopic images of the chip surface after the first and the

second run, respectively. As seen in these figures, the coverage of the chip surface in Figure 5.10 (c) is more than in Figure 5.10 (b). Figure 5.10 (d) depicts the cleaned chip surface after the second run.

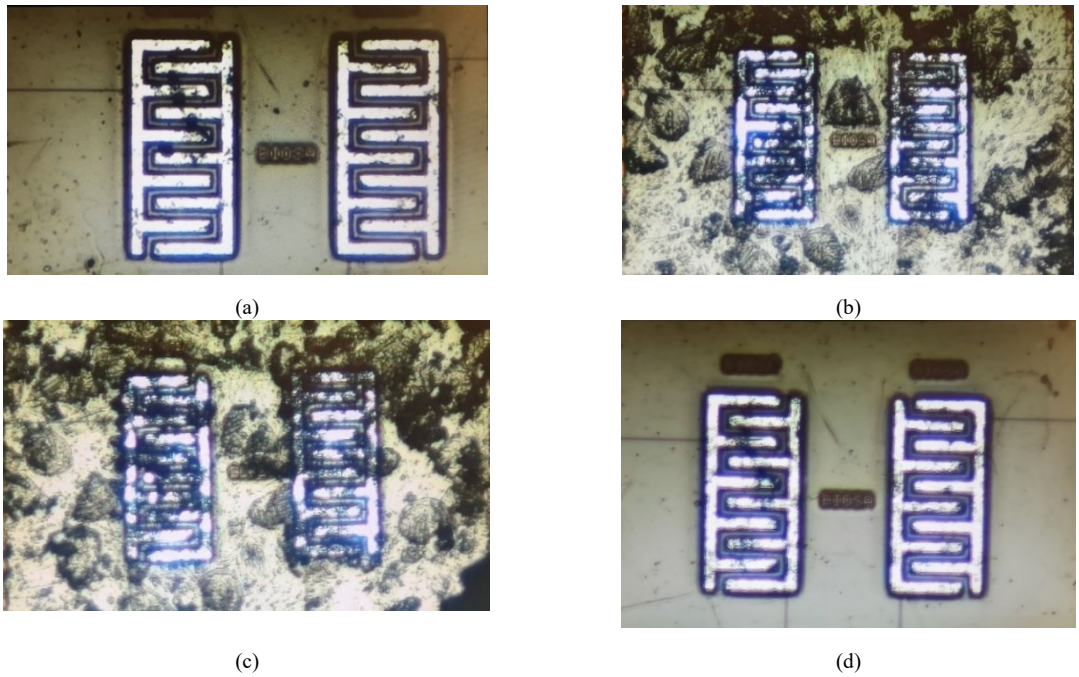
The experimental results almost agree with the COMSOL simulation results presented in Section 5.2.3. The experimental equivalent capacitance for the sensor in the dry mode when the sensing area is empty and surrounded by air is around 109 fF while the simulation has shown a capacitance of 117.415 fF for this condition. The small difference between these values can be because of the environmental issues in the real experiment, as well as the differences in the models of CMOS layers used in COMSOL in comparison to the fabricated circuit.

Figure 5.11 (a) and (b) show the capacitance variations versus time. Real-time measurement of the output during these two trials and after the washing procedure results in three groups of 3D profiles, as shown in Figure 5.12. Each group includes two 3D profiles for the two electrodes on the left and right.

According to the simulations, the sensor initially gets saturated by introducing the sample and then drops down during the evaporation of the liquid. As shown in Figure 5.11 (a) and Figure 5.12, the extracted capacitance and the digital output follow the same trend over time. As aforementioned, the saturation state due to the large capacitance of the liquid is shown by zero in Figure 5.11 (a) and Figure 5.12. During the evaporation of the liquid, the output decreases until it reaches a steady-state level.

Figure 5.11 (b) illustrates the steady states of the two trials, and after washing the chip surface. As seen in this figure, adding the new sample to the surface in run 2 without washing after run 1 results in an accumulative output which is higher than the steady-state level of run 1. More coverage of the electrodes by the cells, shown in Figure 5.10, has led to this

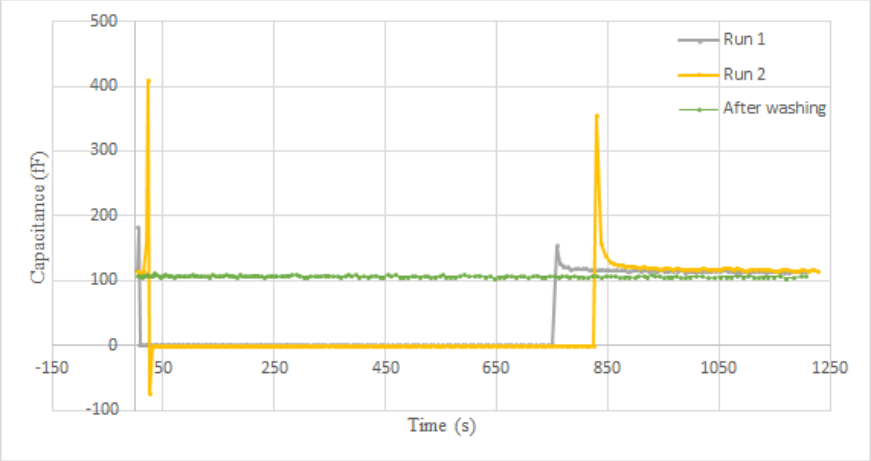
increasing trend for steady-state capacitance. Washing the surface causes the output to return to the baseline which is around 109 fF.



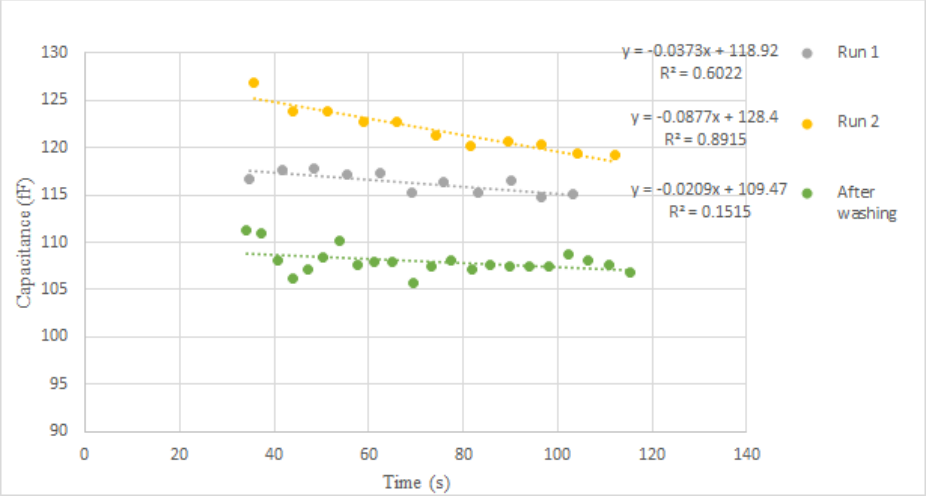
(a) (b)

(c) (d)

Figure 5.10. The microscopic images of the surface of the chip for the second experiment: (a) After washing and before run 1, (b) After putting the first sample (run 1), (c) After putting the second sample (run 2), (d) The cleaned surface after run 2.

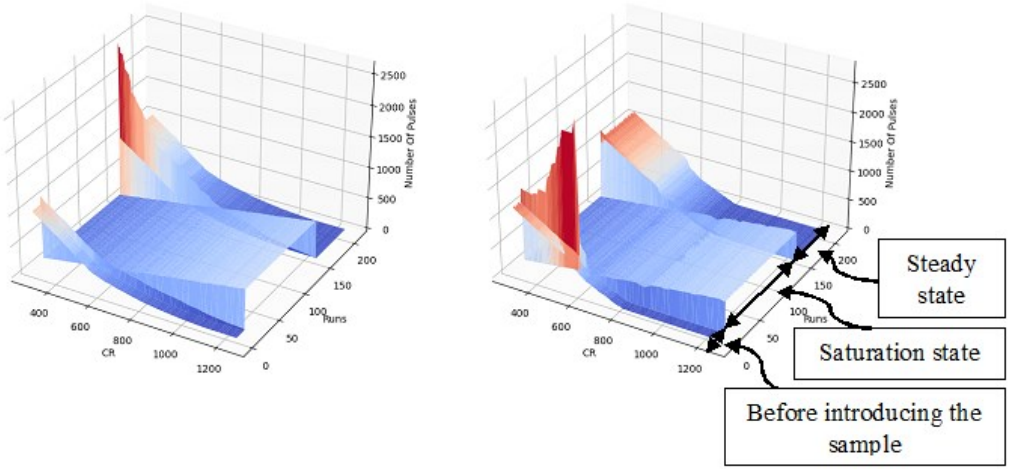


(a)



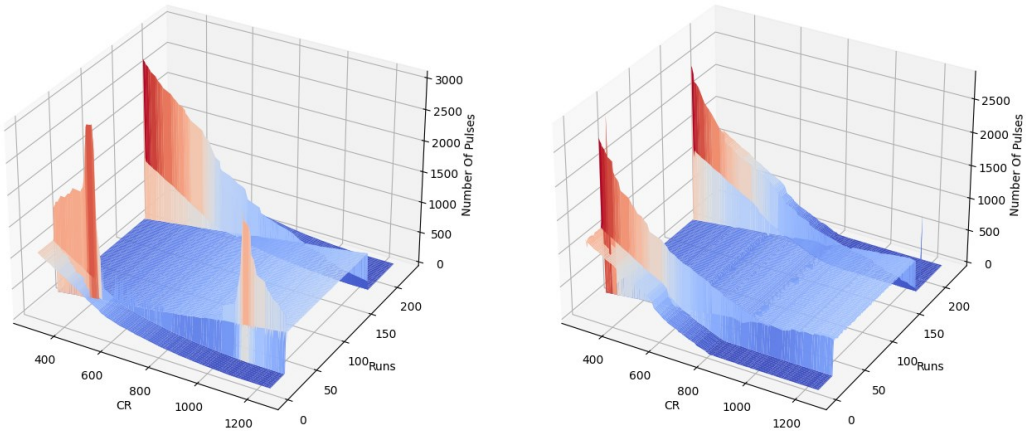
(b)

Figure 5.11. Real-time capacitance measurement result from the right electrode for the second experiment showing: (a) the baseline, the saturation state, the transient between the saturation and steady state, as well as the steady state (The saturation state is shown by zero in the figure), (b) Steady state (from about 30 seconds after the peak of the curves depicted in (a) for each run).



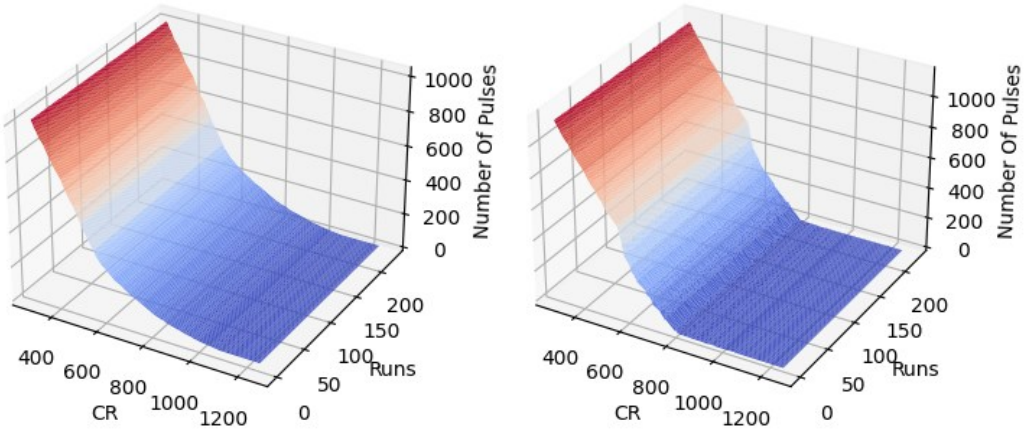
(a) (b)

Group 1: The first run



(C) (D)

Group 2: The second run



(E) (F)

Group 3: After washing

Figure 5.12. The 3D output of the chip for the second experiment for: (a) Run 1, left electrode, (b) Run 1, right electrode, (c) Run 2, left electrode, (d) Run 1, right electrode, (e) After washing, left electrode, (f) After washing, right electrode.

5.4 Discussion

In this chapter, we utilized the capacitive sensing platform for monitoring oral cells and likely, in the future, analyzing them to understand their links to inflammatory diseases. Herein, we demonstrated the presence of epithelial and neutrophil cells and their effects on capacitive sensors. This takes us one step closer to developing the capacitive sensing PoC device for monitoring and counting the cells. In this direction, there are several practical considerations to be addressed in the future, as discussed below.

5.4.1 Isolation of Cells from Saliva

Saliva is composed of 99% water and only 1% immunoglobulins, protein, mucus, enzymes, salts, and electrolytes such as sodium, potassium, calcium, magnesium, bicarbonate, and phosphates as well as different types of cells like epithelial cells or intact and lysed inflammatory cells specifically oPMNs [169], [170]. Herein, the standard filtering technique is used to isolate oral cells from saliva. Neutrophils can only be kept alive within a short time frame, and physical techniques are used to purify the sample. To develop a handheld sensing device for monitoring oral neutrophils, which are small, microfluidic techniques are also required to separate them from epithelial cells and the debris in the saliva. The more the purity of the sample, the more accuracy of the measurement result.

5.4.2 The Effects of the Evaporation of the Sample

As explained in Section 5.3.7, the measurement results depend on the evaporation of the sample. For a reliable measurement, a microfluidic device can be designed to direct the sample toward the sensing site and prevent or control the evaporation of the liquid.

5.4.3 Bubble Creation

Since pipetting the sample on the chip surface is done manually, some errors are inevitable. For instance, one of the practical problems during the experimental results was the creation of bubbles on top of the sensing area. This phenomenon results in a meaningless output, including fluctuations depending on the bubbles' presence or absence, as shown in Figure 5.13. Providing a microfluidic device to control and even automate putting the sample on the chip surface can help avoid bubble formation. In addition, microfluidics

makes it possible to put the sample on top of the sensing electrodes more precisely, leading to more accurate measurement results.

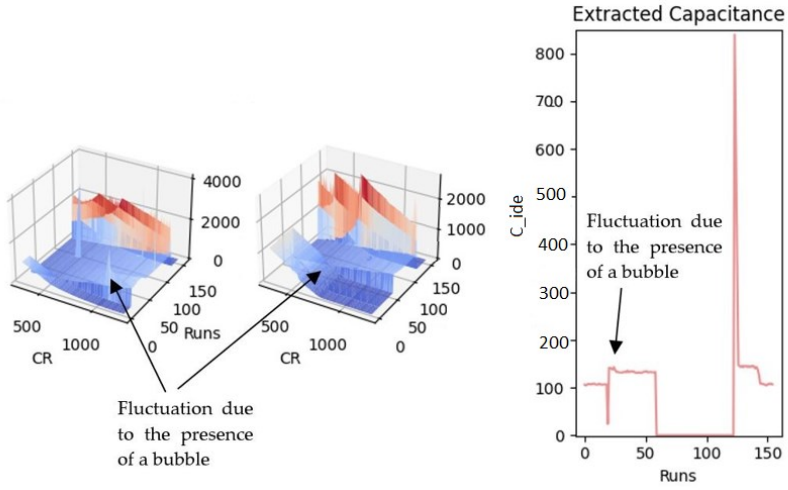


Figure 5.13. The fluctuated pattern due to the presence of a bubble created during sample placement.

5.4.4 Sensing Electrodes

The appropriate location of the cells on top of the sensing area and the amount of cell coverage can affect the measurement results. Since the electrodes do not cover the whole area of the substrate, the cells might be placed over the non-sensitive or less sensitive area, for example in between the electrodes. As a result, the sensor cannot sense them perfectly. To avoid such errors, a new integrated circuit is required whose electrodes cover the whole area of the substrate.

The size of the electrode can also affect its sensitivity. Although we almost cancel the offset in the proposed circuit, the value of the offset and parasitic capacitances might be higher than the sensing capacitance for too large electrodes resulting in a low sensitive measurement. If the size of the electrode is much bigger than the size of the cells, ΔC will be much smaller than C0 leading to a small ECR. On the other hand, although the smaller sizes of the electrodes help increase the ECR, we will need a large number of them to cover the whole area of the substrate so that the circuit can read their outputs in parallel. Herein,

we tested a two-electrode sensor with oral cells as a proof of concept. To further our research, we intend to present a new sensor composed of many electrodes for this application.

5.4.5 Read-out Circuit Specifications

Various factors such as parasitic effects, systematic errors, environmental factors, and experiment-time offset variation due to the remnants of the cells can create a time-variant offset capacitance that might saturate the sensor's output. So, the sensor should have a wide IDR to show the target cells' concentration. The proposed sensor had a wider IDR than the other reported capacitive sensors. In addition, the IDR of the sensor was programmable, and the employed calibration-free technique based on sweeping the reference capacitor paved the way to mitigate the effects of undesired time-variant offsets significantly.

5.5 Summary

This chapter demonstrated the applicability of the proposed CMOS capacitive sensor for monitoring oral cells in saliva samples. The capacitance of the on-chip IDEs was mathematically modeled by considering the existing parasitic and fringe capacitances. A COMSOL simulation was performed to qualitatively gain insight from the sensor response to the biological cells. Simulations were qualitatively in agreement with the experiment and confirmed the functionality of devices in terms of sensitivity to change in the dielectric of added material on its sensing surface. The difference between the capacitance values before and after water evaporation could represent the amount of electrode surface coverage by oral cells. By taking advantage of the wide IDR of the sensor and the programmable bank of reference capacitors, the accumulation of the cells could be assessed over four runs

without washing. To avoid the electrodes' conditions being manipulated after each run, no washing steps were applied to the electrodes exposed to the oral cells sample. The experiments showed that the accumulation of the cells after each run decreases the sensor's sensitivity. So, a cleaning procedure was employed to remove the cells from the chip surface. The results were encouraging regarding developing reusable, integrated sensing devices that can set the stage for quantifying and analyzing oral cells, including neutrophils and epithelial cells, in the future.

Chapter 6: Future Considerations

In this thesis, we reviewed several circuit and system topologies for CMOS capacitive sensors with a wide range of applications in life science. Many of these sensor systems have been shown to effectively detect the presence of bioparticles. Despite their ability to detect target molecules, practical challenges still existed. Despite the successful commercialization of some biosensors, such as IonTorrentTM, these practical issues were yet to be tackled for the employment of capacitive sensors in PoC diagnosis by the end users. Thus, in this thesis, we focused on the design and implementation of novel CMOS capacitive sensors intending to confront the existing challenges including limited IDR, offset problems due to remnants, and high-throughput differential capacitance to digital sensors.

After a literature review in Chapter 1, a new CMOS capacitive sensor was proposed in Chapter 2. The experimental results supported that the design objectives of higher linearity for the differential capacitive block and the high IDR were achieved. Furthermore, a measurement technique was proposed that could prevent the need for recalibration during the experiment. In Chapter 3, we introduced the array version of the proposed sensor with further design optimizations for precise high-throughput monitoring. The successful test and characterization of the array chip were presented using chemical solvents with different dielectric constants. In Chapter 4, a novel way of DNA nano-mass monitoring has been proposed that relied on measuring the nano-mass with the need for a recognition layer and DNA hybridization. In Chapter 5, the applicability of the proposed sensor for the detection

of oral cells outside of the culture medium was shown which could be used in hand-held devices for rapid diagnosis of periodontal diseases.

Four journal papers have been published from this thesis in IEEE TBioCAS journal, IEEE TIM Journal, IEEE Sensors Journal, and Bioengineering MDPI in addition to five conference papers.

6.1 Contributions

- A novel CBCM circuit with increased linearity of three times compared to the state-of-the-art sensors
- a new topology for conversion of differential capacitance to current and directly to frequency
- maintaining a high resolution of 0.5 ff
- a novel array structure with low parasitic effect due to the implementation of the multiplexing scheme on the clock signals
- addition of a programmable bank of capacitors as a reference capacitor
- proposing the calibration-free measurement technique to cover a wide range of remnants and sedimentation
- fabrication of two CMOS chips
- design and implementation of two full embedded systems including dedicated circuits, PCB, and GUI for each of the chips
- achieving a high-accuracy toolset for droplet analysis with the designed chips, PCBs and GUI
- characterization of the sensitivity using chemical solvents, ethanol, methanol, and water

- measurement of DNA nano mass without hybridization for ultra-low DNA concentration for DNA data storage memories
- quantification of deposited oral cells for diagnosis of periodontal diseases

6.2 Practical Challenges

6.2.1 Limiting factors for further improving

In the proposed ECBCM topology, the feedback that has been provided via the OpAmp has improved the range by increasing the linearity. However, with a larger range of differential input capacitance the OpAmp will be saturated. In addition, the design is based on a linear current controlled relaxation oscillator. There is a range of input current for the oscillator to act linearly and the oscillation either stops or enters a nonlinear mode outside of the linear range which is a limiting factor. The resolution of the sensor also depends on the frequency of the oscillator since smaller changes in the current can be detected with higher oscillation frequencies. To achieve higher frequency, the input current of the oscillator must increase which in turn can limit its linear range. We have optimized this circuit topology to maximize the resolution and dynamic range and further improvement might require changes in the topology.

The oscillator has reached a maximum of 300 MHz in this topology after minimizing the charge/discharge capacitor. Further decreasing the capacitor was not possible simply due to parasitic capacitors in the layout. In addition, around 260 μA input current, the oscillator starts entering the nonlinear region and its sensitivity to noise increases thus limiting the range of input differential capacitance.

6.2.2 limit of Detection

In the measurement of dried DNA and screening of orall cells there were practical difficulties resulting in reducing the limit of detection. One major problem was the hydrophilic area of the Silicon oxide and the hydrophilic area of electrodes. This causes a shear force from the electrodes towards the outer surface of the electrode which slightly repels the sample towards the edge of the sensing chamber. As a result, after evaporation of the sample, a large amount of DNA or cells were observed outside of the sensitive IDE area. In later designs this can be addressed by adding a customized passivation layer that has a hydrophobic property.

6.2.3 Number of channels and the readout speed

In the design of array of sensors, a single ECBCM circuit is shared for 128 IDEs to minimize the pixel area and thus a denser array and higher spatial resolution. As a result, there is only one digital output for all 128 channels. The downside of this topology is decreasing the readout speed by 128 times. With the 66 kHz clock it takes only 15 µs for reading each pixel and this time is a few milliseconds for all 128 pixels. Even though it is sufficiently fast for cell monitoring applications, for applications with faster dynamic such as dust screening it can be a limiting factor.

6.2.4 Process corners

As explained in chapter 2, the overall change in the output of the chip for fixed differential input can reach 61% as a result of worse case process corners. This problem can

be addressed by implementing the chip in higher feature size technologies such as 0.3µm or 0.6µm technologies which have smaller process variation.

6.3 Future Work

In this section, we focus on the areas in which the proposed capacitive sensors can be further developed toward being a candidate for commercialization. These developments can be foreseen in four major categories as discussed here.

6.3.1 System-Level Development

One of the side effects of a large array of electrodes is the increased time for data acquisition from all the electrodes. As reported in Chapter 2 and Chapter 3, our sensor has a fast response of 15 µs per measurement. In the scan mode, for a single electrode, the data acquisition time reaches 2ms per electrode in the ideal scenario when any overhead related to the transfer of data to a processing node, such as PC in this thesis, has not been considered. For instance, a complete transfer in the CR mode for a single electrode from the MCU to PC using UART port takes about one second. Transmission of data for our array chip takes about 7 minutes for all 256 electrodes where 1028 data points should be sent in the CR sweep measurement mode. Adding multiple read-out circuitry for parallel data acquisition can significantly contribute to the measurement speed. Moreover, adding a processor core with memory to the chip can be an important step for a larger array size. The presence of memory can significantly reduce communication overhead by buffering the data and sending a large packet size between measurements. In addition, the required signal processing such as µ average filters on the data and the extraction of capacitance from the

3D data can be done using the on-chip processor core which in turn can reduce the amount of raw data that is required for transmission.

Furthermore, the implementation of a reference voltage block and clock generator on the chip can help higher noise immunity. In our design, we have used external voltage references and PWM port of a general-purpose microcontroller for generating the required non-overlapping signals which are prone to higher levels of noise compared to on-chip blocks.

Figure 6.1 is a schematic of the proposed system-level improvements that can be made for a future CMOS ECBCM capacitive sensor. As shown in Figure 6.1, a set of IDEs can be connected to n number of ECBCM circuits to fulfill a parallel data acquisition to increase the speed. A processor core is responsible for the data acquisition and feature extraction in communication with a memory unit. The required supply and reference voltages can be supplied through a power unit. The necessary clock generation and clock gating can also be implemented on a unified block.

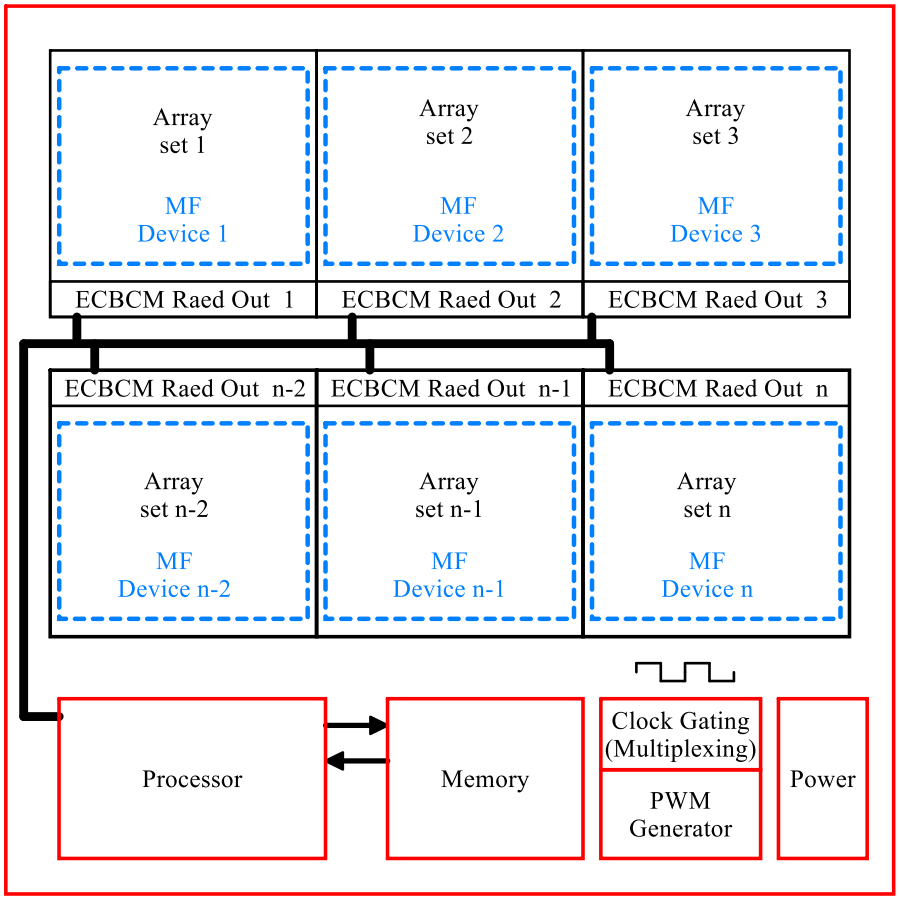


Figure 6.1: The Future of CMOS ECBCM capacitive sensor. MF stands for the microfluidic device.

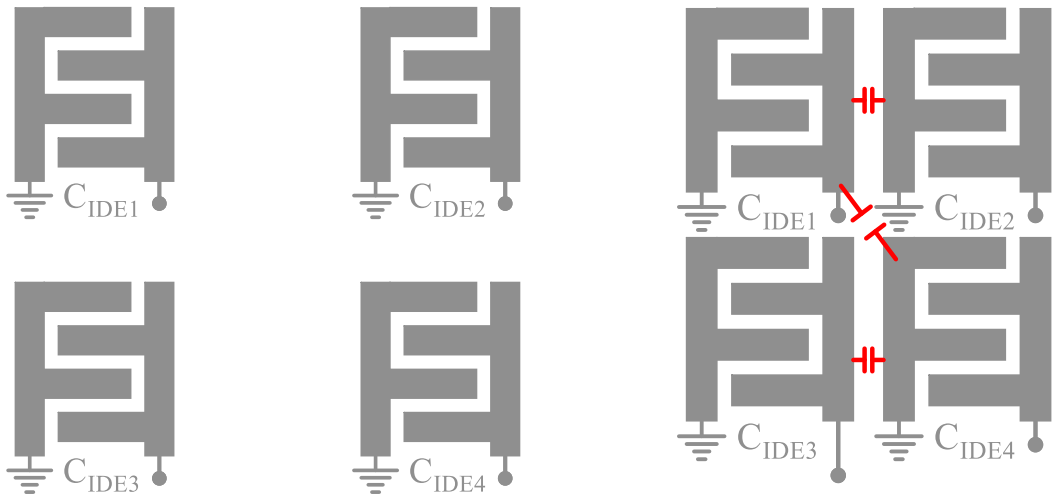
6.3.2 Circuit-Level Development

Despite the enhancements that were made to the ECBCM and the CCO circuit in the array design to achieve higher resolution, there is still room for further increase with a different CCO topology. A higher frequency of oscillation in a fixed measurement time can result in a higher resolution. Thus, developing new CCO topologies with high IDR and higher oscillation frequency can result in higher resolutions in future chips. The CCO of the array chip can reach up to 90 MHz when its input current reaches about 1 mA. Any CCO topology that can maintain the wide IDR and increase the oscillation frequency, therefore, can result in an increased resolution.

Another parameter is the resolution of the bank of capacitors. In the calibration-free measurement technique, discussed in Section 2.5, the obtained curves are the result of the sweep of the value of the bank of capacitors. As discussed in Section 4.4, the extraction of capacitance depends on the calculation of the shift of the curve in the horizontal axis. Thus, higher resolution in the steps of the bank of capacitors can result in higher accuracy in the calculation of the capacitance.

6.3.3 Higher Array Density and Accuracy

To achieve a denser array, the pitch of the IDEs can be considered to decrease. As shown in Figure 6.2 (a), there is space left between the IDEs to avoid any crosstalk between the cells. Especially, since the capacitance is measured based on the fringe electric field between the two plates of the IDEs, close IDEs can interfere with each other through parasitic capacitances shown in Figure 6.2 (b). In this case, cross talk of the sensors and added parasitic elements require further electric and electromagnetic simulation and modeling, for example in Sonnet software, to optimize the topology and reach the minimum possible pitch for higher spatial resolution.



(A) (B)

Figure 6.2: The pitch put between the IDEs in the array chip to any cross talk.

Another aspect of more accurate chips is to implement a mechanism for post-fabrication trimming to confront the effect of process variation. This can, for instance, be done by adding current mirrors with programmable gain at the input stage of the CCO for adjusting the threshold of the oscillation current. Regarding the design of the array chip, the process variation resulted in the creation of two different patterns at the output of the chip. More details can be found in Appendix I.

6.3.4 Microfluidics

One essential aspect that is required for the proposed sensors is the micrometer-sized biocompatible fluidic pathways to control the flow of samples on the chip. These pathways are required not only to protect the electrically conductive parts of the chip such as pads and bond wires but also in high-throughput screening to allow individual screening of multiple samples. Microfluidic packaging, in general, is a post-CMOS chip fabrication process and allows for tests under perfusion. In biological tests, evaporation of the sample liquid is a

serious issue that can only be solved with proper microfluidic devices. Compared to the electronic side of hybrid microfluidic/CMOS technology, microfluidic packaging is severely less developed. Although developing microfluidic devices was out of the scope of this thesis, it is an indispensable part to be integrated for future chips. In Figure 6.1, possible microfluidic chamber footprints are shown for each set of array sensors. Using soft lithography in the current technologies a minimum feature size in the range of some hundreds of microns can be achieved. The goal for the high-throughput devices is to reach a microfluidic device that can provide a separate chamber on top of each IDE to test different samples on every IDE. A schematic of the concept is shown in Figure 6.3 where one chamber is placed on top of each IDE and a separator microfluidic device can separate the samples and send them to different IDEs.

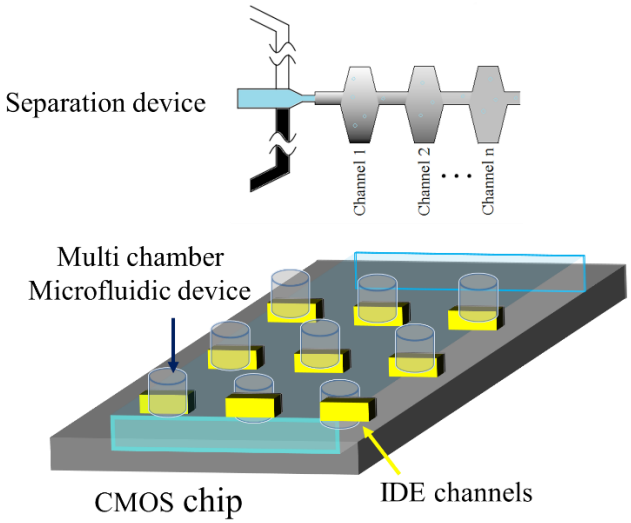
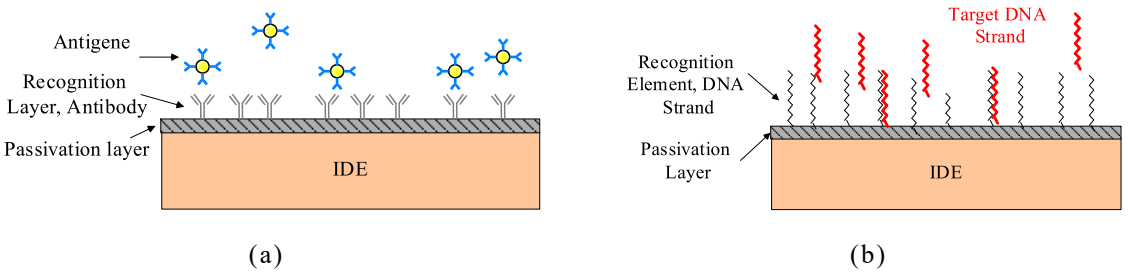


Figure 6.3: Multi-channel microfluidic device for future high throughput experiments.

6.3.5 Biofunctionalized Capacitive Sensor

The proposed sensors may be used for detecting specific cells or molecules in the future. In this case, a recognition element must be covered on the surface of the electrodes. Covering the surface of electrodes with the recognition elements is a complicated bioengineering

design task that requires the addition of linkers to the recognition material to link and fix it on the surface of the electrode. The recognition element for antigens that cause diseases, is the related antibody protein, as shown in Figure 6.4 (a). The same can be considered for the detection of a specific strand of DNA. In this case, the complementary strand of the DNA can be covered on the surface of the electrodes, as shown in Figure 6.4 (b).



(a) (b)

Figure 6.4: (a) antibody covered on the IDE for the selective detection of antigens (b) DNA strands covered on the IDE to detect target DNA strands

Appendix I: Practical Aspects of the Fabricated Chips

The chip has been implemented in AMS 350 μm CMOS technology. In the layout, an array of 8×16 sensors have been implemented and connected to a single read-out circuit consisting of an ECBCM array circuit, the CCO, and a 12-bit counter-serializer. To increase the number of electrodes, this layout has been repeated in the opposite direction to build a 16×16 array. As a result, the whole chip is composed of two independent compartments each consisting of 128 electrodes with a shared read-out circuit with a single digital output. Also, the IDEs have been implemented as both passivated and non-passivated in both compartments. As a result, each compartment has an 8×8 passivated and an 8×8 non-passivated array of electrodes. A die micrograph has been shown in Figure 7.1. A PCB board and a GUI like the previous chip have been developed. Details about the PCB, microcontroller code, and the GUI can be found in Appendix II.

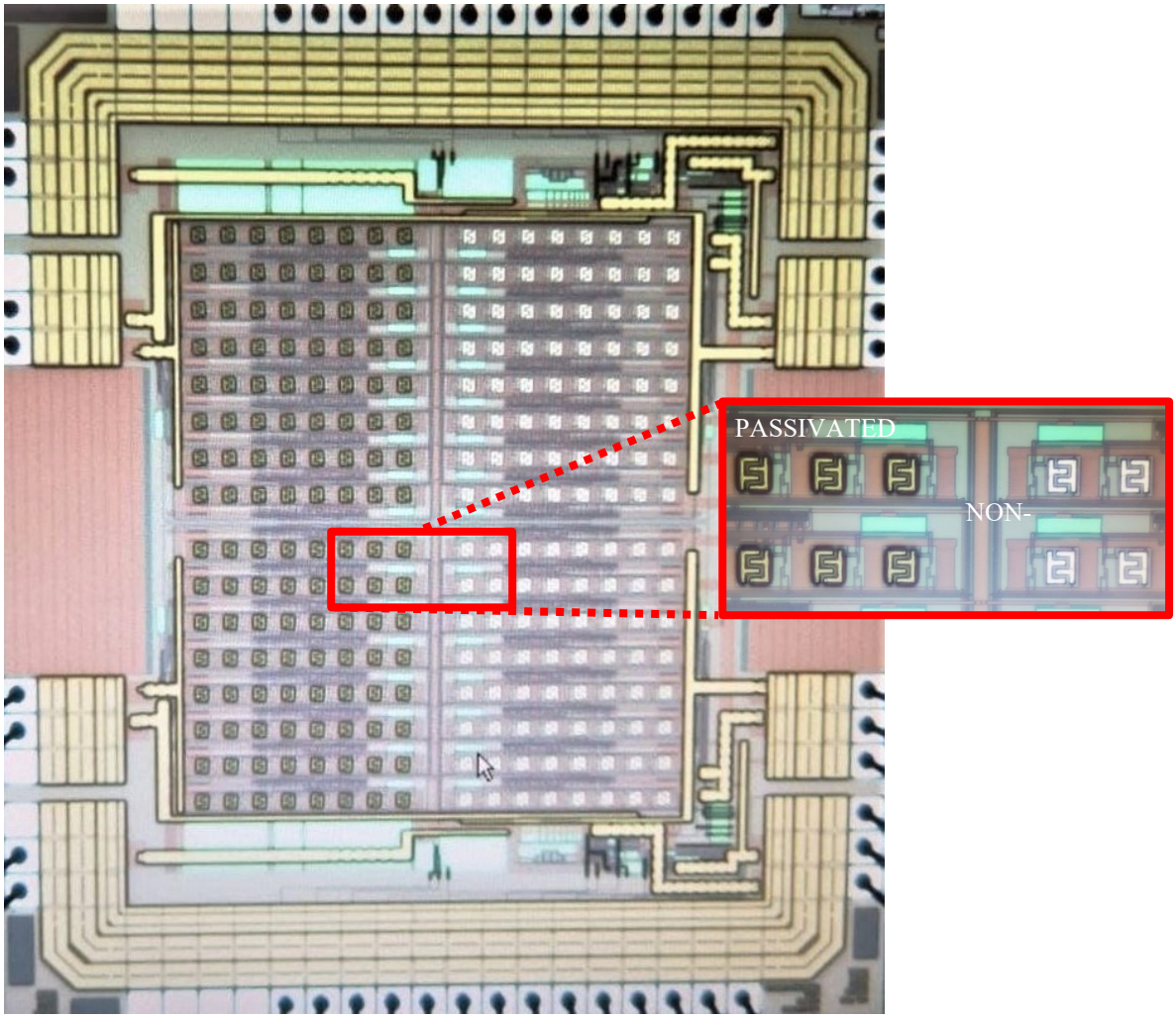


Figure 7.1: Die Micrograph with both passivated and non-passivated electrodes

7.1 Characterization Results

Output curves without samples have revealed that there is another, step-like, curve (shown in Figure 7.2). This pattern is meaningful and is described in detail in this appendix.

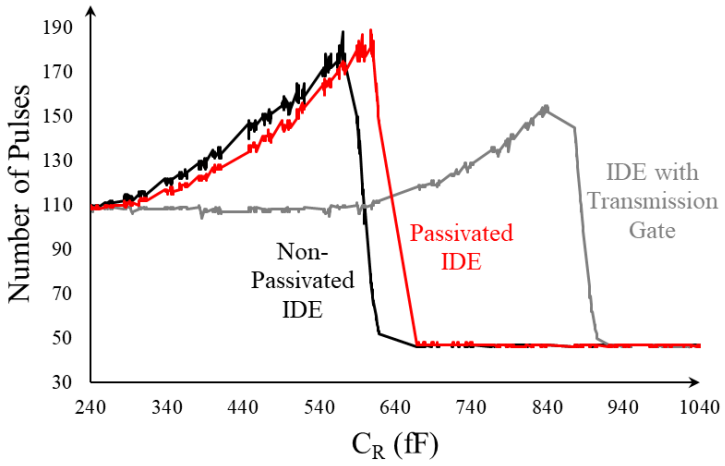


Figure 7.2: The Step-like Pattern

7.2 Analyzing the Pattern

The pattern is observed on a chip for the upper and lower compartments as well as in some chips only in one half of the chip. Since the layouts for both compartments are the same, the source of the difference in patterns has been tracked down to process variation. The decreasing pattern is the well-known pattern seen in Chapter 2 and 3 due to the gradual increase in CR in the sweep and drop in the output of the chip. To explain the step-like pattern, corner analysis has been investigated.

Based on the corner simulation results of the CCO block shown in Figure 7.3, oscillation stops at about IMAX = 900 µA at the slow corner, while it stops at about IMAX =1.2 mA at the typical corner, and at about IMAX =1.5 mA at the fast corner. From another side, based on post-layout simulations (see Figure 7.4), the saturated output current of ECBCM array block, ioutsat, can vary from around 650 µA to around 1.15 mA in the range of slow corner devices to fast corner ones. The oscillation happens only for the part of the iout waveform where ioutsat < IMAX of the CCO. In the process corner where ioutsat < IMAX, the oscillation continues until the end of the evaluation window (where Φ1 goes high again). Since larger dC results in an earlier transition, the total number of pulses counted in the

evaluation window decreases with lower dC, and therefore the decreasing pattern is generated. However, when ioutsat > IMAX, oscillation exists only during the transition of the output current of the ECBCM. In this case, as long as the transition of current happens within the evaluation window, the output shows a higher number of pulses compared to when the transition happens outside of the evaluation window. In the sweep, as CR keeps increasing, after some CR value, no transition happens in the Φ1 evaluation window. This value is where we see the sharp drop in the step-like pattern. This is illustrated shown in Figure 7.5. The sharp drop happens for larger CR values for higher CIDE values. The calculation of capacitance for these values is explained in Section 7.3.

In addition, by looking at the curves in Figure 7.2, there is a bump in the output value, exactly before the sharp decrease happens. This is because of the slight change in the pattern of the ECBCM output current curve, as shown in Figure 7.6, before reaching ioutsat. The peak in the curve happens in higher values as the pattern reaches the end of the Φ1 evaluation window. This is equal to a higher average in the ECBCM output current that translates slightly higher output value before the sharp drop.

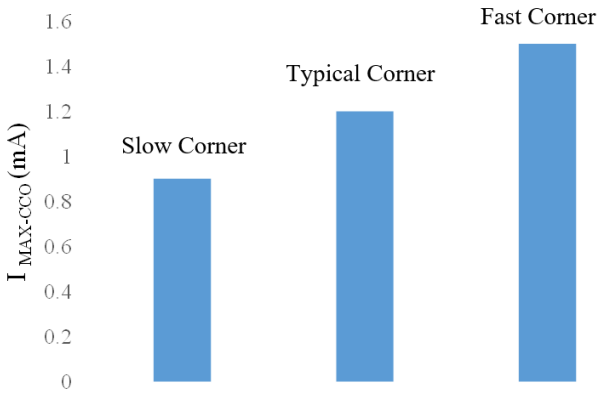


Figure 7.3: Maximum current that causes oscillation based on post-layout simulation, slow corner oscillation stops at 900 µA, Typical corner, oscillation stops at 1.2 mA, and Fast corner, the oscillation stops at about 1.5 mA.

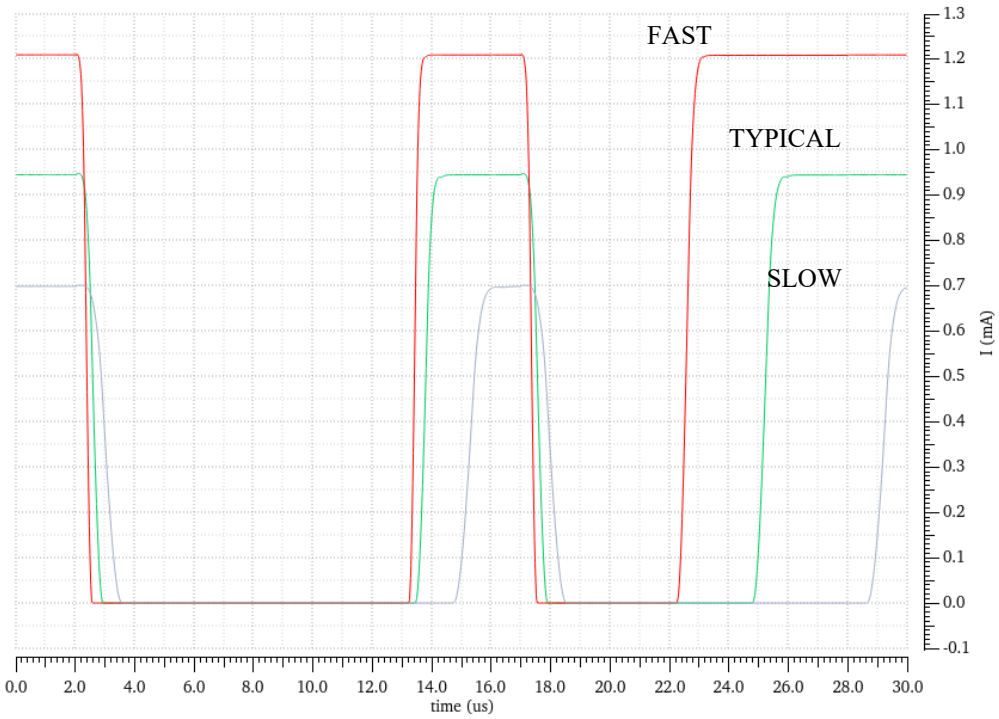


Figure 7.4: Post-layout simulation result for output current of the ECBCM Array block, Slow corner (Purple) with a maximum current of about 650 µA, Typical corner (white) with a maximum current of about 870 µA, and Fast corner (yellow) a maximum current of about 1.1 mA.

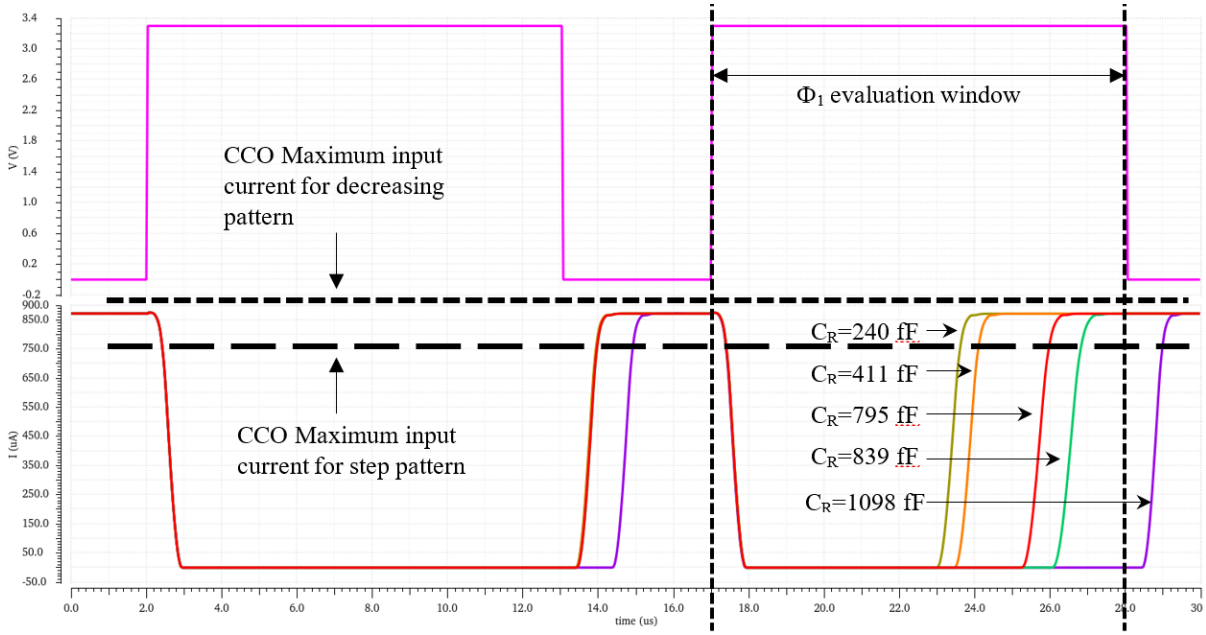


Figure 7.5: Φ1 evaluation window, the change in ECBCM array current due to an increase in CR, and the position of maximum input current that can cause oscillation in the CCO compared to the ECBCM array current. When the IDR of the CCO is higher than the maximum current of ECBCM Array, the decreasing pattern is created, and the step-like pattern happens otherwise.

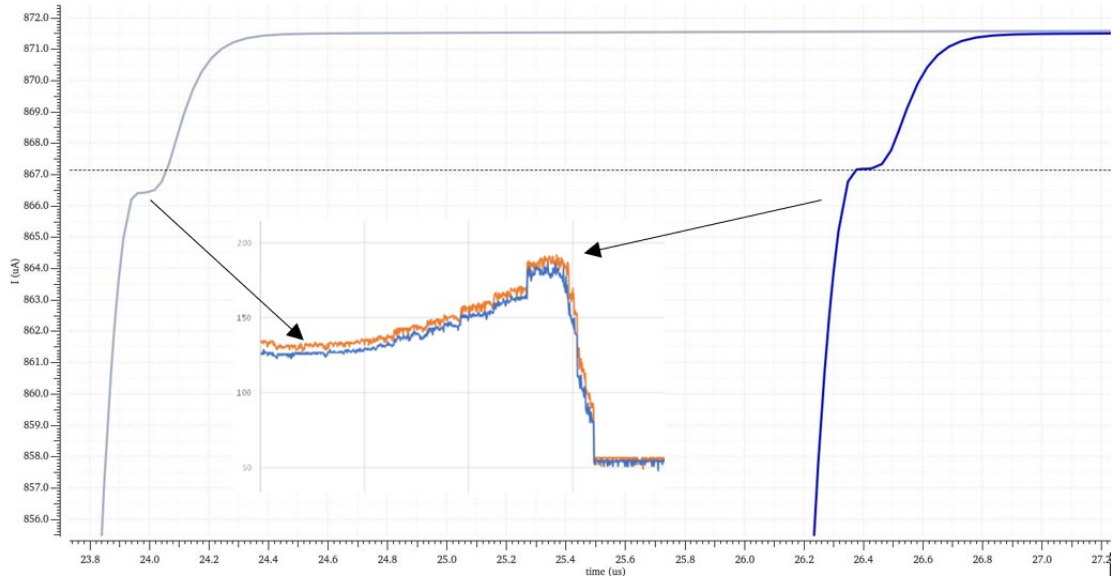


Figure 7.6: The trend of the ECBCM Array output current waveforms tends to peak at a higher level toward the end of the Φ1 evaluation window which is responsible for the increase in the output toward the end of the Φ1 evaluation window.

7.3 Capacitance Measurement within the Different Patterns

After putting the samples, to quantify the capacitance, and change within the decreasing pattern, we obtain two full CR sweep curves one before and one after putting the sample. As shown in Figure 7.7, the difference between the two curves has been calculated and shown in black. The difference curve reflects the difference in the output of the chip for a range of CR values, thus an average of the difference over the CR values has been considered as the final output of the chip because of the presence of samples.

In the step-like function, the shift in the value of CR indicates the change in the capacitance as discussed in Section 7.2. A MATLAB script has been written to analyze the shift from the baseline for the obtained data after putting the sample. As illustrated in Figure 7.8, first the difference between the two curves has been calculated as shown in black. Then, the amount of shift is calculated by the difference on the x-axis (CR) between the maximum and minimum of the difference curve.

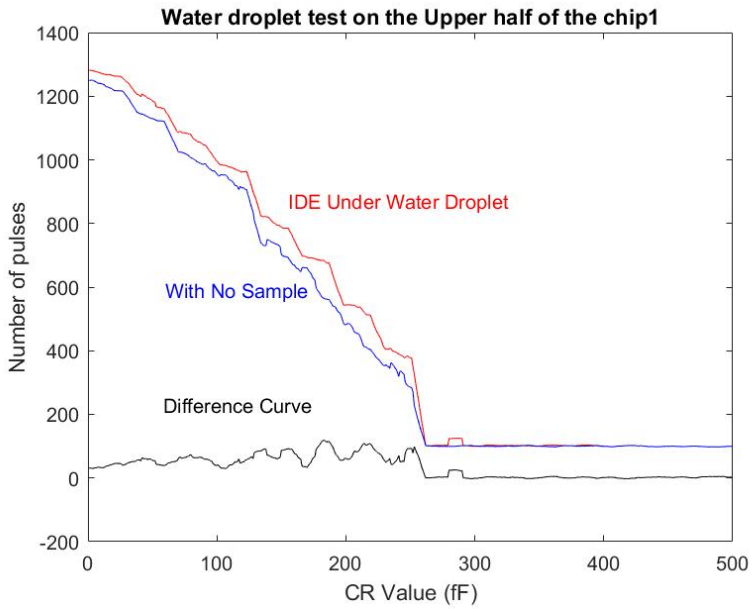


Figure 7.7: In the decreasing pattern, an increase in the IDE capacitance is reflected as a shift of the curve. To measure this change, we have considered the average of the difference between the two curves (the black curve).

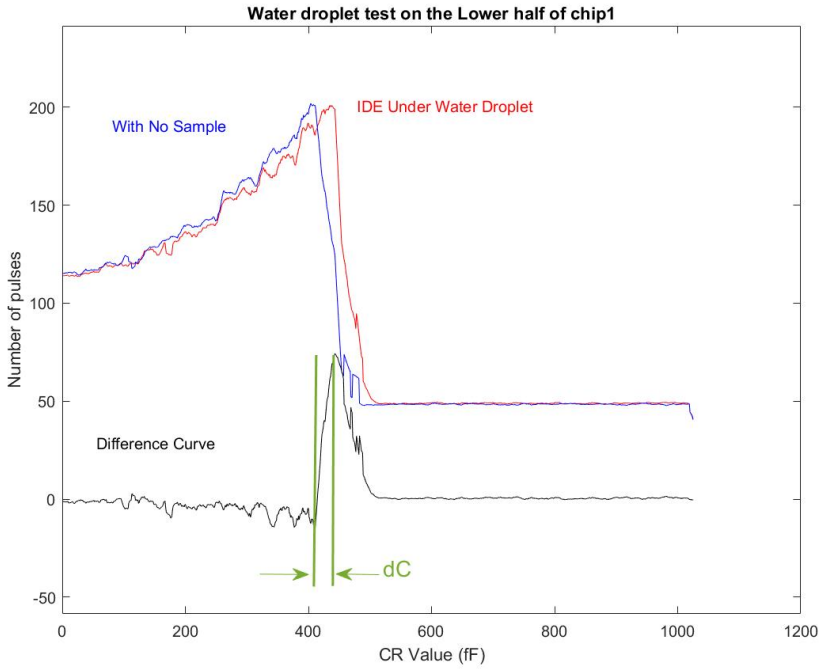


Figure 7.8: In the step-like pattern the increase in IDE capacitance reflects as a shift to right in the sharp decreasing pattern. To calculate the capacitance change, the value of capacitance for which the differential curve (curve shown in black) peaks has been subtracted from the value for which the curve has a minimum.

7.4 Summary

In this appendix, we show the new pattern that has emerged and tracked back to the process variations. It is shown that this pattern can also be used for capacitance measurement. In addition, by considering the process variation for future chips, one of the patterns can be favored against the other.

Appendix II: Test Bench Details for the Non-array Chip

8.1 Chip Pin Configuration and Description

Pin configuration and explanation for each of the pins of the chip are shown in Table 8.1. This table concerns the pin configuration of the chip packaged on an 85-pin SMD grid array package from KYOCERA corporation with a symbol named U0 implemented in the circuit schematic shown in Figure 8.1.

Table 8.1: Pin configuration and explanation for each of the pins

Pin number on the package	Description	Physical location of the Pin on Package
16	AVDD-R	H1
17	AGND	H2
18	Vref	J1
19	Nout-R	K1
20	DVDD-R	J2
21	DGND	L1
24	Phi3	L2
25	Phi2	L3
26	Phi1	K4
27	G3	L4
28	G2	J5
29	G1	K5
30	Sclk	L5
31	Sin	K6
32	DVDD-Pad	J6
33	Ca7-R	J7
34	Sin	L7
35	Sclk	K7
36	G1	L6
37	G2	L8
38	G3	K8
39	Phi1	L9
40	Phi2	L10
41	Phi3	K9

Pin number on the package	Description	Physical location of the Pin on Package
43	DGND	K10
44	DVDD-L	J10
45	Nout-L	K11
46	Vref	J11
47	AGND	H10
48	AVDD-L	H11

8.2 Breakdown of power consumption of each block in the chip

Post layout simulation results for the power consumption of each block on the chip is shown in Table 8.2.

Table 8.2: Power consumption break down of the ciruit blocks

Block	**Power consumption**
ECBCM	21.4 µW
CCO	7.3 µW
Counter/Serializer	0.2 µW

8.3 The Test Bench Circuit and System

On the board, five different voltage regulators and one multiplexer has been implemented as shown in the circuit schematic in Figure 8.1. Four voltage regulators are TLV75533PDBVR, 500-mA, high-PSRR, low-IQ, low-dropout voltage regulator with 5 V enable voltage, SOT-23 package and -40 to 125°C operating temperature where each of them was used to power analog and digital voltages (two for the right side and two for the left) to 3.3V. For the required 1.85 V reference voltage for the oscillator Vref pin, TLV713185PDBVT, 500-mA, high-PSRR, low-IQ, low-dropout voltage regulator with 5 V enable voltage, SOT-23, and -40 to 125°C operating temperature was used. All LDOs' enable pins were tied to the input voltage. TMUX1247DCKR, a precision analog multiplexer with 30 Ohm ON resistance and rail-to-rail capability was used. Decoupling capacitors were used for all the component's input power and output power supplies to

reduce the noise. Figure 8.1 shows the detailed schematic. All the pins of the chip are detailed in Table 8.1.

8.4 SPI Port Communication

The SPI is a synchronous 4-wire, full-duplex communication protocol. Half duplex can be used when there is no need for bi-directional communication. As in our case, the MCU has been configured as master and the chip is a slave where data transmits from the chip to the MCU with a shared clock bus, Φ3. The reading happens as soon as the slave select (ss) pin goes low. In our system, Φ3 which is the PWM signal output from the MCU is the shared clock bus while MISO pin is the output of the chip connected to the MISO pin of the microcontroller board (Arduino DUE). In addition, Φ1 is the ss pin which enables the SPI reading when it goes low as shown in the timing diagram in Figure 2.17 (d). These connections are shown in Figure 8.1.

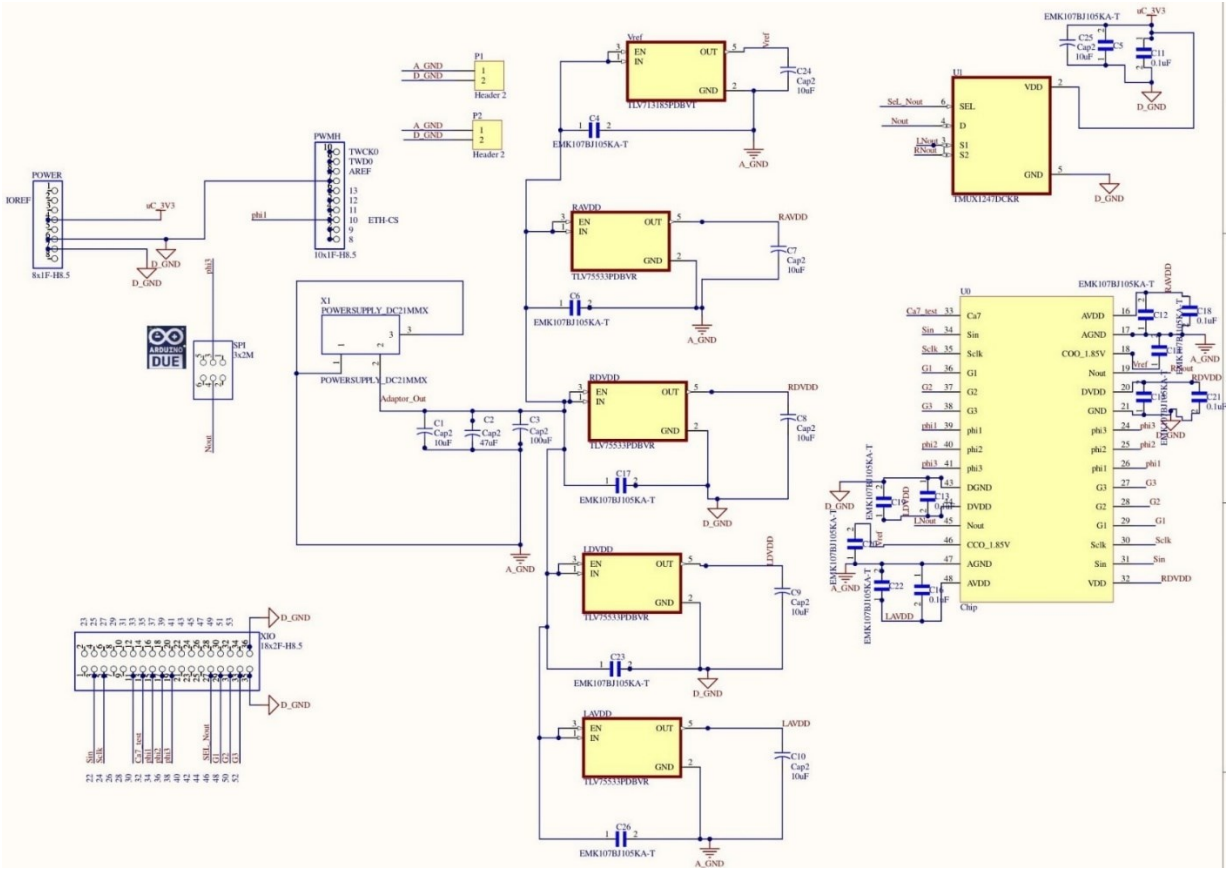


Figure 8.1: Schematic block diagram of the implemented PCB. The PCB hosts the chip, shown as U0, four 3.3 LDO voltage regulators for AVDD and DVDD of right and left blocks shown as RAVDD, RDVDD, LAVDD, and LDVDD, a 1.85 V voltage regulator, shown as Vref, serving as a reference for the CCO, and a rail-to-rail multiplexer to switch between the right and left blocks shown as U1.

8.5 Printed Circuit Board and Assembly

Figure 8.2 illustrates the PCB board of the circuit schematic shown in Figure 8.1. The list of the used components is given in Table 8.3.

Table 8.3: List and detail of the of components on the PCB

Designator	Comment	Link
C1, C2, C3, C7, C8, C9, C10, C24, C25	Cap	-
C4, C5, C6, C12, C14, C15, C17, C19, C20, C22, C23, C26	CAP	https://www.digikey.ca/en/products/detail/taiyo-yuden/EMK107BJ105KA-T/931028
C11, C13, C16, C18, C21	Cap	https://www.digikey.ca/en/products/detail/samsung-electro-mechanics/CL10B104KB8NNNL/10320686
LAVDD, LDVDD, RAVDD, RDVDD	TLV75533PDBVR	https://www.digikey.ca/en/products/detail/texas-instruments/TLV75533PDBVR/9685550
P1, P2	DGND and AGND ground Header 2	-
POWER	8x1M-H8.5	-

Designator	Comment	Link
PWMH	10x1M-H8.5	-
SPI	3x2F-H8.5	-
U0	Chip Socket	-
U1	TMUX1247DCKR	https://www.digikey.ca/en/products/detail/texas-instruments/TMUX1247DCKR/10445173
Vref	TLV713185PDBVT	https://www.digikey.ca/en/products/detail/texas-instruments/TLV713185PDBVT/10665155
XIO	18x2F-H8.5	-

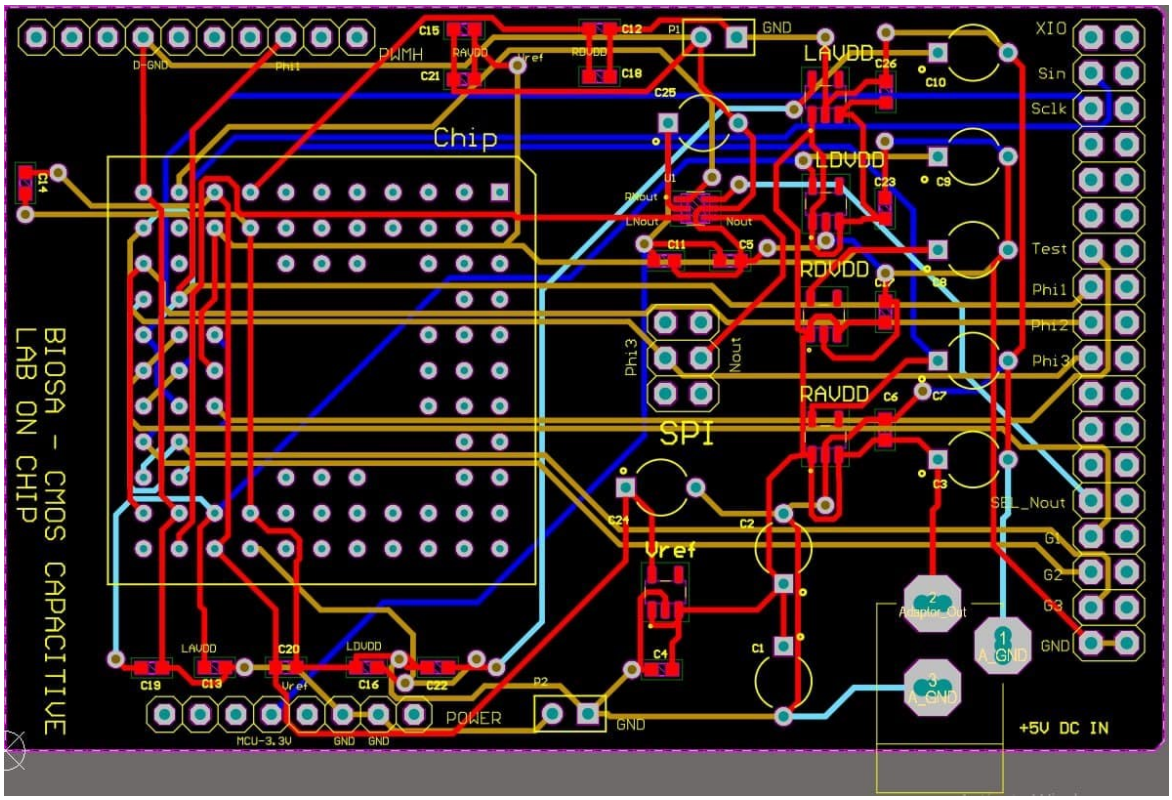


Figure 8.2: The implemented PCB for the circuit shown in Figure 8.1.

8.6 Microcontroller Design

The microcontroller used for the test bench is an Arduino DUE development board. It has distinct tasks as listed below. Under each section, a brief description of the task is given and the corresponding firmware is revealed.

8.7 Generation of Φ_1, Φ_2, Φ_3 Clock Pulses

Three PWL channels of the Arduino Due board have been used to generate Φ1 (15 µs period, 12 µs duty cycle), Φ2 (15 µs period, 8 µs duty cycle, and 2 µs delay), and Φ3 (1 µs period, 0.5 µs duty cycle). The corresponding code for the clock pulse generation is given below with comments on each line of the code.

```
    REG_PMC_PCER1 |= PMC_PCER1_PID36;// POWER UP PWM CLOCK
     REG_PWM_WPCR = PWM_WPCR_WPCMD(0);//UNLOCK USER INTERFACE FOR PWM
     REG_PWM_CLK = PWM_CLK_PREA(0) | PWM_CLK_DIVA(21); //CONFIG THE PWM CLOCK GENERATOR: CLOCK A, 84/21 = 4MHZ
     REG_PWM_SCM = PWM_SCM_SYNC0 | PWM_SCM_SYNC1; //SYNCHRONIZE PHI1 AND PHI2 FOR THEY HAVE THE SAME FREQUENCY
     //CONFIG PHI1, OUTPUT PIN PC2, DIGITAL PIN 34
     REG_PIOC_ABSR |= PIO_ABSR_P2; // TRANSFER PIN CONTROL FROM PIO TO PWM
     REG_PIOC_PDR |= PIO_PDR_P2;   // SET PWM PIN TO AN OUTPUT
     REG_PWM_CMR0 = PWM_CMR_CPRE_CLKA; //MODE CONFIGURATION FOR CHANNEL 0: CLOCK A, LEFT ALIGNED, WAVEFORM
START AT HIGH
     REG_PWM_CPRD0 = PWM_CPRD_CPRD(60);//CONFIG PERIOD FOR PWM 60/(4MHZ)
     REG_PWM_CDTY0 = PWM_CDTY_CDTY(16);// 80/3% DUTY CYCLE(16)
     REG_PWM_ENA = PWM_ENA_CHID0;// ENABLE PWM CHANNEL0

     //CONFIG PHI2, OUTPUT PIN PC4, DIGITAL PIN 36
     REG_PIOC_ABSR |= PIO_ABSR_P4; // TRANSFER PIN CONTROL FROM PIO TO PWM
     REG_PIOC_PDR |= PIO_PDR_P4;   // SET PWM PIN TO AN OUTPUT
     REG_PWM_CMR1 = PWM_CMR_CPRE_CLKA | PWM_CMR_DTE; //MODE CONFIGURATION FOR CHANNEL 0: CLOCK A, LEFT
ALIGNED, WAVEFORM START AT HIGH
    REG_PWM_CPRD1 = PWM_CPRD_CPRD(60);//CONFIG PERIOD FOR PWM 60/(4MHZ)
     REG_PWM_DT1 = PWM_DT_DTL(4); //CREATE THE 1US(DELAY)
     REG_PWM_CDTY1 = PWM_CDTY_CDTY(12);// 80/6% DUTY CYCLE(12)
     REG_PWM_ENA = PWM_ENA_CHID1;// ENABLE PWM CHANNEL1

     //CONFIG PHI3, OUTPUT PIN PC6, DIGITAL PIN 38
     REG_PIOC_ABSR |= PIO_ABSR_P6; // TRANSFER PIN CONTROL FROM PIO TO PWM
     REG_PIOC_PDR |= PIO_PDR_P6;   // SET PWM PIN TO AN OUTPUT
     REG_PWM_CMR2 = PWM_CMR_CPRE_CLKA;//MODE CONFIGURATION FOR CHANNEL 0: CLOCK A, LEFT ALIGNED, WAVEFORM
START AT LOW |PWM_CMR_CALG
     REG_PWM_CPRD2 = PWM_CPRD_CPRD(4);//CONFIG PERIOD FOR PWM 2/(4MHZ)
     REG_PWM_CDTY2 = PWM_CDTY_CDTY(2);//50% DUTY CYCLE(1)
     REG_PWM_ENA = PWM_ENA_CHID2;// ENABLE PWM CHANNEL2
```

8.8 SPI Communication

The SPI communication takes place with Φ3 as the SPI clock and Φ1 as the slave select as described in SPI communication section. The corresponding code for the clock pulse generation is given below with comments on each line of the code.

```
//SPI SERIAL RECEIVE
 REG_PMC_PCER0 |= PMC_PCER0_PID24;// POWER UP SPI CLOCK
 REG_SPI0_WPMR = 0 << SPI_WPMR_WPEN; //UNLOCK USER INTERFACE FOR SPI
 //INSTANCE SPI0, MISO: PA25, (MISO), MOSI: PA26, (MOSI), SCLK: PA27, (SCLK), NSS: PA28, DIGITAL PIN 10
 REG_PIOA_ABSR |= PIO_ABSR_P25; // TRANSFER PIN CONTROL FROM PIO TO SPI
 REG_PIOA_PDR |= PIO_PDR_P25;   // SET MISO PIN TO AN OUTPUT
 REG_PIOA_ABSR |= PIO_ABSR_P26; // TRANSFER PIN CONTROL FROM PIO TO SPI
 REG_PIOA_PDR |= 0 << PIO_PDR_P26; // SET MOSI PIN TO AN INPUT
 REG_PIOA_ABSR |= PIO_ABSR_P27; // TRANSFER PIN CONTROL FROM PIO TO SPI
 REG_PIOA_PDR |= 0 << PIO_PDR_P27; // SET SCLK PIN TO AN INPUT
 REG_PIOA_ABSR |= PIO_ABSR_P28; // TRANSFER PIN CONTROL FROM PIO TO SPI
 REG_PIOA_PDR |= 0 << PIO_PDR_P28; // SET NSS PIN TO AN INPUT
 //REG_ISER0 = 1<<24; //ENABLE INTERRUPT CONTROLLER
 REG_SPI0_CR = 1; // ENABLE SPI
 REG_SPI0_MR = 0; // SLAVE MODE
 REG_SPI0_IER = 1 << SPI_IER_RDRF | 1 << SPI_IER_OVRES | 1 << SPI_IER_NSSR; //ENABLE INTERRUPTS
 SPI0->SPI_CSR[0] = SPI_CSR_BITS_12_BIT; // CAPTURE ON FALLING EDGE AND TRANSFER 12 BITS.
```

8.9 Setting the Value of the Reference Capacitor

The microcontroller uses GPIO pins to set the 8 bits into the shift register when the right circuit is selected and set 7 bits into the shift register when the left circuit is selected. Below the corresponding code has been shown and commented.

```
VOID INPUTSIG(CHAR TESTSEQ[])
{
 DELAYMICROSECONDS(5);
 //FULLY RESET THE INPUT REGISTERS
 FOR (INT I = 13; I > 0 ; I--)
 {
  DIGITALWRITE(22, LOW);
  DIGITALWRITE(24, LOW);
  DELAYMICROSECONDS(5);
  DIGITALWRITE(24, HIGH);
  DELAYMICROSECONDS(5);
 }
 //APPLY INPUT SEQUENCES
 FOR (INT I = 0; I <=7 ; I++)
 {
  IF (TESTSEQ[I] == '0')
  {
   DIGITALWRITE(22, LOW);
   DIGITALWRITE(24, LOW);
   DELAYMICROSECONDS(5);
   DIGITALWRITE(24, HIGH);
   DELAYMICROSECONDS(5);
  }
  ELSE IF (TESTSEQ[I] == '1')
  {
   DIGITALWRITE(22, HIGH);
```

```
    DIGITALWRITE(24, LOW);
    DELAYMICROSECONDS(5);
    DIGITALWRITE(24, HIGH);
    DELAYMICROSECONDS(5);
   }
   ELSE
   {
    DIGITALWRITE(22, LOW);
    DIGITALWRITE(24, LOW);
    DELAYMICROSECONDS(10);
   }
  }
  DIGITALWRITE(22, LOW);
  DIGITALWRITE(24, LOW);
  DELAYMICROSECONDS(5);
```

8.10 Basic Communication using MCU

The microcontroller and GUI communicate through 4 simple commands initiated through the serial port by sending ‘S’, ‘G’, ‘W’, and ‘R’ for setting the number of samples, CCO configuration, the value of CR, and receiving the data from the SPI port.

After command ‘S’, the GUI sends the number of samples that tells the microcontroller the number of times that the same measurement is supposed to be repeated for higher accuracy and noise reduction. After ‘G’, the GUI sends one of the strings that the user has set, 000, 001, 011, or 111. The inherent frequency of the oscillator is maximum when the input is 000 and is minimum when the input is 111. The order of bits in these strings doesn’t change anything. After ‘W’, the 7-bit or 8-bit string of ones and zeros are sent to set the value into the shift register of the bank of capacitors for the left and right blocks, respectively. After ‘R’, the microcontroller reads the received data from the SPI port receive buffer. The code for this part is given and commented on below.

```
VOID LOOP() {
 CHAR CALIN_I[8];
 CHAR CALIN_G[3];
 IF (SERIAL.AVAILABLE() > 0) // CHECK IF SERIAL IS AVAILABLE
 {
  //SERIAL.PRINTLN(2);
  CHAR CMD = SERIAL.READ(); // READ THE SERIAL AND PUT IN CMD
```

```
        SWITCH (CMD)
        {
         CASE 'S': // IF THE COMMAND WAS 'S'
         {
          STRING N_SAMPLE_S = SERIAL.READSTRINGUNTIL('\0'); // READ THE SERIAL AGAIN IN THE FORM OF NONSTOP UNTIL
REACHING A '\0' AND PUT IN N_SAMPLE_S
          N_SAMPLE = N_SAMPLE_S.TOINT(); // CONVERT N_SAMPLE_S TO INTEGER AND PUT IN N_SAMPLE
          SERIAL.PRINT(N_SAMPLE);
          SERIAL.PRINT(TERMINATION_CHAR);
          BREAK;
         }
         CASE 'G': // IF THE COMMAND WAS 'G', THE OSCILLATION FREQUENCY WILL BE SET
         {
          FOR (INT I = 0; I < 3; )
          {
           IF (SERIAL.AVAILABLE() > 0)
           {
            CALIN_G[I] = SERIAL.READ(); // READ EACH VALUE IN THE CCO BOX (3 DIGITS MUST BE ENTERED) AND SET G1(48+0),
G2(48+2) AND G3(48+4)
            IF (CALIN_G[I] == '1')
             DIGITALWRITE(48 + 2*I, HIGH);
            ELSE
             DIGITALWRITE(48 + 2*I, LOW);
            I++;
           }
          }
          CALIN_G[3] = '\0'; // WRITE A \0 AT THE END OF THE CALIN_G[I] STRING TO MAKE IT READY FOR SERIAL PRINT TO SHOW THE
MESSAGE ON THE GUI
          SERIAL.PRINT(CALIN_G); // PRINT OUT CALIN_G
          SERIAL.PRINT(TERMINATION_CHAR);
          BREAK;
         }
         CASE 'W': // IF THE COMMAND WAS 'W' START SETTING THE CR VALUE
         {
          FOR (INT I = 0; I <= 7; )
          {
           IF (SERIAL.AVAILABLE() > 0)
           {
            CALIN_I[I] = SERIAL.READ(); // READ THE STRING OF SIZE 8 AND PUT IN CALIN_I
            I++;
           }
          }
          IF(CALIN_I[7] == ' ') // IF '0' -> CH=LEFT, IF '1' -> CH=RIGHT
          {
           DIGITALWRITE(46, LOW);
          }
          ELSE
          {
           DIGITALWRITE(46, HIGH);
          }

          INPUTSIG(CALIN_I); // NOW THAT THE CALIN_I HAS BEEN FILLED WITH THE VALUES SENT FROM THE GUI, CALL INPUTSIG
FUNCTION TO APPLY IT
          CALIN_I[8] = '\0';  // PUT A \0 AT THE END OF THE STRING AND SEND OUT THE WHOLE STRING
          SERIAL.PRINT(CALIN_I);
          SERIAL.PRINT(TERMINATION_CHAR);
          BREAK;
         }
```

```
        CASE 'R': // IF THE COMMAND WAS R, THEN IT IS TIME TO READ THE DATA FROM SPI PORT
        {
         INT BUF[N_SAMPLE];
         FOR (INT I = 0; I < N_SAMPLE;)
         {
          IF (REG_SPI0_SR & 1)
          {
//          BUF[I] = I;
          BUF[I] = REG_SPI0_RDR;
          I++;
          }
         }

         CHAR BUFFERR[4*N_SAMPLE+N_SAMPLE];
         INT N = 0;
         FOR (INT I = 0; I < N_SAMPLE; I++) {
            N += SPRINTF (&BUFFERR[N], "%04D,", BUF[I]);
         }
         BUFFERR[4*N_SAMPLE+N_SAMPLE-1] = '\0';

         SERIAL.PRINT(BUFFERR);
         SERIAL.PRINT(TERMINATION_CHAR);
         BREAK;
        }
        DEFAULT:
        {
         SERIAL.PRINT("MEOW");
         SERIAL.PRINT(TERMINATION_CHAR);
         BREAK;
        }
       }
      }
     }
```

8.11 GUI Main Configuration Window

The commands are generated based on the multiple input options that are designed and implemented on the graphical interface. Figure 2.28 illustrates the designed GUI. After running the GUI (by opening the command prompt window in windows by typing cmd in Windows search, going to the directory address of the GUI, and typing main.exe), the GUI will automatically find the microcontroller board if it has been connected through the USB port to the PC. By clicking on Connect, the GUI will establish serial communication with the microcontroller. Connecting to the board will activate the input fields for the user to configure the measurement. Since this GUI works with both 2-electrode CMOS chip and

the Array chip, the cmos or Array should be selected first based on the chip that is being used. Then Left, Right, Internal Capacitance, or Left&Right can be selected for the channel. Internal capacitance mode sets the transmission gate on the right to open them, resulting in the disconnection of IDE from the circuit. Capacitance sweep or fixed point are the two options for the mode of measurement. In the sweep mode, the reference programable capacitance will be swept in its full range whilst, in fixed point mode, the user is required to input the desired value for the reference capacitance in the reference value field as a number between 0 to 127 which represent 0 fF and 1270 fF, respectively. CCO resolution as explained can be one of the 000, 001, 011, or 111 values. For the highest resolution, we almost always choose 000. The number of samples is the field that the user inputs the number of times that the same measurement should be repeated. The excel sheet in this case will print the raw value of measurements in one raw consecutively for each CR value; however, the plot will be created based on the average of these points. With higher numbers, smoother curves can be obtained at the cost of increased time of measurement due to repeating the measurements. The number of repeats for the whole experiment is defined in repeats field. For example, putting 20 by the user in this part results in 20 different curves and 20 rows of data in the printed excel sheet. This GUI is capable of handling both time-based and repeat-based measurements meaning that if repeat interval and stop time fields are given non-zero values, the GUI will determine the number of repeats by dividing the stop time by the interval. This option is good for time-based measurements when the user doesn't exactly know when the experiment will finish. If the interval, that the user inputs, turn out to be less than the time it takes for each measurement, the GUI shows a warning in the measurement log section after the start of the experiment. This is just to let the user know it and it will not stop GUI from continuing to run the measurements. If any of the repeat interval and stop

time are left zero, the GUI will consider the number in the repeats filed as the number of repetitions for the measurements.

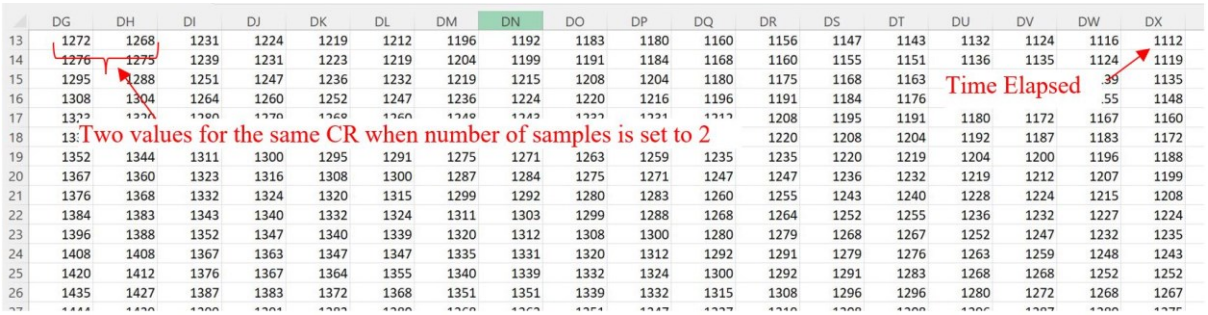
8.12 Plot Types

As shown in Figure 2.28, there is a field to set the type of plot to 2D or 3D. The main difference between these two modes is the presence of the time axis in the 3D view while in 2D all time-resolved curves append on a 2D curve. Whenever the right electrode is selected an always 2D curve will also be shown that will show the value of the extracted capacitance for the right side. The technique uses the number of pulses obtained from the internal curve for CR=400 fF, and then finds the capacitance values in the right block that matches the obtained number of pulses.

8.13 Saved Excel Sheets

The data is written in real-time to the excel sheets. As a result, the excel sheets must not be kept open during the experiments. The excel sheets can be found in the GUI's directory in a folder named output. The name of each excel sheet is very meaningful. It starts with Right, for the right channel, Left, for the left channel, and CIDE for the values of the extracted capacitance. Then, the type of measurement is shown with the name of SM or FP representing sweep mode or fixed-point experiment. Next, the data followed by the time of measurement appears. Finally, the number after Cmos represents the number of samples that the user has inputted. Inside the excel sheet, each raw corresponds to one measurement curve. In the case that the number of samples is more than one, the repeated numbers show the obtained values for a given CR beside each other. At the end of the raw, the total time spent on data acquisition of the raw is shown. This is valuable data showing the user the

amount of real time passed for obtaining each curve. The CIDE is the extracted capacitance from each curve. As a result, it is only one point value at each raw. See Figure 8.3 for details.



	DG	DH	DI	DJ	DK	DL	DM	DN	DO	DP	DQ	DR	DS	DT	DU	DV	DW	DX
13	1272	1268	1231	1224	1219	1212	1196	1192	1183	1180	1160	1156	1147	1143	1132	1124	1116	1112
14	1276	1275	1239	1231	1223	1219	1204	1199	1191	1184	1168	1160	1155	1151	1136	1135	1124	1119
15	1295	1288	1251	1247	1236	1232	1219	1215	1208	1204	1180	1175	1168	1163			39	1135
16	1308	1304	1264	1260	1252	1247	1236	1224	1220	1216	1196	1191	1184	1176			55	1148
17	1322	1320	1280	1270	1268	1260	1248	1243	1232	1231	1212	1208	1195	1191	1180	1172	1167	1160
18	13											1220	1208	1204	1192	1187	1183	1172
19	1352	1344	1311	1300	1295	1291	1275	1271	1263	1259	1235	1235	1220	1219	1204	1200	1196	1188
20	1367	1360	1323	1316	1308	1300	1287	1284	1275	1271	1247	1247	1236	1232	1219	1212	1207	1199
21	1376	1368	1332	1324	1320	1315	1299	1292	1280	1283	1260	1255	1243	1240	1228	1224	1215	1208
22	1384	1383	1343	1340	1332	1324	1311	1303	1299	1288	1268	1264	1252	1255	1236	1232	1227	1224
23	1396	1388	1352	1347	1340	1339	1320	1312	1308	1300	1280	1279	1268	1267	1252	1247	1232	1235
24	1408	1408	1367	1363	1347	1347	1335	1331	1320	1312	1292	1291	1279	1276	1263	1259	1248	1243
25	1420	1412	1376	1367	1364	1355	1340	1339	1332	1324	1300	1292	1291	1283	1268	1268	1252	1252
26	1435	1427	1387	1383	1372	1368	1351	1351	1339	1332	1315	1308	1296	1296	1280	1272	1268	1267

Figure 8.3: A snapshot of the saved data in the excel sheet

8.14 Steps for Performing the Experiments

1- the chip must be placed first before connecting the power and the usb.

2- connect the usb cable first, as shown in FIGURE 8.4. the programming port of the arduino port must be used (the microusb close to the power jack of the board).

3- connect the pcb (not the arduino board) to the ac power adaptor (see FIGURE 8.4).

4- run the gui. to run the gui, you should know the folder that has all the gui files. open the command prompt window in windows by typing *cmd* in windows search bar. set the directory in the command prompt window. you can copy the address of the folder and paste it into the window after typing "*cd* ". the space must exist after *cd* and then you can paste the address. type *main.exe* (see FIGURE 8.5). the gui will run.

5- to access the excel sheets you can refer to the *outputs* folder in the same gui folder.

6- make sure to disconnect the power and usb every time you want to remove the chip.

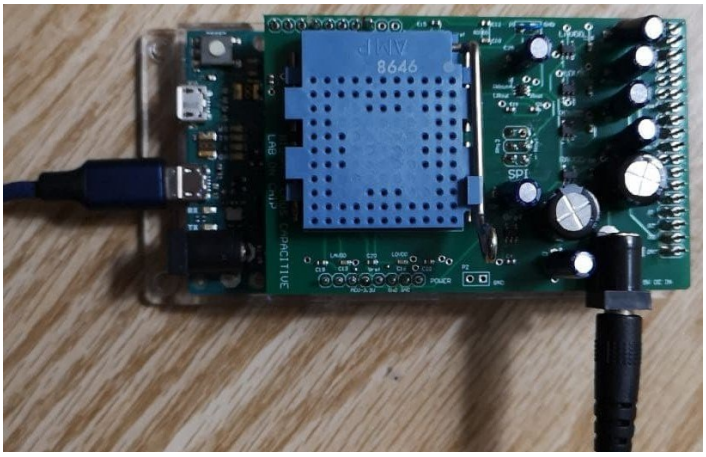


Figure 8.4: A snapshot of the Test bench.

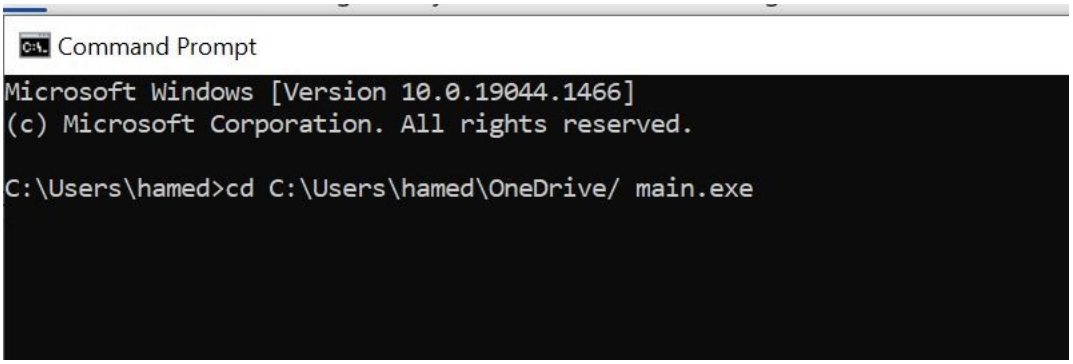


Figure 8.5: A snapshot of the command prompt window to run the GUI.

Appendix III: Test Bench Details for the Array Chip

9.1 Chip Pin Configuration and Description

Pin configuration and explanation for each of the pins of the chip are shown in Table 9.1. This table concerns the pin configuration of the chip packaged on an 85-pin SMD grid array package from KYOCERA corporation with a symbol named chip implemented in the circuit schematic shown in Figure 9.2.

Table 9.1: Pin configuration and explanation for each of the pins

Pin Number	Pin Code On the package	Signal	On The PCB
Up Circuit			
18	J1	VA_U	AVDD_U
19	K1	GND	GND
20	J2	Vdd_U	DVDD_U
21	L1	GND	GND
28	J5	A_U	A_U
29	K5	B_U	B_U
30	L5	C_U	C_U
31	K6	D_U	D_U
32	J6	Vdd_U	DVDD_U
33	J7	Ca10_U	Ca10_U
34	L7	Sin_U	Sin_U
35	K7	Clk_U	Sclk_U
36	L6	E_U	E_U
37	L8	F_U	F_U
38	K8	G_U	G_U
39	L9	Phi1_U	Phi1_U
40	L10	Phi2_U	Phi2_U
41	K9	Phi3	Phi3
43	K10	GND	GND
44	J10	Vdd_U	DVDD_U
45	K11	Nout_U	Nout_U
46	J11	Vref	Vref
47	H10	GND	GND

Pin Number	Pin Code On the package	Signal	On The PCB
48	H11	VA_U	AVDD_U
Down Circuit			
1	B2	GND	GND
2	C2	Vdd_D	DVDD_D
3	B1	GND	GND
4	C1	VA_D	AVDD_D
58	D11	VA_D	AVDD_D
59	D10	GND	GND
60	C11	Vref	Vref
61	B11	Nout_D	Nout_D
62	C10	Vdd_D	DVDD_D
63	A11	GND	GND
65	B9	Phi3	Phi3
66	A10	Phi2_D	Phi2_D
67	A9	Phi1_D	Phi1_D
68	B8	G_D	G_D
69	A8	F_D	F_D
70	B6	E_D	E_D
71	B7	Clk_D	Sclk_D
72	A7	Sin_D	Sin_D
73	C7	Ca10_D	Ca10_D
74	C6	Vdd_D	DVDD_D
75	A6	D_D	D_D
76	A5	C_D	C_D
77	B5	B_D	B_D
78	C5	A_D	A_D

9.2 The Test Bench Circuit and System

On the board, five different voltage regulators and one multiplexer has been implemented as shown in the circuit schematic in Figure 9.1. Four voltage regulators are TLV75533PDBVR, 500-mA, high-PSRR, low-IQ, low-dropout voltage regulator with 5 V enable voltage, SOT-23 package, and -40 to 125°C operating temperature ranges where each of them was used to power analog and digital voltages (two for the right side and two for the left) to 3.3V. For the required 1.85 V reference voltage for the oscillator Vref pin, TLV713185PDBVT, 500-mA, high-PSRR, low-IQ, low-dropout voltage regulator with 5 V enable voltage, SOT-23 and -40 to 125°C operating temperature ranges was used. All LDOs' enable pins were tied to the input voltage. TMUX1247DCKR, a precision analog multiplexer with 30 Ohm ON resistance and rail-to-rail capability was used. Decoupling

capacitors were used for all the component's input power and output power supplies to reduce the noise. Figure 9.2 shows the detailed schematic. All the pins of the chip are detailed in Table 9.1. The fabricated PCB is shown in Figure 9.3.

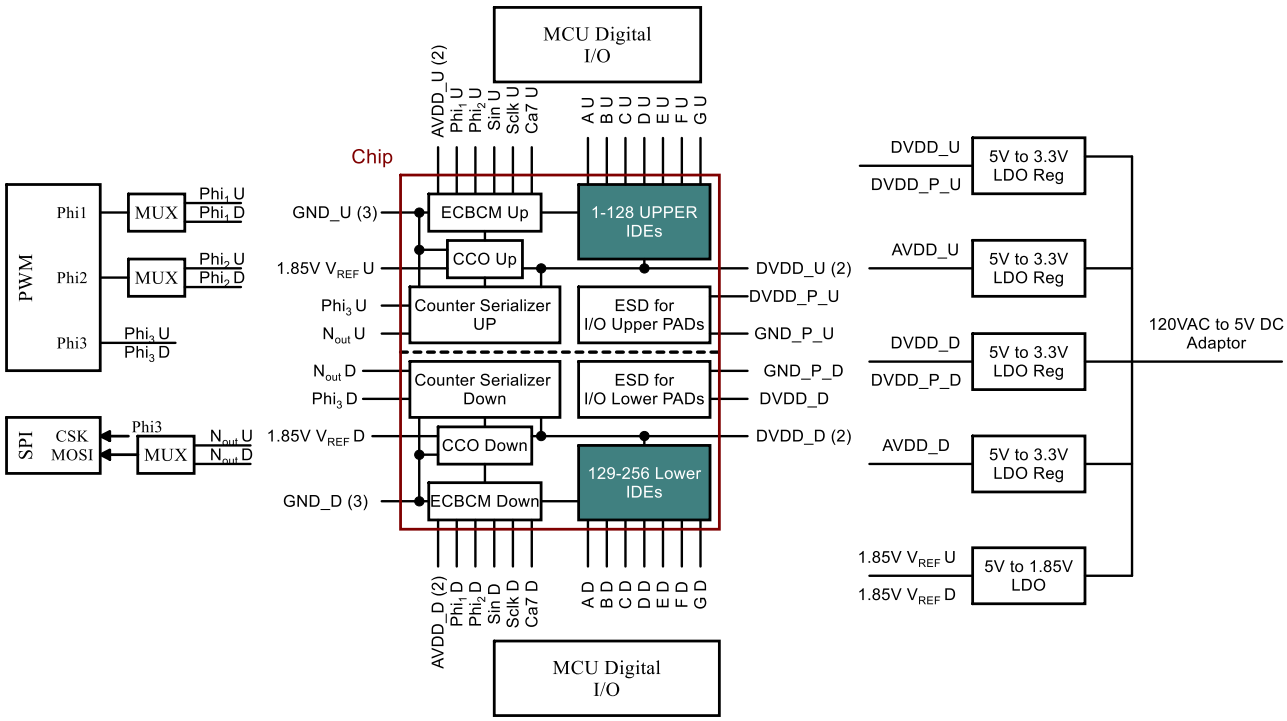


Figure 9.1: Circuit Schematic of the test bench for the array chip.

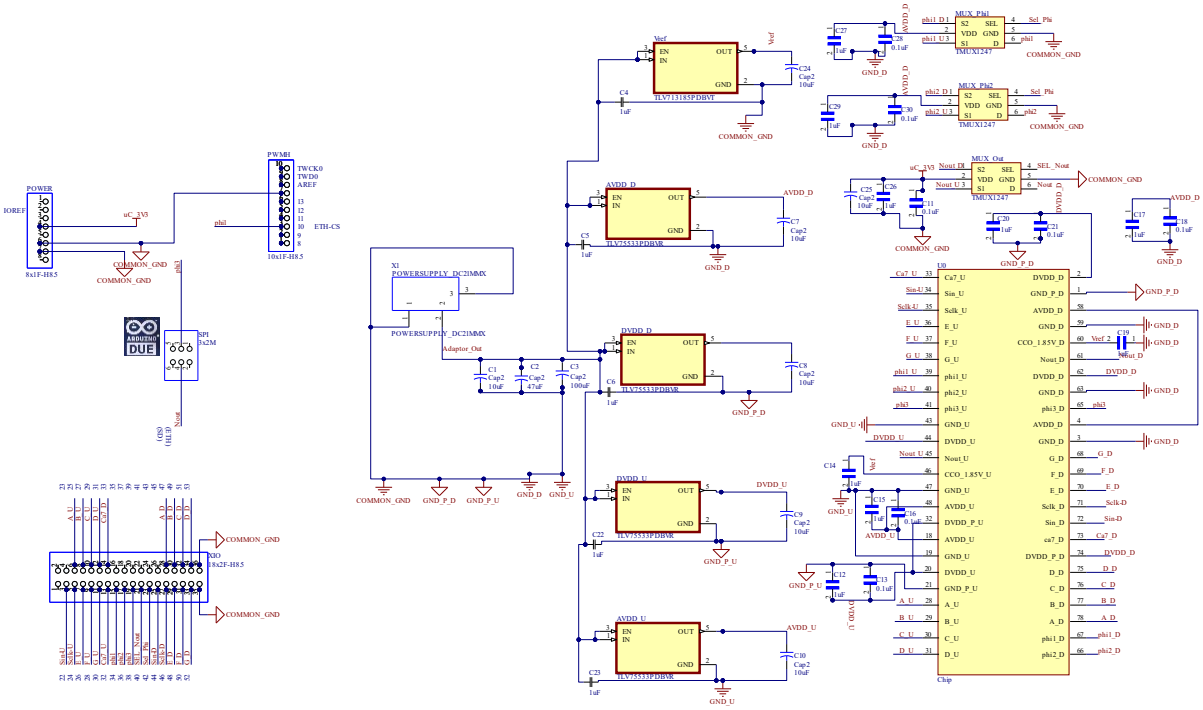


Figure 9.2: PCB circuit schematic of the test bench for the array chip.

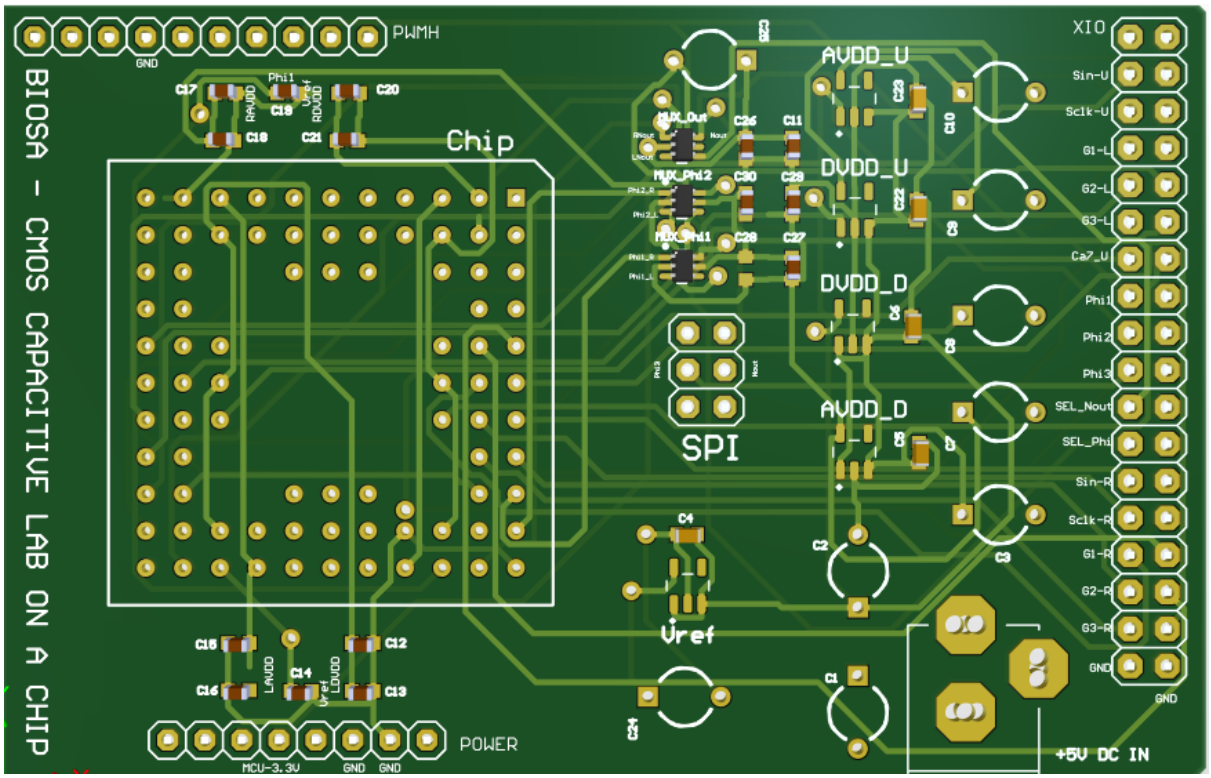


Figure 9.3: PCB Schematic of the test bench for the array chip.

9.3 Microcontroller Design

The microcontroller used for the test bench is an Arduino DUE development board. In this design, we have unified all the commands in an integer array. It is a 23-bit command and the detail of each member is shown below.

```
STRING COMMAND;
//{[0]UORD,
[1]NS{0}, [2]NS{1}, [3]NS{2},
[4]G, [5]F, [6]E, [7]D, [8]C, [9]B, [10]A,
[11]CA10,[12]CA9,[13]CA8,[14]CA7,[15]CA6,[16]CA5,[17]CA4,[18]CA3,[19]CA2,[20]CA1,
[21]CS,
[22] SWEEP(S) OR KNOWN REFERENCE(R)]
```

The first integer determines which circuit is measuring, the upper circuit (0) or the lower circuit (1). The next three integers are numbers from 0 to 999 representing the number of samples that need to be measured. The next seven integers set the multiplexers value for IDE selection. 10 integers are dedicated to the value that is set to the 10-bit bank of capacitors from 11 to 20. Integer 21 is the value that turns the two transmission gates

implemented on the R1C1 and R16C1 IDEs. The last member is the ascii code of S or R which determines the mode of measurement to be a sweep of capacitance (S) or a fixed reference (R).

9.4 MCU Flowchart and the Code Snippet

The flowchart based on which the microcontroller works is shown in Figure 9.4. After a serial communication port is set up between the MCU and the PC, the command explained in Section 9.3 that is received from the GUI is decoded. The number of samples, the measurement mode, and the input of the multiplexers are then set based on the decoded command. After the measurement is performed, the data is sent to the GUI through the SPI port.

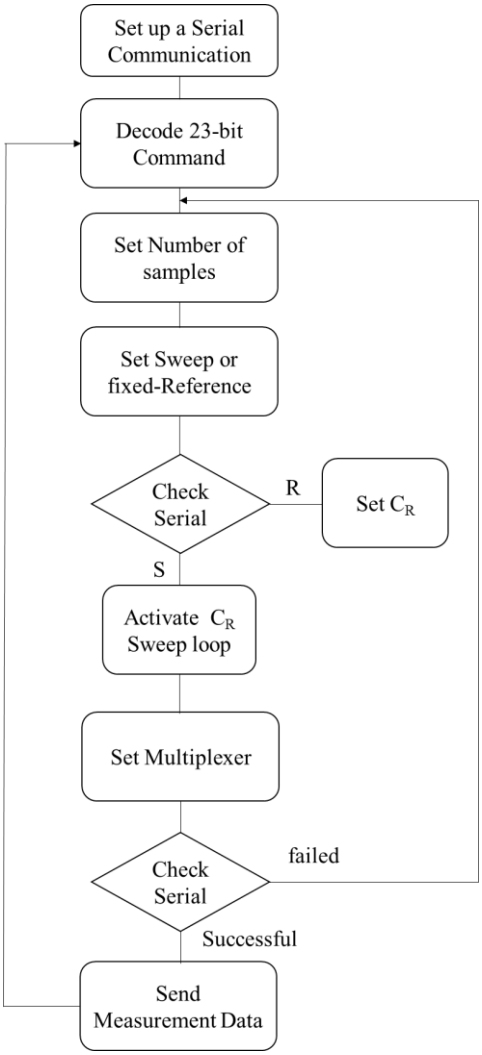


Figure 9.4: Flowchart of the MCU code for the array test bench

The code modules for setting the bank of capacitors and number of samples as well as the SPI communication are the same as the code modules of the non-array test bench. The code that runs on the Arduino DUE board is given below with explanations in the comment mode.

```
    CONST CHAR TERMINATION_CHAR = '#';
    CONST CHAR OPERATION_DONE= '-';
    CONST INT MASK=0X800;
    INT DATA;
    INT SAT_COUNTER=0; // COUNTS THE NUMBER OF TIMES THAT THE OUTPUT COMES SATURATED BY MISTAKE
    STRING COMMAND;
//{[0]UORD,[1]NS{0},[2]NS{1},[3]NS{2},[4]G,[5]F,[6]E,[7]D,[8]C,[9]B,[10]A,[11]CA10,[12]CA9,[13]CA8,[14]CA7,[15]CA6,[16]CA5,[17]CA4,[18]CA3,[
19]CA2,[20]CA1,[21]CS,[22]SWEEP(S) OR KNOWN REFERENCE(R)]
    SHORT RESULT = 0;
    INT N_SAMPLE = 10;
     // PIN DEFINITION
      #DEFINE SIN_U 22
      #DEFINE SCLK_U 24
```

```
#DEFINE E_U 26
#DEFINE F_U 28
#DEFINE G_U 30
#DEFINE CA10_U 32
#DEFINE SEL_NOUT 40
#DEFINE SEL_PHI 42
#DEFINE SIN_D 44
#DEFINE SCLK_D 46
#DEFINE E_D 48
#DEFINE F_D 50
#DEFINE G_D 52
#DEFINE A_U 25
#DEFINE B_U 27
#DEFINE C_U 29
#DEFINE D_U 31
#DEFINE CA10_D 33
#DEFINE A_D 47
#DEFINE B_D 49
#DEFINE C_D 51
#DEFINE D_D 53
VOID SETUP() {
SERIAL.BEGIN(115200);
PINMODE(SIN_U, OUTPUT);
PINMODE(SCLK_U, OUTPUT);
DIGITALWRITE(SCLK_U,LOW);
PINMODE(E_U, OUTPUT);
PINMODE(F_U, OUTPUT);
PINMODE(G_U, OUTPUT);
PINMODE(CA10_U, INPUT);
PINMODE(SEL_NOUT, OUTPUT);
PINMODE(SEL_PHI, OUTPUT);
PINMODE(SIN_D, OUTPUT);
PINMODE(SCLK_D, OUTPUT);
DIGITALWRITE(SCLK_D,LOW);
PINMODE(E_D, OUTPUT);
PINMODE(F_D, OUTPUT);
PINMODE(G_D, OUTPUT);
PINMODE(A_U, OUTPUT);
PINMODE(B_U, OUTPUT);
PINMODE(C_U, OUTPUT);
PINMODE(D_U, OUTPUT);
PINMODE(CA10_D, INPUT);
PINMODE(A_D, OUTPUT);
PINMODE(B_D, OUTPUT);
PINMODE(C_D, OUTPUT);
PINMODE(D_D, OUTPUT);
DELAY(10);
// PUT YOUR SETUP CODE HERE, TO RUN ONCE:
REG_PMC_PCER1 |= PMC_PCER1_PID36;// POWER UP PWM CLOCK
REG_PWM_WPCR = PWM_WPCR_WPCMD(0);//UNLOCK USER INTERFACE FOR PWM
REG_PWM_CLK = PWM_CLK_PREA(0) | PWM_CLK_DIVA(21); //CONFIG THE PWM CLOCK GENERATOR: CLOCK A, 84/21 = 4MHZ
REG_PWM_SCM = PWM_SCM_SYNC0 | PWM_SCM_SYNC1 ; //SYNCHRONIZE PHI1 AND PHI2 IN THE NEW VERSION FOR THEY HAVE
THE SAME FREQUENCY
//CONFIG PHI1, OUTPUT PIN PC2, DIGITAL PIN 34, HAS PWML0
REG_PIOC_ABSR |= PIO_ABSR_P2; // TRANSFER PIN CONTROL FROM PIO TO PWM
REG_PIOC_PDR |= PIO_PDR_P2;   // SET PWM PIN TO AN OUTPUT
REG_PWM_CMR0 = PWM_CMR_CPRE_CLKA | PWM_CMR_CPOL; //MODE CONFIGURATION FOR CHANNEL 0: CLOCK A, LEFT
ALIGNED, WAVEFORM START AT HIGH
```

```
    REG_PWM_CPRD0 = PWM_CPRD_CPRD(60);//CONFIG PERIOD FOR PWM 60/(4MHZ)
    REG_PWM_CDTY0 = PWM_CDTY_CDTY(16);// 80/3% DUTY CYCLE(16)
    REG_PWM_ENA = PWM_ENA_CHID0;// ENABLE PWM CHANNEL0
    //CONFIG PHI1 INVERTED TO BE USED AS NSS IN THE SPI, OUTPUT PIN PC3, DIGITAL PIN 35, HAS PWMH0 WHICH IS THE
COMPLEMENTARY PIN OF PWML0 (PHI1 )
    REG_PIOC_ABSR |= PIO_ABSR_P3; // TRANSFER PIN CONTROL FROM PIO TO PWM
    REG_PIOC_PDR |= PIO_PDR_P3;   // SET PWM PIN TO AN OUTPUT
    //CONFIG PHI2, OUTPUT PIN PC4, DIGITAL PIN 36
    REG_PIOC_ABSR |= PIO_ABSR_P4; // TRANSFER PIN CONTROL FROM PIO TO PWM
    REG_PIOC_PDR |= PIO_PDR_P4;   // SET PWM PIN TO AN OUTPUT
    REG_PWM_CMR1 = PWM_CMR_CPRE_CLKA | PWM_CMR_DTE| PWM_CMR_CPOL; //MODE CONFIGURATION FOR CHANNEL 0: CLOCK
A, LEFT ALIGNED, WAVEFORM START AT HIGH, WITH DEADTIME GENERATOR ENABLED BECAUSE WE WANT SOME DELAY IN THIS
CHANNEL
    REG_PWM_CPRD1 = PWM_CPRD_CPRD(60);//CONFIG PERIOD FOR PWM 60/(4MHZ)
    REG_PWM_DT1 = PWM_DT_DTL(4); //CREATE THE 1US(DELAY)
    REG_PWM_CDTY1 = PWM_CDTY_CDTY(12);// 80/6% DUTY CYCLE(12)
    REG_PWM_ENA = PWM_ENA_CHID1;// ENABLE PWM CHANNEL1
    //CONFIG PHI3, OUTPUT PIN PC6, DIGITAL PIN 38
    REG_PIOC_ABSR |= PIO_ABSR_P6; // TRANSFER PIN CONTROL FROM PIO TO PWM
    REG_PIOC_PDR |= PIO_PDR_P6;   // SET PWM PIN TO AN OUTPUT
    REG_PWM_CMR2 = PWM_CMR_CPRE_CLKA | PWM_CMR_CPOL ;//MODE CONFIGURATION FOR CHANNEL 0: CLOCK A, LEFT
ALIGNED, WAVEFORM START AT LOW |PWM_CMR_CALG
    REG_PWM_CPRD2 = PWM_CPRD_CPRD(3);//CONFIG PERIOD FOR PWM 2/(4MHZ)
    //REG_PWM_DT2 = PWM_DT_DTL(1); //CREATE THE 1US(DELAY)
    REG_PWM_CDTY2 = PWM_CDTY_CDTY(2);//50% DUTY CYCLE(1)
    REG_PWM_ENA = PWM_ENA_CHID2;// ENABLE PWM CHANNEL2
    //SPI SERIAL RECEIVE
    REG_PMC_PCER0 |= PMC_PCER0_PID24;// POWER UP SPI CLOCK
    REG_SPI0_WPMR = 0 << SPI_WPMR_WPEN; //UNLOCK USER INTERFACE FOR SPI
    //INSTANCE SPI0, MISO: PA25, (MISO), MOSI: PA26, (MOSI), SCLK: PA27, (SCLK), NSS: PA28, DIGITAL PIN 10
    REG_PIOA_ABSR |= PIO_ABSR_P25; // TRANSFER PIN CONTROL FROM PIO TO SPI
    REG_PIOA_PDR |= PIO_PDR_P25;   // SET MISO PIN TO AN OUTPUT
    REG_PIOA_ABSR |= PIO_ABSR_P26; // TRANSFER PIN CONTROL FROM PIO TO SPI
    REG_PIOA_PDR |= 0 << PIO_PDR_P26; // SET MOSI PIN TO AN INPUT
    REG_PIOA_ABSR |= PIO_ABSR_P27; // TRANSFER PIN CONTROL FROM PIO TO SPI
    REG_PIOA_PDR |= 0 << PIO_PDR_P27; // SET SCLK PIN TO AN INPUT
    REG_PIOA_ABSR |= PIO_ABSR_P28; // TRANSFER PIN CONTROL FROM PIO TO SPI
    REG_PIOA_PDR |= 0 << PIO_PDR_P28; // SET NSS PIN TO AN INPUT
    //REG_ISER0 = 1<<24; //ENABLE INTERRUPT CONTROLLER
    //REG_SPI0_CR = 1; // ENABLE SPI IT SHOULD MOVE TO WHERE WE WANT TO READ THE SPI PORT
    REG_SPI0_MR = 0; // SLAVE MODE
    REG_SPI0_IER = 1 << SPI_IER_RDRF | 1 << SPI_IER_OVRES | 1 << SPI_IER_NSSR; //ENABLE INTERRUPTS
    SPI0->SPI_CSR[0] = SPI_CSR_BITS_12_BIT; // CAPTURE ON FALLING EDGE AND TRANSFER 12 BITS.
  }
  VOID LOOP() {
    INT I=0;
    REG_SPI0_CR = 0; // FIRST DISABLE SPI READING TO CONFIG THE HARDWARE
    IF (SERIAL.AVAILABLE() > 0) // CHECK IF SERIAL IS AVAILABLE
    {
     COMMAND = SERIAL.READSTRINGUNTIL('\0'); // READ THE SERIAL AND PUT IN CMD
      IF(COMMAND[22]=='R'){
       HERE_R:
      IF (COMMAND[0]=='U')
      {DIGITALWRITE(SEL_NOUT,HIGH); DIGITALWRITE(SEL_PHI,HIGH);
      IF ( COMMAND[1]<'0' || COMMAND[1]>'9'){SERIAL.PRINT("E1");RETURN;}
      IF ( COMMAND[2]<'0' || COMMAND[2]>'9'){SERIAL.PRINT("E2");RETURN;}
      IF ( COMMAND[3]<'0' || COMMAND[3]>'9'){SERIAL.PRINT("E3");RETURN;}
```

```
        N_SAMPLE = 100*(COMMAND[1]-'0')+10*(COMMAND[2]-'0')+COMMAND[3]-'0'; // CONVERT N_SAMPLE_S TO INTEGER AND PUT IN
N_SAMPLE
        IF (COMMAND[4]=='0') {DIGITALWRITE(G_U,LOW);} ELSE IF (COMMAND[4]=='1') {DIGITALWRITE(G_U,HIGH);} ELSE
{SERIAL.PRINT("E4");RETURN;}
        IF (COMMAND[5]=='0') {DIGITALWRITE(F_U,LOW);} ELSE IF (COMMAND[5]=='1') {DIGITALWRITE(F_U,HIGH);} ELSE
{SERIAL.PRINT("E5");RETURN;}
        IF (COMMAND[6]=='0') {DIGITALWRITE(E_U,LOW);} ELSE IF (COMMAND[6]=='1') {DIGITALWRITE(E_U,HIGH);} ELSE
{SERIAL.PRINT("E6");RETURN;}
        IF (COMMAND[7]=='0') {DIGITALWRITE(D_U,LOW);} ELSE IF (COMMAND[7]=='1') {DIGITALWRITE(D_U,HIGH);} ELSE
{SERIAL.PRINT("E7");RETURN;}
        IF (COMMAND[8]=='0') {DIGITALWRITE(C_U,LOW);} ELSE IF (COMMAND[8]=='1') {DIGITALWRITE(C_U,HIGH);} ELSE
{SERIAL.PRINT("E8");RETURN;}
        IF (COMMAND[9]=='0') {DIGITALWRITE(B_U,LOW);} ELSE IF (COMMAND[9]=='1') {DIGITALWRITE(B_U,HIGH);} ELSE
{SERIAL.PRINT("E9");RETURN;}
        IF (COMMAND[10]=='0') {DIGITALWRITE(A_U,LOW);} ELSE IF (COMMAND[10]=='1') {DIGITALWRITE(A_U,HIGH);} ELSE
{SERIAL.PRINT("E10");RETURN;}
      // CONFIGURING THE CR FOR UPPER CIRCUIT
       //TURN OFF THE PHI CLOCK PULSES
       REG_PWM_DIS = PWM_DIS_CHID0;
       REG_PWM_DIS = PWM_DIS_CHID1;
       REG_PWM_DIS = PWM_DIS_CHID2;
       DELAYMICROSECONDS(5);
       //FULLY RESET THE INPUT REGISTERS
       FOR ( I = 13; I > 0 ; I--)
       {
        DIGITALWRITE(SIN_U, LOW);
        DIGITALWRITE(SCLK_U, LOW);
        DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
        DIGITALWRITE(SCLK_U, HIGH);
        DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
       }
       //APPLY INPUT SEQUENCES
       FOR ( I = 11; I <=21 ; I++)
       {
        IF (COMMAND[I] == '0')
        {
         DIGITALWRITE(SIN_U, LOW);
         DIGITALWRITE(SCLK_U, LOW);
         DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
         DIGITALWRITE(SCLK_U, HIGH);
         DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
        }
        ELSE IF (COMMAND[I] == '1')
        {
         DIGITALWRITE(SIN_U, HIGH);
         DIGITALWRITE(SCLK_U, LOW);
         DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
         DIGITALWRITE(SCLK_U, HIGH);
         DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
        }
        ELSE {SERIAL.PRINT("E"); SERIAL.PRINT(I);RETURN;}
       }
       DIGITALWRITE(SIN_U, LOW);
       DIGITALWRITE(SCLK_U, LOW);
       DELAYMICROSECONDS(5);
      //TURN THE PHI PULSES BACK ON
       REG_PWM_ENA = PWM_ENA_CHID0;
       REG_PWM_ENA = PWM_ENA_CHID1;
```

```
        REG_PWM_CMR2 = 0;
        REG_PWM_CMR2 = PWM_CMR_CPRE_CLKA;
        REG_PWM_CMR2 &= ~PWM_CMR_CPOL;
        REG_PWM_ENA = PWM_ENA_CHID2;
        DELAYMICROSECONDS(20);
            DELAYMICROSECONDS(50);
          //IF (!((DIGITALREAD(CA10_U)==LOW && COMMAND[11]=='0')||(DIGITALREAD(CA10_U)==HIGH &&
COMMAND[11]=='1'))){SERIAL.PRINT("EM");}
          //SERIAL.PRINTLN(TERMINATION_CHAR);
          }
          ELSE IF (COMMAND[0]=='D') {DIGITALWRITE(SEL_NOUT,LOW); DIGITALWRITE(SEL_PHI,LOW);
          IF ( COMMAND[1]<'0' || COMMAND[1]>'9'){SERIAL.PRINT("E1");RETURN;}
          IF ( COMMAND[2]<'0' || COMMAND[2]>'9'){SERIAL.PRINT("E2");RETURN;}
          IF ( COMMAND[3]<'0' || COMMAND[3]>'9'){SERIAL.PRINT("E3");RETURN;}
          N_SAMPLE = 100*(COMMAND[1]-'0')+10*(COMMAND[2]-'0')+COMMAND[3]-'0'; // CONVERT N_SAMPLE_S TO INTEGER AND PUT IN
N_SAMPLE
          IF (COMMAND[4]=='0') {DIGITALWRITE(G_D,LOW);} ELSE IF (COMMAND[4]=='1') {DIGITALWRITE(G_D,HIGH);} ELSE
{SERIAL.PRINT("E4");RETURN;}
          IF (COMMAND[5]=='0') {DIGITALWRITE(F_D,LOW);} ELSE IF (COMMAND[5]=='1') {DIGITALWRITE(F_D,HIGH);} ELSE
{SERIAL.PRINT("E5");RETURN;}
          IF (COMMAND[6]=='0') {DIGITALWRITE(E_D,LOW);} ELSE IF (COMMAND[6]=='1') {DIGITALWRITE(E_D,HIGH);} ELSE
{SERIAL.PRINT("E6");RETURN;}
          IF (COMMAND[7]=='0') {DIGITALWRITE(D_D,LOW);} ELSE IF (COMMAND[7]=='1') {DIGITALWRITE(D_D,HIGH);} ELSE
{SERIAL.PRINT("E7");RETURN;}
          IF (COMMAND[8]=='0') {DIGITALWRITE(C_D,LOW);} ELSE IF (COMMAND[8]=='1') {DIGITALWRITE(C_D,HIGH);} ELSE
{SERIAL.PRINT("E8");RETURN;}
          IF (COMMAND[9]=='0') {DIGITALWRITE(B_D,LOW);} ELSE IF (COMMAND[9]=='1') {DIGITALWRITE(B_D,HIGH);} ELSE
{SERIAL.PRINT("E9");RETURN;}
          IF (COMMAND[10]=='0') {DIGITALWRITE(A_D,LOW);} ELSE IF (COMMAND[10]=='1') {DIGITALWRITE(A_D,HIGH);} ELSE
{SERIAL.PRINT("E10");RETURN;}
          // CONFIGURING THE CR FOR UPPER CIRCUIT
        //TURN OFF THE PHI CLOCK PULSES
        REG_PWM_DIS = PWM_DIS_CHID0;
        REG_PWM_DIS = PWM_DIS_CHID1;
        REG_PWM_DIS = PWM_DIS_CHID2;
        DELAYMICROSECONDS(5);
        //FULLY RESET THE INPUT REGISTERS
        FOR ( I = 13; I > 0 ; I--)
        {
         DIGITALWRITE(SIN_D, LOW);
         DIGITALWRITE(SCLK_D, LOW);
         DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
         DIGITALWRITE(SCLK_D, HIGH);
         DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
        }
        //APPLY INPUT SEQUENCES
        FOR ( I = 11; I <=21 ; I++)
        {
         IF (COMMAND[I] == '0')
         {
          DIGITALWRITE(SIN_D, LOW);
          DIGITALWRITE(SCLK_D, LOW);
          DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
          DIGITALWRITE(SCLK_D, HIGH);
          DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
         }
         ELSE IF (COMMAND[I] == '1')
         {
```

```
          DIGITALWRITE(SIN_D, HIGH);
          DIGITALWRITE(SCLK_D, LOW);
          DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
          DIGITALWRITE(SCLK_D, HIGH);
          DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
         }
         ELSE {SERIAL.PRINT("E"); SERIAL.PRINT(I);RETURN;}
       }
       DIGITALWRITE(SIN_D, LOW);
       DIGITALWRITE(SCLK_D, LOW);
       DELAYMICROSECONDS(5);
       //TURN THE PHI PULSES BACK ON
       REG_PWM_ENA = PWM_ENA_CHID0;
       REG_PWM_ENA = PWM_ENA_CHID1;
       REG_PWM_CMR2 = 0;
       REG_PWM_CMR2 = PWM_CMR_CPRE_CLKA;
       REG_PWM_CMR2 &= ~PWM_CMR_CPOL;
       REG_PWM_ENA = PWM_ENA_CHID2;
       DELAYMICROSECONDS(20);
          DELAYMICROSECONDS(50);
          //IF (!((DIGITALREAD(CA10_D)==LOW && COMMAND[11]=='0')||(DIGITALREAD(CA10_D)==HIGH && COMMAND[11]=='1')))
{SERIAL.PRINT("EM");}
          //SERIAL.PRINTLN(TERMINATION_CHAR);

          }
          ELSE {SERIAL.PRINT("E0"); RETURN;}
           /// START READING THE DATA
           INT BUF[N_SAMPLE];
           REG_SPI0_CR = 1; //ENABLE SPI NOW TO READ THE CHIP OUTPUT
           FOR (INT I = 0; I < N_SAMPLE;)
           {
            IF (REG_SPI0_SR & 1)
            {
              DATA = REG_SPI0_RDR | MASK;
              IF (DATA==0XFFF && SAT_COUNTER<2 ) {SAT_COUNTER++; GOTO HERE_R;}  // CHECKS IF THE OUTPUT IS 4097(SATURATED).
IF IT HAPPENS IT SETS THE SIGNALS AGAIN AND CAPTURES NEW DATA
              //AND INCREMENTS SAT_COUNTER. IF IT HAPPENS AGAIN, AGAIN IGNORES AND SETS THE SIGNALS AND CAPTURES NEW
DATA. IF IT HAPPENS FOR THE THIRD TIME IT MEANS THE OUTPUT HAS A REALLY HUGE CAPACITANCE SO IT JUST RECORDS IT IN THE
BUFFER.
              ELSE IF (DATA==0XFFF && SAT_COUNTER>=2){FOR (I=0; I<N_SAMPLE; I++) {BUF[I]=0XFFF;} SAT_COUNTER=0; GOTO
PRINT_DATA_R;}
              DATA = DATA - 2047;
              BUF[I] = DATA;
              //REG_SPI0_RDR=0;
              I++;
            }
           }
           PRINT_DATA_R:
           CHAR BUFFERR[4*N_SAMPLE+N_SAMPLE];
           INT N = 0;
           FOR (INT I = 0; I < N_SAMPLE; I++) {
              N += SPRINTF (&BUFFERR[N], "%04D,", BUF[I]);
           }
           BUFFERR[4*N_SAMPLE+N_SAMPLE-1] = '\0';

           SERIAL.PRINT(BUFFERR);
           SERIAL.PRINT(TERMINATION_CHAR);
           //SERIAL.PRINT("\N");
```

```
      }
    ////////////\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\/FOR R
      ELSE IF (COMMAND[22]=='S')
      {
       FOR (INT J=0 ; J<1024 ; J++)
       {
        INT K=J;
        IF ((K&1)==0){COMMAND[20]='0';} ELSE IF ((K&1)==1) {COMMAND[20]='1';} ELSE {SERIAL.PRINT("ERROR 20");}
        K=K>>1;
        IF ((K&1)==0){COMMAND[19]='0';} ELSE IF ((K&1)==1) {COMMAND[19]='1';} ELSE {SERIAL.PRINT("ERROR 19");}
        K=K>>1;
        IF ((K&1)==0){COMMAND[18]='0';} ELSE IF ((K&1)==1) {COMMAND[18]='1';} ELSE {SERIAL.PRINT("ERROR 18");}
        K=K>>1;
        IF ((K&1)==0){COMMAND[17]='0';} ELSE IF ((K&1)==1) {COMMAND[17]='1';} ELSE {SERIAL.PRINT("ERROR 17");}
        K=K>>1;
        IF ((K&1)==0){COMMAND[16]='0';} ELSE IF ((K&1)==1) {COMMAND[16]='1';} ELSE {SERIAL.PRINT("ERROR 16");}
        K=K>>1;
        IF ((K&1)==0){COMMAND[15]='0';} ELSE IF ((K&1)==1) {COMMAND[15]='1';} ELSE {SERIAL.PRINT("ERROR 15");}
        K=K>>1;
        IF ((K&1)==0){COMMAND[14]='0';} ELSE IF ((K&1)==1) {COMMAND[14]='1';} ELSE {SERIAL.PRINT("ERROR 14");}
        K=K>>1;
        IF ((K&1)==0){COMMAND[13]='0';} ELSE IF ((K&1)==1) {COMMAND[13]='1';} ELSE {SERIAL.PRINT("ERROR 13");}
        K=K>>1;
        IF ((K&1)==0){COMMAND[12]='0';} ELSE IF ((K&1)==1) {COMMAND[12]='1';} ELSE {SERIAL.PRINT("ERROR 12");}
        K=K>>1;
        IF ((K&1)==0){COMMAND[11]='0';} ELSE IF ((K&1)==1) {COMMAND[11]='1';} ELSE {SERIAL.PRINT("ERROR 11");}
        K=K>>1;

            HERE_S:
       IF (COMMAND[0]=='U')
       {DIGITALWRITE(SEL_NOUT,HIGH); DIGITALWRITE(SEL_PHI,HIGH);
       IF ( COMMAND[1]<'0' || COMMAND[1]>'9'){SERIAL.PRINT("E1");RETURN;}
       IF ( COMMAND[2]<'0' || COMMAND[2]>'9'){SERIAL.PRINT("E2");RETURN;}
       IF ( COMMAND[3]<'0' || COMMAND[3]>'9'){SERIAL.PRINT("E3");RETURN;}
       N_SAMPLE = 100*(COMMAND[1]-'0')+10*(COMMAND[2]-'0')+COMMAND[3]-'0'; // CONVERT N_SAMPLE_S TO INTEGER AND PUT IN
N_SAMPLE
       IF (COMMAND[4]=='0') {DIGITALWRITE(G_U,LOW);} ELSE IF (COMMAND[4]=='1') {DIGITALWRITE(G_U,HIGH);} ELSE
{SERIAL.PRINT("E4");RETURN;}
       IF (COMMAND[5]=='0') {DIGITALWRITE(F_U,LOW);} ELSE IF (COMMAND[5]=='1') {DIGITALWRITE(F_U,HIGH);} ELSE
{SERIAL.PRINT("E5");RETURN;}
       IF (COMMAND[6]=='0') {DIGITALWRITE(E_U,LOW);} ELSE IF (COMMAND[6]=='1') {DIGITALWRITE(E_U,HIGH);} ELSE
{SERIAL.PRINT("E6");RETURN;}
       IF (COMMAND[7]=='0') {DIGITALWRITE(D_U,LOW);} ELSE IF (COMMAND[7]=='1') {DIGITALWRITE(D_U,HIGH);} ELSE
{SERIAL.PRINT("E7");RETURN;}
       IF (COMMAND[8]=='0') {DIGITALWRITE(C_U,LOW);} ELSE IF (COMMAND[8]=='1') {DIGITALWRITE(C_U,HIGH);} ELSE
{SERIAL.PRINT("E8");RETURN;}
       IF (COMMAND[9]=='0') {DIGITALWRITE(B_U,LOW);} ELSE IF (COMMAND[9]=='1') {DIGITALWRITE(B_U,HIGH);} ELSE
{SERIAL.PRINT("E9");RETURN;}
       IF (COMMAND[10]=='0') {DIGITALWRITE(A_U,LOW);} ELSE IF (COMMAND[10]=='1') {DIGITALWRITE(A_U,HIGH);} ELSE
{SERIAL.PRINT("E10");RETURN;}

    // CONFIGURING THE CR FOR UPPER CIRCUIT
     //TURN OFF THE PHI CLOCK PULSES
     REG_PWM_DIS = PWM_DIS_CHID0;
     REG_PWM_DIS = PWM_DIS_CHID1;
     REG_PWM_DIS = PWM_DIS_CHID2;
     DELAYMICROSECONDS(5);
     //FULLY RESET THE INPUT REGISTERS
```

```
      FOR ( I = 13; I > 0 ; I--)
      {
       DIGITALWRITE(SIN_U, LOW);
       DIGITALWRITE(SCLK_U, LOW);
       DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
       DIGITALWRITE(SCLK_U, HIGH);
       DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
      }
      //APPLY INPUT SEQUENCES
      FOR ( I = 11; I <=21 ; I++)
      {
       IF (COMMAND[I] == '0')
       {
        DIGITALWRITE(SIN_U, LOW);
        DIGITALWRITE(SCLK_U, LOW);
        DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
        DIGITALWRITE(SCLK_U, HIGH);
        DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
       }
       ELSE IF (COMMAND[I] == '1')
       {
        DIGITALWRITE(SIN_U, HIGH);
        DIGITALWRITE(SCLK_U, LOW);
        DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
        DIGITALWRITE(SCLK_U, HIGH);
        DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
       }
       ELSE {SERIAL.PRINT("E"); SERIAL.PRINT(I);RETURN;}
      }
      DIGITALWRITE(SIN_U, LOW);
      DIGITALWRITE(SCLK_U, LOW);
      DELAYMICROSECONDS(5);
     //TURN THE PHI PULSES BACK ON
      REG_PWM_ENA = PWM_ENA_CHID0;
      REG_PWM_ENA = PWM_ENA_CHID1;
      REG_PWM_CMR2 = 0;
      REG_PWM_CMR2 = PWM_CMR_CPRE_CLKA;
      REG_PWM_CMR2 &= ~PWM_CMR_CPOL;
      REG_PWM_ENA = PWM_ENA_CHID2;
      DELAYMICROSECONDS(20);
        DELAYMICROSECONDS(50);
        //IF (!((DIGITALREAD(CA10_U)==LOW && COMMAND[11]=='0')||(DIGITALREAD(CA10_U)==HIGH && COMMAND[11]=='1')))
{SERIAL.PRINT("EM");}
        //SERIAL.PRINTLN(TERMINATION_CHAR);
        }

        ELSE IF (COMMAND[0]=='D') {DIGITALWRITE(SEL_NOUT,LOW); DIGITALWRITE(SEL_PHI,LOW);
        IF ( COMMAND[1]<'0' || COMMAND[1]>'9'){SERIAL.PRINT("E1");RETURN;}
        IF ( COMMAND[2]<'0' || COMMAND[2]>'9'){SERIAL.PRINT("E2");RETURN;}
        IF ( COMMAND[3]<'0' || COMMAND[3]>'9'){SERIAL.PRINT("E3");RETURN;}
        N_SAMPLE = 100*(COMMAND[1]-'0')+10*(COMMAND[2]-'0')+COMMAND[3]-'0'; // CONVERT N_SAMPLE_S TO INTEGER AND PUT IN
N_SAMPLE
        IF (COMMAND[4]=='0') {DIGITALWRITE(G_D,LOW);} ELSE IF (COMMAND[4]=='1') {DIGITALWRITE(G_D,HIGH);} ELSE
{SERIAL.PRINT("E4");RETURN;}
        IF (COMMAND[5]=='0') {DIGITALWRITE(F_D,LOW);} ELSE IF (COMMAND[5]=='1') {DIGITALWRITE(F_D,HIGH);} ELSE
{SERIAL.PRINT("E5");RETURN;}
```

```
        IF (COMMAND[6]=='0') {DIGITALWRITE(E_D,LOW);} ELSE IF (COMMAND[6]=='1') {DIGITALWRITE(E_D,HIGH);} ELSE
{SERIAL.PRINT("E6");RETURN;}
        IF (COMMAND[7]=='0') {DIGITALWRITE(D_D,LOW);} ELSE IF (COMMAND[7]=='1') {DIGITALWRITE(D_D,HIGH);} ELSE
{SERIAL.PRINT("E7");RETURN;}
        IF (COMMAND[8]=='0') {DIGITALWRITE(C_D,LOW);} ELSE IF (COMMAND[8]=='1') {DIGITALWRITE(C_D,HIGH);} ELSE
{SERIAL.PRINT("E8");RETURN;}
        IF (COMMAND[9]=='0') {DIGITALWRITE(B_D,LOW);} ELSE IF (COMMAND[9]=='1') {DIGITALWRITE(B_D,HIGH);} ELSE
{SERIAL.PRINT("E9");RETURN;}
        IF (COMMAND[10]=='0') {DIGITALWRITE(A_D,LOW);} ELSE IF (COMMAND[10]=='1') {DIGITALWRITE(A_D,HIGH);} ELSE
{SERIAL.PRINT("E10");RETURN;}
        // CONFIGURING THE CR FOR UPPER CIRCUIT
      //TURN OFF THE PHI CLOCK PULSES
      REG_PWM_DIS = PWM_DIS_CHID0;
      REG_PWM_DIS = PWM_DIS_CHID1;
      REG_PWM_DIS = PWM_DIS_CHID2;
      DELAYMICROSECONDS(5);
      //FULLY RESET THE INPUT REGISTERS
      FOR ( I = 13; I > 0 ; I--)
      {
       DIGITALWRITE(SIN_D, LOW);
       DIGITALWRITE(SCLK_D, LOW);
       DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
       DIGITALWRITE(SCLK_D, HIGH);
       DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
      }
      //APPLY INPUT SEQUENCES
      FOR ( I = 11; I <=21 ; I++)
      {
       IF (COMMAND[I] == '0')
       {
        DIGITALWRITE(SIN_D, LOW);
        DIGITALWRITE(SCLK_D, LOW);
        DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
        DIGITALWRITE(SCLK_D, HIGH);
        DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
       }
       ELSE IF (COMMAND[I] == '1')
       {
        DIGITALWRITE(SIN_D, HIGH);
        DIGITALWRITE(SCLK_D, LOW);
        DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
        DIGITALWRITE(SCLK_D, HIGH);
        DELAYMICROSECONDS(5); // ORIGINALLY 5, I CHANGED TO 1
       }
       ELSE {SERIAL.PRINT("E"); SERIAL.PRINT(I);RETURN;}
      }
      DIGITALWRITE(SIN_D, LOW);
      DIGITALWRITE(SCLK_D, LOW);
      DELAYMICROSECONDS(5);
      //TURN THE PHI PULSES BACK ON
      REG_PWM_ENA = PWM_ENA_CHID0;
      REG_PWM_ENA = PWM_ENA_CHID1;
      REG_PWM_CMR2 = 0;
      REG_PWM_CMR2 = PWM_CMR_CPRE_CLKA;
      REG_PWM_CMR2 &= ~PWM_CMR_CPOL;
      REG_PWM_ENA = PWM_ENA_CHID2;
      DELAYMICROSECONDS(20);
        DELAYMICROSECONDS(50);
```

```
          //IF (!((DIGITALREAD(CA10_D)==LOW && COMMAND[11]=='0')||(DIGITALREAD(CA10_D)==HIGH && COMMAND[11]=='1')))
{SERIAL.PRINT("EM");}
          //SERIAL.PRINTLN(TERMINATION_CHAR);
          }
          ELSE {SERIAL.PRINT("E0"); RETURN;}
           /// START READING THE DATA
           INT BUF[N_SAMPLE];
           REG_SPI0_CR = 1; //ENABLE SPI NOW TO READ THE CHIP OUTPUT
           FOR (INT I = 0; I < N_SAMPLE;)
           {
            IF (REG_SPI0_SR & 1)
             {
              DATA = REG_SPI0_RDR | MASK;
              IF (DATA==0XFFF && SAT_COUNTER<=8*N_SAMPLE ) {SAT_COUNTER++; GOTO HERE_S;}  // CHECKS IF THE OUTPUT IS
4097(SATURATED). IF IT HAPPENS IT SETS THE SIGNALS AGAIN AND CAPTURES NEW DATA
              //AND INCREMENTS SAT_COUNTER. IF IT HAPPENS AGAIN, AGAIN IGNORES AND SETS THE SIGNALS AND CAPTURES NEW
DATA. IF IT HAPPENS FOR THE THIRD TIME IT MEANS THE OUTPUT HAS A REALLY HUGE CAPACITANCE SO IT JUST RECORDS IT IN THE
BUFFER.
              ELSE IF (DATA==0XFFF && SAT_COUNTER>8*N_SAMPLE){FOR (I=0; I<N_SAMPLE; I++) {BUF[I]=0XFFF;} SAT_COUNTER=0;
GOTO PRINT_DATA_S;}
              DATA = DATA - 2047;
              BUF[I] = DATA;
              //REG_SPI0_RDR=0;
              I++;
             }
           }
           PRINT_DATA_S:
           CHAR BUFFERR[4*N_SAMPLE+N_SAMPLE];
           INT N = 0;
           FOR (INT I = 0; I < N_SAMPLE; I++) {
              N += SPRINTF (&BUFFERR[N], "%04D,", BUF[I]);
           }
           BUFFERR[4*N_SAMPLE+N_SAMPLE-1] = '\0';
           SERIAL.PRINT(BUFFERR);
           SERIAL.PRINT(',');
          }
          SERIAL.PRINT(TERMINATION_CHAR);
         }
        ELSE {SERIAL.PRINT("E22");}
        }
       }
```

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