Step-up Converter Interfaces for Magnetron Power Supply

MATTHEW BAKALIAN

A THESIS SUBMITTED TO THE FACULTY OF GRADUATE STUDIES

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF APPLIED SCIENCE

GRADUATE PROGRAM IN ELECTRICAL ENGINEERING AND COMPUTER ENGINEERING

YORK UNIVERSITY

TORONTO, ONTARIO

DECEMBER 2022

Abstract

Fine particulate matter like carbon soot harms the respiratory system. One approach to reducing soot pollution is microwave-assisted soot oxidation. The magnetron, which generates microwave energy requires a high-voltage gain converter. In this thesis, a DC/DC converter is proposed to supply the two voltages required by a magnetron by utilizing dual resonant circuit modules. By combining the switches of the step-up resonant stage with a bridgeless power factor correction (PFC) stage, an AC/DC topology is proposed. The proposed AC/DC topology allows for a high power factor (PF) and reduced input conduction losses. The converter utilizes a parallel CL resonant circuit with voltage doubler output to achieve a high-voltage gain, and an LLC resonant circuit to provide the step-down. The circuit is then verified through PSIM with a peak of 1.8kW. A proof-of-concept hardware test with AC input testing step-up 822V and step-down 1.3V outputs simultaneously with a 0.96PF is performed.

Acknowledgement

I would like to extend my gratitude to Dr. John Lam for his continual guidance and support with this work, as well as his support during the entire duration of the master's program.

I would also like to thank the other graduate students who helped me with certain questions and challenges I faced during this work. Thank you to Kajanan Kanathipan, Mehdi Abbasi, and Reza Emamalipour

Thank you to the sponsors of this work, Omtec Inc.

Table of Contents

List of Tables

List of Figures

Nomenclature

Variables / Components

ω_s / f_s	Switching frequency
ω_0 / f_0	Resonant frequency
ω_r / f_r	Relative operating frequency
L_f	Input filter inductor
C_f	Input filter capacitor
L_B / L_{Boost}	Input boost inductor
D_1 & D_2	Input bridgeless diodes
C_{DC}	DC-link capacitor
S_1 & S_2	Primary resonant switch pair
S_3 & S_4	Secondary resonant switch pair
C_{r_CL}	Primary resonant capacitor
L_{m_CL}	Primary magnetizing inductor
C_{r_LLC}	Secondary resonant capacitor
L_{r_LLC}	Secondary resonant inductor
L_{m_LLC}	Secondary magnetizing inductor
N_{CL}	Primary transformer turns ratio
N_{LLC}	Secondary transformer turns ratio
D_3 & D_4	Primary resonant output diodes
D_5 & D_6	Secondary resonant output diodes

L_O	Output inductance
C_{O1} & C_{O2}	Output voltage doubler capacitors
C_{O3}	Low voltage output capacitor

Abbreviations

AC	Alternating current
D	Duty Ratio
DC	Direct current
BCM	Boundary conduction mode
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
DSP	Digital signal processor
IC	Integrated Circuit
PF	Power Factor
PSIM	Power Sim
PM	Particulate matter
Q	Quality factor
SMPS	Switch mode power supply
THD	Total Harmonic Distortion
ZCS	Zero-current switching
ZVS	Zero-voltage switching

1. Introduction

1.1. Carbon Soot

Carbon soot is a form of air pollution that is formed as a chain of carbon and hydrogen atoms. Soot is primarily formed as a result of fuel combustion [1] such as diesel engines, burning of fossil fuels, and wood fueled fires. From the fuel combustion, nucleation of soot molecules occurs and then undergo coalescence and agglomeration, which are processes in which small particles group together and form larger particles. These now larger, but still small, soot particles are known as a particulate matter (PM), which is one of the issues which makes it considered a pollutant. PM can cause both short term and long term risks to human health such as increased risk of myocardial infarction[1], myocardial ischemia[2], and risk of cardiovascular mortality [2]. One way to reduce soot mass is for it to go through a process of oxidation in which the soot particles are converted back to gasses such as CO and CO_2 [1][3]. One approach to increase the rate of soot oxidation is the use of microwave energy [4][5][6][7].

[1] One or more areas of the heart muscle don't get enough oxygen

[2] Reduced blood flow to the heart

1.2. Microwave Energy

Microwaves are a form of electromagnetic waves that operate in the 300MHz to 300GHz frequency range [8]. In this frequency band, the frequency range of 2.45Ghz +- 50MHz is commonly utilized to realize dielectric heating. This frequency range heats up particles by applying an electric force on charge particles which cause them to orientate in a direction, and then by modulating that field at the high frequency causes the particles to create friction which results in heating [9]. Dielectric heating differs from traditional heating in that the mass of particles that heat up will heat up from the inside and transfer the heat outwards allowing for a more uniform heating, instead of external heating that must transfer the heat to the center of the mass. This heating comparison can be observed in Figure 1-1.

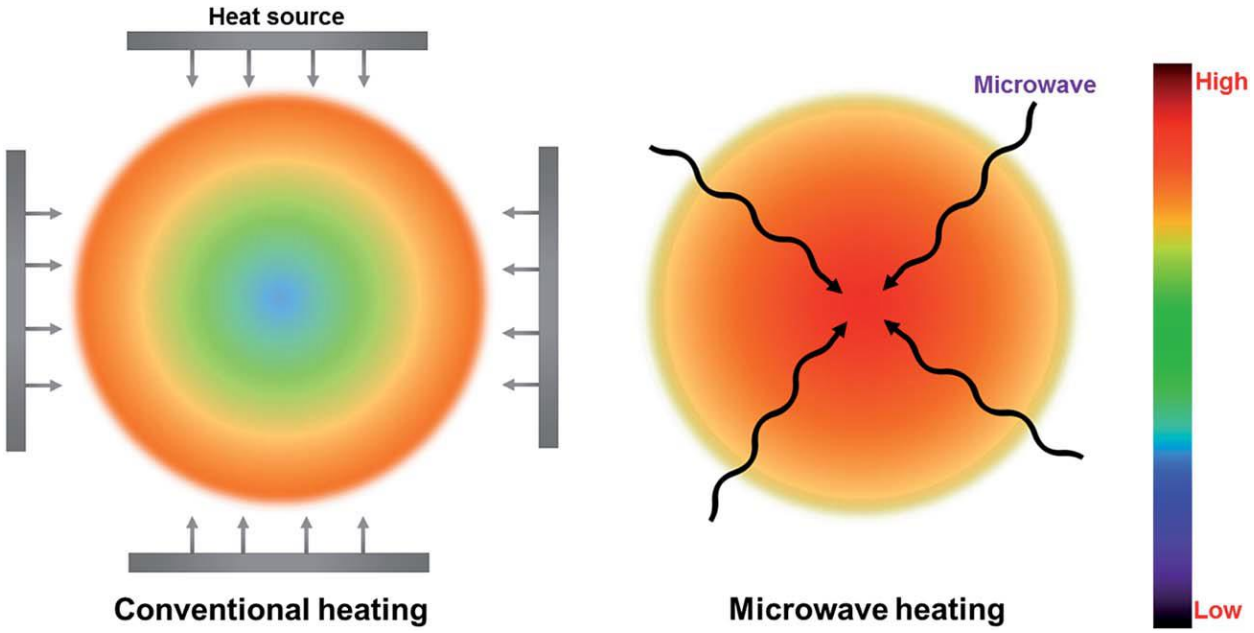


Figure 1-1: Conventional heating and microwave dielectric heating from [10]

Another unique feature of dielectric heating is that some materials will be 'microwave invisible'. This refers to the fact that some materials will not absorb microwave energy and will allow the waves to continue through them. An example of why this can be advantageous is heating up solutions, such as a solution containing hydrocarbons, which are flowing through a tube of a microwave invisible material. This will result in less energy being wasted, in comparison to conventional heating, on heating up the tube. To determine if a material will absorb microwave energy or let the waves pass through, Equation 1-1 and Equation 1-2 can be used. In these equations, ε' is the real component of the material's relative permeability, and ε'' is the imaginary component at the specific frequency. Tanδ is the materials ability to convert electromagnetic waves to heat [9], with a lower value representing a better ability to convert to heat. λ_o is the wavelength of the microwave, and D_p is the penetration depth. It can be noted that if tanδ is large, then D_p is also large. Thus, if a material does not absorb the energy, it will be able to pass through with ease.

$$\tan\delta = \frac{\varepsilon'}{\varepsilon''} \qquad \text{Equation 1-1}$$

$$D_P = \lambda_o \sqrt{\frac{\varepsilon'}{\varepsilon''}} \qquad \text{Equation 1-2}$$

Due to the characteristics of microwave energy, microwaves are used for multiple applications. Whilst many will recognize microwaves as a kitchen appliance which is commonly used for heating up food products, some industrial applications for microwave energy include microwave-assisted pyrolysis [11][12][13], soot oxidation [4][7][6][14], and heating of textiles[15] along other applications.

1.3. Magnetron

The magnetron is a device which is used to generate microwaves. The primary discussion of this paper will focus on the resonant cavity magnetron. A structural diagram of a resonant cavity magnetron can be observed in Figure 1-2. The generation of microwaves is done in multiple steps, the first being to apply a high current to the filament, which is sometimes referred to as the heater. By applying a high current, the filament heats up and undergoes a process known as thermionic emission in which the filament releases electrons into the surrounding space. The electrons then accelerate towards the anode due to the charge differential and emit radiation due to this acceleration. To extend the path that the electrons accelerate over permanent magnets are used, or electrically induced magnets for larger industrial magnetrons. During this extended path that the electrons take, the anodes resonant cavities will have an induced oscillations created by the loose electrons getting in close proximity to the anode, which causes the anodes resonant cavities to shift electrons away and create shifting fields that will make up the magnetic fields which are then outputted by the magnetron [16].

To realize the above operation the resonant cavity magnetron will require a voltage between the anode and cathode, and additionally a high current through the filament. This results in two different voltage requirements for the magnetron, which are visually shown in Figure 1-3. The first voltage in this diagram, voltage 1, is a high magnitude voltage with the negative terminal connected to the cathode and the positive grounded to the anode. The second voltage, voltage 2, is connected across the cathode and filament to provide the high current for thermionic emission to be possible.

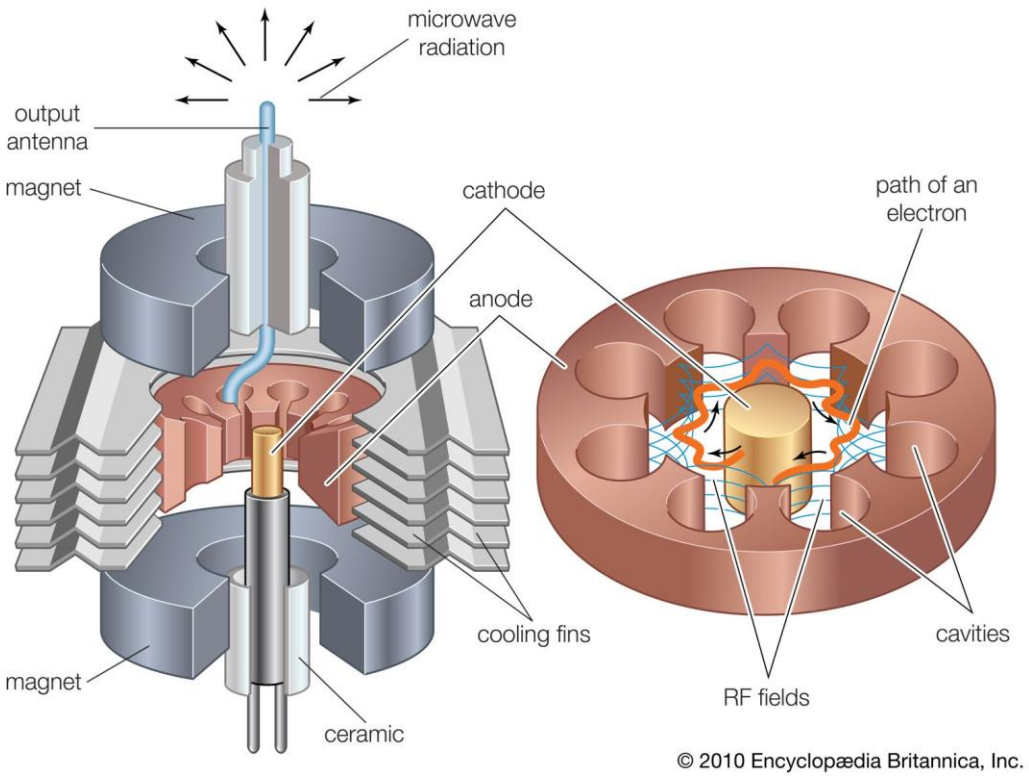


Figure 1-2: Magnetron breakdown view [17]

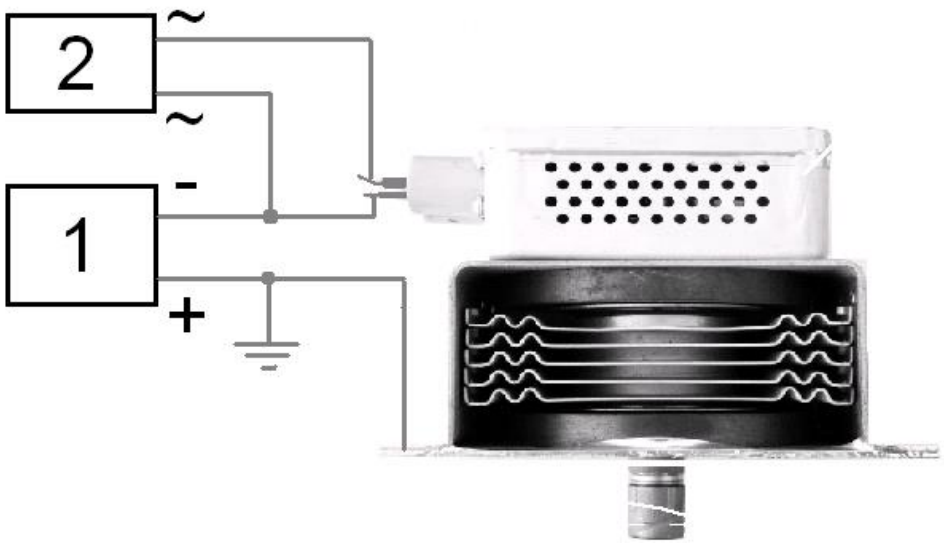


Figure 1-3: Connection scheme of the magnetron unit from [18].

Connection 1 is high voltage between anode (+) and cathode (-) and connection 2 is low voltage filament connection

1.4. Power Converters

1.4.1. Switching Power Losses

Whilst switch mode power supplies (SMPS) are able to operate with high efficiency, they still experience inefficiencies. Two of these inefficiencies can be observed at the switches, switching losses and conduction losses.

Switching losses occur when the switch turns on or off. This is a result of semiconductors having an internal capacitance which causes the voltage across the switch to not be able to instantaneously turn on or off, but instead have a turn on time referred to as the fall time and turn off time referred to as the rise time in datasheets. This rise and fall time of the voltage results in the switches having a voltage at the same time current is flowing which results in a power loss known as hard switching. This can be observed in Figure 1-4 which shows a sample voltage in black and current in blue for a switching event and the switching power losses in red, along with a mathematical expression provided by Equation 1-3.

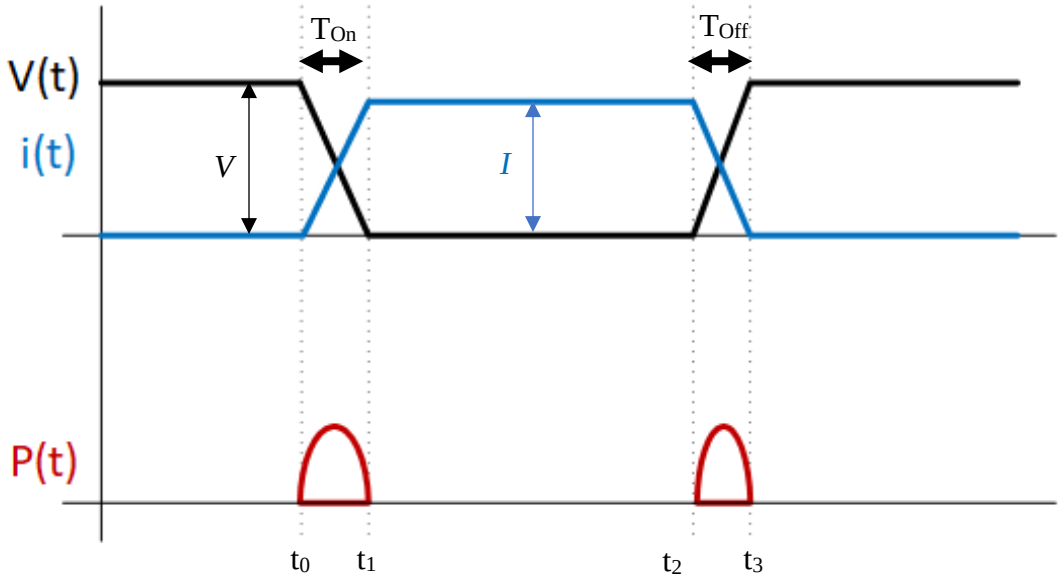


Figure 1-4: Hard switching example diagram

$$P_{Loss} = 0.5VI(T_{On} + T_{Off})f_s \quad \text{Equation 1-3}$$

One approach to reduce this power loss is known as soft switching. Soft switching is often achieved by utilizing an anti-parallel diode across the switch during the turn-on period and designing the circuit such that the current will be negative when the switch turns on. When the current is negative, the voltage is able to reach zero before current becomes positive, this is known as zero-voltage switching (ZVS). For the turn-off losses a snubber circuit, which can be as simple as a parallel capacitor, can be placed across the switch to prevent the voltage from instantaneously going to its max value whilst the current is still flowing through the switch. When the current can drop to zero before the voltage across the switch can increase, this is known as zero-current switching (ZCS). In addition to these two changes, a small dead-time would be applied to the switches to allow for the voltage and current drops to finish going to zero before turning on some other switch in the circuit and causing a short circuit being created. It should be noted that for practical design that MOSFET's have an output capacitance and a body diode which can be utilized for soft switching without the purchase of additional components.

The second inefficiency, conduction losses, is caused by the switch having an internal resistance. For MOSFET's this resistance is often referred to as $R_{DS,On}$ in the datasheets. This resistance results in conduction losses when the switch is on, and current is flowing through the switch based on the well-established ohm's law given in Equation 1-4. To reduce this loss either the current through the switch must be reduced, which may not always be possible, or by selecting a switch which has the lowest $R_{DS,On}$ whilst still complying with other requirements.

$$P = I_{RMS}^2 R_{DS,On} \quad \text{Equation 1-4}$$

1.4.2. Power Factor

When using a circuit that will be connected to an AC power source, the power factor (PF) must be considered to ensure power is not wasted. PF is defined by Equation 1-5 in which P is the real power, given by Equation 1-6, and S is the apparent power, given by Equation 1-7. For an ideal sinusoidal current and voltage, the PF will express the phase shift between input voltage and input current, given by θ, which can be expressed as the cosine of the angle equalling the PF, given by Equation 1-8.

$$PF = \frac{P}{S} \quad \text{Equation 1-5}$$

$$P = V_{RMS} I_{RMS} \cos(\theta) \quad \text{Equation 1-6}$$

$$S = V_{RMS} I_{RMS} \quad \text{Equation 1-7}$$

$$PF_{Ideal} = \cos(\theta) \quad \text{Equation 1-8}$$

When the input current is not perfectly sinusoidal, the harmonics of the current also factor into the calculation of the power factor. Equation 1-9 [19] expresses the PF for a non ideal input current in which $I_{1,RMS}$ is the fundamental harmonic of the input current and θ_1 is the phase between the fundamental current harmonic and the voltage. Even for the non ideal equation, the voltage is assumed to be ideal. When dealing with a non ideal input current, it is also beneficial to know the total harmonic distortion (THD), provided by Equation 1-10, as this metric can be used to determine if the harmonics are the source of a decreased power factor.

$$PF_{non-ideal} = \frac{I_{1,RMS}\cos(\theta_1)}{I_{total,RMS}}$$ Equation 1-9

$$THD = 100\frac{\sqrt{\sum_{n=2}^{\infty} i_{n\_rms}}}{i_{1\_rms}}$$ Equation 1-10

In addition to low power factor resulting in more wasted power, having a low power factor can create new limits on equipment that is used to distribute electricity. Notably, a low PF can put extra current stress on conductors such as distribution wires as the phase shift and poor harmonic distortion result in higher current peaks [20]. The larger current peaks will also propagate through the switches in the SMPS resulting in bulkier and more expensive components being required.

1.4.3. Buck/Boost Converters

Three of the basic converters in power electronics are the boost, buck, and buck-boost converters. These three converters offer the ability to take a DC input and either step it up, step it down, or do both respectively. As the magnetron required a high voltage, which would be the result of a step-up, and a separate low voltage, resulting from a step-down, the boost and buck converters could potentially be considered.

The boost converter is a converter that is able to take a DC input and step it up to a higher voltage by adjusting the duty ratio of a single switch at a fixed frequency and can be observed in Figure 1-5 (b). The gain for the boost converter is given by Equation 1-11 in which D represents the duty ratio of the switch. Based on this equation, the gain of the boost converter can theoretically boost the input by a factor of one to infinity however, in practical use the gain would become too susceptible to factors such as noise and switch delays at large gains.

$$\frac{v_o}{v_i} = \frac{1}{1-D} \qquad \text{Equation 1-11}$$

The buck converter is a converter that can take a DC input and steps it down to a lower voltage by adjusting the duty ratio. The buck converter can be observed in Figure 1-5 (a). The gain for the buck converter is given by Equation 1-12. Based on this equation, the buck converter can step-down the input by a factor of zero to one.

$$\frac{v_o}{v_i} = D \qquad \text{Equation 1-12}$$

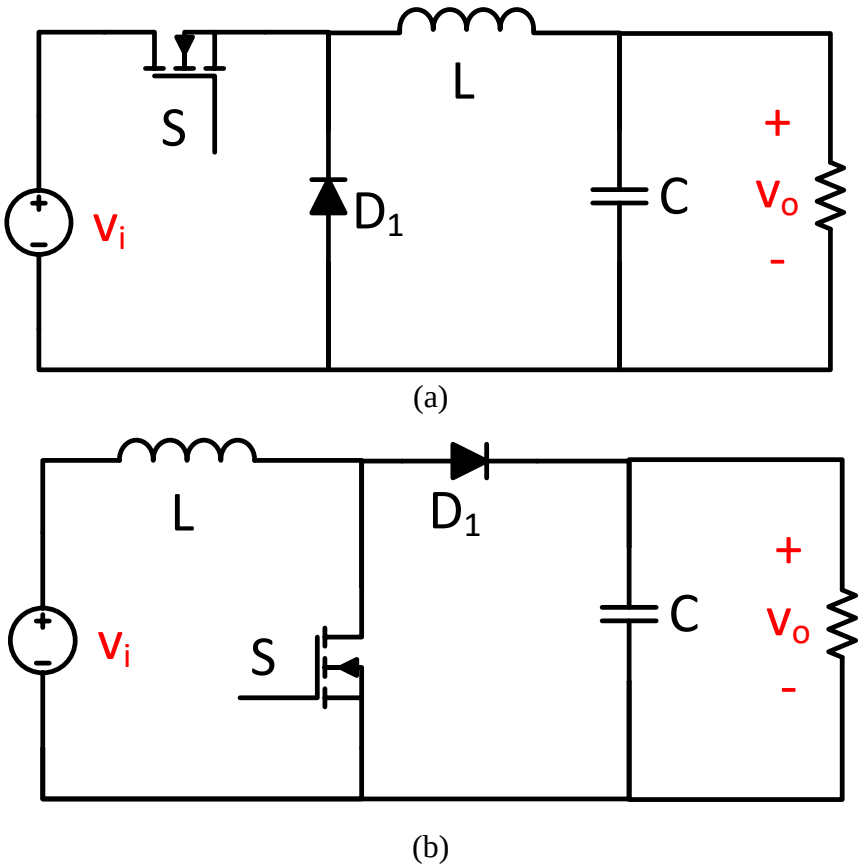


Figure 1-5: (a) buck converter, (b) boost converter.

These converters do have some major drawbacks, such as the switching power losses that will occur due to the one switch not operating with any soft switching conditions. Additionally, the topology does not allow for the output to be isolated, which could cause issues when a high voltage output is needed. As these converters also require a DC input, they would require additional circuitry to provide the conversion of AC to DC.

1.4.4. Resonant Converters

Resonant converters are a type of topology that take a DC input, convert the voltage to AC using a switch network, pass the AC voltage through a resonant stage which can either step-up or step-down the voltage based on the design, and then to a rectification and filtering stage. A block diagram of a generic resonant converter is shown in Figure 1-6. Each of these stages have a function for the resonant converter and can be achieved in multiple ways.

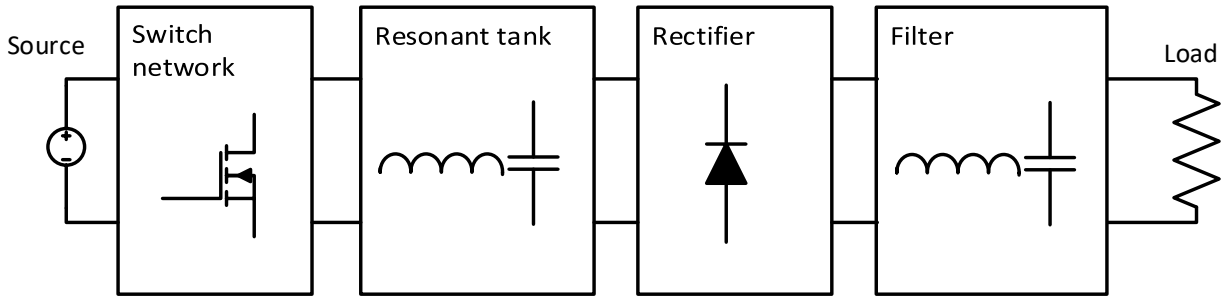


Figure 1-6: Resonant circuit block diagram.

The switch networks function in the resonant converter is to convert the DC input into a square wave. Converting the DC input to a square wave will result in the output of the switch network stage having high frequency components, which will correspond to the frequency at which the switches are operating and allow for the voltage to interact with inductive and capacitive components of the resonant tank. Some examples of switch networks are a full bridge inverter which operates with four switches, a half-bridge inverter which operates with two switches and two capacitors, and a totem pole PFC inverter which has two switches and two diodes as well as being capable of operating with an AC input at near unity PF. These three examples are shown in Figure 1-7, with the accompanying source type shown.

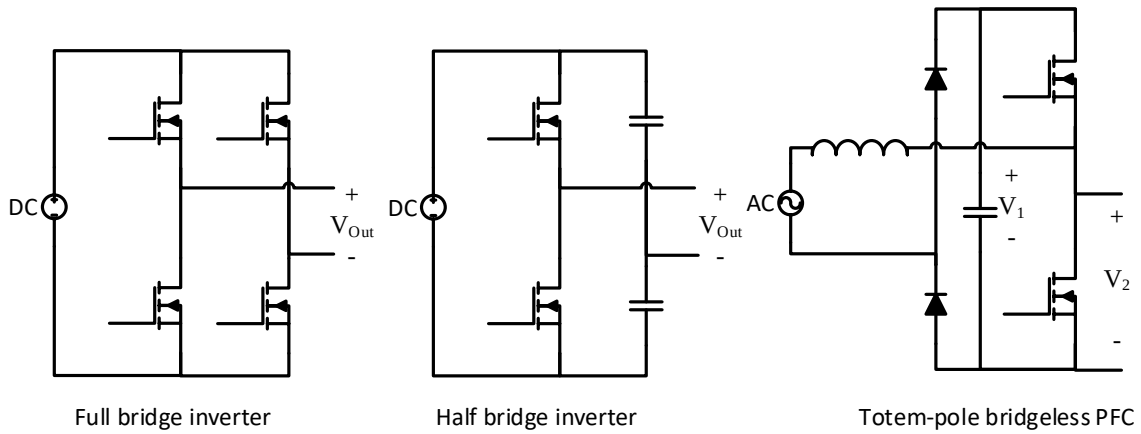


Figure 1-7: Example switch networks

In conjunction with the switching frequency set by the switch network, the resonant tank can step-up or step-down the voltage that will be outputted by the converter. This is done by operating the switches in the switch network at a frequency relative to the resonant tank's fundamental frequency, as near this frequency the gain of the voltage will change based on the type of resonant tank used and the specific values of the inductors, capacitors, and effective resistance of the load. The resonant tank is also able to provide galvanic isolation of the input and output by use of a transformer, which has an effective parallel and series inductance which can be used as part of the resonant tanks design. In addition to applying a gain to the voltage, the resonant tank can also be used to apply a phase shift to the current, which can assist in operating the switches in the switch network with soft switching. Three examples of resonant tank stages are shown in Figure 1-8. Each of these resonant tanks will provide a different voltage gain and current phase shift profile, which can be picked based on the requirements of the overall converter. For these examples the series inductors L_S can be realized with a transformer's leakage inductance, and the parallel inductors L_P can be realized with a transformer's magnetizing inductance. This allows for less components to be required.

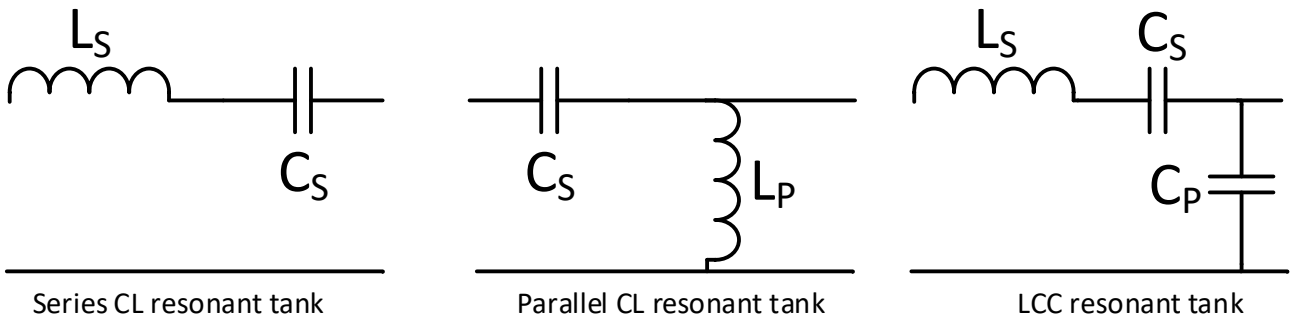


Figure 1-8: Example resonant tank stages

Next is the rectifier stage, which will take the AC output of the resonant tank and rectify it in such a way as to make the output of this stage all positive voltage. This stage is typically done with either a full bridge rectifier comprising of four diodes or if the transformer used in the previous stage is center tapped, a center tapped full wave rectifier can be used comprising of only two diodes. This stage can also be performed with circuits such as a voltage doubler to further increase the voltage. The three examples mentioned are also shown in Figure 1-9. The final stage is the filter stage, which acts as a low pass filter such that the output is a stable DC output. This is typically done with a capacitor in parallel with the load, and potentially an inductor in series.

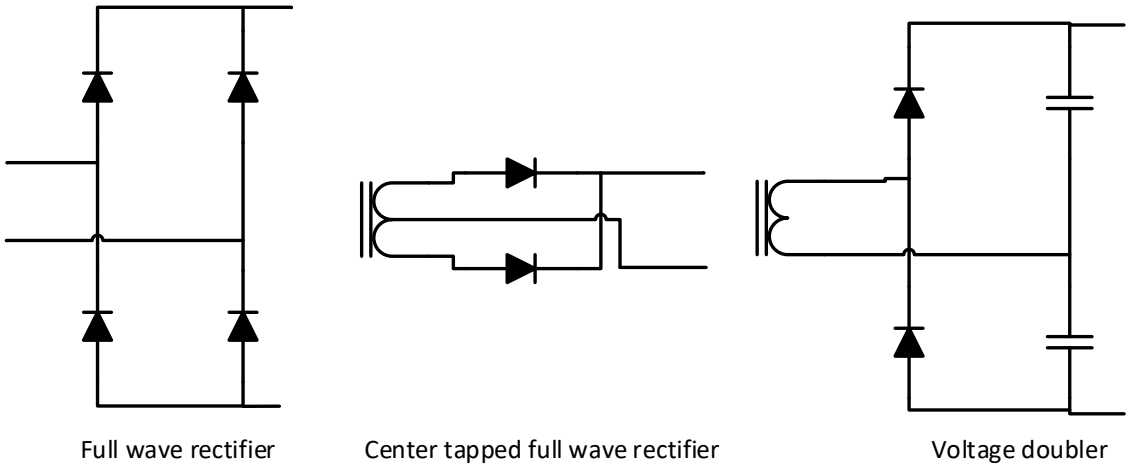


Figure 1-9: Example rectifier stages

Whilst resonant circuit may use significantly more components than that of buck and boost converters, they come with some major advantages not available to those topologies. One of the biggest advantages of the resonant circuit is its ability to operate the switches with soft switching. As mentioned in section 1.4.1, soft switching is achieved when either the voltage or current of a switch is zero before the other parameter increases. This is achieved primarily by the resonant stage which can apply a phase shift to the current. Taking this phase shift current, the switches in the switch network will have an anti-parallel diode across them that allows the current to flow opposite the typical direction, which allows the current through the switch to be zero whilst the voltage is dropping, achieving ZVS turn-on. For the turn-off, a snubber capacitor is used across the switch to allow the current to drop/reduce whilst slowing the rate at which the voltage can increase, allowing for ZCS or near ZCS turn-off. The resonant circuit is also able to utilize a transformer between the input stages and the output, which can be used for galvanic isolation.

1.4.5. Existing Magnetron Power Converters

To better understand the existing power converters that are used for magnetrons, some topologies from literature will be reviewed.

Figure 1-10 shows the converter proposed in [21]. The converter utilizes a large number of components on the output stage, notably the 24 diodes and 6 capacitors along with the 3 transformers used for only the high voltage cathode-anode output. This will cause this circuit to be more expensive to produce, require more space, and result in more conduction losses as a result of having more diodes. Additionally, this converter utilizes a DC input which means it will either need to be connected to an additional circuit to provide AC/DC PFC or have a DC supply available. To achieve the step-up of the input DC voltage the converter uses a full bridge inverter followed by three parallel connected resonant tanks that are connected in series through transformers and full bridge rectifier outputs. For the filament voltage, the paper suggests using an AC source directly connected to a transformer to supply the filament voltage. Whilst the converter has such a large number of diodes and transformers, due to the series output the voltage rating of each of the output diodes and the winding isolation of each of the transformers can be lower. However, the use of multiple transformers also results in each output stage having slight voltage variations due to minor differences in transformer windings turns ratio or impedances.

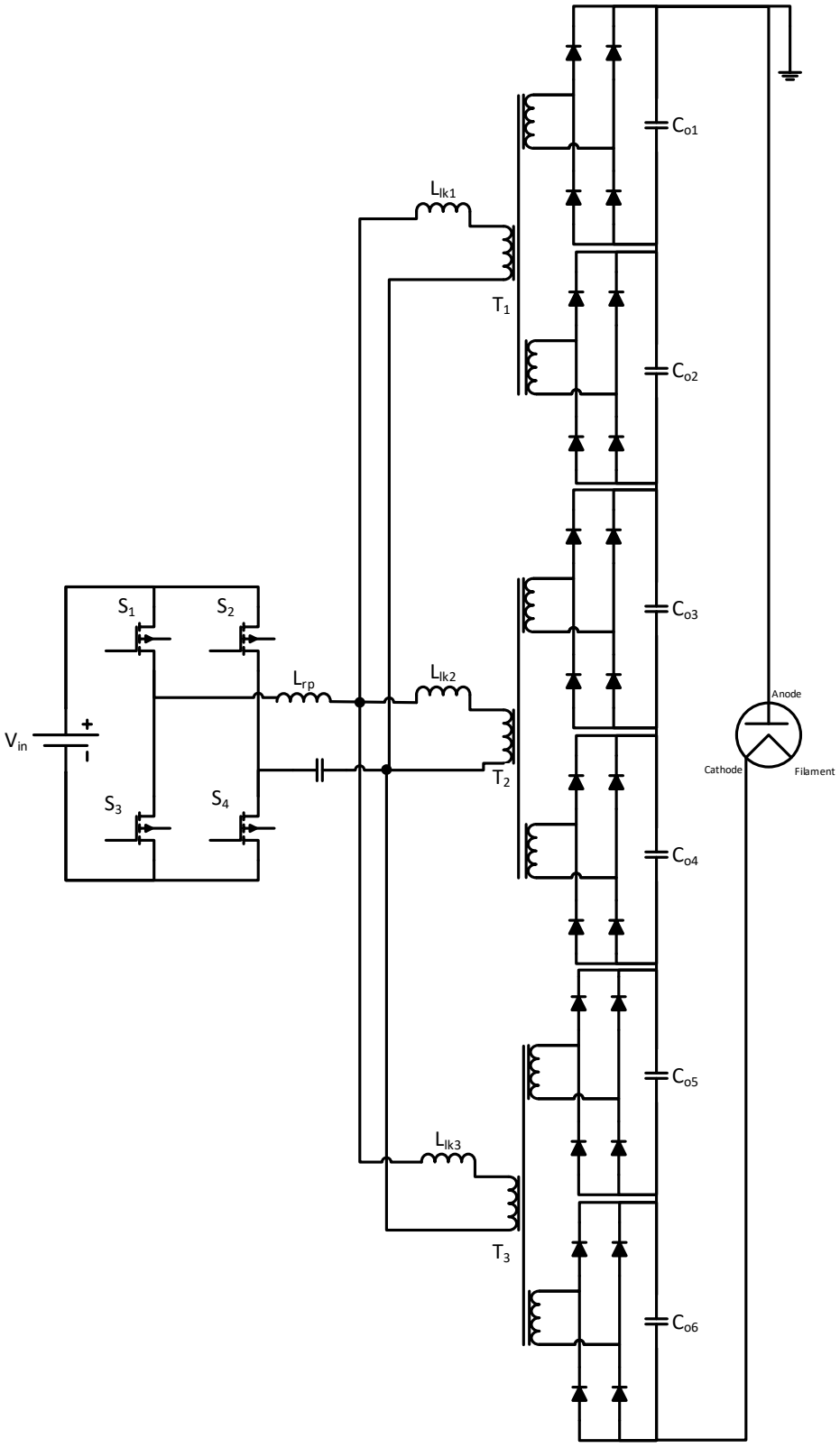


Figure 1-10: Magnetron power supply from [21]

Figure 1-11 shows the converter proposed in [22]. The converter does utilize an AC/DC PFC stage, however this is done as a separate stage from the resonant stage. This again results in more components being used. The accompanying paper mentions an efficiency of 95% to 96% for this PFC stage, which also results in a decrease to the topologies overall efficiency, and an efficiency of 95% to 96% for the step-up high voltage stage. This brings the PFC and step-up efficiency to about 92%. However, the paper does not include the efficiency of the filament supply, which is due to the filament supply utilizing a switch that will undergo hard switching, which results in the efficiency of the converter to decrease significantly. This converter operates with 8 diodes, with 2 of the diodes being high voltage, and 6 switches.

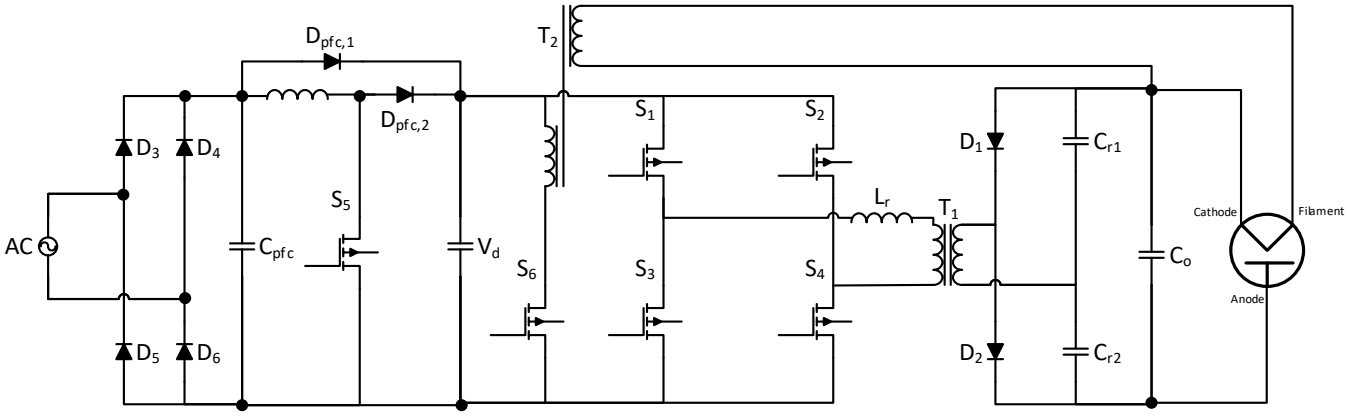


Figure 1-11: Magnetron power supply from [22]

Finally, in [23] a converter for extremely low power magnetrons is discussed. This topology is discussed from the DC-to-DC stage but requires additional circuitry for an AC input and the filament voltage. The DC-to-DC stage uses a flyback resonant topology to obtain the boost along with a parallel stacked transformer connected in series to obtain the output voltage required. For these stages, the circuit requires 1 switch and 5 diodes. Whilst this converter operates as a DC-DC converter, the paper mentions an additional PFC stage is used to supply the DC input which

would result in an additional 1 or 2 switches, as well as multiple additional diodes. This paper also mentions that the converter can only be operated with magnetrons with a low power requirement.

From these three topologies discussed Table 1 was created to summarize each of the designs.

Table 1: Magnetron Power Supplies from Literature

	Topology 1 [21]	**Topology 2** [22]	**Topology 3** [23]
Configuration	DC input with full bridge resonant and parallel in series output	Full bridge rectifier followed by PFC stage supplying DC voltage hard switching heater switch and step-up full bridge resonant converter with voltage doubler output	DC input with Quasi-resonant flyback topology followed by a boost circuit consisting of parallel transformer windings connected in series out.
Semiconductor Count	Diodes: 24 Switches: 4	Diodes: 8 Switches: 6	Diodes: 5 Switches: 1
Efficiency	Not mentioned	91.5%	> 85%
Voltage Gain	300V to 2.5kV-5kV	220Vrms to 4kV	85-264Vrms to 4kV
Power Output	5kW	400W 1600W (pulsed)	200W
Notes	DC input meaning additional circuitry needed for AC input	Operates at lower power by pulsing output on and off	Additional circuity required for filament voltage and AC input which are only mentioned but not discussed in detail. Only works for extremely low power magnetrons

1.5. Thesis Motivation

Observing alternative magnetron power supply topologies discussed in literature, a new double DC output power supply topology will be proposed to serve as the power supply for the full project work shown in Figure 1-12. The proposed topology will have the following features

1. Based on existing supplies from literature requiring an additional PFC stage / circuit to supply the converters DC input / DC-link that will result in some inefficiency, the proposed converter will have a combined PFC stage with the step-up stage to operate with an AC input whilst providing near unity PF, low harmonics, and a high efficiency value which are in line or improvements over the converters discussed in literature. As well as decreasing the number of semiconductor components required.
2. Multiple converters from literature do not allow for the filament to be operated individually, as such the proposed converter should offer the ability to operate the low filament voltage independently of the high voltage output, to allow for low filament voltage to decrease after the high voltage enters the oscillating region of operation.
3. Operate all switches with ZVS turn-on and near ZCS turn-off soft switching to reduce power losses to switches and allow for higher frequency operation, further allowing for component size reductions.

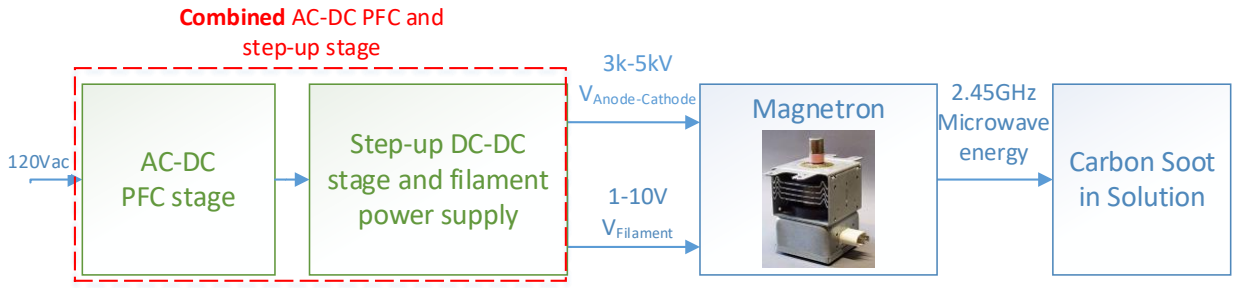


Figure 1-12: Thesis contribution block diagram

2. Proposed Topologies

2.1. DC-DC Proposed Topology

The proposed topology in this paper will come in two stages, one with a DC input and another with an AC input which will be introduced in section 2.2. The first stage will be for a DC input that will provide a DC-DC conversion for both of the outputs that will consist of two resonant converters to supply one high voltage output and one low voltage output for the magnetron unit. The proposed topology can be observed in Figure 2-1.

The circuit consists of two resonant converters, a parallel CL resonant step-up converter, and an LLC resonant step-down converter. The step-up inverter consists of $Switch_1$ abbreviated as S_1, $Switch_2$ abbreviated as S_2, and C_{DC}. The CL resonant tank and voltage doubler output filter consist of C_{r_CL}, L_{m_CL}, T_1, D_3, D_4, L_O, C_{O1}, C_{O2}, and the magnetron's anode to cathode connection, $V_{Anode-Cathode}$. The step-down inverter starts with the shared C_{DC} and uses $Switch_3$ abbreviated as S_3, and $Switch_4$ abbreviated as S_4. The LLC resonant tank and center tapped full wave rectifier consists of C_{r_LLC}, L_{r_LLC}, L_{m_LLC}, T_2, D_5, D_6, C_{O3}, and the magnetrons filament connection, $V_{Filament}$.

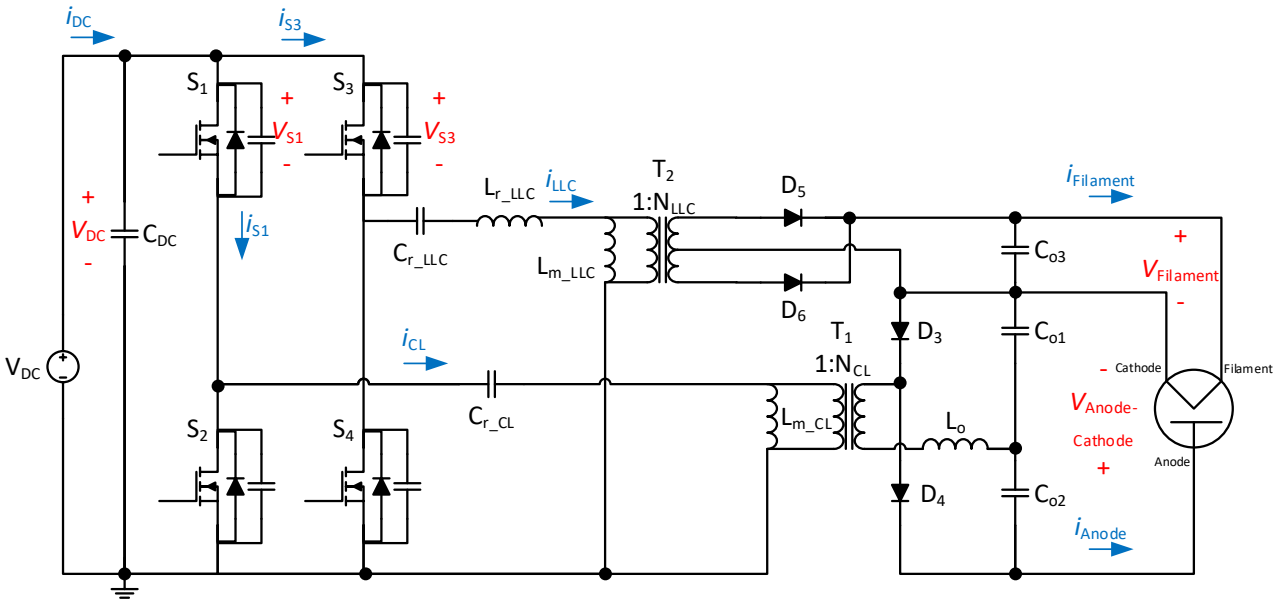


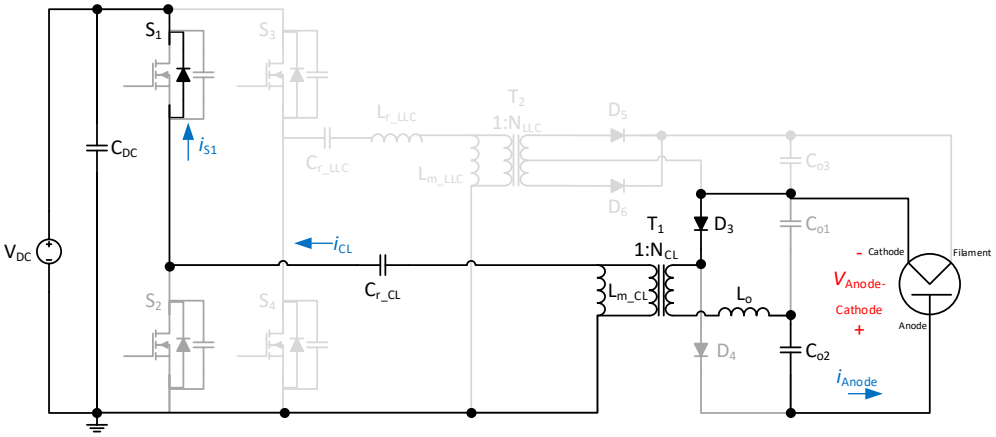
Figure 2-1: Proposed doubled output DC-DC converter

2.1.1. CL Resonant Step-Up and Voltage Doubler

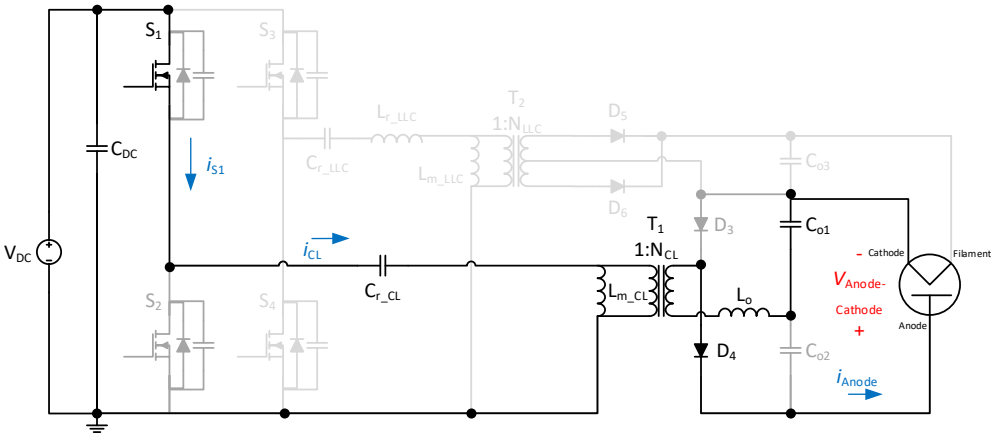
The step-up resonant circuit of the converter serves to provide a high voltage across the anode and cathode of the magnetron. The step-up portion of the converter takes the voltage V_{DC} set by the capacitor C_{DC} , and steps that up using a parallel CL resonant circuit, a step-up transformer, and a voltage doubler circuit. This part of the circuit operates with 6 modes as described below. The following stages are shown in Figure 2-2.

1. [t_0 < t < t_1] Mode 1 starts with S_1 turning on. During this interval, the anti-parallel diode in the switch has current flowing through it, being provided by the resonant circuit.
2. [t_1 < t < t_2] Mode 2 starts when the anti-parallel diode's current reaches zero, and S_1 starts to conduct. This allows the switch to achieve zero-voltage switching (ZVS) turn-on. During this mode, the resonant circuit is supplied with V_{DC} Volts.

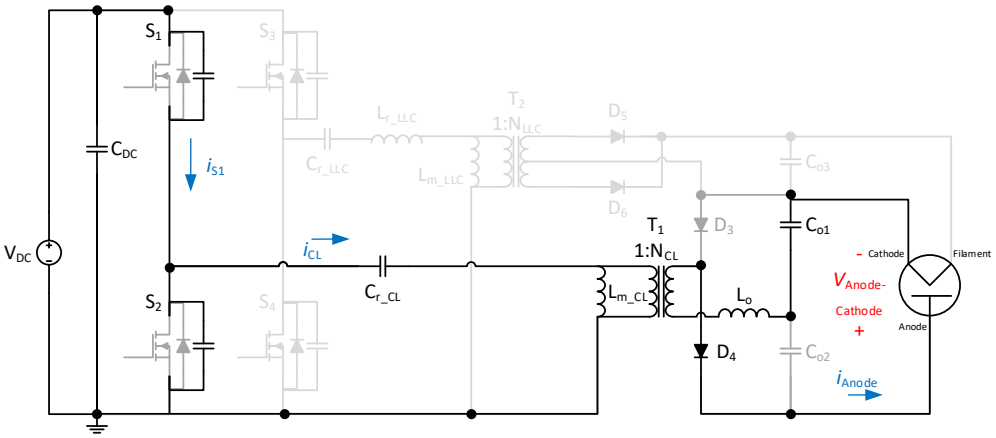
3. [t_2 < t < t_3] Mode 3 occurs when S_1 turns off. During this period, the snubber capacitor C_{S1} charges up from zero to V_{DC} whilst the snubber C_{S2} discharges to zero volts. The snubber capacitor allows for S_1 to have near zero-current switching (ZCS) turn-off.
4. [t_3 < t < t_4] Mode 4 occurs when S_2 turns on. During this interval, the anti-parallel diode of S_2 conducts. This interval ends when the current across the anti-parallel diode crosses zero.
5. [t_4 < t < t_5] Mode 5 starts when the anti-parallel diode current crosses zero and S_2 starts to conduct. This allows S_2 to achieve ZVS turn-on. During this mode, the resonant voltage input is zero volts.
6. [t_5 < t < t_6] Mode 6 occurs with S_2 turning off. The voltage across the switch capacitor C_{S2} increases from zero to V_{DC} and the voltage across C_{S1} drops to zero. The snubber capacitor allows for S_2 to have near ZCS turn-off.



Mode 1



Mode 2



Mode 3

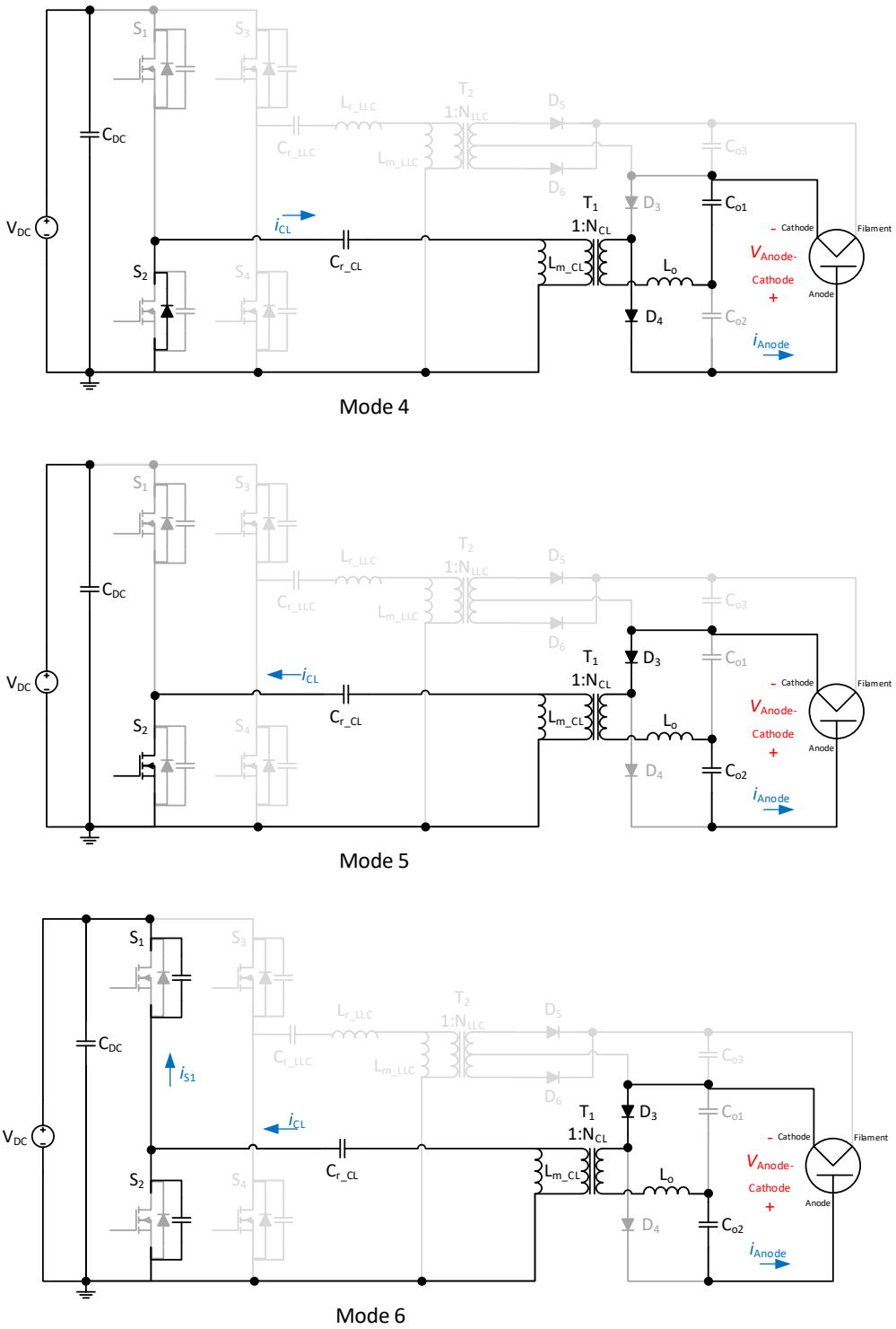


Figure 2-2: Proposed DC/DC converter's voltage step-up operating stages

The step-up portion of the circuit has three parts to obtain the required voltage gain. The resonant circuit, the transformer, and the voltage doubler. To obtain the gain of the resonant circuit, the following important equations must be established. Equation 2-1 is the equivalent resistance from the primary side of the transformer. Equation 2-2 is the quality factor of the resonant circuit. Equation 2-3 is the resonant angular frequency. Equation 2-4 is the relative operating frequency.

$$R_{eq\_CL} = \frac{2}{\pi^2 N_{CL}{}^2} R_{Anode-Cathode} \qquad \text{Equation 2-1}$$

$$Q_{CL} = \frac{R_{eq\_CL}}{\omega_{o\_CL} L_{m\_CL}} = \omega_{o\_CL} C_{r\_CL} R_{eq\_CL} \qquad \text{Equation 2-2}$$

$$\omega_{o\_CL} = \frac{1}{\sqrt{L_{m\_CL} C_{r\_CL}}} \qquad \text{Equation 2-3}$$

$$\omega_{r\_CL} = \frac{\omega_{s\_CL}}{\omega_{o\_CL}} \qquad \text{Equation 2-4}$$

Using the above variables and solving for the gain of the resonant circuit, as shown in the appendix, Equation 2-5 can be obtained. Additionally, the resonant circuits impedance phase can be obtained as Equation 2-6, which can be used to obtain the resonant current phase shift to ensure ZVS turn-on. Equation 2-5 and Equation 2-6 can be observed in Figure 2-3 and Figure 2-4 respectively. The max gain of the resonant circuit is approximately Q_{CL} , however, as the current must operate above resonance to achieve the required phase shift for ZVS turn-on, the actual max gain is slightly less. The overall gain of the step-up converter can be approximated by Equation 2-7 however, this only considers the fundamental harmonic of the resonant circuit and will not provide the exact voltage value.

$$|G_{CL}| = \frac{1}{\sqrt{(1-\frac{1}{\omega_{r\_CL}^2})^2 + (\frac{1}{\omega_{r\_CL} Q_{CL}})^2}}$$ Equation 2-5

$$\angle Z_{i\_CL} = \arctan(\omega_{r\_CL} Q_{CL}(1-\frac{1}{\omega_{r\_CL}^2})) - \arctan(\frac{\omega_{r\_CL}}{Q_{CL}})$$ Equation 2-6

$$\frac{V_{Anode-Cathode}}{V_{DC}} = \frac{4|G_{CL}|N_{CL}}{\pi}$$ Equation 2-7

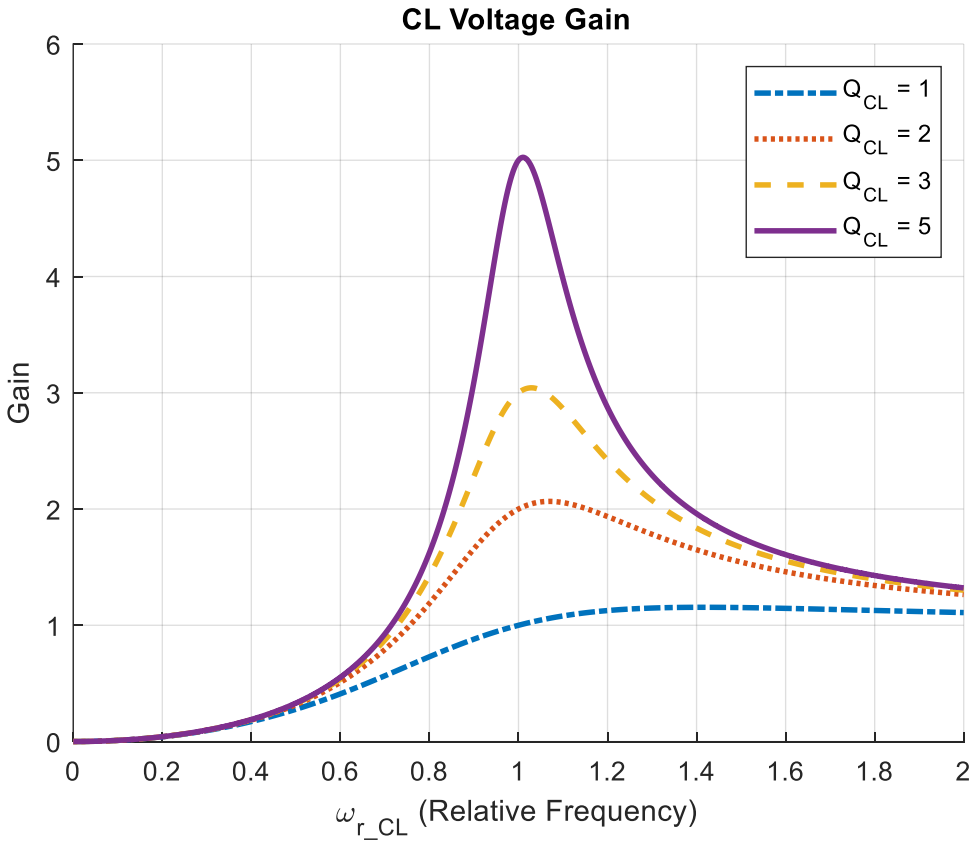


Figure 2-3: Voltage gain of a CL resonant circuit

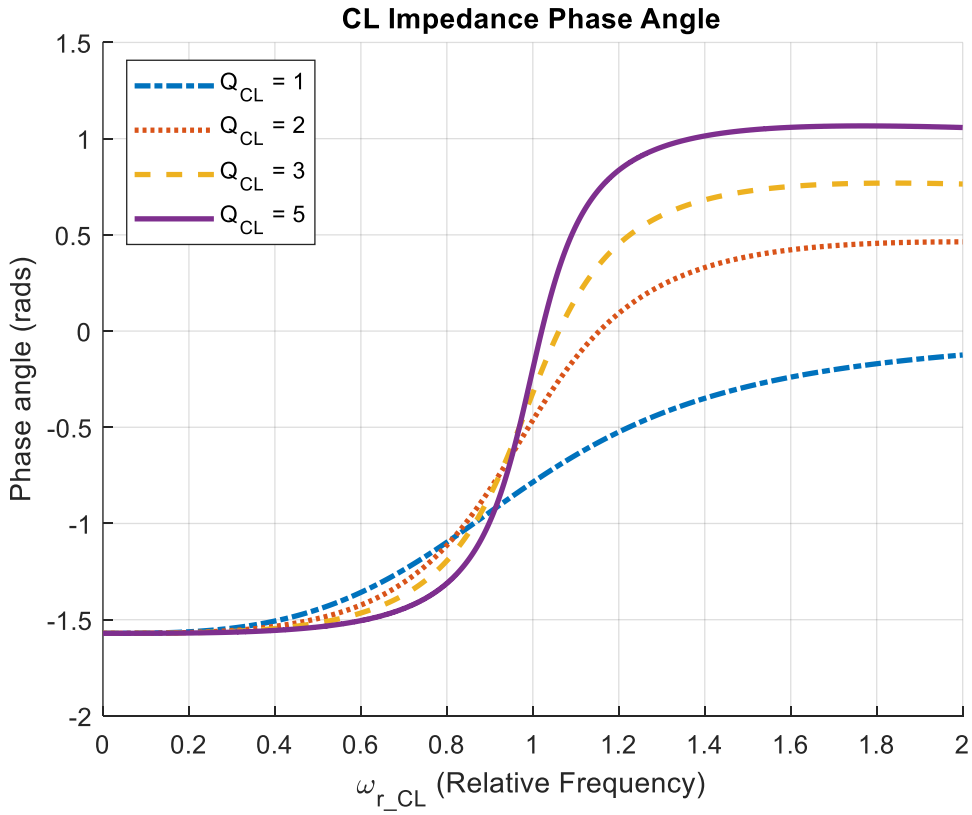


Figure 2-4: Input phase angle plot of a CL resonant circuit

Once the frequency is chosen for a design, the duty ratio will be used to provide control of the output voltage. The duty ratio of the primary switch should be designed for the max voltage gain and then decreased to lower the output voltage.

2.1.2. LLC Resonant Step-Down

The second resonant circuit provides power to the magnetron heater/filament component. In comparison to the anode to cathode voltage, the filament requires low voltage and higher current. To obtain this stepped-down voltage from V_{DC}, the resonant circuit provides a step-down with further step-down provided by the transformer. The operation of the LLC resonant circuit is similar to that of the CL resonant circuit, with the anti-parallel diodes and resonant capacitors allowing the switches, S_3 and S_4, to achieve ZVS turn-on and near ZCS turn-off. The operation of S_3 and S_4 will differ from the CL resonant, as they will be controlled by adjusting the frequency instead of the duty ratio. These two switches will also be able to operate asynchronously of S_1 and S_2.

The gain of the LLC resonant circuit will be used for its step-down function. To obtain step-down from this resonant configuration, the ratio 'k' given by Equation 2-8 must be large or the resonant converter will operate as a step-up for lower frequencies. Having a large L_m value, the circuit will be able to operate as a regular series LC resonant circuit whilst also considering the transformer's magnetizing inductance.

$$k = \frac{L_{m\_LLC}}{L_{r\_LLC}} \qquad \text{Equation 2-8}$$

To obtain the gain of the resonant converter the primary side equivalent resistance of the output must be obtained, which for the accompanying output stage is Equation 2-9. After then defining the fundamental angular frequency Equation 2-10 and the quality factor Equation 2-11, the gain of the resonant stage can be obtained as Equation 2-12. Equation 2-12 can be observed with a constant value of k = 10 in Figure 2-5, and a constant value of Q = 1 in Figure 2-6. For the

use in this converter, S_3 and S_4 will be adjusted by changing the operating frequency. As the step-down resonant converter is realized with the V_{DC} capacitor as a DC source.

$$R_{eq\_LLC} = \frac{8R_{Filament}}{\pi^2 N_{LLC}^{\ 2}} \qquad \text{Equation 2-9}$$

$$\omega_{o\_LLC} = \frac{1}{\sqrt{L_{r\_LLC}C_{r\_LLC}}} \qquad \text{Equation 2-10}$$

$$Q_{LLC} = \frac{\sqrt{L_{r\_LLC}}}{\sqrt{C_{r\_LLC}}R_{eq\_LLC}} = \frac{\omega_{o\_LLC}L_{r\_LLC}}{R_{eq\_LLC}} = \frac{1}{\omega_{o\_LLC}C_{r\_LLC}R_{eq\_LLC}} \qquad \text{Equation 2-11}$$

$$\left|G_{LLC}\right| = \frac{1}{\sqrt{(1+\frac{1}{k}-\frac{1}{\omega_{r\_LLC}^2 k})^2 + (Q_{LLC}(\omega_{r\_LLC}-\frac{1}{\omega_{r\_LLC}}))^2}} \qquad \text{Equation 2-12}$$

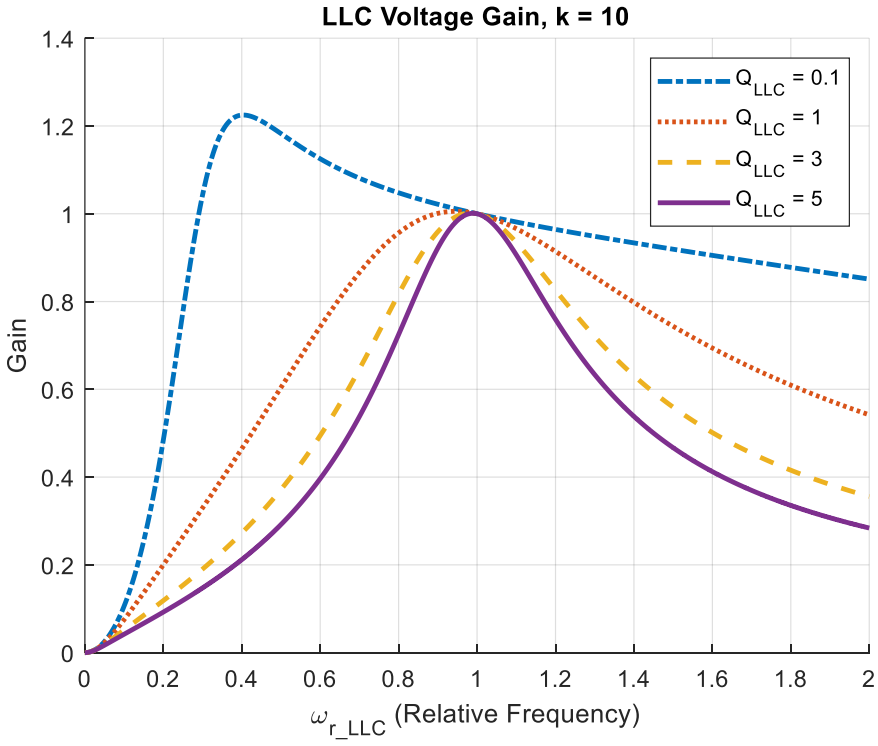


Figure 2-5: Voltage gain of LLC resonant circuit with varying Q_{LLC} and constant k = 10

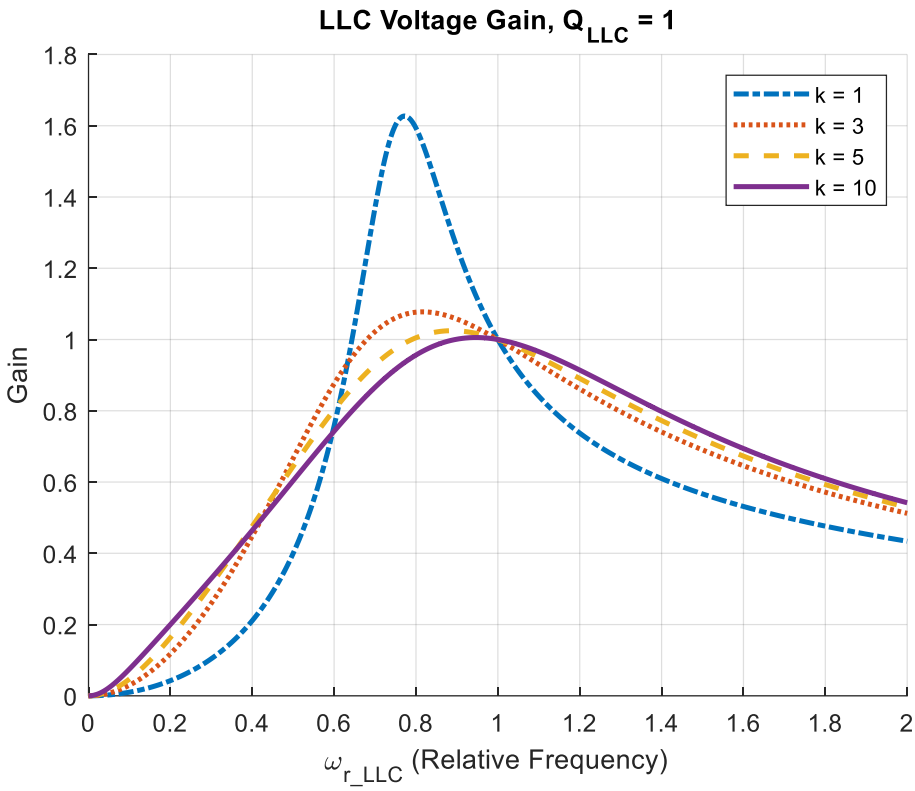


Figure 2-6: Voltage gain of LLC resonant circuit with varying k and constant $Q_{LLC} = 1$

2.2. AC Input Proposed Topology

The circuit proposed in this paper in Figure 2-7 builds upon the proposed converter from section 2.1 and [24] to provide the circuit with an AC input instead of a DC input. The first output is the cathode-anode of the magnetron, and the second output is the magnetron's filament voltage.

The circuit consists of two parts, the AC/DC PFC step-up converter, and the DC/DC step-down converter. The AC/DC step-up converter consists of L_{Boost}, D_1, D_2, $Switch_1$ abbreviated as S_1, $Switch_2$ abbreviated as S_2, C_{DC}. Additionally, the CL step-up resonant circuit and voltage doubler which consists of C_{r_CL}, L_{m_CL}, T_1, D_3, D_4, L_O, C_{O1}, C_{O2}, and the magnetron's anode to cathode connection, $V_{Anode-Cathode}$. The DC/DC step-down converter starts with the shared C_{DC} and uses $Switch_3$ abbreviated as S_3, $Switch_4$ abbreviated as S_4, C_{r_LLC}, L_{r_LLC}, L_{m_LLC}, T_2, D_5, D_6, C_{O3}, and the magnetrons filament connection, $V_{Filament}$. The AC input v_{ac} is expressed as Equation 2-13.

$$v_{ac} = \sqrt{2}V_{IN}\sin(\omega t) \qquad \text{Equation 2-13}$$

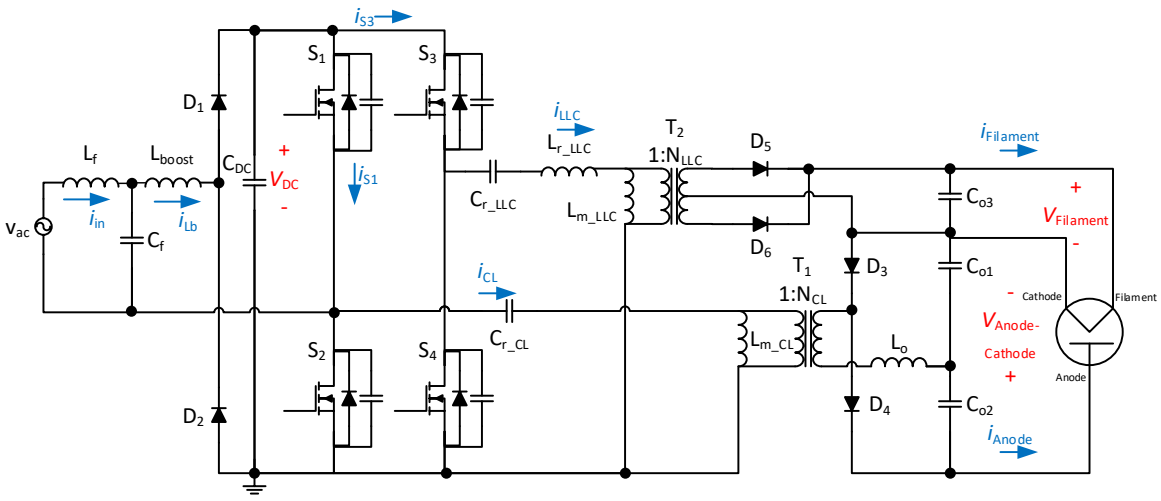


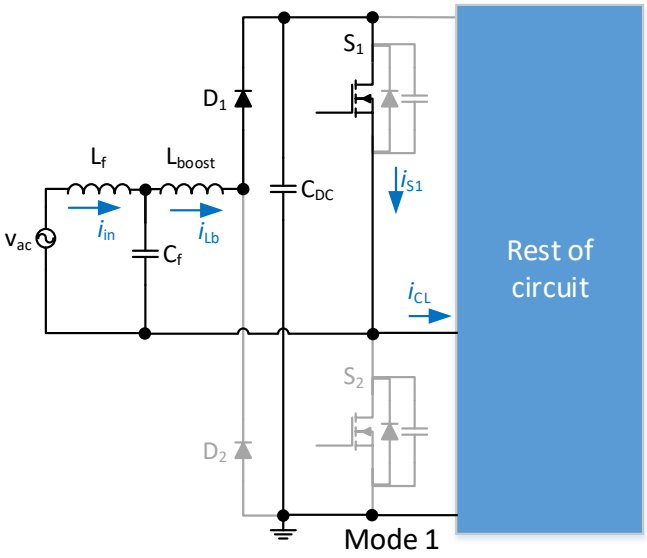
Figure 2-7: Proposed double-output AC/DC bridgeless converter

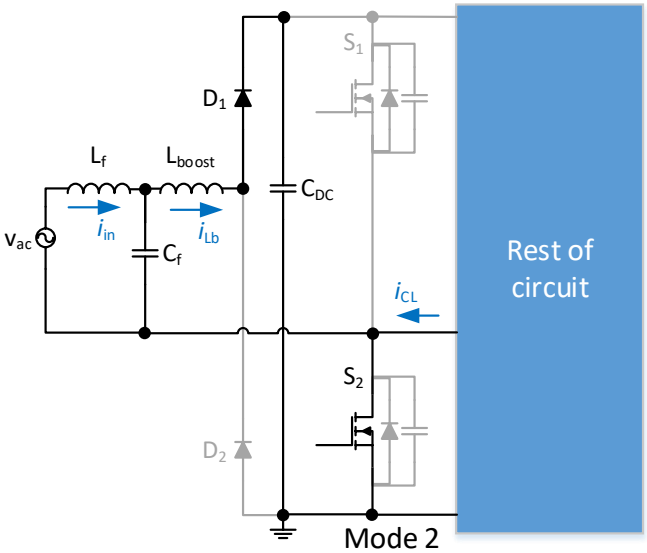
2.2.1. Bridgeless PFC Stage

The bridgeless PFC stage of the converter is achieved by operating the boost inductor L_B or L_{Boost} in discontinuous conduction mode (DCM). The bridgeless portion is realized by sharing the two switches of the step-up resonant converter in place of the second pair of diodes in a full bridge rectifier. This stage supplies the DC link capacitor, C_{DC}, with the charge required to act as a DC input for both the resonant circuits.

This stage can be broken down into three modes, ignoring the dead time delays of the switches, for when the input voltage is positive, and another three when it is negative. The positive input modes are described in detail below, with the corresponding operating stages shown in Figure 2-8. During the negative line stages, the input diodes will swap and the duty ratio of the two switches will also swap. Additionally, the boost inductor current for two switching periods during a positive line cycle are shown in Figure 2-9.

1. [$t = 0 < t < D T_S$] During mode 1 D_1 conducts, S_1 is turned on, S_2 is turned off, and the current through L_B increases. During this mode C_{DC} charges. The resonant tank sharing $S_1 \& S_2$ has a voltage potential of V_{DC}, with current flowing into the resonant tank.
2. [$D T_S < t < (D + \Delta) T_S$] During mode 2 D_1 conducts, S_1 is turned off, and S_2 is turned on. The current through L_B decreases to zero, which indicates the end of this mode. The shared resonant tank has a voltage potential of zero, with current flowing out of the resonant tank.
3. [$(D + \Delta) T_S < t < T_S$] During mode 3 the current through L_B is zero. During this mode, the link capacitor provides power to the two resonant circuits. The shared resonant tank has a voltage potential of zero, with current flowing out of the resonant tank.


S1
D1
Lf
Lboost
CDC
iS1
vac
iin
iLb
Cf
Rest of circuit
iCL
S2
D2
Mode 1


S1
D1
Lf
Lboost
CDC
vac
iin
iLb
Cf
Rest of circuit
iCL
S2
D2
Mode 2

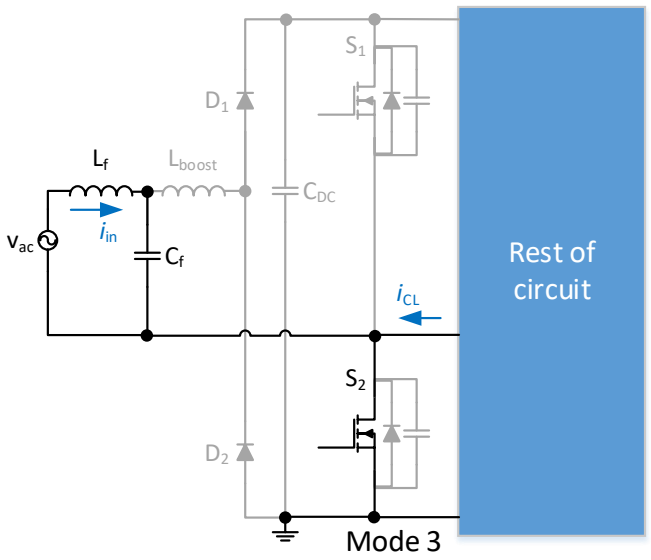


Figure 2-8: Proposed AC converter's bridgeless PFC operating stages during positive line cycle

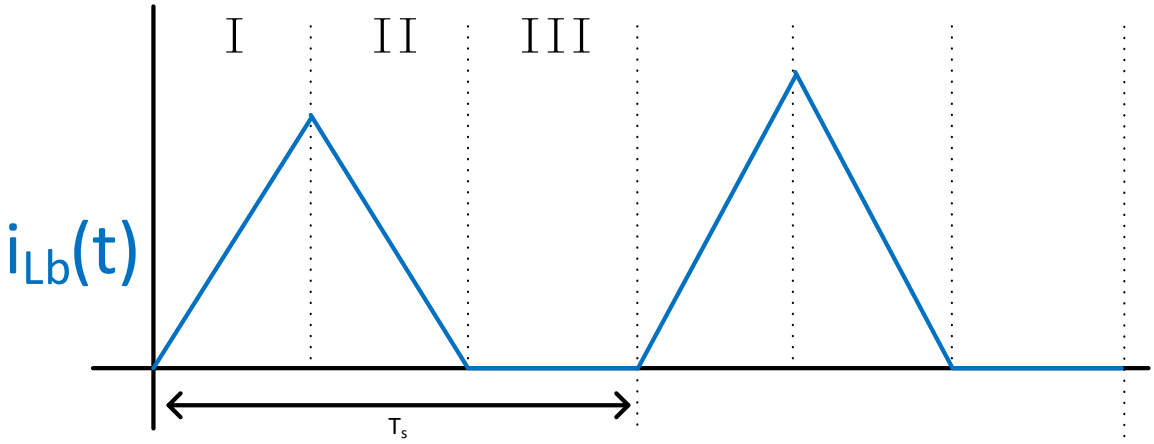


Figure 2-9: Boost inductor current over two switching periods during positive line cycle

2.2.2. Control Scheme

As the controls of the converter's main pair of switches can cause the DC-link voltage, V_{DC}, to increase or decrease, which in turn will impact both output voltages, the topology will heavily benefit from the use of a feedback loop controller to keep the high voltage output stable. To keep the control scheme simple to allow a focus on the converter itself, a simple closed loop will be implemented with the high voltage output to the control of $S_1 \& S_2$ duty ratio. This will be done using a PI controller to adjust the output voltage to the desired value. As this will impact the voltage of V_{DC}, it will also change the output of the low voltage output however, as the low voltage output applies a large step-down to this voltage, the DC voltage would need to change by a large amount for the low voltage to change by an impactful amount. As such, the low voltage output's switches, $S_3 \& S_4$ will be operated with a fixed frequency with adjustments made if required. The feedback loop used for the main switch pair that is used during the simulation stage can be observed in the appendix under the appendix portion of this paper, with a block diagram shown in Figure 2-10. In this block diagram, V_{Ref} is the reference voltage that will determine the desired output voltage, the e(t) term refers to the error between the reference and output, the PI block is the feedback control variables, c(t) is the value that will be compared to the sawtooth wave to output the duty ratio d(t). The input $v_{ac}(t)$ is then checked for its absolute value to set which switch is the main and which is the sync, along with a check for zero crossings to temporarily turn off the switches during the input voltage zero crossing. The converter then takes these two values and d(t) to produce the output which is fed back to the input with a sensor that will reduce the voltage from the output and isolate this output voltage so as to not damage the circuit.

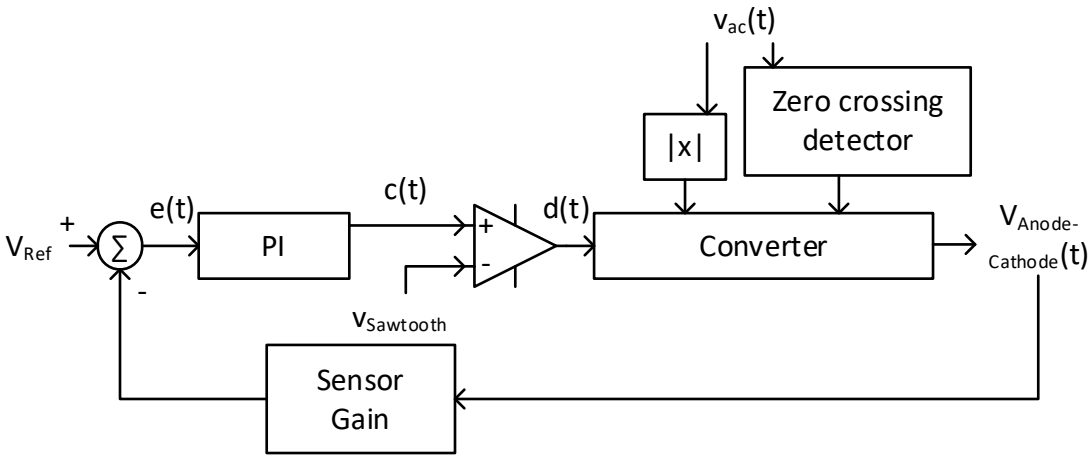


Figure 2-10: Control Feedback loop block diagram

Additionally, as the main pair of switches swap duty ratio when the line voltage crosses zero, the feedback loop will also need to swap the switch controls during this time. This will create issues of current spikes across the switches during the line voltage zero crossings. These spikes need to be considered as the large current spikes can damage the switches. One way that is discussed in literature to reduce these spikes is to turn off all the switches near the zero crossings, and then soft start the main switch, the switch controlled by the duty ratio, and then the sync switch, controlled by one minus the duty ratio [25][26].

2.3. Circuit Analysis

2.3.1. Boost Inductor

As mentioned previously, the bridgeless PFC stage is being utilized to draw from an AC source with a near unity power factor. This is achieved by operating the boost inductor, L_B, in DCM. To operate in DCM the boost inductor must comply with Equation 2-14, where V_{pk} is the peak value of the input voltage, D_{Min} is the lowest duty ratio that the $S_{1/2}$ pair will operate with, and $P_{O,Max}$ is the max output power of the entire circuit.

$$L_B < \frac{V_{pk}^2 D_{Min} T_S}{2P_{O,Max}} \qquad \text{Equation 2-14}$$

The boost inductor current i_{L_B} is important for understanding the stresses on the semiconductors and for selecting/designing an inductor for this application. Equation 2-15 gives the peak inductor current that will pass through the inductor. Observing that the peak current in Equation 2-15 increases as the inductor is made smaller, the inductor value should be chosen as close as possible to the max value determined in Equation 2-14 to minimize the current that will go through the switches, which will be discussed in chapter 2.3.3. The moving average of the boost inductor current is given by Equation 2-16.

$$i_{L_B,peak} = \frac{V_{pk} D T_S}{L_B} \qquad \text{Equation 2-15}$$

$$i_{L_B,avg} = \frac{2P_{in}}{V_{pk}} |\sin(\omega t)| \qquad \text{Equation 2-16}$$

2.3.2. Resonant Currents

The resonant current of both pairs will play a role in determining the current stresses for each of the switches. To determine the resonant currents, the resonant circuit impedances must first be determined. For the CL resonant circuit, the impedance is provided by Equation 2-17 and for LLC resonant circuit the impedance is provided by Equation 2-18 with the quality factor, relative operating frequency, equivalent resistance, and inductor ratio of the corresponding resonant circuit. Using these impedances, the corresponding peak resonant current can be obtained using Equation 2-19 and the RMS current from Equation 2-20.

$$|Z_{CL}| = R_{eq\_CL}\frac{\sqrt{(1-\omega_{r\_CL}{}^2)^2+(\frac{\omega_{r\_CL}}{Q_{CL}})^2}}{\sqrt{(\omega_{r\_CL}{}^2)^2+(Q_{CL}\omega_{r\_CL})^2}}$$ Equation 2-17

$$|Z_{LLC}| = R_{eq\_LLC}Q_{LLC}\frac{\sqrt{(k^2Q_{LLC}\omega_{r\_LLC}{}^2)^2+(k^2Q_{LLC}{}^2\omega_{r\_LLC}{}^3-k^2Q_{LLC}{}^2\omega_{r\_LLC}-\frac{1}{\omega_{r\_LLC}}+\omega_{r\_LLC}+k\omega_{r\_LLC})^2}}{k^2Q_{LLC}{}^2\omega_{r\_LLC}{}^2+1}$$

Equation 2-18

$$i_{Res,Pk} = \frac{v_{Pk}}{|Z_{Res}|}$$ Equation 2-19

$$i_{Res,RMS} = \frac{v_{RMS}}{|Z_{Res}|}$$ Equation 2-20

2.3.3. Switch Stresses

In the proposed topology there are 2 sets of switches, the two input PFC and step-up resonant converter switches $S_1 \& S_2$, and the two step-down resonant converter switches $S_3 \& S_4$.

For the selection of the switches, the peak voltage and current stresses will be analysed. The voltage stresses across $S_1 \& S_2$ are V_{DC} when the switch is off and roughly zero when the switch is on. The current through $S_1 \& S_2$ are given in Equation 2-21 and Equation 2-22 for when respective switches are on, with both equations remaining for both the negative and positive line cycles.

$$i_{S1} = i_{CL} + i_{Lb} \quad \text{Equation 2-21}$$

$$i_{S2} = -i_{Lb} - i_{CL} \quad \text{Equation 2-22}$$

Additionally, the peak current stresses during the positive input line cycle of $S_1 \& S_2$ are approximated by Equation 2-23 and Equation 2-24.

$$i_{S1\_Peak} = i_{CL,avg} + \Delta i_{CL} + i_{Lb,Peak} \quad \text{Equation 2-23}$$

$$i_{S2\_Peak} = i_{CL,avg} - \Delta i_{CL} - i_{Lb,Peak} \quad \text{Equation 2-24}$$

Similar to the previous set of switches, $S_3 \& S_4$ have a voltage stress of V_{DC} when the switch is off and roughly zero when the switch is on. For these two switches, the current stress is exclusively dictated by the resonant current which is expressed in Equation 2-25 for when the corresponding switch is on. This makes the peak stress of these two switches Equation 2-26.

$$i_{S3/S4} = i_{LLC} \quad \text{Equation 2-25}$$

$$i_{S3/S4,peak} = i_{LLC,avg} + \Delta i_{LLC} \quad \text{Equation 2-26}$$

2.3.4. Diode Stresses

In the proposed topology there are 3 sets of diodes, the two input diodes $D_1 \& D_2$, the two output switches for the high voltage anode-cathode side $D_3 \& D_4$, and the two output switches for the low voltage filament side $D_5 \& D_6$.

The two input diodes $D_1 \& D_2$ will have a voltage stress of V_{DC} when they are not conducting and zero when they are conducting. Additionally, the current across the diodes will be i_{Lb} when they are conducting and zero when they are off. This results in the peak current stress being given by Equation 2-27.

$$i_{D_1/D_2} = i_{L_B,peak} \qquad \text{Equation 2-27}$$

The two output diodes for the high voltage output, $D_3 \& D_4$, have voltage stresses of $V_{Anode-Cathode}$ when they are not conducting and zero when they are conducting. The current stresses of diodes are given by the output inductor which is expressed in Equation 2-28.

$$i_{D_3/D_4,peak} = i_{L_O,peak} \qquad \text{Equation 2-28}$$

The two output diodes for the low voltage output, $D_5 \& D_6$, have a voltage stress given by Equation 2-29 when they are not conducting and zero when they are conducting. The current stresses of the diodes are given by Equation 2-30.

$$V_{D_5/D_6} = V_{secondary\_LLC} - V_{Filament} \qquad \text{Equation 2-29}$$

$$i_{D_5/D_6,peak} = \frac{\pi}{2} I_{Filament} \qquad \text{Equation 2-30}$$

2.3.5. Design Procedure

The design procedure that was used to obtain the values of passive components and the operating conditions is detailed in Figure 2-11. The steps shown are explained in more detail below.

1. Select a value for the switching frequency of S_3 & S_4 such that the gain is as required, and the phase is positive to allow for soft switching. On the first iteration, this frequency should be selected based on being high enough to reduce passive component sizes. For our implementation, a frequency of 120kHz was selected as the first iteration.
2. Determine the Boost inductor value using Equation 2-14.
3. Determine the DC-link value from the previous simulation. On the first iteration, this value can be assumed to be about 350V if using a 120Vac input.
4. Determine the quality factor, Q_{CL}, and transformer 1 turns ratio, N_{T1}, that will allow for the desired output voltage to be achieved with the DC-link voltage determined in step 3. The output should consider slightly higher than required, as the DC-link voltage will drop slightly after adding the step-down stage. It should be noted that these two values are not independent of each other, and as such should be calculated together.
5. After running the simulation, the boost inductor should be confirmed as operating in DCM, the anode-cathode output voltage should be equal to or greater than the max output voltage. The switches should also be checked to ensure soft switching.
6. After completing the step-up stage, the step-down resonant stage will need to be designed. With the DC link voltage from before, determine the quality factor, Q_{LLC}, inductance ratio,

k, turns ratio, N_{T2}, and switching frequency, F_{s_LLC}, that will be used to obtain the filament voltage.

7. Check that the filament voltage is as desired, the low voltage switches have soft switching, the cathode-anode voltage has not dropped below the max required voltage, and that the boost inductor remains in DCM. Should the cathode-anode voltage be too low, then go back to step 3 with the new known DC-link voltage.

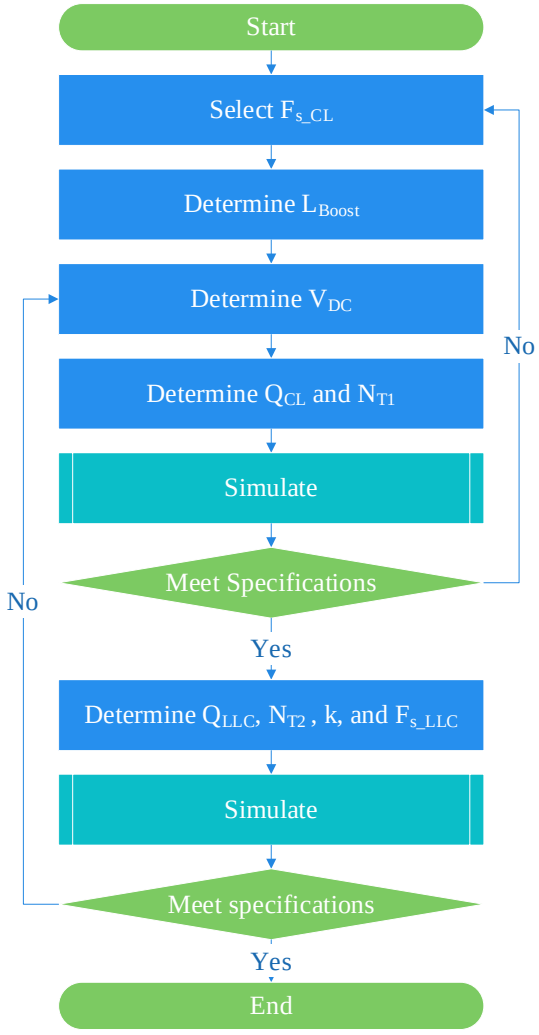


Figure 2-11: Design parameters flowchart

2.4. Summary

In this chapter, the DC-DC proposed topology is discussed for providing a double DC output with a single DC input. The second proposed topology is then discussed which builds upon the first by combining a bridgeless PFC stage with one of the switch pairs. The combined topology has its operating stages and formulas discussed along with the control scheme, component stresses, and design procedure.

3. Implementation

3.1. Design Values

To confirm the theory of the above topology the circuit was recreated in software and then further validated through hardware testing. To realize these two sets of testing, actual values were selected for all components to provide the required outputs of a magnetron. The expected values of this magnetron are provided in Table 2. To obtain the outputs required by this magnetron, the component values provided in Table 3 were selected. With the specified values from these two tables, some notable calculated values are provided in Table 4. These values were used during the simulation portion, with values being prone to small modifications during hardware testing.

Table 2: Magnetron Specifications

Magnetron Specifications	
Filament Voltage (Volts)	5 V
Filament Current (Amps)	25 A
Average Anode current (mA)	350 mA
Peak Anode Voltage (kV)	4.7 kV
Output Power (W)	1850 W

Table 3: Component Values

Component	Value
Input Voltage	120 Vac
Line Frequency	60 Hz
Line Inductor	1.5mH
Line Capacitor	2.2uF
Boost Inductor	15uH
DC-Link Capacitor	680uF
Snubber Capacitors	500pF
CL Capacitor	100nF
CL Magnetizing Inductance	29.2uH
CL Turns Ratio	1:4
CL Output Inductor	3mH
CL Doublers Capacitors	3uF
CL Switching Frequency	106kHz
CL Duty Ratio	Varies (Control Parameter)
LLC Capacitor	5nF
LLC Series Inductor	515.6uH
LLC Magnetizing Inductance	1mH
LLC Turns ratio	18:1:1
LLC Output Capacitor	100uF
LLC Switching Frequency	Varies (Control Parameter)
LLC Duty Ratio	0.5

Table 4: Calculated Parameters

Component	Value
CL Equivalent Resistance	189 Ohm
LLC Equivalent Resistance	52.5 Ohm
CL Quality Factor (Q)	11.11
LLC Quality Factor (Q)	6.11
LLC Inductance Ratio (k)	1.94

3.2. Simulations - Powersim (PSIM)

The circuit was first designed, tested, and validated through the PSIM software, with the layout shown in Figure A-1. The approach to testing the circuit that will be used is to start with a 120Vac input and have the max rated output power tested whilst ensuring the boost inductor remained in DCM and validating the power factor and efficiency of the overall simulation. Then remaining at a 120Vac input, a lower output voltage of the anode-cathode connection will be tested to ensure the output can be controlled correctly. Along with these tests of the anode-cathode connection, a test of the filament low voltage will be validated to confirm the output voltage can be changed by adjusting the LLC resonant circuits switching frequency and to ensure ZVS is occurring for the low voltage output. Additionally, the feedback loop at that used in the simulations for $S_1 \& S_2$, with the layout shown in Figure A-2, has a gain of 11.11 and a time constant of 0.015, with the triangular wave having a peak of 10V.

3.2.1. 120 Vac Max Voltage Output Test

For testing with 120Vac input and max voltage output in PSIM, a feedback loop was implemented for the high voltage output which regulated the step-up switch pair's duty ratio with a fixed frequency of 106kHz, and the duty ratio fluctuating about .45 ± 0.05 to keep the output at 4.7kV.

First, the input boost inductor current was checked to ensure that the inductor was operating in DCM to allow for power factor correction in the input current. This is validated in Figure 3-1 which shows the full waveform from the 60Hz input perspective and the zoomed in waveforms of the positive input phase and the negative input phase. As can be observed in the positive cycle current, the current drops to zero for a very short time, and in the negative waveform the current drops to zero for a very short moment, which is more of a boundary conduction mode (BCM) operation. This BCM operation is what is currently setting the max power of the design, as any further increase will result in continuous conduction mode (CCM) operation which will distort the input current. The input current that is obtained as a result of the DCM operated boost inductor can be observed in Figure 3-2, which shows the input current along with the input voltage to show the two waveforms are correctly in phase. Whilst the current looks as though it is starting to distort, by observing the power factor in Figure 3-3 the power factor can be observed as approximately 0.98 which is close to unity PF. Additionally, the input current's total harmonic distortion (THD) can be observed in Figure 3-4, which shows that the THD is approximately 21% with the majority of the distortion at 180Hz or three times the fundamental frequency.

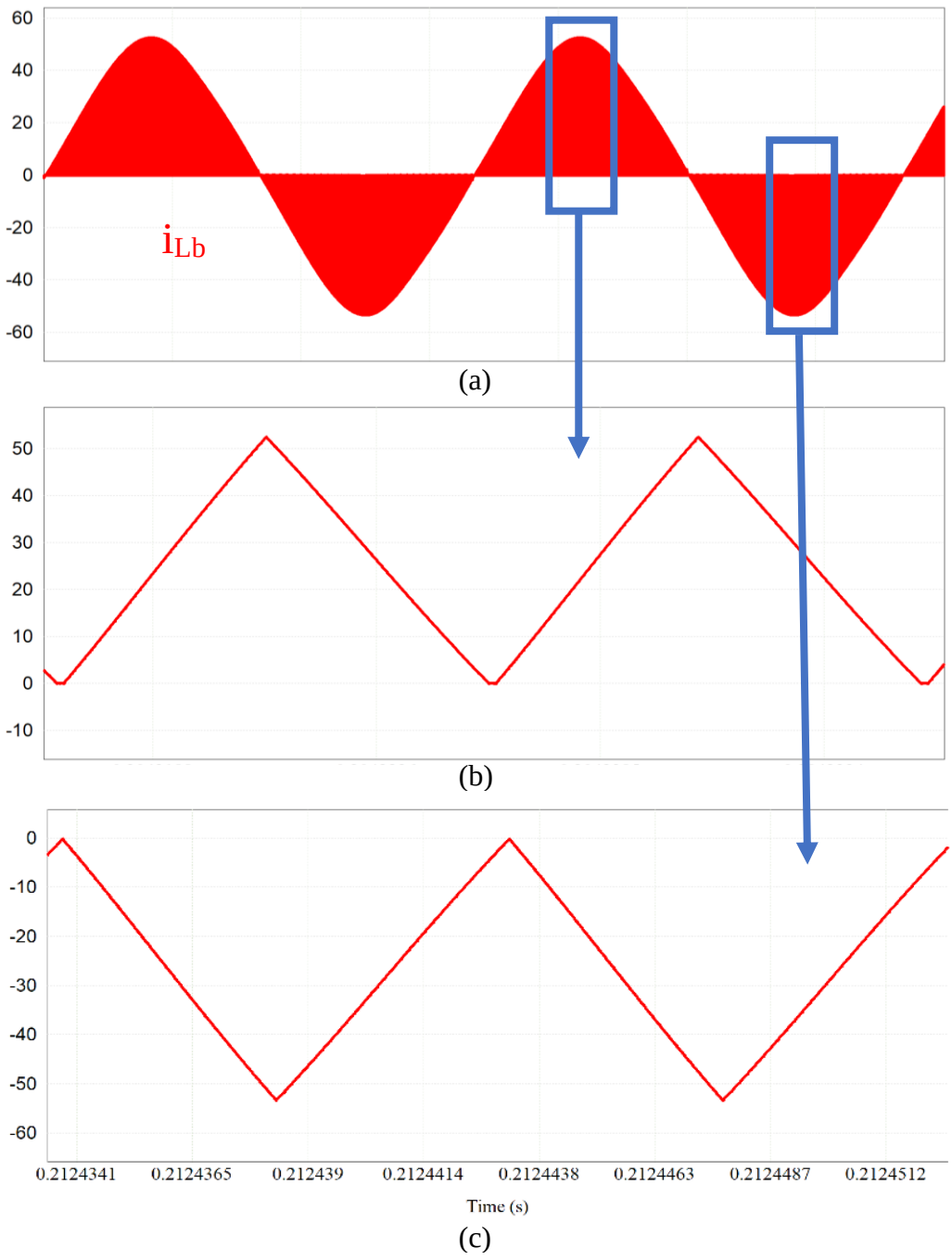


Figure 3-1: Boost inductor current at peak output. (a) boost inductor current from view of two 60Hz cycles, (b) zoomed in view of peak positive current cycles, (c) zoomed in view of peak negative current cycles

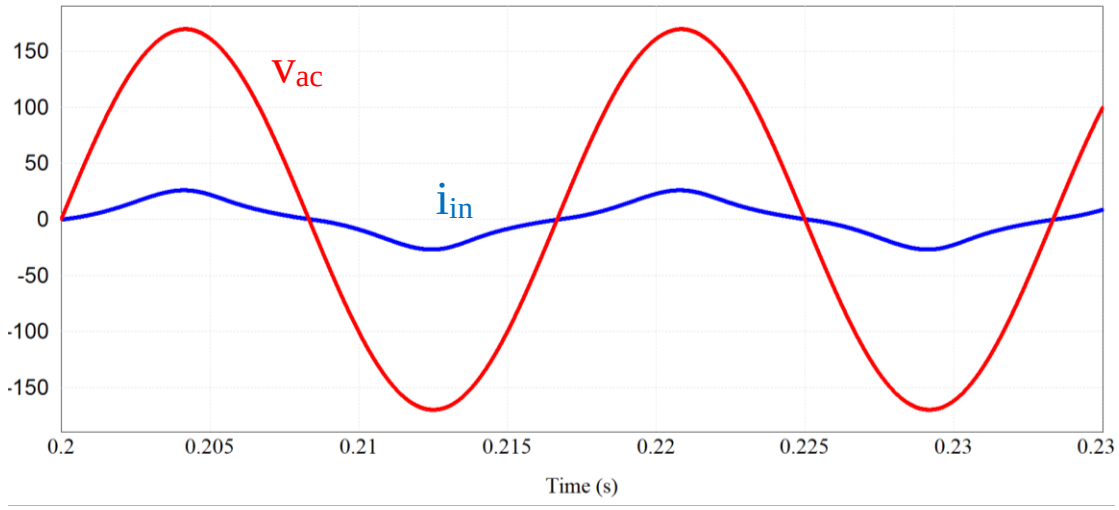


Figure 3-2: Input voltage and current with peak output.

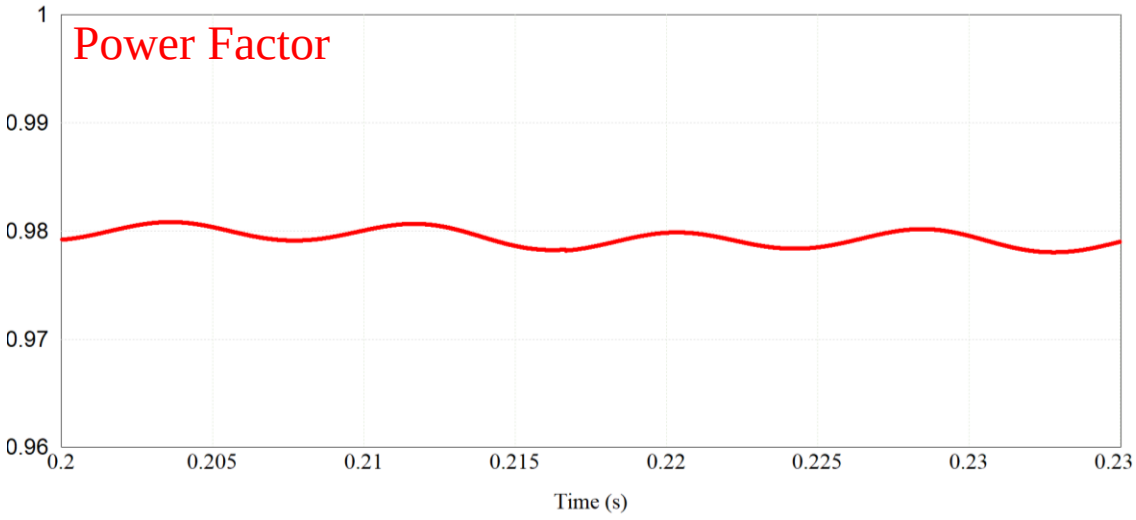


Figure 3-3: Power factor at peak output.

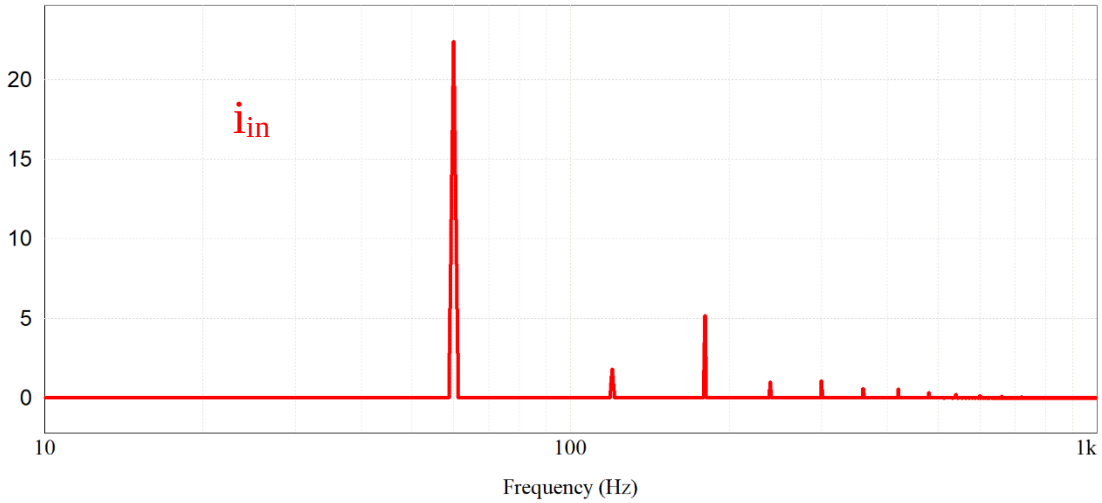


Figure 3-4: Input current's total harmonic distortion at peak output.

Confirming the switches operate with soft switching is the next step in validating the circuit's operation. The waveforms of switch 1, which is the high side switch of the PFC and the step-up stages of the topology, can be observed in Figure 3-5. During both the negative and positive periods of the input voltage, the current can be observed to be as negative during the switch turn-on confirming that switch 1 has ZVS turn-on. During turn-off, the switch is able to obtain near ZCS with a dead time of 0.02 of the switching frequency which can be observed in Figure 3-6. However, due to the limitations of PSIM this dead time may need to be adjusted further during the hardware testing.

Whilst switch 1 and 2 are running, the switches 3 and 4 are also running. Switches 3 and 4 are running at 108kHz which can adjust the output, a fixed duty ratio of 50%, and a dead time of 2%. Figure 3-7 shows switch 3 current in red and voltage in blue. As the current is negative while the switch turns on, the starting current flows through the anti-parallel diode and results in ZVS turn-on soft switching. Additionally, the observable spikes in the current indicate when the switch is turned on, further verifying that switch 3 experiences ZVS turn-on.

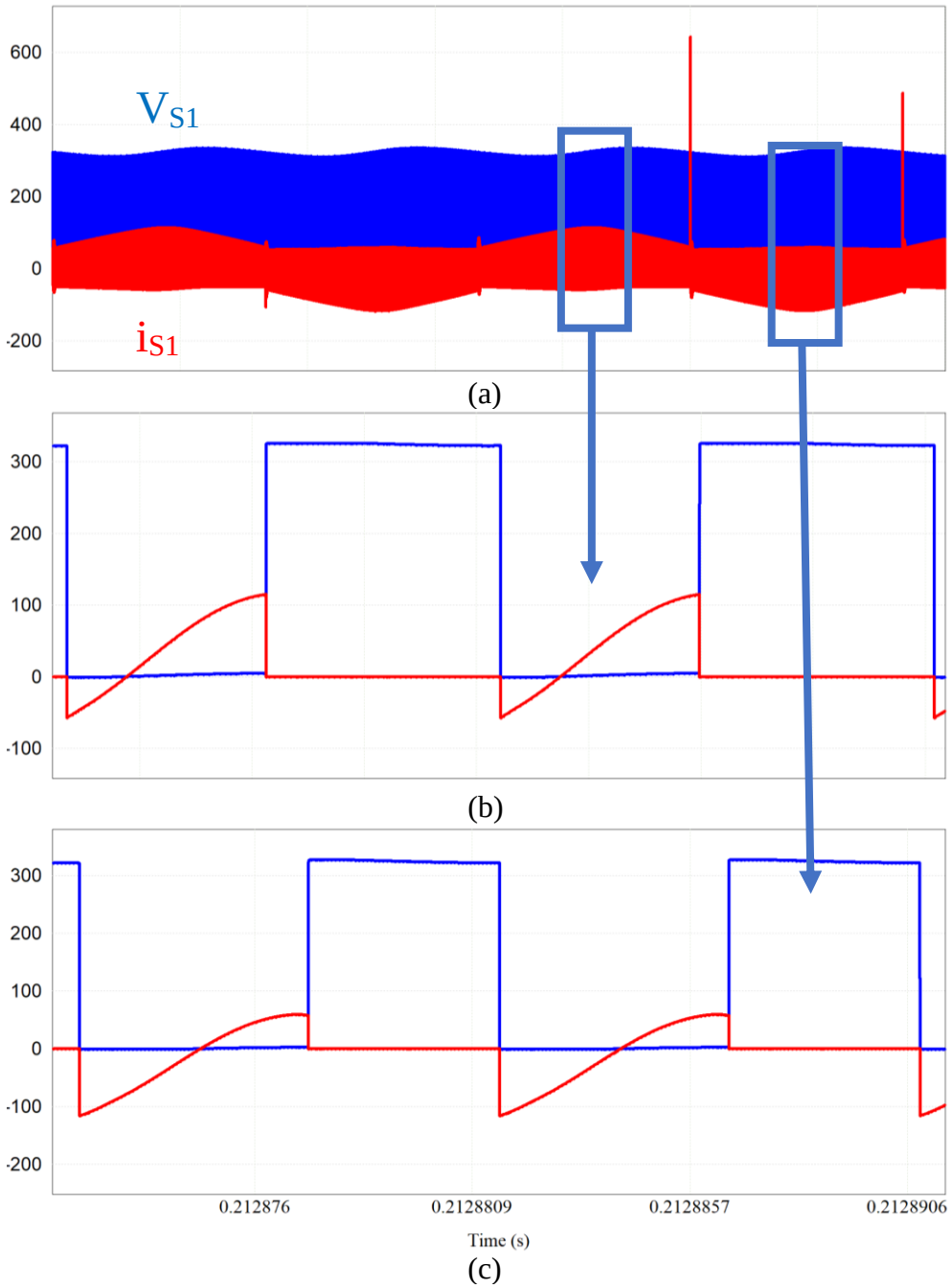


Figure 3-5: Switch 1 waveforms at peak output. (a) view of two 60Hz cycles, (b) zoomed in view of peak positive current cycles, (c) zoomed in view of peak negative current cycles

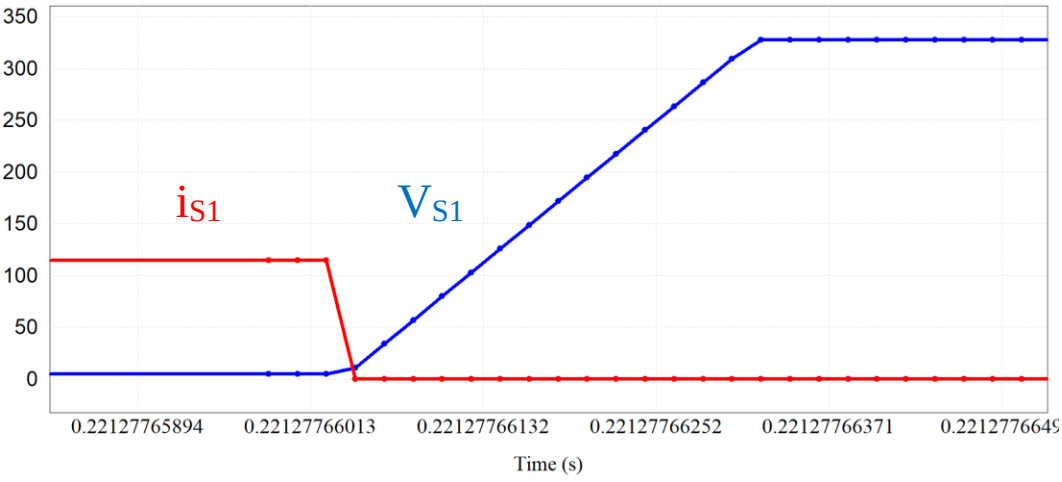


Figure 3-6: Switch 1 near ZCS turn-off at peak output.

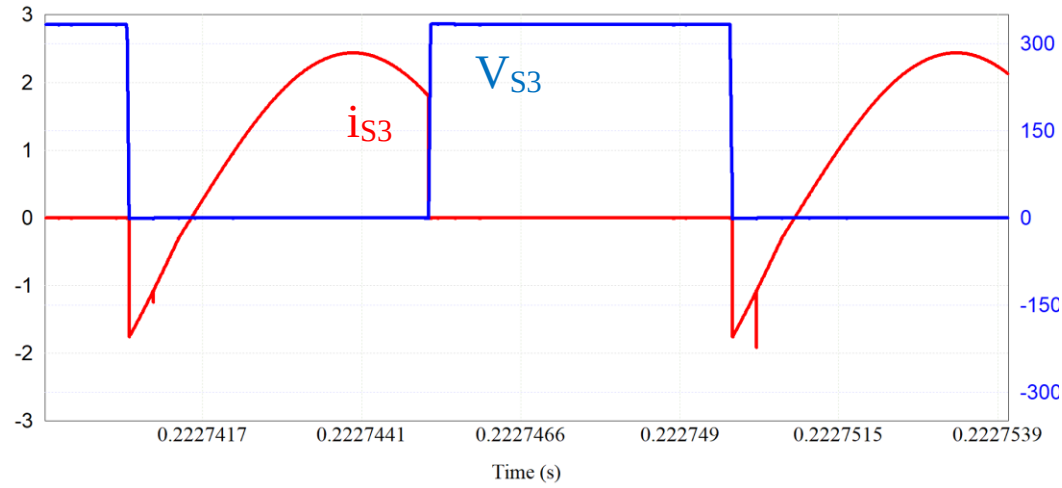


Figure 3-7: Switch 3 voltage and current waveforms at peak output.

Next, the outputs are verified in Figure 3-8 with the DC link capacitor voltage shown in blue and the cathode-anode voltage shown in red. The anode-cathode voltage has an average voltage of 4.7kV, which is the expected peak value. The DC link capacitor has an average value of 322V while running at these conditions. Figure 3-9 shows the DC link in blue and the filament voltage in red which has an average value of 5.41V. Using these waveforms and the input

waveforms obtained in Figure 3-2, the overall efficiency of the design is approximately 90% at peak output.

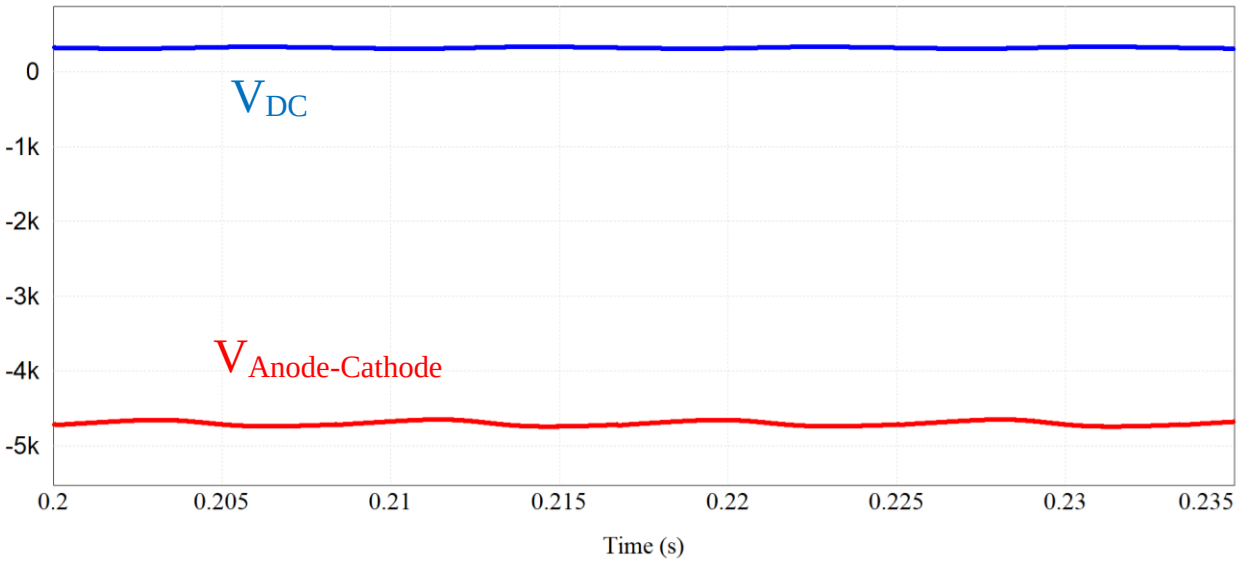


Figure 3-8: VDC and cathode-anode voltage at peak output.

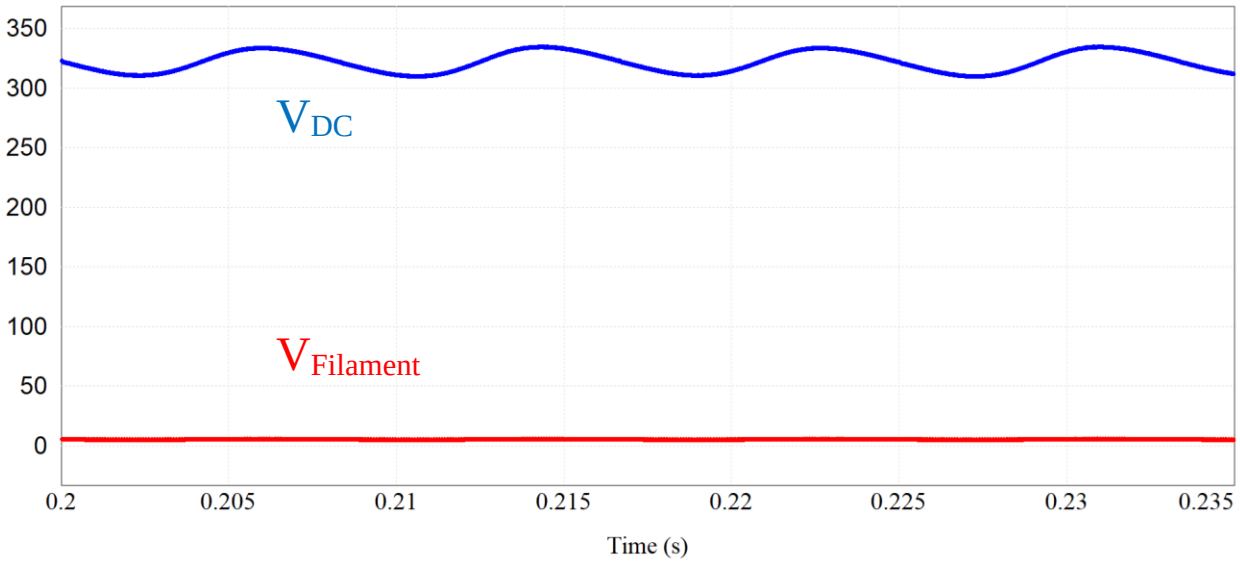


Figure 3-9: VDC and Filament voltage at peak output.

3.2.2. 120 Vac Nominal Output Test

For testing at the nominal output, an anode-cathode voltage of -4kV was simulated along with maintaining the switching frequency of the step-down stage to observe how changing the high voltage output impacts the low voltage output. For obtaining the output of -4kV, the control loop kept the duty ratio fluctuating around 0.37 ± 0.03.

Figure 3-10 shows the boost inductor current with the nominal high voltage test condition. In comparison to the current at the peak output conditions, the current during this lower output voltage operation can be observed to be reduced with the peak current dropping from 52A to 42A, or an RMS change of 19.1A RMS to 14.7A RMS over a full 60Hz period.

Figure 3-11 shows the input voltage (red) and input current (blue). Here we observe that with a fixed 120Vrms input voltage, dropping the output voltage from its peak to nominal causes the current to drop from $15.4A_{rms}$ to $11.2A_{rms}$. Further, by observing Figure 3-12 the power factor is approximately 0.983 which is a small improvement over the peak output conditions. Figure 3-13 shows the input currents FFT, which in comparison to the peak output conditions in Figure 3-4, the harmonic at 120Hz is almost entirely gone and the harmonics above 180Hz are significantly reduced bringing the THD down to about 19% from the previous 21%. With these observations of the input current, the topology is confirmed to be able to achieve a high PF for both its peak output and nominal output. This aligns with the theory, which tells us that the input will have a high PF if the boost inductor remains in DCM.

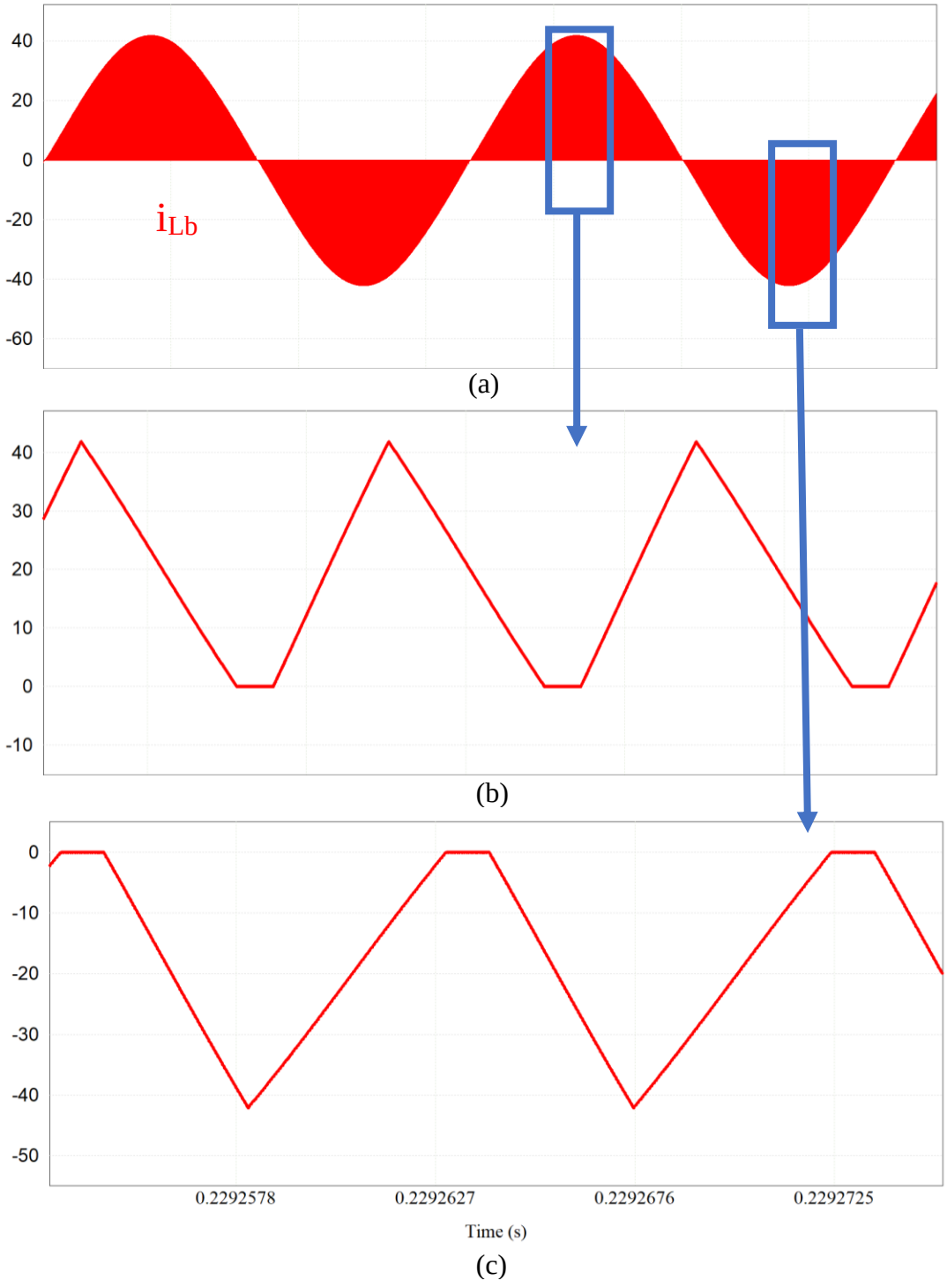


Figure 3-10: Boost inductor current at nominal output voltage (a) boost inductor current from view of two 60Hz cycles, (b) zoomed in view of peak positive current cycles, (c) zoomed in view of peak negative current cycles.

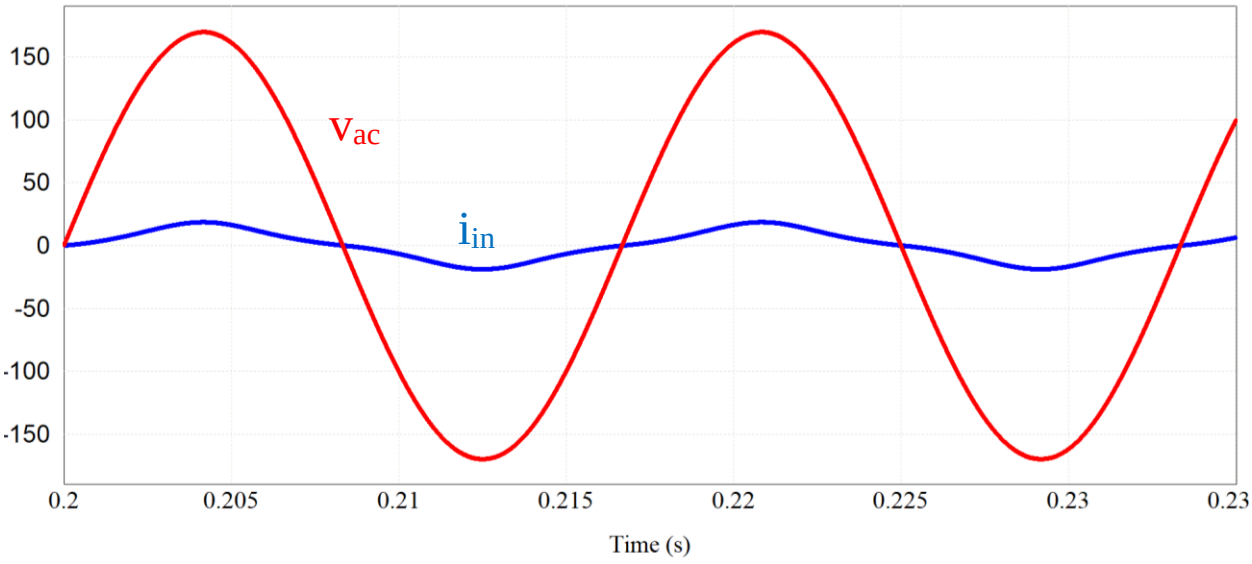


Figure 3-11:Input voltage and current with nominal output voltage.

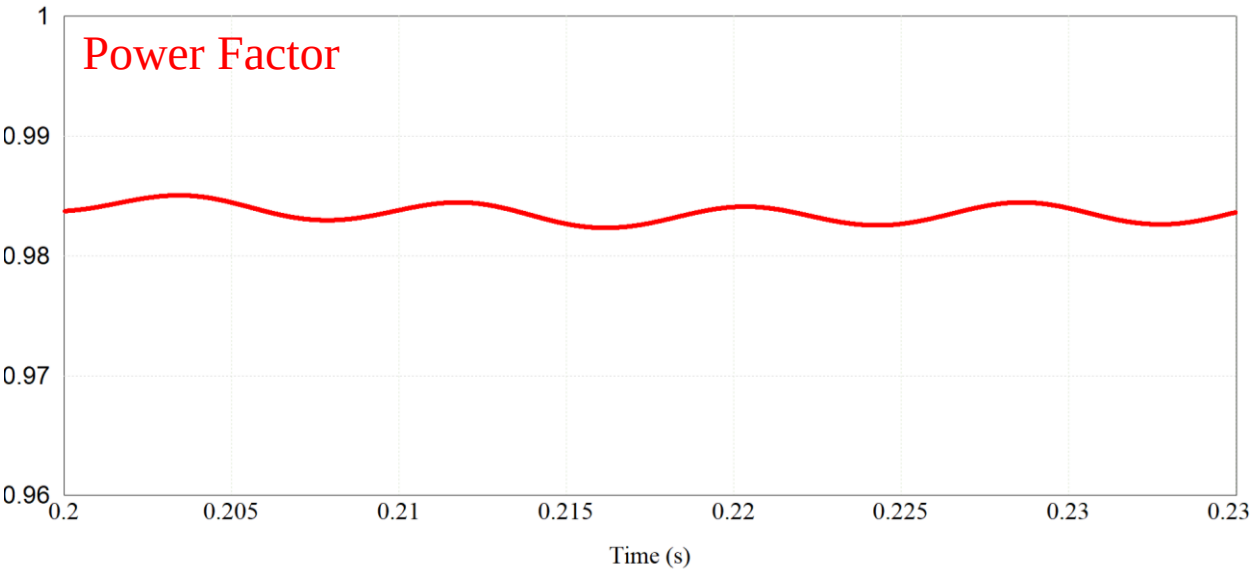


Figure 3-12: Power Factor with nominal output voltage.

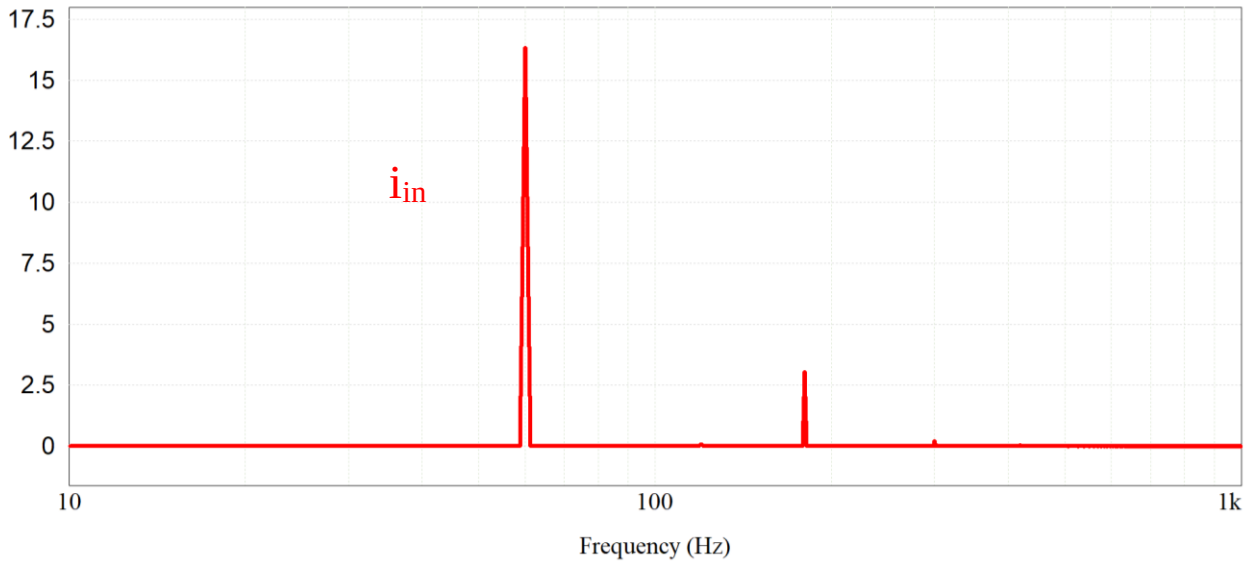


Figure 3-13:Input current's total harmonic distortion at nominal output.

Figure 3-14 shows the switch 1 current in red and voltage in blue with (a) showing the input 60Hz cycles, (b) showing two switching periods during the positive input peak, and (c) showing two switching periods during the negative input peak. Observing (b) and (c) shows that the current is negative when the switches turn on, indicating that the switches experience ZVS turn-on. Additionally, during the peak current of the positive input shown in (b) the current is measured as 95A. Whilst this high current only occurs for a short amount of time, it is an indicator that the switches used should have a low R_{DS_On} to prevent the switches from overheating during their respective peak current periods. Figure 3-15 shows the current for Switch 1 along with the combined current of the resonant step-up resonant circuit and the input boost inductor current.

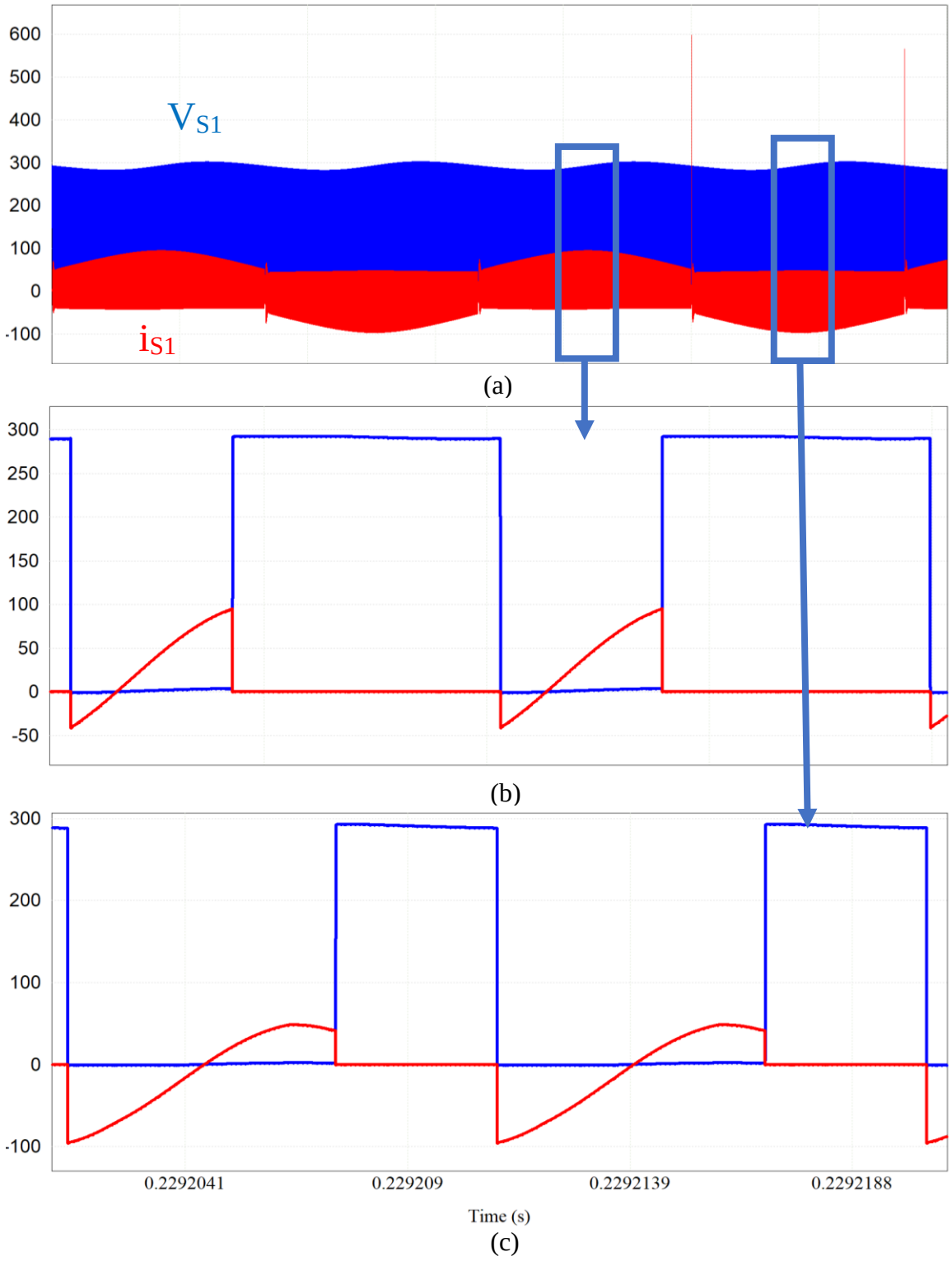


Figure 3-14: Switch 1 waveforms at nominal output. (a) view of two 60Hz cycles, (b) zoomed in view of peak positive current cycles, (c) zoomed in view of peak negative current cycles

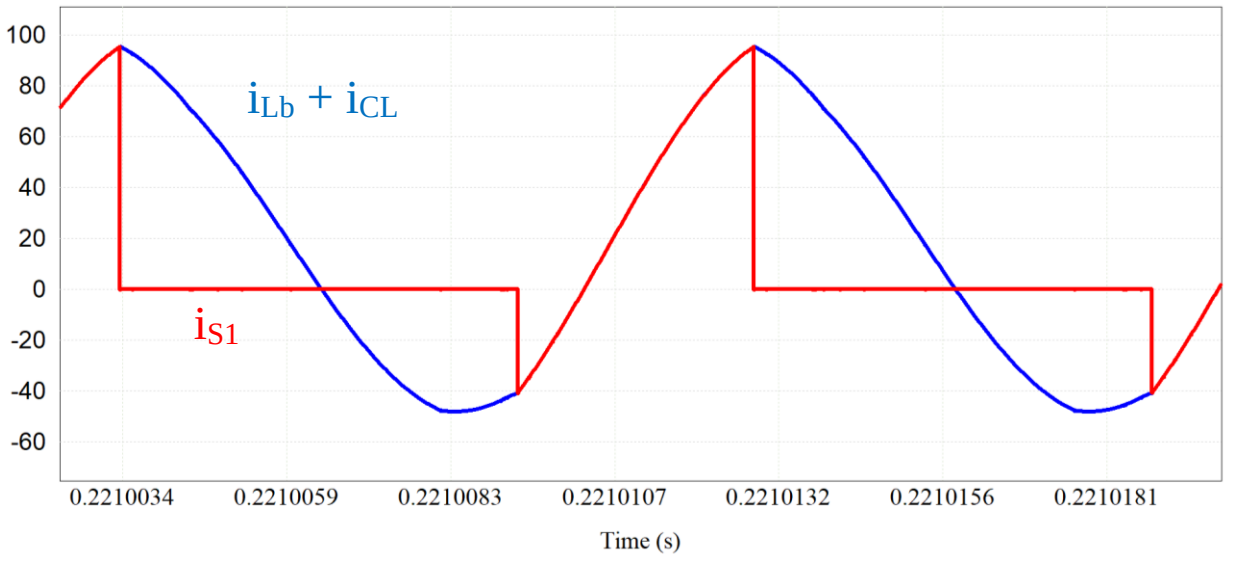


Figure 3-15: Switch 1 current and source of current stress

Figure 3-16 shows the switch 3 current in red and voltage in blue. From this waveform the switch current can be observed to be similar to the max output, confirming that changing the step-up control duty ratio only impacts the voltage provided to the step-down resonant circuit.

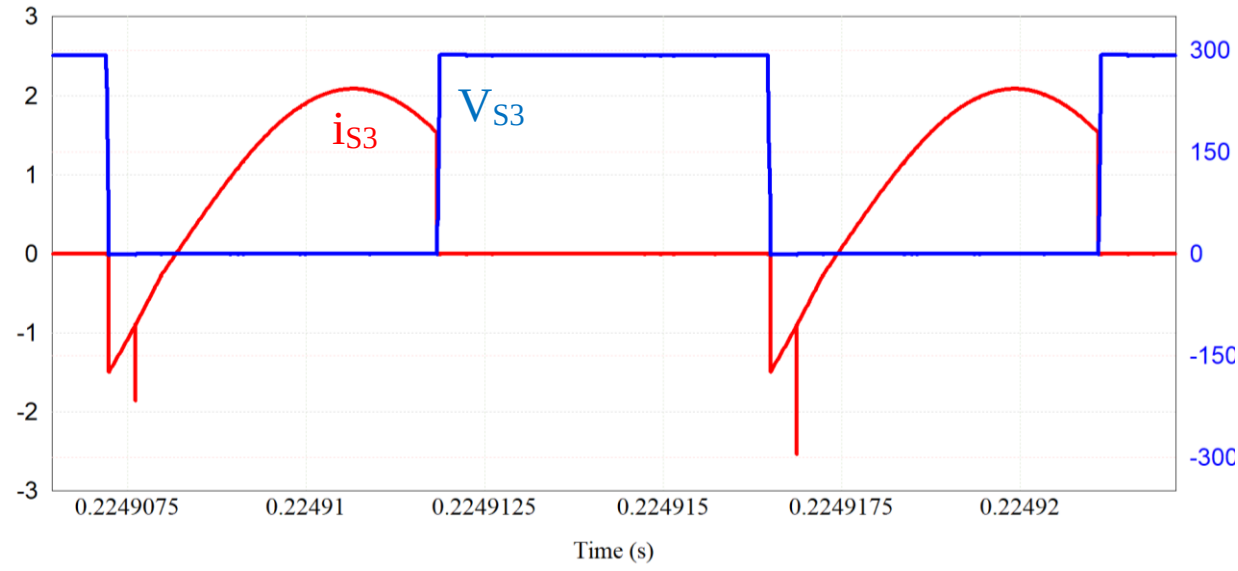


Figure 3-16: Switch 3 voltage and current during nominal output without adjusting control

Figure 3-17 shows the output high voltage anode-cathode voltage in red and the DC link voltage in blue. The DC voltage here is 292V and the output voltage is the 4kV nominal voltage that was selected. In comparison to the peak output conditions, the DC link voltage dropped from 322V to 292V from only adjusting the duty ratio of the step-up switch pair of the converter.

Figure 3-18 shows the filament voltage in red and the same DC link voltage in blue. The filament voltage is 4.81V. In comparison to the peak output conditions the filament voltage dropped from 5.41V to 4.81V, which is a result of the decreased DC link voltage. To adjust the voltage of the filament the switching frequency of switch 3 and switch 4 can be decreased. This was confirmed by running another simulation in which the switching frequency of the switch 3 and 4 is reduced from 108kHz to 106kHz, which decreases the DC link voltage from 292V to 290V and increases the filament voltage from 4.81V to 5.33V. The overall efficiency of the converter at the nominal output remains at approximately 90%.

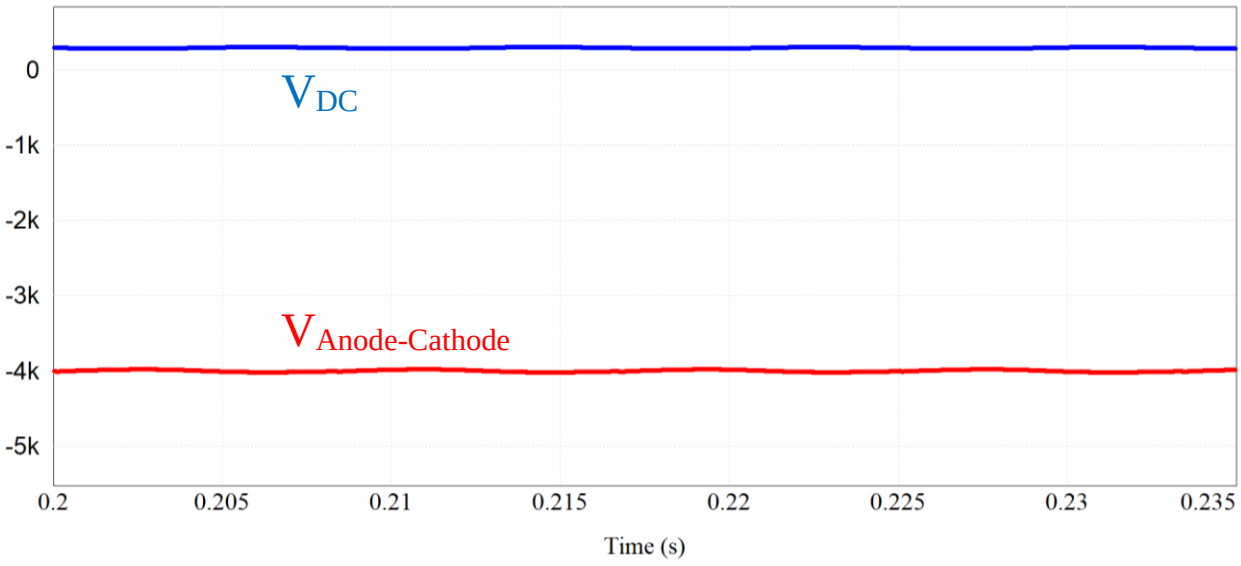


Figure 3-17: VDC and cathode-anode voltage at nominal output

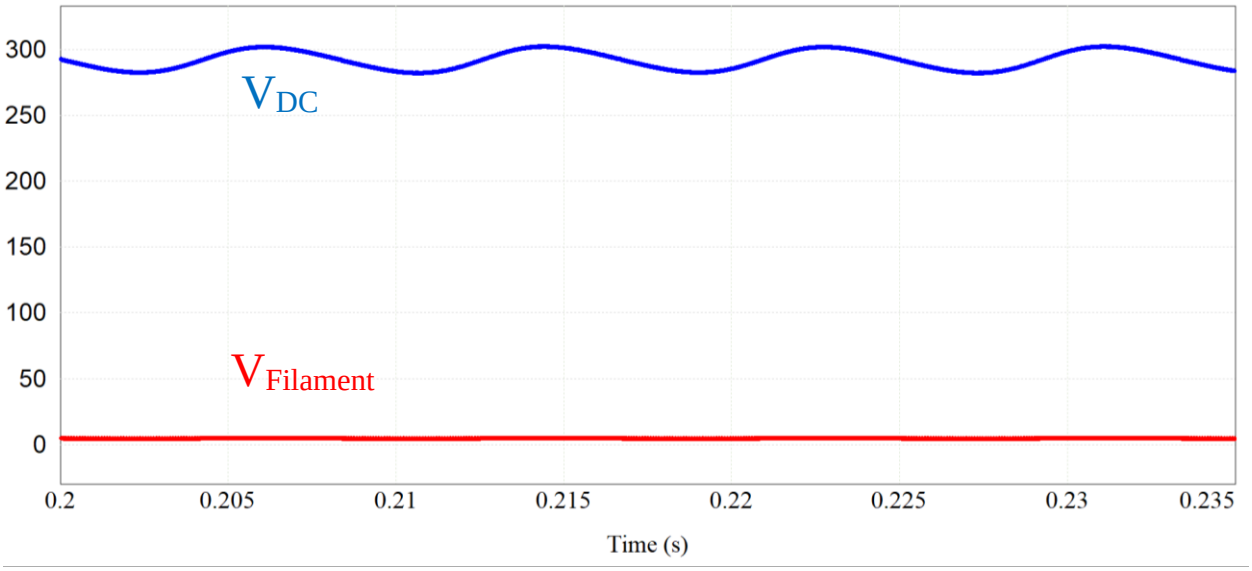


Figure 3-18: VDC and Filament voltage at nominal output.

3.3. Hardware Testing

To expand the proof of concept beyond just simulations for the proposed circuit a printed circuit board (PCB) was created using Altium designer using footprints of selected components based on the previous simulations. To ensure the PCB could be evaluated with different frequencies and duty ratios, a digital signal processor (DSP) board was used with connection pads included on the PCB design. Additionally, extra spots were placed on the PCB for wires to be connected for current probes and an extra pad to test with DC input. The Altium PCB design is shown in the appendix.

3.3.1. Hardware Specifications

For performing the hardware tests, specific semiconductors had to be selected to meet the current and stress requirements provided in Table 5, with additional margins considered for voltage overshoot and noise. The specific semiconductors used during the testing are provided in Table 6. As the semiconductors and the inductors in the design will not be able to act with ideal values, the non-ideal parameters are provided in Table 7.

Table 5: Semiconductor Stresses

Component	**Voltage Stress**	**Current Stress**
S1 & S2 (HV switches)	V_{DC}	$i_{CL,avg} + \Delta i_{CL} + i_{Lb,Peak}$ $i_{CL,avg} - \Delta i_{CL} - i_{Lb,Peak}$
S3 & S4 (LV switches)	V_{DC}	$i_{LLC,avg} + \Delta i_{LLC}$
D1 & D2 (Input Diodes)	V_{DC}	$i_{Lb,peak}$
D3 & D4 (HV Output diodes)	$V_{Anode-Cathode}$	$i_{L_O,peak}$
D5 & D6 (LV output diodes)	$V_{secondary\_LLC} - V_{Filament}$	$\frac{\pi}{2} i_{Filament}$

Table 6: Semiconductors

Semiconductor	**Component**
Input Diodes D_1 & D_2	VS-E4PH6006L-N3
HV output diodes D_3 & D_4	US3M-13
LV output diodes D_5 & D_6	DSS60-0045B
CL MOSFETs S_1 & S_2	UF3C065030T3S
LLC MOSFETs S_3 & S_4	IPA60R360P7SXKSA1
DSP Board	TMDSDOCK28335
DSP Processor	TMS320F28335

Table 7: Non-Ideal Parameters

Parameter	Value	Units
Input filter inductor resistance	2.3	mΩ
Boost inductor resistance	2.16	mΩ
Input diode forward voltage	1.48	V
Step-up resonant		
Switch drain source resistance	27	mΩ
Switch diode forward voltage	1.3	V
Switch output capacitance	293	pF
Transformer primary resistance	250	mΩ
Transformer secondary resistance	90	mΩ
Transformer primary leakage	3.55	µH
Transformer secondary leakage	47	µH
Output diode forward voltage	1.5	V
Step-down resonant		
Switch drain source resistance	360	mΩ
Switch diode forward voltage	0.9	V
Switch output capacitance	10	pF
Transformer primary resistance	64	mΩ
Transformer secondary resistance	33	mΩ
Transformer tertiary resistance	37	mΩ
Transformer primary leakage	28.4	µH
Transformer secondary leakage	1.61	µH
Transformer tertiary leakage	1.4	µH
Output diode forward voltage	0.6	V

3.3.2. DC Input Step-Up Resonant Operation

To evaluate the step-up resonant circuit, the resonant circuit is supplied a DC voltage across the capacitor C_{DC} which will be slowly increased to the value obtained during the simulation stage. For the following test, the resonant stage is then operated with a frequency of 110kHz with a duty ratio of 50% and a deadtime of 3% and a final input voltage of 52.5V.

Figure 3-19 shows the waveforms of S_1 with the current in green and voltage in yellow, along with the CL resonant current in blue. From this waveform, the green switch current can be observed as negative during the turn-on. This means that the current is flowing through the anti-parallel diode during the turn-on which confirms that the switch experiences ZVS turn-on soft switching. Additionally, the resonant current in blue is observed to match the expected response from the theoretical section, with the addition of some noise.

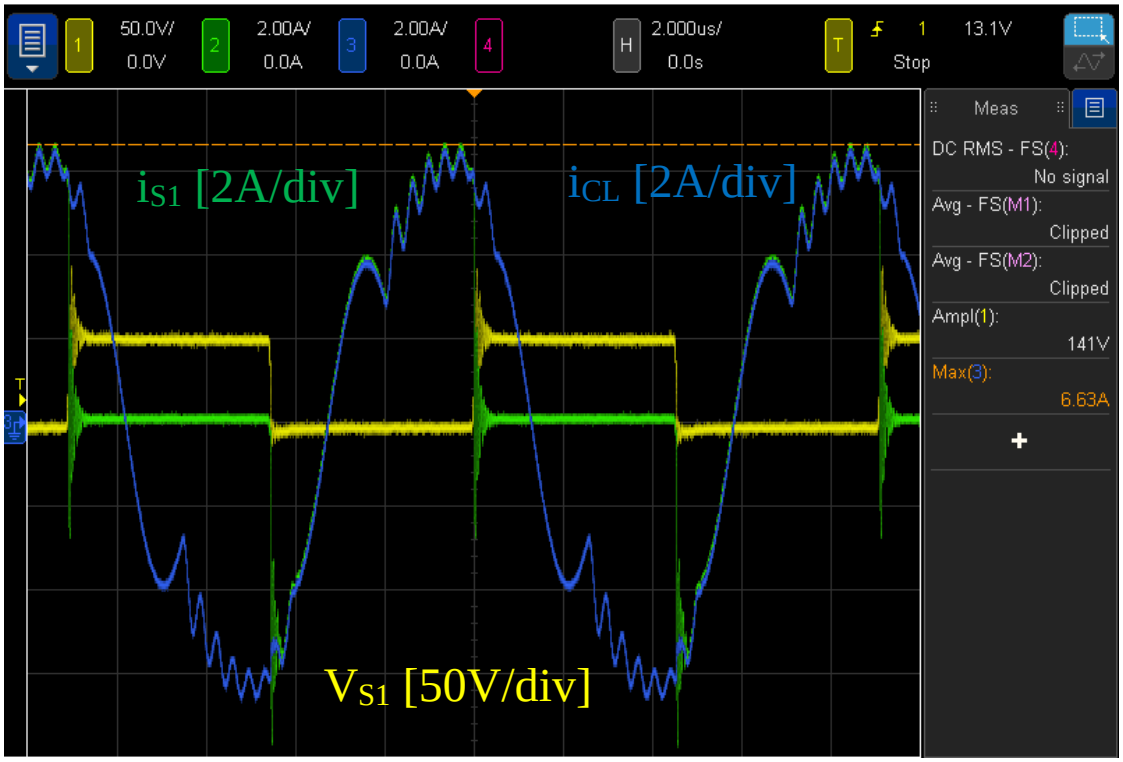


Figure 3-19: S1 current and voltage & CL resonant current hardware testing waveforms

Figure 3-20 shows the zoomed in turn-off waveforms of S_1 with the voltage shown in yellow and current in green. Here the switch current can be observed as not fully reaching zero before the snubber capacitor is able to charge up to V_{DC}, resulting in an overshoot of the voltage which causes further oscillations. Whilst this is undesired, at a higher voltage the snubber capacitor will require more time to fully charge which will allow for more time for the current to reduce to zero.

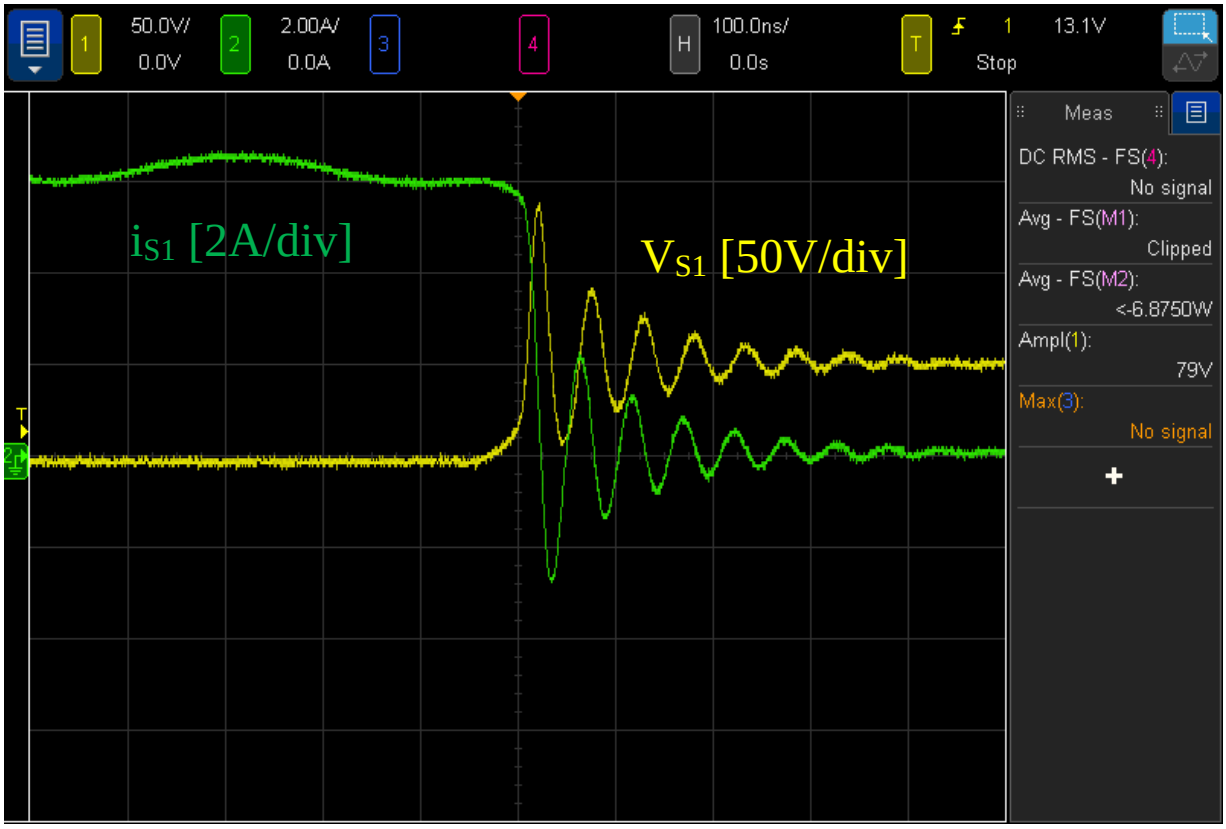


Figure 3-20: S1 turn-off waveforms

Figure 3-21 Shows the input and output waveforms to observe the power and efficiency of the step-up stage with a DC input. The input voltage shown in yellow, and the input current shown in green, provide the power which is shown as 61.127W on the sidebar through “M1”. The output

voltage in red, and output current in blue show the output voltage on the sidebar as 51.614W through “M2”, which may be slightly lower than actual due to imperfect calibration of current probe at low values. Finally, the instantaneous efficiency is shown in pink with the average being shown on the sidebar as 85.4% with “M3”. This also shows that with the input voltage of 52.5V an output voltage of 921V is able to be achieved for a step-up ratio of 17.5. Using this ratio allows for the 4kV output to be estimated as requiring an input of 228V.

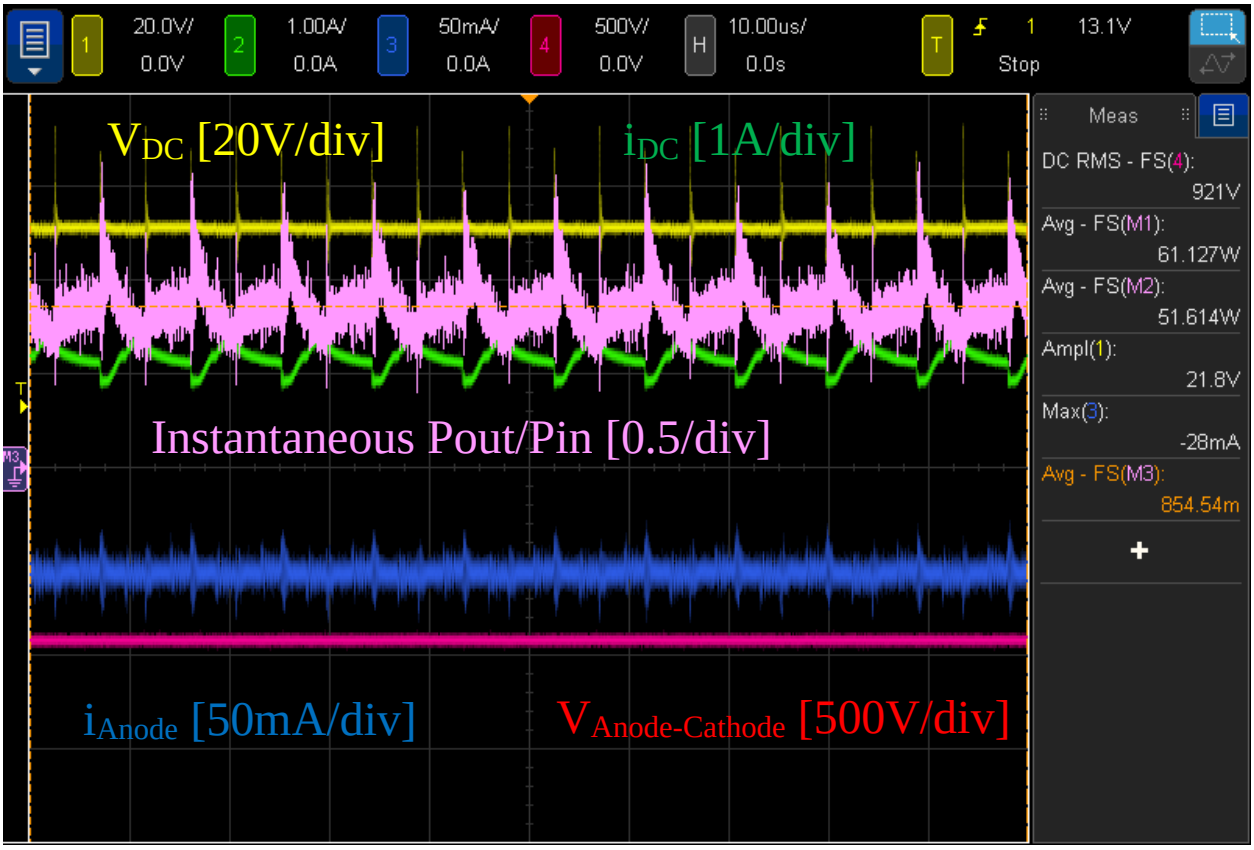


Figure 3-21: Input and output waveforms with efficiency

3.3.3. DC Input Step-Down Resonant Operation

To evaluate the step-down resonant circuit, the resonant circuit is supplied a DC voltage across the capacitor C_{DC} which will be slowly increased to the value obtained during the simulation stage. For the following test, the resonant stage is then operated with a frequency of 108kHz with a duty ratio of 50% and a deadtime of 3% and a final input voltage of 241.5V.

Figure 3-22 shows the switch measurements for S_3 of the step-down resonant circuit along with the LLC resonant current. The switch current, shown in green, can be observed to be negative during the period when the voltage across the switch, shown in red, which confirmed that S_3 is operating with ZVS turn-on. Additionally, the resonant current, shown in blue, can be observed as matching the current across S_3 which matches the expected results obtained from the theory and simulations. Finally, whilst the waveform operates as expected, ringing can be observed in the switch and resonant currents.

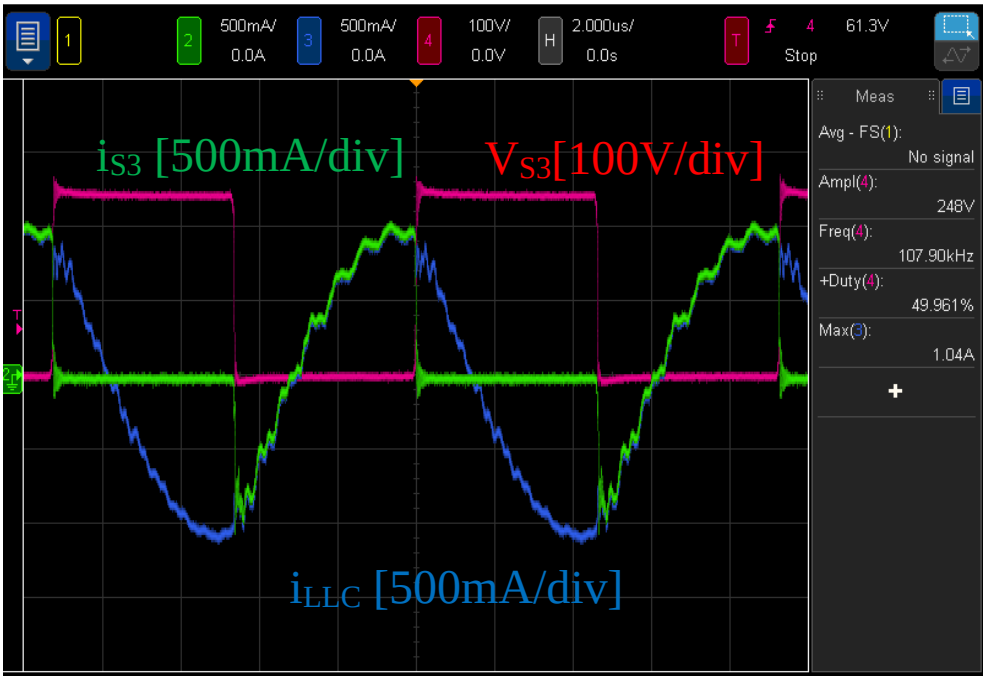


Figure 3-22: S3 current and voltage & LLC resonant current hardware testing waveforms

Figure 3-23 Shows a zoomed in section of the switch current and voltage at turn-off. Here the current, shown in green, is shown to be significantly reduced before the voltage increases. As the current is not fully zero, this shows that the switch experiences near ZCS turn-off.

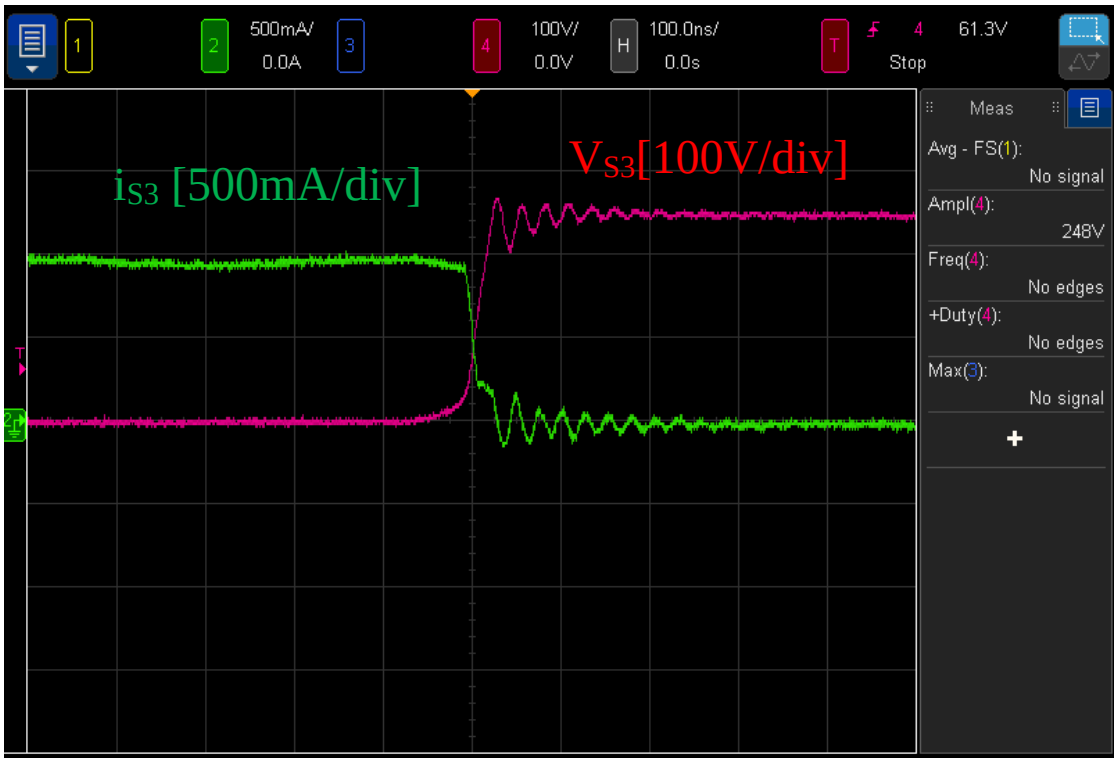


Figure 3-23: S3 Turn-off near ZCS hardware testing

Figure 3-24 shows the output diode waveforms for D_5 & D_6. For D_5 the current is shown in blue and the voltage is in yellow. For D_6 the current is shown in green. From these waveforms, the two diode currents are shown to be half sine waves as expected with ringing shown during the switching waveforms still being present. The voltage is also as expected being negative whilst the corresponding diode is not conducting and is 1.3V, shown on the right-side measurement bar, when the diode is conducting which corresponds to the threshold voltage.

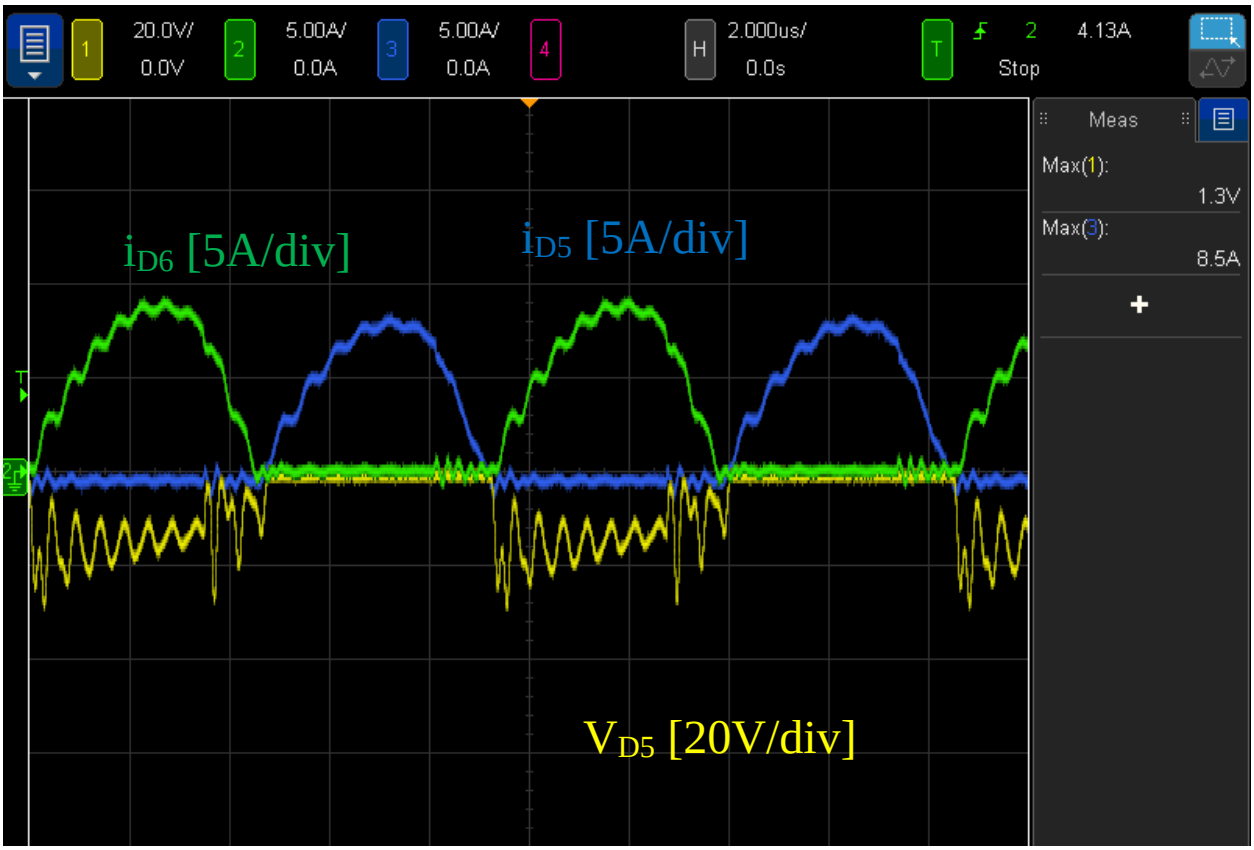


Figure 3-24: Output diode D5 voltage and current from hardware testing

Figure 3-25 shows the input voltage in red, input current in blue, output voltage in yellow, and output current in green. From these waveforms, the power of the step-down stage can be calculated as 35.44W in, 27.06W out, and an efficiency of 77.6% which can be observed on the measurement bar. Additionally, this waveform confirms that an input voltage of 243V is being stepped down to 5.25V under the tested operating conditions.

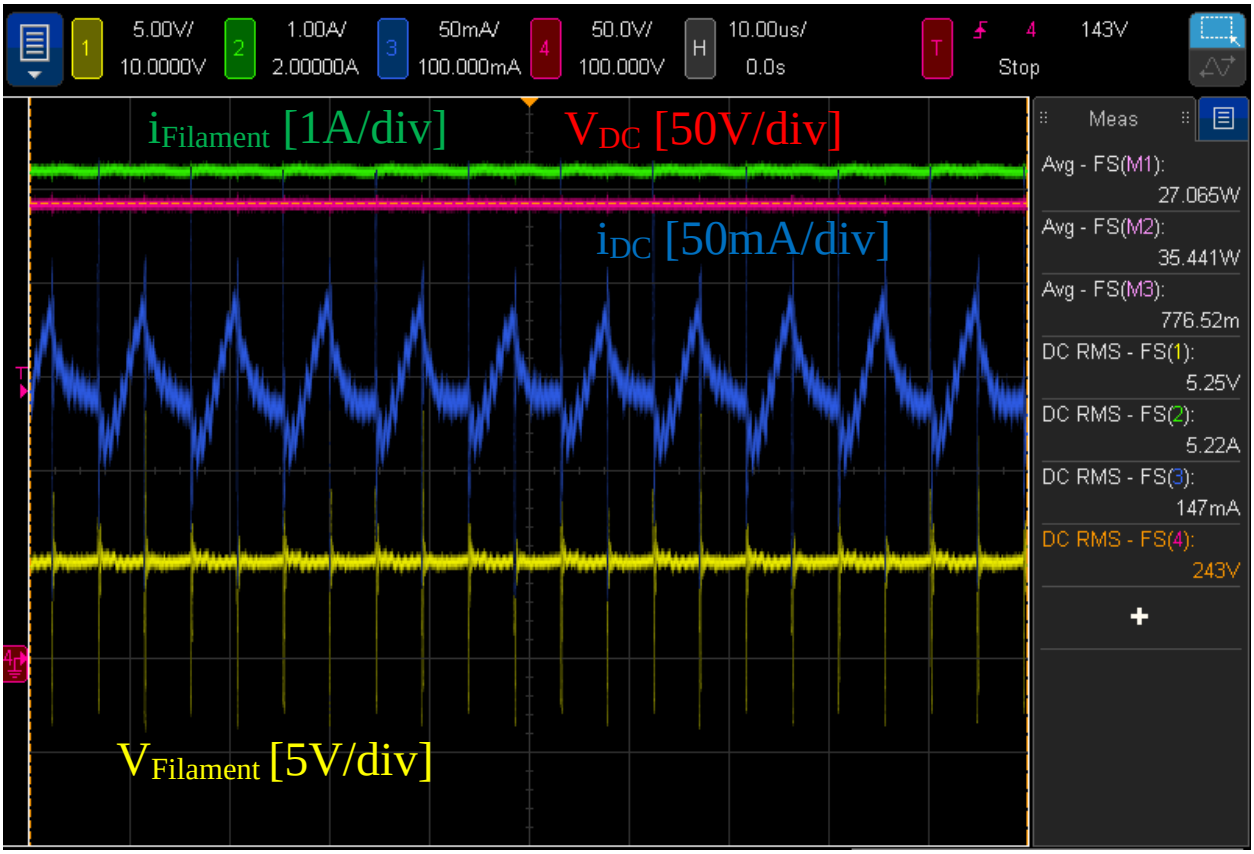


Figure 3-25: LLC input and output currents and voltages.

3.3.4. DC Input Combined Operation

To evaluate the combined resonant circuit operation, the resonant circuits are supplied a DC voltage across the capacitor C_{DC} which will be slowly increased to the value obtained during the simulation stage. For the following test, the step-up resonant stage is operated with a frequency of 110kHz with a duty ratio of 50% and a deadtime of 3%, the step-down resonant stage is operated with a frequency of 108kHz with a duty ratio of 50% and a dead time of 3% and a final input voltage of 50.4V.

Figure 3-26 shows the input voltage and current in yellow and blue respectively, along with the low voltage output in green and the high voltage output in red. From these waveforms, it can be observed that both of the output voltages match the expected results of the previous hardware tests and simulations with the input voltage of 50.4V, high voltage output of 889V, and low voltage output of 1.5V based on the sidebar measurements. Based on the input current and voltage waveform, the average input power is measured as 55.466W on the sidebar measurements. With the known resistances of 15.2kΩ for the high voltage load and 1Ω for the low voltage load, the output power is calculated to be approximately 53.9W. An additional observation that can be made is that the DC-link voltage has some noise when the $S_1 \& S_2$ switches turn off, which will be improved in future work by adding an additional RC snubber to filter out the higher frequency noise.

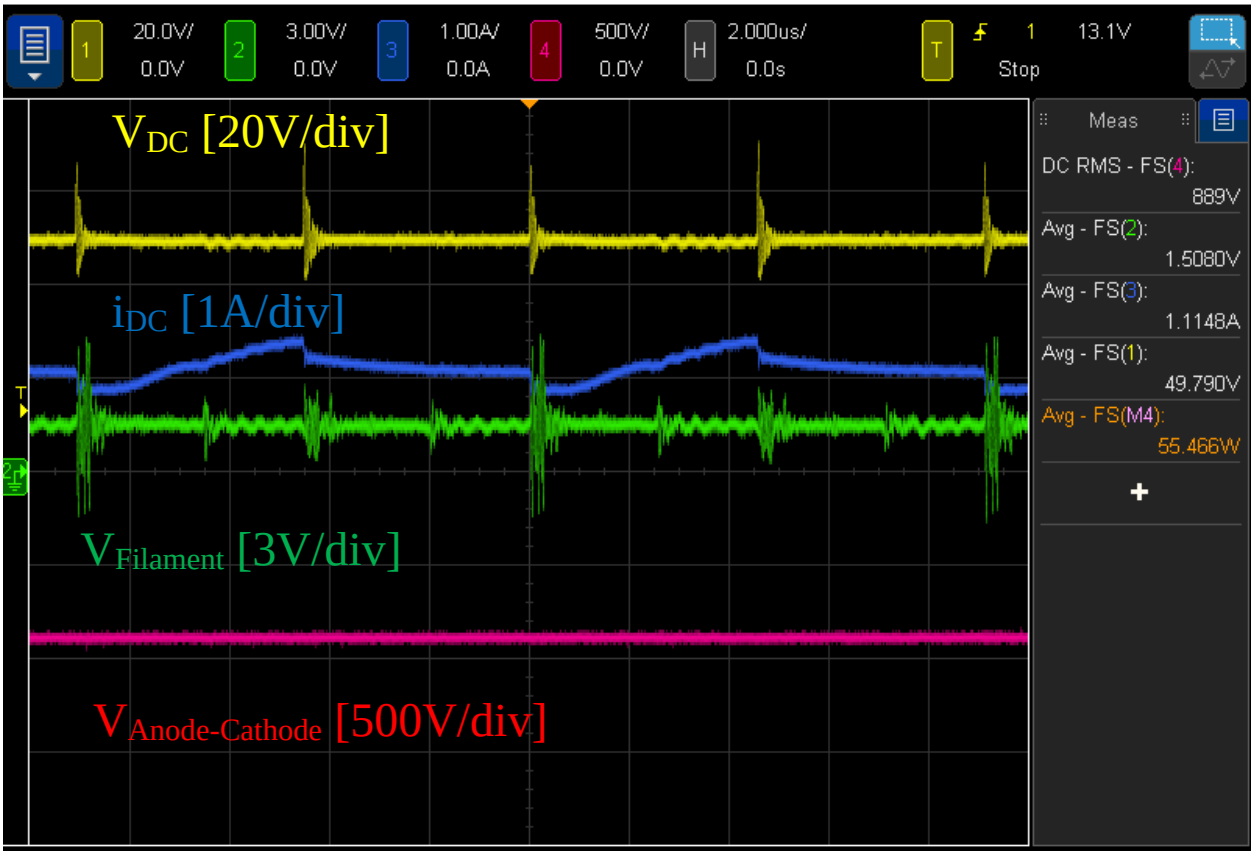


Figure 3-26: Combined DC test inputs and output voltages

Figure 3-27 shows the S_1 voltage in green and the current in red. Comparing the results to those in Figure 3-19 from section 3.3.2 shows that the combined DC input operation does not impact the step-up resonant switches.

Figure 3-28 shows the S_3 voltage in yellow, the current in blue, and the S_1 voltage in green. Comparing the S_3 waveforms from Figure 3-22 in section 3.3.3 the current waveforms can be observed as experiencing spikes of noise. These noise spikes can also be observed as occurring when S_1 turns off. This will be improved in future work with the previously mentioned DC-link snubber along with adding a larger ground plane. Aside from the noise produced by the S_1 & S_2 pair, the waveforms match the results of the simulations and previous hardware tests.

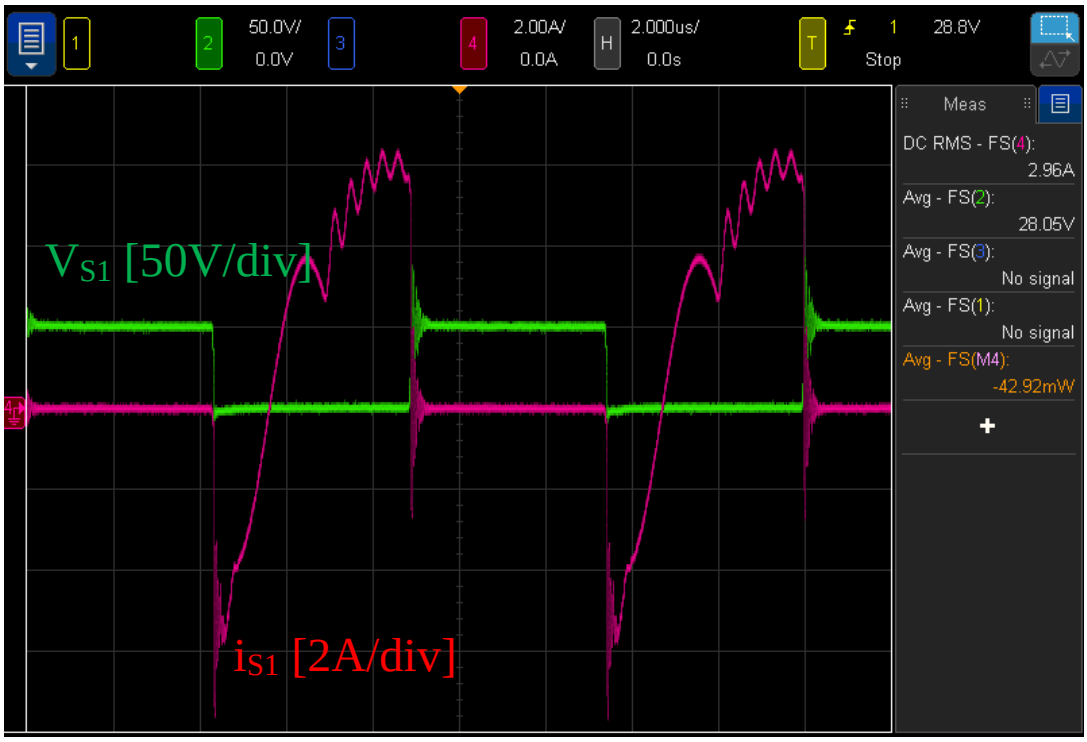


Figure 3-27: Switch 1 voltage and current during combined DC test

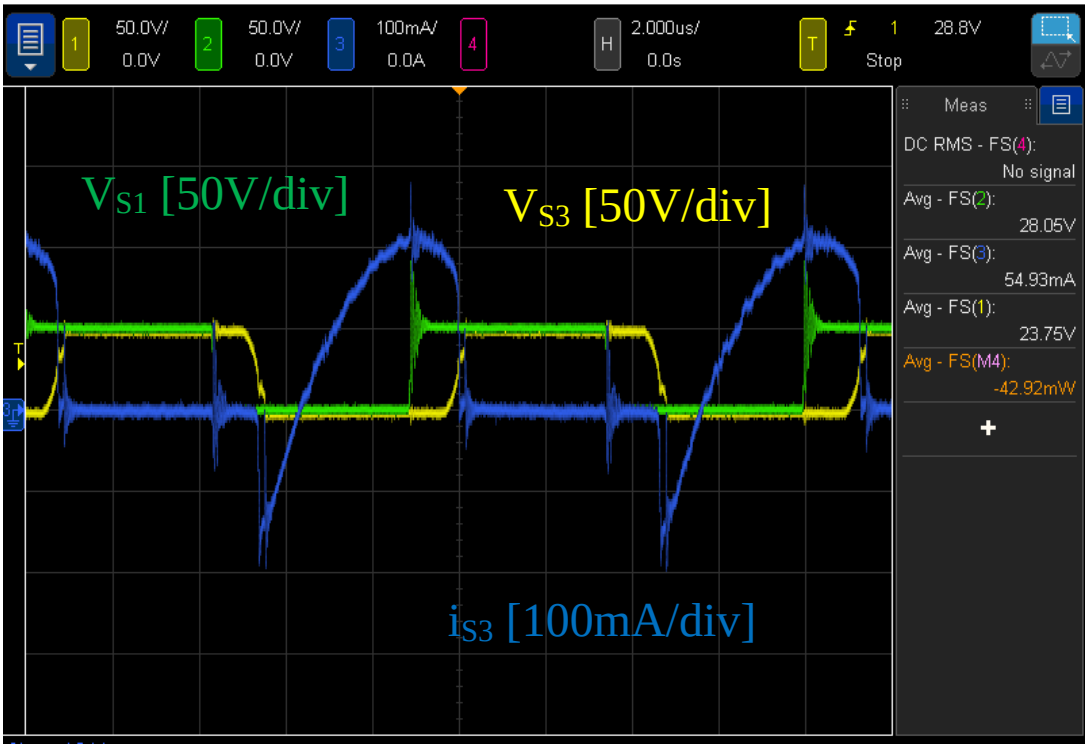


Figure 3-28: Switch 3 current and voltage and Switch 3 voltage during combined DC test

3.3.5. AC Input Full Circuit Operation

Having confirmed both DC resonant circuits operate as expected, the AC input proposed topology can be tested and validated. For validation of the AC input a $20V_{RMS}$, 60Hz input voltage was supplied to the input. This value was selected such that V_{DC} matches the maximum tested DC link voltage tested in sections 3.3.2 and 3.3.4. The switching frequencies also matched the previous section with the step-up resonant circuit having a switching frequency of 110kHz at 50% duty ratio and a dead time of 3%, whilst the step-down resonant circuit has a switching frequency of 108kHz at 50% duty ratio and a dead time of 3%. Additionally, the input boost inductor of 15µH was swapped for a 10µH inductor for these proof-of-concept tests to ensure DCM operation whilst the efficiency of the circuit is being improved. This change will only result in slightly higher current peaks through the input inductor, input diodes, and $S_1 \& S_2$ switch pair.

Figure 3-29 shows the input current in blue. From this waveform, the input current can be observed as near sinusoidal with a slight distortion at the peaks, which matches the results from the simulations. Observing Figure 3-30 also shows the power analysis for the input voltage and current. From this figure, the PF can be observed to be 0.962 under these specific operating conditions, which again matches the expected value obtained during simulations and also confirms that the input current is in phase with the input voltage.

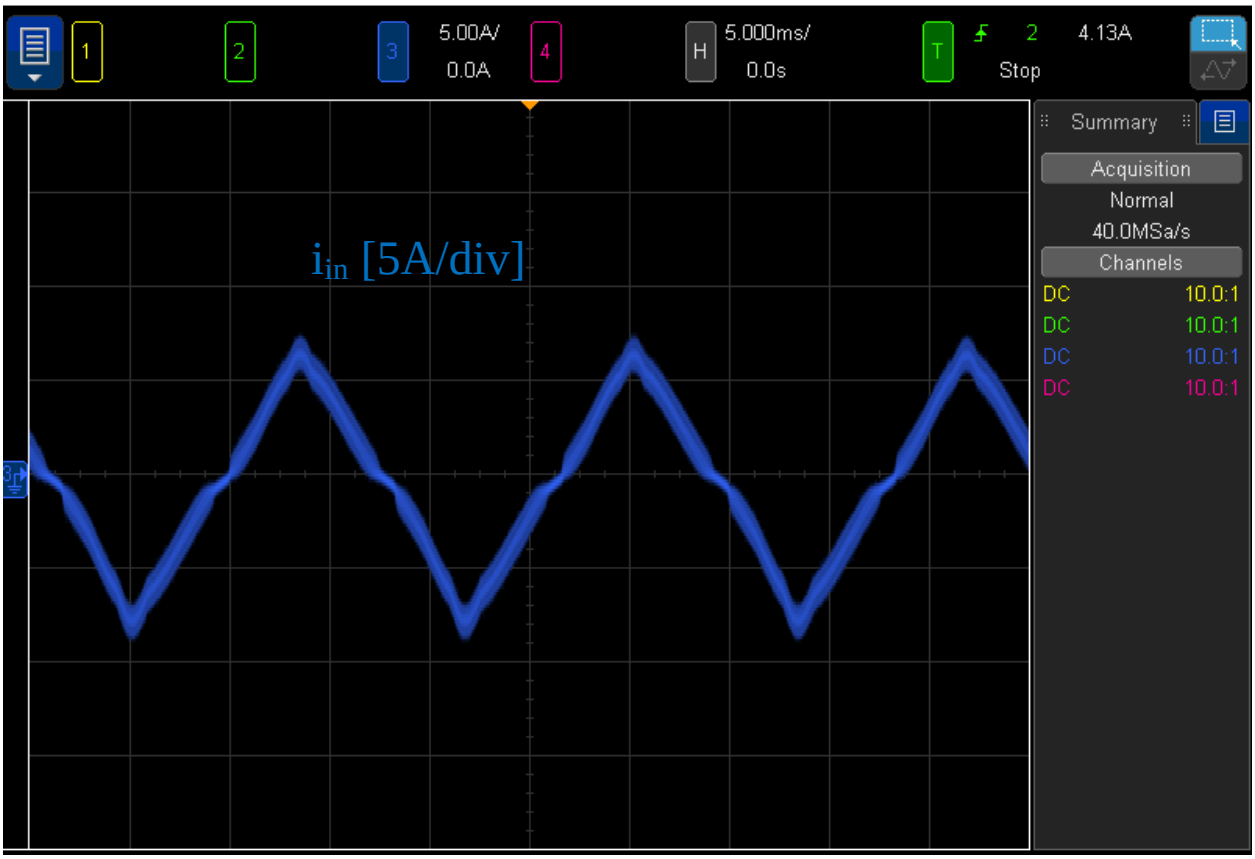


Figure 3-29:AC input currents

Measure	Current	Mean	Min	Max	Std Dev	Count
Avg - FS(1):	-1.053V	-1.1840V	-3.330V	-360mV	327.15mV	1.955k
Power Factor(1→3):	962m	962.00m	962m	962m	0.0	1
Real(M1):	78.4W	78.400W	78.4W	78.4W	0.0W	1
Apparent(1→3):	81.5VA	81.500VA	81.5VA	81.5VA	0.0VA	1
Reactive(1→3):	22.3VAR	22.300VAR	22.3VAR	22.3VAR	0.0VAR	1
Crest(1):	3.136	3.1360	3.136	3.136	0.0	1
Crest(3):	2.130	2.1300	2.130	2.130	0.0	1
Phase Angle(1→3):	15.90°	15.900°	15.90°	15.90°	0.0°	1
DC RMS - Cyc(1):	19.6V	19.600V	19.6V	19.6V	0.0V	1
Freq(1):	60.02Hz	60.010Hz	60.01Hz	60.01Hz	0.0Hz	1

Figure 3-30: Input power analysis measurements

Figure 3-31 shows the zoomed-out waveforms of S_1 with voltage in yellow and current in blue along with the boost inductor current in green. From these waveforms, the voltage can be observed as operating around the 50V with some low frequency ripple that corresponds to the ripple of the V_{DC} voltage. Additionally, the overshoot can be observed as peaking at about 90V over the entire duration of the line cycle. Observing the switch current shows that its magnitude closely follows the form of the boost inductor, which is as expected from the theory and simulation sections. Finally observing the boost inductor current shows that for the majority of its operation it is in DCM whilst a small portion is in CCM. Whilst this is not desired, the THD and PF observed above show that this small section of CCM operation does not impact the input current too drastically. The reason for this result not matching those of the simulations is due to the lower efficiency in the hardware tests which impacts the maximum boost inductor value to remain in DCM. Improving this will be part of future work. Figure 3-32 shows a zoomed in portion of the same waveforms during a negative line cycle and Figure 3-33 shows a zoomed in portion during a positive line cycle. From these two figures, the switch current can be observed as operating with ZVS turn-on. The switch current can also be observed as following the boost inductor current and resonant currents from the DC test stage, which matches Equation 2-21, Equation 2-22, and the simulations.

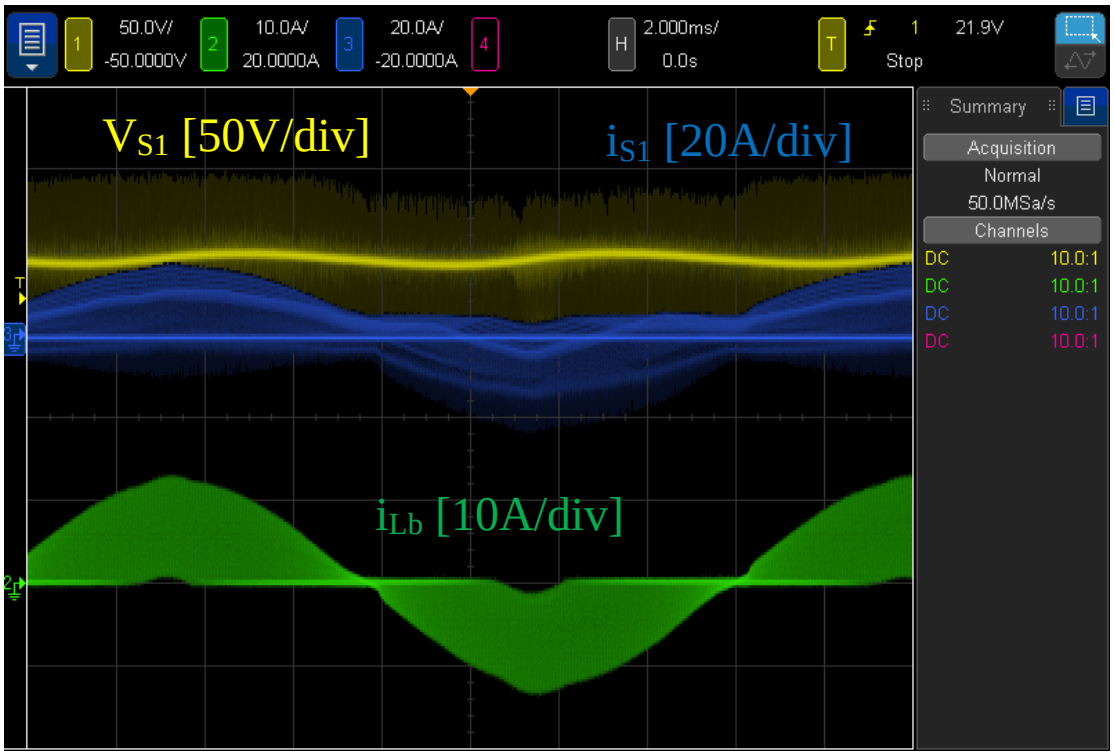


Figure 3-31: S_1 voltage (yellow), current (blue), and boost inductor current (green) zoomed out.

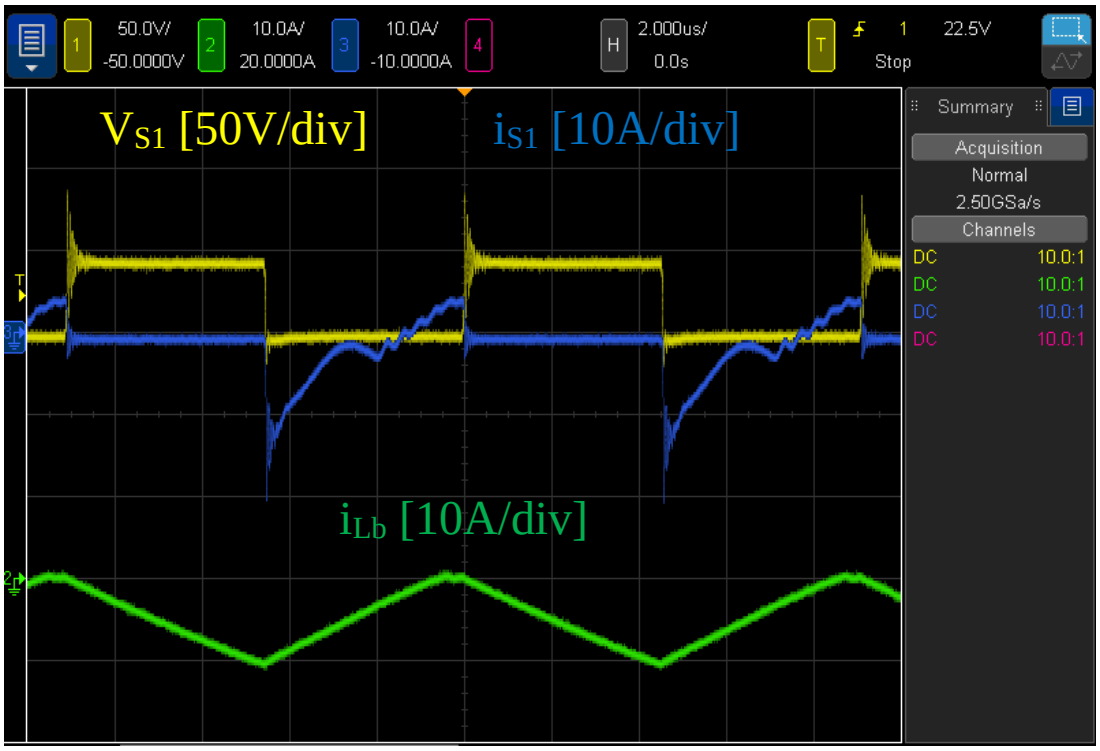


Figure 3-32: S_1 voltage (yellow), current (blue), and boost inductor current (green) zoomed in [negative line input]

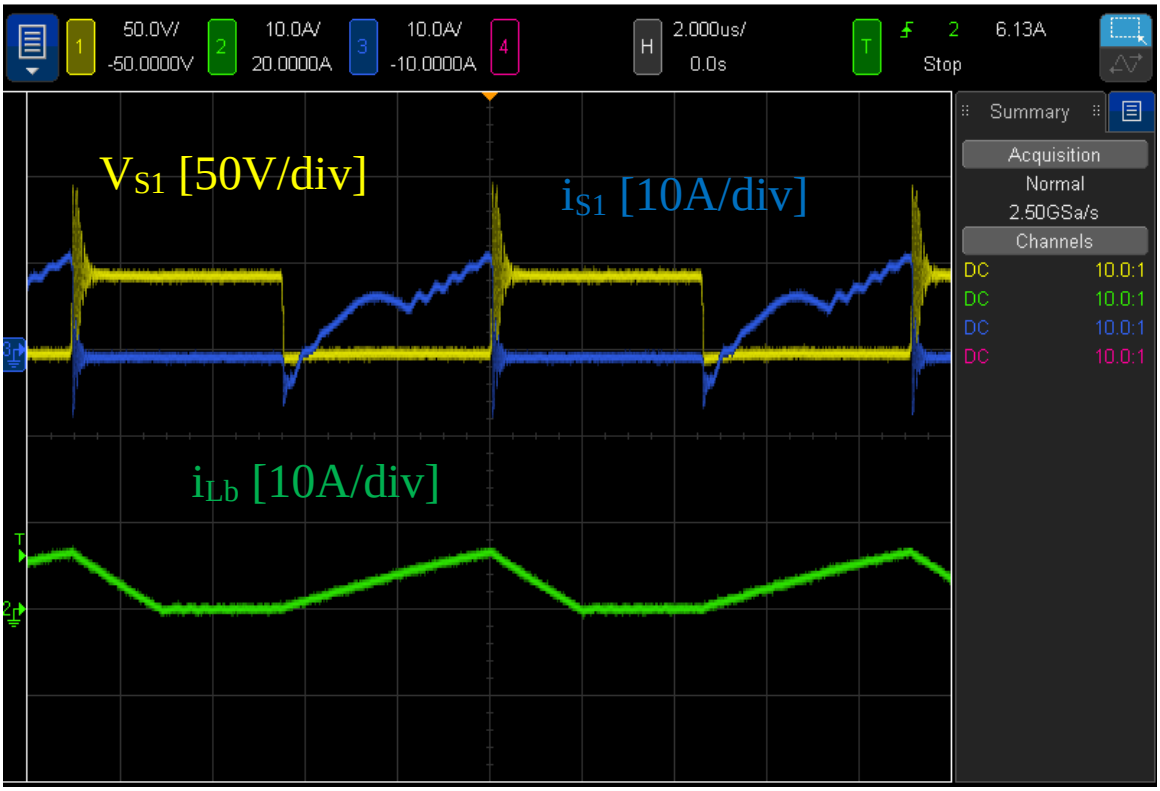


Figure 3-33: S_1 voltage (yellow), current (blue), and boost inductor current (green) zoomed in [positive line input]

Figure 3-34 shows the two outputs and the DC-link voltages, with the high voltage cathode-anode voltage in green, the low voltage filament in red, and the DC-link voltage in yellow. From the sidebar of the oscilloscope view the values can be read as 46.02V for the DC-link, -822.9V for the cathode-anode voltage, and 1.298V for the filament voltage. These results show that the AC input test matches similar gain ratios from V_{DC} to the two outputs as that of the DC input tests. Additionally, a test with no load for the cathode-anode output was tested with the V_{DC} and outputs shown in Figure 3-35. This test confirms that V_{DC} is nonzero when the cathode-anode resonant circuit has no load, allowing for the filament to still operate and be pre-heated when the magnetron would be in the non-oscillation region.

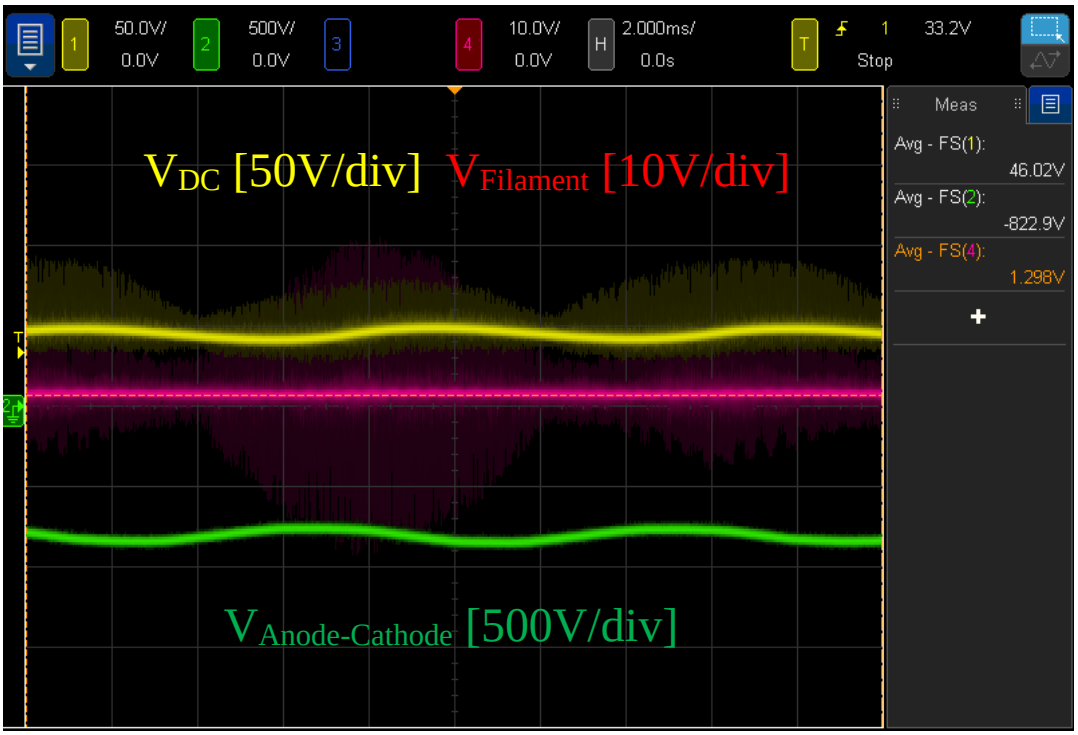


Figure 3-34: VDC (yellow), low voltage output (red), high voltage output (green)

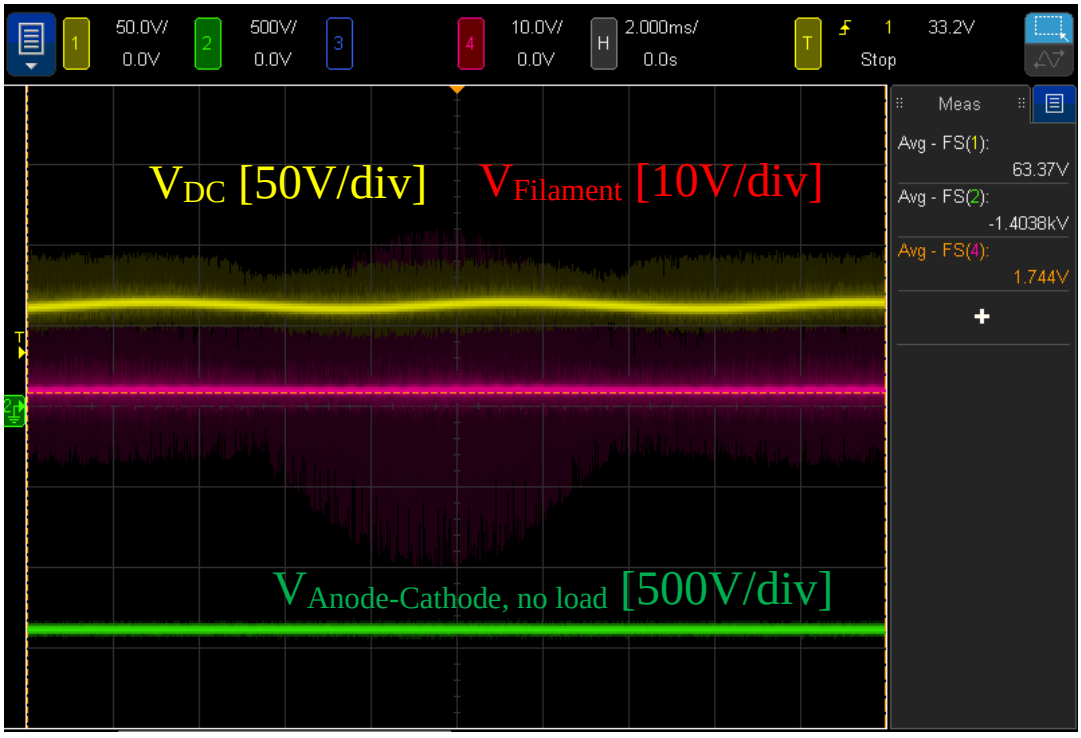


Figure 3-35: VDC (yellow), low voltage output (red), high voltage output (green). No load cathode-anode condition.

During the operation with an AC input under the above conditions, the main components that heat was observed through are the $S_1 \& S_2$ pair, and the input diodes $D_1 \& D_2$ which can be observed in Figure 3-36. During these tests, the cooling provided to these components was natural convection along with heatsinks. As the switches reached temperatures of approximately 51°C, increasing the supply conditions will require better heat dissipation such as forced airflow, or redesign of the PCB to allow for the drain tab to connect to the PCB and utilize it as a heat spreader.

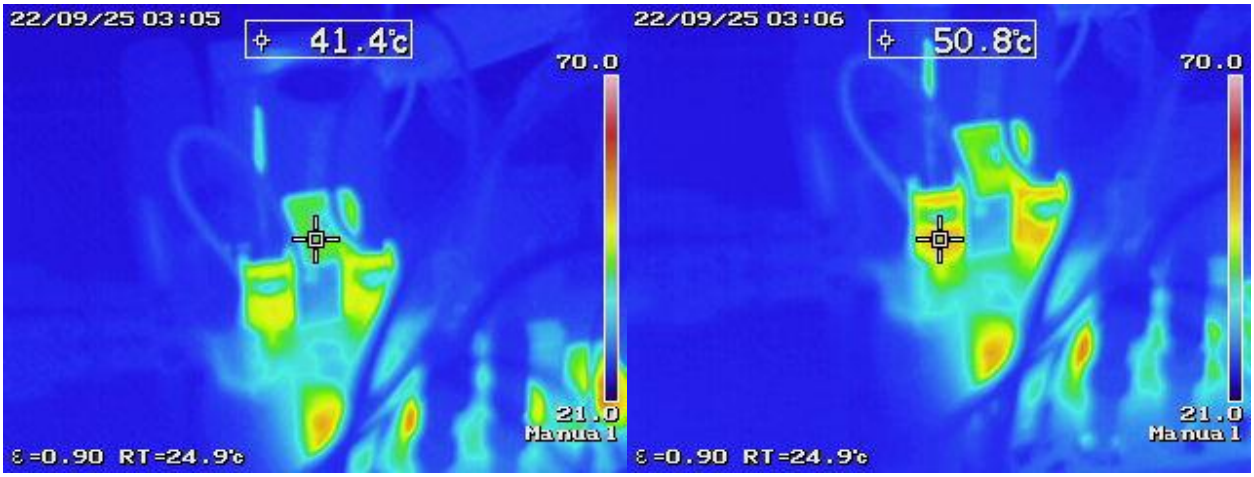


Figure 3-36: Thermal images. Left: D_2. Right: S_1

3.4. Comparison

To better understand the results of the proposed converter, it will be compared to multiple other magnetron converters discussed in literature. Provided by Table 8 is a comparison of the proposed converter to some converters from literature. The table compares the number of semiconductors, switches and diodes, the different input voltages for operation, the PF for AC supplied converters, the efficiency, and if the converter allows for the filament voltage to be controlled independent of the high voltage output.

Starting with the converter in [21], this converter utilizes a large amount of semiconductor components with 4 switches and 24 diodes. The large number of diodes will result in significant conduction losses. Additionally, this converter does not offer a separately controllable voltage for the filament supply, which can cause issues as the magnetron will require the filament voltage to be lowered when the high voltage has a higher power output. Finally, this converter will require an additional AC/DC PFC stage to work with an AC input, which will result in a decrease to the efficiency.

The second converter to compare with is from [22]. This converter utilizes 6 switches and 8 diodes, which is 2 switches and 2 diodes more than the proposed converter. The primary reason for these additional components is this circuits use of a separate PFC stage. This separate stage impacts the converters efficiency, as the paper mentions the PFC stage efficiency as 95% to 96% based on load conditions. Additionally, whilst the converter proposed by this paper does provide the ability to control the filaments voltage, the switch for the filament control undergoes hard switching which will reduce the efficiency for the low voltage output and wasn’t included as part of the efficiency.

The third converter that will be compared against is from [23]. This converter utilizes 1 switch and 5 diodes for the DC-DC stage. Whilst this appears as a low component count, the paper excludes mention of the PFC stage, which would add an expected 1 or 2 switches and up to 6 diodes. This converter also does not offer a separately controllable filament voltage, and instead has it again depended on the high voltage output. Finally, this converter has a lower efficiency than some of the other converters reviewed with only an 85% efficiency, whilst most others are in the low 90%.

The fourth converter discussed in [27] is a high power supply that utilizes a 3-phase source. This supply utilizes 6 switches, and 12 diodes. Whilst this converter does have an AC input, it only uses a full bridge rectifier which would result in a lower PF, which isn't mentioned by the paper. This converter does offer a high efficiency during its full load to 60% load conditions, however at lower output conditions it has a significantly reduced efficiency. Additionally, this converter like many of the others does not offer a separately controlled filament voltage.

Comparing to the other converters, the proposed AC converter from this paper has a reduced component count compared to the other converters of 4 switches and 6 diodes by combining the PFC stage and the step-up resonant stage. By combining these two stages the PF stage does not result in a decreased efficiency similar to that of [22]. For the simulated results, the converter achieved a high PF of 0.98 which matched the expected results from other converters being over 0.95, and the efficiency of 90% was achieved for the entire converter which sits amongst the efficiency of the converters from literature. Additionally, compared to many of the other converters the proposed converter offers separate control of the filament voltage.

Table 8: Magnetron Supply Comparison

Converter	**Component count**		**Input voltage**	**Power factor**	**Efficiency**	**Filament Control**
	Switches	Diodes				
[21]	4	24	300 V (DC)	-	Unmentioned	No
[22]	6	8	220 V_{rms} 60 Hz	0.95	91.5%	Yes
[23]	1* (DC-DC stage)	5* (DC-DC stage)	85-264 V_{rms} 47-63 Hz	0.95	85%	No
[27]	6	12	3-phase 380 V_{rms}	Unmentioned	78% at 30% load 90-95% above 60% load	No
Proposed converter (simulation)	4	6	120 V_{rms} 60 Hz	0.98	90%	Yes

3.5. Summary

Chapter 3 presents a set of actual component values to realize the proposed AC input topology, and then performs simulations of the topology in PSIM. After verifying the proposed topology and selected values work max output and nominal output operating conditions, the chapter then moves to verify the results through hardware testing. The hardware testing starts by confirming the proof of concept for the DC input proposed topology, and then once the two simultaneous outputs are confirmed to receive gains as expected the AC input proposed topology is tested with hardware. The AC input proposed topology has its proof of concept confirmed that it can provide PFC, the DC-link voltage and that the DC-link then can be stepped up for one output and stepped down for the other.

4. Conclusion & Future Work

4.1. Summary

To reduce particulate carbon soot, microwave energy is discussed in the literature to assist in oxidizing. To emit this microwave energy, a magnetron unit is used. Powering off the magnetron unit requires two inputs, a high voltage DC and a low voltage AC or DC. Traditional magnetron supplies suffer from low PF due to only using high turns ratio lines frequency transformers for step-up, and literature discussed magnetron supplies tend to require additional circuitry for AC inputs with some even disregarding the low voltage output in the topologies design. As such, this thesis aimed to design a topology that can operate with an AC input, high PFC, and supply both voltages required by a magnetron unit.

4.2. Contributions

The contributions of this thesis are

1. Double DC output DC-DC converter with accompanying theoretical circuit analysis, reduced semiconductor count, and comparable efficiency to converters discussed in literature.
2. Double DC output AC-DC converter with combined PFC stage for high PF and efficiency, with reduced semiconductor count to literature reviewed topologies, and accompanying theoretical analysis.

3. Proposed converter allows for filament voltage to be controlled independent of high voltage output to allow filament voltage to decrease as the high voltage increases, allowing for improved lifespan of magnetron in comparison to other discussed converter topologies.
4. Proposed converter operates with ZVS turn-on and near ZCS turn-off soft switching to allow for high frequency 100kHz switching resulting in the use of smaller passive components.
5. Simulations and proof-of-concept hardware tests performed to confirm the circuits theoretical analysis and an estimate as to the achievable efficiency and PF of the proposed converter.

4.3. Future Work

Future work for this project includes:

4.3.1. Implementation Of Feedback Loops

As mentioned during the simulation portion, a feedback loop was implemented to keep high voltage output at its desired value. The future work regarding the feedback loops includes implementing the loops in actual hardware, improving the simulation loop to provide small signal correction, and adding a feedback loop for the low voltage output.

4.3.2. Reduce Noise Throughout Circuit

Throughout the hardware testing performed in section 3.3, noise was evident in multiple forms. This noise was noticeable in the DC link voltage during the DC input tests, the switch currents, and the step-down output voltage. Some of the suspected sources of noise throughout the circuit are hard switching turn-off of switches at lower voltages and components resonating with each other such as stray inductances and switch capacitances. Some of the potential ways to reduce

these sources of noise include adding RC snubbers for the DC link, ferrite beads for the switch gates, using RC snubbers for the switches to dampen the overshoot at lower power to discharge capacitors faster, adding a ground plane, reducing PCB loop sizes, and improving decoupling capacitors placement near switching IC's.

4.3.3. Further Increase Efficiency of Hardware

Throughout hardware testing, different stages ranged in efficiencies from 80% to 92% for the tests performed. Future work includes determining the sources of power loss and improving them. Currently, the magnetic components with DC resistances, such as transformers and inductors, along with semiconductor components with conductive losses and switching losses, diodes, and switches, are the main focus for power loss. Additionally, the PCB design may be reviewed to ensure that high current traces are short to prevent trace conduction losses.

4.3.4. Hardware Test Real Magnetron

Whilst two different models of a magnetron were confirmed for simulation, the hardware testing thus far has included only with fixed load resistance tests. Future work includes testing the power supply up to the full voltage required high voltage and then connecting a real magnetron to the power supply to ensure that the magnetron works as anticipated with the design. This future work will require additional safety to be taken due to the increased voltage required along with the microwave radiation that will be produced by the magnetron.

4.4. Conclusions

To conclude, a double DC output converter with either AC or DC input was proposed for the function of providing the required inputs of a magnetron. The topologies theoretical analysis was performed to understand its operation. The proposed topology utilized soft switching technique ZVS turn-on and near ZCS turn-off to allow for a significantly reduced switching loss to allow for a higher frequency to be utilized. This higher frequency allowed for smaller sized passive components to be utilized. The topology was then simulated in PSIM and verified to work under two separate operating conditions. Finally, hardware testing was performed to validate the topologies' proof-of-concept. From the hardware proof-of-concept, the topology was shown to operate with a high PF with the AC input.

Publications

M. Bakalian and J. Lam, "A Double-Output Soft-Switched Step-Up AC/DC Bridge-Less Converter for Microwave Energy Application," in Proceedings of the IECON 2021 – 47th Annual Conference of the 2021 IEEE Industrial Electronics Society, 2021, pp. 1-6

M. Bakalian and J. Lam, "Dual CL/LLC DC/DC Resonant Circuit Modules for Step-up Power Interface in Microwave Magnetron Application," submitted to the 2022 IEEE Industrial Electronics Society Annual On-Line Conference (ONCON).

Bibliography

[1] H. Omidvarborna, A. Kumar, and D.-S. Kim, "Recent studies on soot modeling for diesel combustion," *Renew. Sustain. Energy Rev.*, vol. 48, pp. 635–647, Aug. 2015.

[2] H. Törnqvist *et al.*, "Persistent Endothelial Dysfunction in Humans after Diesel Exhaust Inhalation," *Am. J. Respir. Crit. Care Med.*, vol. 176, no. 4, pp. 395–400, Aug. 2007.

[3] H. Omidvarborna, A. Kumar, and D. S. Kim, "Characterization of particulate matter emitted from transit buses fueled with B20 in idle modes," *J. Environ. Chem. Eng.*, vol. 2, no. 4, pp. 2335–2342, 2014.

[4] H. B. Al-Wakeel, Z. A. A. Karim, and H. H. Al-Kayiem, "A technique for localized rapid soot oxidation using metal aided microwave radiation," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 1, pp. 37–43, 2016.

[5] M. Feulner, F. Seufert, A. Müller, G. Hagen, and R. Moos, "Influencing Parameters on the Microwave-Based Soot Load Determination of Diesel Particulate Filters," *Top. Catal.*, vol. 60, no. 3–5, pp. 374–380, Mar. 2017.

[6] E. Meloni, V. Palma, and V. Vaiano, "Optimized microwave susceptible catalytic diesel soot trap," *Fuel*, vol. 205, pp. 142–152, 2017.

[7] J. Ma, M. Fang, P. Li, B. Zhu, X. Lu, and N. T. Lau, "Microwave-assisted catalytic combustion of diesel soot," *Appl. Catal. A Gen.*, vol. 159, no. 1–2, pp. 211–228, 1997.

[8] D. E. Clark, D. C. Folz, and J. K. West, "Processing materials with microwave energy," *Mater. Sci. Eng. A*, vol. 287, no. 2, pp. 153–158, Aug. 2000.

[9] S. A. Galema, "Microwave chemistry," *Chem. Soc. Rev.*, vol. 26, no. 3, p. 233, 1997.

[10] X. Zhang, K. Rajagopalan, H. Lei, R. Ruan, and B. K. Sharma, “An overview of a novel concept in biomass pyrolysis: microwave irradiation,” *Sustain. Energy Fuels*, vol. 1, no. 8, pp. 1664–1699, 2017.

[11] J. Sun, W. Wang, C. Ma, and Y. Dong, “An exploratory study of electronic waste treatment: Microwave-induced pyrolysis,” *Asia-Pacific Power Energy Eng. Conf.*, pp. 10–13, 2010.

[12] X. Y. Li, J. Yan, H. Yang, T. Peng, and Q. C. Yang, “Study on processing technology for microwave pyrolysis of municipal solid waste,” *ICMREE2011 - Proc. 2011 Int. Conf. Mater. Renew. Energy Environ.*, vol. 1, pp. 336–340, 2011.

[13] M. A. Budianto, S. Anis, and W. Sumbodo, “Study of thermal heating of waste engine oil in a microwave pyrolysis reactor,” *J. Phys. Sci.*, vol. 29, pp. 39–52, 2018.

[14] J. E *et al.*, “Effects analysis on optimal microwave energy consumption in the heating process of composite regeneration for the diesel particulate filter,” *Appl. Energy*, vol. 254, no. April, p. 113736, Nov. 2019.

[15] M. Heggannavar and H. Kulkarni, “Design of Magnetron power source from three phase supply,” *Int. Conf. Energy Syst. Appl. ICESA 2015*, no. Icesa, pp. 552–556, 2016.

[16] E. G. Linder and J. E. Brittain, “The Magnetron,” *Phys. Today*, vol. 39, no. 1, pp. 115–116, Jan. 1986.

[17] “Magnetron view.” [Online]. Available: https://www.britannica.com/facts/magnetron#/media/1/357510/137. [Accessed: 21-Mar-2022].

[18] V. Surducan, E. Surducan, R. Ciupa, and C. Neamtu, “Microwave generator for scientific and medical applications,” *AIP Conf. Proc.*, vol. 1425, no. April 2015, pp. 89–92, 2012.

[19] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power electronics converters, applications*

and design, Third. John Wiley & Sons, INC, 2003.

[20] L. Wuidart, "Understanding Power Factor," *STMicroelectronics*. pp. 1–5, 1999.

[21] S. W. Choi, I. O. Lee, and J. Y. Lee, "Design of 5-kV/5-kW Magnetron Power Supply Using PWM SRC with PISO-Connected Transformer," *IEEE Trans. Plasma Sci.*, vol. 46, no. 8, pp. 2840–2847, 2018.

[22] M. J. Kim, W. S. Choi, I. W. Jeong, H. C. Park, and K. H. Park, "A New Driving Method of the Magnetron Power Supply for a Sulfur Plasma Lamp," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5416–5424, 2016.

[23] B. M. Song, M. H. Kye, and R. Y. Kim, "Design of a cost-effective DC-DC converter with high power density for magnetron power supplies," *2010 Int. Power Electron. Conf. - ECCE Asia -, IPEC 2010*, pp. 137–141, 2010.

[24] W.-Y. Choi and J.-S. Yoo, "A Bridgeless Single-Stage Half-Bridge AC/DC Converter," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3884–3895, Dec. 2011.

[25] B. B. Sun, "Control challenges in a totem-pole PFC," *Analog Appl. J.*, pp. 1–5, 2017.

[26] B. Sun, "How to reduce current spikes at AC zero-crossing for totem-pole PFC," *Analog Appl. J.*, no. 4Q, 2015.

[27] S. R. Jang, H. J. Ryoo, S. H. Ahn, J. Kim, and G. H. Rim, "Development and optimization of high-voltage power supply system for industrial magnetron," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1453–1461, 2012.

[28] Wikipedia contributors, "Kondensatoren-Kap-Versus-Spg-English," *Wikimedia Commons*, 2012. [Online]. Available: https://commons.wikimedia.org/wiki/File:Kondensatoren-Kap-Versus-Spg-English.svg#filehistory. [Accessed: 03-Oct-2022].

A. Appendix

Additional Diagrams

Psim Diagrams

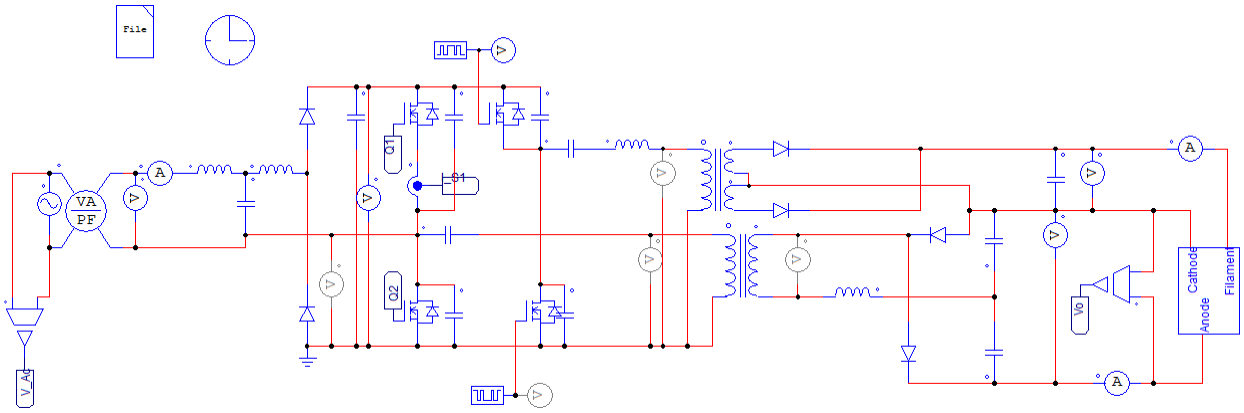


Figure A-1: PSIM Schematic

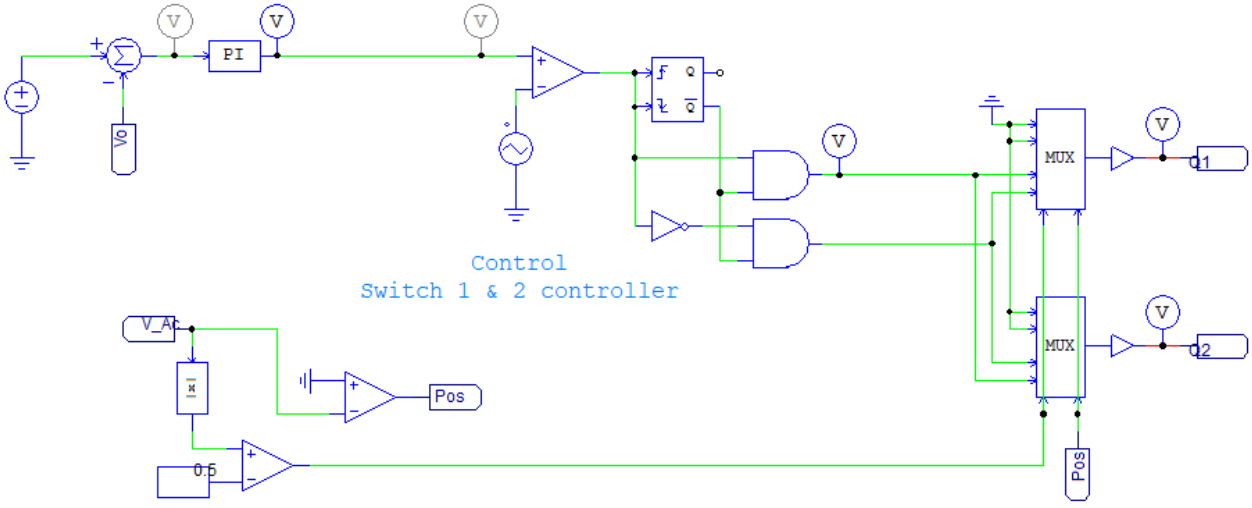


Figure A-2: PSIM Switch 1 & 2 Controller

a

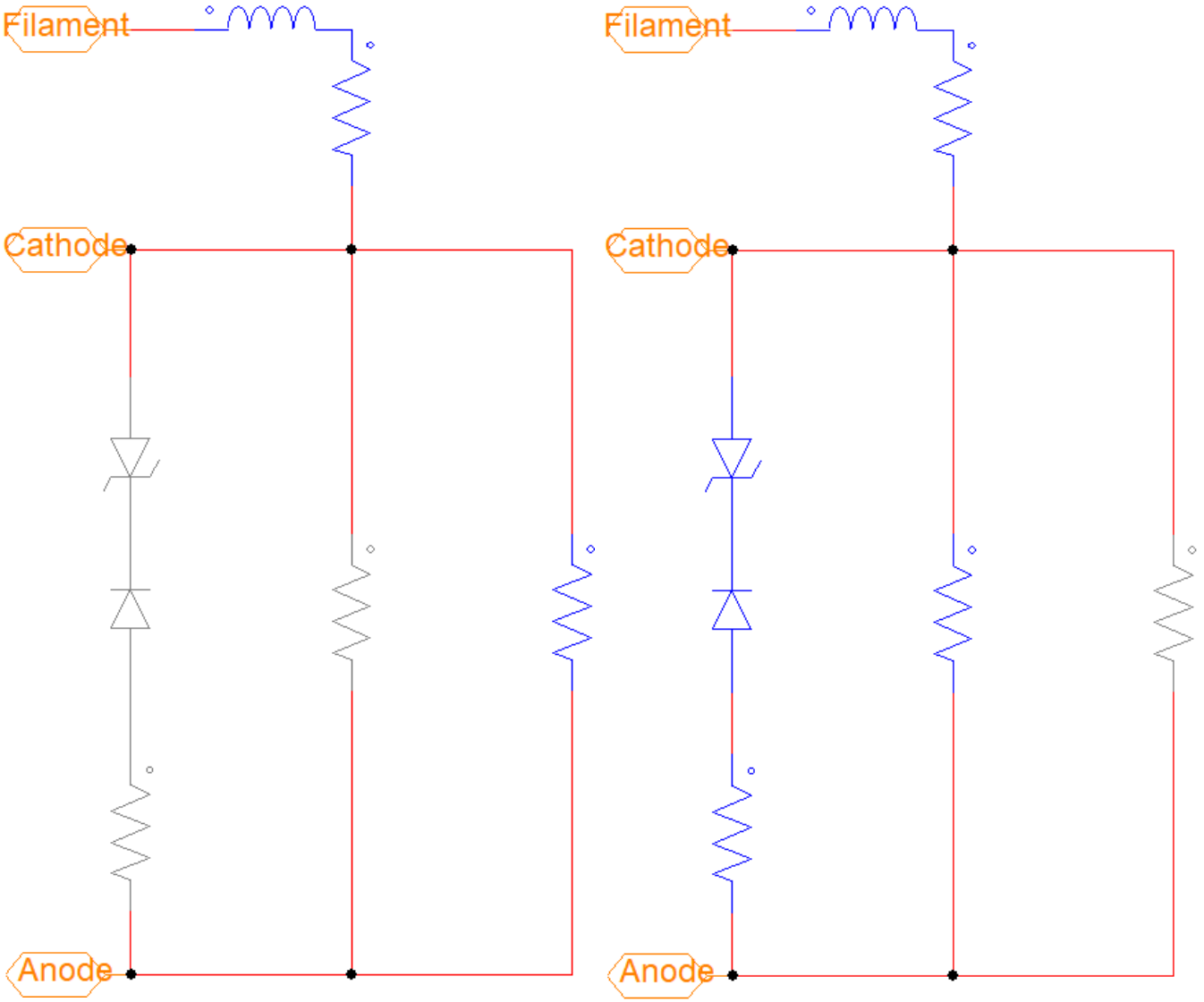


Figure A-3: Magnetron PSIM Schematic (a) Testcase 1, fixed resistance (b) Testcase 2, voltage adjusted resistance.

b

PCB Layout

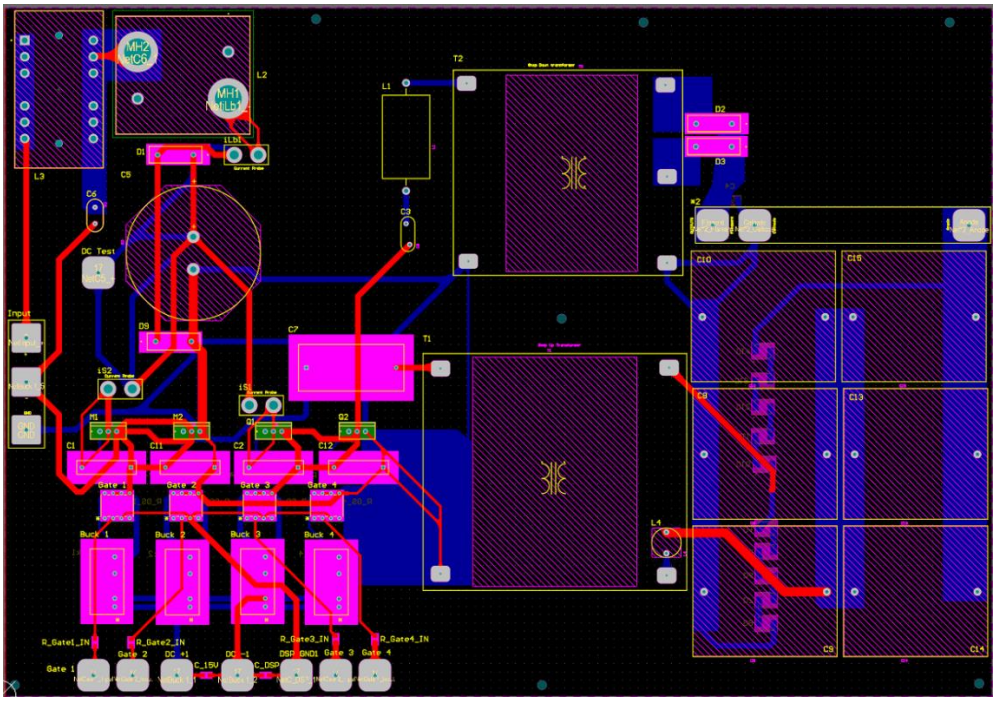


Figure A-4: PCB top layer in Altium Designer

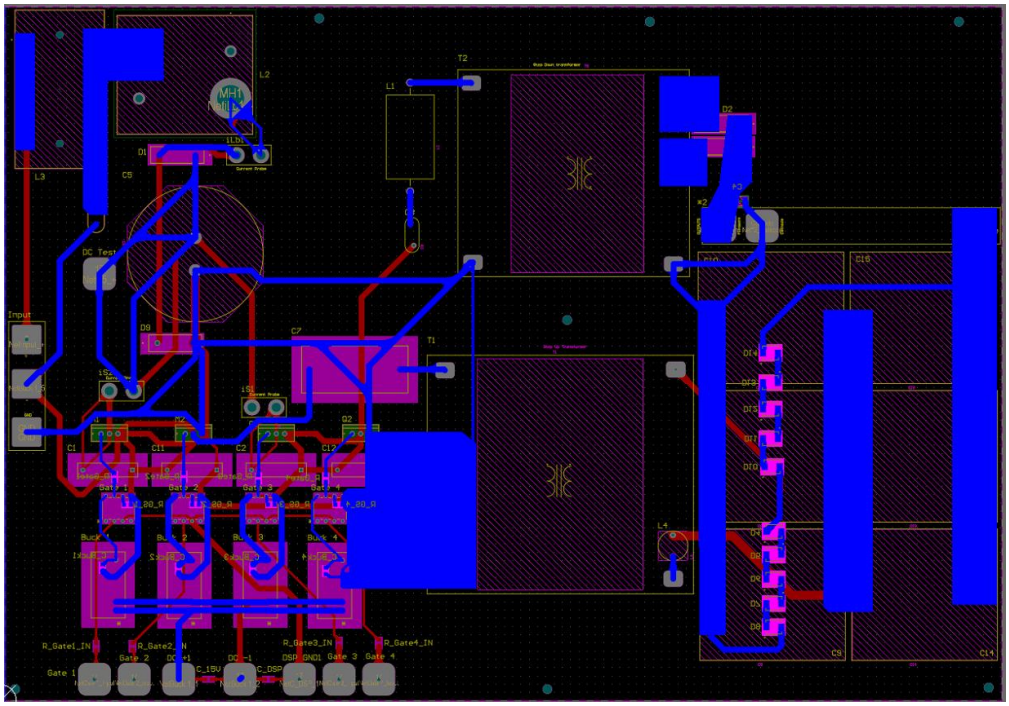


Figure A-5: PCB Bottom Layer in Altium Designer

Lab Setup

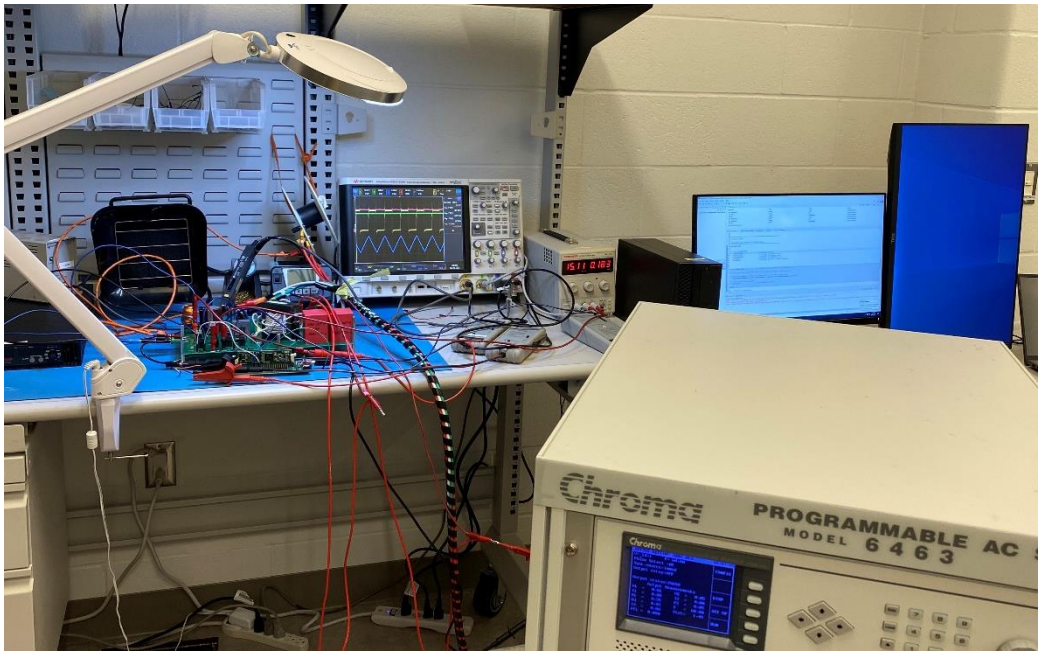


Figure A-6: Full lab setup view

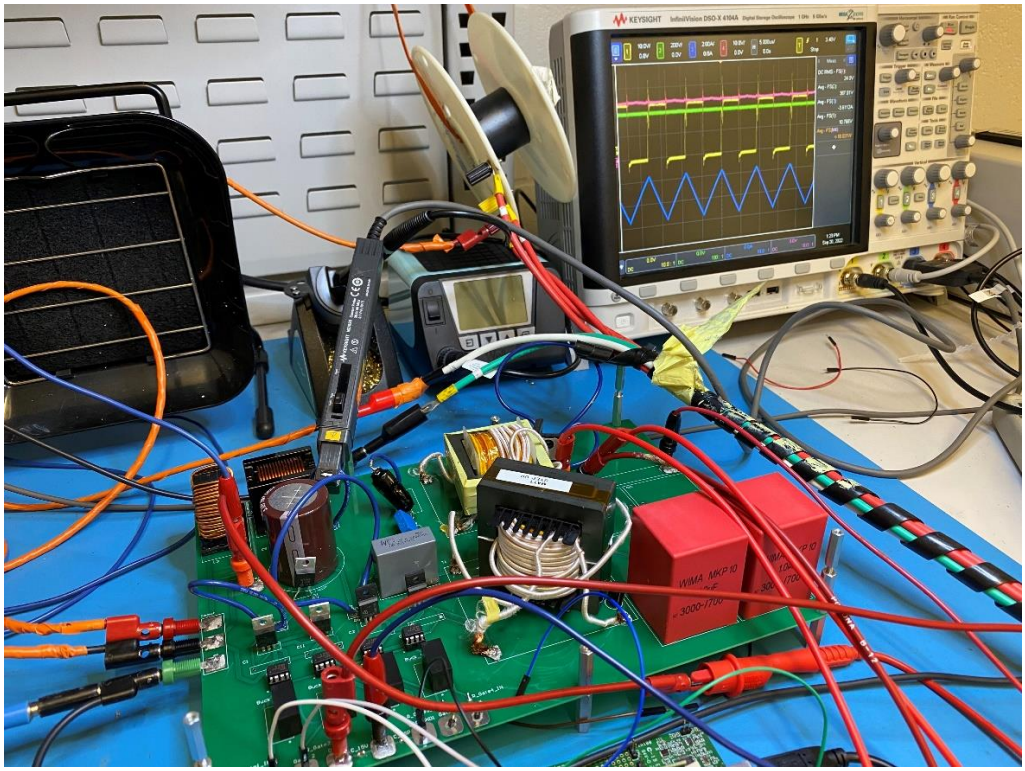


Figure A-7: PCB lab setup view

d

Math

CL Resonant Gain

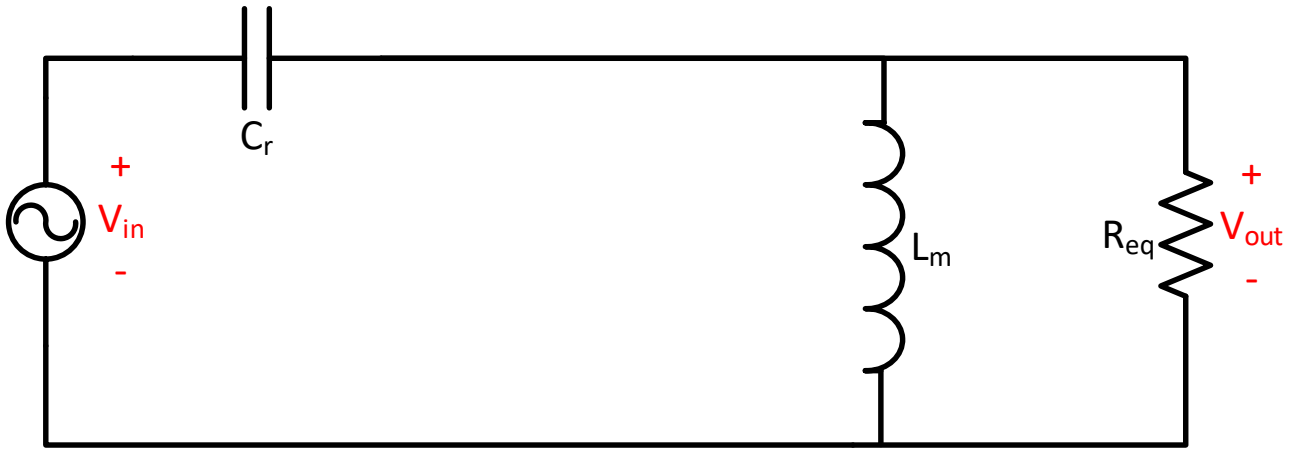


Figure A-8: CL Resonant equivalent circuit

$$\frac{V_{Out}}{V_{In}} = G = \frac{X_L \parallel R}{(X_L \parallel R) + X_C} \qquad \text{Equation 3-1}$$

$$G = \frac{\frac{X_L R}{X_L + R}}{\frac{X_L R}{X_L + R} + X_C} \qquad \text{Equation 3-2}$$

$$G = \frac{X_L R}{X_L R + X_C X_L + X_C + R} \qquad \text{Equation 3-3}$$

$$G = \frac{j\omega LR}{j\omega LR - \frac{j}{\omega C}\, j\omega L - \frac{j}{\omega C} R} \qquad \text{Equation 3-4}$$

$$G = \frac{\frac{j\omega L}{R}\frac{\omega_o}{\omega_o}}{\frac{j\omega L}{R}\frac{\omega_o}{\omega_o} + \frac{L}{CR^2}\frac{\omega_o}{\omega_o} - \frac{j}{\omega CR}\frac{\omega_o}{\omega_o}}$$

Equation 3-5

$$Q = \frac{R}{\omega_o L} = \omega_o CR$$

Equation 3-6

$$\omega_r = \frac{\omega}{\omega_o}$$

Equation 3-7

$$G = \frac{\frac{j\omega_r}{Q}}{\frac{j\omega_r}{Q} + \frac{1}{Q^2} - \frac{j}{\omega_r Q}}$$

Equation 3-8

$$G = \frac{j}{j + \frac{1}{Q\omega_r} - \frac{j}{\omega_r^2}}$$

Equation 3-9

$$|G| = \frac{1}{\sqrt{(1 - \frac{1}{\omega_r^2})^2 + (\frac{1}{Q\omega_r})^2}}$$

Equation 3-10

f

LLC Resonant Gain

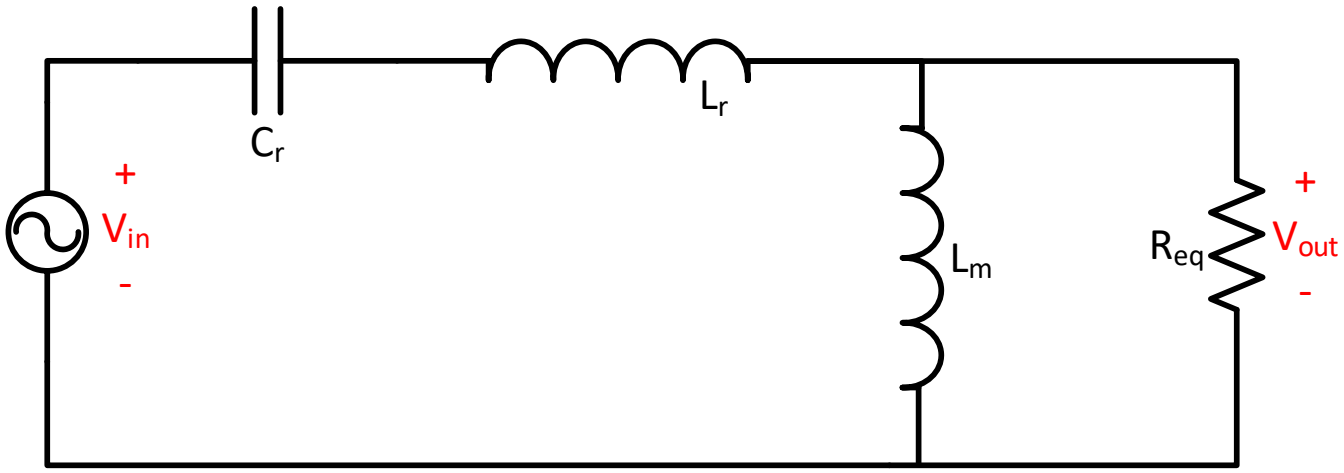


Figure A-9: LLC Resonant equivalent circuit

$$G = \frac{\frac{j\omega L_m R}{j\omega L_m + R}}{\frac{j\omega L_m R}{j\omega L_m + R} + j\omega L_r - \frac{j}{\omega C}}$$ Equation 3-11

$$G = \frac{j\omega L_m R}{j\omega L_m R + j\omega L_r (j\omega L_m + R) - \frac{j(j\omega L_m + R)}{\omega C}}$$ Equation 3-12

$$G = \frac{1}{1 + \frac{L_r (j\omega L_m + R)}{L_m R} - \frac{j\omega L_m + R}{\omega^2 L_m R C}}$$ Equation 3-13

$$k = \frac{L_m}{L_r}$$ Equation 3-14

$$\omega_o = \frac{1}{\sqrt{L_r C_r}}$$ Equation 3-15

$$Q = \frac{\sqrt{L_r}}{R\sqrt{C_r}} = \frac{1}{\omega_o C_r R} = \frac{L_r \omega_o}{R}$$ Equation 3-16

$$G = \frac{1}{1 + \frac{1}{k}\frac{j\omega L_m}{R} + \frac{1}{k} - \frac{j}{\omega RC} - \frac{1}{\omega^2 L_m C}}$$ Equation 3-17

$$G = \frac{1}{1 + \frac{1}{k} - \frac{1}{\omega_r^2 k} + jQ(\omega_r - \frac{1}{\omega_r})}$$ Equation 3-18

$$|G| = \frac{1}{\sqrt{(1 + \frac{1}{k} - \frac{1}{\omega_r^2 k})^2 + (Q(\omega_r - \frac{1}{\omega_r}))^2}}$$ Equation 3-19

LLC Phase Angle

$$Z = \frac{1}{j\omega C_r} + j\omega L_r + \frac{j\omega L_m R}{j\omega L_m + R}$$ Equation 3-20

$$Z = \frac{j\omega L_m + R + j\omega L_r\, j\omega C_r (j\omega L_m + R) + j\omega C_r (j\omega L_m R)}{j\omega C_r (j\omega L_m + R)}$$ Equation 3-21

$$Z = \frac{j\omega L_m + R - j\omega^3 L_r C_r L_m - \omega^2 L_r C_r R - \omega^2 C_r L_m R}{-\omega^2 C_r L_m + j\omega C_r R}$$ Equation 3-22

$$Z = R\frac{j\omega_r kQ + 1 - j\omega_r^3 Qk - \omega_r^2 - \omega_r^2 k}{-\omega_r^2 k + j\frac{\omega_r}{Q}}$$ Equation 3-23

h

$$Z = R\frac{\frac{1}{\omega_r} - \omega_r - \omega_r k + jkQ(1-\omega_r^2)}{-\omega_r k + j\frac{1}{Q}}$$

Equation 3-24

$$Z = R\frac{\frac{-1}{\omega_r} + \omega_r + k\omega_r + j(kQ\omega_r{}^2 - kQ)}{\frac{1}{Q}(kQ\omega_r - j)} * \frac{kQ\omega_r + j}{kQ\omega_r + j}$$

Equation 3-25

$$Z = RQ\frac{-kQ + kQ\omega_r{}^2 + k^2Q\omega_r{}^2 + j(k^2Q^2\omega_r{}^3 - k^2Q^2\omega_r) + j(\frac{-1}{\omega_r} + \omega_r + k\omega_r) - (kQ\omega_r{}^2 - kQ)}{k^2Q^2\omega_r{}^2 + 1}$$

Equation 3-26

$$Z = RQ\frac{k^2Q\omega_r{}^2 + j(k^2Q^2\omega_r{}^3 - k^2Q^2\omega_r - \frac{1}{\omega_r} + \omega_r + k\omega_r)}{k^2Q^2\omega_r{}^2 + 1}$$

Equation 3-27S

$$\angle Z = \arctan(\frac{k^2Q^2\omega_r^3 - k^2Q^2\omega_r - \frac{1}{\omega_r} + \omega_r + k\omega_r}{k^2Q\omega_r^2})$$

Equation 3-28

R_{eq} Center Tapped Transformer Full Wave Rectifier Output

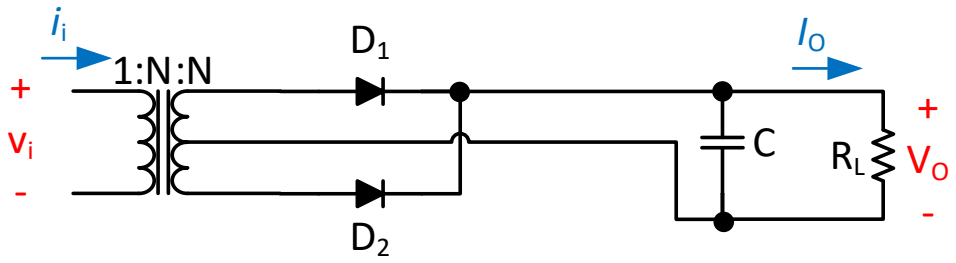


Figure A-10: Center tapped transformer full wave rectifier output stage for equivalent resistance calculations

$$i_i = i_{pk}\sin(\omega t) \qquad \text{Equation 3-29}$$

$$I_O = \frac{1}{\pi}\int_0^{\pi} N i_{pk}\sin(\omega t)d(\omega t) \qquad \text{Equation 3-30}$$

$$i_{pk} = \frac{\pi}{2} I_O N \qquad \text{Equation 3-31}$$

$$i_i = \frac{\pi}{2} I_O N \sin(\omega t) \qquad \text{Equation 3-32}$$

$$v_{i1} = \frac{4v_{pk}}{\pi}\sin(\omega t) \qquad \text{Equation 3-33}$$

$$v_{pk} = \frac{V_O}{N} \qquad \text{Equation 3-34}$$

$$v_{i1} = \frac{4V_O}{\pi N}\sin(\omega t) \qquad \text{Equation 3-35}$$

$$R_{eq\_LLC} = \frac{v_{i1}}{i_i} = \frac{(\frac{4V_O}{\pi N})\sin(\omega t)}{(\frac{\pi N I_O}{2})\sin(\omega t)} = \frac{8}{\pi^2 N^2}\frac{V_O}{I_O} = \frac{8R_L}{\pi^2 N^2}$$ Equation 3-36

R_{eq} Voltage Doubler Output

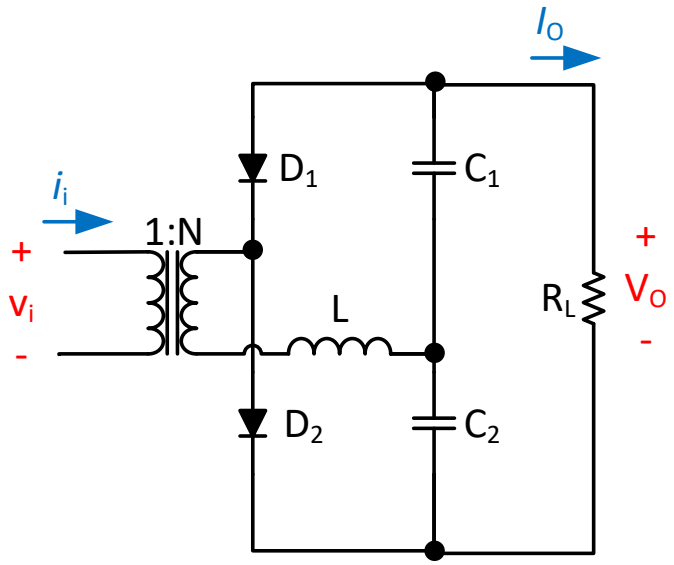


Figure A-11: Voltage doubler output stage for equivalent resistance calculations

$$i_i = i_{pk}\sin(\omega t)$$ Equation 3-37

$$I_O = \frac{1}{2\pi}(\int_0^{\pi} i_{pk}\sin(\omega t)d(\omega t) + \int_{\pi}^{2\pi} i_{pk}\sin(\omega t)d(\omega t))$$ Equation 3-38

$$I_O = \frac{2i_{pk}}{N2\pi} = \frac{i_{pk}}{N\pi}$$ Equation 3-39

$$i_i = N\pi I_O \sin(\omega t)$$ Equation 3-40

$$v_{i1} = \frac{4v_{pk}}{\pi}\sin(\omega t)$$ Equation 3-41

k

$$2v_{pk}N = V_O \qquad \text{Equation 3-42}$$

$$v_{i1} = \frac{4(\frac{V_O}{2})}{N\pi}\sin(\omega t) = \frac{2V_O}{N\pi}\sin(\omega t) \qquad \text{Equation 3-43}$$

$$R_{eq\_CL} = \frac{v_{i1}}{i_i} = \frac{(\frac{2V_O}{N\pi})\sin(\omega t)}{(N\pi I_O)\sin(\omega t)} = \frac{2}{N^2\pi^2}\frac{V_O}{I_O} = \frac{2R_L}{N^2\pi^2} \qquad \text{Equation 3-44}$$

Additional Considerations

Transformers

Wires

The wires used for winding around the transformer core should be chosen based on multiple considerations. The first consideration is the frequency that will be used, as at high frequency the skin effect will cause electrons to travel on the surface of the wire instead of through the entire conductor. As such, litz wire or other stranded type wires should be used at higher frequencies as well as being easier to wind due to better flexibility of wires. Next is the gauge of the wire, which will determine how much current the wire will be able to conduct. This is due to thicker wires, or lower gauge numbers, having a lower resistance resulting in fewer conduction losses which will result in heat. As the transformer will step-up/down the current, the primary and secondary do not require the same wire gauge. The third major consideration is the available space. With higher gauge wires, less loops can be made around the core before the diameter of the windings becomes too large to fit within the core.

Core

Selection of the transformer core is important to ensure that the transformer will not saturate under the expected operating conditions. Equation 3-45 is an equation that should be considered to ensure the core does not saturate with B_{max} being the max flux density, V_{rms} being the applied RMS voltage to the transformer, f being the frequency of the voltage, N being the number of turns on the side V_{rms} is applied, and A being the cross-sectional area of the core. Based on this equation we can increase the voltage by any combination of increasing the frequency, turns, core effective area, or core material for the flux density.

$$B_{max} = \frac{V_{rms}}{4.44\,fNA} \text{ [T]} \qquad \text{Equation 3-45}$$

m

Capacitors

The following figure, Figure A-12, was used to assist in determining the capacitor type that should be used as specific points in the design. For hardware testing, the primary capacitor types used are ceramic capacitors, aluminum electrolytic capacitors, and film capacitors. The ceramic capacitors were used primarily for the low voltage and low capacitance portions of the gate driver circuitry, as these types of capacitors offered extremely small footprints allowing for better bypass capacitor placements on the board. The aluminum electrolytic capacitor was used for the DC link capacitor, as it provided a high capacitance for the component size as well as meeting the moderate voltage requirement. For the resonant capacitors, film capacitors were used for their high voltage rating and low capacitance options. For the high voltage output film capacitors were again used due to the high voltage, 3kV, options for slightly higher capacitances.

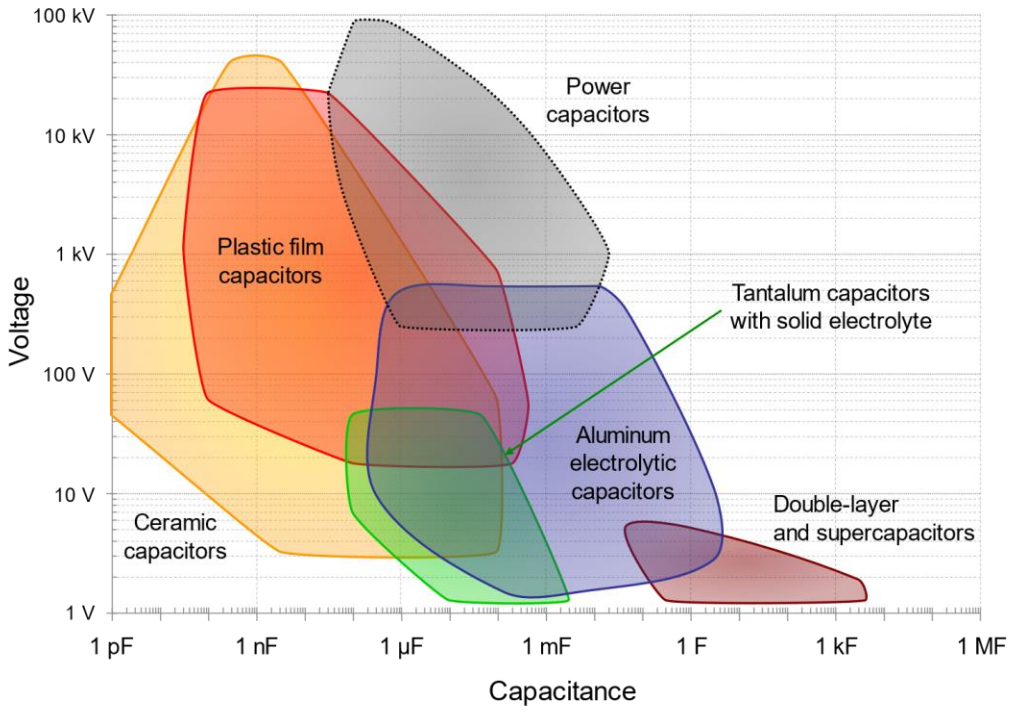


Figure A-12: Capacitor type capacitance to voltage [28]

n