A SOFT SWITCHED, SINGLE-SWITCH ELECTROLYTIC CAPACITOR-LESS STEP-UP CONVERTER FOR PHOTOVOLTAIC ENERGY APPLICATION

KAJANAN KANATHIPAN

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ABSTRACT

Due to the harmful effects and limited quantity of fossil fuels, countries have been moving towards the use of renewable energy systems. In particular, solar energy has been seeing a rapid and increased growth year on year. In a solar energy conversion power architecture, a common DC grid is used to facilitate efficient high voltage power conversion. Since the output voltage of a typical solar panel is much lower than the grid level, a power electronic converter is employed to step-up the panel's output voltage as well as to convert the captured solar energy into useable electrical energy. Solar energy is intermittent in nature. It is known that for each solar irradiation level, there exists one operating point, called the maximum power point (MPP) at which the maximal amount of solar energy can be extracted from the system. This operating point can be determined through the use of control based algorithms integrated with a power electronic converter. Existing step-up power electronic converters reported in literature for solar energy power conversion either require multiple power switches, suffer from some switching power losses in some operating conditions, or require the use of additional auxiliary circuitry to achieve step-up voltage conversion.

In this thesis, a single switch, electrolytic capacitor-less quasi-resonant step-up DC/DC converter is proposed for solar energy applications. The proposed converter is an improved coupled-magnetic based topology that requires only a single switch. By operating the input inductor of the proposed converter in continuous conduction mode (CCM) the required input capacitance is reduced and hence, this allows for a small sized film capacitor to be used. In addition, the proposed circuit is able to achieve a large step-up gain while minimizing the ratio between the peak switch voltage and the circuit output voltage. Two different modes of operation are presented and discussed for the proposed circuit which can achieve a very large gain and a very

small peak switch voltage to circuit output voltage ratio simultaneously. A maximum power point tracking controller is also developed to work with the proposed step-up DC/DC converter through the use of variable frequency control scheme. Simulation and experimental results on a proof-of-concept, 35V/380V, 100W, 100kHz, hardware prototype are provided for both modes of operation for fixed and varying light intensities to highlight the merits and performance of the proposed converter.

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NOMENCLATURE

C_r	Resonant capacitor
C_p	Snubber capacitor
D	Duty cycle
f_s	Resonant frequency
i_{D1}	Diode current
i_i	Input current
i_{in}	Input capacitor current
i_{Lr}	Resonant inductor current
i_{mpp}	Current at the maximum power po int
i_{sc}	Short circuit current
i_{sw}	Switch current
L_{in}	Input inductor
L_l	Leakage inductance
L_m	Magnetizing inductance
L_p	Primary winding inductance
L_r	Resonant inductance
L_s	Secondary winding inductance
L_t	Tertiary winding inductance
v_{D1}	Diode voltage
v_{ds}	Switch voltage
v_{ds_max}	Maximum switch voltage
v_{gs}	Switch gate voltage
v_i	Input voltage
v_{Lin}	Input inductor voltage
v_{Lr}	Resonant inductor voltage

v_{mpp}	Voltage at the maximum power point
v_o	Output voltage
v_{oc}	Open circuit voltage
v_{pri}	Primary winding voltage
v_{sec}	Secondary winding voltage
v_{tri}	Tertiary winding voltage
Z	Characteristic impedance
ω_0	Operation frequency
AC	Alternating current
ADC	Analog to digital converter
CCM	Continuous conduction mode
DC	Direct current
DCM	Discontinuous conduction mode
GPIO	General purpose input output
ISSBC	Interleaved soft-switched based converter
KCL	Kirchoff's Current Law
KVL	Kirchoff's Voltage Law
MOSFET	Metal oxide semiconductor field effect transistor
MPPT	Maximum Power Point Tracking
NB	Negative big
NS	Negative small
P&O	Perturb and Observe
PB	Positive big
PS	Positive small
PSIM	Power Sim

SSSBC	Single switch soft-switched based converter
ZCS	Zero-current switching
ZE	Zero
ZVS	Zero-voltage switching

1. Introduction

1.1 Solar Energy Systems

Currently 79.5% of the total yearly energy consumption is provided through the use of non-renewable energy sources such as fossil fuels [1]. In 2015, there was over 9 gigatonnes (gt) of global carbon emissions [2]. Fig. 1-1 shows the breakdown of total emission per country [1, 3]. The use of fossil fuels has several downsides. Fossil fuels are a major source of pollution as they contribute to the emission of greenhouse gases such as carbon dioxide and methane. In particular, global energy-related carbon dioxide emissions rose by 1.4% in 2017. Another downside is that fossil fuels are a finite resource. It is predicted that supplies would have been completely consumed by the year 2088 [4]. As a result there has been a general trend in transformation towards the use of renewable energy sources.

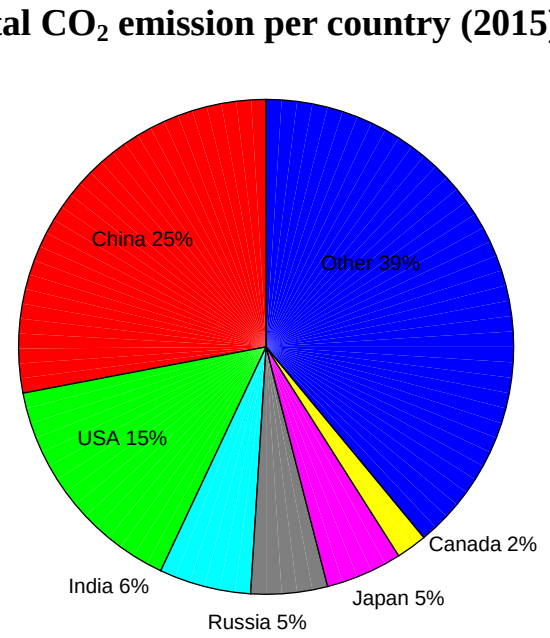


Figure 1-1: Total CO_2 emissions per country from 2015 [1, 3]

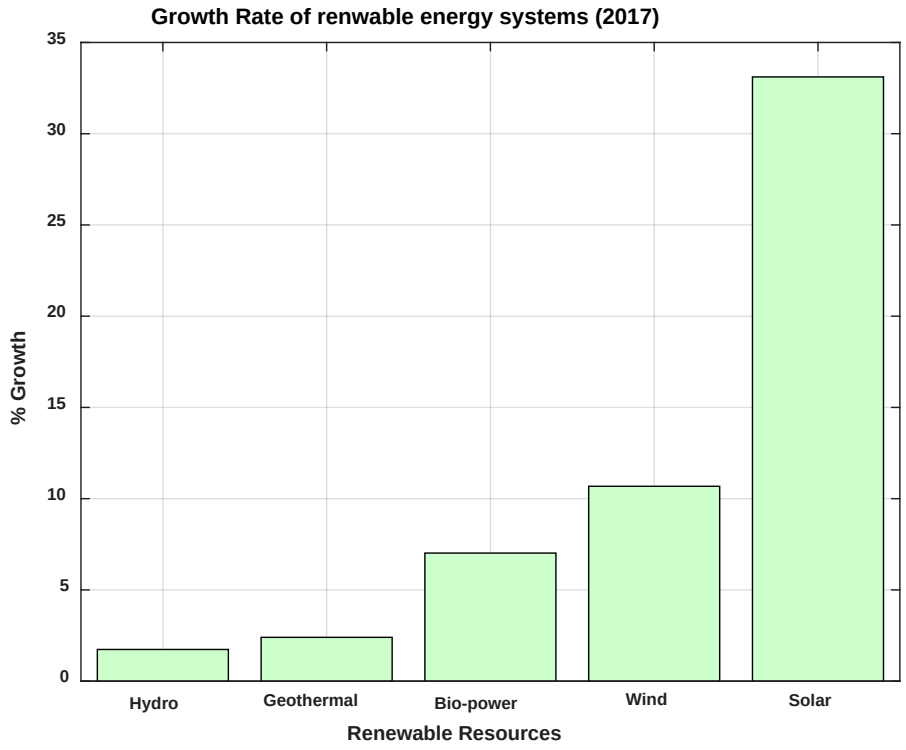


Figure 1-2: Growth rate of renewable energy capacity [5]

Renewable energy is energy that is obtained at a rate that is equal or faster than the rate at which it is consumed, including energy generated from a source that is inexhaustible. These include sources such as solar, wind, geothermal, and hydro-power. These sources are infinite in use however the amount of energy that can be obtained is usually limited per unit of time. For example solar energy can only be obtained while sunlight is present and wind energy can only be obtained when wind is present.

Solar energy is one of the most promising renewable energy sources due to the simplicity and the advancement in their field. Fig. 1-2 shows the growth rate of various renewable energy systems in 2017. It can be seen that the solar energy had the highest growth rate which increased by over 33%. In 2017, the total renewable power generation capacity increased by an estimated 178GW with solar energy accounting for nearly 55% of this increase [5]. The total global capacity of

solar energy has increased from 6.01GW to 402GW from 2006 to 2017 [5] and is predicted to have increased by an additional 575GW by 2023 [6].

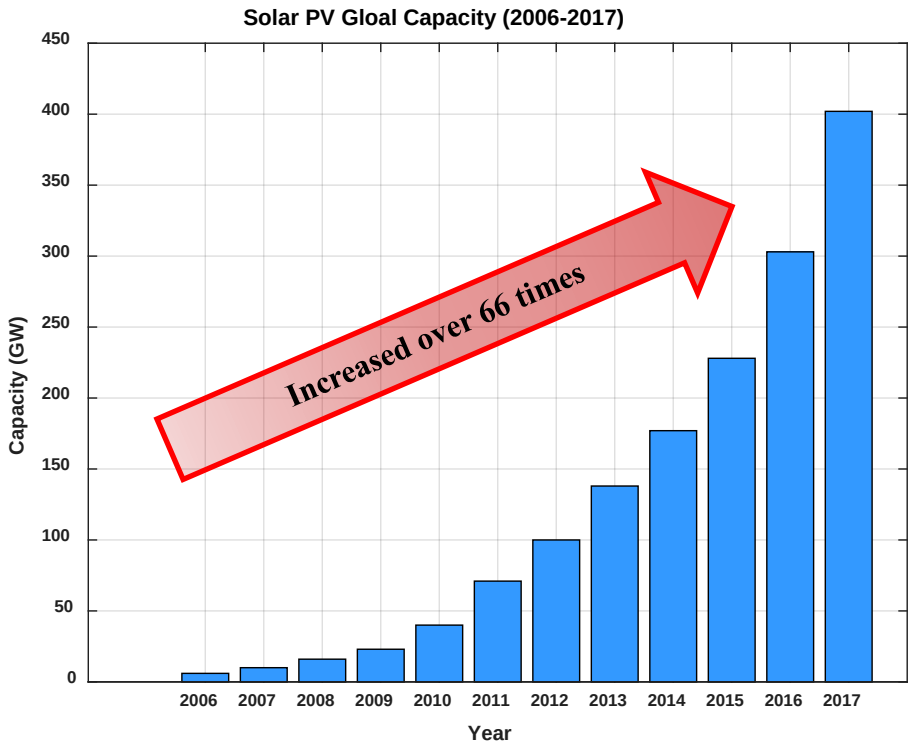


Figure 1-3: Solar PV global capacity from 2006 to 2015 [4]

In Canada, 17% of our energy is provided through renewable energy. Most of this generated renewable energy is provided through hydro-power; however, the generated solar energy has been on the rise. The installed capacity of solar power in Canada has increased from 16.7MW to 2911MW from 2005 to 2017[7]. In Ontario, it is estimated that each hour 320 tonnes of CO_2 avoided each hour through the use of solar energy and the amount is projected to continue to increase [8].

1.2 Power Conversion for Solar Energy Systems

The energy captured by a solar system cannot be immediately used by the load and has to be converted into electrical energy. This is accomplished through the use of a power electronic converter which converts the solar energy to electrical energy which is then provided to the load or grid. The output voltage of a typical solar panel ranges from 12V to 40V while the typical grid voltage level is 380V [9-11]. Since the output voltage is much lower than the grid level, the power electronic converter also utilized to step-up the panel output voltage such that it matches the grid. Fig. 1-4 shows an example of a PV array system connected to power electronic converters. A power electronic converter consists of active components such as switches and diodes and passive components such as inductors and capacitors. Different configurations of these components allow for the assembly of circuits that could carry out the required performance.

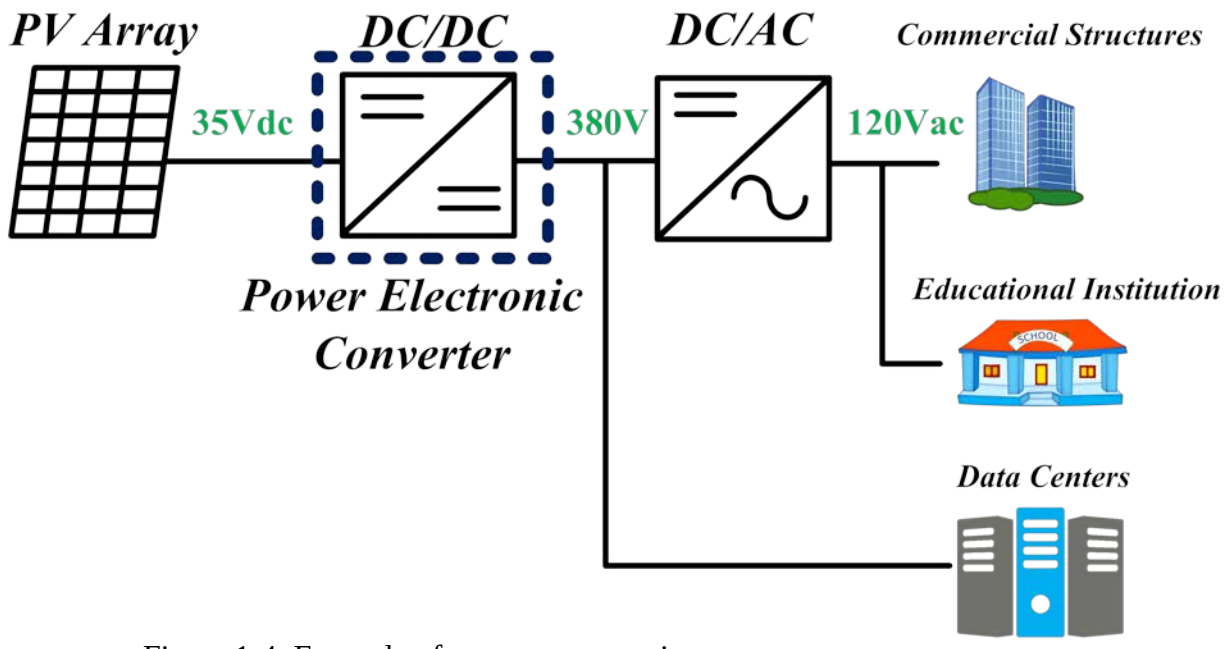


Figure 1-4: Example of a power conversion system

1.3 Power Loss in Converters

As mentioned in section 1.2, power electronic converters are utilized to convert solar energy into electrical energy as well as to step up the panel's output voltage to match the grid. These converters do not operate at 100% efficiency as there are losses during the conversion. There are two main power losses in the power conversion process: switching power loss [12] and conduction power loss [13].

An example of switching power loss is shown in fig. 1-5 which shows the switch voltage (v_s) and the switch current (i_s) waveforms as a function of time. Switching power losses occur when a device such as a metal oxide semiconductor field effect transistor (MOSFET) is transitioning from either its off state to on state or its on state to off state. During these two transition states there is an overlap in the switch voltage and current which causes power loss. This scenario is known as hard switching [12]. Power loss that results from hard switching is a function of the switch voltage, switch current, operating frequency (f_s), and the overlap time (t_{on} or t_{off}) (Eq.1-5).

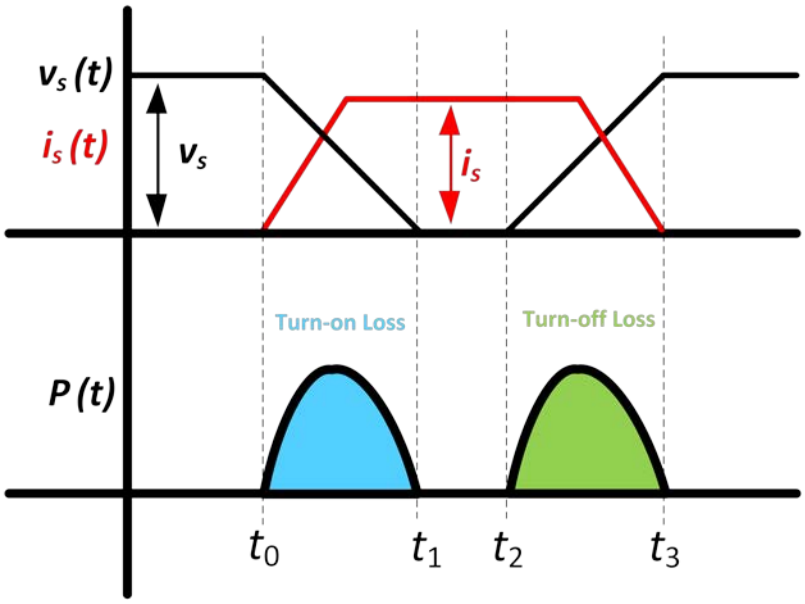


Figure 1-5: Example of switching power loss (hard switching)

$$P_{loss} = 0.5 v_s i_s f_s (t_1 - t_0) \quad \text{(Eq. 1-1)}$$

$$P_{loss} = (E_{on} - E_{off}) f_s \quad \text{(Eq. 1-2)}$$

$$P_D = I_s^{\,2} \times R_{ds_{on}} \quad \text{(Eq. 1-3)}$$

In order to eliminate hard switching a technique known as soft-switching is employed to reduce the voltage and current overlap for both the turn on and turn off transition states. This is usually implemented through the use of additional inductors and capacitors. Two ways to classify resonant converters are resonant and quasi-resonant. The main difference between them is that in resonant converters, resonance occurs throughout the entire circuit operation for a resonant converter while for a quasi-resonant converter it only occurs for a portion of the circuit operation.

During the time period in which the gate signal is applied, current flows through the switch. The switch is not ideal and has a resistance known as the on resistance (R_{dson}). This represents the resistance between the drain and the source of the circuit in which current flows through. R_{dson} varies based on the type (MOSFET, GaN) and rating (voltage, current, power) of the switch being used. This resistance contributes to the power loss of the circuit as shown in equation 1-3 where P_D is the dissipated power across the switch and I_{sw} is the RMS value of the switch current. This type of loss is known as conduction loss [13]. From equation 1-3 it can be seen that this loss is proportional to both the ON resistance of the switch and the RMS value of the switch current during the on state. As a result, this loss is proportional to the duty cycle of the switch. A larger duty ratio implies larger turn-on duration for the converters switch. If a converter operates at a high duty cycle the conduction losses will be larger which reduces the overall efficiency.

1.4 Existing Power Electronic Converters for Solar Energy Systems

Power electronic converters are essential in order to step-up a solar panels output voltage such that it matches that of the grid. Several standard power electronic converters capable of increasing or decreasing the input voltage exist. In order to improve the performance of these converters for use in specific applications many alternative converters have been discussed in literature.

1.4.1 Standard DC/DC Converter

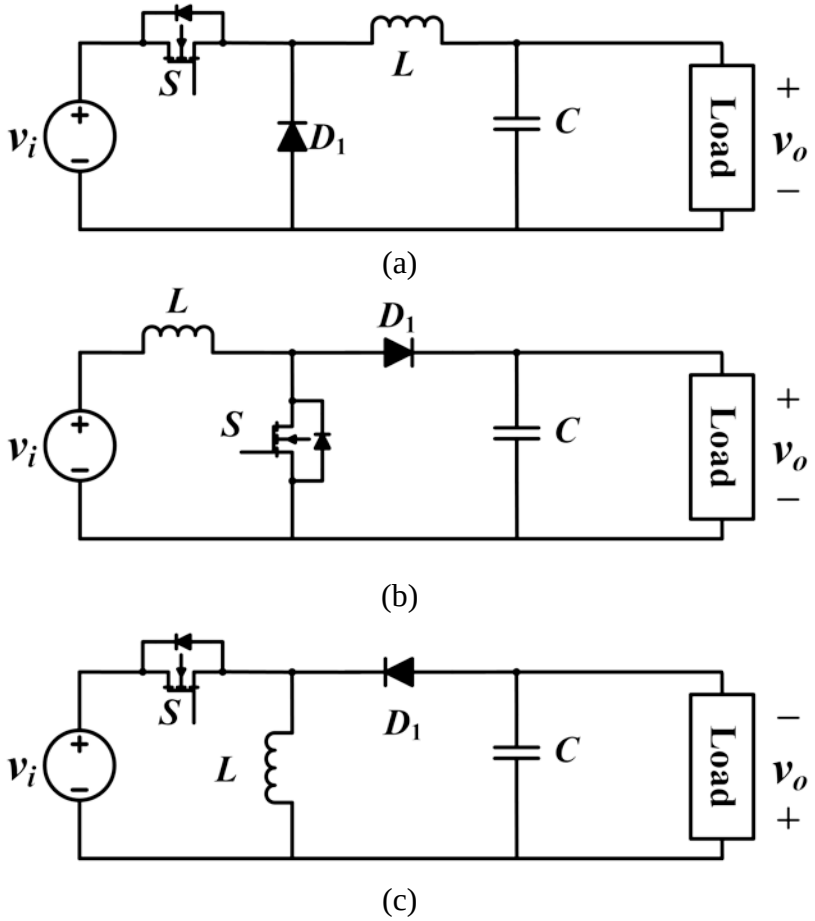


Figure 1-6: Standard DC/DC converters: (a) buck, (b) boost, (c) buck boost

Three of the basic DC/DC converters include the buck, boost, and buck-boost converters [14]. Fig. 1-6(a) shows the circuit diagram of a buck converter. This converter is capable of stepping down the input voltage which is to say the output voltage is lower than the input voltage. The converter contains an inductor, diode, capacitor and a single switch. When the switch is on, the diode is off and the input voltage is directly connected to the inductor. This allows the input current to flow through the inductor which stores energy. When the switch is turned off, the diode turns on and the inductor is now directly connected to the ground. As a result the energy stored in the inductor is transferred to the load. The gain of the converter is related to the fraction of time for which the switch is active in a given period. This time is referred to as the duty cycle (*D*) and ranges from 0 to 1. The gain of the converter is provided in equation 1-4 and from here it can be seen that the gain is equal to the duty cycle. That is to say, the higher the duty cycle the higher the gain. It can also be understood that the gain ranges from 0 to 1 and as a result this converter cannot step-up the input voltage. As a result, buck converters are mainly used in applications such as battery chargers or audio amplifiers [14-15].

$$\frac{v_o}{v_i} = D \qquad \text{(Eq. 1-4)}$$

Fig. 6(b) shows an example of a boost converter. As with the buck converter it consists of an inductor, diode, capacitor and a switch however the location of a few components are different. As the circuit steps-up the voltage the inductor must be connected to the input at all times. The inductor must be able to charge while not connected to the load and discharge when connected to the load. As a result the switch is connected between the inductor and ground while the diode is connected between the inductor and the load. The gain of the circuit is provided in equation 1-5

and is once again is proportional to the duty cycle. As the duty cycle of the converters switch increases the gain of the circuit increases. The duty cycle is located in the denominator of equation 1-5 which shows that as the duty cycle increases the denominator decreases. It can be seen that as the duty cycle approaches 1 the gain approaches positive infinity. As a result the gain of a conventional boost converter ranges from 1 to positive infinity.

$$\frac{v_o}{v_i} = \frac{1}{1-D} \qquad \text{(Eq. 1-5)}$$

Fig. 6(c) shows the circuit diagram for a buck-boost converter. As from the name, this converter is able to either step-up or step-down the input voltage based on the switch's duty cycle. The circuit diagram is similar to that of a buck converter however its inductor and diode have swapped places. However due to the connection of the diode the current flows in the opposite direction to the load and as a result the voltage polarity of the load is reversed as can be seen in fig. 6(c) The gain of this converter is shown in equation 1-6 and it can be seen that both the numerator and denominator contain the duty cycle. When the duty cycle is less than 0.5 the gain is less than 1 (buck operation) and when the duty cycle is greater than 0.5 the gain is greater than 1 (boost operation).

$$\frac{v_o}{v_i} = \frac{D}{1-D} \qquad \text{(Eq. 1-6)}$$

The gain of all three converters is a function of their switches duty cycle. Fig. 1-7 shows a graph showing this relation with the blue, red and gold waveforms representing the gain of a buck, boost, and buck-boost converter respectively for a duty cycle range of 0 to 90%. From here it can

be seen that the gain of a buck converter ranges from 0 to 1 and as a result is unable to step up the input voltage. Both the buck and buck-boost converters have a gain larger than 1 however the buck-boost can achieve a gain less than 1 when operating at a duty cycle less than 50%. Although both these converters can achieve a large gain they must operate at a high duty cycle. For example if a solar panel has an output voltage of 35V which needs to increase to 380V the converters would have to operate at a duty cycle of above 90%. As previously mentioned, operating at a high duty cycle results in larger conduction losses. Another downside to operating at a large duty cycle is that it results in a narrow turn off period for the switch which increases switching losses and current ripple [16].

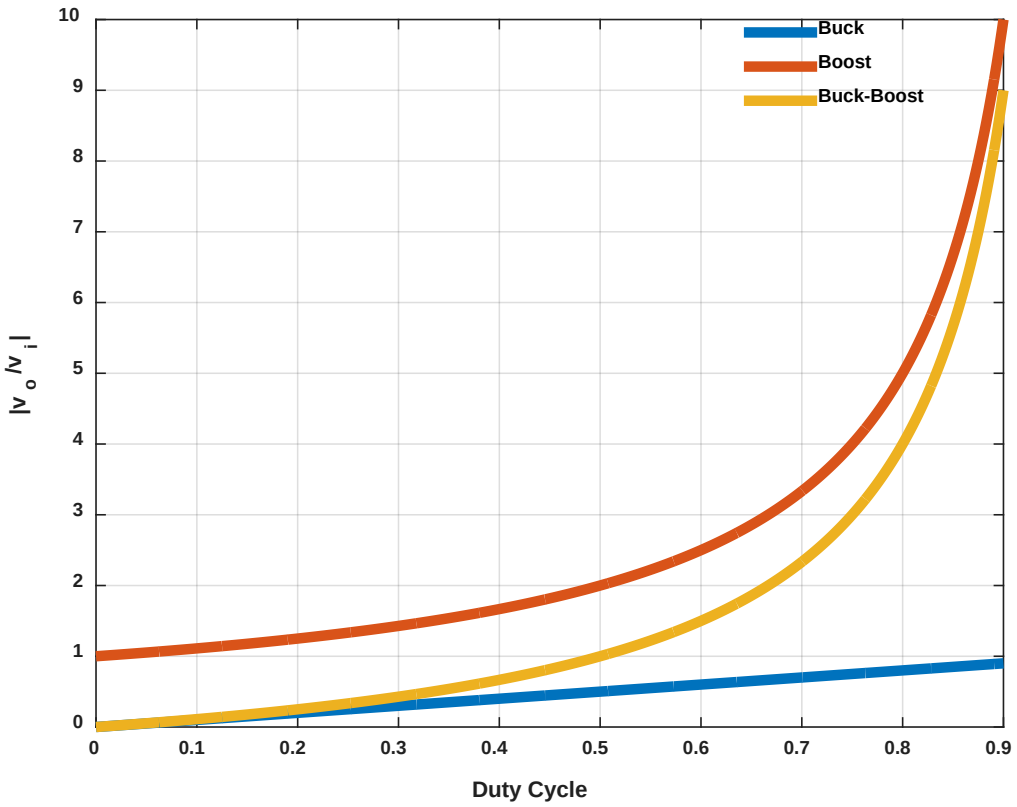


Figure 1-7: Gain as a function of duty cycle for Buck, Boost, and Buck-Boost converters

1.4.2 Step-up Converters Discussed in literature

In order to step-up the output voltage of a solar panel to match that of the grid the gain of the power electronic converter must be greater than 1. As a result the buck type converter cannot be used and instead the boost and buck-boost type circuits are employed. However, in order to achieve a high gain these power converters employ the use of a large duty cycle which can increase conduction losses. Besides these standard DC/DC boost converter topology, several alternative step-up converter topologies that utilize different circuit configurations to achieve a high gain have been reported in literature [16-21].

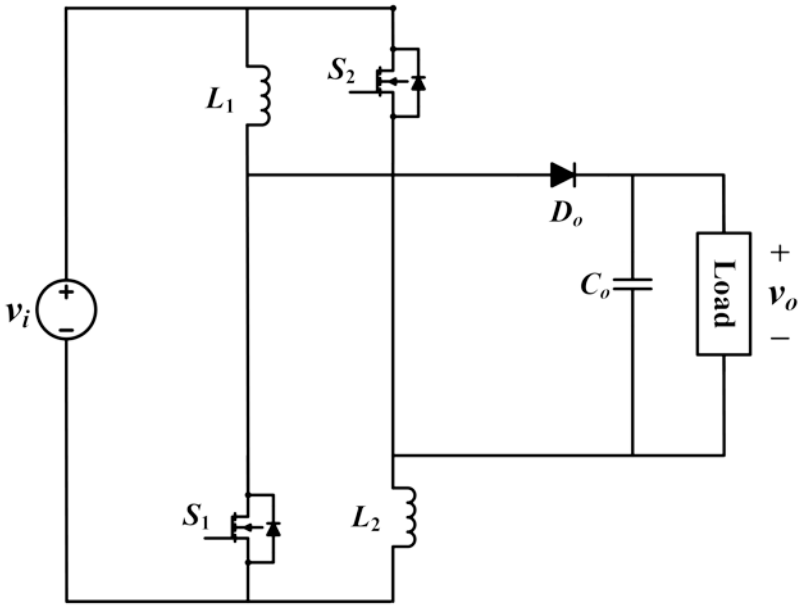


Figure 1-8: Transformer-less high step-up DC/DC Converter discussed in [17]

Fig. 1-8 shows an example of a step up DC/DC converter discussed in literature. This circuit consists of two inductors and two switches as well as an output diode and capacitor. Both switches are controlled by the same signal, which is to say they operate at the same frequency and duty cycle. The circuit has two modes of operation which are when the switches are on and

when the switches are off. During the time the switches are on, the output diode is off and the load is supplied by the capacitor. When the switches are off, the input current flows towards the output through the inductors and diode. The gain of the circuit is provided in equation 1-7 [17].

$$M = \frac{v_o}{v_i} = \frac{1+D}{1-D} \quad \text{(Eq. 1-7)}$$

$$v_{sw_{pk}} = \frac{v_o + v_i}{2} \quad \text{(Eq. 1-8)}$$

$$v_{sw_{pk}} = v_o \quad \text{(Eq. 1-9)}$$

$$v_{D_{pk}} = v_o + v_i \quad \text{(Eq. 1-10)}$$

$$v_{D_{pk}} = v_o \quad \text{(Eq. 1-11)}$$

One benefit of this circuit is the maximum voltage stress across each switch (equation 1-8) is less than the conventional boost converter (equation 1-9) which allows for lower rated switches to be used in the circuit. However, the maximum voltage stress across the diode (equation 1-10) is larger than the conventional boost converter (equation 1-11) which results in the need of a larger voltage rating for the diode. Although the gain equation of this circuit is greater than conventional boost converter it suffers from the same issue regarding the duty cycle. For example in order to achieve a gain of 11 the circuit must operate at a duty cycle of 83%. This high duty cycle implies there will be high conduction losses. The addition of a second switch implies that a second gate driver circuit is required which increases the size of the system.

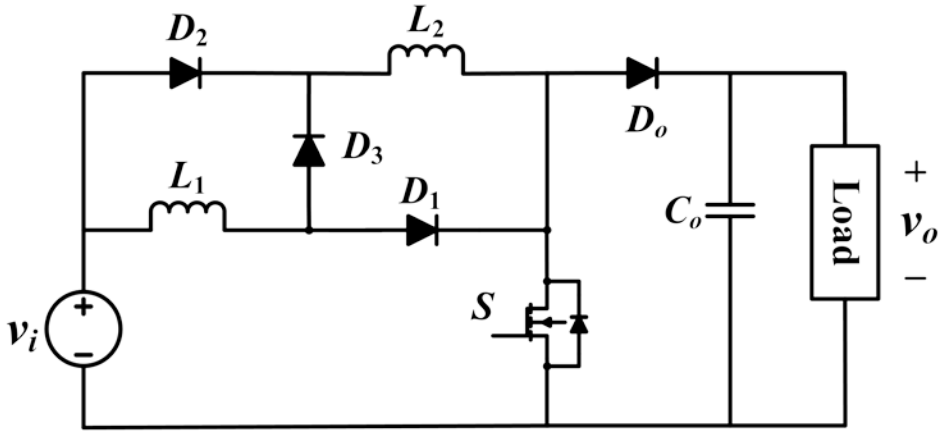


Figure 1-9: Transformer-less high step-up DC/DC Converter discussed in [18]

Fig. 1-9 shows an example of another transformer-less high step up DC/DC converter. This circuit is similar that to the conventional boost converter shown in fig 1-6(b) with the addition of three diodes and an inductor. These components create what is called a switch inductor structure. When the switch is on, diode D_3 and D_o are off and the two inductors are charged in parallel by the input current. When the switch is off, diodes D_1 and D_2 are off and the inductors discharge in series. Equation 1-12 contains the gain of this converter which can be seen to be $(1 + D)$ times larger than the conventional boost converter [18]. This converter achieves the same gain as the circuit in fig. 1-8.

$$M = \frac{v_o}{v_i} = \frac{1+D}{1-D} \qquad \text{(Eq. 1-12)}$$

This converter still suffers from similar issues to the conventional converters as well as the previously discussed transformer-less circuit. As the duty cycle ranges from 0 to 1, this converter's gain can only reach 2 times greater than the conventional converter. To step up a solar panel's output voltage from 35V to 380V this converter would need to operate at a duty

cycle of 83%. The peak switch voltage and output diode voltage stress are provided in equations (1-13) and (1-14) respectively and can be seen to be equal to the conventional boost converter. In the case of the three additional diodes their peak voltage stress are a function of the input voltage and as a result are quite low (equation 1-15 to 1-17) [18].

$$v_{sw\_pk} = v_o \quad \text{(Eq. 1-13)}$$

$$v_{D_{o\_pk}} = v_o \quad \text{(Eq. 1-14)}$$

$$v_{D_{1\_pk}} = \frac{v_i}{2} \quad \text{(Eq. 1-15)}$$

$$v_{D_{2\_pk}} = \frac{v_i}{2} \quad \text{(Eq. 1-16)}$$

$$v_{D_{3\_pk}} = v_i \quad \text{(Eq. 1-17)}$$

Another example of a step-up DC/DC converter is shown in fig. 1-10. This circuit is a modified version of the one shown in fig. 1-8 as it contains an additional diode and capacitor. The addition of these components has an effect on the circuit operation and the gain. As with the previous case when the switches are on the output diode is off, however, now the additional diode is on which allows the new capacitor to charge. When the switch is off the energy stored in the new capacitor is provided to the load.

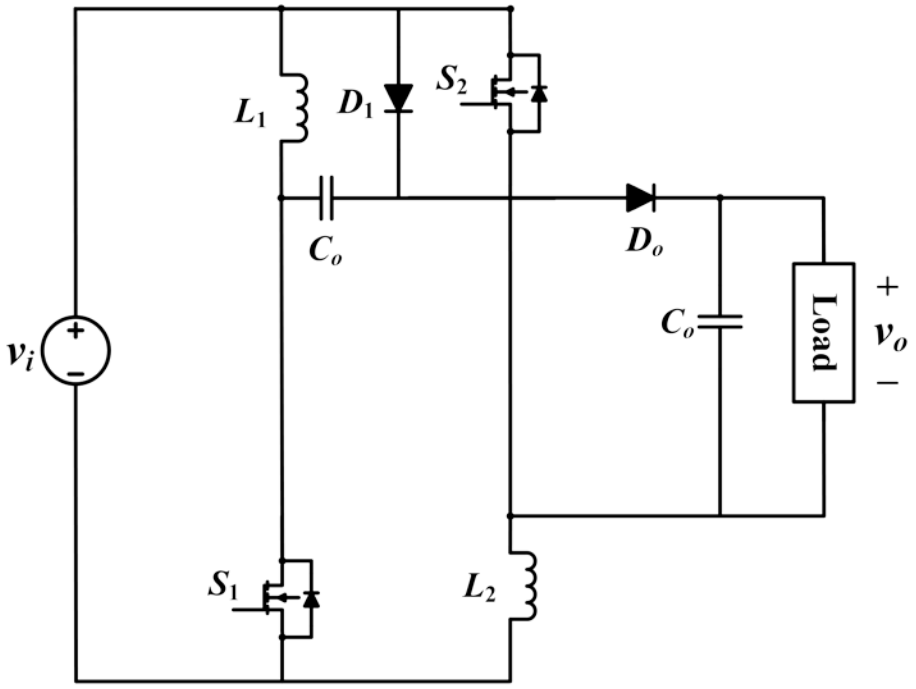


Figure 1-10: Transformer-less high step-up DC/DC Converter also discussed in [17]

$$M = \frac{v_o}{v_i} = \frac{2}{1-D} \qquad \text{(Eq. 1-18)}$$

Equation 1-18 contains the gain of the circuit. Here it can be seen that the numerator is no longer a function of the duty cycle and the gain is double that of the conventional boost converter. As a result the circuit can achieve a higher gain with a lower duty cycle. For example a duty cycle of 60% is required for a gain of 5.

In the case of operation with a solar panel, a gain of approximately 11 is required. For this the circuit would need to operate at a duty cycle of 80%. Although this is 3% lower than the two circuits shown in fig. 1-8 and 1-9 it is still quite high. From these three circuits it can be seen that there is a need for an alternative way to step-up the input voltage without operating at a high duty cycle.

1.4.3 Coupled Inductor Based Converters Discussed in Literature

In order to step-up the output voltage of a solar panel such that it can be equal to the load another technique of voltage step-up is required. Coupled-inductor based topologies in particular are an attractive solution as they can be utilized to increase the gain of the converter without the need of a large duty ratio [16, 20-29]. Figure 1-11 shows an example of a one such converter discussed in [16]. This converter is similar to that of a conventional boost converter with a few changes. An additional inductor, diode and switch have been added in parallel which creates what is known as an interleaved structure. A voltage multiplier cell containing two inductors, one capacitor, and one diode has been added to improve the gain of the circuit. Each inductor in the voltage multiplier cell is coupled to one of the inductors in the interleaved circuit. The gain of this circuit is provided in 1-19 where *D* is the duty cycle and *N* is the turn ratio of the coupled inductors.

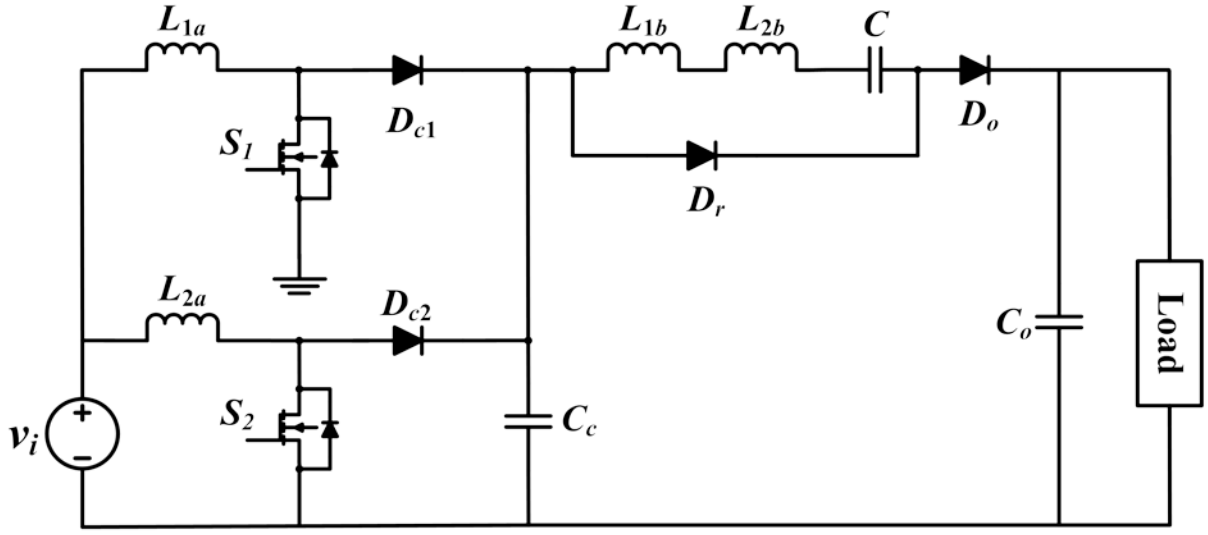


Figure 1-11: Multi-switch coupled inductor based step-up circuit discussed in [16]

$$M = \frac{v_o}{v_i} = \frac{2N+1}{1-D} \quad \text{(Eq. 1-19)}$$

It can be seen that the gain of this converter is a function of both the duty cycle and the turns ratio. By ensuring the turns ratio is greater than 1 the circuit is able to achieve a gain greater than the circuits shown in figure (1-8) to (1-10).

One issue with this circuit is the limitations imposed by the coupled inductor. As discussed in [16], in order to achieve the desired circuit operation the coupled inductor's magnetizing inductance must be 95μH. To achieve the desired magnetizing inductance without causing saturation the coupled inductor requires several turns per winding. For both coupled inductors 22 turns were chosen for both the primary and secondary windings. This results in a bulky inductor which increases the overall size of the system.

$$v_{sw_{pk}} = \frac{v_o}{2N+1} \quad \text{(Eq. 1-20)}$$

The peak switch voltage stress for both of the converters switches is provided in equation 1-20. It can be seen that this voltage is always less than the output voltage and the larger the turns ratio the smaller the value. Although the switch voltage stress across each switch is quite low the current through each of them is quite high. In [16] it is seen that the peak switch current is greater than 25A when the coupled inductor turns ratio is 1:1. If this turns ratio would increase the peak switch current would continue to increase. This will increase the overall conduction losses which decreases the circuit efficiency.

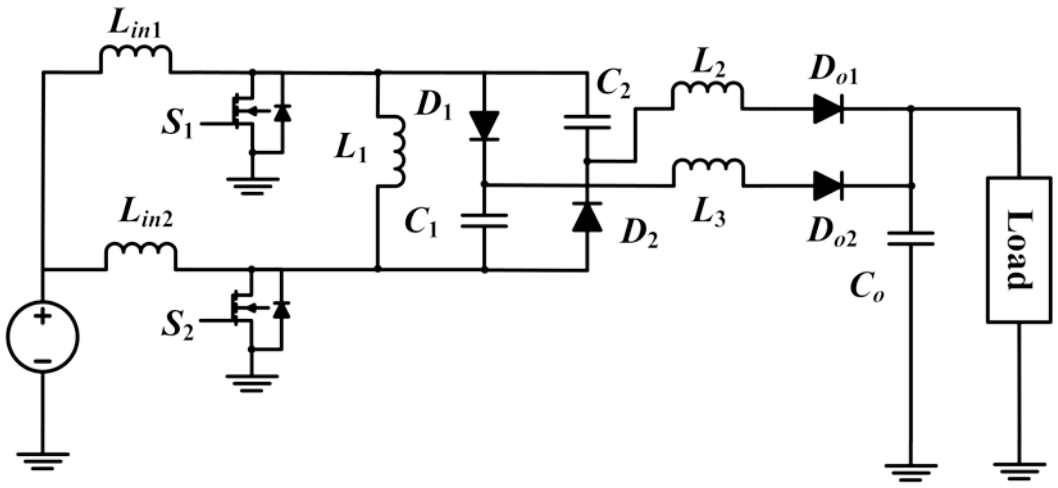


Figure 1-12: Multi-switch Coupled Inductor based step-up circuit discussed in [20]

Figure 1-12 shows another example of a high step-up coupled inductor converter designed for renewable energy systems. This circuit contains two switches, two input inductors, one three winding coupled inductor, and four diodes. The gain of this circuit is provided in equation 1-21 while the peak switch voltage and peak diode voltage are provided in 1-22 and 1-23 respectively.

$$M = \frac{v_o}{v_i} = \frac{2+N}{1-D} \quad \text{(Eq. 1-21)}$$

$$v_{sw_{pk}} = \frac{v_o}{2+N} \quad \text{(Eq. 1-22)}$$

$$v_{D_{pk}} = v_o \quad \text{(Eq. 1-23)}$$

The gain of this circuit is smaller than the previously discussed circuit for large turns ratio however this circuit has the benefit of a lower switch voltage stress. This circuit also operates under hard switching which implies lower circuit efficiency as well as a restricted operating

frequency. This in turn has an impact on the passive components such as the inductors and capacitors as a lower operating frequency results in the use of larger components.

The previously discussed converters shown in fig 1-11 and 1-12 consisted of multiple switches and diodes. The benefit of multiple switches is that the voltage stress is across each low however, it implies the need for additional gate driver circuits. Multiple switches also require additional resonant circuit for each switch. The converters discussed so far do not employ resonant circuits and as a result operate under hard switching. In order to remove the need for additional gate drivers and resonant circuits there are coupled inductor based circuits that consists of a single switch.

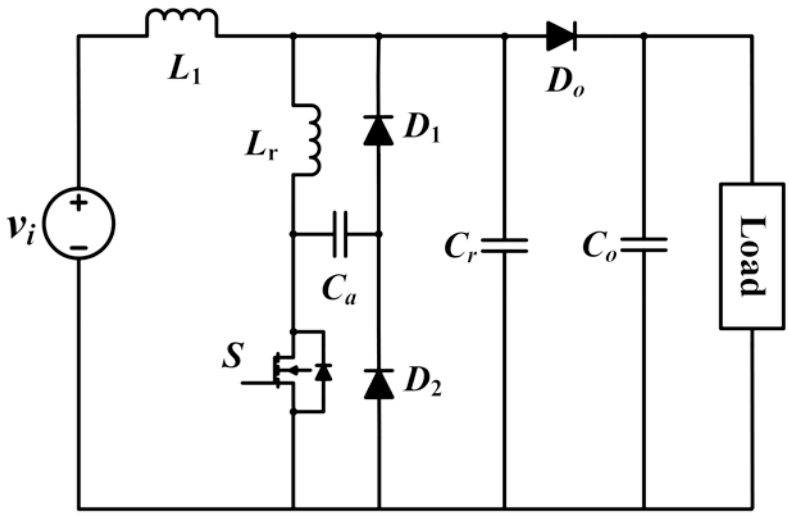


Figure1-13: SSSBC [29]

Fig. 1-13 shows an example of a single switch soft switched based step-up circuit (SSSBC) for photovoltaic systems discussed in [29]. This circuit consists of an input inductor, resonant inductor, resonant capacitor, three diodes, an auxiliary capacitor, output capacitor and a switch. Compared to the conventional boost converter, an additional three components were added. The

circuit also contains a resonant circuit which is composed of the resonant inductor and capacitor. This circuit can also be modified to obtain an interleaved version (ISSBC) as seen in fig 1-14. The gain of this circuit is not provided, however a graph containing the peak switch voltage to output voltage ratio is provided. Their results are summarized in table 1-1.

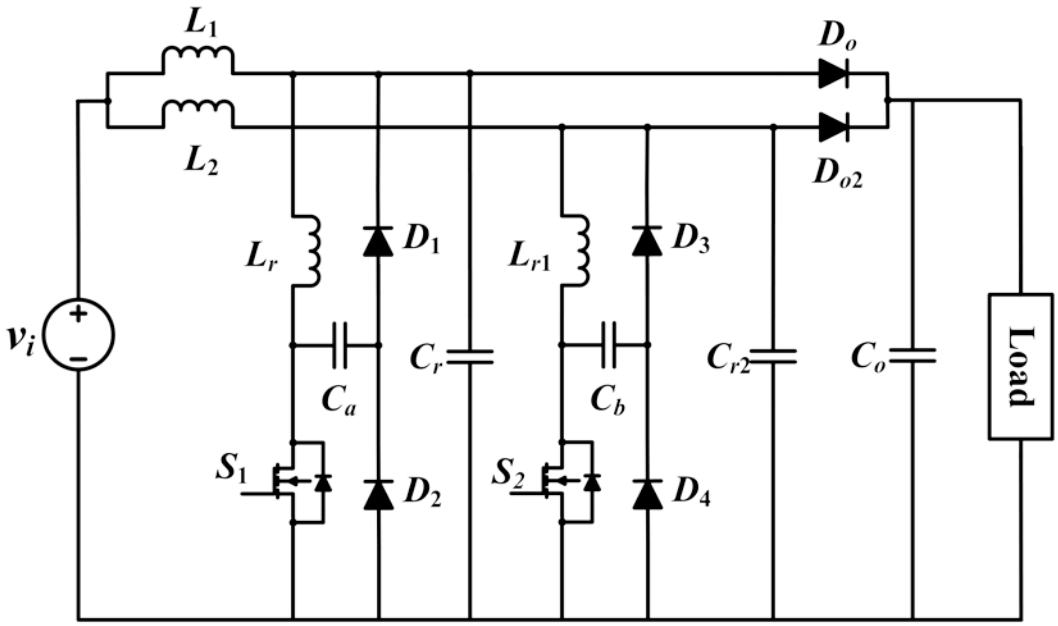


Figure 1-14: ISSBC [29]

Table 1-1: Maximum switch voltage to output voltage ratio at different duty cycles for the converters discussed in [29]

Duty Cycle %	**SSSBC** V_{sw_max}/V_o	**ISSBC** V_{sw_max}/V_o
10	1.97	1.92
20	2.21	2.09
30	2.19	2.03
40	2.3	2.07
50	2.36	2.07
60	2.5	2.15

From table 1-1 it can be understood that as the duty cycle increases the ratio between the peak switch voltage and the output voltage increases for both the single switch and interleaved converter. It can also be seen that the ratio is much higher for the single switch converter. At a duty cycle greater than only 20% the peak switch voltage is already greater than two times the output voltage for both converters. If this circuit was to step-up the voltage to 380V this would mean the peak switch voltage stress is already 760V. This implies the need for higher rated components as well as additional heat capacity requirements for the converters switch, increasing the overall size and cost of the system. According to [29], the switch voltage is directly related to the auxiliary and resonant capacitor voltage as given in equation 1-24. This implies that higher rated components are also required for both these capacitors. The use of higher rated components also implies a higher cost for the system.

$$v_{sw} = v_{ca} + v_{cr} \quad \text{(Eq. 1-24)}$$

Another downside is that for the circuit to achieve the required step-up gain it must operate in continuous conduction mode (CCM). This means that the input current of the converter must always be positive and never reach zero. If the current does reach zero then the circuit operates in discontinuous conduction mode (DCM) which changes the circuit operation and the equations that govern them. In most cases the size of the converters input inductor affects this operation. For this converter an input inductor of 1mH is required such that it can operate in CCM. This value is quite high which implies a large size for the converter.

1.5 Electrolytic and Film Capacitors

For several step-up converters discussed in literature, electrolytic capacitors are used for the input capacitor. This is due to its high energy storage and low cost. Electrolytic capacitors have an energy density greater than that of film and ceramic capacitors at the same rated voltage. However, the lifetime expectancy of an electrolytic capacitor is much less than that of the overall converter and a prone to large failure rates [31-32]. For example, 10μF electrolytic capacitors have a lifespan on the range from 1,000h to 10,000h while the lifespan of the system can range up to 50,000h [56]. Table 1-2 contains a comparison of parameters for various electrolytic capacitors available in the market.

Table 1-2. Comparison of electrolytic capacitor parameters

Electrolytic Capacitor	**Capacitance**	**Rated voltage**	**Life expectancy**	**Dimensions(mm)**
NLW25-100 [33]	25 μF	100 V	1000 h	10.1 x 22
EEE-2AA [34]	10 μF	100 V	2000 h	8.0 x 6.2
B41041A [35]	25 μF	100 V	2000 h	6.3 x 12.5
187KXM100M [36]	180 μF	100 V	5000 h	7.5 x 0.8

In order to circumvent this issue, film capacitors can be employed at the input of converters. Unlike electrolytic capacitors, film capacitors have a life expectancy greater than that of the overall system [31-32]. Table 1-3 contains a comparison of parameters for various film capacitors available in the market. For applications with a solar panel at the input the required rated voltage is in the range of 30 to 100V. It can be seen that the life expectancy of the film capacitors are much larger than that of the electrolytic capacitors listed in table 1-2 at the same rated voltage. By employing the use of film capacitors at the input of a power electronic converter instead of an electrolytic capacitor the life expectancy of the overall system can be improved.

Table 1-3. Comparison of film capacitor parameters

Film Capacitor	**Capacitance**	**Rated voltage**	**Life expectancy**	**Dimensions (mm)**
EF1106 [37]	10 μF	100 V	15000 h	26 x 11.5
JSNEK5250 [38]	25 μF	100 V	17500 h	17.3 x 21.5
EZP-E5025 [39]	25 μF	500 V	>24 months	41.5 x 20
MKT1820 [40]	180 μF	100 V	>24 months	57.5 x 25

1.6 Review on Maximum Power Point Tracking Techniques for Solar Energy Systems

Unfortunately, solar energy systems do not generate a constant amount of power. Their output is directly affected by factors such as the position of the sun, cloud cover, and clarity of the atmosphere. A solar panel's Power-Voltage and Current-Voltage characteristics are non-linear and vary with the irradiation and temperature. Fig 1-15 shows an example of a solar panel Power-Voltage curve for different light intensities. From here it can be seen that there is one operating point on each curve where the panel operates at its maximum power. This location is known as the Maximum Power Point (MPP). Solar energy systems do not naturally operate at this condition and during operation the location of the MPP is unknown. However, the MPP can be located through the use of calculation models and search algorithms. Therefore, a maximum power point tracking (MPPT) controller is required to locate the optimal operation point such that the panels maximum power can be extracted at every operating condition. An example of the overall system is shown in fig 1-16.

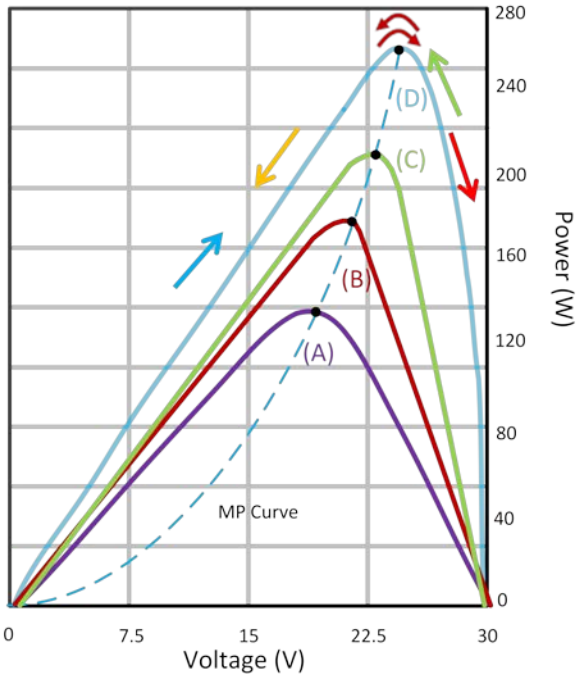


Figure 1-15: Power voltage curve of a solar panel for various light intensities: D > C > B > A

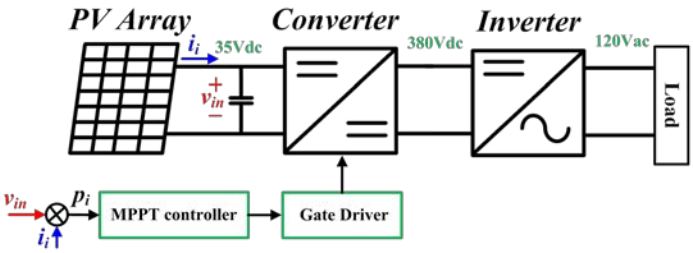


Figure 1-16: PV array connected to a power electronic converter with an integrated MPPT controller.

Several different MPPT techniques have been presented in literature for use in solar energy system. This section will introduce some of these techniques including perturb and observe, incremental conductance, and first order differential fuzzy logic [41-56].

1.6.1 Perturb and Observe

The perturb and observe (P&O) method is one of the basic MPPT techniques used in solar energy systems. It involves varying one of the operating parameter (duty cycle or frequency) of the power electronic converter which will modify the operating voltage of the solar panel. From here the change in power is recorded and compared to that of the previous iteration. The controller then determines how to change the operating parameter again such that the system operates at the maximum power [30-41]. An example of a duty cycle based P&O method is shown in fig 1-17 which consists of two P-V curves of a solar panel. In this example, when the light intensity changes from low to high the optimal operating point shifts from 29V to 35V as seen in fig 1-17 (a) and 1-17 (b) respectively. However the operating point of the solar panel has not changed as it is 29V. The controller then varies the duty cycle to see how the input power

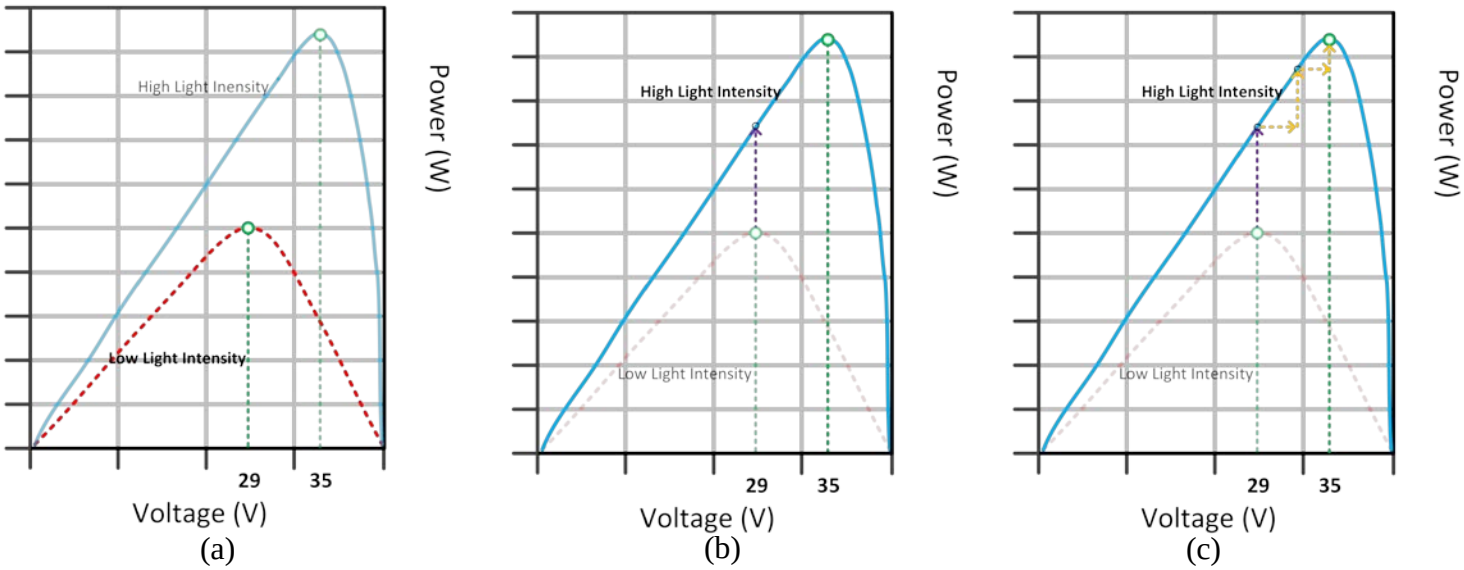


Figure 1-17: Maximum power point tracking using conventional perturb and observe: (a) low light intensity MPP operation, (b) Light intensity increased, (c) moving towards high light intensity MPP operation

changes. If the duty cycle change results in an increase in the input power, the controller will continue to move in that direction until the maximum operating point is reached as seen in fig 1-17 (c) [48-49].

One issue with the P&O method is that it will never operate at the maximum power point. Instead it will oscillate around it as the controller will constantly vary the duty cycle or frequency. In order to minimize this oscillation the control variable step size is small but as a result of this the controller takes time to reach closer to the best operating point [48-49].

1.6.2 Incremental Conductance

The P&O method compared the change in the input power to that of the previous cycle. Another method to track the maximum power point without checking the input power is known as incremental conductance [41-47, 52, 53]. In this method the controller checks the rate of change of the input current as a function of the rate of change of the input voltage. There are three conditions that the controller checks for which are shown in equations 1-25 to 1-27 respectively.

$$\frac{di}{dv} > -\frac{i}{v} \quad \text{(Eq. 1-25)}$$

$$\frac{di}{dv} < -\frac{i}{v} \quad \text{(Eq. 1-26)}$$

$$\frac{di}{dv} = -\frac{i}{v} \quad \text{(Eq. 1-27)}$$

If the rate of change of the input current as a function of the rate of change of the input voltage is greater than the negative of the input current divided by the input voltage then the system is

operating to the left of the MPP. The controller then changes the control variable such that the system operates closer to the MPP. If instead the value is less than the negative of the input current divided by the input voltage then the system is operating to the right of the MPP. If the values are equal then the system is operating at the MPP.

Unlike the P&O method, the incremental conductance method can determine when the system is operating at the maximum power point which can minimize oscillation. However it relies on more complex mathematical equations which results in a longer time taken to reach the maximum power point. As a result, the incremental conductance method faces difficulties operating under rapidly changing atmospheric conditions [52, 53].

1.6.3 Fuzzy Logic

In the case of P&O and incremental conductance the controller changes the control variable based on true and false comparisons. Fuzzy logic is a control based approach that deals with multiple truths. That is to say it works off of degrees of truth such as partially true or partially false. It consists of three stages: fuzzification, inference, and defuzzification. In the fuzzification stage the controller converts the input parameters to linguistic variables that are used by the controller. From here the variables are mapped to a lookup table such as the one shown in table I. [41-47, 54, 55]

TABLE 1-4. Rule base table with five fuzzy levels [55]

Linguistic Variable	**NB**	**NS**	**ZE**	**PS**	**PB**
NB	PB	PB	PS	PB	PB
NS	PB	PS	PS	PS	PB
ZE	NS	NS	ZE	PS	PS
PS	NB	NS	NS	NS	NB
PB	NB	NB	NS	NB	NB

In table I. there are five different fuzzy levels which are negative big (NB), negative small (NS), zero (ZE), positive small (PS), and positive big (PB). The more levels a fuzzy logic controller uses the more accurate its performance is, however additional levels increases the difficulty of implementation. Once the variables have been mapped using the lookup table the controller then converts the results from a linguistic variable back to an output variable and uses this result to vary the control variable.

1.7 Research Motivation

The integration of solar energy systems with power electronic converters is required to ensure optimal system operation. Existing converters suffer from several drawbacks such as lower efficiency due to hard switching, low switching frequency to maintain continuous conduction mode, and large size and cost due to high rated component. These drawbacks hinder the circuits from being able to achieve desirable performance. The discussed converters can handle many of these drawbacks but not all of them at once. The research motivation for this thesis is to address the drawbacks of existing converters and devise an improved topology that can be applied for solar energy systems as well as can be integrated with a maximum power point tracker.

1.8 Thesis Contributions

By taking into account the drawbacks of conventional converters as well as converters discussed in literature, a new single-switched quasi-resonant DC/DC converter will be devised in this thesis. The features of this proposed converter are as follows:

1. The proposed converter is designed to operate with a single 35V solar panel while maintaining an output voltage between 380V and 400V.
2. The converter's gain will be achieved through the use of a single switch.
3. Quasi-resonant zero-voltage switching will be employed in the circuit to improve the overall efficiency. By minimizing the switching power loss, the circuit can operate at a high switching frequency on the order of hundreds of kilohertz. This will decrease the size of all the required passive components, allowing for a reduced cost.

4. The input inductor of the proposed circuit will operate in continuous conduction mode, allowing for the use of a small-sized film capacitor at the input side instead of an electrolytic capacitor. This extends the lifespan of the overall system.
5. The proposed converter will employ an improved coupled inductor structure to achieve a high step-up ratio.
6. The switch voltage to output voltage ratio will be significantly decreased compared to the circuit topologies discussed in order to minimize the required switch voltage rating.
7. A maximum power point tracking controller will be designed and integrated with the proposed converter that will function at various light intensities.

2. Proposed Quasi-Resonant Soft-Switched DC/DC Converter

2.1 Introduction and Description

The proposed quasi-resonant step up coupled-inductor circuit is shown in Fig. 2-1. Table 2-1 contains a list of each component. The converter consists of a single switch (S) which operates under quasi resonant zero-voltage switching (ZVS) condition. This operating condition is made possible through the use of the converter's resonant components which are the inductor (L_r) and the capacitor (C_r). The resonant capacitor is connected in parallel with the switch and as a result the switch voltage is the same as the capacitor voltage. The switch is controlled through the use of variable switching frequency and duty cycle. Variable switching frequency control is employed when operating in maximum power point tracking mode while variable duty cycle control is employed in all cases to maintain a larger frequency range for soft-switching. The circuit contains a three-winding coupled inductor with an inverted polarity for the primary winding as shown by the location of the dot in fig 2-1. The secondary winding has one node connected to the load while the other is connected to a diode D_1. This diode does not conduct throughout the entire circuit operation and as a result the secondary winding is only active partially throughout a switching cycle. The tertiary winding is connected between the input inductor and the two output capacitors. As it is not connected to a diode the winding is active throughout the entire circuit operation. For this coupled inductor the positive node of the primary is directly connected to the negative of the tertiary.

Table 2-1: Components used in the proposed quasi-resonant step-up converter

Component	Description
C_1	Input Capacitor
C_2	Output Capacitor
C_3	Output Capacitor
C_r	Resonant Capacitor
L_{in}	Input Inductor
L_r	Resonant Inductor
L_p	Primary Winding
S	Switch

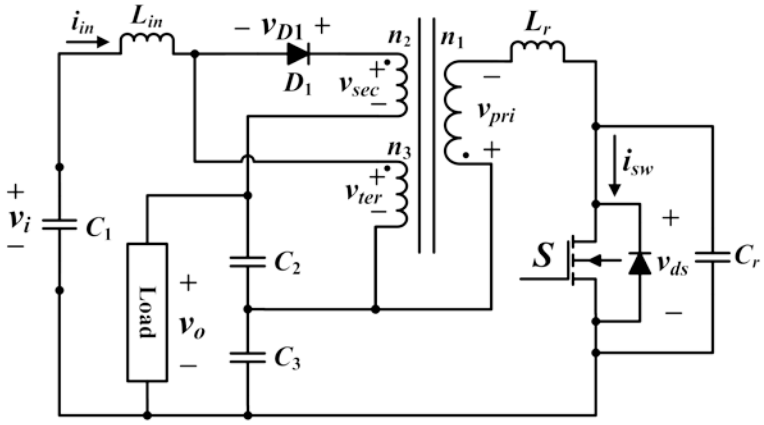


Figure 2-1: Proposed quasi-resonant step-up converter

Kirchhoff's voltage law (KVL) states that for a series closed loop path the sum of the voltage across each component is equal to 0. The voltage-second balance principle states that the average inductor voltage is zero. By applying KVL and the voltage-second balance principle a few features of the circuit can be noted. Figure 2-2(a) shows the proposed circuit with a closed loop consisting of the input capacitor C_1, input inductor L_{in}, tertiary winding L_{ter}, and the output capacitor C_3 with the voltage across each shown in the figure. Equation 2-1 can be obtained by applying KVL to this loop. However from the voltage-second balance principle it is known that the average voltage across the input inductor and the tertiary winding is zero. From this it can be seen that the average voltage across C_3 is equal to the input voltage (equation 2-2). Since the capacitor is active throughout the circuit operation causes the voltage to be constant. Another feature of the circuit can be observed in equation 2-3. As the average voltage across L_{in} and L_{ter}, are equal to zero and since they are the only inductors in the closed loop their voltages are equal but opposite in magnitude.

$$v_{c_1} = -v_{Lin} + v_{ter} + v_{c_3} \quad \text{(Eq. 2-1)}$$

$$v_{c_1} = v_{c_3} \quad \text{(Eq. 2-2)}$$

$$v_{L_{in}} = -v_{ter} \quad \text{(Eq. 2-3)}$$

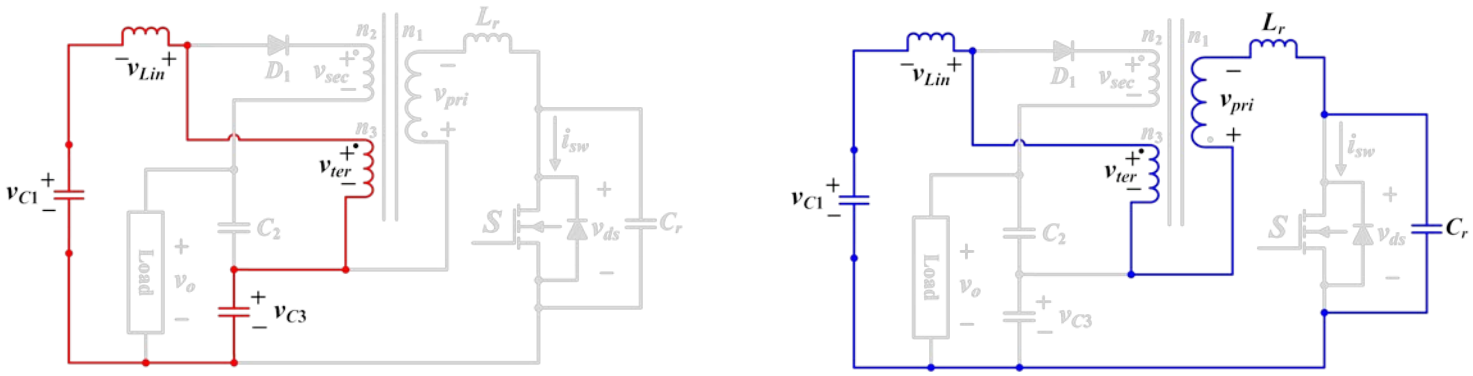


Figure 2-2: KVL loop: (a) input capacitor, input inductor, tertiary winding, and output capacitor, (b) input capacitor, input inductor, tertiary winding, primary winding, resonant inductor and resonant

This same technique can be applied to the blue loop show in fig. 2-2 (b) which contains C_1, L_{in}, L_{ter}, primary winding L_{pri}, resonant inductor L_r, and the resonant capacitor C_r which results in equation 2-4. From here all the inductor voltage components are removed as their average is 0. This results in equation 2-5 from which it can be seen that the average switch voltage is equal to the input voltage. However unlike with the output capacitor the resonant capacitor is not active throughout the entire circuit operation which means the peak switch voltage will be much higher than the input voltage.

$$v_{c_1} = -v_{Lin} + v_{ter} + v_{pri} + v_{Lr} + v_{ds} \quad \text{(Eq. 2-4)}$$

$$\int_o^t v_{ds} = v_{c_1} \quad \text{(Eq. 2-5)}$$

The chosen coupled inductor for the circuit consists of three-windings. Coupled inductors can be modeled as a transformer with the magnetizing inductance representing the primary winding. This also implies that the equations for a transformer hold true for the coupled inductor. There is a relationship between the turns ratio and the voltage across each winding. The voltage across the secondary and tertiary windings can be written in terms of the primary as shown in equation 2-6 while the inductance of these windings can be written in terms of the primary as shown in equation 2-7.

$$v_{pri} = -v_{\text{sec}} \frac{N_1}{N_2} = -v_{ter} \frac{N_1}{N_3} \quad \text{(Eq. 2-6)}$$

$$L_{pri} = L_{\text{sec}} \left(\frac{N_3}{N_1} \right)^2 = L_{ter} \left(\frac{N_3}{N_1} \right)^2 \quad \text{(Eq. 2-7)}$$

The voltage across each winding can also be written in terms of the rate of change of the current flowing through all three windings and the mutual inductance. The mutual inductance is a relation between two windings and depends on the properties of the transformer such as the winding inductance and the number of turns. Equations 2-8 to 2-11 contain the mutual inductance for the three possible combinations.

$$M_{12} = \frac{L_p N_1 N_2}{N_1^{\,2}} \qquad \text{(Eq. 2-8)}$$

$$M_{13} = \frac{L_p N_1 N_3}{N_1^{\,2}} \qquad \text{(Eq. 2-9)}$$

$$M_{23} = \frac{L_p N_2 N_3}{N_1^{\,2}} \qquad \text{(Eq. 2-10)}$$

Equations 2-11 to 2-13 contain the voltage across each winding in terms of the mutual inductance and rate of change of the current. This shows that the polarity of the winding plays a role in the equation. As the primary winding has an inverted polarity, its voltage treats the secondary and tertiary currents as negative. The secondary and tertiary voltage equations also treat the primary current as negative. By comparing equations 2-11 to 2-13 with equations 2-6 and 2-7 it can be seen that the turn's ratio relation still holds. As previously mentioned the secondary winding is not active throughout the entire circuit operation. During these stages the rate of change of current through the secondary winding is zero and as a result its contribution is removed from the equation.

$$v_{pri} = L_p \frac{di_1}{dt} - M_{12} \frac{di_2}{dt} - M_{13} \frac{di_3}{dt} \qquad \text{(Eq. 2-11)}$$

$$v_{ter} = L_t \frac{di_3}{dt} - M_{13} \frac{di_1}{dt} + M_{23} \frac{di_2}{dt} \qquad \text{(Eq. 2-12)}$$

$$v_{\text{sec}} = L_s \frac{di_2}{dt} - M_{12} \frac{di_1}{dt} + M_{23} \frac{di_3}{dt} \qquad \text{(Eq. 2-13)}$$

2.2 Operating Principles

There are two different modes of operation for this circuit named A and B respectively. Mode A allows for a higher voltage gain in exchange for a larger switch voltage stress. This results in a switch voltage to output voltage ratio greater than one. Mode B allows for a lower switch voltage stress such that the ratio between the switch voltage and the output voltage is less than one. However, mode B has a lower gain compared to mode A and has a larger peak switch current. Each mode of operation is broken down into four stages. This section will discuss the four stages and then theoretical analysis for both the mode A and mode B.

2.2.1 Mode A

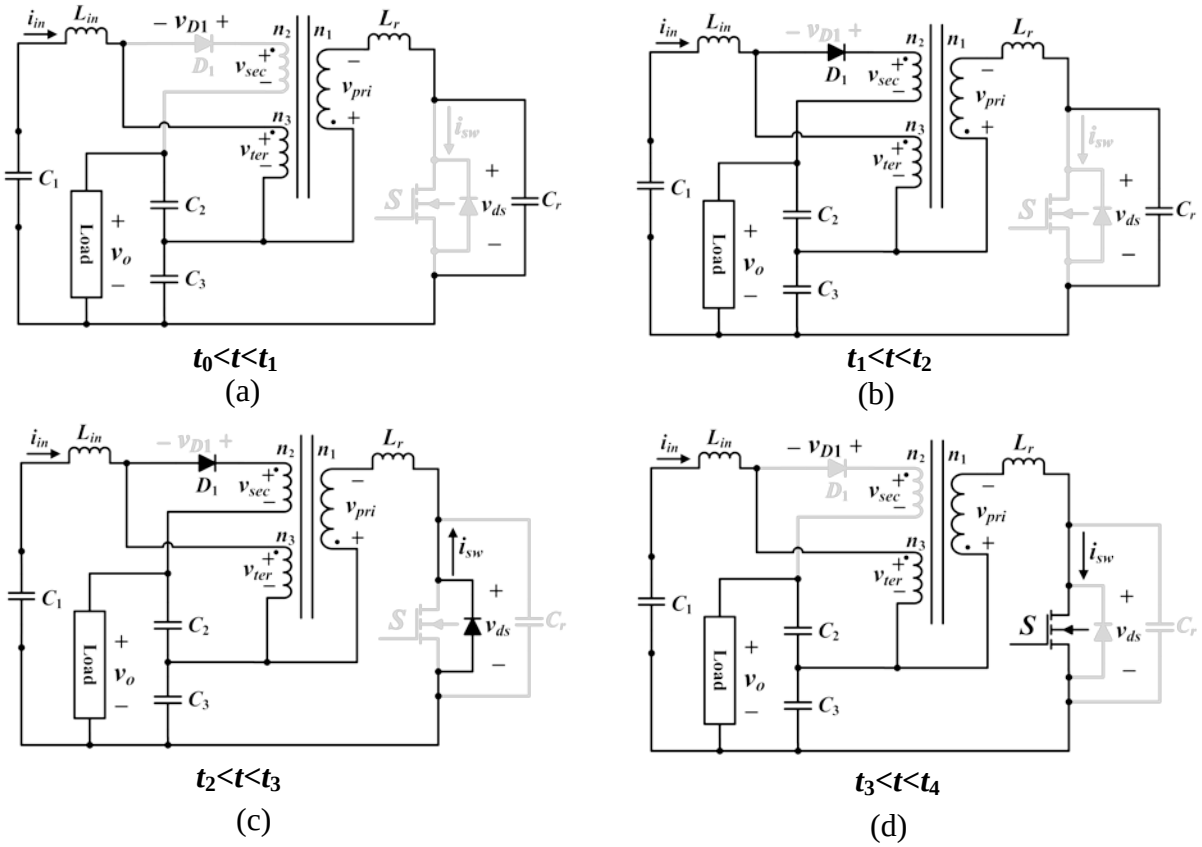


Figure 2-3: Mode A: (a) Resonant capacitor charge stage, (b) Resonant stage, (c) Resonant inductor charge stage 1, (d) Resonant inductor charge stage 2

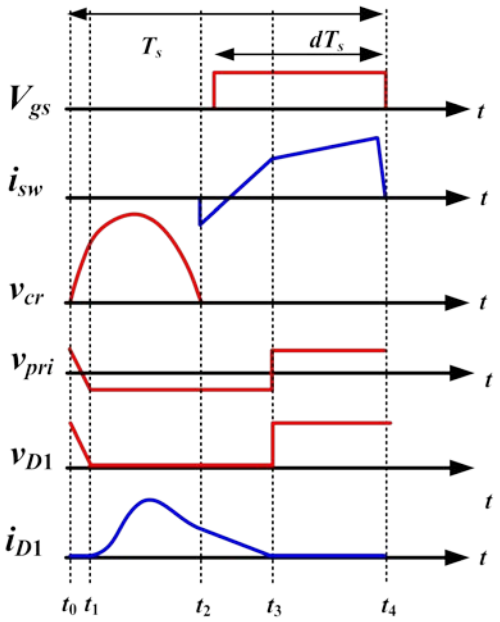


Figure 2-4: Theoretical operation waveforms for the proposed converter during mode A

Fig. 2-3 shows the four stages of operation for mode A. The paths and components in the figure that are black are active while the paths and components that are grey are inactive. Fig. 2-4 shows the theoretical waveforms for several of the circuit components when operating in mode A. The waveforms are broken down into four stages which range from t_0 to t_4.

Mode A Stage I ($t_0 < t < t_1$): Fig. 2-3(a) depicts the circuit during the resonant capacitor charging stage. At time t_0 the gate signal is removed from the switch (S) which causes it to turn off. The current that was flowing through S now begins to flow through the resonant capacitor (C_r). As this current is positive, C_r begins to charge. The current flowing through C_r is sinusoidal which results in a sinusoidal increase in the capacitor voltage. However, due to the small time duration of stage I it can be considered as a linear increase as shown in Fig. 2-4. The frequency at which this sinusoidal waveform operates is a function of the resonant inductor (L_r), C_r, the primary inductance (L_p), the input inductance (L_{in}), and the transformer turns ratio. This is provided in equation 2-14 with the derivation shown in the appendix. By applying to KVL to the closed loop containing the output capacitor (C_3), L_p, L_r, and C_r (equation 2-1) it can be seen that

in order for the C_r to charge the voltage of the other three must decrease. However since the voltage across C_3 is constant throughout the operation only the voltage across L_p and L_r can decrease. In order for this stage to end a component of the circuit must change states (on to off or off to on) and in this case it is the diode D_1. D_1 is currently off due to the voltage across it being negative. The time duration for this stage is provided in equation 2-15 while the derivation is shown in the appendix.

$$\omega_0 = \frac{1}{\sqrt{\frac{L_p L_{in} + L_{in} L_r + L_r L_p N_3^{\,2}}{L_{in} + L_p N_3^{\,2}} C_r}} \quad \text{(Eq. 2-14)}$$

$$t_1 = \frac{1}{\omega_0}\left(\sin^{-1}\left[\frac{C - B}{\sqrt{A^2 + B^2}} \right] - \cos^{-1}\left[\frac{A}{\sqrt{A^2 + B^2}} \right] \right) \quad \text{(Eq. 2-15)}$$

$$A = i_{Lr}(t_0) Z \quad \text{(Eq. 2-16)}$$

$$B = v_i \quad \text{(Eq. 2-17)}$$

$$C = \left[1 + \frac{L_{in} + L_p N_3^{\,2}}{L_p L_{in}} \right] \left[v_i - \frac{v_o - v_i}{n_2 - n_3} \right] \quad \text{(Eq. 2-18)}$$

$$Z = \sqrt{\frac{\frac{L_p L_{in} + L_{in} L_r + L_r L_p N_3^{\,2}}{L_{in} + L_p N_3^{\,2}}}{C_r}} \quad \text{(Eq. 2-19)}$$

Mode A Stage II ($t_1 < t < t_2$): Fig. 2-3(b) depicts the circuit during the resonant stage. At time t_1 the diode D_1 has turned on and the circuit has entered its second operating stage. The voltage v_{pri} is constant throughout this operating stage which implies the voltage v_{ter} and v_L are also constant. By applying this to equation 2-4, it can be determined that only the voltage across L_r and C_r are changing. As a result, during this resonant stage the inductor and capacitor are exchanging energy. This resonance results in a sinusoidal waveform for both the switch voltage (v_{ds}) and current (i_{Lr}) as seen in Fig. 2-4. This equation for v_{ds} is provided in equation 2-20 where ω_0 is the resonant frequency provided in 2-21 and Z is the characteristic impedance provided in 2-22. When comparing these values to the ones from stage 1 it can be seen that several factors have been removed. This is because only the resonant inductor and capacitor are resonating during stage II. The voltage v_{ds} will continue to increase until the current i_{Lr} has reached zero. At this point v_{ds} has reached its peak (equation 2-23) and will begin to decrease. This stage ends once the v_{ds} has reached zero and the total stage time period is provided in (equation 2-24). The equation that governs i_{Lr} during stage II is provided in equation 2-28. As mentioned previously, during this stage D_1 is on which implies that current is flowing through it. The equation that governs i_{D1} during stage II is provided in equation 2-29. As this stage ends when the switch voltage reaches zero, current will still be flowing through the diode during the stage transition.

$$v_{ds} = v_i - v_{pri} + i_{lr}(t_0)Z\sin(\omega_0 t) + (v_i - v_{pri} + v_{ds}(t_1))\cos(\omega_0 t) \quad \text{(Eq. 2-20)}$$

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \quad \text{(Eq. 2-21)}$$

$$Z = \sqrt{\frac{L_r}{C_r}} \quad \text{(Eq. 2-22)}$$

$$v_{ds\_\max} = v_i - v_{pri} + i_{lr}(t_0)Z \quad \text{(Eq. 2-23)}$$

$$t_2 = \frac{1}{\omega_0}\left(\cos^{-1}\left[\frac{F}{\sqrt{D^2+E^2}}\right] - \tan^{-1}\left[\frac{E}{D}\right]\right) \quad \text{(Eq. 2-24)}$$

$$D = i_{Lr}(t_1)Z \quad \text{(Eq. 2-25)}$$

$$E = v_{ds}(t_1) + \frac{v_o - v_i}{n_2 - n_3} - v_i \quad \text{(Eq. 2-26)}$$

$$F = v_i - \frac{v_o - v_i}{n_2 - n_3} \quad \text{(Eq. 2-27)}$$

$$i_{Lr} = \frac{-F\sin(\omega_0 t)}{Z} + i_{Lr}(t_1)\cos(\omega_0 t) \quad \text{(Eq. 2-28)}$$

$$i_{D1} = \frac{v_p}{\omega_0(n_2-n_3)}\left[\frac{L_{in}+L_p n_3^{\,2}}{L_{in}L_p}\right]t - \frac{v_p}{\omega_0(n_2-n_3)}\left[\frac{L_{in}+L_p n_3^{\,2}}{L_{in}L_p}\right]\sin(\omega_o t) - \frac{i_s(1)}{n2-n3}\cos(\omega_o t) + \frac{i_s(1)}{n2-n3} \quad \text{(Eq. 2-29)}$$

Mode A Stage III ($t_2 < t < t_3$): Once the switch voltage v_{ds} has reached zero the resonant capacitor has fully discharged and the circuit proceeds to the stage III. The current i_{Lr} that was once flowing through the resonant capacitor, which is still negative in polarity, is diverted to the anti-parallel diode of the switch. This current continues to increase slowly as seen in figure 2-4. By ensuring the gate signal is applied to the switch before the current becomes positive the circuit will operate under ZVS condition. Now that resonance has ended the current flowing through the diode begins to decrease linearly during this stage at a rate given in equation 2-30. This stage ends once the diode D_1 is switched off.

$$i_{D1} = \frac{\left[\left(v_o - v_i\right)\left(L_{in}L_p + L_{in}L_r + L_pL_r{n_3}^2\right) - L_pL_rv_i\left(n_2 - n_3\right)\right]}{L_{in}L_pL_rv_i\left(n_2 - n_3\right)^2} \quad \text{(Eq. 2-30)}$$

$$t_3 = T - t_1 - t_2 - t_4 \quad \text{(Eq. 2-31)}$$

Mode A Stage IV (t_3 < t < t_4): The secondary winding diode D_1 has switched off which disconnects the winding from the circuit. This results in a decrease in the switch current slope. As the primary and tertiary windings are still active the voltage across each winding can be calculated by applying the voltage formula for close-coupled inductors. These two equations are provided in equation 2.32 and 2.33 respectively.

$$v_{pri} = L_p\frac{di_1}{dt} - M\frac{di_2}{dt} \quad \text{(Eq. 2-32)}$$

$$v_{ter} = L_t\frac{di_2}{dt} - M\frac{di_1}{dt} \quad \text{(Eq. 2-33)}$$

The currents i_1 and i_2 represent the current flowing through the primary and tertiary windings respectively. As the current flowing through the primary winding and the resonant inductor are the same, the resonant inductor current can be represented in terms of i_1. The same can be done for the input inductor voltage and i_2.

By applying KVL to the primary (eq. 2-34) and tertiary windings (eq. 2-35) the rate of change for the switch current and the input inductor current can be calculated. These equations are provided in equation 2-36 and 2-37 respectively.

$$v_{c3} = L_p \frac{di_1}{dt} + L_p \frac{n_3}{n_1} \frac{di_3}{dt} + L_r \frac{di_1}{dt} \quad \text{(Eq. 2-34)}$$

$$0 = L_p \frac{n_3}{n_1} \frac{di_1}{dt} + L_p \left(\frac{n_3}{n_1} \right)^2 \frac{di_3}{dt} + L_{in} \frac{di_3}{dt} \quad \text{(Eq. 2-35)}$$

$$\frac{di_1}{dt} = v_i \left[\frac{L_{in} + L_p {n_3}^2}{L_p L_r {n_3}^2 + L_{in} L_p + L_{in} L_r} \right] \quad \text{(Eq. 2-36)}$$

$$\frac{di_3}{dt} = v_i \left[\frac{L_p n_3}{L_p L_r {n_3}^2 + L_{in} L_p + L_{in} L_r} \right] \quad \text{(Eq. 2-37)}$$

These equations also prove that the input current is transferred to the primary side through the tertiary windings. This mode ends once the switch turns off and the circuit re-enters capacitor charging state and its duration is given in (16).

$$t_4 = \frac{(T - t_1)(v_O - v_i + n_2 v_{pri})}{L_{in} \frac{di_3}{dt} + (v_O - v_i + n_2 v_{pri})} \quad \text{(Eq. 2-38)}$$

2.2.2 Mode B

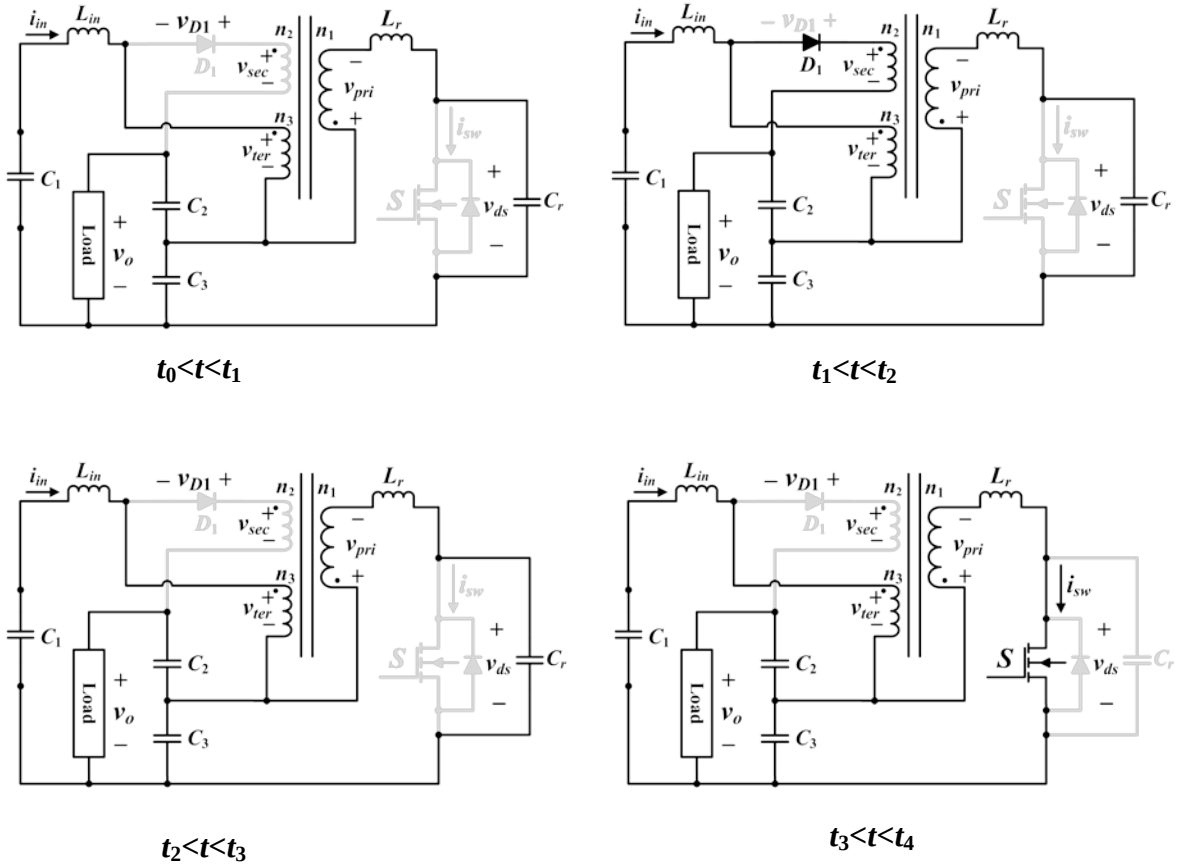


Figure 2-5: Mode B: (a) Resonant capacitor charge stage, (b) Resonant stage, Resonant capacitor discharge state, Resonant inductor charge stage

Fig. 2-5 shows the four stages of operation for mode B. The paths and components in the figure that are black are active while the paths and components that are grey are inactive. Fig. 2-6 shows the theoretical waveforms for several of the circuit components when operating in mode B. As with mode A, the waveforms are broken down into four stages which range from t_0 to t_4. These represent the waveforms during each operating stage.

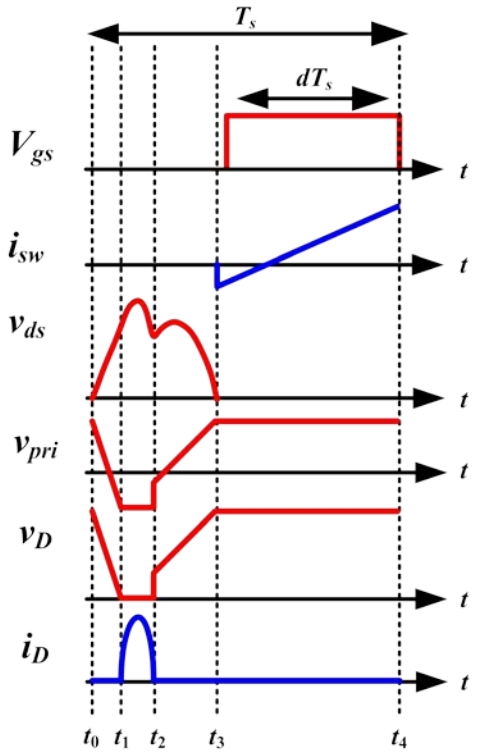


Figure 2-6: Theoretical operation waveforms for the proposed converter during mode B

Mode B Stage I ($t_0 < t < t_1$): Stage I of mode B is similar to that of mode A. At time t_0 the gate signal is removed and the switch (S) is turned off. As a result the current that was flowing through S is now redirected into the resonant capacitor (C_r) which allows it to begin charging. As with the mode A, the primary winding voltage v_{pri} begins to decrease until the voltage polarity across the diode D_1 is positive. The condition for this is provided in equation 2-41.

$$\omega_0 = \frac{1}{\sqrt{\frac{L_p L_{in} + L_{in} L_r + L_r L_p N_3^{\,2}}{L_{in} + L_p N_3^{\,2}} C_r}} \qquad \text{(Eq. 2-39)}$$

$$Z = \sqrt{\frac{\frac{L_p L_{in} + L_{in} L_r + L_r L_p N_3^{\,2}}{L_{in} + L_p N_3^{\,2}}}{C_r}} \qquad \text{(Eq. 2-40)}$$

$$t_1 = \frac{1}{\omega_0}\left(\sin^{-1}\left[\frac{C-B}{\sqrt{A^2+B^2}} \right] - \cos^{-1}\left[\frac{A}{\sqrt{A^2+B^2}} \right] \right) \quad \text{(Eq. 2-41)}$$

$$A = i_{Lr}(t_0)Z \quad \text{(Eq. 2-42)}$$

$$B = v_i \quad \text{(Eq. 2-43)}$$

$$C = \left[1 + \frac{L_{in} + L_p N_3^{\,2}}{L_p L_{in}} \right] \left[v_i - \frac{v_o - v_i}{n_2 - n_3} \right] \quad \text{(Eq. 2-44)}$$

Mode B Stage II ($t_1 < t < t_2$): At time t_1 the diode D_1 has turned on and the circuit has entered stage II. As with mode A stage II, the resonant capacitor and resonant inductor begin to resonate and exchange energy with a resonant frequency given in equation 2-45.

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \quad \text{(Eq. 2-45)}$$

As D_1 is now on, current is able to flow through the secondary winding. Part of the current that flows through the input inductor begins to flow through the secondary winding before reaching the load. The equation that governs this current is provided in equation 2-46.

$$i_{D1} = \frac{v_p}{\omega_0(n_2 - n_3)} \left[\frac{L_{in} + L_p n_3^{\,2}}{L_{in} L_p} \right] t - \frac{v_p}{\omega_0(n_2 - n_3)} \left[\frac{L_{in} + L_p n_3^{\,2}}{L_{in} L_p} \right] \sin(\omega_o t) - \frac{i_s(1)}{n2 - n3} \cos(\omega_o t) + \frac{i_s(1)}{n2 - n3} \quad \text{(Eq. 2-46)}$$

From equation 2-46 it can be seen that the diode current is a function of the primary voltage which is now constant, the secondary and tertiary turns ratio, the resonant frequency for stage II, and the resonant inductor current at the end of stage I. It consists of two sinusoidal components,

a linear component, and a constant. This equation can be simplified to 2-47 by realizing that there are two main constants in this equation.

$$i_D = at - a\sin(\omega_o t) - b\cos(\omega_o t) + b \quad \text{(Eq. 2-47)}$$

The voltage across the resonant capacitor (v_{ds}) continues to increase until it reaches its peak which is provided in equation 2-48. At this point the current (i_{Lr}) is negative and as a result v_{ds} begins to decrease from its maximum.

$$v_{ds\_\max} = v_i - v_{pri} + i_{lr}(t_0)Z \quad \text{(Eq. 2-48)}$$

Unlike mode A, the resonant capacitor will not fully discharge during stage II. Instead the current through the diode will reach zero. The total time of stage II can be determined by solving for *t* in equation 2-49. However, equation 2-49 is a transcendental function which means it is not possible to solve the equation in terms of *t*. This time period can instead be calculated through recursive formulas or through plotting the left and right hand side of equation 2-49 as a function of time and determining the intersection of the two plots.

$$at + b = a\sin(\omega_o t) + b\cos(\omega_o t) \quad \text{(Eq. 2-49)}$$

Mode B Stage III ($t_2 < t < t_3$): Once the secondary winding diode (D_1) has switched off the circuit enters stage III. The secondary winding has been disconnected from the circuit and as a result the equation that governed the switch voltage and current no longer apply. The resonant frequency has now changed from the equation provided in 2-45 back to equation 2-50 as the same components that were active in the first stage are now active. This can be seen by comparing figure 2-5(a) and (c).

$$\omega_0 = \frac{1}{\sqrt{\frac{L_p L_{in} + L_{in} L_r + L_r L_p N_3^{\,2}}{L_{in} + L_p N_3^{\,2}} C_r}} \qquad \text{(Eq. 2-50)}$$

As a result of this change, the current through the resonant capacitor begins to decrease. Once this value reaches zero the capacitor voltage v_{ds} has reached its second peak and begins to decrease. This stage ends once v_{ds} has reached zero.

Mode B Stage IV ($t_3 < t < t_4$): The resonant capacitor has fully discharged as the switch voltage has reached zero and the converter now proceeds to the final stage. The current that was flowing through the resonant capacitor is now redirected to the antiparallel diode of the switch. This current is negative in polarity and is slowly increasing. Before this value becomes positive the gate signal is applied to the switch which allows ZVS operation to be achieved. Once the current has become positive it begins to flow through the switch and continues to increase. This current will continue to increase until the gate signal is removed from the switch and the circuit re-enters stage 1.

2.3 Theoretical Analysis of the Proposed Converter

2.3.1 Converter Voltage Gain

The gain equation of both operating modes can be obtained by applying the voltage-second balance principle to the primary winding. As the primary winding of the transformer is an inductor the average voltage from t_0 to t_4 is zero. The stage time periods as well as the primary voltage level have been provided in terms of known parameters. From here the equation can be re-arranged and simplified to solve for gain of each circuit. Equation 2-51 contains the gain equation for (A) mode where t_1 to t_4 are provided in equations 2-15, 2-24, 2-31, and 2-38. Equation 2-52 contains the gain equation for (B) mode. Both equations are also a function of several inductors in the circuit including the input inductor (L_{in}), resonant inductor (L_r), and the primary winding inductance (L_p). The constant L_α represents a combination of these parameters. From both equations it can be seen the gain is always greater than 1 which is expected from a step-up converter.

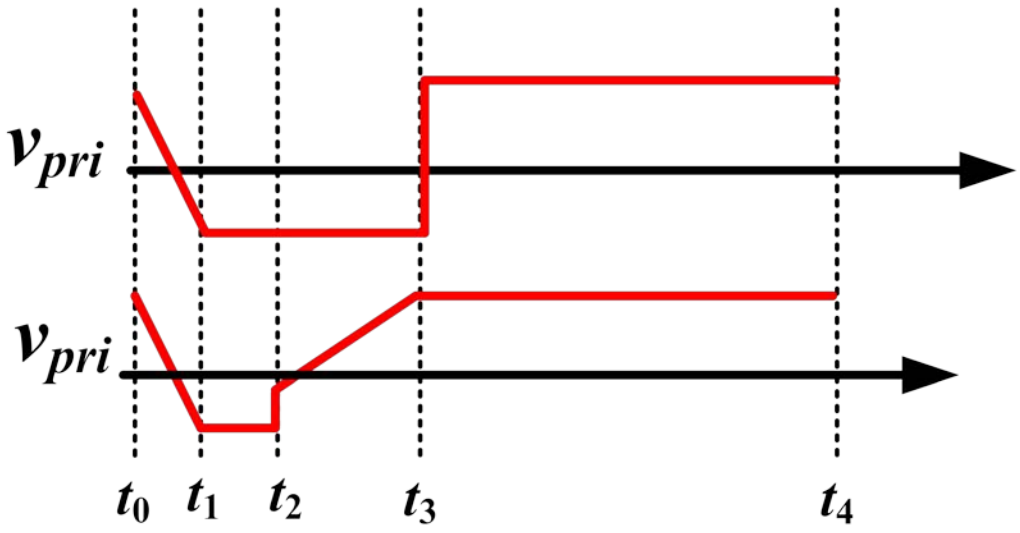


Figure 2-7: Coupled inductor primary winding voltage for both mode A and mode B.

$$\frac{v_o}{v_i} = 1 + \frac{\frac{t_1(n_2 - n_3 - 1)}{2} + (t_2 + t_3) + \frac{t_4(n_2 - n_3)}{L_\alpha}}{t_2 + t_3 - \frac{t_1}{2}} \quad \text{(Eq. 2-51)}$$

$$\frac{v_o}{v_i} = 1 + \frac{\left(\frac{n_2 - n_3}{n_1}\right)\left(\frac{t_3}{2} + \frac{1}{L\alpha}\left(t_4 + \frac{t_1}{2} + \frac{t_3}{2}\right)\right)}{t_2 + \frac{t_1}{2}} \quad \text{(Eq. 2-52)}$$

$$L_\alpha = \frac{L_p L_r \frac{n_3}{n_1}^2 + L_{in}L_p + L_{in}L_r}{L_{in}L_p} \quad \text{(Eq. 2-53)}$$

2.3.2 Voltage Gain vs Frequency

The operating frequency of the proposed converter affects the time duration of stages 1 to 4 for both operating modes. As a result the gain of the circuit can be controlled by varying the operating frequency. Fig. 2-8 shows the gain of both operating modes as a function of frequency. The frequency ranges from 100kHz to 250kHz and from here it can be seen that Mode A can achieve a higher gain than Mode B. To obtain an output voltage of 380V with an input voltage of 35V a gain of approximately 11 is required. For mode A, to achieve a gain of 11 the circuit must operate at a frequency of 120kHz while for mode B the required frequency is 110kHz.

The graphs also show that the gain of the converter is inversely proportional to the switching frequency. That is the higher the switching frequency the lower the converter's gain. It can also be seen that gain of the converter drops faster when operating in Mode B than with Mode A as the freuquency increases.

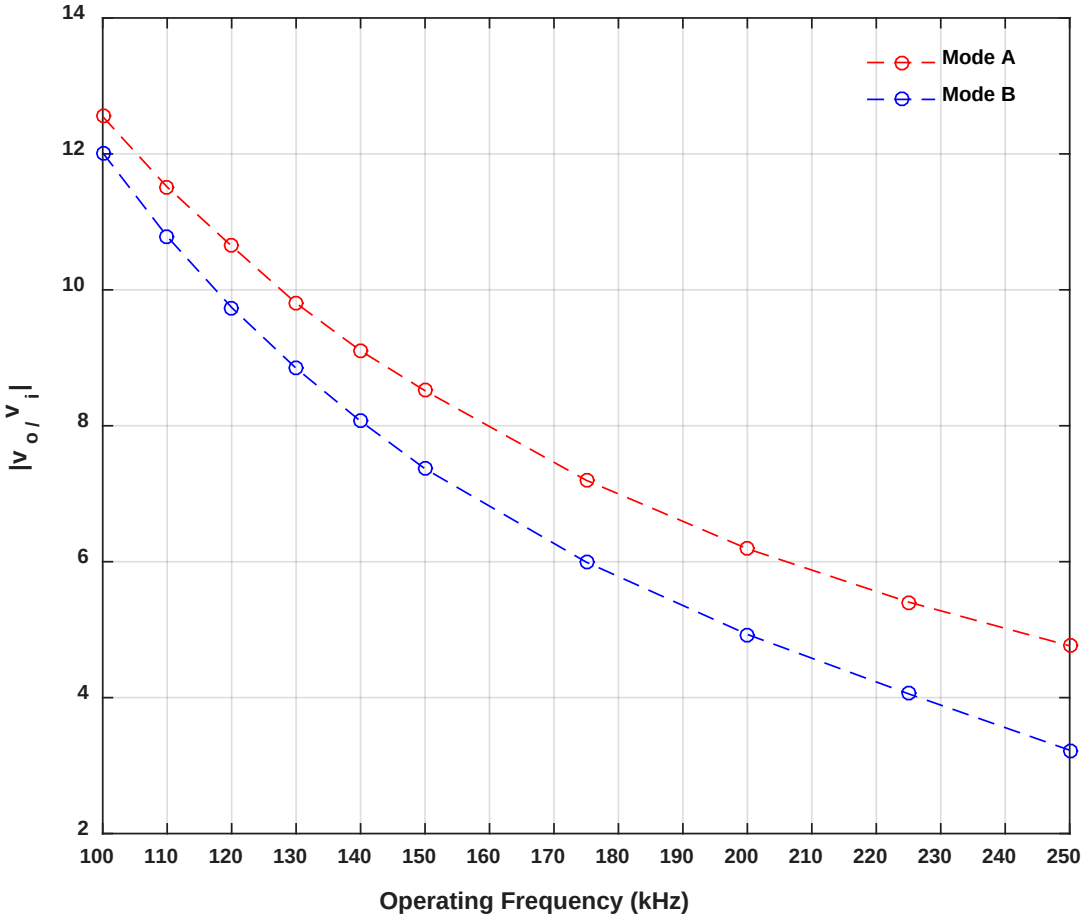


Figure 2-8: Gain of proposed converter as a function of frequency for both mode A and mode B.

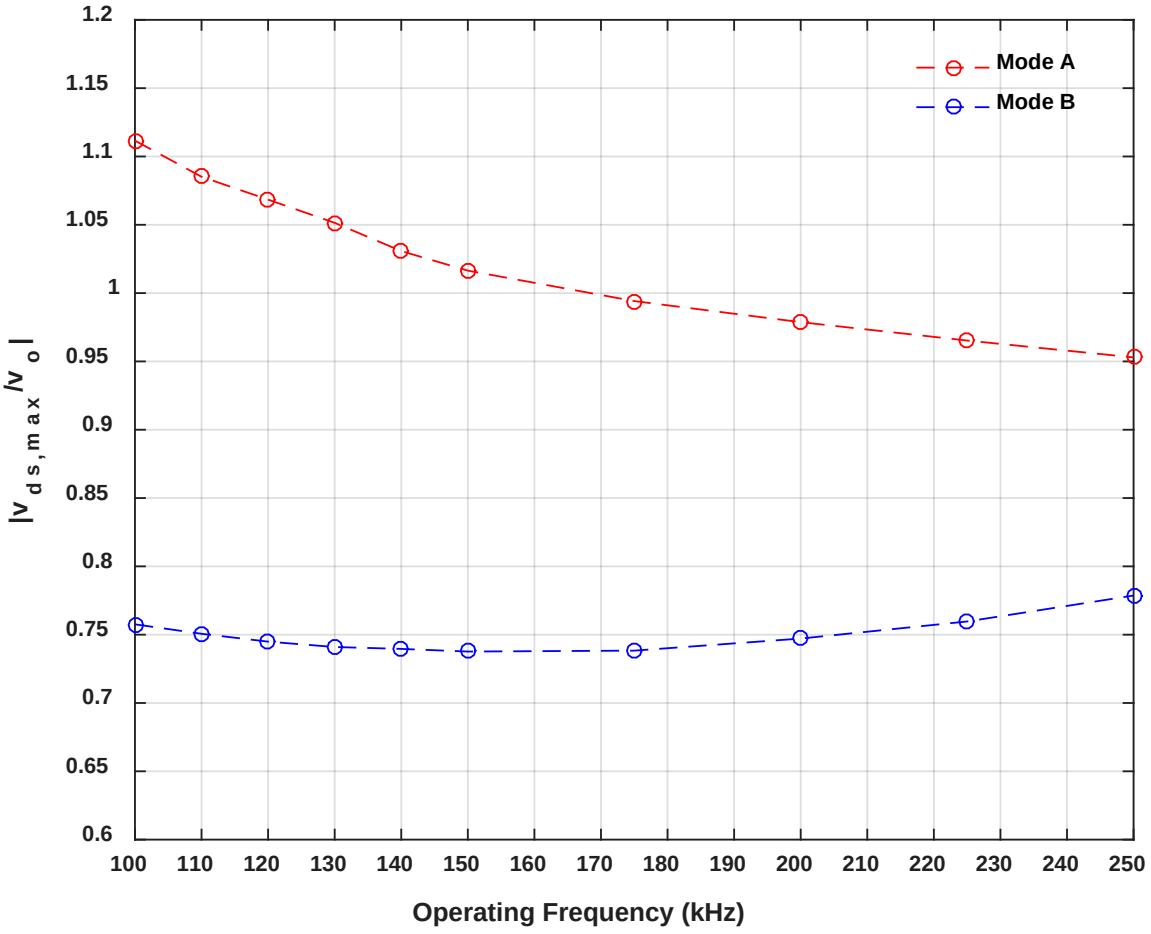


Figure 2-9: Peak switch voltage stress as a function of frequency for both mode A and mode B.

2.3.3 Switch Voltage Stress to Output Voltage Ratio

As mentioned in section 2.2 the maximum switch voltage stress occurs during stage 2 of both mode (A) and mode (B). This maximum is a function of known parameters such as the resonant components (L_r and C_r), input inductor (L_{in}) and the primary winding inductance (L_p). Fig. 2-9 shows a plot of the ratio of the switch voltage stress and output voltage for both mode A (red) and mode B (blue) as a function of frequency. Here it can be seen that the proposed circuit operating in mode B has a ratio less than one and there is a specific operating frequency at which the minimum ratio is obtained. In the case of the proposed circuit operating in mode A, the ratio

is greater than one. As the operating frequency increases the ratio begins to decrease and becomes less than one at frequencies greater than 160kHz.

The loading condition of the converter has an impact on ratio between the maximum switch voltage (v_{ds_max}) and the output voltage (v_o). Figure 2-10 shows the peak switch voltage to output voltage ratio as a function of frequency for mode A at different loading conditions. These conditions are 100% (2000Ω), 66% (3000Ω), 50% (4000Ω), and 40% (5000Ω).

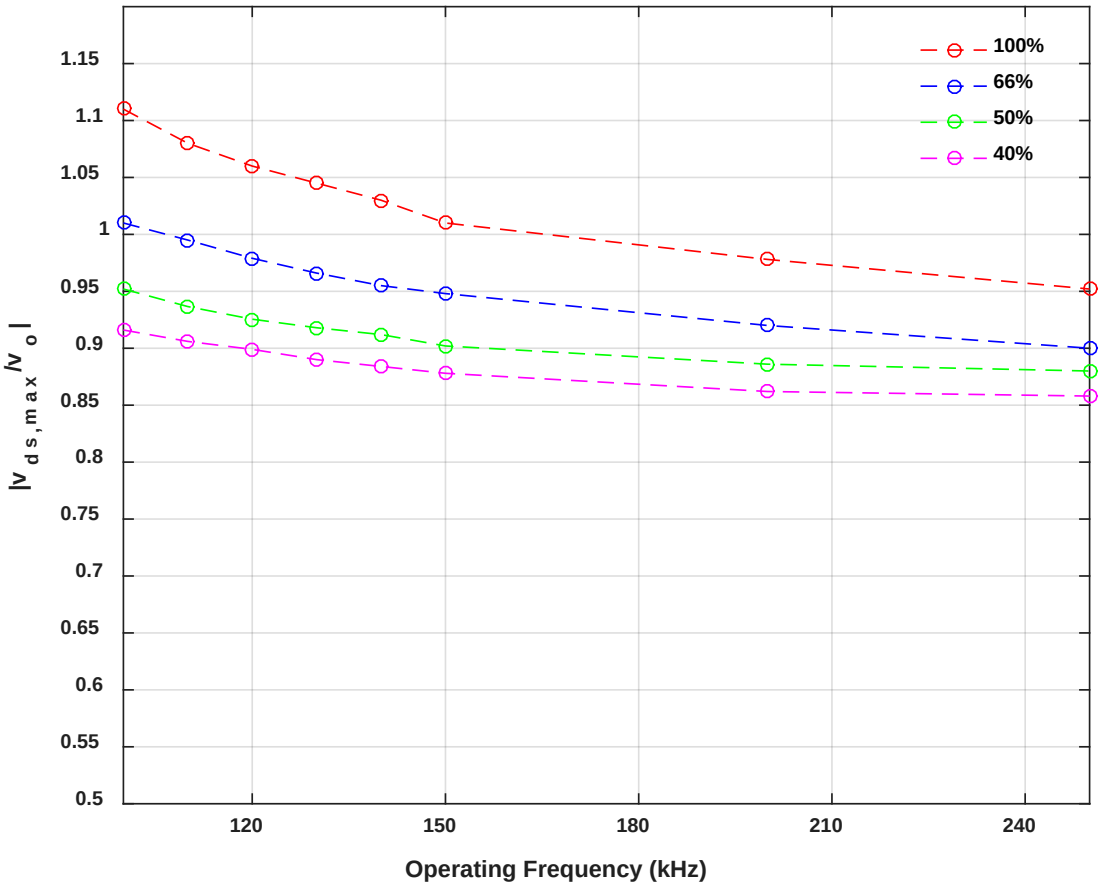


Figure 2-10: Peak switch voltage to output voltage ratio as a function of frequency for mode A at various loading conditions.

From this figure it can be seen that at smaller loading conditions the ratio between the switch voltage and the output voltage is lower. When compared to fig 2-9 it can see that all loading conditions follow the same trend which is as the frequency increases the ratio decreases.

Fig 2-11 shows the peak switch voltage to output voltage ration as a function of frequency for mode B at the same loading conditions for mode A. Once again it can be seen that the smaller the loading condition the smaller the ratio. From this it can be determined that for both operating conditions the peak switch voltage to output voltage ratio can be lowered by decreasing the loading.

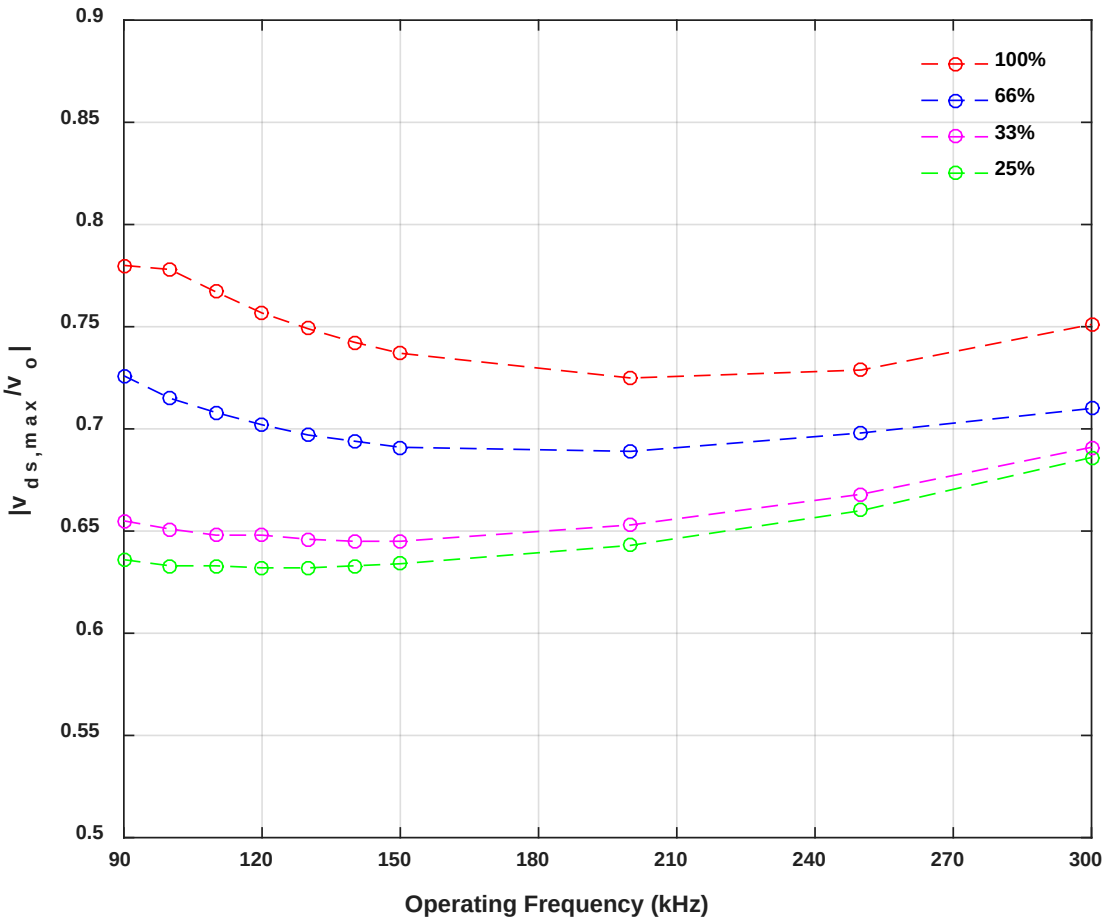


Figure 2-11: Peak switch voltage to output voltage ratio as a function of frequency for mode A at various loading conditions.

2.3.4 Switch Current Stress

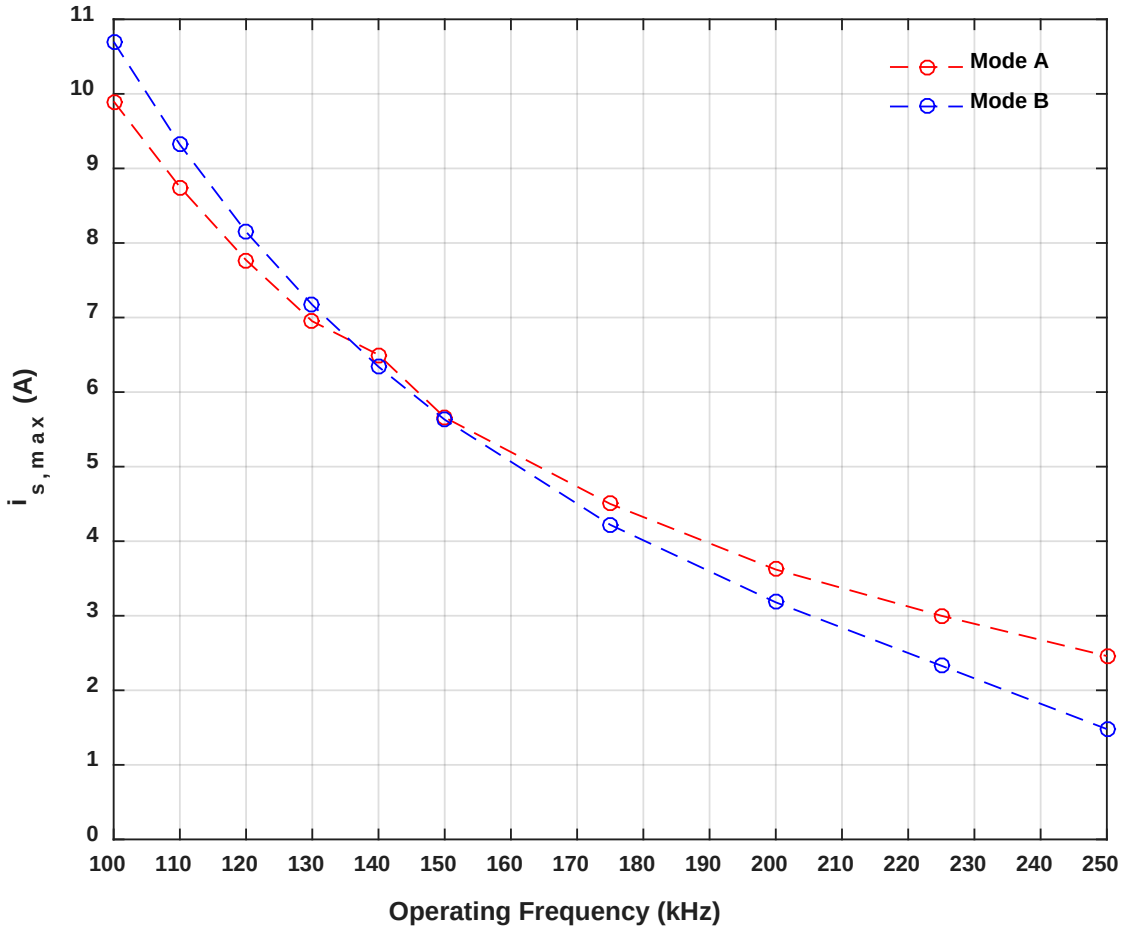


Figure 2-12: Peak switch current as a function of frequency for both mode A and mode B

The operating frequency of the proposed converter also has an impact on the peak switch current stress. Fig. 2-12 shows the stress current stress for the proposed converter as a function of the operating frequency. The red curve represents the converter operating in mode A while the blue curve represents mode B operation. It can be seen that for frequencies below 150 kHz mode B has a larger peak current stress than mode A. However for frequencies above 150 kHz mode B has a lower peak current stress and the gap continues to increase as the frequency continues to increase.

As previously mentioned in section 2.2 in order to maintain ZVS operation for the proposed circuit the gate signal must be applied to the switch after the resonant capacitor has completely discharged but before the current through the switch becomes positive. As a result there is a range for the switch's duty cycle where ZVS operation is achieved. The control variable of the circuit used for maximum power point operation is the operating frequency. If the operating frequency of the converter is changed there is a chance for ZVS operation to be lost. In order to address the issue duty cycle of the switch can be controlled in order to maintain ZVS operation.

Table 2-2: Duty cycle range that achieves soft switching operation per frequency for Mode A

Frequency (kHz)	**Duty Cycle (%)**
100	63.3 to 87.7
125	58.3 to 84.5
150	54.2 to 80.1
175	49.9 to 75.9
200	46.5 to 71.8
225	42.3 to 66.4
250	38.5 to 61.6
275	35.5 to 56.1
300	32.3 to 50.2

Table 2-3: Duty cycle range that achieves soft switching operation per frequency for Mode B

Frequency (kHz)	**Duty Cycle (%)**
100	59.8 to 80.2
125	56.1 to 75.0
150	53.6 to 70.7
175	49.8 to 66.2
200	45.3 to 61.6
225	42.0 to 56.7
250	37.0 to 50.0
275	31.8 to 42.0
300	26.2 to 29.2

2.3.5 Switch Voltage Stress

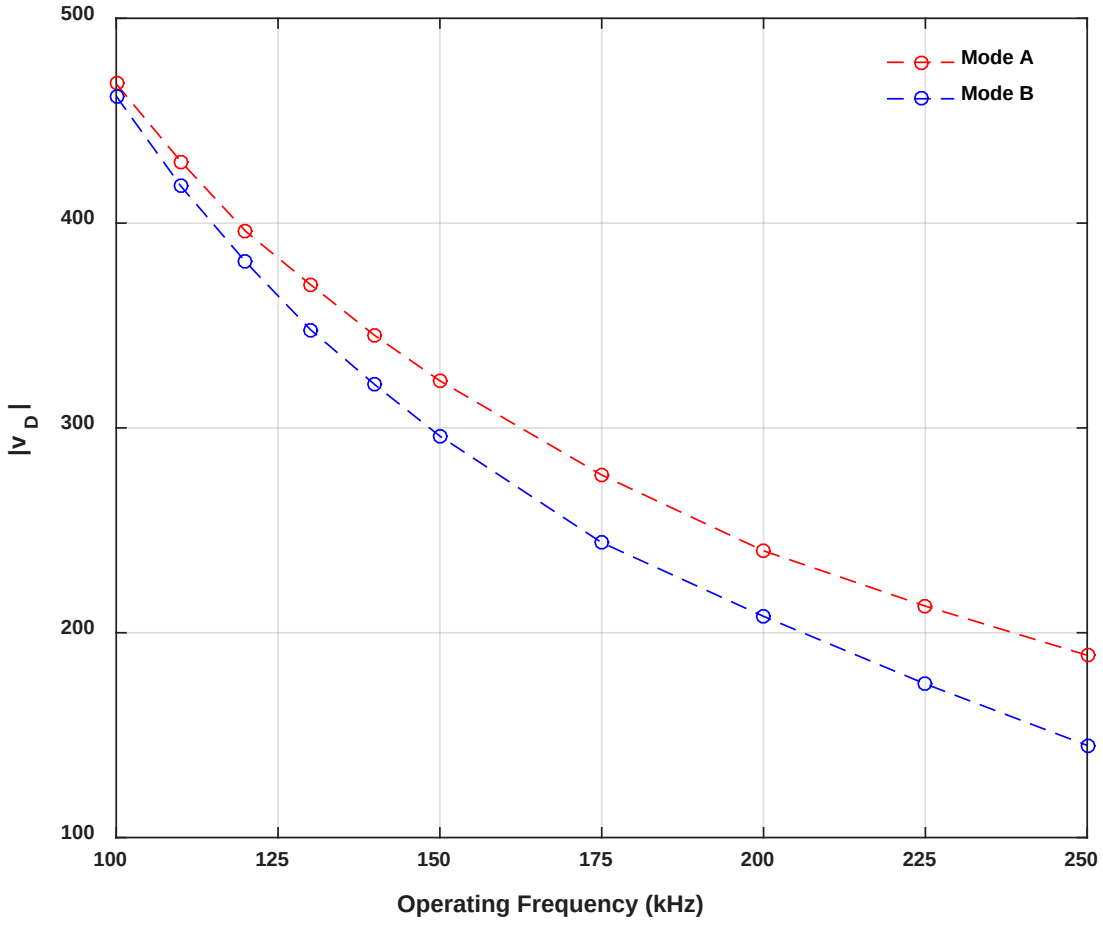


Figure 2-13: Peak diode voltage as a function of frequency for both mode A and mode B

As with the peak switch voltage and current the peak diode voltage of the proposed converter also varies with the frequency. From fig 2-4 and 2-6 it can be seen that the peak diode voltage occurs during stage IV which is when the switch is on and the secondary winding is disconnected from the circuit. By applying KVL to the proposed converter for the loop containing the input capacitor, input inductor, diode, secondary winding, and the load the equation governing the diode voltage for all stages can be determined. This relationship is provided in equation 2-54

$$v_D = v_p\left(n_2 - n_3\right) + \left(v_o - v_i\right) \qquad \text{(Eq. 2-54)}$$

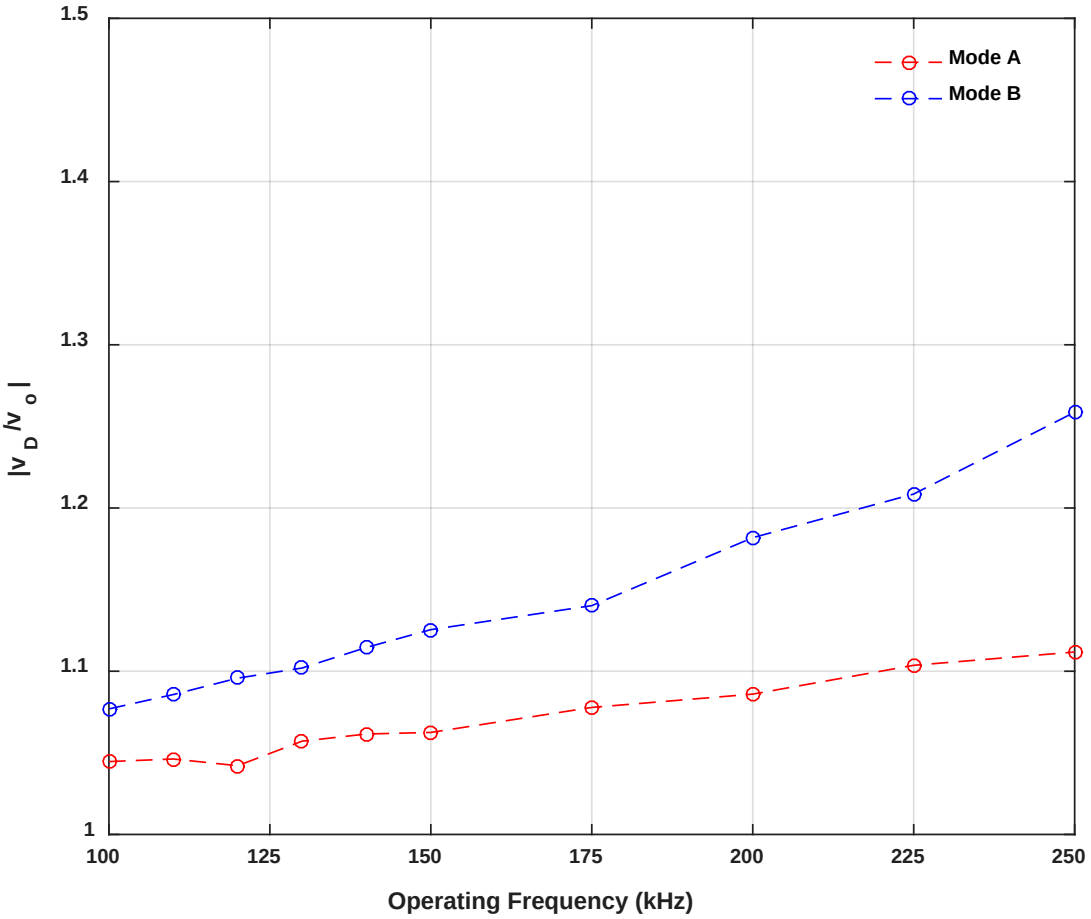


Figure 2-14: Ratio between the peak diode voltage and output voltage as a function of frequency for both mode A and mode B

Fig 2-13 and 2-14 respectively show the peak diode voltage as well as the ratio between this voltage and the output voltage. From here it can be seen that the diode voltage is greater than the output voltage however the ratio is not large. As the frequency increases this ratio also increases which is the opposite of what happens to the switch voltage to output voltage ratio. It can also be seen that the ratio is larger when the circuit operates in mode B than in mode A.

2.4 Summary

Chapter 2 introduces the proposed single switch quasi-resonant coupled inductor based step-up DC/DC converter. Operating stages for the two modes of operation are discussed in detail with equation provided. Theoretical analysis based on the circuit parameters are also discussed to highlight the similarities and differences between the two modes of operation.

3. MPPT Control Scheme for Proposed Converter

3.1 Theory

Based on the maximum power tracking techniques described in section 1.5 the method chosen to be implemented with the proposed controller was a modified perturb and observe. This is because the P&O method is the easiest to implement while maintaining ZVS operation for the circuit. In the case of incremental conductance integrals are required while for fuzzy logic several additional linguistic variables are required which increases the complexity of the controller.

One drawback of the basic P&O method is that the circuit will never operate at the maximum power point (MPP). Instead it will oscillate around it with this oscillations being a function of the control variable step size. As a result the controller has a small control variable step size to minimize the oscillation but due to this the controller takes longer to reach the best operating point when the light intensity changes. In order to overcome this drawback the modified P&O controller would check to see if the input power has changed by less than a specified amount (γ) compared to the previous cycle. If this is the case then the circuit is operating very close to the MPP and will no longer change the control variable. As the size of the control variable is no longer an issue the controller no longer needs to have a small step size and instead can change it based on the operating condition.

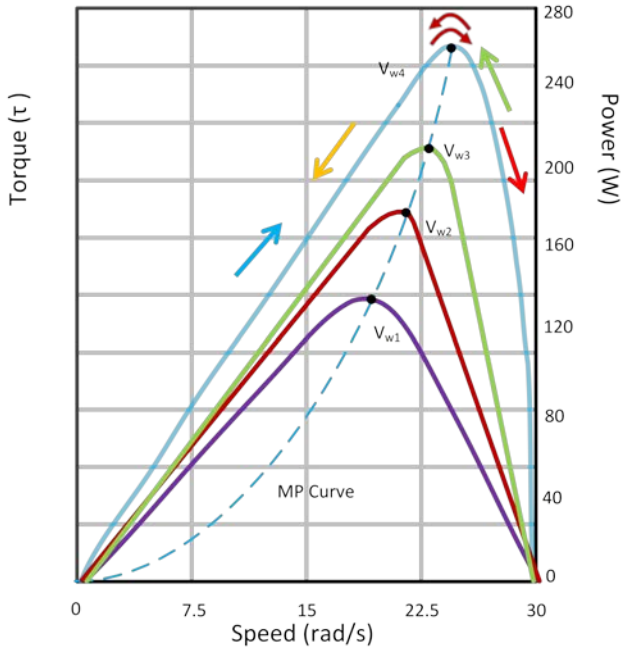


Figure 3-1: Voltage-power curve and MPP curve for different light intensities

Table 3-1: MPP tracking scenarios for the modified P&O method

Case #	Change in Power	Change in Voltage	Frequency
1	↑	↑	↓
2	↑	↓	↑
3	↓	↓	↓
4	↓	↑	↑
5	< γ	↑ or ↓	No change

3.2 Logic

The modified P&O method consists of five scenarios which are dependent on the change in power with respect to the previous iteration and the location of the panels operating point. These cases are shown in both fig. 3-1 and table 3-1. In the case of the proposed quasi-resonant converter the operating point of the input panel can be varied by controlling the converter's frequency The operating voltage and frequency of the converter's switch are inversely proportional, which implies that when the operating frequency increases the operating voltage decreases. We can use this relationship to estimate the current operating location of the panel and the direction of the MPP. If the operating voltage and the output power have increased compared to the previous iteration we know that the panel is operating to the left of the MPP and the direction of perturbation is correct. This is shown in Case 1 located in table 3-1 as well as with the blue arrow in fig. 3-1 However, if both the operating voltage and the output power decreased then the direction of perturbation is incorrect and needs to be reversed. To correct this, the

frequency must be decreased as shown in Case 3. As previously mentioned to minimize the ripple around the MPP the controller checks to see if the change in power is less than γ and in that case the controller halts the frequency variation. This is shown in Case 5.

Fig 3-2 shows a flowchart depicting how the modified P&O MPPT controller operates. The controller first obtains the operating parameters which are the panel voltage and current. Then from here the controller calculates the new operating power using equation 3-1 where *k* denotes the current operating state. The controller then calculates the change in power and voltage from the previous state using equations 3-2 and 3-3 respectively.

$$P(k) = v(k) \times i(k) \quad \text{(Eq. 3-1)}$$

$$\Delta P = P(k) - P(k-1) \quad \text{(Eq. 3-2)}$$

$$\Delta v = v(k) - v(k-1) \quad \text{(Eq. 3-3)}$$

Now that the change in power has been calculated the controller checks to see if the change in power is less than γ to see if the circuit is operating close to the MPP as shown in equation 3-4. If this is not the case the controller proceeds to determine how the control variable must be perturbed such that the circuit can reach the MPP. This is achieved by checking the polarity of the power and voltage change which was obtained previously through equation 3-2 and 3-3.

$$\Delta P \leq \gamma \quad \text{(Eq. 3-4)}$$

$$d(k) = d(k-1) \pm \delta \quad \text{(Eq. 3-5)}$$

Once this has been determined the controller will either increase or decrease the control variable as given in equation 3-5. From here the values for the power and voltage from this iteration are stored as shown in equation 3-6 and 3-7 respectively. One issue is that the controller operates at a much higher frequency compared to the converter. As a result a delay must be implemented such that the power/voltage check stage is done once every converter cycle. This is implemented through the use of a counter. The controller enters a separate loop which counts how many cycles have passed until the control variable needs to be changed again. This can be seen in the top right of fig 3-2.

$$P(k-1) = P(k) \quad \text{(Eq. 3-6)}$$

$$v(k-1) = v(k) \quad \text{(Eq. 3-7)}$$

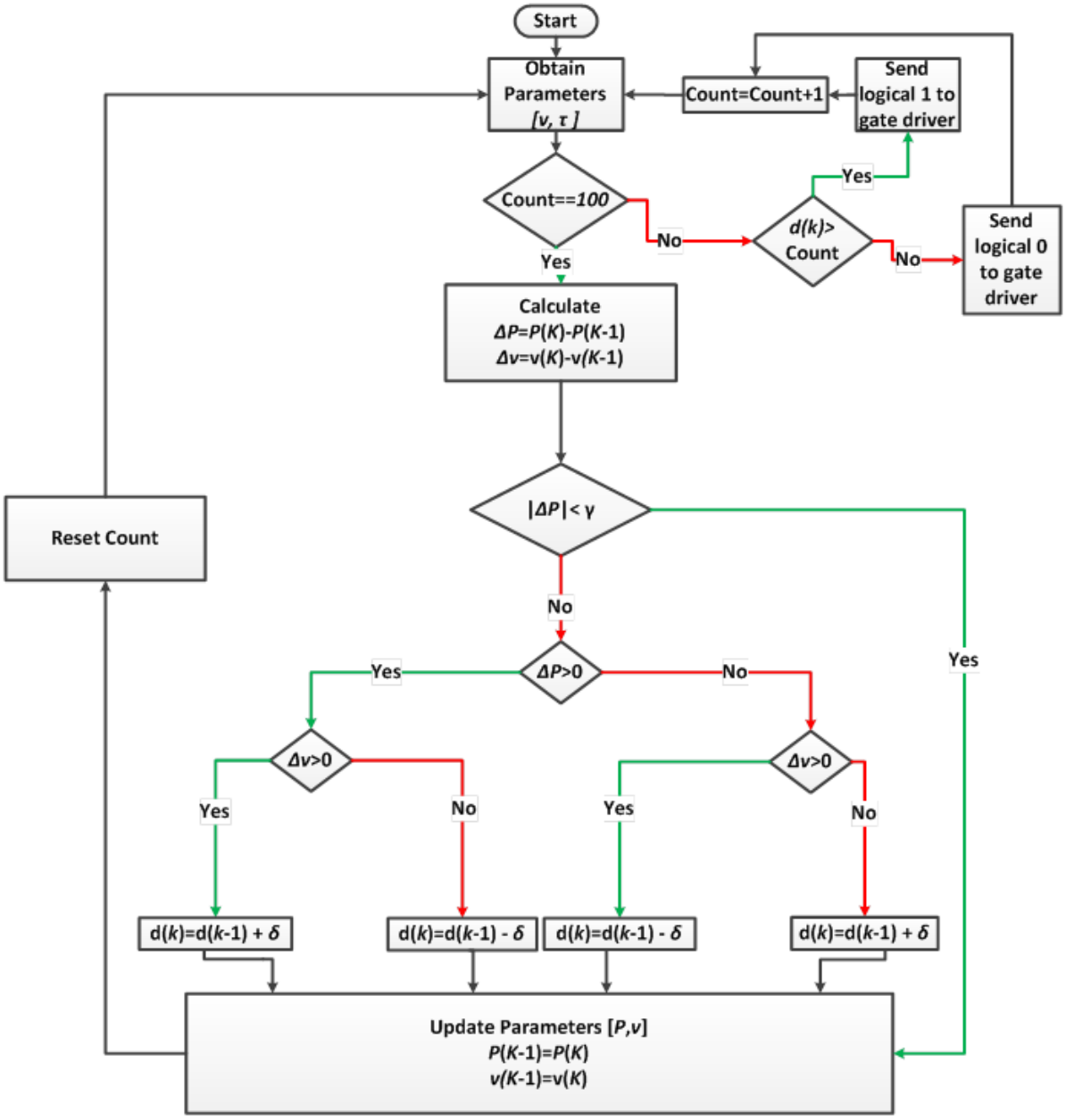


Figure 3-2: Modified Perturb and Observe maximum power point tracking controller implemented with the proposed converter.

3.3 Summary

This chapter presented the maximum power point tracking control scheme to be implemented with the proposed quasi-resonant DC/DC converter. The chosen control scheme was based off the perturb and observe control scheme discussed in section 1.5. This scheme was modified to reduce the oscillation around the maximum power point while still being able to accurately track maximum power point operation for various light intensities through the use of variable frequency control. A flowchart of the maximum power point tracking controller has been provided to illustrate its operation.

4. Design and Performance of the Proposed Converter

4.1 Introduction

In this chapter the proposed converter is tested through the use of simulation software and with a proof-of-concept prototype for both mode A and mode B. The performances of both modes are tested to confirm whether they can obtain an output voltage of 380V. At the same time as the circuit is tested to see if it operates under continuous conduction mode and utilizes soft switching. Both modes of operation are also tested with the designed controller to confirm that maximum power point operation can be achieved at several irradiation conditions while maintaining soft switching operation at various frequencies.

The equations that govern the operating stages of the proposed converter discussed in section 2.2 are then plotted in MATLAB and compared to the results obtained with the circuit simulation software to confirm the validity.

This chapter will also present a laboratory scale proof-of-concept hardware prototype. Using this prototype, both mode A and mode B will be tested for 380V operating to show the feasibility of the system. The prototype will also be tested for maximum power point tracking functionality through the use of a solar panel emulator and a micro-controller. The converters operating waveforms will be provided to highlight the functionality and features of the system.

4.2 Design Specifications

To verify the validity of the proposed converter both mode A and mode B need to be tested. The gain of both circuit are different and as a result to maintain 380V at the output both modes need to operate at different frequencies. Although both operating modes consist of the same components, the component values are different. Table 4-1 contains the component values for the (A) operating stage while table 4-2 contains the component values for the (B) operating stage.

Table 4-1: Mode A component values

Parameter	Component Value
Input Voltage	35V
Rated Power	75W
Output Voltage	380V
Input Capacitor	10 µF
Output Capacitor	10 µF
Resonant Capacitor	13 nF
Input Inductor	48 µH
Resonant Inductor	4.7 µH
Primary Winding Magnetizing Inductance	45 µH
Primary Turns	2
Secondary Turns	8
Tertiary Turns	4
Operating Frequency	120kHz
Duty cycle	70%

Table 4-2: Mode B component values

Parameter	Component Value
Input Voltage	35V
Rated Power	75W
Output Voltage	380V
Input Capacitor	10 µF
Output Capacitor	10 µF
Resonant Capacitor	20 nF
Input Inductor	100 µH
Resonant Inductor	1.5 µH
Primary Winding Magnetizing Inductance	45 µH
Primary Turns	2
Secondary Turns	8
Tertiary Turns	4
Operating Frequency	100kHz
Duty Cycle	70%

In the case of the component values shown in table 4-1 and 4-2 only the ideal components are shown. However, to mimic a real life scenario the non-ideal parameters such as the inductor resistance, diode forward voltage, and the switch on resistance were also used in PSIM. Some of these parameters were obtained from the components datasheet while others such as the transformer leakage inductance were measured. These values are shown in table 4-3.

Table 4-3: Non-ideal parameters

Parameter	**Component Value**
Input Inductor resistance	16 mΩ
Resonant Inductor resistance	17 mΩ
Primary Winding Leakage Inductance	1.3 µH
Secondary Winding Leakage Inductance	0.38 µH
Tertiary Winding Leakage Inductance	1.0 µH
Primary Winding Resistance	19 mΩ
Secondary Winding Resistance	3 mΩ
Tertiary Winding Resistance	8 mΩ
Diode Foward Voltage	1.25 V
Diode Resistance	300 mΩ
Switch On Resistance	80 mΩ
Switch Diode Forward Voltage	0.9V
Switch Diode Resistance	300 mΩ
Switch Output Capacitance	37 pF

4.3 Powersim

The circuit simulation software Powersim (PSIM) was used to test the validity of both modes of operation. The circuit consisted of a voltage source attached to the proposed converter as shown in the appendix. The voltage source was chosen to provide 35V at the input of the circuit while the frequency of the converters switch (*S*) was chosen such that the required output voltage of 380V could be achieved. The duty cycle of the converters switch was chosen such that zero-voltage switching would be achieved. The frequency and duty cycle were implemented through the use of a square wave voltage source. In the case where maximum power point tracking (MPPT) operation is to be achieved, the input voltage source was replaced with a solar panel. This solar panel was designed through the use of the "solar panel physical model" in PSIM. Various parameters were obtained from a chosen solar panel's datasheet in order to re-create the panel's power-voltage and current voltage curves such that the panel can be accurately recreated in simulation. To achieve maximum power point tracking the controller previously discussed in section 3.3 was integrated with the proposed circuit. This is done by feeding in the converters input voltage (v_i) and current (i_i) into the controller and having its output connected to the gate of the switch. As the controller is now being utilized, the operating frequency and duty cycle are no longer constant and the square wave voltage source has also been removed.

4.31 Results: Mode A 380V Operation

To achieve an output voltage of 380V the circuit under mode A was operated at a frequency of 120kHz with a duty cycle of 60%. The duty cycle was chosen such that the switch would operate under soft-switching condition. Fig. 4-1 (a) shows the output voltage (v_o) and switch voltage (v_{ds}) at this operating condition with the switch voltage shown in blue and the output voltage shown in red. From here it can be seen that the circuit is able to step-up the input voltage from 35V to 380V when operating at the given condition. v_{ds} is also seen to be just slightly higher than v_o. The peak switch voltage at this operating condition was 380V which gives a peak switch voltage to output voltage ratio of 1:05:1.

Fig. 4-1 (b) shows the switch current (i_s) shown in orange and the resonant inductor current (i_{Lr}) in green. It could be observed that for most of the time the switch current and the resonant inductor current are the same. At one point the switch current drops to zero while the resonant inductor current does not. This represents the beginning of stage I of mode A as the gain signal has been removed from the switch. The peak switch current is approximately 7.7A at this operating condition.

Fig. 4-1(c) shows the i_{Lr} in green and the resonant capacitor current (i_{cr}) in magenta. From this it can be understood that when the gate signal is removed from the switch the current is redirected into the resonant capacitor, confirming what has been said in regarding stage I in section 2.2. During the time when the gate signal is applied to the switch (S) the current flowing through the resonant inductor (L_r) and S are the same however when S is off the current is redirected to the resonant capacitor (C_r).

For soft switching to occur the switch voltage must be zero before the switch current is positive and the gate signal must be applied before the current becomes positive. By comparing fig. 4-1(a) and (b) it can be seen that the when the switch voltage has reached zero the current is negative. This means the current is flowing through the anti-parallel diode of the switch. A small spike can be seen in the switch current waveform. This is an indicator of when the gate signal has been applied. From here it is understood that the gate signal was applied before the switch current became positive and as a result soft switching has been achieved.

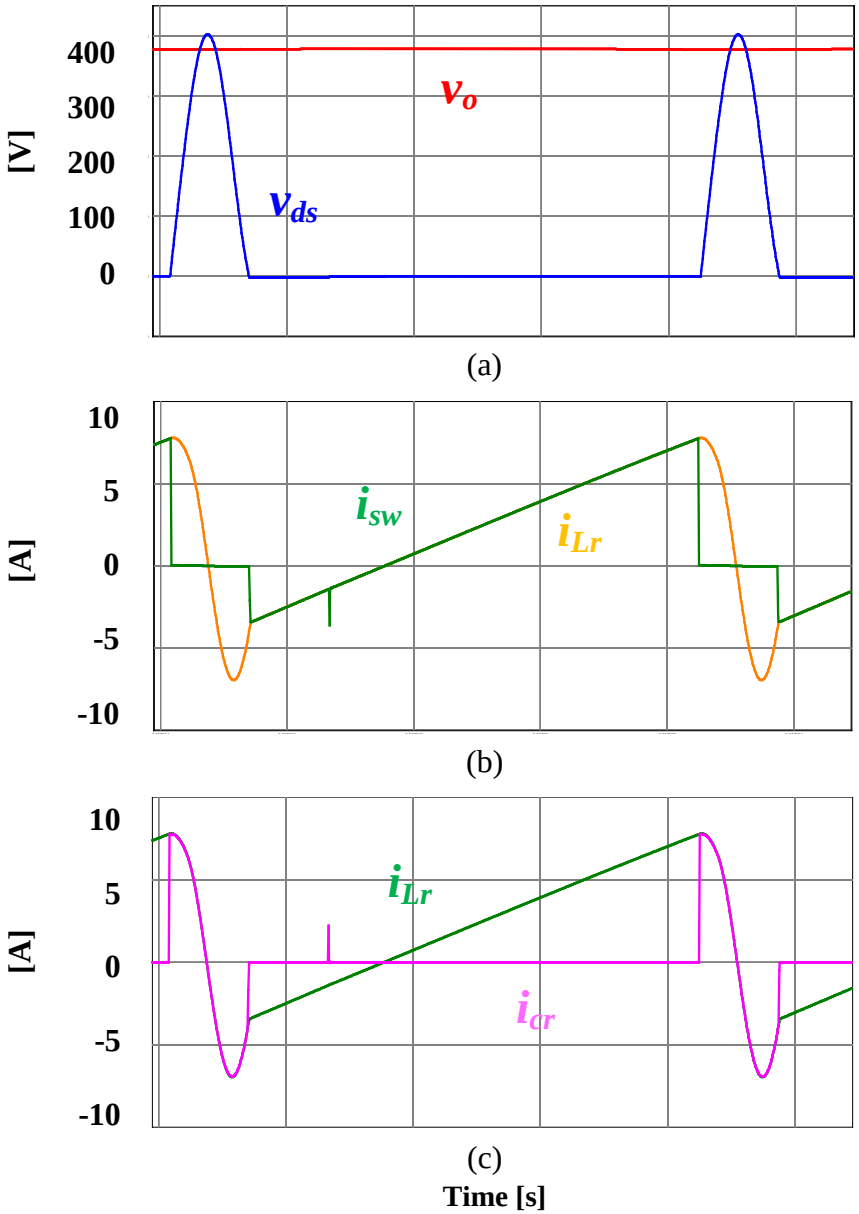


Figure 4-1: Mode A simulation waveforms: (a) Output voltage and switch voltage, (b) resonant inductor current and switch current, (c) resonant inductor current and resonant capacitor current

Fig. 4-2 (a) shows the voltage waveform across the secondary winding diode (D_1) in red as well as the output voltage in blue. From here it can be stated that the maximum voltage across the diode is almost the same as the peak switch voltage. Comparing fig. 4-1 (a) and (b) it can be seen that the diode voltage begins to decrease once the gate signal is removed from the switch and the resonant capacitor starts to charge. As mentioned in section 2.2, once the diode voltage reaches zero the converter enters stage II. This change in the switch voltage waveform and resonant inductor current waveform confirms this.

Fig. 4-2 (b) shows the diode current waveform in red. Two information's that can be perceived from this waveform is that the diode current begins to increase after the diode voltage has reached zero and this current reaches zero before the voltage begins to increase. This implies that soft-switching is also achieved for the diode. When comparing this figure to Fig. 4-1 (a), the switch voltage reaches zero before the diode current reaches zero. This indicates the transition between stage II and stage III of mode A. However in this case the diode current is almost zero which indicates the duration of stage III is very short.

One benefit of the proposed converter was that it would not require an electrolytic capacitor at the input of the circuit due to the fact that the converter operates in continuous conduction mode. Fig. 4-2 (c) shows the current through the input capacitor. From here it can be understood that the minimum input capacitor current is greater than zero which confirms the converter is operating in continuous conduction mode. This figure shows that during stages I and II the input current is increasing while in stages III and IV the input current is decreasing. This represents the charging and discharging of the input inductor.

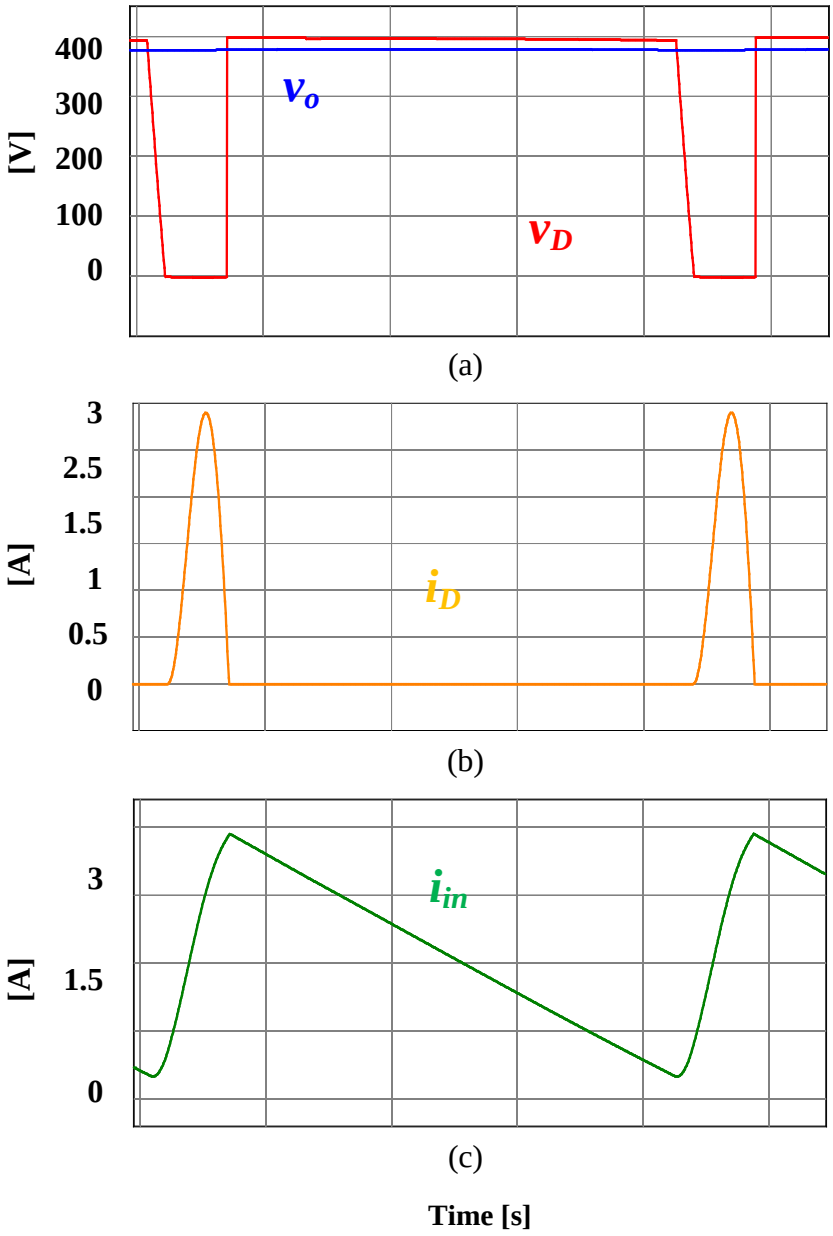


Figure 4-2: Mode A simulation waveforms: (a) Output voltage and diode voltage, (b) diode current, (c) input current

4.32 Results: Mode B 380V Operation

The previous simulation results were for mode A operation. Mode B operation was also tested in simulation through the use of PSIM. In order to achieve an output voltage of 380V the converter was operated at a frequency of 100kHz and a duty cycle of 70% was employed to ensure ZVS operation. Fig 4-3 (a) shows the output voltage (v_o) and switch voltage (v_{ds}) at this operating condition with the switch voltage shown in blue and the output voltage shown in red. Like mode A, this mode of operation is also able to step-up the voltage from 35V to greater than 380V. In this case the peak switch voltage stress is much less than the output voltage. At this operating condition the peak switch voltage is 300V which results in a ratio of 0.75:1 which is much less than the ratio for mode A.

Once again soft switching operation is achieved in the converter as shown in Fig. 4-3 (b), which contains the switch current (i_s) shown in green and the resonant inductor current (i_L) in orange. The switch voltage has reached zero and the gate signal is applied before the switch current becomes positive. The peak switch current value in mode B was found to be 9.7A while with mode A the peak switch voltage from fig. 4-1 (b) was 7.7A. This confirms that the proposed converter has a higher peak switch current while operating in mode B compared to mode A. It can be seen that there is an abrupt change in the resonant inductor current at one point when the current is negative. This shows the transition state from stage II to stage III as the diode has turned off and the equations that governed the current has changed. This can also be seen in fig. (a) as the switch voltage begins to decreases at a lower rate.

Fig. 4-3 (c) shows the resonant inductor and resonant capacitor current waveforms shown in red and magenta respectively. When comparing these waveforms to fig. 4-3 (b), it can be seen that

the when the gate signal is removed from the switch the current flowing through the switch is redirected to the resonant capacitor. The duration of stage III can also be seen as the start is represented by the change in the resonant inductor current and the end is represented by the resonant capacitor current changing to 0.

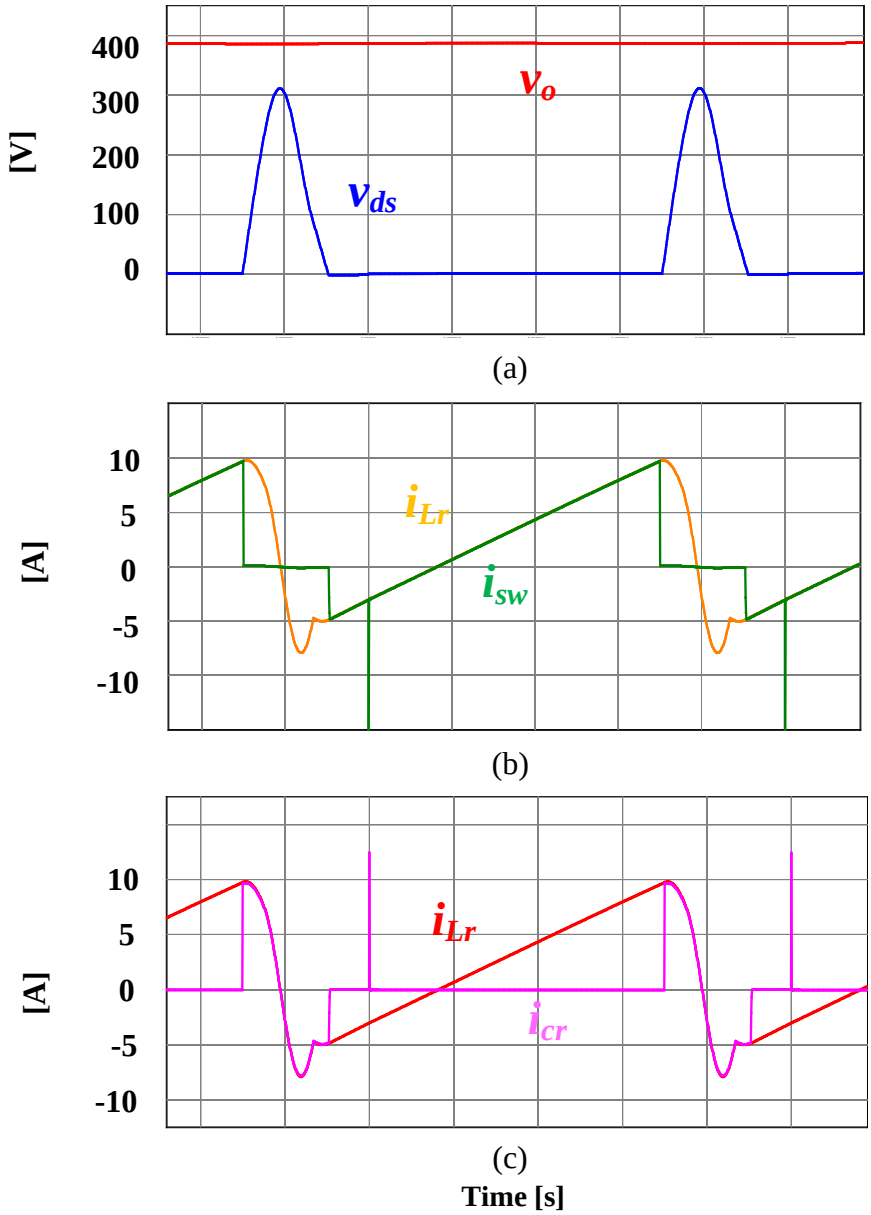


Figure 4-3: Mode B simulation waveforms: (a) Output voltage and switch voltage, (b) resonant inductor current and switch current, (c) resonant inductor current and resonant capacitor current

Fig 4-4 (a) shows the voltage waveform across the secondary winding diode (D_1). Unlike mode A, the diode voltage stress and the peak switch voltage stress are not about the same value. For mode B the diode voltage stress is slightly greater than the output voltage. This coincides with the equation 2-54 provided in section 2.3 as the diode voltage stress is a function of the output voltage. It can also be seen that the diode voltage does not immediately proceed from 0 to its maximum when the diode turns off. Instead there is a jump to a lower value followed by a gradual increase towards the maximum.

Fig. 4-4 (b) shows the current waveform across the secondary winding diode (D_1). Once again it can be seen that soft switching operation is achieved for D_1 as the voltage is zero before the current increases and the current is zero before the voltage begins to increase. At the point when the current reaches zero it can be seen in fig. 4-3 (a) that the rate at which the switch voltage decreases has been reduced. This shows the transition from stage II to stage III for mode B. This can also be confirmed from the current waveform in fig. 4-3 (b) as when the current through D_1 reaches zero the converter transitions from stage II to stage III.

Fig. 4-4 (c) shows the current through the input inductor. As with mode A, it can once again be seen that the minimum input inductor current is greater than zero. This confirms that the converter is operating in continuous conduction mode during mode B as well. This figure shows that during stages I and II the input current is increasing while in stages III and IV the input current is decreasing. This represents the charging and discharging of the input inductor.

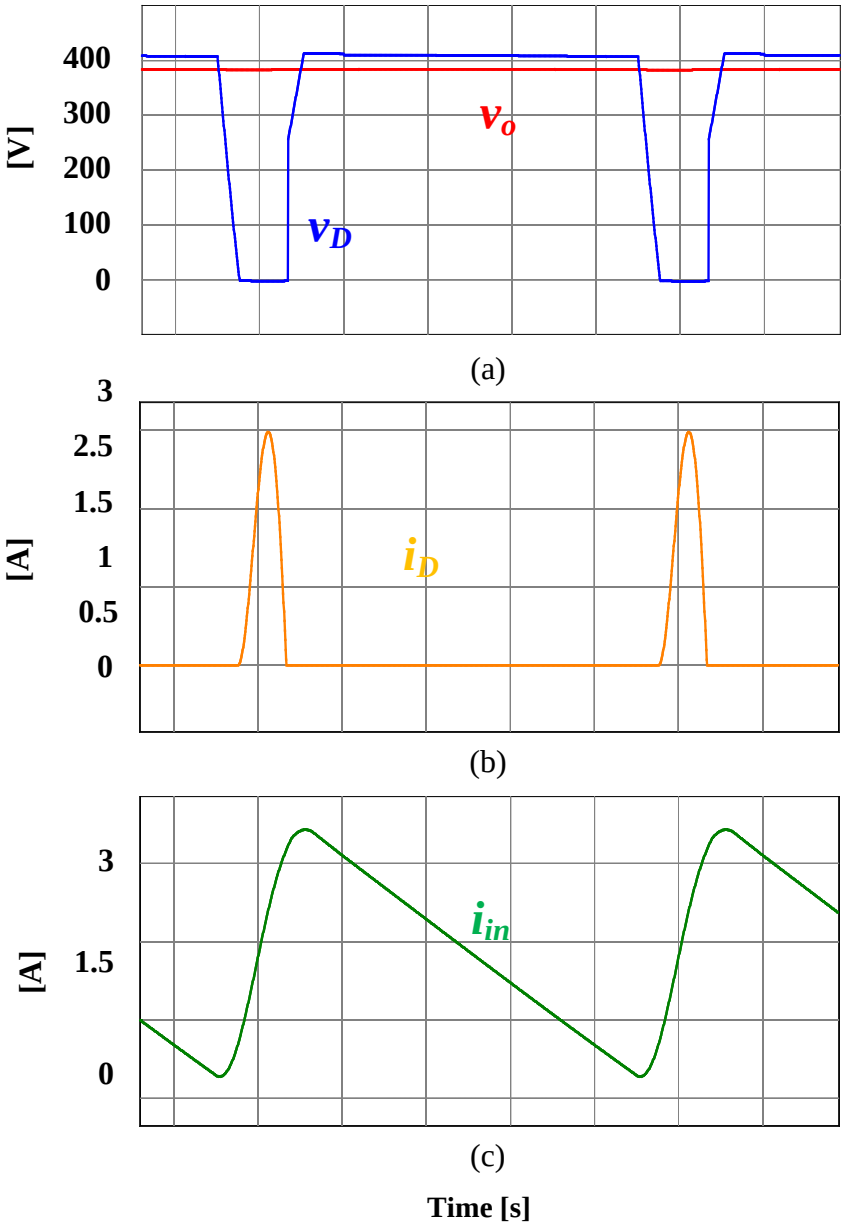


Figure 4-4: Mode B simulation waveforms: Output voltage and diode voltage, (b) diode current, (c) input current

4.33 Results: Mode A MPPT Operation

The previous simulation results dealt with the use of an input voltage source operating at 35V. However the proposed converter was designed to be connected to a solar panel. Therefore, simulation in PSIM was also performed with a solar panel at the converters input. In order to account for various atmospheric changes the light intensity of the solar panel was varied from a chosen minimum to a chosen maximum. As mentioned in section 1.5 when the light intensity varies, the optimal operating point for the system changes. Consequently the modified maximum power point tracking controller discussed in section 3 was implemented with the system.

In order to design a solar panel in PSIM various parameters such as the cell type, amount of cells, voltage and current levels, and the maximum power are required. The parameters can be obtained from a commercial solar panel's data-sheet. An ALEKO 140W solar panel was chosen to be modeled in PSIM. The required parameters obtained from the panels datasheet are located in table 4-4. The solar module (physical model) in PSIM was employed to design the solar panel. By inputting the parameters obtained from the datasheet, the simulation software would be able to design the power-voltage and current-voltage curves for the panel at various light intensities. Fig. 4-5 shows an example of the solar module (physical model). Some parameters such as the band gap energy, ideality factor, and shunt resistance are not provided in the datasheet but can be obtained through other means such as cell type. For example the band gap energy represents the minimum amount of photon energy to remove an electron from a crystalline structure. In the case of a monocrystaline panel this is 1.12 electron volts [57].

Table 4-4: Mode A component values

Parameter	Component Value
Model	ALEKO 140 Watt
Number of Cells	72
Cell type	Monocrystalline
Maximum power rating (P_{max})	140W
Open Circuit Voltage (V_{oc})	44.2V
Short Circuit Current (I_{sc})	4.0A
Voltage at maximum power point (V_{mpp})	36.1V
Current at maximum power point (I_{mpp})	3.88A

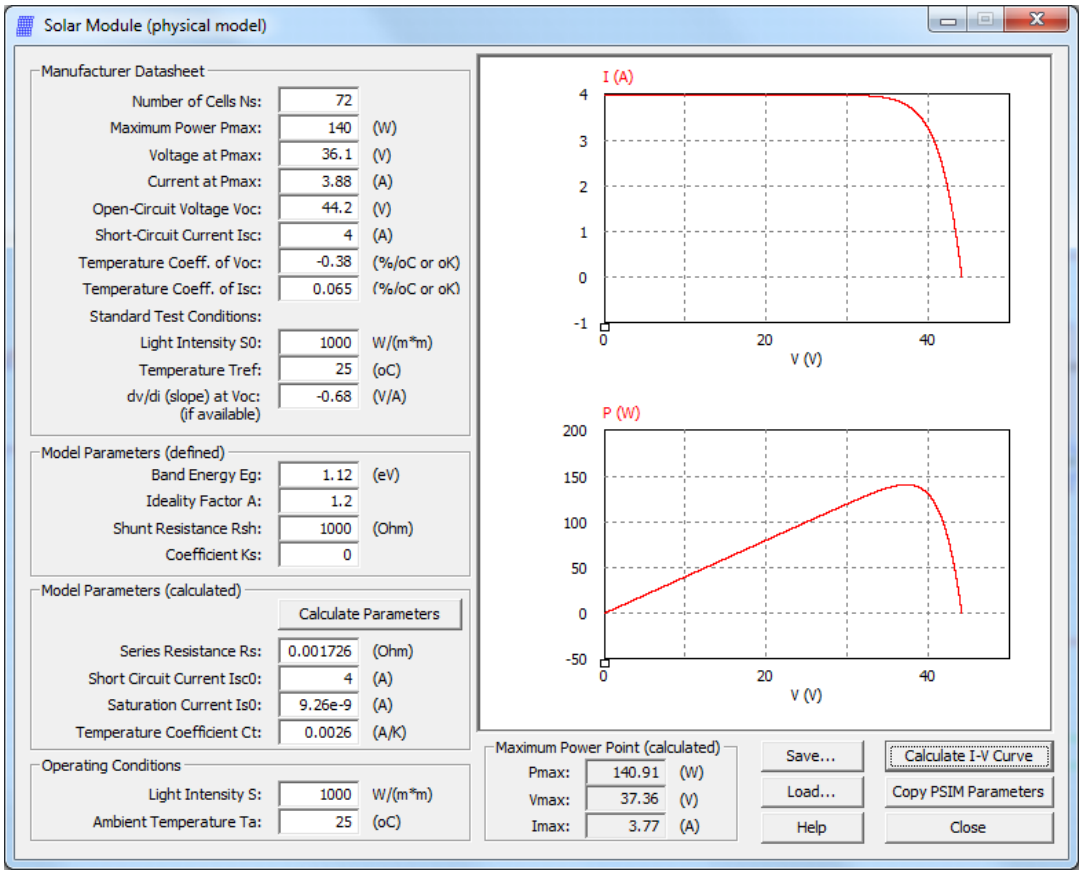


Figure 4-5: Solar Module (physical model) from PSIM

Fig. 4-6 displays the results of the system with a light intensity varying from 200W/m^2 to 700W/m^2. Fig. 4-6 (a) shows the varying light intensity while fig 4.6 (b) shows the maximum panel voltage in red and the output power of the panel in blue. From here it can be seen that the controller is able to bring the output power of the panel to its maximum. Fig. 4-7 (a) and (b) shows a zoom-in of the power waveforms for when the light intensity changes. It can be seen that the controller takes approximately 7ms to bring the output power to its maximum.

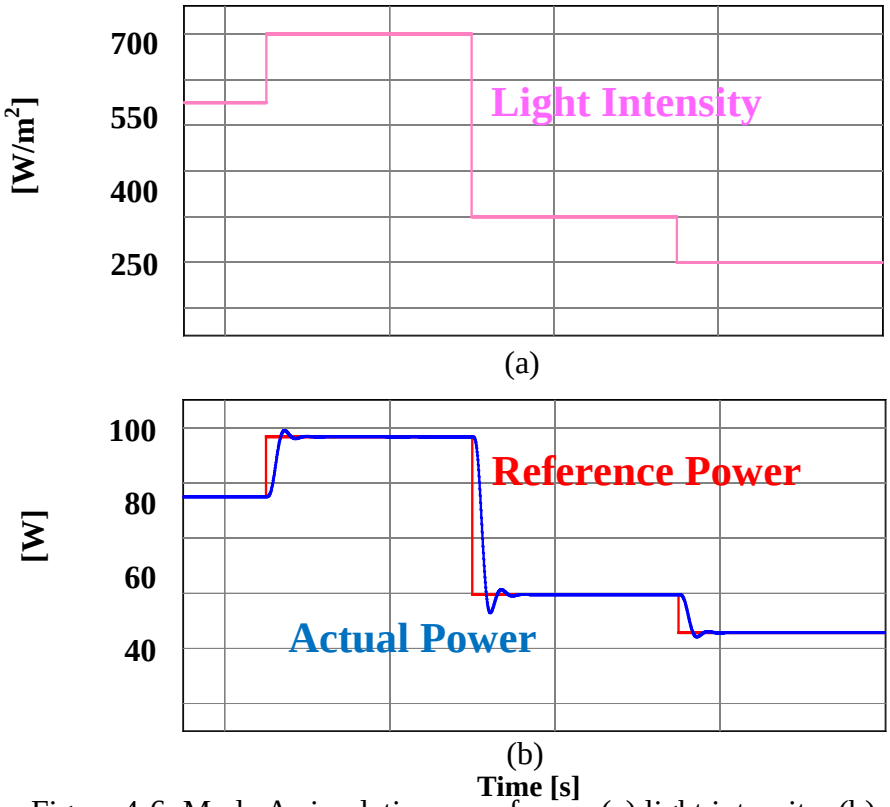


Figure 4-6: Mode A simulation waveforms: (a) light intensity, (b) maximum panel power and panel output power

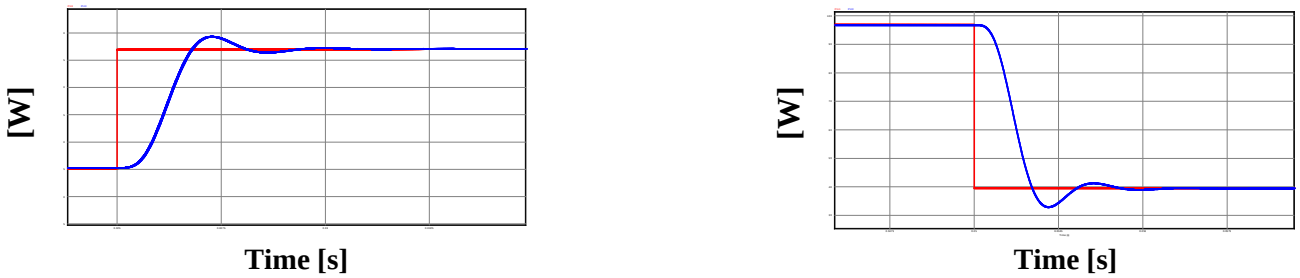


Figure 4-7: Mode A simulation waveforms: (a) Maximum power point increases, (b) maximum power point decreases

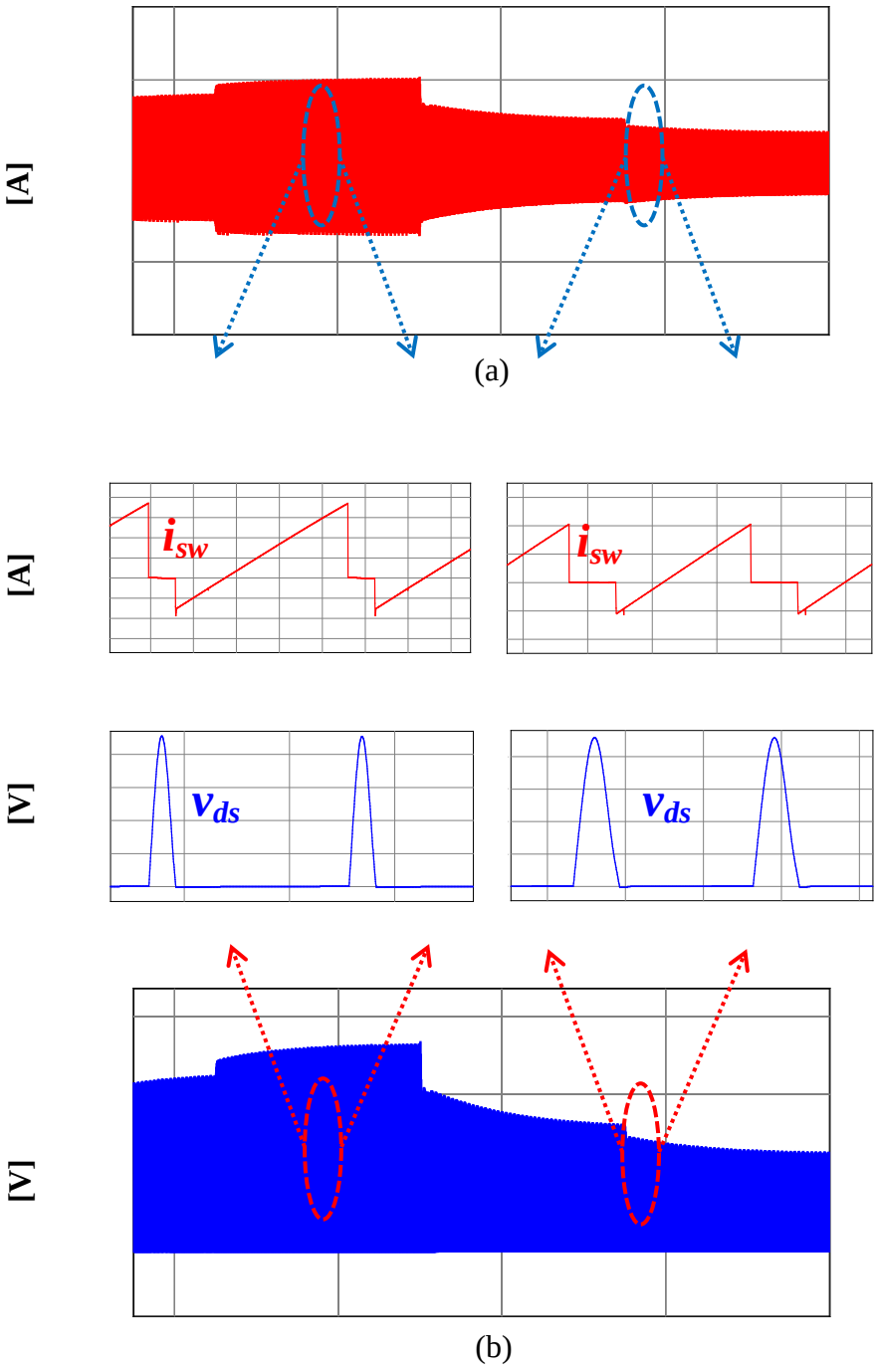


Figure 4-8: Mode A simulation waveforms: (a) Switch current waveform, (b) switch voltage waveform.

Fig. 4-8 shows switch current waveform as well as the switch voltage waveform. From these figures it can be seen that their peak values vary with the input power. It can also be seen that zvs operation is achieved at all operating conditions. When comparing the zoomed-in current waveforms it can be seen that the time period where the switch current is zero is much smaller when operating at a higher power level. The same can be seen in the zoomed in voltage waveforms. This confirms the analysis from table 2-2 and 2-3. This is because operating at a higher power level requires a lower operating frequency which in turn requires a larger duty cycle to achieve ZVS operation.

4.34 Results: Mode B MPPT Operation

Mode B was also tested for maximum power point tracking operation through PSIM. Fig. 4-9 shows displays the results of the system with a light intensity varying from 200W/m^2 to 700W/m^2 which is the same range as from the mode A results. Fig. 4-9 (a) shows the varying light intensity while fig 4.9 (b) shows the maximum panel voltage in red and the output power of the panel in blue. As with mode A, it is once again seen that the controller is able to bring the panel power by varying the frequency of the converters switch. Figure 4-10 (a) and (b) contain a zoom-in of the power waveforms for when the light intensity changes. It can be seen that the controller takes approximately 7ms to bring the output power to its maximum. As this was the same for mode A, it can be concluded that the controller operates properly with the proposed converter regardless of which mode it is operating under.

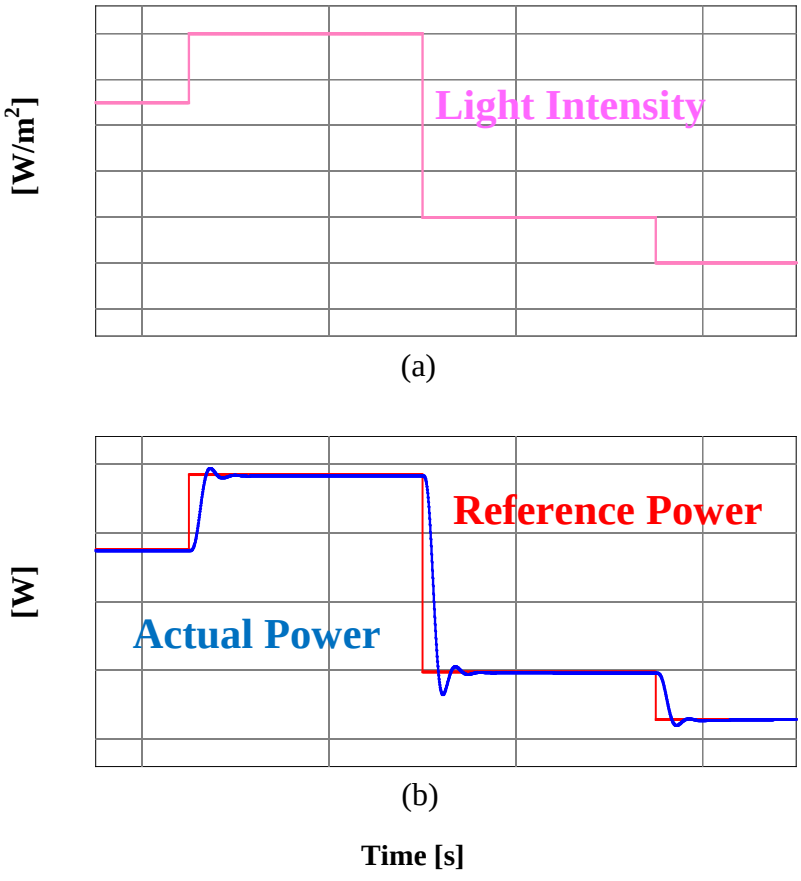


Figure 4-9: Mode B simulation waveforms: (a) Light Intensity, (b) Panel maximum power and output power.

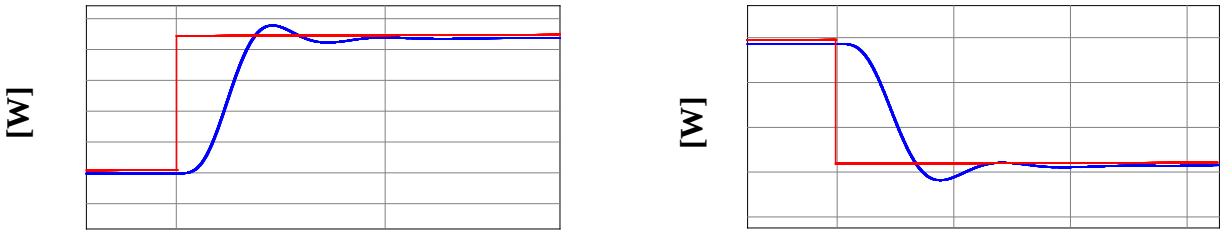


Figure 4-10: Mode B simulation waveforms: (a) Maximum power point increases, (b) maximum power point decreases

Fig. 4-11 shows switch current waveform as well as the switch voltage waveform. From these figures it can be seen that their peak values vary with the input power which is what occurred with mode A as well. ZVS operation is once again achieved at all operating conditions.

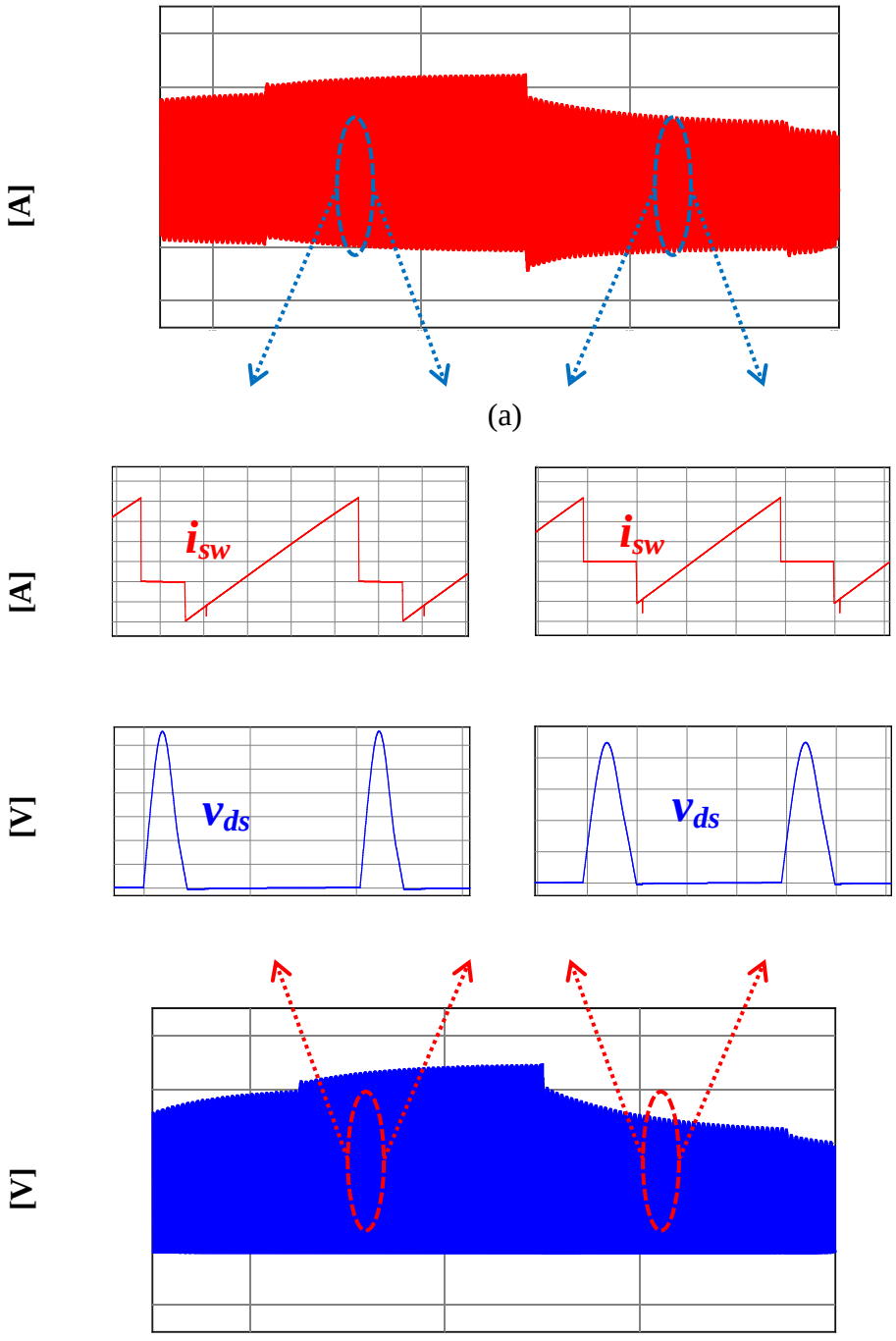


Figure 4-11: Mode B simulation waveforms: (a) Switch current waveform, (b) switch voltage waveform.

4.4 MATLAB

In section 2.2 and 2.3 the equations that govern the proposed converter for both the (A) mode and the (B) mode were discussed. In section 4.3.2 simulation results for the proposed converter were provided. In order to confirm that the equations for each operating stage are correct they can be plotted and compared to the results obtain from PSIM. To create a plot of these equations MATLAB was employed. The operating parameters of the proposed converter were obtained from table 4-1 and 4-2 such that the results would be similar to that of the simulation results from PSIM. The switch voltage waveform and the switch current waveforms were then plotted to confirm the stage equations transition correctly.

$$v_{ds} = v_i\left(1-\cos\omega_0 t\right)+i_{Lr}\left(t_0\right)L\omega_0\sin\omega_0 t \qquad \text{(Eq. 4-1)}$$

$$v_{ds} = \left(v_i - v_p\right)\left(1-\cos\omega_0 t\right)+i_{Lr}\left(t_0\right)L\omega_0\sin\omega_0 t + v_{ds}\left(t_1\right)\cos\omega_0 t \qquad \text{(Eq. 4-2)}$$

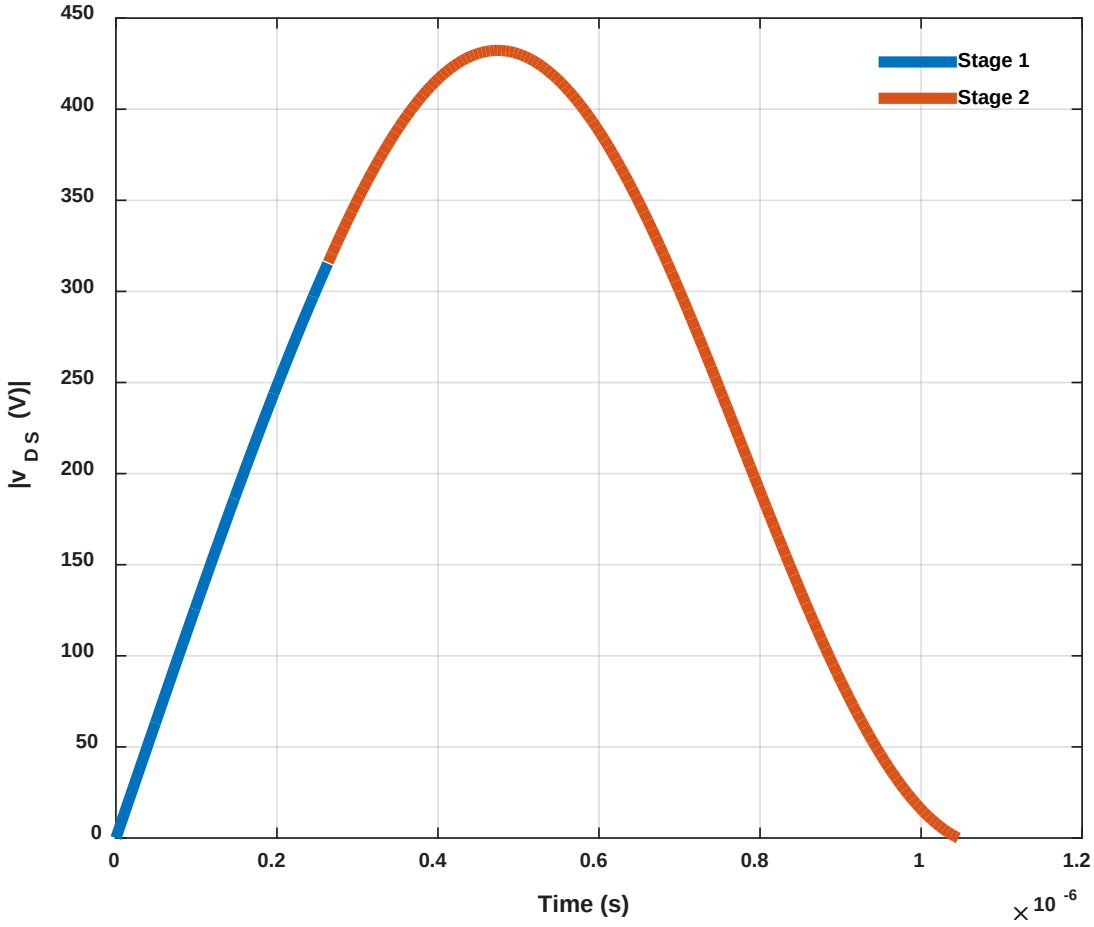


Figure 4-12: Mode A Switch Voltage for stage I (blue) and stage II (orange)

Equation 4-1 and 4-2 shows the switch voltage waveform for stages I and II respectively where *L* is a combination of several inductor parameters listed in the appendix. Through the use of MATLAB these equations were plotted using the parameters provided in table 4-2 for mode A and table 4-2 for mode B. Fig. 4-12 shows the plot of the switch voltage waveform for stage I and stage II. Here it can be seen that the equations transition correctly between stage I and stage II. It can also be seen that the maximum switch voltage is around 430V. When compared to fig

4-1 (a) it can be seen that this voltage is slightly higher than the voltage obtained in PSIM. This can be accounted for due to the fact that non-ideal components were used in PSIM while plots of the equations without accounting for losses were obtained with MATLAB.

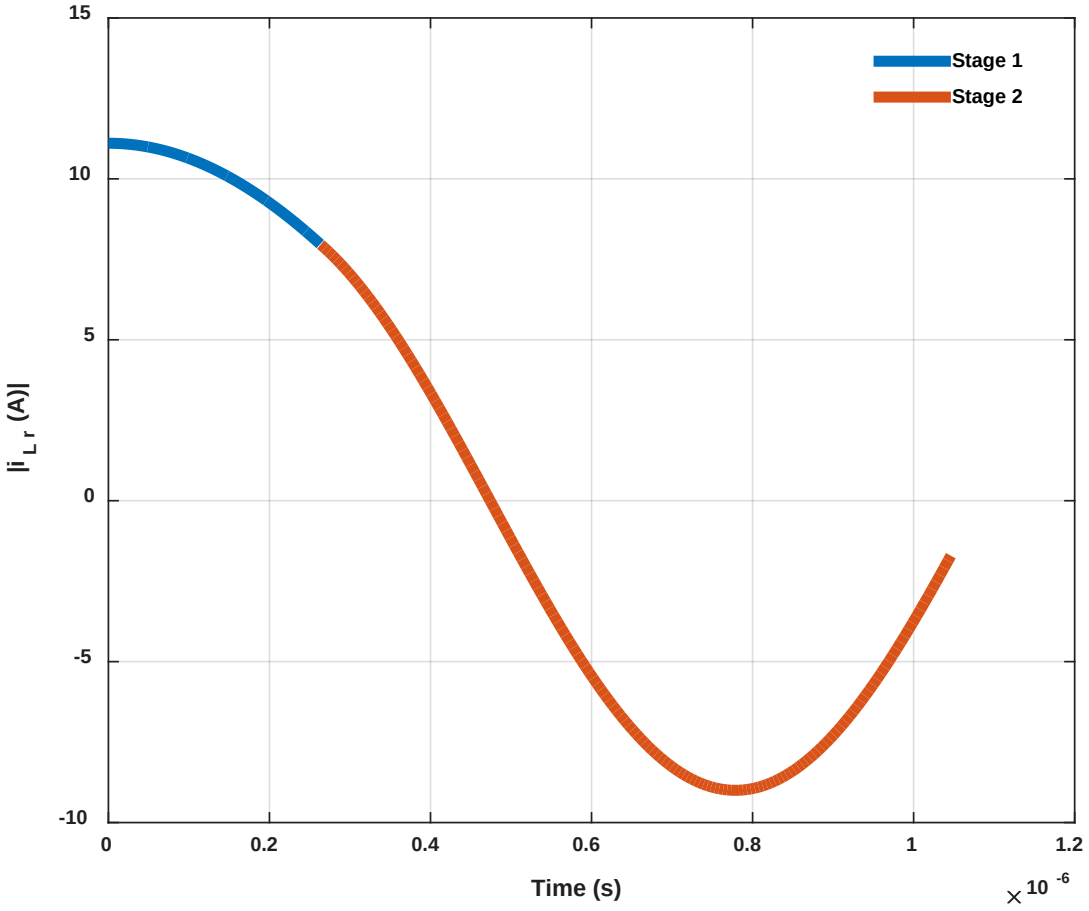


Figure 4-13: Mode A Resonant inductor Current for stage I (blue) and stage II (orange)

Fig. 4-13 shows the resonant inductor current waveform for stage I and stage II obtained by plotting equations 4-3 and 4-4 in MATLAB.

$$i_{Lr} = \frac{v_i}{Z}\sin(\omega_0 t) + i_{Lr}(t_0)\cos(\omega_0 t) \qquad \text{(Eq. 4-3)}$$

$$i_{Lr} = \frac{(v_i - v_p - v_{ds}(t_1))}{Z}\sin(\omega_0 t) + i_{Lr}(t_1)\cos(\omega_0 t) \qquad \text{(Eq. 4-4)}$$

When compared to fig. 4-12 it can be seen that the resonant inductor current reaches zero when the switch voltage reaches its max which confirms the statement about Mode A stage II in section 2.2. It can also be seen that the waveform matches that of fig 4-1 (b) and (c). From this it can be determined that the switch voltage and resonant inductor current equations are correct. Detailed steps and calculations for determining these equations are provided in the appendix.

4.5 Hardware Experiment Testing

In order to confirm the feasibility of the proposed circuit a laboratory scale proof-of-concept hardware prototype was designed. The printed circuit board (PCB) design software Altium was employed to create a PCB of the proposed converter to be printed. The footprints of the converter's components were designed based off the footprints provided in their datasheets. The width of the traces was designed based on the rated current flowing through each component. The voltage and current sensors were integrated into this PCB through the use of a resistor bridge and a kelvin sense resistor respectively. The layout of the proposed converters PCB is shown in the appendix.

4.51 Snubber Circuit Design

When designing the hardware prototype the three winding coupled inductor was wound by hand with a turns ratio of 1:4:2 for the primary, secondary, and tertiary winding respectively. The chosen magnetizing inductance for this coupled inductor was 45μH. However there is also a leakage inductance that is present in this coupled inductor caused by the imperfect magnetic link from one winding to another. This inductance can resonate with the output capacitance of the diode connected to the secondary winding of the coupled inductor. This resonance results in significant spikes and ringing in some of the converters waveforms.

Fig. 4-14 shows the switch voltage and switch current waveforms for the proposed converter operating in mode B. The voltage waveform matches that of the one seen in fig. 4-3 (a) however the current waveform is quite different from the one seen in fig. 4-3 (b). Here we can see the current waveform oscillating (ringing) rather than an expected constant slope. Fig. 4-15 shows the switch current waveform and the diode voltage waveform for the same operating condition. From here it can be seen that there is also ringing in the diode voltage waveform and that it matches with the current waveform. Hence, it can be understood that the leakage inductance of the coupled inductor is resonating with the output capacitance of the diode which creates this ringing.

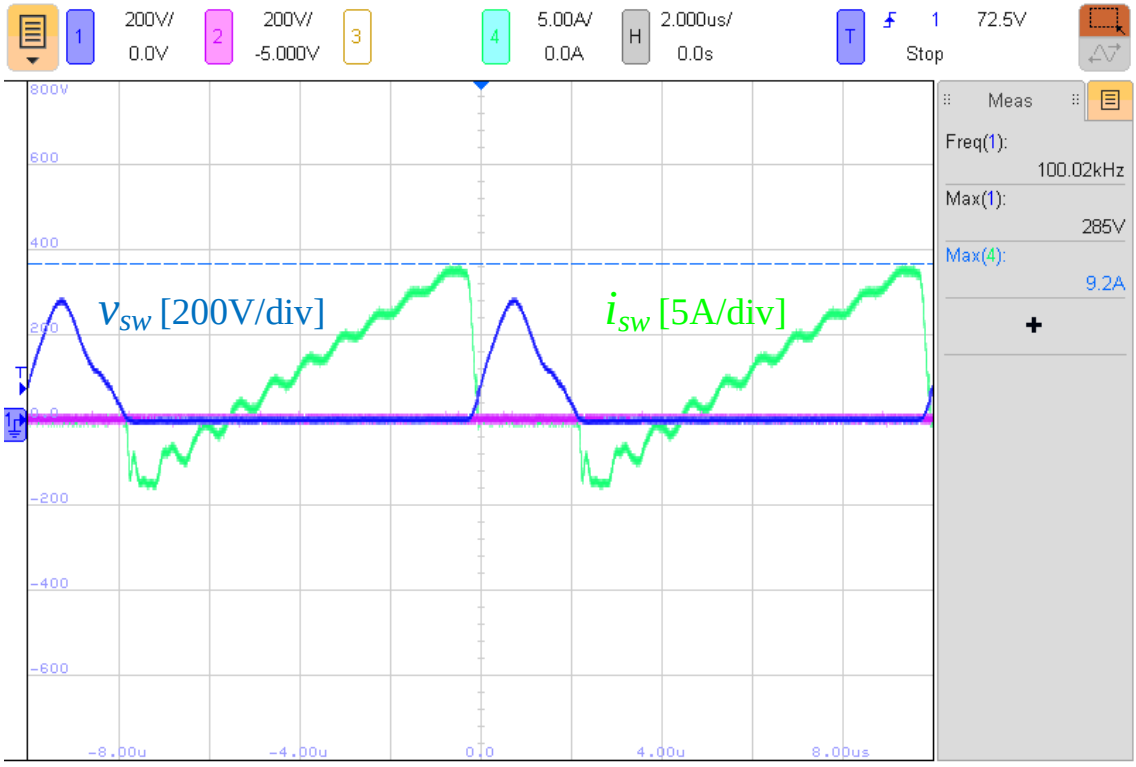


Figure 4-14: Switch voltage and current waveform for Mode B

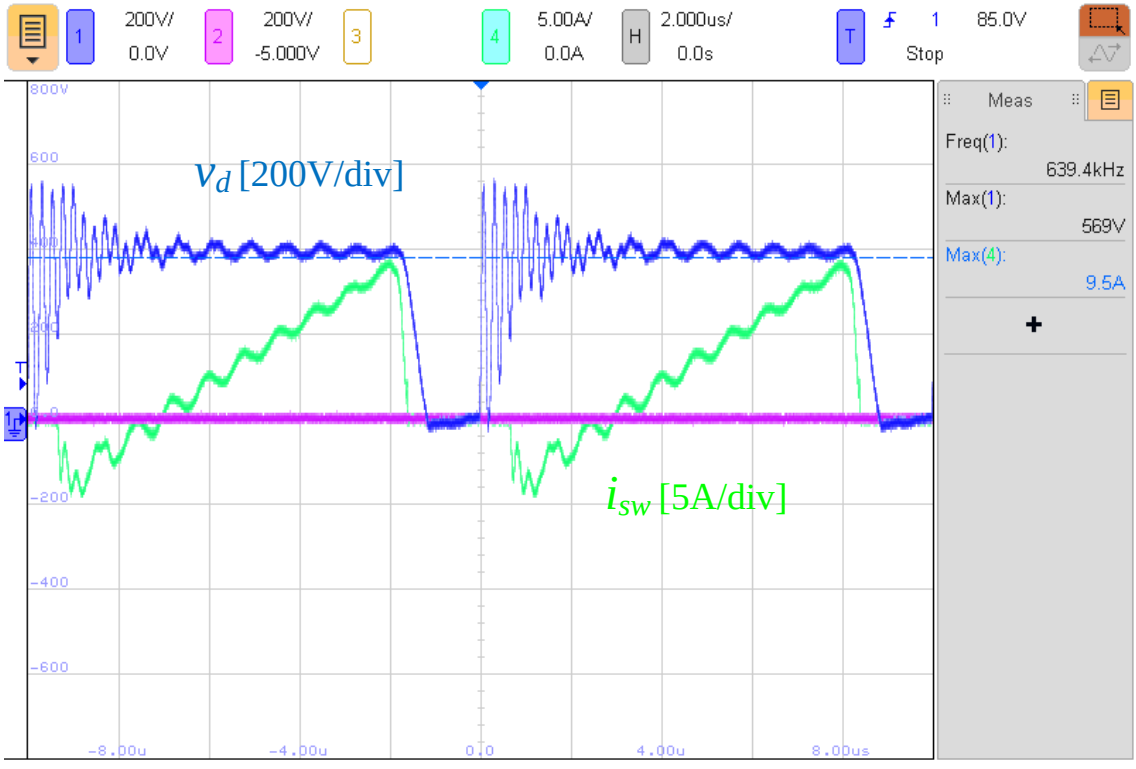


Figure 4-15: Switch current and diode voltage waveform for Mode B

In order to remove this ringing from the converter waveforms a snubber capacitor must be employed. Fig. 4-16 shows the proposed converter with an additional RC snubber circuit. This circuit consists of a single capacitor and resistor whose values are chosen based on the leakage inductance and ringing frequency.

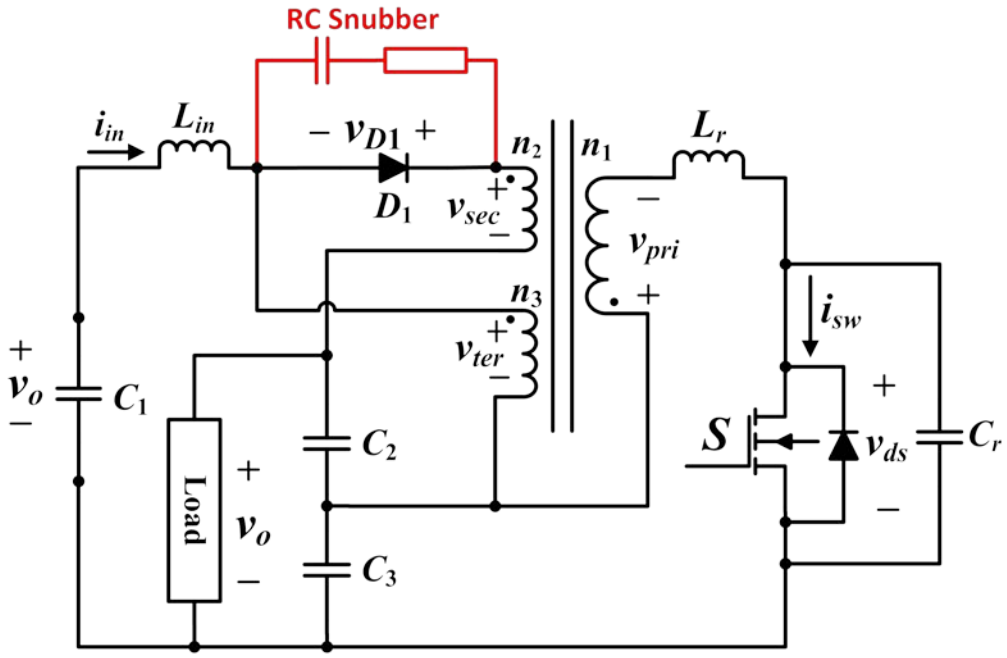


Figure 4-16: Proposed Converter with an additional RC snubber circuit

To obtain the value of the leakage inductance an LCR meter was employed. The positive and negative nodes of the primary winding were connected to the meter while the secondary and tertiary windings were shorted. As a result the measured inductance would be the leakage inductance. This was then performed with the secondary and tertiary windings respectively to obtain their leakage inductance.

The ringing frequency was obtained through the oscilloscope. Fig 4-17 shows the diode voltage waveform zoomed into the ringing. From here the time between two peaks was found to be 240ns which corresponded to a frequency of approximately 4.16Mhz.

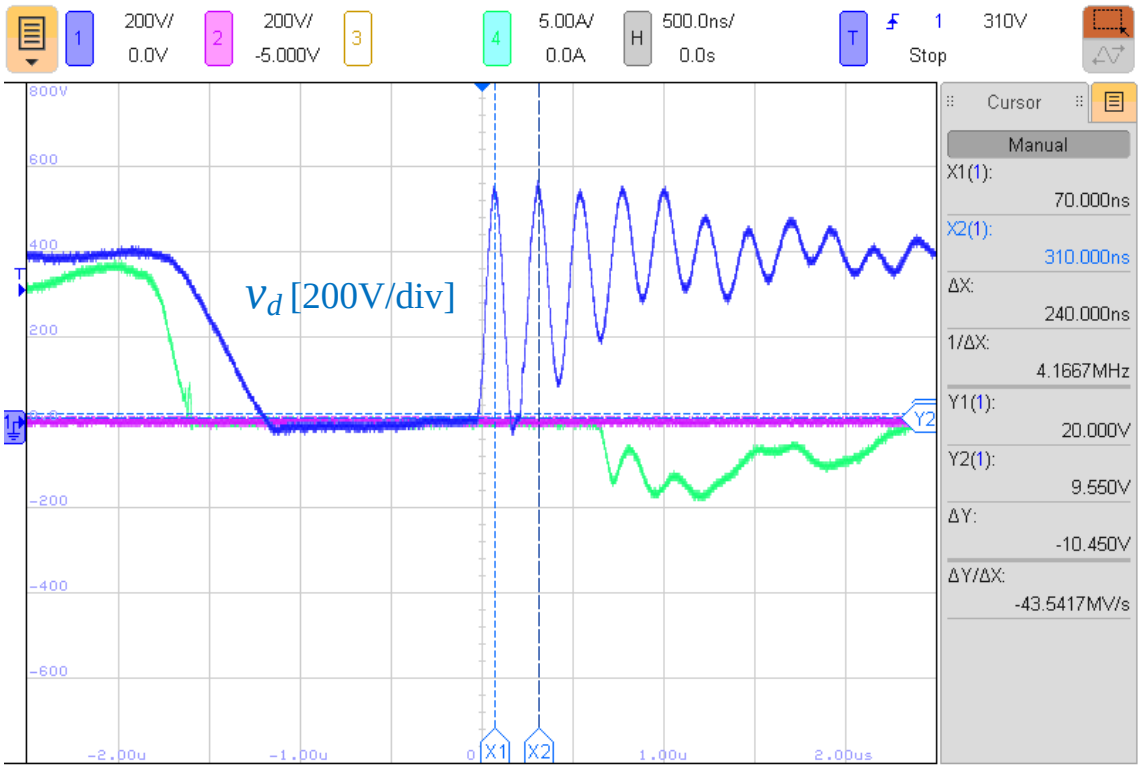


Figure 4-17: Zoom-in of the oscillation in the diode voltage waveform

The equations required to calculate the snubber capacitor and snubber resistnace are given in equation 4-5 and 4-6 respectively. From here it was found that the required capacitance was 0.9nF and the required resistance was 41Ω respectively. The addition of the snubber circuit introduces losses in the circuit. This power loss is related to the chosen capacitance, the voltage across the diode, and the switching frequency of the circuit. The equation that governs this loss is provided in equation 4-7. In order to decrease this loss the snubber capacitance and resistance can be varied slightly while ensuring that the ringing is still suppressed [47-49].

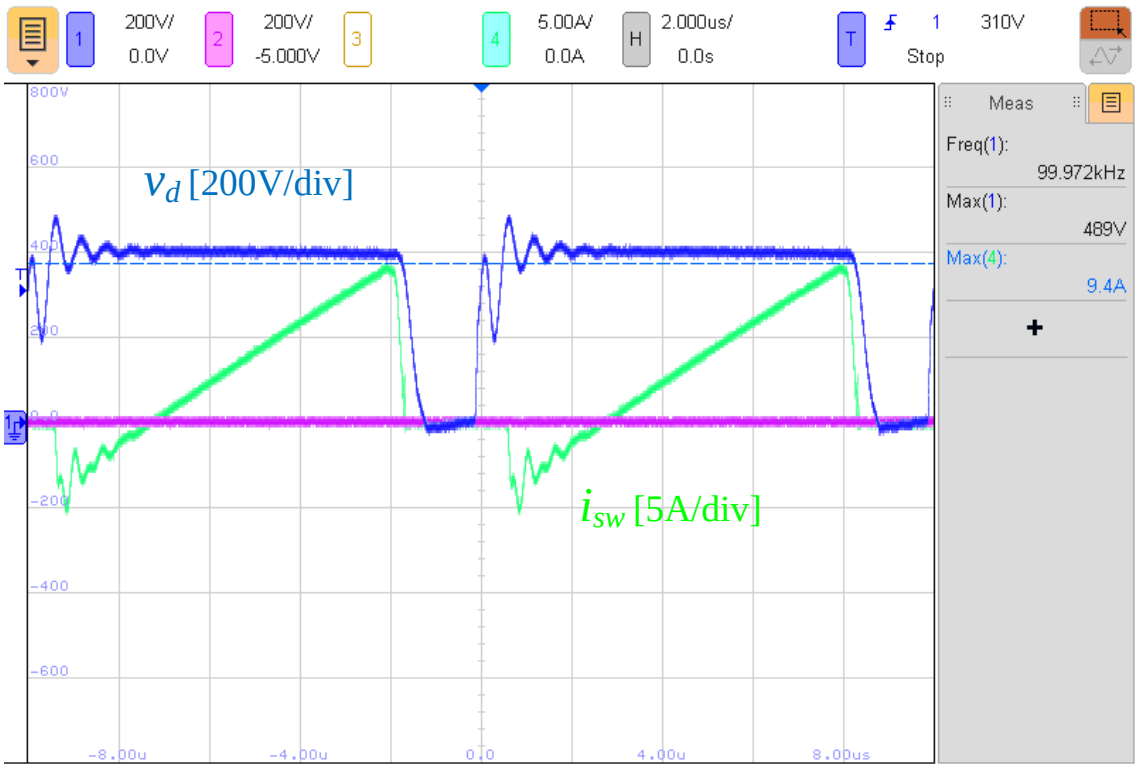


Figure 4-18: Switch current and diode voltage waveform of the converter operating under mode B with the snubber circuit integrated.

Figure 4-18 shows the switch current waveform and the diode voltage waveform for the proposed converter operating in mode B with the snubber circuit in parallel with the secondary winding diode. From here it can be observed that the ringing has been supressesd due to the addition of the snubber circuit.

$$c_p = \frac{1}{(2\pi f_r)^2 L_p} \qquad \text{(Eq. 4-5)}$$

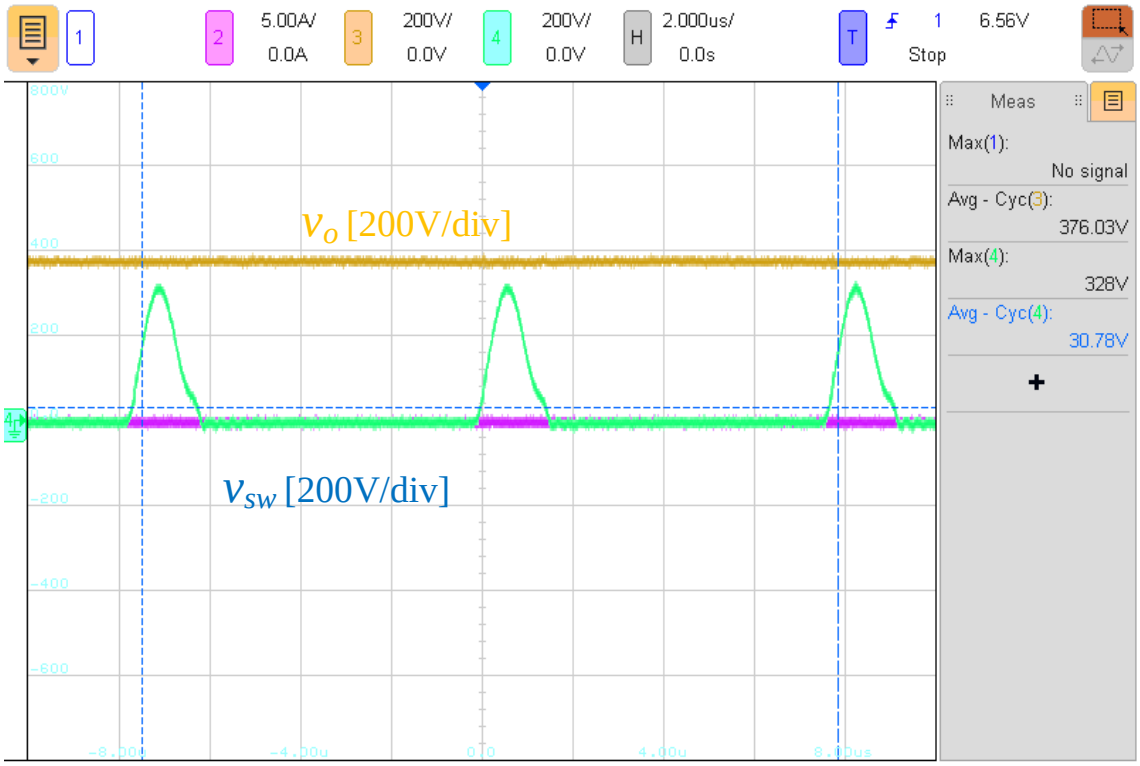
$$R_s = Z_p = \sqrt{\frac{L_p}{c_p}} \qquad \text{(Eq. 4-6)}$$

$$P_L = c_p v_D{}^2 f_s \qquad \text{(Eq. 4-7)}$$

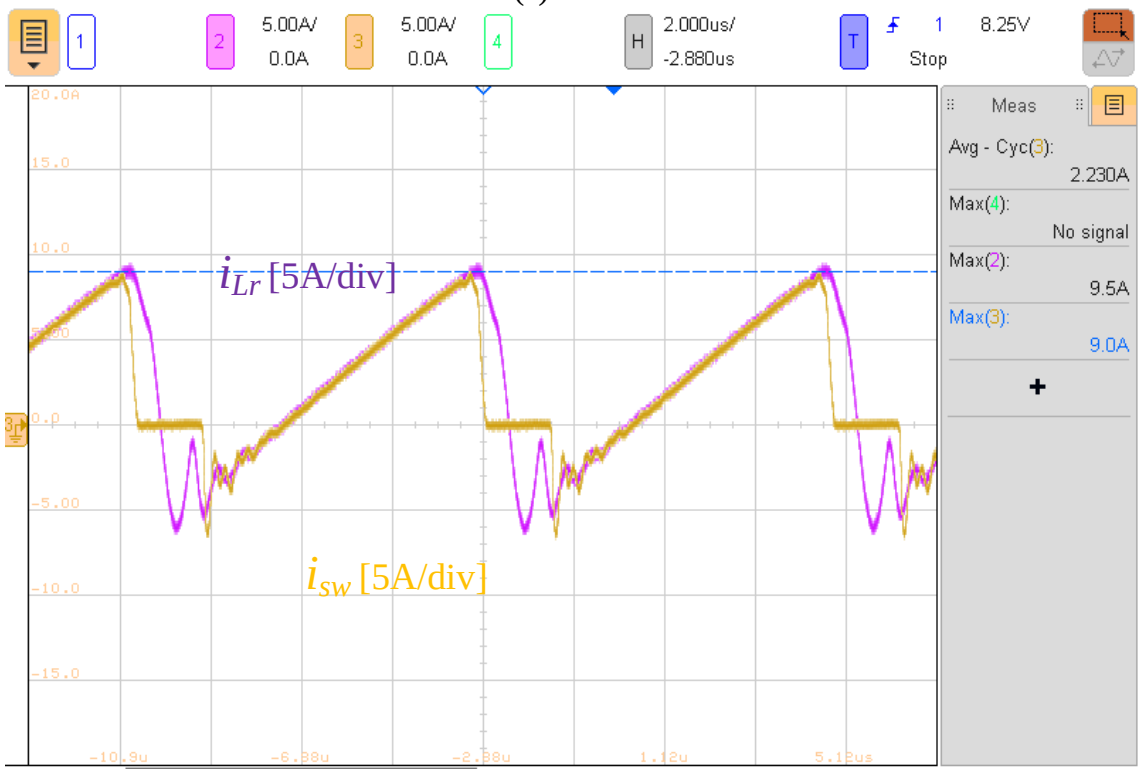
4.52 Prototype Results: Mode A 380V Operation

In the case of the proposed converter operating in mode A, to achieve an output voltage of around 380V the converter was operated at a frequency of 130 kHz with a duty cycle of 60%. The duty cycle was chosen such that the switch would operate under soft-switching condition. Fig. 4-19 (a) shows the output voltage (v_o) and switch voltage (v_{ds}) at this operating condition with the switch voltage shown in green and the output voltage shown in gold. From here it can be seen that the circuit is able to step-up the input voltage from 35V to approximately 380V when operating at the given condition. The reading from the oscilloscope gives a peak switch voltage of 328V while the average output voltage was approximately 376V. From here the ratio between the peak switch voltage and the output voltage is found to be approximately 0.9:1.

Fig. 4-19 (b) shows the switch current (i_s) shown in purple and the resonant inductor current waveform (i_{Lr}) in gold. By comparing this figure to that of fig. 4-18 (a) it can be seen that the converter has achieved ZVS operation. The peak switch current is approximately 9A while the peak resonant inductor current is around 9.5A. These results make sense as the resonant inductor current continues to increase during stage 1 while the current through the switch is redirected to the resonant capacitor.



(a)



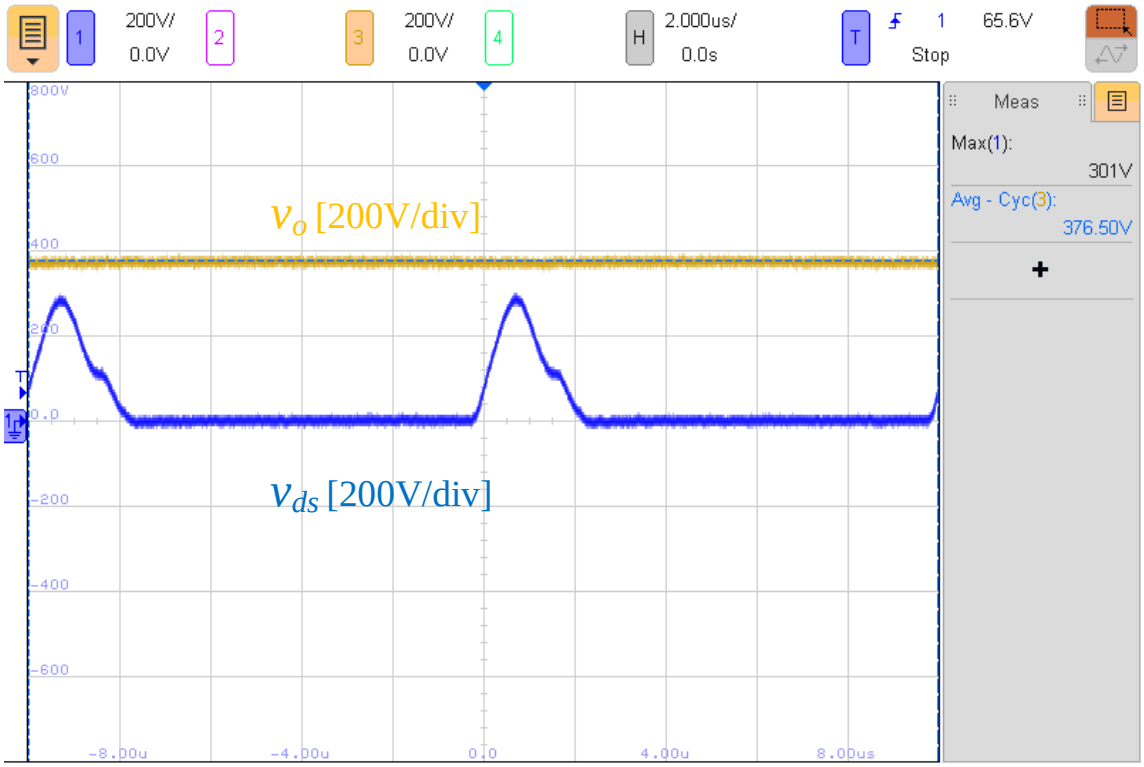
(b)

Figure 4-19: Mode A: (a) output voltage and switch voltage, (b) switch voltage and switch current.

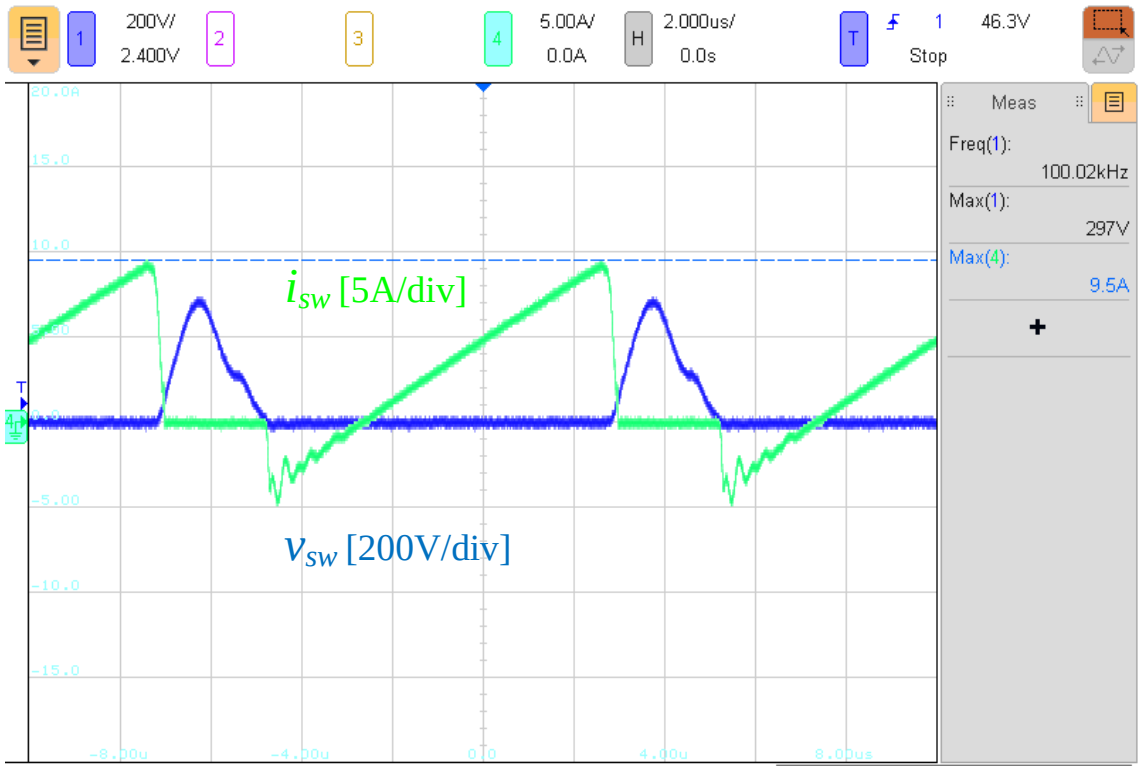
4.53 Prototype Results: Mode B 380V Operation

To achieve an output voltage of around 380V the circuit under mode B was operated at a frequency of 100kHz with a duty cycle of 60%. As with the simulation results, the duty cycle was chosen such that the switch would operate under soft-switching condition. Fig. 4-20 (a) shows the output voltage (v_o) and switch voltage (v_{ds}) at this operating condition with the switch voltage shown in blue and the output voltage shown in gold. From here it can be seen that the circuit is able to step-up the input voltage from 35V to 380V when operating at the given condition. The switch voltage v_{ds} is also seen to be much lower than v_o. The reading from the oscilloscope gives a peak switch voltage of 301V while the average output voltage was approximately 376.5V. From here the ratio between the peak switch voltage and the output voltage is found to be approximately 0.8:1.

Fig. 4-20 (b) shows the switch current (i_s) shown in green and the switch voltage waveform (v_{ds}) in blue. It can be seen that when the switch voltage begins to rise, the switch current waveform drops to zero and stays zero during the time the switch voltage is positive. When the switch voltage reaches zero the switch current immediately changes to a negative value and begins to rise. This change shows the resonant capacitor current being redirected into the anti-parallel diode of the switch. It can also be seen that the switch current becomes positive while the switch voltage is positive which shows that ZVS operation is achieved. When observing the switch voltage waveform it can be seen that there is a second peak that occurs when the voltage was decreasing. This peak represents a point when the resonant inductor current became positive and also shows the transition between stage II and III for mode B.



(a)



(b)

Figure 4-20: Mode B: (a) output voltage and switch voltage, (b) switch voltage and switch current.

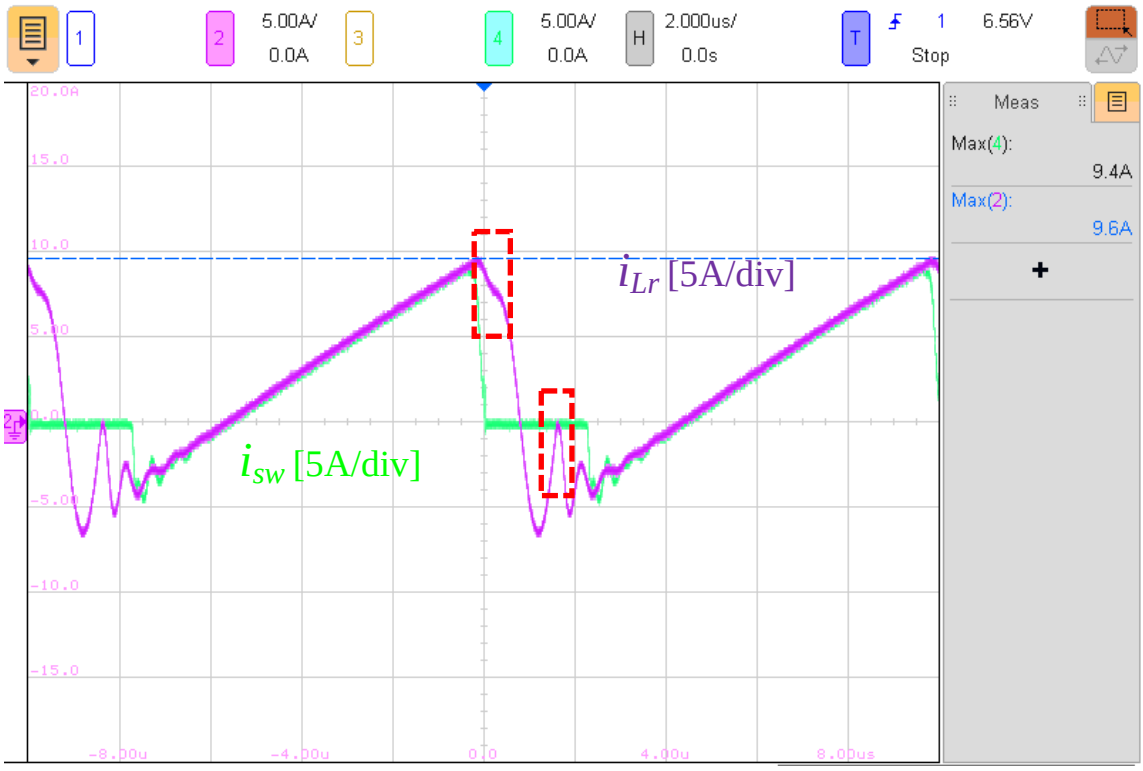


Figure 4-21: Mode B: switch current and resonant inductor current.

Fig. 4-21 shows the switch current (i_s) shown in green and the resonant inductor current waveform (i_{Lr}) in purple. Here it can be seen that the switch current and resonant inductor current are identical except for the section where the switch current drops to zero. When observing the inductor current waveform the transitions between stage I and II and stage II and III can be seen. The first transition is shown by a change in the current waveform which represents when the diode turned on. The second transition is also shown by a change in the waveform which represents when the diode turned off. The peak switch current is higher than that of mode A which confirms what was discussed regarding the peak switch current in section 2-3.

Figure 4-22: Mode B: Diode voltage and current

Fig. 4-22 contains the diode voltage (v_D) shown in gold and the diode current waveform (i_D) in purple. Here it can be seen that soft-switching operation has been achieved for the diode. The oscillations in the diode voltage and current waveforms have been suppressed through the use of the snubber circuit. The peak diode voltage is 502V while the steady state diode voltage is approximately 400V which is slightly larger than the output voltage.

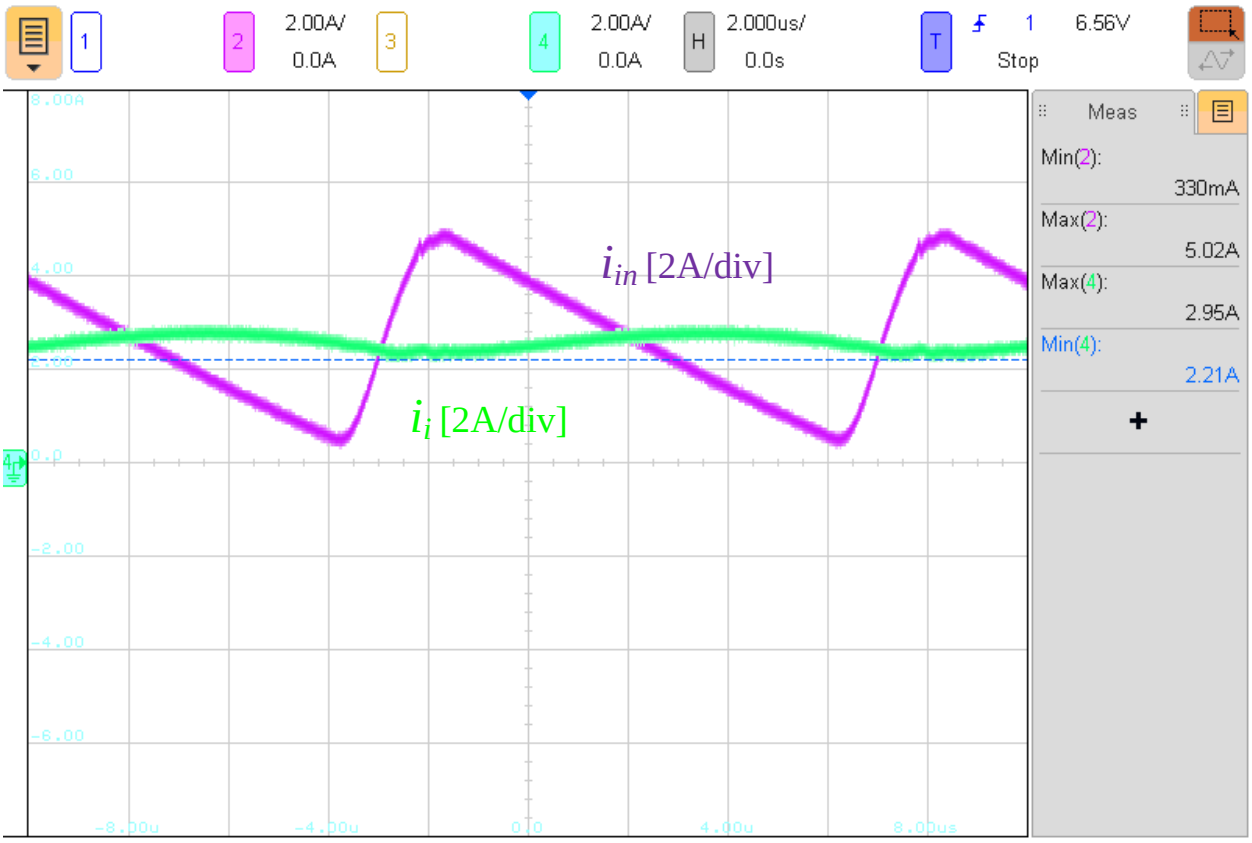


Figure 4-23: Mode B: Input current and input capacitor current

Fig. 4-23 contains the input current (i_i) shown in green and the input capacitor current (i_{in}) in purple. As with mode A and the waveforms obtained from simulation, it can once again be seen that the minimum current value is greater than zero, which confirms that continuous conduction mode is being achieved in the proposed converter.

4.54 MPPT Controller Operation Mode A

In order to test the proposed converter hardware prototype for maximum power point tracking operation the circuit must be integrated with a MPPT controller and have a solar panel at its input. A keysight E4360A Modular Solar Array Simulator was chosen as the input source for the converter. This simulator is able to accurately model a solar array system when provided its characteristics found from a panel's datasheet. Table 4-5 shows the (specifics) of the simulator. The maximum possible output voltage is much higher than what the proposed converter requires however the maximum output current is close to the rated value. As a result the two channels of the solar emulator were connected in parallel such that the maximum possible current that could be drawn was increased.

Table 4-5: Solar Panel Emulator Parameters [61]

Name	**Value**
Model	E4360A
Maximum Power	1200W
Maximum Output Voltage	300V
Maximum Output Current	2.55A
Number of Channels	2
Channel Configuration	Series or Parallel

A TMS320F28335 DSP microcontroller was employed to provide MPP control for the converter. Table 4-6 contains the parameters of the microcontroller. The controller was programmed through the use of the integrated development environment (IDE) code composer studio (CCS). The required code was input onto the program and then loaded onto the microcontroller. The frequency at which the microcontroller sampled at was 150MHz, however the proposed converter operated at a frequency range on the order of kilohertz. In order to circumvent this issue a delay was introduced into the controller code such that the micro-controller would sample at a rate equal to the converters frequency. Jumper wires were connected from the proposed converter to the ADC pins of the microcontroller such that the required parameters for the MPPT controller could be obtained. The gate signal was sent from one of the micro-controllers general purpose input output (GPIO) pins to the gate driver of the converter.

Table 4-6: DSP Board Parameters [62]

Name	**Value**
Model	TMS320F28335
Frequency	150MHz
ADC Modules	2
ADC Resolution	12-bit
ADC Voltage	Up to 3.3V
GPIO Pins	62
Ground Pins	11

The experimental setup was designed such that the micro-controller would receive the converters input voltage and current which would then be used to calculate the operating power. From here the controller would then perform a series of checks to determine how the frequency should be varied such that maximum power operation can be achieved. The controller would then output a waveform with the desired frequency and duty cycle to the MOSFET driver. In order to provide the input voltage and current to the micro-controller a voltage and current sensor were integrated into the converter. Fig. 4-24 shows the experimental set-up.

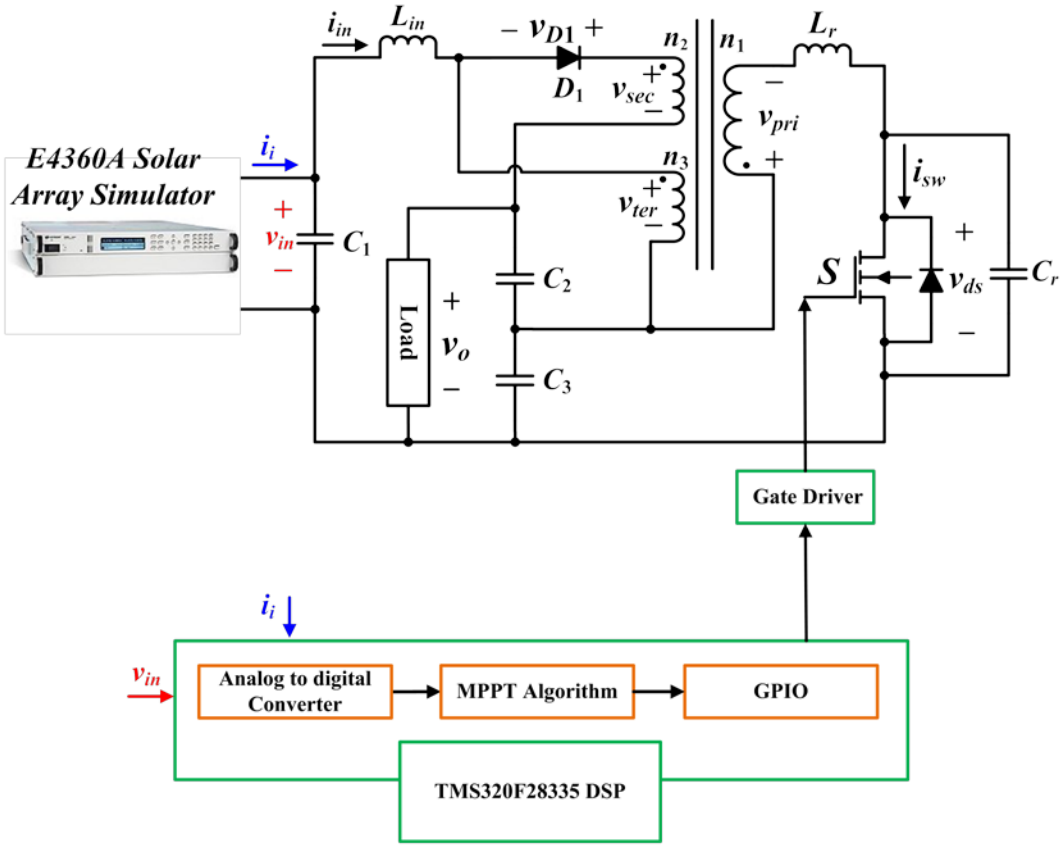
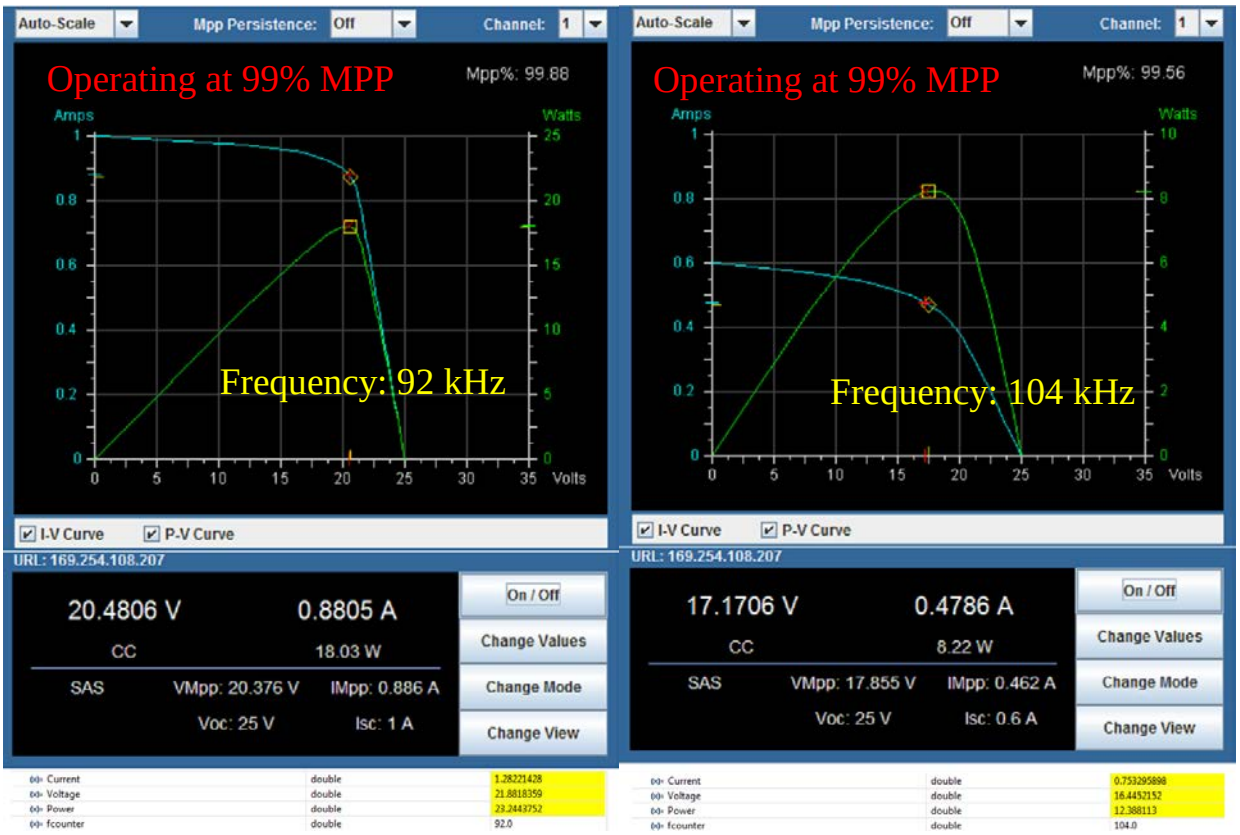


Figure 4-24: System diagram of the experimental setup: Proposed converter connected to the solar panel emulator as well as the micro-controller.

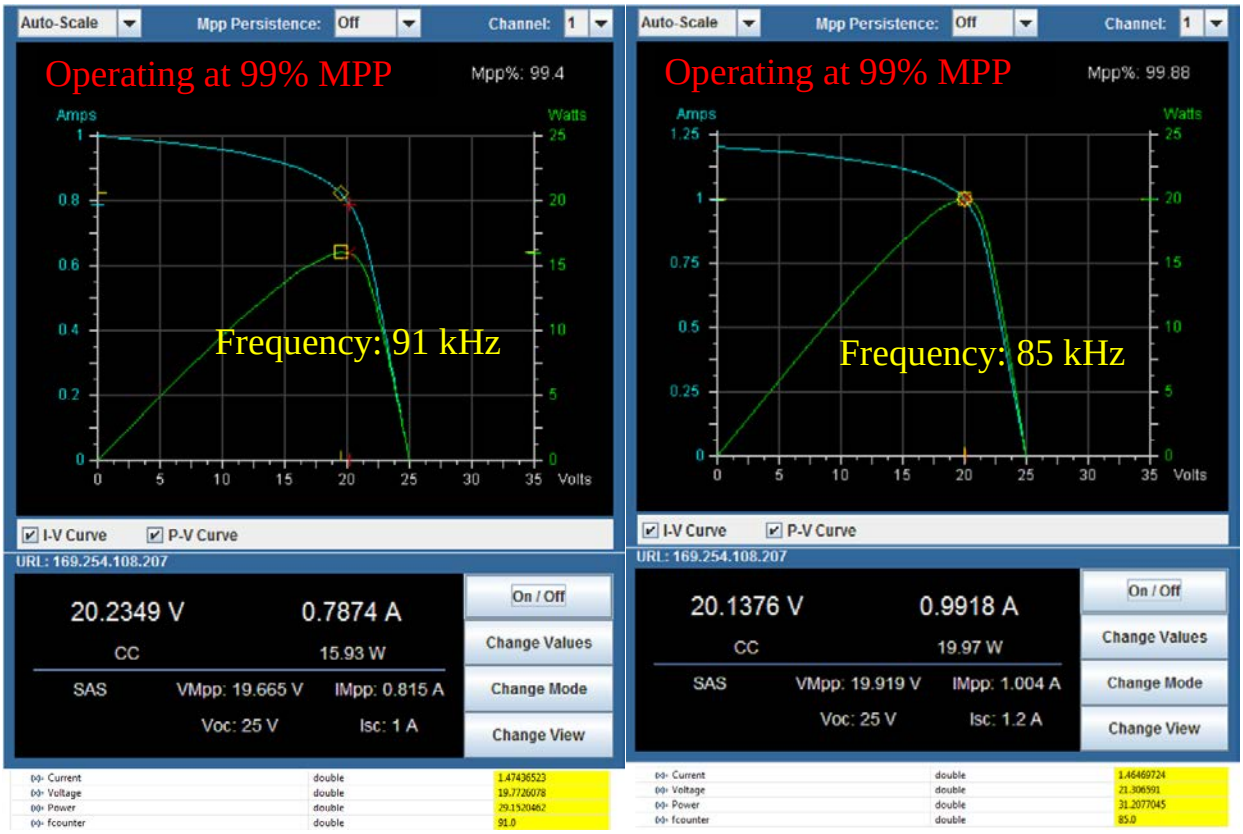


(a) (b)

Figure 4-25: Power-voltage and current voltage curves of the solar panel emulator: (a) high light intensity low frequency, (b) low light intensity high frequency

Fig. 4-25 (a) and (b) shows the power-voltage and current-voltage curves of the solar panel emulator. Two different scenarios were chosen to be tested with the converter operating in mode A. For both scenarios the voltage and current at the maximum power point were different and as a result the required frequency to operate at this point was different. These figures also contain the measured current and voltage from the microcontroller, the calculated operating power, and the frequency of the signal sent to the converters switch. From this figure it can be seen that the designed maximum power point tracking controller was able to change the operating frequency of the converter such that the panel could operate at its maximum.

4.55 MPPT Controller Operation Mode B



(a) (b)

Figure 4-26: Power-voltage and current voltage curves of the solar panel emulator: (a) high light intensity low frequency, (b) low light intensity high frequency

Fig. 4-26 (a) and (b) contains the power-voltage and current-voltage curves of the solar panel emulator for when the converter was operating in mode B. Once again two different scenarios were employed which had a different operating voltage and current at the maximum power point. The controller would vary the frequency of the proposed converter such that the system would operate at the maximum. As with mode A, it can be seen that the maximum power point operation has been achieved, which confirms that the controller was integrated successfully with the converter.

4.6 Analysis

Table 4-7 contains a summary of several step-up converters and their features including the proposed converter for both mode A and mode B operation. These features include a breakdown of their components, their peak switch and diode voltage, the converter gain, their switching condition and the operating frequency. From this table it can be seen for the converters [17] and [18] have identical voltage gain however they each have a different peak switch and diode voltage. In both cases the converters require a large duty cycle to operate at 380V. The gain of converters discussed in [16], [21], and [22] are similar. While [16] and [17] have identical peak switch and diode voltages the converter discussed in [22] is able to obtain a much lower peak diode voltage. The converters [21] and [22] require up to four switches and diodes which imply the circuit are bulky in size. The need for four switches also implies additional gate driver circuits. The converter discussed in [24] consists of a single switch. Although the gain equation is not directly provided it is shown to achieve 380V at the output. Compared to these circuits, the proposed converter is able to achieve the same step-up gain with the minimum number of total components while ensuring a low switch to output voltage ratio.

Table 4-7: Comparison of various step-up DC/DC Converters for PV energy applications

Converter	Number of Components				Typical Value		Peak switch voltage	Peak diode voltage	Gain	Coupled Inductor	Switching Type	Operating Frequency
	S	D	C	L	C	L						
[17]	2	1	1	2	70µF	100µH	$\frac{v_o + v_i}{2}$	$v_o + v_i$	$\frac{1+D}{1-D}$	No	Hard	100kHz
[18]	1	4	1	2	20µF	400µH	v_o	v_i	$\frac{1+D}{1-D}$	No	Hard	100kHz
[16]	2	4	4	3	10µF	50µH	$\frac{v_o}{2(n+1)}$	$\frac{2n+1}{2(n+1)}v_o$	$\frac{2n+1}{1-D}$	Yes	Hard	100kHz
[21]	4	2	3	4	47µF	40µH	$\frac{v_o}{2(n+1)}$	$\frac{2n+1}{2(n+1)}v_o$	$\frac{2(n+1)}{1-D}$	Yes	Hard	50kHz
[22]	4	4	4	4	470µF	47µH	$\frac{v_o}{2n}$	$\frac{v_o}{2}$	$\frac{2n}{1-D}$	Yes	Soft	100kHz
[24]	1	3	3	2	10µF	50µH	$v_{ca} + v_{cr} > 2v_o$	-	-	Yes	Soft	30kHz
[24]	2	6	4	4	10µF	50µH	$v_{ca} + v_{cr} > 2v_o$	-	-	Yes	Soft	30kHz
Proposed work: Mode A	1	1	4	3	10µF	1.5µH	$v_i - v_{pri} + i_{lr}(t_0)Z$	$v_p(n_2 - n_3) + (v_o - v_i)$	$1 + \frac{\frac{t_1(n_2-n_3-1)}{2} + (t_2+t_3) + \frac{t_4(n_2-n_3)}{L_\alpha}}{t_2 + t_3 - \frac{t_1}{2}}$	Yes	Soft	Up to 300kHz
Proposed work: Mode B	1	1	4	3	10µF	4.7µH	$v_i - v_{pri} + i_{lr}(t_0)Z$	$v_p(n_2 - n_3) + (v_o - v_i)$	$1 + \frac{\left(\frac{n_2-n_3}{n_1}\right)\left(\frac{t_2}{2} + \frac{1}{L\alpha}\left(t_4 + \frac{t_5}{2} + \frac{t_2}{2}\right)\right)}{t_2 + \frac{t_1}{2}}$	Yes	Soft	Up to 300kHz

The efficiency of the proposed converter in simulation was found to be approximately 91% for mode A and 93% for mode B. This was determined through dividing the output power by the input power. For the hardware prototype the efficiency was found to be 86% and 88% for mode A and mode B respectively. This was determined by obtaining the input and output voltage and current waveforms from the oscilloscope and then removing the known power losses. These power losses include the sense resistor used for measuring the input current as well as the snubber circuit used for minimizing oscillations in the diode voltage and switch current waveform.

Fig 4-27 shows a thermal image of the proof-of-concept hardware prototype obtained through a Keysight true IR thermal imager. The temperature indicator was chosen to range from approximately 27°C to 69°C such that the colour scaled with the temperature. In fig 4-27 (a) it can be seen that the two components that are the hottest are the converters switch and the load. Fig 4-27 (b) contains a zoon-in of the switch with a heat sink attached which can be seen to be at a temperature of 47.8°C. As the converter operates under quasi-resonant soft switching, it can be concluded that this heat is generated through conduction loss which is contributing to the power loss. Fig. 4-27 (c) shows the coupled inductor. From here it can be seen that its temperature is around 32.3°C which implies that it does not contribute much to the power loss.

(a)

(b)

(c)

Figure 4-27: Thermal image: (a) Overall system, (b) switch *S*, (c) coupled inductor

4.7 Summary

This chapter presented the results and performance of the proposed single switch, quasi-resonant step-up DC/DC converter. Simulation results have been provided to confirm the operation of both mode A and mode B for the proposed converter for 380V output as well as maximum power point tracking operation. The derived equations were plotted and found to match that the waveforms obtained from simulation. A laboratory scale proof of concept hardware prototype was built and tested with 380V output operation as well as maximum power point tracking through the use of a solar panel emulator and a micro-controller to show the feasibility of the system. The simulation and hardware results also confirmed that the converter is able to achieve ZVS and CCM operation.

5. Summary and Conclusion

5.1 Summary

The total global capacity of renewable energy has been increasing year on year. In particular solar energy has seen a rapid growth in install capacity and total energy produced. In order to convert this produced energy into useable electrical energy power electronic converters are required. These converters can also assist the solar panel in operating at the point of maximum energy through the use of maximum power point tracking.

In order to match the output voltage of the panel with that of the load, step-up DC/DC converters are required. Conventional step-up converters suffer from issues such:

1. Requiring a large duty cycle to achieve a large gain.
2. Operating under hard switching, restricting the operating frequency, and increasing the size of passive components.
3. Operating under soft-switching through the use of auxiliary components.
4. Requiring multiple components to achieve a large gain.
5. Operating in discontinuous conduction mode which requires the use of a large electrolytic capacitor.
6. High peak switch voltage stress when operating with a single switch.

The focus of this thesis was to develop a single-switch, electrolytic capacitor-less quasi-resonant step-up DC/DC converter for solar energy system.

5.2 Contributions

The contributions from this thiesis have been summarized below

1. A new single switch, coupled inductor based step-up DC/DC converter has been presented.
2. The proposed converter able to operate with a DC source or with a solar panel and is able to step-up the input voltage up to the rated voltage of 380V with the use of a single switch.
3. The input inductor of the proposed converter operated in continuous conduction mode, allowing for the use of a small-sized film capacitor at the input side instead of an electrolytic capacitor. This extended the lifespan of the overall system.
4. Quasi-resonant zero-voltage switching was employed in the circuit to improve the overall efficiency. The reduction of switching losses allowed for the use of a large operating frequency.
5. By operating at a frequency on the order of hundreds of kilohertz, the size of the passive components in the proposed converter have been reduced. This allows for a small compact system.
6. Theoretical analysis and the operating stages of two different modes of operation have been provided and discussed in detail.
7. Simulation results were presented through the use of a circuit simulation software (PSIM) to confirm the operation of the proposed converter.
8. A developed laboratory scale proof-of-concept hardware prototype has been developed, tested, and compared to the simulation results to validate the feasibility of the proposed converter.

9. A maximum power point tracking controller was designed and integrated with the proposed converter such that the maximal amount of energy can be extracted when operating with a solar panel.

5.3 Future work

Possible future work in regards to the proposed work are listed below.

1. Optimization of the RC snubber circuit. As mentioned in section 4.51 and 4.6, the power loss from the snubber circuit is quite high. In order to reduce this loss the values for the capacitor and resistor can be tuned to minimize the power loss while reducing the oscillation caused in the diode voltage and switch current waveform.
2. Implementing a GaN switch. In section 1.3 conduction loss was discussed. This type of power loss is a function of the on resistance of the switch. With the recent technology advancement in wide band-gap devices, such as GaN power switch with much lower on-resistance, one approach to further improve the power efficiency of the proposed converter is to investigate the use of various types of GaN switches and apply them to the proposed topologies.

5.4 Conclusions

In conclusion, a single switch, electrolytic capacitor-less quasi-resonant step-up DC/DC converter has been presented in this thesis for solar energy systems. The converter is able to achieve a large step up gain with a single switch through the use of a coupled inductor. The converters resonant components allow for ZVS operation without the need of additional auxiliary components, allowing for a cost effective and compact system. The converter operates in continuous conduction mode allowing for a small thin-film capacitor to be used in the input. Simulation results from PSIM have been presented to verify the performance of the proposed topology. Experimental results on a proof-of-concept hardware prototype have also been provided to highlight the merits and feasibility of this converter.

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APPENDIX

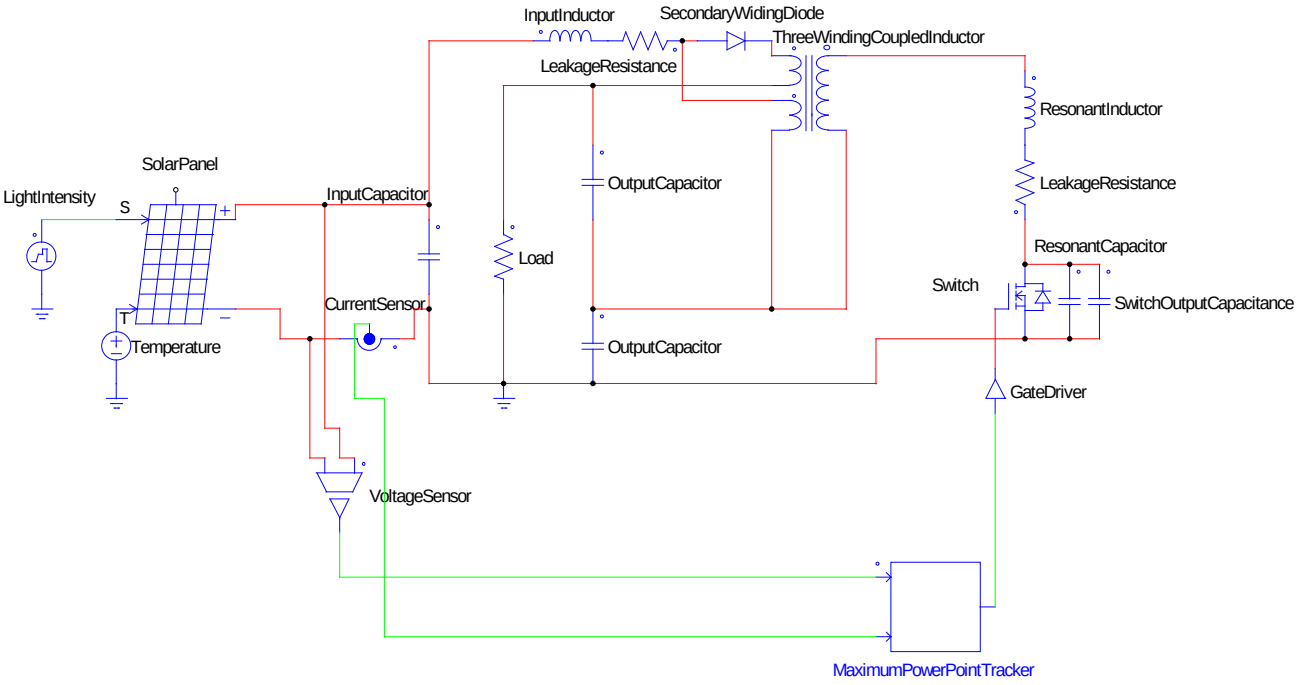

Figure A-1: PSIM schematic

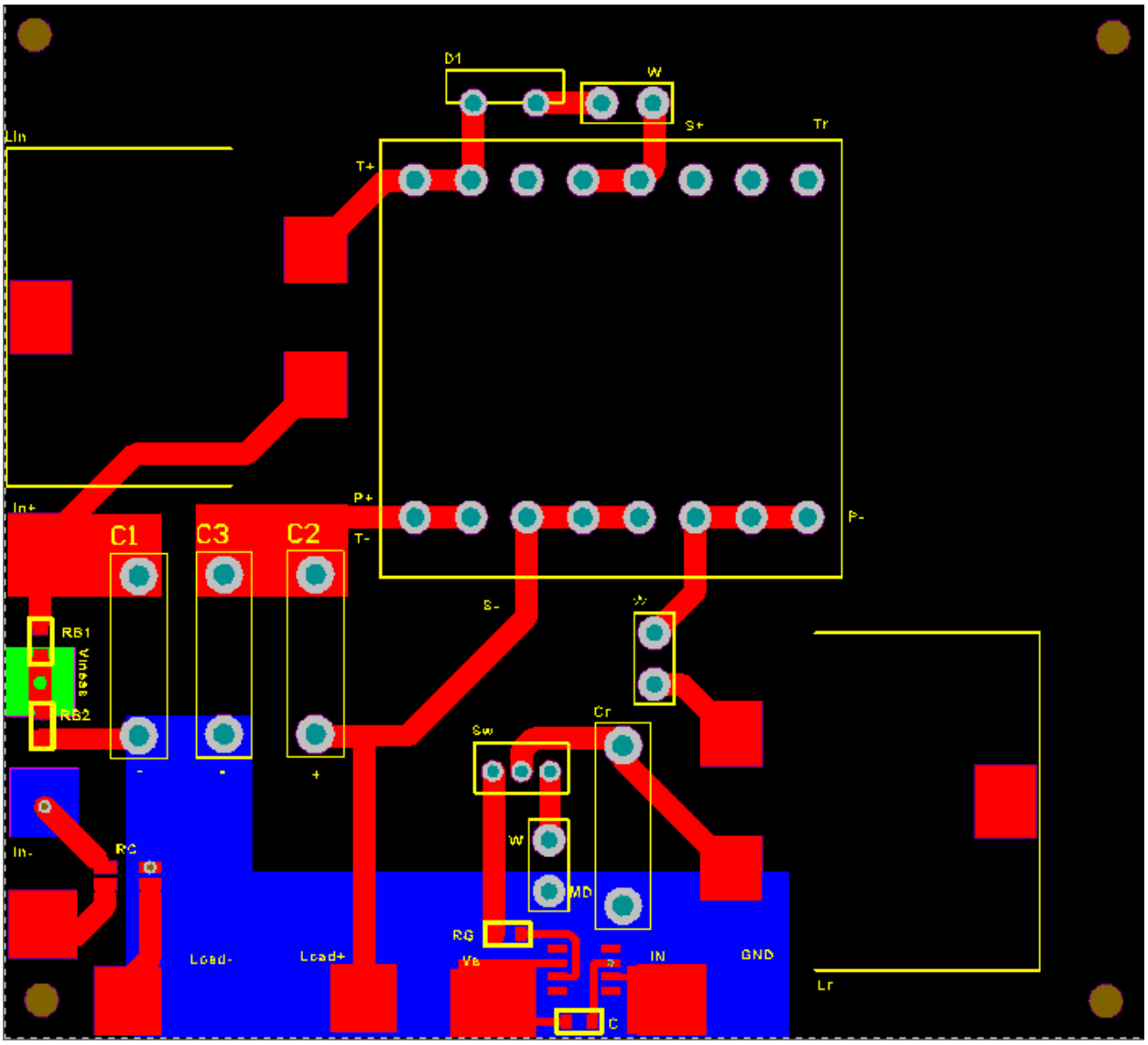

Figure A-2: PCB Layout designed in Altium Designer

MODE A and B: Stage I

Simplifying the primary voltage equation:

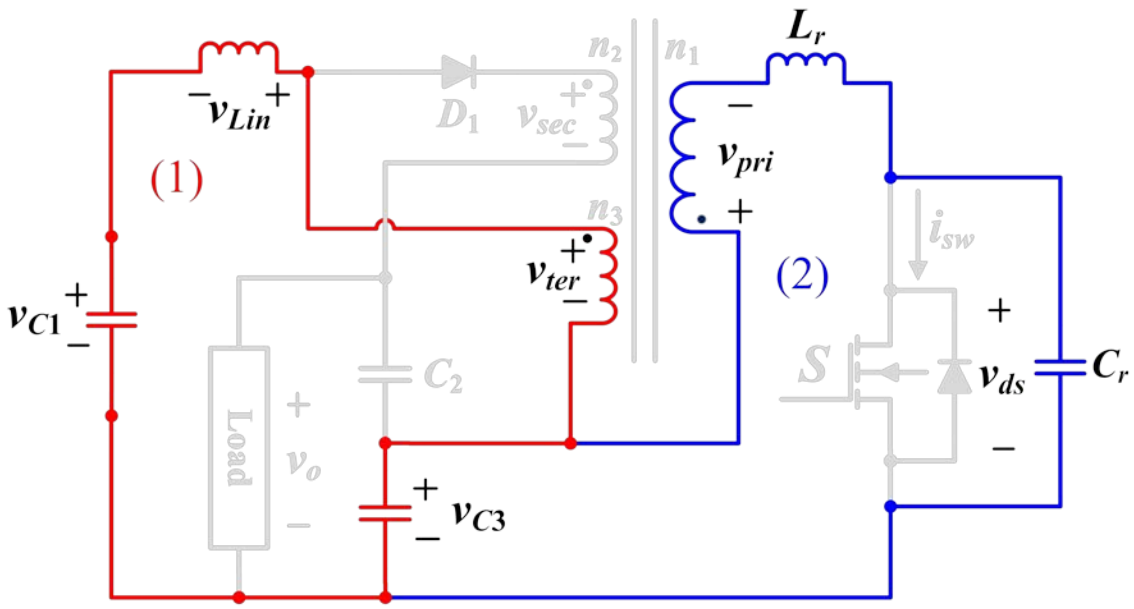

Figure A-3: Stage I for Mode A and Mode B

From (1):

$$v_i = v_{Lin} + v_{ter} + v_{c3}$$

$$v_i = L_{in}\frac{di_3}{dt} + L_p n_3{}^2\frac{di_1}{dt} + L_p n_3{}^2\frac{di_3}{dt} + v_i$$

$$L_{in}\frac{di_3}{dt} + L_p n_3{}^2\frac{di_3}{dt} = -L_p n_3{}^2\frac{di_1}{dt}$$

$$\frac{di_3}{dt} = \frac{-L_p n_3}{L_{in} + L_p n_3^{\,2}} \frac{di_1}{dt}$$

Rate of change of the input current in terms of the rate of change of the primary winding current

$$v_p = L_p \frac{di_1}{dt} - M \frac{di_3}{dt}$$

$$v_p = L_p \frac{di_1}{dt} - \frac{L_p^{\,2} N_3^{\,2}}{L_{in} + L_p N_3^{\,2}} \frac{di_1}{dt}$$

$$v_p = \frac{di_1}{dt}\left[\frac{L_p L_{in} + L_p^{\,2} N_3^{\,2}}{L_{in} + L_p N_3^{\,2}} - \frac{L_p^{\,2} N_3^{\,2}}{L_{in} + L_p N_3^{\,2}} \right]$$

$$v_p = \frac{di_1}{dt}\left[\frac{L_p L_{in}}{L_{in} + L_p N_3^{\,2}} \right]$$

Solving for v_{ds}

From (2):

$$i_{Cr} = i_{Lr}$$

$$C_r \frac{dv_{ds}}{dt} = i_{Lr} \quad \textbf{(A)}$$

Laplace Transform

$$C_r\left[s\left(v_{ds}(s)\right) - v_{ds}(t_0)\right] = i_{Lr}(s)$$

$$C_r\left[s\left(v_{ds}(s)\right)\right] = i_{Lr}(s)$$

From equation 2-1:

$$v_i = v_p + v_{Lr} + v_{ds}$$

Subsitute for *vp*

$$v_i = \frac{di_1}{dt}\left[\frac{L_p L_{in}}{L_{in} + L_p N_3{}^2}\right] + \frac{di_1}{dt} L_r + v_{ds}$$

$$v_i - v_{ds} = \frac{di_1}{dt}\left[\frac{L_p L_{in} + L_{in} L_r + L_r L_p N_3{}^2}{L_{in} + L_p N_3{}^2}\right]$$

$$v_i - v_{ds} = L\frac{di_1}{dt}$$

Laplace transform

$$L\left[s\left(i_{Lr}(s)\right)-i_{Lr}(t_0)\right]=\frac{v_i}{s}-v_{ds}(s) \qquad \textbf{(B)}$$

Subsitute i_{Lr} with **(A)**

$$sLC_r\left[s\left(v_{ds}(s)\right)\right]=\frac{v_i}{s}-v_{ds}(s)+Li_{Lr}(t_0)$$

$$s^2LC_r\left(v_{ds}(s)\right)+v_{ds}(s)=\frac{v_i}{s}+Li_{Lr}(t_0)$$

$$v_{ds}(s)\left(1+s^2LC_r\right)=\frac{v_i}{s}+Li_{Lr}(t_0)$$

Subsitite LC_r with $1/\omega_0{}^2$

$$v_{ds}(s)\left(\frac{s^2+\omega_0{}^2}{\omega_0{}^2}\right)=\frac{v_i}{s}+Li_{Lr}(t_0)$$

$$v_{ds}(s)=\frac{v_i}{s}\left(\frac{\omega_0{}^2}{s^2+\omega_0{}^2}\right)+Li_{Lr}(t_0)\left(\frac{\omega_0{}^2}{s^2+\omega_0{}^2}\right)$$

Inverse Laplace Transform

$$v_{ds}=v_i\left(1-\cos\omega_0 t\right)+i_{Lr}(t_0)L\omega_0\sin\omega_0 t$$

Switch voltage equation for Stage I

Solving for t_1

End condition for Stage I: $\dfrac{v_o - v_i}{n_2 - n_3}\left[1 + L\right] + v_i = v_{ds}$

$$\frac{v_o - v_i}{n_2 - n_3}\left[1 + L\right] + v_i = v_i\left(1 - \cos\omega_0 t\right) + i_{Lr}\left(t_0\right) Z \sin\omega_0 t$$

$$C = B\left(1 - \cos\omega_0 t\right) + A\sin\omega_0 t$$

$$t_1 = \frac{1}{\omega_0}\left(\sin^{-1}\left[\frac{C - B}{\sqrt{A^2 - B^2}}\right] + \cos^{-1}\left[\frac{A}{\sqrt{A^2 - B^2}}\right]\right)$$

Time period for Stage I

Solving for i_{Lr}

Substitute **(B)** into **(A)** to solve for the resonant inductor/capacitor current

$$i_{Lr}(s) = C_r\left[s\left(v_{ds}(s)\right)\right]$$

$$i_{Lr}(s) = C_r\left[sL\left[s\left(i_{Lr}(s)\right) - i_{Lr}(t_0)\right] - sv_i\right]$$

$$i_{Lr}(s) + s^2 LC_r i_{Lr}(s) = sC_r v_i + sLC_r i_{Lr}(t_0)$$

$$i_{Lr}(s)\left[1 + s^2 LC_r\right] = sC_r v_i + sLC_r i_{Lr}(t_0)$$

$$i_{Lr}(s) = sC_r v_i\left(\frac{\omega_0^{\,2}}{s^2 + \omega_0^{\,2}}\right) + sLC_r i_{Lr}(t_0)\left(\frac{\omega_0^{\,2}}{s^2 + \omega_0^{\,2}}\right)$$

Inverse Laplace Transform

$$i_{Lr} = \frac{v_i}{Z}\sin(\omega_0 t) + i_{Lr}(t_0)\cos(\omega_0 t)$$

Resonant Inductor current equation for Stage I

MODE A and B: Stage II

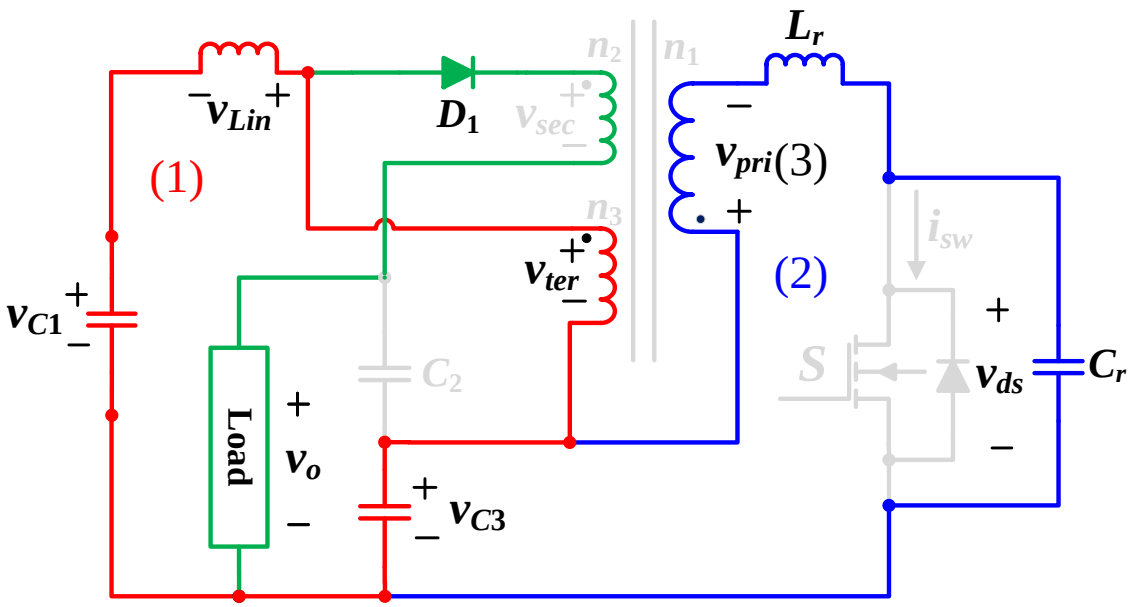

Figure A-4: Stage II for Mode A and Mode B

Solving for v_{ds}

From (2):

$$i_{Cr} = i_{Lr}$$

$$C_r \frac{dv_{ds}}{dt} = i_{Lr}$$

Laplace Transform

$$C_r\left[s\left(v_{ds}(s)\right)-v_{ds}(t_1)\right]=i_{Lr}(s)$$

From equation 2-1:

$$v_i = v_p + v_{Lr} + v_{ds}$$

Duirng stage II v_p is a constant.

$$v_i = v_p + L_r\frac{di_{Lr}}{dt} + v_{ds}$$

Laplace transform

$$L\left[s\left(i_{Lr}(s)\right)-i_{Lr}(t_1)\right]=\frac{v_i}{s}-\frac{v_p}{s}-v_{ds}(s) \quad \textbf{(B)}$$

Subsitute i_{Lr} with **(A)**

$$sLC_r\left[s\left(v_{ds}(s)\right)-v_{ds}(t_1)\right]=\frac{v_i-v_p}{s}-v_{ds}(s)+L_r i_{Lr}(t_1)$$

$$s^2LC_r\left(v_{ds}(s)\right)+v_{ds}(s)=\frac{v_i-v_p}{s}+sL_rC_r v_{ds}(t_1)+L_r i_{Lr}(t_1)$$

$$v_{ds}(s)\left(1+s^2LC_r\right)=\frac{v_i-v_p}{s}+sL_rC_r v_{ds}(t_1)+L_r i_{Lr}(t_1)$$

Substitute L_rC_r with $1/\omega_0{}^2$

$$v_{ds}(s)\left(\frac{s^2+\omega_0{}^2}{\omega_0{}^2}\right)=\frac{v_i-v_p}{s}+sL_rC_rv_{ds}(t_1)+L_ri_{Lr}(t_1)$$

$$v_{ds}(s)=\frac{v_i-v_p}{s}\left(\frac{\omega_0{}^2}{s^2+\omega_0{}^2}\right)+sL_rC_rv_{ds}(t_1)\left(\frac{\omega_0{}^2}{s^2+\omega_0{}^2}\right)+L_ri_{Lr}(t_1)\left(\frac{\omega_0{}^2}{s^2+\omega_0{}^2}\right)$$

Inverse Laplace Transform

$$v_{ds}=(v_i-v_p)(1-\cos\omega_0 t)+i_{Lr}(t_0)L\omega_0\sin\omega_0 t+v_{ds}(t_1)\cos\omega_0 t$$

Switch voltage equation for
Stage II

Solving for i_{Lr}

From (2):

$$i_{Lr}(s) = C_r\left[s(v_{ds}(s)) - v_{ds}(t_1)\right]$$

$$v_{ds}(s) = \frac{i_{Lr}(s)}{sC_r} + \frac{v_{ds}(t_1)}{s}$$

Substitute back into voltage equation

$$L_r\left[s(i_{Lr}(s)) - i_{Lr}(t_1)\right] = \frac{v_i}{s} - \frac{v_p}{s} - v_{ds}(s)$$

$$L_r\left[s(i_{Lr}(s)) - i_{Lr}(t_1)\right] = \frac{v_i}{s} - \frac{v_p}{s} - \frac{i_{Lr}(s)}{sC_r} - \frac{v_{ds}(t_1)}{s}$$

$$L_r s(i_{Lr}(s)) + \frac{i_{Lr}(s)}{sC_r} = \frac{v_i - v_p - v_{ds}(t_1)}{s} + L_r i_{Lr}(t_1)$$

$$i_{Lr}(s)\left[\frac{1 + s^2 L_r C_r}{sC_r}\right] = \frac{v_i - v_p - v_{ds}(t_1)}{s} + L_r i_{Lr}(t_1)$$

$$i_{Lr}(s)\left[\frac{s^2 + {\omega_0}^2}{{\omega_0}^2 sC_r}\right] = \frac{v_i - v_p - v_{ds}(t_1)}{s} + L_r i_{Lr}(t_1)$$

$$i_{Lr}(s) = \left(v_i - v_p - v_{ds}(t_1)\right)\left(\frac{\omega_0{}^2 C_r}{s^2 + \omega_0{}^2}\right) + L_r i_{Lr}(t_1)\left(\frac{\omega_0{}^2 s C_r}{s^2 + \omega_0{}^2}\right)$$

$$i_{Lr}(s) = \left(v_i - v_p - v_{ds}(t_1)\right)\left(\frac{\omega_0{}^2 C_r}{s^2 + \omega_0{}^2}\right) + L_r i_{Lr}(t_1)\left(\frac{\omega_0{}^2 s C_r}{s^2 + \omega_0{}^2}\right)$$

Inverse Laplace Transform

$$i_{Lr} = \left(v_i - v_p - v_{ds}(t_1)\right)(\omega_0 C_r)\sin(\omega_0 t) + i_{Lr}(t_1)\cos(\omega_0 t)$$

$$i_{Lr} = \frac{\left(v_i - v_p - v_{ds}(t_1)\right)}{Z}\sin(\omega_0 t) + i_{Lr}(t_1)\cos(\omega_0 t)$$

Resonant Inductor current equation for Stage II

Solving for i_{D1}

From (1):

$$v_i = v_{Lin} + v_{ter} + v_{c3}$$

$$v_{Lin} = -v_{ter}$$

$$L_{in}\left(\frac{di_2}{dt} + \frac{di_3}{dt}\right) = -n_3 L_p\left(\frac{di_1}{dt} + n_2\frac{di_2}{dt} + n_3\frac{di_3}{dt}\right)$$

From (2):

$$v_{c3} = v_{pri} + v_{Lr} + v_{ds}$$

$$v_i = L_p\left(\frac{di_1}{dt} + n_2\frac{di_2}{dt} + n_3\frac{di_3}{dt}\right) + L_r\left(\frac{di_1}{dt}\right) + v_{ds}$$

Where

$$v_{ds} = v_i - v_{pri} + i_{lr}(t_0)Z\sin(\omega_0 t) + \left(v_i - v_{pri} + v_{ds}(t_1)\right)\cos(\omega_0 t)$$

From (3):

$$v_{pri} = L_p\left(\frac{di_1}{dt} + n_2\frac{di_2}{dt} + n_3\frac{di_3}{dt}\right)$$

$$\frac{v_o - v_i}{n_2 - n_3} = L_p\left(\frac{di_1}{dt} + n_2\frac{di_2}{dt} + n_3\frac{di_3}{dt}\right)$$

Three are now three equations and three unknowns which are the rate of change of the primary, secondary, and tertiary currents. MATLAB was employed to solve for each of these unknowns. In particular, the rate of change of the secondary winding is useful in determining the total time for stage II.

From MATLAB after simplifying:

$$\frac{di_2}{dt} = \frac{v_p}{n_2 - n_3}\left[\frac{L_{in} + L_p n_3^{\,2}}{L_{in}L_p}\right](1 - \cos\omega_0 t) + \frac{\omega_0 i_0}{n_2 - n_3}\sin\omega_0 t$$

Integrating this equation will determine the current through the secondary winding.

$$\int \frac{di_2}{dt} = i_2 = \frac{v_p}{n_2 - n_3}\left[\frac{L_{in} + L_p n_3^{\,2}}{L_{in} L_p}\right]t - \frac{v_p}{\omega_0 (n_2 - n_3)}\left[\frac{L_{in} + L_p n_3^{\,2}}{L_{in} L_p}\right]\sin \omega_0 t - \frac{i_0}{n_2 - n_3}\cos \omega_0 t + c$$

Solve for i_2 when $t = 0$

$$0 = 0 - 0 - \frac{i_0}{n_2 - n_3} + c$$

$$c = \frac{i_0}{n_2 - n_3}$$

As a result:

$$i_2 = \frac{v_p}{n_2 - n_3}\left[\frac{L_{in} + L_p n_3^{\,2}}{L_{in} L_p}\right]t - \frac{v_p}{\omega_0 (n_2 - n_3)}\left[\frac{L_{in} + L_p n_3^{\,2}}{L_{in} L_p}\right]\sin \omega_0 t - \frac{i_0}{n_2 - n_3}\cos \omega_0 t + \frac{i_0}{n_2 - n_3}$$

Current through the secondary winding and the diode during Stage II

Solving for Mode A t_2

End condition for Mode A Stage II: $v_{ds} = 0$

$$v_{ds} = (v_i - v_p)(1 - \cos\omega_0 t) + i_{Lr}(t_0)L\omega_0 \sin\omega_0 t + v_{ds}(t_1)\cos\omega_0 t$$

$$-v_i + v_p = i_{Lr}(t_0)L\omega_0 \sin\omega_0 t + (v_i - v_p + v_{ds}(t_1))(\cos\omega_0 t)$$

$$C = A\sin\omega_0 t + B\cos\omega_0 t$$

$$t_2 = \frac{1}{\omega_0}\left(\cos^{-1}\left[\frac{C}{\sqrt{A^2 - B^2}}\right] + \tan^{-1}\left[\frac{B}{A}\right]\right)$$

Solving for Mode B t_2

End condition for Mode B Stage II: $i_2 = 0$ for $t \neq 0$

$$i_2 = \frac{v_p}{n_2 - n_3}\left[\frac{L_{in} + L_p n_3^{\,2}}{L_{in} L_p}\right]t - \frac{v_p}{\omega_0 (n_2 - n_3)}\left[\frac{L_{in} + L_p n_3^{\,2}}{L_{in} L_p}\right]\sin \omega_0 t - \frac{i_0}{n_2 - n_3}\cos \omega_0 t + \frac{i_0}{n_2 - n_3}$$

$$\frac{v_p}{n_2 - n_3}\left[\frac{L_{in} + L_p n_3^{\,2}}{L_{in} L_p}\right]t + \frac{i_0}{n_2 - n_3} = \frac{v_p}{\omega_0 (n_2 - n_3)}\left[\frac{L_{in} + L_p n_3^{\,2}}{L_{in} L_p}\right]\sin \omega_0 t + \frac{i_0}{n_2 - n_3}\cos \omega_0 t$$

$$at + b = a \sin \omega_0 t + bos \omega_0 t$$

As this is a transcendental function a recursive method can be used to determine the value of t that satisfies this equation.

MODE B STAGE III

Solving for v_{ds}

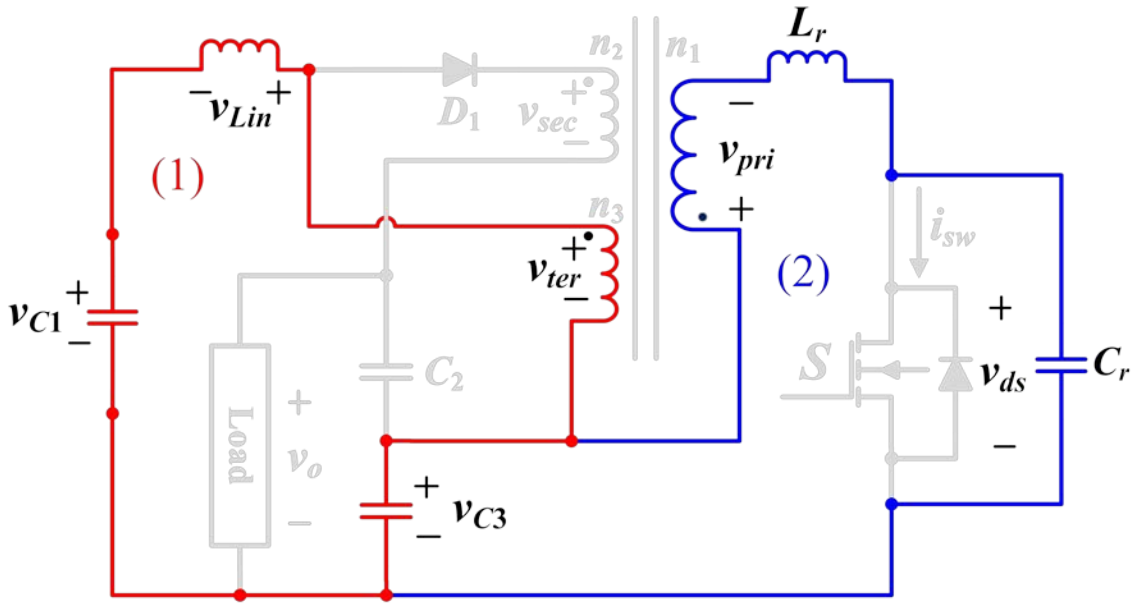

Figure A-5: Stage III for Mode B

From (2):

$$v_i = v_p + v_{Lr} + v_{ds}$$

Laplace transform

$$L\left[s\left(i_{Lr}(s)\right) - i_{Lr}(0)\right] = \frac{v_i}{s} - v_{cr}(s)$$

$$i_{Lr}(s)=\frac{\frac{\frac{v_i}{s}-v_{cr}(s)}{L}-i_{Lr}(0)}{s}$$

$$i_{Cr}=i_{Lr}$$

Laplace transform

$$C_r\left[sv_{ds}(s)-v_{ds}(0)\right]=i_{Lr}(s)$$

Substitute into *iLr*

$$C_r sv_{ds}(s)-C_r v_{ds}(0)=\frac{\frac{\frac{v_i}{s}-v_{ds}(s)}{L}-i_{Lr}(0)}{s}$$

$$C_r s^2 v_{ds}(s)+\frac{v_{ds}(s)}{L}=\frac{v_i}{sL}-i_{Lr}(0)+C_r v_{ds}(0)$$

$$v_{ds}(s)\left[1+LC_r s^2\right]=\frac{v_i}{s}-i_{Lr}(0)L+LC_r v_{ds}(0)$$

$$v_{ds}(s)=\frac{v_i}{s}\left(\frac{\omega_0{}^2}{s^2+\omega_0{}^2}\right)-i_{Lr}(0)L\left(\frac{\omega_0{}^2}{s^2+\omega_0{}^2}\right)+v_{ds}(0)\left(\frac{s}{s^2+\omega_0{}^2}\right)$$

Inverse Laplace Transform

$$v_{ds}=v_i(1-\cos\omega_0 t)+i_{Lr}(0)L\omega_0\sin\omega_0 t+v_{ds}(0)\cos\omega_0 t$$

$$v_{ds}=v_i+i_{Lr}(0)Z\sin\omega_0 t+\left(v_{ds}(0)-v_i\right)\cos\omega_0 t$$

Switch voltage equation for Stage III

Solving for t_3

End condition for Stage III: *vds* = 0

$$-v_i = i_{Lr}(0)Z\sin\omega_0 t + (v_{cr}(0) - v_i)\cos\omega_0 t$$

$$C = A\sin\omega_0 t + B\cos\omega_0 t$$

$$t_2 = \frac{1}{\omega_0}\left(\cos^{-1}\left[\frac{C}{\sqrt{A^2 - B^2}}\right] + \tan^{-1}\left[\frac{B}{A}\right]\right)$$

MODE A and B: Stage IV

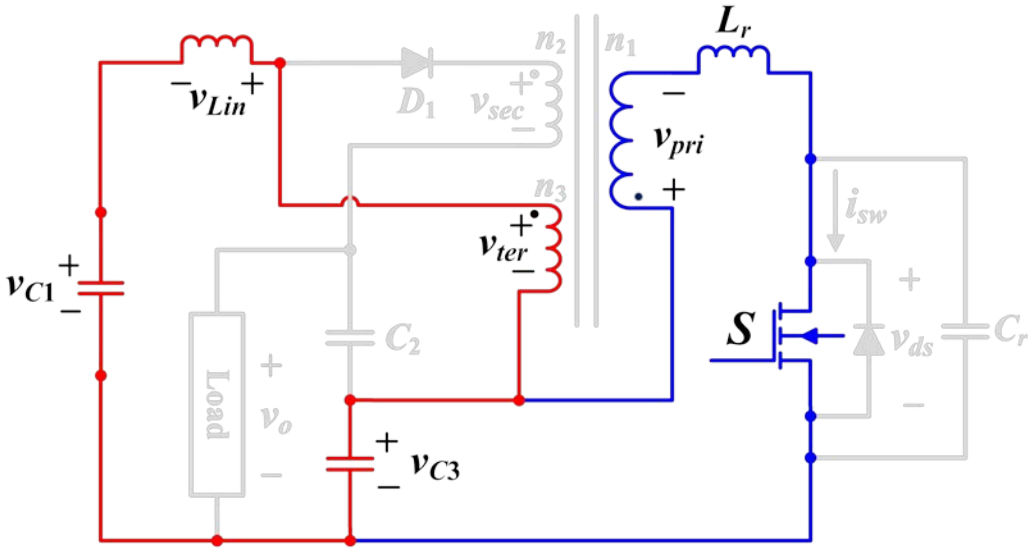

Figure A-6: Stage IV for Mode A and B

From (1):

$$v_i = v_{Lin} + v_{ter} + v_{c3}$$

$$v_{Lin} = -v_{ter}$$

$$L_{in}\left(\frac{di_3}{dt}\right) = -n_3 L_p\left(\frac{di_1}{dt} + n_3\frac{di_3}{dt}\right)$$

From (2):

$$v_{c3} = v_{pri} + v_{Lr}$$

$$v_i = L_p\left(\frac{di_1}{dt} + n_3\frac{di_3}{dt}\right) + L_r\left(\frac{di_1}{dt}\right)$$

Three Winding Coupled Inductor Design

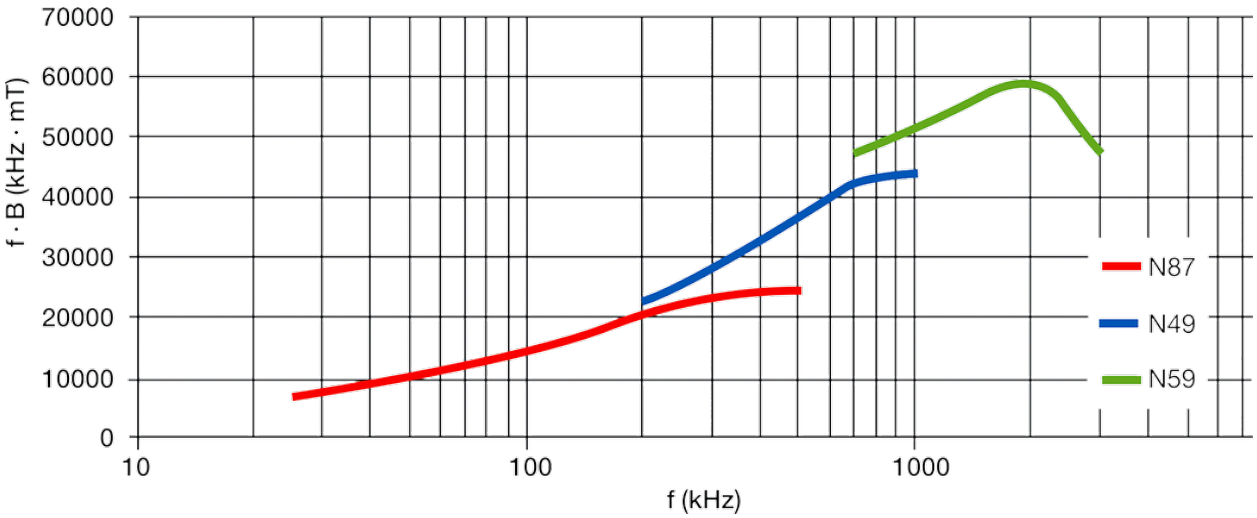

Figure A-7: Power factor as a function of frequency for different ferrite material obtained from [63]

One of the components of the proposed converter is a three winding coupled inductor. When creating the hardware prototype, this coupled inductor was required to be created by hand. Two different coupled inductors were designed for this thesis and this section will discuss the design procedure.

The determined turns ratio was to be 1:4:2 for the primary, secondary, and tertiary respectively and the magnetizing inductance was to be 45µH. When designing the inductor the two main parameters to check is the magnetic flux density and the number of turns. Fig. A-7 shows the power factor of a ferrite material as a function of frequency. From here the maximum flux

density can be obtained by dividing the power factor by the maximum circuit operating frequency.

For the first coupled inductor the chosen bobbin was an EPCOS B66252 [with dimensions of 55x28x21. The e-core used with this bobbin was an EPCOS B66335. From the datasheet it was found that the cross sectional area of the e-core was 354mm^2. From here the voltage per turn of the primary winding can be calculated by applying the equation below where f is the operating frequency, B_m is the maximum flux density, and A_e is the cross sectional area.

$$\frac{volt}{turn} = 4.44 \times f \times B_m \times A_e$$

The voltage per turn is the voltage across a single turn of the primary winding. By dividing the RMS voltage of the winding by this value the required amount of turns to prevent saturation from occurring can be determined. The RMS voltage can be obtained through simulation. The calculated voltage per turn was found to be 23.7V/turn and the RMS voltage was found to be 72V which gave a result of 3.03 turns for the primary winding. From here the required secondary and tertiary windings can be obtained by using the ratio of 1:4:2.

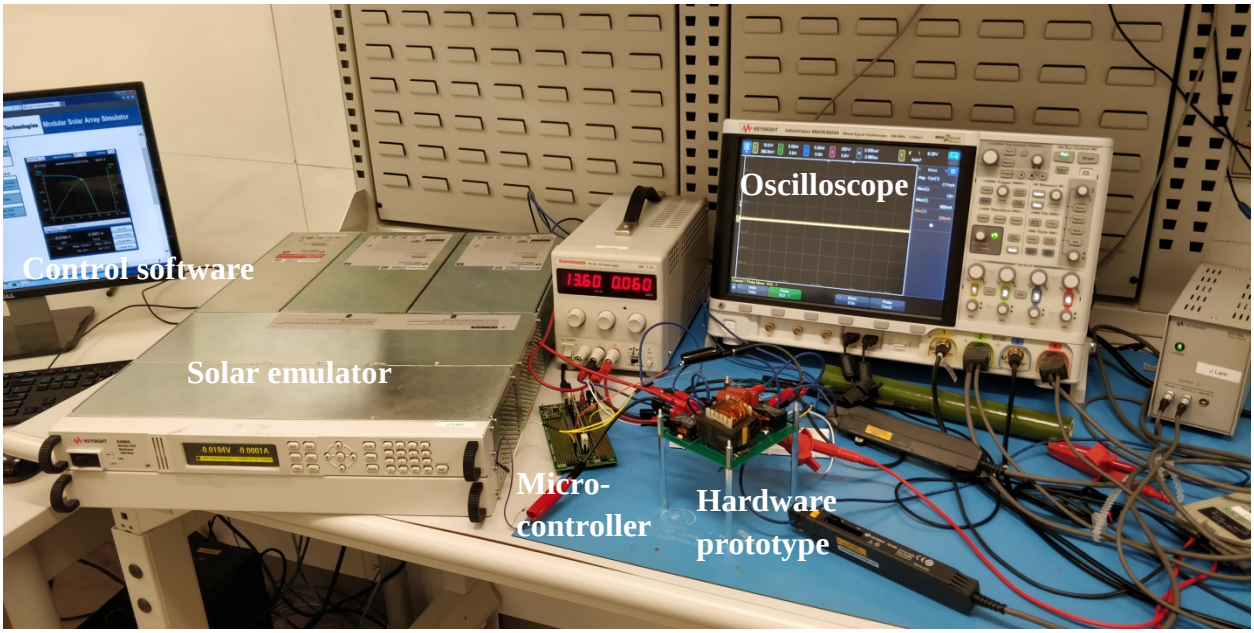

Figure A-8: Hardware experiment system overview

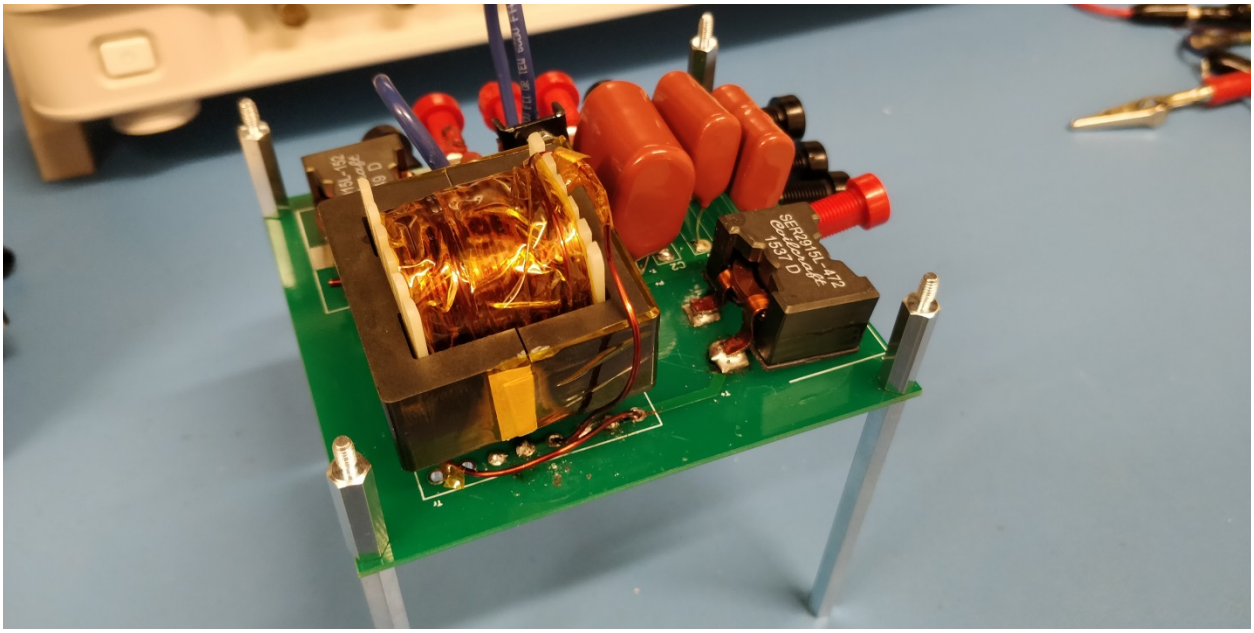

Figure A-9: Proof of concept hardware prototype

Figure A-10: Keysight E4360A Solar Emulator

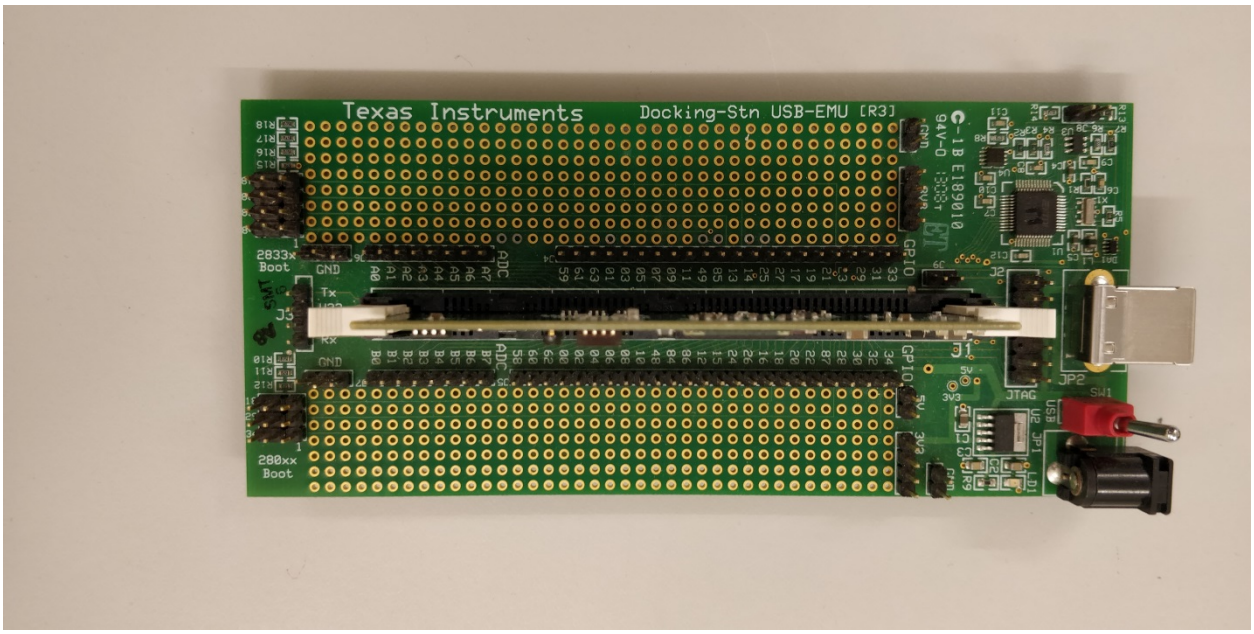

Figure A-11: TMS320 F28335 DSP

MPPT Code

```
{

v  = in[0];  // Read in the input voltage of the converter
i  = in[1];  // Read in the input current of the converter


if (outputcounter >= a)
{
p = v*i;               // Calculate the input power
oldp =  oldv*oldi;     // Calculate the input power from the previous cycle
dp = (p-oldp);         // Calculate the change in power
dv = (v-oldv);         // Calculate the change in power
di = (i-oldi);

if (p > oldp)
{

if( (p - oldp) < p/(counter*100))
{
        counter = counter;
        outputcounter = 1;
        }
else
                if (dv>0)
                {
                        if (counter >=max)
                                counter = max;
                        else
                                counter = counter + x;
                }
                else
                {
                        if (counter <= min)
                           counter = min;
                        else
                                counter = counter - x;
                }
```

```
                        outputcounter = 1;

        }

else
{

if( (oldp - p) < p/(counter*100))
{
        counter = counter;
        outputcounter = 1;
        }
else
                if (dv<0)
                {
                        if (counter >= max)
                                counter = max;
                        else
                                counter = counter + x;
                }
                else
                {
                        if (counter <= min)
                                counter = min;
                        else
                                counter = counter - x;
                }
        outputcounter = 1;
        }

outputcounter = 1;
out[0]=1;
out[2]=counter;

a = (1/((counter)*1000))/(0.01/(10*10*10*10*10*10));

oldv = v;
oldi =  i;

}

else
{
        if(outputcounter <= a*0.7)
```

```
                out[0] = 1;

        else
                out[0] = 0;

        outputcounter = outputcounter+1;

out[2] = counter;

}


}
```