TRANSFORMER DIFFERENTIAL PROTECTION UNDER GEOMAGNETICALLY INDUCED CURRENT CONDITIONS

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Abstract

Solar activities result in fluctuations in the Earth's magnetic field, referred to as geomagnetic disturbances (GMDs). During the GMDs, geomagnetically induced currents (GICs) flow through the power transformers with grounded neutrals. The transformers subjected to the GIC experience part-cycle core saturation creating significant magnetizing current harmonics, including dominant second harmonics. The GIC-caused harmonics can pose issues for protection systems, such as transformer differential relays. The majority of real-world transformer differential relays employ harmonic blocking (HB) modules to prevent malfunctions during transformer energization leading to inrush currents containing high levels of second harmonics. Considering that the GIC-related transformer current second harmonics can be significant, the differential relays are prone to be blocked during the GMDs and remain blocked for the faults occurring in their protection zones, which may damage the transformers and threaten the system's resiliency.

This dissertation conducts in-depth time-domain analyses on the performance of differential relays, equipped with various HB logics, for internal/in-zone faults under the GIC conditions. It is revealed that regardless of the employed HB logic, such relays are unwantedly blocked for the faults with specific ranges of fault resistances in the presence of GIC, and therefore, fail to trip for the faults. To address this issue, different unblocking schemes are proposed, which can detect the GIC flow in the transformer and override the blocking signals, generated by the relay's HB module, during the internal faults. The effectiveness of the developed schemes is extensively investigated to ensure (i) dependability for the co-existence of internal faults and GIC and (ii) security during the GMDs in the absence of faults as well as the transformer energization and external faults, especially under the current transformer (CT) saturation.

Moreover, detailed real-time hardware-in-the-loop (HIL) tests verify that a commercial transformer differential relay fails to operate for terminal and transformer turn faults owing to the harmonic blocking during the GIC when the post-fault different current fundamental component decreases below certain levels. Furthermore, it is shown that the relay equipped with a proposed unblocking scheme is effectively unblocked in real time and operates in the internal fault cases where the commercial relay cannot trip.

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I am grateful for all the support of my friends and relatives during the Ph.D. journey. Special thanks go to my cousins, Hamid and Hamed, for their precious insight and encouragement, which gave me extra motivation to embark on this journey.

Last but not least, I cannot thank my mother, father, and sister enough for their continuous love, support, and encouragement during my Ph.D. studies far from home.

Dedication

to my dear

mother,

father,

and sister

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List of Abbreviations

ABA	Average-Based Algorithm
ABM	Average Blocking Method
ABS	Absolute Value
AVG	Average Value
BKP	Breakpoint
CB	Circuit Breaker
CBM	Cross-Blocking Method
CME	Coronal Mass Ejection
COMTRADE	Common Format for Transient Data Exchange
CT	Current Transformer
DC	Direct Current
EC	Equivalent Circuit
EKF	Extended Kalman Filter
ESP	Earth Surface Potential
EXF	External Fault
GIC	Geomagnetically Induced Current
GMD	Geomagnetic Disturbance
HB	Harmonic Blocking
HIL	Hardware-in-the-Loop
HV	High Voltage
INF	Internal Fault
LMP	Low-Magnitude Period
LPF	Low-Pass Filter
LV	Low Voltage
MAX	Maximum

MHB	Modified Harmonic Blocking
MIN	Minimum
MMF	Magnetomotive Force
NERC	North American Electric Reliability Corporation
NOAA	National Oceanic and Atmospheric Administration
OP	Operation
PBM	Per-Phase Blocking Method
PKP	Pickup
PU	Per Unit
RCC	Rate of Change of Current
REF	Restricted Earth Fault
RES	Restraint Value
RT	Restraint
RTDS	Real-Time Digital Simulator
SBM	Summing-Type Blocking Method
SC	Short-Circuit
SCL	Short-Circuit Level
SHR	Second Harmonic Ratio
SNR	Signal-to-Noise Ratio
SUP	Supplementary
UB	Unblocking
WGD	Waveform-Based GIC Detection

Nomenclature

$\boldsymbol{D}$	Waveform asymmetry index of average-based algorithm
$\mathbf{d}\boldsymbol{I}/\mathbf{d}\boldsymbol{t}$	Current derivative
$\boldsymbol{dRCC}$	Difference between the rate of change of currents
$\boldsymbol{i}_1$	Scaled-down transformer current on HV side
$\boldsymbol{i}_2$	Scaled-down transformer current on LV side
$\bar{\boldsymbol{I}}_1$	Fundamental-frequency phasor of i_1
$\bar{\boldsymbol{I}}_2$	Fundamental-frequency phasor of i_2
$\boldsymbol{I}_{\mathbf{2nd}}$	Differential current second harmonic magnitude
$\boldsymbol{I}_{\mathbf{4th}}$	Differential current fourth harmonic magnitude
$\boldsymbol{I}_{\mathbf{5th}}$	Differential current fifth harmonic magnitude
$\boldsymbol{I}_{\mathbf{bkp}}$	Breakpoint current
$\boldsymbol{I}_{\mathbf{h}}$	Differential current h^{th} harmonic magnitude
$\boldsymbol{I}_{\mathbf{op}}$	Operation current
$\boldsymbol{I}_{\mathbf{pkp}}$	Pickup current
$\boldsymbol{I}_{\mathbf{rt}}$	Restraint current
$\boldsymbol{I}_{\mathbf{unrt}}$	Unrestrained current
$\boldsymbol{i}_{\mathbf{CT}}$	CT current
$\boldsymbol{i}_{\mathbf{Diff}}$	Differential current waveform
$\boldsymbol{L}_{\mathbf{0\text{-}air}}$	Inductance of transformer winding's surrounding air
$\boldsymbol{L}_{\mathbf{0\text{-}Avr}}$	Equivalent inductance of transformer zero-sequence characteristics
$\boldsymbol{L}_{\mathbf{12}}$	Short-circuit inductance
$\boldsymbol{L}_{\mathbf{CW}}$	Air-path inductance between main leg and LV-side transformer winding
$\boldsymbol{L}_{\mathbf{gap}}$	Inductance of airgap between transformer's core and tank
$\boldsymbol{L}_{\mathbf{m}}$	Saturable inductance of transformer core's main leg
$\boldsymbol{L}_{\mathbf{tank}}$	Inductance of the transformer tank

L_{yoke}	Inductance of yokes between two adjacent transformer core legs
n_{HV}	Transformer's HV-side turns ratio
n_{LV}	Transformer's LV-side turns ratio
R_{F}	Short-circuit fault resistance
RCC_{rt}	Rate of change of restraint current
S_{A}	Average-based algorithm's output
S_{Block}	Gap detection algorithm's output
S_{EXF}	External fault detection logic's output
S_{GIC}	GIC detection module's output
S_{H}	Harmonic-based algorithm's output
S_{HB}	Harmonic blocking signal
S_{HB2}	Second harmonic blocking signal
S_{HB5}	Fifth harmonic blocking signal
S_{HBh}	h^{th} harmonic blocking signal
S_{MHB}	Modified harmonic blocking signal
S_{PKP}	Output of "OR" gate receiving relay's pickup signals
S_{RCC}	Rate of change of operation current detection logic's output
S_{S}	Shift-based algorithm's output
S_{Sup}	Supplementary module's output
S_{UB}	Unblocking signal
S_{UBNOT}	Logical "NOT" of unblocking signal
S_{W}	Waveform-based method's output
Si_{Diff}	Shifted differential current waveform
$Sum\text{-}I_{\mathrm{h}}$	Sum of three-phase differential current h^{th} harmonic magnitudes
s_1	First slope of differential relay's operation-restraint characteristic
s_2	Second slope of differential relay's operation-restraint characteristic
T	One cycle
t	Time
t_{D}	Dropout time setting of relay's trip signal

t_{LMP}	Low-magnitude period's time duration
t_{P}	Pickup time setting of relay's trip signal
t_{PKP}	Pickup time setting of relay's pickup signal
t_{set}	Pickup/dropout time setting
thr_{2nd}	Second harmonic blocking threshold
thr_{4th}	Fourth harmonic blocking threshold
thr_{5th}	Fifth harmonic blocking threshold
thr_{AVG}	Average-based algorithm's threshold
thr_{dRCC}	External fault detection logic's *dRCC* threshold
thr_{h}	h^{th} harmonic blocking threshold
thr_{RCC}	Rate of change of current detection threshold
$thr1$	WGD (shift-based) algorithm's current threshold
$thr2$	WGD (shift-based) algorithm's lower time-ratio threshold
$thr3$	WGD (shift-based) algorithm's upper time-ratio threshold
tr	Time-ratio calculated by WGD (shift-based) algorithm
V_{HV}	Transformer's HV-side terminal voltage
V_{LV}	Transformer's LV-side terminal voltage
Z^{+}	Positive-sequence impedance
Z^{-}	Negative-sequence impedance
Z^{0}	Zero-sequence impedance
Z_{SC}	Short-circuit impedance
ΔI_{op}	Change of operation current in a time window
Θ_{I2nd}	Differential current second harmonic phase angle
Θ_{I2ndp}	Filtered differential current second harmonic phase angle
Θ_{set}	Harmonic-based algorithm's phase angle threshold
Φ	Magnetizing flux
Φ_{0}	GIC-caused zero-sequence flux
Φ_{m}	Magnetizing flux of transformer core's main leg

$\mathscr{R}_{\mathbf{o\text{-}air}}$	Reluctance of transformer winding's surrounding air
$\mathscr{R}_{\mathbf{gap}}$	Reluctance of airgap between transformer's core and tank
$\mathscr{R}_{\mathbf{tank}}$	Reluctance of transformer tank

Chapter 1

Introduction

1.1 Background

In this section, first, it is discussed what geomagnetically induced current (GIC) is and how it is created in power systems. Afterward, the general impacts of geomagnetic disturbances (GMDs) on power systems and mitigation approaches from the system point of view are stated. Furthermore, a brief review of the GIC effects on the protection schemes is presented.

1.1.1 Geomagnetically Induced Current

Solar activities, comprised of sunspots, solar flares, and coronal mass ejections (CMEs), follow a cycle of 11 years. These activities cause the emission of protons and electrons plasma from the sun, known as solar wind particles. The complex interaction between these particles and the Earth's magnetic field, i.e., geomagnetic field, results in electrojets that are auroral currents as big as millions of amperes, located in the ionosphere, the area between the lower atmosphere and the vacuum of space [1, 2]. The auroral currents lead to the fluctuations of the geomagnetic field, referred to as the GMD [1], inducing electric fields at the Earth's surface [3]. The induced electric field, called earth surface potential (ESP), can get as high as 6 V/km [4] and is key to the GIC determination in a power system [5]. How the GICs are created can be explained using Faraday's and Ohm's laws. A varying geomagnetic field leads to an electric field (Faraday's law), which causes the currents to flow through the conductors (Ohm's law) [5]. The duration of a GMD is about 1 to 2 days, intermittently producing high levels of the GICs, but continuously creating low and moderate levels of these currents. Compared to the nominal frequency of 50 or 60 Hz, the GICs can be counted as quasi-DC currents since their frequency is in the range of 0.1 mHz to 0.1 Hz [6]. Similar to the zero-sequence currents, the quasi-DC GICs have the same magnitudes and phase angles in three phases; thereby, these currents exist where there are transformers with grounded neutrals [7, 8].

1.1.2 A Review of Major GMD Events

According to the recorded data, the power systems in Canada and the United States experienced one of the first GMD-caused failures in March 1940, where for example, Philadelphia Electric Company reported significant voltage and reactive power variations [4]. In March 1989, a CME, as the most important solar phenomenon [3], led to a highly destructive GMD which blacked the Hydro-Quebec power system out for about 9 hours. It also damaged a power plant transformer on the east coast (New Jersey) of the United States [5, 9]. This event played a pivotal role in directing the research towards the GMD effects on power systems and the measures that should be taken to mitigate the effects [1, 4]. Another considerable GMD event was recorded in southern Sweden in October 2003, which caused a blackout [3, 10, 11]. The most recent solar storm, creating tangible GIC levels in the power lines of the Kola peninsula, Russia, was reported in March 2015 [12].

Although the GMDs affecting the performance of power systems are mainly reported in regions with high latitudes, including Canada, Finland, and Scandinavia, the systems located in the lower latitudes, such as the United States, China, and Japan, also experience GIC-related events, which suggests taking such disturbances serious worldwide [3].

1.1.3 GMD Impacts on Power Systems and Mitigation Measures

The impacts of solar geomagnetic storms on power systems and equipment are extensively discussed in the literature [1, 6, 13-15]. The source of issues, raised during the GIC flow, is the core saturation of the transformers with the grounded neutrals [9]. The direct consequences of GIC-caused part-cycle saturation of the transformer core are the harmonic currents, increase in the transformer reactive power consumption, and transformer hot-spot heating [1, 10, 16]. In general, the performance of protective relays can be affected by the harmonics, and voltage instability is likely a result of the higher reactive power demand [10, 17]. Table 1.1 summarizes the potential effects of GMDs with various severity levels on power systems, as forecasted by the U.S. National Oceanic and Atmospheric Administration (NOAA) [4].

TABLE 1.1. POSSIBLE GMD IMPACTS ON POWER SYSTEMS [4]

Level of Severity	Possible Impacts
Extreme	• Damage to the transformers • Wide-area control and protection issues • Blackouts
Severe	• Wide-area voltage control problems • Malfunctions of the protective relays
Strong	• Significant voltage issues • False alarms triggered by the protective relays
Moderate	• Damage to the transformers for long-lasting events • Tangible voltage variation in the power systems located in the regions with high latitudes
Minor	• Minor voltage, current, and power fluctuations

The followings are some measures to alleviate the GMD impacts on power systems and provide more resiliency under the GIC conditions:

- Installing the blocking devices at the transformers' neutrals [18-22] to prevent/limit the GIC flow in the transformers.

- Inserting series capacitors in the transmission lines [23] to confine the GIC flow and improve the system stability.
- Reducing the system loading and providing adequate reactive power supply by switching devices, such as shunt capacitor banks [23, 24], in order to address the voltage issues and avoid voltage instability.

The GIC monitoring networks, such as Hydro One's monitoring network, can provide the operators in control rooms with the necessary data on power system conditions to take proper mitigation actions during the GMDs [24]. Furthermore, there are reliability and planning standards, developed by North American Electric Reliability Corporation (NERC) [25, 26], for the safe operation of the power systems in the presence of GIC [10].

1.1.4 GIC Effects on Protection Schemes

The malfunctions of protective relays mainly caused the blackouts in the Hydro-Quebec and Swedish power networks during the GMDs in 1989 and 2003, respectively [23, 27, 28]. Hence, it is essential to investigate the performance of protective relays during the GMDs in order to pinpoint the potential issues and develop methods to avoid possible failures/malfunctions of protection schemes under the GIC conditions.

The GIC effects on protection schemes, such as overcurrent [29-33], negative-sequence [1, 21, 34], and distance relays [30, 35], are discussed in the literature. According to the studies of [29], due to the harmonics divisible by three caused by the transformer core saturation under the GIC conditions, less sensitive settings are required to avoid the maloperation of zero-sequence overcurrent relays that function based on the RMS value of zero-sequence current waveform. Slightly delayed operation of overcurrent relays is likely for in-zone short-circuit faults in view of current transformer (CT) saturation caused by the GIC [30]. Neutral overcurrent relays of the shunt capacitors are prone to maloperation under the GIC conditions since the capacitors represent lower impedances as exposed to the harmonics, compared to the fundamental frequency [31]. The performance of negative-sequence protection, such as generator negative-sequence relays, can be affected by the GIC-caused harmonics, resulting in malfunctions [21, 31, 34]. According to the studies of [30, 32, 35], the distance relays may underreach and operate with a delay for in-zone faults owing to the GIC-related CT saturation.

1.2 Problem Statement

Differential relays, the main protection scheme of transformers, employ harmonic blocking (HB) modules [36-40]. The HB module is utilized to avoid malfunctions and provide security by blocking the differential relay operation if the transformer currents heavily include harmonics in conditions such as transformer energization resulting in inrush currents [38, 41-43]. As discussed in Subsection 1.1.3, the transformer harmonic currents are also elevated during the GIC because of the part-cycle core saturation [21, 39]. Therefore, the transformer differential relays are vulnerable during the GMDs such that these relays may not be dependable for in-zone/internal faults under the GIC conditions due to the unwanted harmonic blocking. One possible consequence of the differential protection blocking for the internal faults during the GIC flow is irreversible damage to the transformers. The uninterrupted in-zone faults also increase the chance of power system instability and blackout. It may be implied that the co-exitance of transformer faults and GMDs is a low-probability concern, assuming that the GMDs and the in-zone faults are independent events with low probabilities. Nevertheless, the transformer faults are not necessarily independent of the GMDs since the GIC-caused electrical and thermal stresses in power transformers mostly make them undergo internal faults.

It should be noted that harmonic restraint-based schemes and non-harmonic-based methods, such as waveform-based inrush detection methods, can also be employed to restrain/block the differential relay operation in the transformer energization conditions [40, 44-48]. However, as the absolute majority of the existing real-world differential relays utilize the HB methods, this dissertation focuses on HB-based transformer differential protection. Subsections 1.2.1 and 1.2.2 highlight the dearth of detailed studies on the performance of transformer differential relays under the GIC conditions.

1.2.1 Transformer Differential Protection

Although in the literature [37, 38, 49-52], the performance of transformer differential protection is extensively studied under conditions, such as internal and out-of-zone/external faults, inrush and sympathetic inrush currents, overexcitation, and transformer winding deformation, the number of publications discussing the GIC effects on transformer differential protection is limited. The studies of [38, 51] compare the performance of the transformer differential protection equipped with different HB schemes, including common and independent HB methods, for the inrush currents and faults; nevertheless, these studies are not carried out under the GIC conditions. Different HB methods are introduced in detail in Chapter 2.

1.2.2 Transformer Differential Protection during GMDs

In [39], it is shown that the transformer differential protection is secure even under extremely high GIC magnitudes, owing to the HB module. In this reference, however, no study is conducted on the differential relay behavior during the faults in the presence of GIC. In spite of providing no time-domain simulation results related to the differential protection performance, the studies done in [53] predict that this protection scheme is unlikely to trip for the internal faults in the presence of GIC owing to the CT saturation. Furthermore, the authors in [54, 55] believe that the GIC may not affect the differential relay performance during the internal and external faults, provided that the CTs are adequately selected to avoid CT saturation. Nevertheless, the CT performance under the GIC condition is analyzed in detail in [30], concluding that the GIC-caused CT saturation does not have significant effects on the operation of the differential relays. In [54], it is also stated that the differential relays with independent HB methods do not have difficulty operating for the internal fault when the transformer is exposed to the GMD-caused DC bias; however, this reference does not conduct any simulation-based investigation to verify this statement.

Transformer differential protection may not operate for the internal faults because of the transformer core saturation under the GIC conditions, as discussed in [35, 56]. The studies of [35, 56], however, lack detailed simulations to prove that the differential protection fails to trip for the faults during the GMDs. The results obtained in [57] necessitate the investigation of the differential relay performance during the internal faults while the transformers are exposed to the GIC. According to the detailed studies of [58], both harmonic-based and restraint-based differential relays are prone to lose dependability for internal faults under the GIC conditions. The studies of [58], however, do not include different transformer models, such as the three-leg transformer model [59, 60], independent HB schemes, different transformer loading conditions, winding/turn faults, and CT saturation.

1.3 Research Objectives

This research aims at improving the dependability of existing transformer differential relays for in-zone faults under the GIC conditions, while maintaining security in conditions such as out-of-zone faults and inrush currents. Accordingly, this dissertation pursues the following objectives:

1. Detailed performance evaluation of transformer differential relays under the GIC conditions is carried out by running both offline simulations and real-time hardware-in-the-loop (HIL) simulations involving a modern commercial transformer differential relay in order to prove the likelihood of failure in operation and show the need for devised protection schemes to ensure the differential relay dependability in the presence of GIC. The studies are conducted by employing an accurate transformer model, as introduced in [59, 60], with a focus on phase operation-restraint differential protection [61] equipped with the HB module. Performance analysis of other transformer protection schemes, such as restricted earth fault (REF) [62, 63] and negative-sequence differential relays [58], is not covered in this research.
2. In Subsection 1.1.3, the installation of GIC blocking devices is discussed as a system-point-of-view solution to avoid transformer part-cycle core saturation, and therefore, the GIC-caused harmonic effects on the differential protection performance. However, such GIC blocking solutions can be costly, complicated, and affecting the performance of protective relays [20]. Thereby, this research focuses on developing protection algorithms/logics to be embedded in existing differential relays for dependability improvement during the GMDs without endangering security. The developed schemes are based on the GIC detection algorithms and fault detection logics, which employ the differential relay's available signals and do not require the installation of additional devices.
3. Extensive offline and real-time performance verification of the developed protection schemes is conducted to show the effectiveness in improving the performance of the differential relays during the internal faults under the GIC conditions, while maintaining security in conditions such as the external faults and inrush currents.

1.4 Dissertation Outline

The rest of this dissertation is organized as follows.

Chapter 2 explains the operation-restraint characteristics of transformer differential protection and presents a generic operation logic of the differential relays. Different HB approaches are also discussed in this chapter.

Chapter 3 scrutinizes the differential relay performance in the presence of GIC using time-domain simulations run in EMTP, considering both common and independent HB methods, and reveals the relay failure cases during the internal faults and GIC due to the unwanted harmonic blocking. Different HB thresholds and transformer loading conditions are considered in the studies of this chapter.

Chapter 4, first, conducts a review of available GIC monitoring and detection schemes. Afterward, this chapter proposes a protection scheme, utilizing a harmonic-based GIC detection algorithm, to unblock the differential relays for the internal faults during the GMDs. The proposed scheme's effectiveness is examined in several GIC- and non-GIC-based scenarios, with and without the CT saturation. Different transformer models are employed to illustrate the scheme's capability to unblock the differential relays for internal faults.

Chapter 5 introduces an alternative unblocking scheme, based on a waveform-based GIC detection algorithm, and investigates the scheme's dependability and security in numerous conditions such as the internal and external faults as well as the inrush currents with and without remnant fluxes. Moreover, the effectiveness of the waveform-based GIC detection algorithm is verified for the measurement noise and different transformer winding connections.

Chapter 6 proposes a hybrid GIC detection approach by combining the harmonic- and waveform-based GIC detection algorithms to achieve more reliability and accuracy in GIC detection. The waveform-based part is supervised by an average-based GIC detection algorithm. This chapter also proposes an external fault detection logic for the unblocking scheme. The proposed scheme performance is extensively analyzed, considering various scenarios including different GIC magnitudes.

Chapter 7 represents the real-time validation test results. First, a detailed response evaluation of a commercial differential relay to the terminal and turn faults in the presence of GIC is carried out using an HIL test setup, showing that there are fault scenarios in which the real-world relay fails to operate. Then, the performance of the proposed scheme of Chapter 6 is validated for the internal faults under the GIC condition using the real-time digital simulator (RTDS) [64].

Chapter 8 concludes the dissertation and suggests some topics for future research.

Chapter 2
Differential Protection Fundamentals

2.1 Differential Relay Characteristics

Figure 2.1 shows a differential relay (87) employed to protect a transformer against internal short-circuit faults that occur between each CT and the transformer. In this figure, i_1 and i_2 are the transformer's HV- and LV-side currents that are scaled down by CT_1 and CT_2, respectively. The relay sends a trip signal to open the circuit breakers (CBs) on both the HV and LV sides, provided that there is an internal fault occurrence. For the external faults, e.g., occurring between the CTs and CBs in the figure, the relay is expected not to operate and issue a trip.

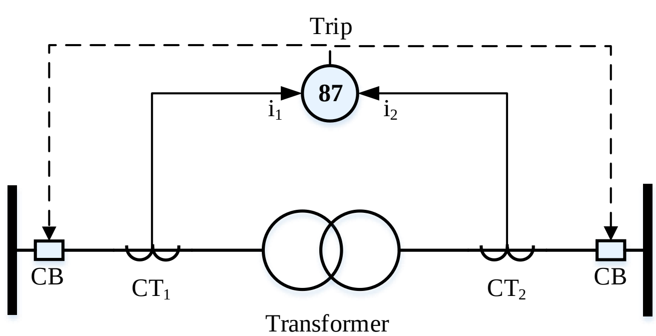

Figure 2.1. A differential relay (87) protecting a transformer.

A typical dual-slope operation-restraint characteristic of the differential protection [61, 65, 66], is shown in Figure 2.2. This figure also depicts the single-slope characteristic which is less secure than the dual-slope characteristic for the external faults, especially during the CT saturation [61]. In Figure 2.2, the vertical axis is the differential current fundamental component or the operation current (I_{op}) which is calculated by (2.1) for all three phases. In this equation, $\overline{I_1}$ and $\overline{I_2}$, respectively, are the phasor values of i_1 and i_2 in Figure 2.1, after the necessary magnitude and phase angle compensations [61, 67] in order to avoid significant I_{op} magnitudes in normal operating conditions. The current magnitude compensation takes into account the transformer ratio, CTs' ratios, and transformer tap location. The phase angle compensation, on the other hand, applies the necessary phase shift in the HV- or LV-side CT's secondary current of each phase, based on the transformer winding connection and vector group, in order to yield a 180° phase angle difference between $\overline{I_1}$ and $\overline{I_2}$ of each phase. The horizontal axis is the restraint current (I_{rt}) that can be determined using (2.2), (2.3), or (2.4) [38, 61]. I_{pkp} and I_{bkp} are respectively the pickup and breakpoint currents. For the dual-slope characteristic, the slope changes from s_1 to s_2 once I_{rt} exceeds I_{bkp}.

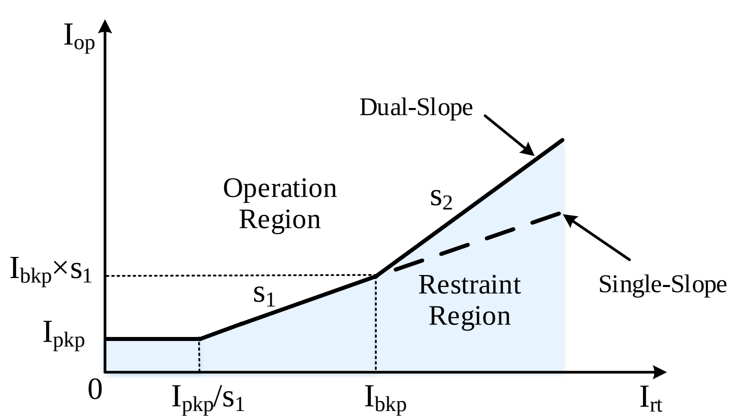

Figure 2.2. Operation-restraint characteristics of differential protection.

$$I_{op} = |\overline{I_1} + \overline{I_2}| \tag{2.1}$$

$$I_{rt} = |\overline{I_1}| + |\overline{I_2}| \tag{2.2}$$

$$I_{rt} = {(|\overline{I_1}| + |\overline{I_2}|)}/{2} \tag{2.3}$$

$$I_{rt} = MAX\ (|\overline{I_1}|, |\overline{I_2}|) \tag{2.4}$$

The I_{pkp} setting in Figure 2.2 determines the minimum I_{op} required for the relay operation and is set high enough to avoid malfunctions in normal conditions (in the absence of faults), considering factors such as CT errors and on-load tap changing [68]. The first slope (i.e., s_1) is set such that the relay remains sensitive and dependable for high impedance/low-current internal faults while maintaining security for distant external faults [65, 67, 68]. As mentioned above, the second slope (s_2) in Figure 2.2 is to provide more security for heavy external faults [65, 68]. Moreover, the slope setting of a single-slope characteristic can be adaptively switched to a larger setting during the external faults to improve security [67].

2.2 Differential Relay's Operation Logic

A generic logic of operation-restraint differential relay is illustrated in Figure 2.3 for phase A. The corresponding logics of phases B and C are similar. In Figure 2.3, the restraint value (RES), as a function of I_{rt}, is calculated by (2.5) that is derived based on the dual-slop characteristic of Figure 2.2. Considering Figure 2.3, if I_{op} is larger than RES, i.e., the point (I_{rt}, I_{op}) is located in the operation region (Figure 2.2), a pickup (PKP) signal is issued after an adjustable pickup time t_{PKP}.

$$RES = \begin{cases} I_{pkp} & 0 \le I_{rt} < \frac{I_{pkp}}{s_1} \\ I_{rt} \times s_1 & \frac{I_{pkp}}{s_1} \le I_{rt} < I_{bkp} \\ (I_{rt} - I_{bkp}) \times s_2 + I_{bkp} \times s_1 & I_{bkp} \le I_{rt} \end{cases} \tag{2.5}$$

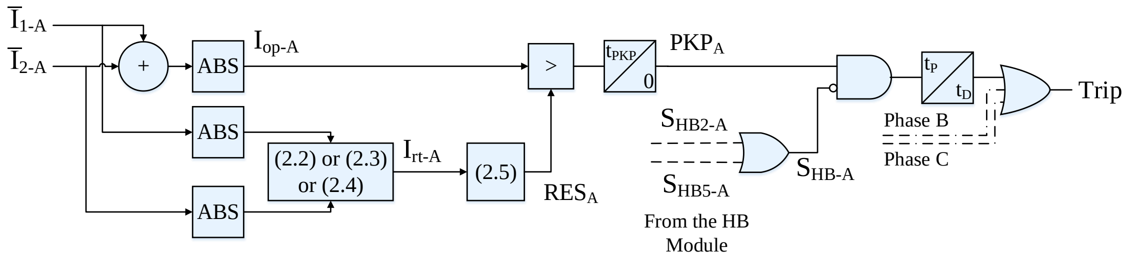

Figure 2.3. The generic logic of operation-restraint transformer differential protection for phase A.

In Figure 2.3, S_{HB2} and S_{HB5} are, respectively, the second and fifth harmonic blocking signals issued by the relay's HB module. Different HB logics are discussed in detail in Section 2.3. For each phase, if either S_{HB2} or S_{HB5} changes from 0 to 1, the resulting harmonic blocking signal (S_{HB}) is set to 1; subsequently, that phase is blocked and does not contribute to sending the trip signal to the CBs (Figure 2.1), even if there is a *PKP* associated with the phase. Otherwise, the trip signal is issued after the pickup time of t_P. In Figure 2.3, t_D is the dropout time to ensure that the trip signal remains asserted for a specific time period. In the offline simulation studies of this thesis, t_p is set at 0 s and t_D is set such that the trip signal, once asserted, is sealed in and does not reset to the end of the simulation runtime.

In the case of a harmonic restraint-based differential relay [66, 67], the relay picks up and operates if the criterion in (2.6) is met. In (2.6), I_{2nd} and I_{4th} are the magnitudes of the second and fourth harmonic components of the differential currents, respectively. The settings, thr_{2nd} and thr_{4th}, denote the second and fourth harmonic blocking thresholds in percent (%), respectively. As discussed in Chapter 1, the harmonic restraint-based element is not covered in this thesis.

$$I_{op} > RES + \left(\frac{100}{thr_{2nd}} \times I_{2nd}\right) + \left(\frac{100}{thr_{4th}} \times I_{4th}\right) \tag{2.6}$$

2.3 Harmonic Blocking Methods

The HB methods employed in transformer differential protection are divided into two categories: (i) common HB and (ii) independent HB approaches [38, 40, 49, 69]. Regarding the common HB methods, such as cross-blocking method (CBM) and average blocking method (ABM), the differential protection is blocked for all three phases at the same time if a harmonic-based requirement is met. However, the harmonic blocking is separately done for each phase when an independent HB method, such as per-phase blocking method (PBM) or summing-type blocking method (SBM), is utilized. Unlike the common HB methods, the independent approaches can face security issues during the transformer energization, and therefore, the differential relays equipped with these approaches are prone to maloperation for the inrush currents [38]. On the contrary, dependability is the main challenge for the common HB methods such that a common HB-based differential relay is likely to operate with a delay [49] or not to be able to operate at all [38] for the internal faults in the transformer energization conditions. Logics of the CBM, ABM, PBM, and SBM are presented in this section.

2.3.1 Cross-Blocking Method

The CBM logic is shown in Figure 2.4, in which I_h is the magnitude of the differential current h^{th} harmonic component. According to Figure 2.4, if the ratio of I_h to I_{op} (I_h/I_{op}) in any phase is higher than a predetermined HB threshold for the h^{th} harmonic component (thr_h), S_{HBh} of that phase becomes 1. This results in the differential protection blocking for all three phases as $S_{HBh-ABC}$ is set to 1, which means that no trip signal is issued even if there is a *PKP* associated with a phase.

The CBM is generally used for transformer differential protection to prevent malfunctions in the case of inrush currents [54, 70, 71]. The authors in [72] recommend employing this method in order to provide more secure differential protection for the transformers that present low levels of second harmonic components during the energization. However, based on the analysis done in [38], the CBM dependability is low.

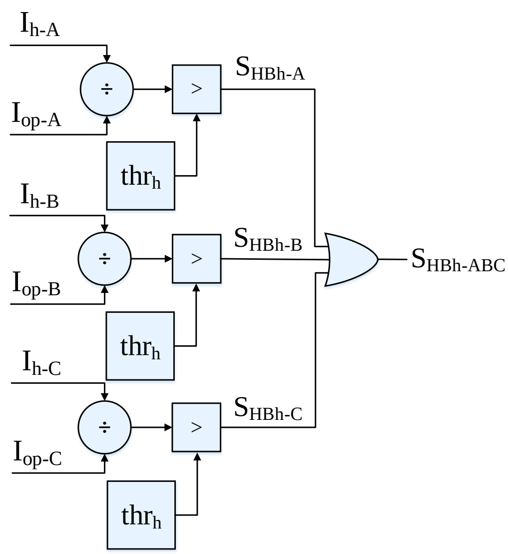

Figure 2.4. The logic of the cross-blocking method for the h^{th} harmonic component.

2.3.2 Average Blocking Method

The ABM determines the average ratio of I_h to I_{op}, as depicted in Figure 2.5. The differential relay blocks the three phases if *Average Ratio* is higher than thr_h. Despite better dependability than the CBM, the ABM can still prevent the relay operation during the faults and transformer energization, provided that the I_h-to-I_{op} ratios in the healthy phases are large enough [38].

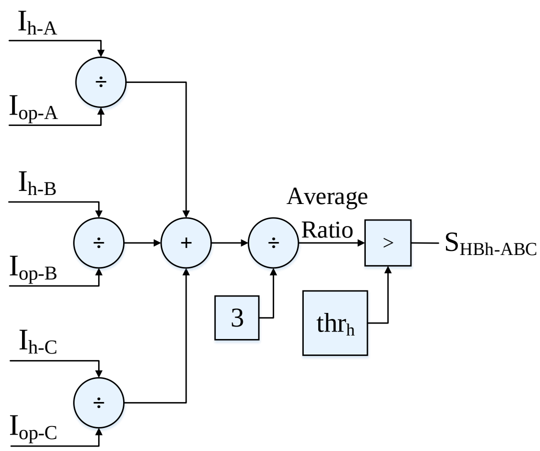

Figure 2.5. The logic of the average blocking method for the h^{th} harmonic component.

2.3.3 Per-Phase Blocking Method

Figure 2.6 shows the PBM logic. The harmonic blocking is independently performed by the PBM for the three phases, which means that there are three different S_{HBh} signals issued by the HB module in this case, unlike the CBM and ABM generating a similar HB signal for all the phases (Figures 2.4 and 2.5). Accordingly, a PBM-based differential relay is able to operate for a fault even if the S_{HBh} signals of two phases are asserted while S_{HBh} of the faulted phase is 0. Although the PBM is the least secure method in transformer energization cases [38, 51, 72], it provides the relay with high dependability during internal faults.

2.3.4 Summing-Type Blocking Method

As depicted in Figure 2.7, the SBM calculates the sum of I_h of the three phases (*Sum*-I_h), divides it by I_{op} in each phase, and compares the resulting values with thr_h. Similar to the PBM, the SBM performs the harmonic blocking independently; nonetheless, the SBM is superior to the PBM in terms of security during the inrush currents [38].

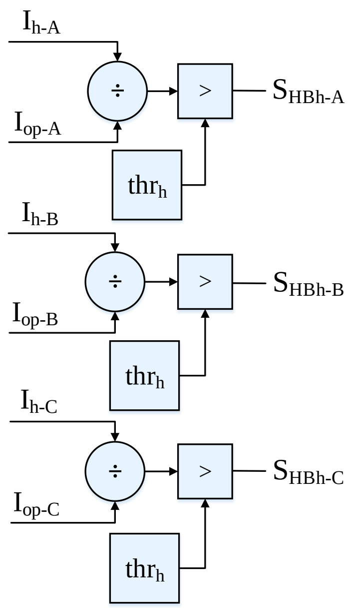

Figure 2.6. The logic of the per-phase blocking method for the h^{th} harmonic component.

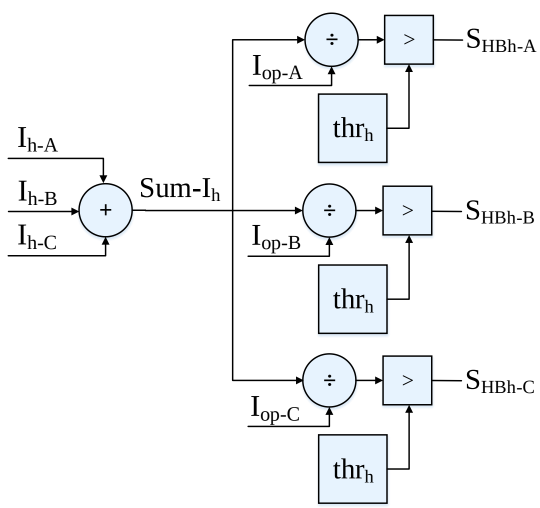

Figure 2.7. The logic of the summing-type blocking method for the h^{th} harmonic component.

2.3.5 2-out-of-3 Blocking Method

This harmonic blocking scheme blocks the relay operation for the three phases if the I_h-to-I_{op}ratios in two phases exceed the corresponding HB threshold [68, 72]. Therefore, in terms of dependability during internal faults, the 2-out-of-3 method is superior to the CBM (1-out-of-3) while still less dependable than the PBM (3-out-of-3). Moreover, this method provides more security compared to the PBM during the inrush currents; however, it is less secure than the CBM. Considering these intermediate characteristics, and also not being as common as the CBM and PBM, the performance of the 2-out-of-3 scheme is not included in the studies of this thesis.

2.4 Summary

The operation-restraint characteristics and generic logic of transformer differential relays were presented in this Chapter. Furthermore, different common and independent HB methods with their logics were discussed. The performance of HB-based differential relays for the in-zone faults is investigated in the next chapter.

Chapter 3
Differential Protection Performance Analysis

3.1 Study System

Figure 3.1 shows the single-line diagram of the study system. In this system, a 500 kV transmission grid with a short-circuit level (SCL) of 40 kA is connected to a 125 MVA, 500/115 kV three-phase transformer through a double-circuit transmission line with a length of 100 km. On the LV side, the transformer energizes a 115 kV sub-transmission network that includes a short 115 kV line supplying a 62.5 MVA load at its remote end. The transmission lines and the load are modeled as the constant parameter and constant impedance, respectively. The transformer winding connection is assumed to be the grounded wye on both HV (500 kV) and LV (115 kV) sides. The three-leg transformer model employed in this chapter is the same as the one presented in [59, 60]

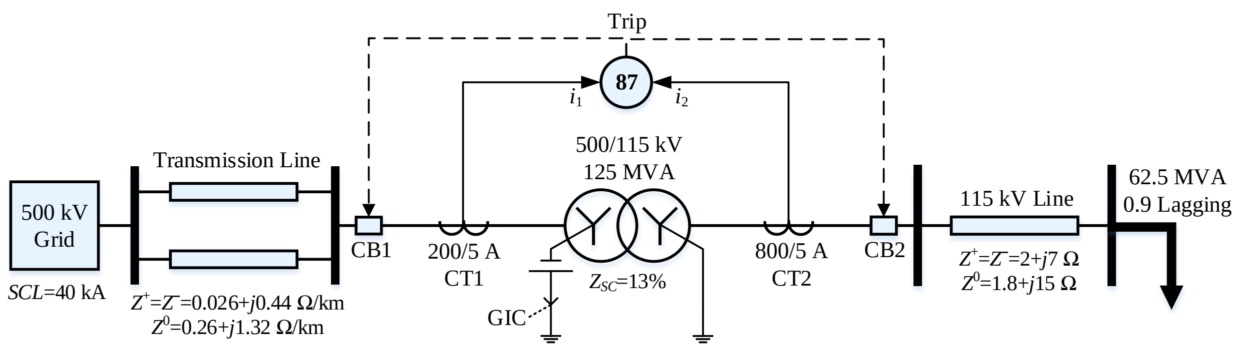

Figure 3.1. Single-line diagram of the study system.

and validated using the GIC experimental results in [16, 60]. More details on the transformer model are provided in Subsection 3.1.3. The study system of Figure 3.1 is implemented in EMTP.

3.1.1 Differential Relay and CTs

As depicted in Figure 3.1, the transformer is protected by a differential relay which receives the scaled-down currents (i_1 and i_2) from 200/5 A and 800/5 A CTs. These ratios are determined by considering the transformer's rated currents on the HV and LV sides with a margin of 25% [73], and selected based on the closest standard CT ratios, as provided in [74]. Furthermore, using these CT ratios, the maximum permissible current on the CTs' secondary sides is not violated during a bolted three-phase external fault on the transformer's LV side in the study system, leading to the maximum fault current. The maximum permissible current is typically defined as 20 times the CT's rated secondary current [67, 75]. The CTs are of class C200 with a burden of 2 Ω [74]. It should be noted that the CT saturation is not modeled in this chapter to solely examine the effects of GIC-caused transformer core saturation on the differential relay performance during the faults. In this regard, a linear core is considered for the CTs of Figure 3.1.

The settings of the relay are given in Table 3.1, which are the default settings of the differential relay model in EMTP [76]. It should be noted that these settings only affect the fault detection sensitivity and security of the relay's operation-restraint characteristic during the internal and external faults, respectively, and they do not change the HB performance results presented in this dissertation. In this chapter, I_{rt} of the relay's operation-restraint characteristic (Figure 2.2) is calculated using (2.2). In addition, only the second harmonic blocking is enabled since the second harmonic components are more significant in the presence of GIC, and thereby, the results are not considerably affected if the fifth harmonic blocking is also included in the relay's operation logic (Figure 2.3). It is worth mentioning that the fifth harmonic blocking is employed to prevent differential relay maloperation during the transformer overexcitation [40].

TABLE 3.1. THE DIFFERENTIAL RELAY SETTINGS

I_{pkp}	0.2 (pu)
I_{bkp}	2 (pu)
s_1	50 (%)
s_2	75 (%)
t_{pkp}	0.02 (s)

In the studies of this chapter, the differential relay's zero-sequence removal function [67, 77] is disabled since the transformer winding connection is the grounded wye on both sides. The zero-sequence removal is employed to remove the zero-sequence components of i_1 and/or i_2 in order to avoid malfunctions during the external phase to ground faults. Such malfunctions can occur if the zero-sequence function is disabled and one side of the transformer has a delta connection (with no zero-sequence current), while the other side is a grounded wye allowing the zero-sequence current to flow [77].

3.1.2 GIC Modeling

As observed in Figure 3.1, a DC voltage source is applied at the neutral of the transformer (on the HV side) in order to model the GIC. It should be noted that the GIC is, in fact, a slowly varying current; however, compared to the fundamental frequency and transients in the power system, its variation frequency is so low (0.1 mHz to 0.1 Hz) that it can be considered as a pure DC current. In this chapter, the magnitude of the DC voltage source is adjusted such that the GIC of 200 A flows from the transformer neutral to the ground. The value 200 A is a reference GIC magnitude employed in the experimental and simulation studies [13, 16, 78, 79]. In [79], the GIC magnitude of 200 A is considered as the peak observed GIC magnitude at the transformer's neutral.

3.1.3 Three-Leg Transformer Model

For the study of the GIC-related phenomena in transformers, the employed transformer model is of great significance. The transformer model should be able to precisely represent the magnetic circuit of the transformer and coupling among the phases. Furthermore, it should be accurate enough to represent the saturation and off-core fluxes in the transformer during the core DC bias due to GIC. This transformer model, based on the three-leg model discussed in [16, 59, 60], is mainly employed in the studies of this research.

A widely used construction of the three-phase transformers is the three-leg core depicted in Figure 3.2, where the outermost (black) and innermost (white) windings denote the HV- and LV-side windings, respectively. The key point of the transformer behavior under the GIC conditions is that the three-phase zero-sequence quasi-DC fluxes produced by GIC, denoted by Φ_{0A}, Φ_{0B}, and Φ_{0C} in Figure 3.2, close their paths through the air and link with the transformer tank. Therefore, the transformer model should include a precise off-core flux representation.

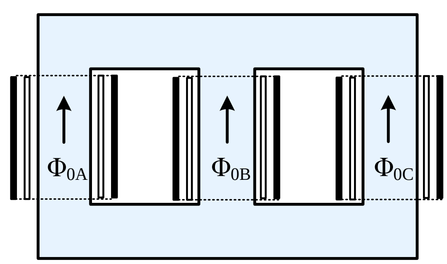

Figure 3.2. The core construction of the three-leg transformer with zero-sequence fluxes due to GIC.

Based on the principle of duality, the equivalent circuit of the transformer can be derived, as shown in Figure 3.3 [59]. In this figure, the saturable inductances L_{mA}, L_{mB}, and L_{mC} represent the three-phase main legs. The top and bottom parts of the yokes between the two adjacent legs (Figure 3.2) are represented by L_{yoke}. The tank and airgap effects are modeled by zero-sequence equivalent circuits, as specified by EC_{0A}, EC_{0B}, and EC_{0C}. These effects and the corresponding model are further described in this subsection. In order to interface the equivalent magnetic circuit of the transformer with the windings and the power grid, ideal transformers are utilized, as shown in Figure 3.3. In this figure, V_{HV} and V_{LV} denote the terminal voltages of the HV- and LV-side windings, and n_{HV} and n_{LV} are the HV- and LV-side turns ratios, respectively. The parameters, L_{12} and L_{CW}, are the short-circuit inductance and the air-path inductance between each main leg and the associated LV-side winding, respectively [60].

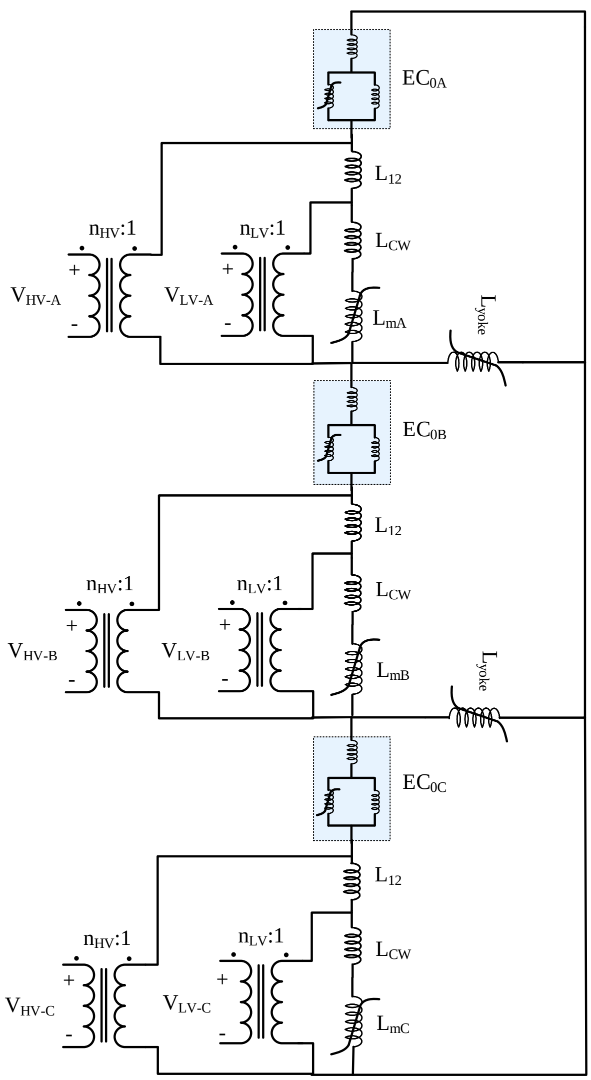

Figure 3.3. Duality-based equivalent circuit of the transformer with the three-leg core.

When GMD happens, the quasi-DC voltages induced on the three-phase conductors of the transmission lines are identical. As a result, the GIC magnitudes in all phases are the same, and they appear as slowly varying zero-sequence currents in the transformer windings. These currents generate zero-sequence magnetomotive force (MMF) and fluxes in the core. Each zero-sequence flux shown in Figure 3.2 exits the core and closes its path through the surrounding air path and the transformer tank, as illustrated in Figure 3.4. In Figure 3.4, $\mathscr{R}_{gap}$, $\mathscr{R}_{tank}$, and $\mathscr{R}_{0\text{-}air}$ are, respectively, the reluctances of the airgap between the core and the tank, the transformer tank, and the winding's surrounding air. The flux Φ_m is the main leg magnetizing flux.

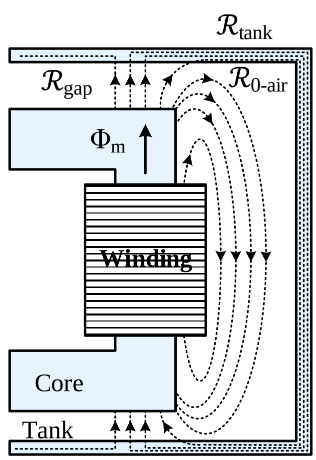

Figure 3.4. Off-core paths for zero-sequence flux.

Figure 3.5(a) shows the equivalent magnetic circuit of the off-core flux paths illustrated in Figure 3.4. Using the principle of duality, the equivalent electric circuit of this magnetic circuit is obtained and shown in Figure 3.5(b), which is represented by EC_{0A}, EC_{0B}, and EC_{0C} in Figure 3.3. In Figure 3.5(b), L_{gap}, L_{tank}, and $L_{0\text{-}air}$ are the inductances corresponding to $\mathscr{R}_{gap}$, $\mathscr{R}_{tank}$, and $\mathscr{R}_{0\text{-}air}$, respectively.

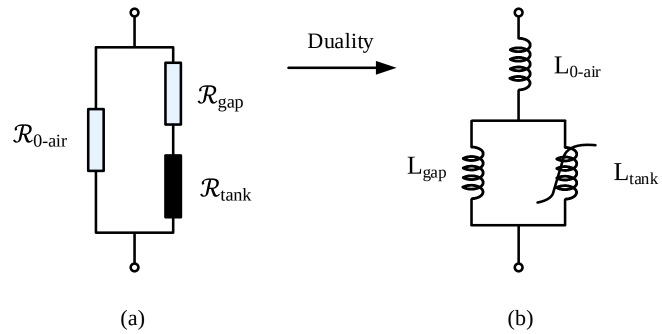

Figure 3.5. Equivalent circuits for the off-core fluxes in transformers: (a) equivalent magnetic circuit and (b) equivalent electric circuit.

The DC magnetization characteristics of the electric circuit of Figure 3.5(b) are shown in Figure 3.6. In this figure, $L_{0\text{-Avr}}$, is the final form of the transformer zero-sequence characteristic which results from the characteristics of inductances L_{gap}, L_{tank}, and $L_{0\text{-air}}$. Although all these three parameters are important, L_{gap} is the most crucial one in the GIC studies, which is introduced and calculated for the first time in [59, 60] and typically ranges from 0.9 pu to a large value of 20 pu (for example) [60]. In this research, L_{gap}, $L_{0\text{-air}}$, and L_{CW} (Figure 3.3) are assumed to be 10 pu, 1 pu, and 0.1 pu, respectively. The transformer's short-circuit impedance (Z_{SC}) is 13%. Moreover, the transformer saturation data are represented in Table 3.2.

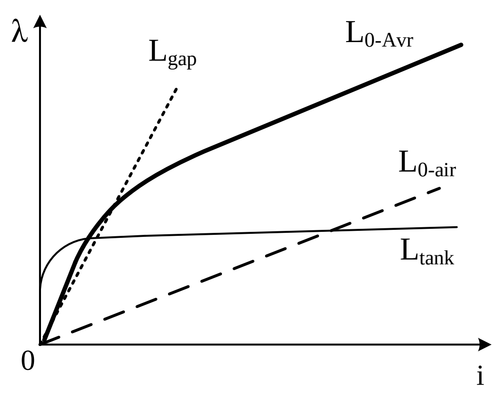

Figure 3.6. Magnetization characteristics of the off-core flux circuit of Figure 3.5(b).

TABLE 3.2. TRANSFORMER SATURATION DATA

Current (A)	0	0.71	1.84	6.12	13.27	35.93
Flux (Wb)	0	1018.9	1132	1245.3	1301.9	1358.6

3.2 Performance Analysis

The performance of the differential relay is analyzed for the occurrence of various types of internal short-circuit faults while there is the GIC in the power system. Furthermore, the effects of factors, such as fault resistance, thr_{2nd}, and the transformer loading, on the relay performance during the GMD are studied. In this section, it is assumed that the relay is equipped with the CBM since this method is commonly employed in differential protection, as discussed in Subsection 2.3.1.

3.2.1 Relay Performance without and with GIC

The differential relay performance is studied for the internal single-, two-, and three-phase to ground faults occurring on the transformer's HV and LV sides without and with the GIC. In the simulations, the permanent faults with 0 Ω/phase resistance (bolted faults) happen at 10 s. The GIC is applied at 0.1 s, and it takes around 9.9 s to reach the final steady-state magnitude of 200 A. The load consumes the nominal power of 62.5 MVA at 0.9 lagging power factor, which is 50% of the nominal power of the transformer. In this subsection, thr_{2nd} is set at a typical value of 20% [37, 38, 41, 80].

The results of the investigation are summarized in Table 3.3. In this table, the word "YES" means that the relay is able to trip for the internal fault, while "NO" means the relay failure to issue the trip signal. According to the table, the relay cannot operate for the single-phase faults occurring on the transformer's HV and LV sides during the GMD. Nonetheless, the fault is detected, and the trip signal is sent to the CBs (Figure 3.1) in the cases of the two- and three-phase faults, no matter if the GIC exists or not.

TABLE 3.3. OPERATION OF THE DIFFERENTIAL RELAY FOR THE BOLTED FAULTS, WITHOUT AND WITH THE GIC

Fault Type/Location	Without GIC	With GIC
Single-Phase/HV Side	YES	NO
Single-Phase/LV Side	YES	NO
Two-Phase/HV Side	YES	YES
Two-Phase/LV Side	YES	YES
Three-Phase/HV Side	YES	YES
Three-Phase/LV Side	YES	YES

For further analysis, the three-phase differential current waveforms (i_{Diff}) and the signals of the differential relay before and after the single-phase fault occurrence on the transformer's LV side (on phase A) in the absence of GIC are shown in Figures 3.7 and 3.8, respectively. Additionally, Figure 3.9 depicts I_{op} and RES of three phases in this condition. In these figures, the currents are in per unit of the CTs' rated secondary currents, i.e., 5 A. According to Figure 3.9, once the fault occurs at 10 s, I_{op} becomes larger than RES for phase A, resulting in issuing the PKP for this phase after passing the 0.02 s time delay, as illustrated in Figure 3.8. Since S_{HB2} is 0 for all three phases around 10.02 s when there is a PKP, the transformer is tripped, as expected.

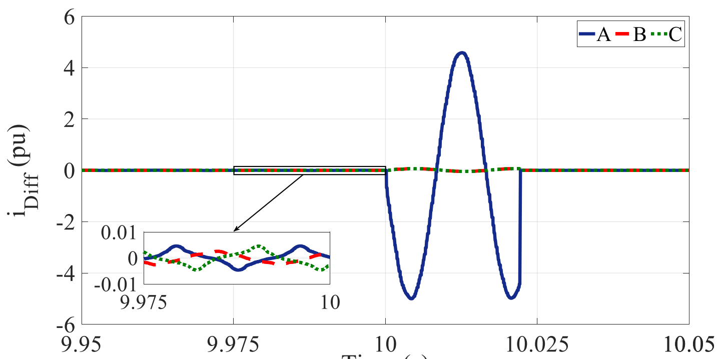

Figure 3.7. Three-phase differential current waveforms for phase A to ground fault (at 10 s) on the LV side in the absence of GIC.

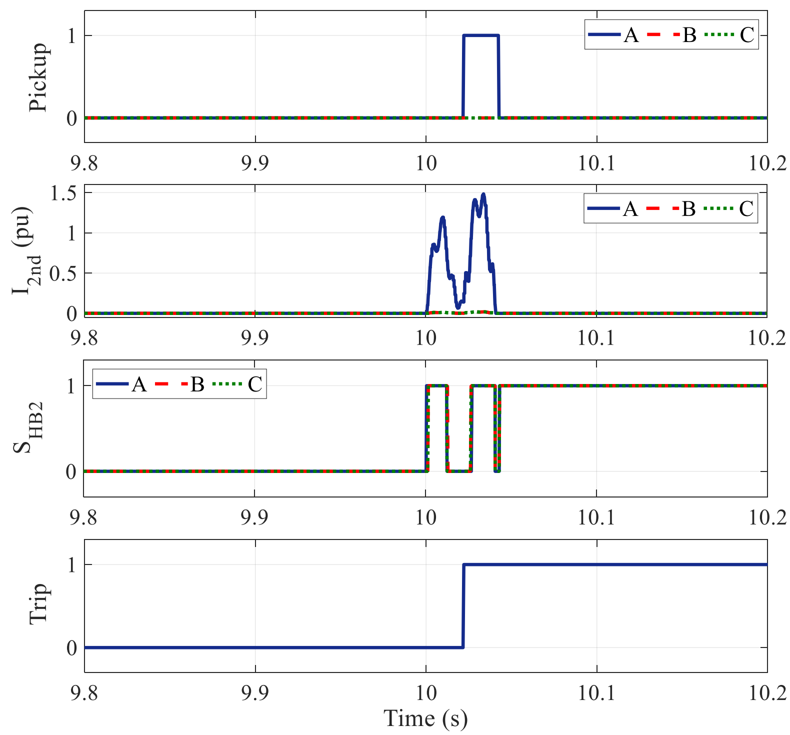

Figure 3.8. The differential relay signals for phase A to ground fault (at 10 s) on the LV side in the absence of GIC.

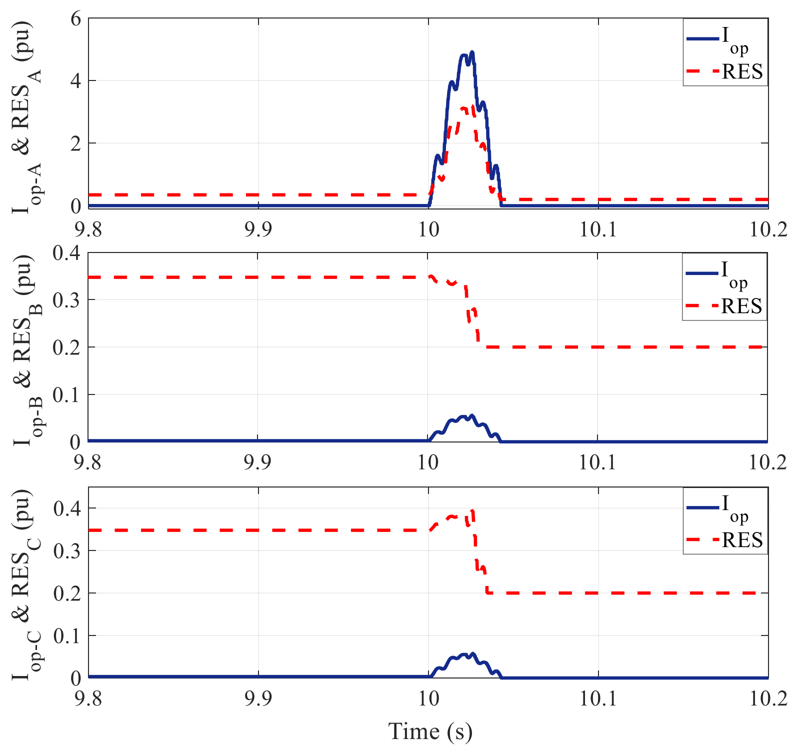

Figure 3.9. I_{op} and RES of three phases for phase A to ground fault (at 10 s) on the LV side in the absence of GIC.

Figure 3.10 shows the three-phase i_{Diff} before and after the fault in the presence of GIC. The relay signals and three-phase I_{op} and RES in this scenario are respectively depicted in Figures 3.11 and 3.12. Considering Figure 3.11, no trip signal is issued during the fault under the GIC condition. This is due to the fact that S_{HB2}, associated with phases B and C, remain 1 after the fault occurrence, and hence, $S_{HB2-ABC}$ remains asserted. This prevents the relay from the operation while there is a PKP since I_{op} of phase A becomes larger than the corresponding RES (Figure 3.12). In Figure 3.11, also observe that S_{HB2} is equal to 1 for all three phases before the fault occurrence owing to the GIC existence; however, S_{HB2} of the faulted phase changes to 0 during the fault, in spite of an overall increase in I_{2nd} of phase A. This is because the increase is less than the one in $I_{op}$of phase A, which makes the value of I_{2nd}/I_{op} smaller than the considered threshold of 20%. It should be mentioned that the spurious transient in I_{2nd} of phase A right after the fault inception is generated by the second harmonic filter that is excited by the sudden change of the differential current due to the fault occurrence. This transient period usually lasts for one cycle, which is equal to the data window of the filter [47].

The studies conducted above reveal that the transformer differential protection, equipped with the commonly used CBM, is vulnerable to the effects caused by a GMD and fails to trip for the

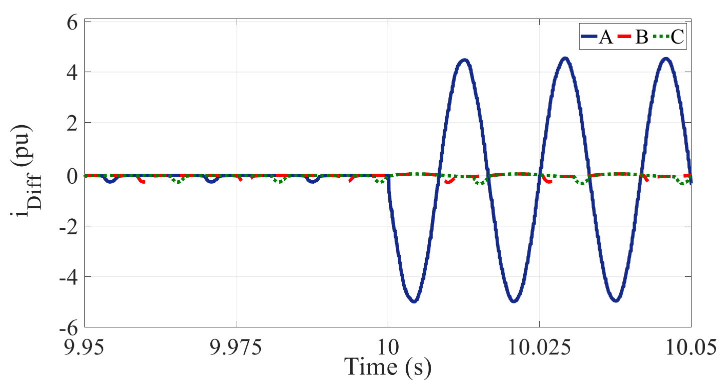

Figure 3.10. Three-phase differential current waveforms for phase A to ground fault (at 10 s) on the LV side in the presence of GIC.

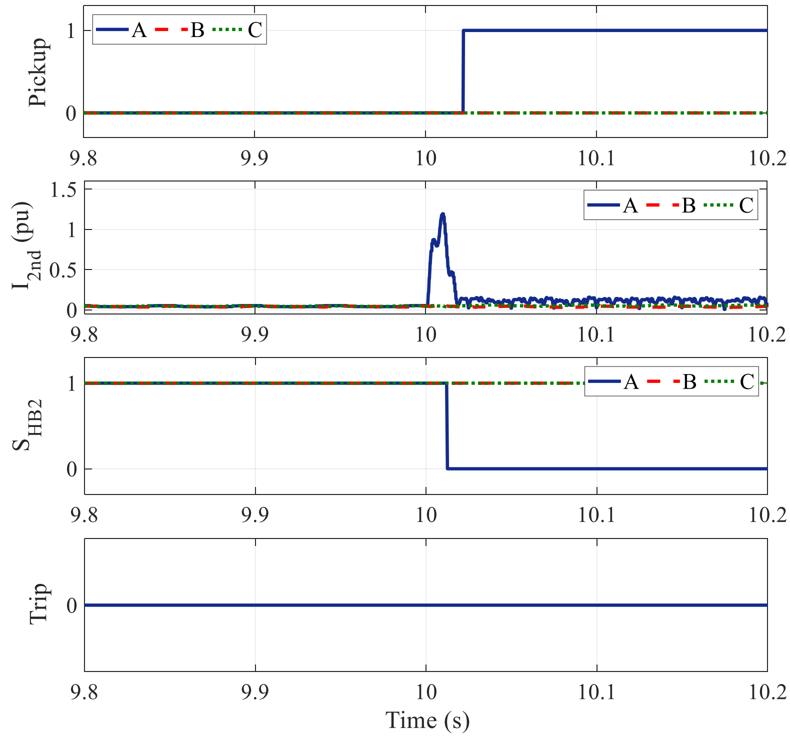

Figure 3.11. The differential relay signals for phase A to ground fault (at 10 s) on the LV side in the presence of GIC.

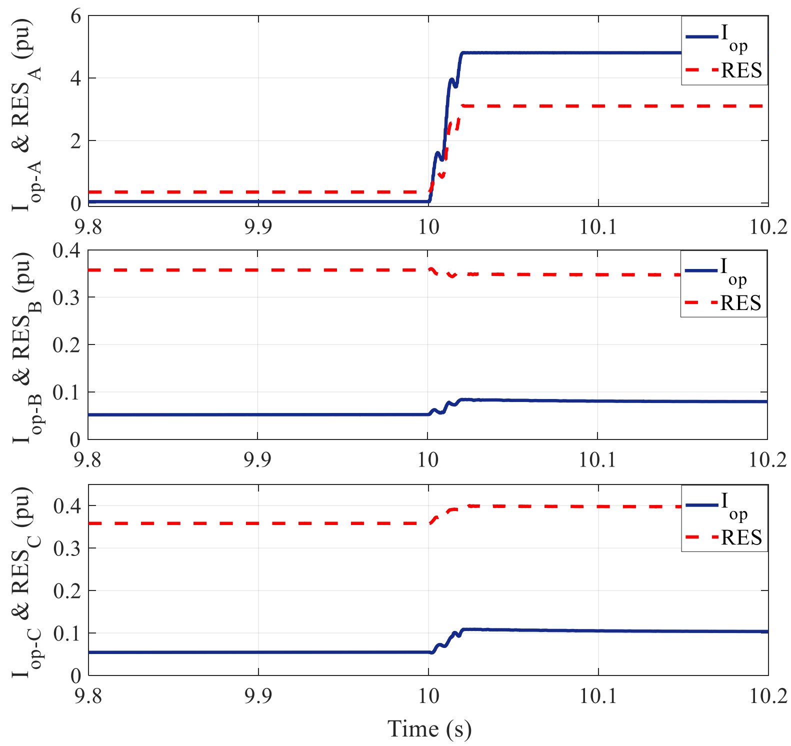

Figure 3.12. I_{op} and RES of three phases for phase A to ground fault (at 10 s) on the LV side in the presence of GIC.

internal single-phase faults in such a condition; nevertheless, the transformer is tripped for these faults when there is no GIC (as expected). It should be noted that some differential relays ignore S_{HB} signals (Figure 2.3) and directly issue the trip signal if I_{op} is larger than an unrestrained current (I_{unrt}) setting with a typical value of 8 pu [58, 66]. However, for example, considering Figure 3.12 in which I_{op} of the faulted phase is smaller than 8 pu, it can be said that such relays still fail to trip for the faults with the I_{op} magnitudes lower than I_{unrt} under the GIC conditions.

3.2.2 Sensitivity Analysis during GIC

In order to study the effects of fault resistance (R_F), thr_{2nd}, and transformer loading on the differential relay performance, the following scenarios are considered. In these scenarios, an internal two-phase to ground fault occurs on the LV side at 10 s under the GIC condition.

- *Scenario I* (the R_F effect): The fault resistance is increased to a value for which the relay stops operating.
- *Scenario II* (the thr_{2nd} effect): The threshold thr_{2nd} is decreased from 20% to 15% [36, 37, 41, 54, 80] while R_F is 0.7 Ω.
- *Scenario III* (the loading effect): The fault with R_F of 0.7 Ω occurs during the nominal load (i.e., 62.5 MVA) and no-load conditions. Similar to *Scenario I*, the value of thr_{2nd} is 20%.

The results of this study are summarized in Table 3.4. Based on this table, in *Scenario I*, for an R_F of 0.9 Ω, the differential relay is not able to operate for the two-phase fault under the GIC condition; however, the fault is interrupted when the resistance is 0 Ω (Tables 3.3 and 3.4). Considering *Scenario II*, the relay with thr_{2nd} of 15% cannot send the trip signal to the CBs for the fault during the GMD. However, for the same fault and thr_{2nd} of 20%, the relay is capable of tripping for the fault. This is because of the fact that by decreasing thr_{2nd}, the relay sensitivity to the second harmonic level in the differential current increases, which causes the relay operation to be more affected by the GIC-caused second harmonics. In *Scenario III*, unlike the nominal load condition, the relay is incapable of operating for the fault in the no-load condition and the presence of GIC, indicating that the relay failure in operation is more likely when the load decreases in this case study. It should be mentioned that in *Scenarios II* and *III*, the fault resistance (i.e., 0.7 Ω) is selected such that the relay fails to operate for the fault by the decrease in thr_{2nd} and the transformer loading, respectively. Moreover, the relay successfully operates in *Scenarios I* to *III* in the absence of GIC.

TABLE 3.4. OPERATION OF THE DIFFERENTIAL RELAY IN *SCENARIOS I* TO *III* DURING THE GIC

I	R_F = 0 Ω	R_F = 0.9 Ω
	YES	NO
II	thr_{2nd} = 20%	thr_{2nd} = 15%
	YES	NO
III	Nominal Load	No-Load
	YES	NO

3.3 Comparison of HB Methods

In Section 3.2, the performance of the differential relay equipped with the CBM is analyzed in detail for different types of internal faults occurring in the presence of GIC. It is concluded that the relay has difficulty operating for the faults when there is a GIC flow in the transformer. In this section, the performance of transformer differential relays, which employ the CBM, ABM, PBM, and SBM, is studied for the single-phase faults under the GIC condition. This fault type is the most common one occurring in power systems, and the differential protection is more likely to fail to operate for such faults during the GMDs due to the harmonic blocking, as shown in Section 3.2.

The studies are carried out for both bolted and unbolted faults in nominal and no-load conditions. Furthermore, it is assumed that thr_{2nd} is 15% in this section.

3.3.1 Bolted Faults

The behavior of the differential relays, utilizing CBM, ABM, PBM, and SBM, is investigated for phase A to ground faults with zero impedances in the presence of GIC. The faults happen on both the HV and LV sides of the transformer at 10 s when the GIC value is around 200 A. The results are presented in Table 3.5. According to this table, the common HB methods CBM and ABM prevent the differential protection from the operation for the faults on both sides of the transformer under the GIC condition; therefore, the faults remain uninterrupted. Nonetheless, the differential relays using the independent HB methods, i.e., the PBM and SBM, have no difficulty operating for the bolted faults during the GMD. It is worth mentioning that for the unloaded transformer/no-load condition, the results are similar to the ones given in Table 3.5.

TABLE 3.5. OPERATION OF THE DIFFERENTIAL RELAYS FOR THE BOLTED FAULTS DURING THE GIC

HB Method	Fault Location	Trip
CBM	HV Side	NO
	LV Side	NO
ABM	HV Side	NO
	LV Side	NO
PBM	HV Side	YES
	LV Side	YES
SBM	HV Side	YES
	LV Side	YES

Figure 3.13 shows the differential relay signals before and after the fault occurrence on the LV side when the ABM is used. It should be noted that the performance of the relay, equipped with the CBM, in the same condition is already discussed in Section 3.2 (Figure 3.11). As seen in Figure 3.13, despite the fact that *Average Ratio* decreases to around 0.35 (or 35%) after the fault occurrence, $S_{HB2-ABC}$ remains equal to 1 as the ratio is still higher than thr_{2nd}. Consequently, the

relay is kept blocked, although there is a *PKP* for phase A at 10.022 s. Hence, similar to the CBM-based relay, the one employing the ABM is also unable to send the trip signal to the CBs during the GMD.

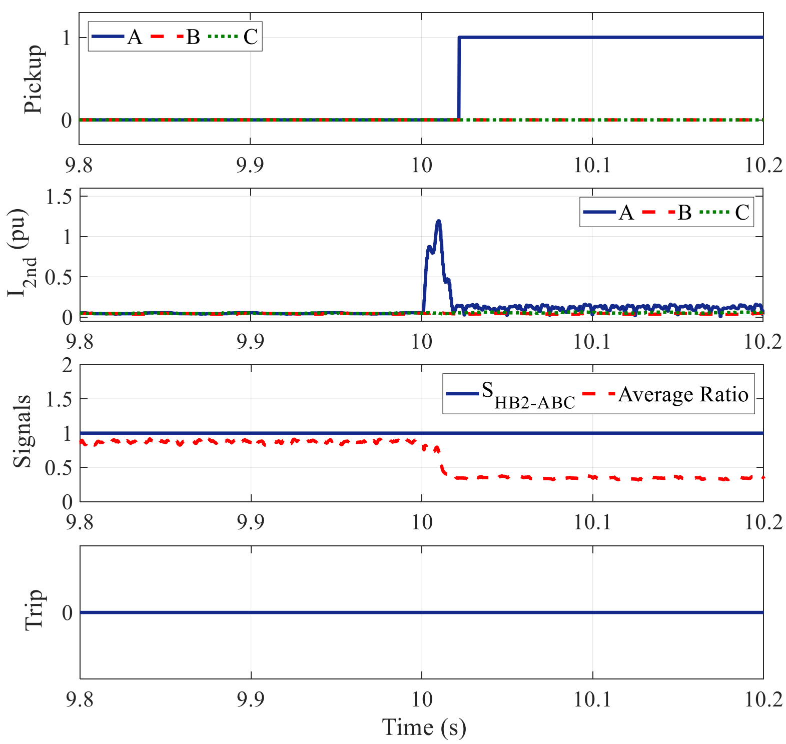

Figure 3.13. The signals of the differential relay employing the ABM for the bolted phase A to ground fault (at 10 s) on the LV side in the presence of GIC.

Figures 3.14 and 3.15 depict the signals of the differential relay equipped with the PBM and SBM, respectively. In Figure 3.14, it can be seen that the trip signal is issued at the same time as there is a *PKP*, even though phases B and C are still blocked. This is because, unlike the CBM, the PBM allows the relay to issue the trip signal if only S_{HB2} of the faulted phase changes from 1 to 0. Here, S_{HB2} of phase A is set to 0 at 10.013 s as I_{2nd} related to this phase decreases after a temporary increase due to the fault occurrence; thereby, the relay is unblocked and can operate for the fault once the *PKP* is issued.

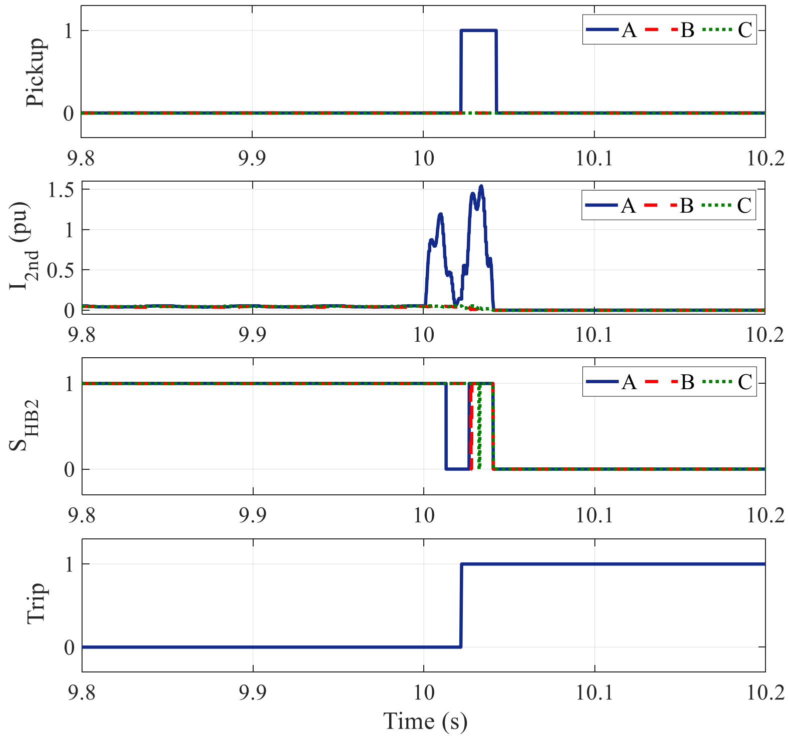

Figure 3.14. The signals of the differential relay employing the PBM for the bolted phase A to ground fault (at 10 s) on the LV side in the presence of GIC.

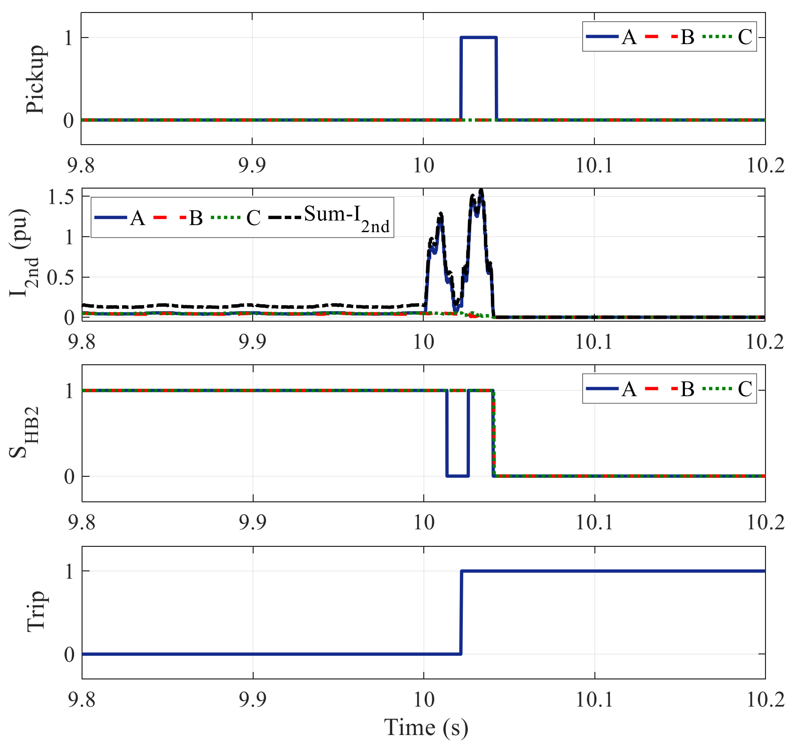

Figure 3.15. The signals of the differential relay employing the SBM for the bolted phase A to ground fault (at 10 s) on the LV side in the presence of GIC.

As shown in Figure 3.15, similar to the differential relay employing the PBM, the one with the SBM can successfully operate for the bolted fault when there is the GIC. The relay is unblocked, 0.014 s after the fault happens as the ratio of *Sum*-I_{2nd} to I_{op} related to the faulted phase decreases to a value smaller than 15%, causing S_{HB2} of phase A to change to 0. Subsequently, the transformer is tripped once the *PKP* is issued at 10.022 s.

Based on the studies carried out in this subsection, it can be concluded that the differential relays equipped with the independent HB methods are less likely to fail to operate for the bolted faults in the presence of GIC, compared to the common HB methods.

3.3.2 Unbolted Faults

In Subsection 3.3.1, it is shown that the differential protection employing the CBM and ABM cannot operate for the faults with zero impedances under the GIC condition. Therefore, the performance of the relays equipped with these methods is not analyzed in this subsection since their failure to trip for the unbolted faults is evident under the GIC condition. This subsection investigates the behavior of the differential relays equipped with the PBM and SBM for phase A to ground faults with non-zero impedances during the GIC. The fault resistance on the HV or LV side of the transformer is increased until the relay fails to operate, although there is a *PKP* for the fault. These investigations are performed for the unloaded transformer and when the transformer supplies the 62.5 MVA load (Figure 3.1). The results are provided in Table 3.6.

According to Table 3.6, when the load is connected, the relay utilizing the PBM is able to trip for the HV- and LV-side faults with the resistance values equal to 2175 Ω and 110 Ω, which lead to I_{op} of 0.663 pu and 0.659 pu for the faulted phase, respectively. It should be mentioned that for larger R_F values, there is no *PKP* signal issued by the relay under the GIC condition. On the contrary, if the SBM is used for the HB purpose, the differential protection cannot trip for the faults

TABLE 3.6. OPERATION OF THE DIFFERENTIAL RELAYS FOR THE UNBOLTED FAULTS DURING THE GIC

Transformer Loading	HB Method	Fault Location	Trip
Loaded	PBM	HV Side	YES
		LV Side	YES
	SBM	HV Side	NO
		LV Side	NO
Unloaded	PBM	HV Side	NO
		LV Side	NO
	SBM	HV Side	NO
		LV Side	NO

with the resistances equal to or higher than 1930 Ω (I_{op} = 0.747 pu) and 105 Ω (I_{op} = 0.689 pu), which occur on the transformer's HV and LV sides, respectively. Figure 3.16 illustrates the signals of the relay employing the SBM for the fault with R_F of 105 Ω when the load is connected to the system. In this figure, observe that the *PKP* signal is issued at 10.041 s; however, there is no trip signal issued. Because of the GIC, S_{HB2} related to each phase is equal to 1 before and after the fault occurrence, which blocks the relay.

Regarding the results of the no-load conditions in Table 3.6, the differential protection equipped with either the PBM or SBM is not able to operate for the unbolted faults in the presence of GIC. The relay utilizing the PBM cannot trip for the HV- and LV-side faults with the resistance values equal to or higher than 4910 Ω (I_{op} = 0.303 pu) and 270 Ω (I_{op} = 0.289 pu), respectively. The relay signals for the fault with R_F of 270 Ω are shown in Figure 3.17. Despite the fact that a *PKP* is released at 10.034 s, the trip signal remains equal to 0 after the fault occurrence at 10 s. This is because S_{HB2} of each phase is kept unchanged and equal to 1 owing to the GIC; hence, the relay is blocked during the fault. Considering the SBM, for the faults on the HV and LV sides of the unloaded transformer, having the resistances equal to or higher than 1550 Ω (I_{op} = 0.935 pu) and 85 Ω (I_{op} = 0.880 pu), respectively, the trip signal is not issued.

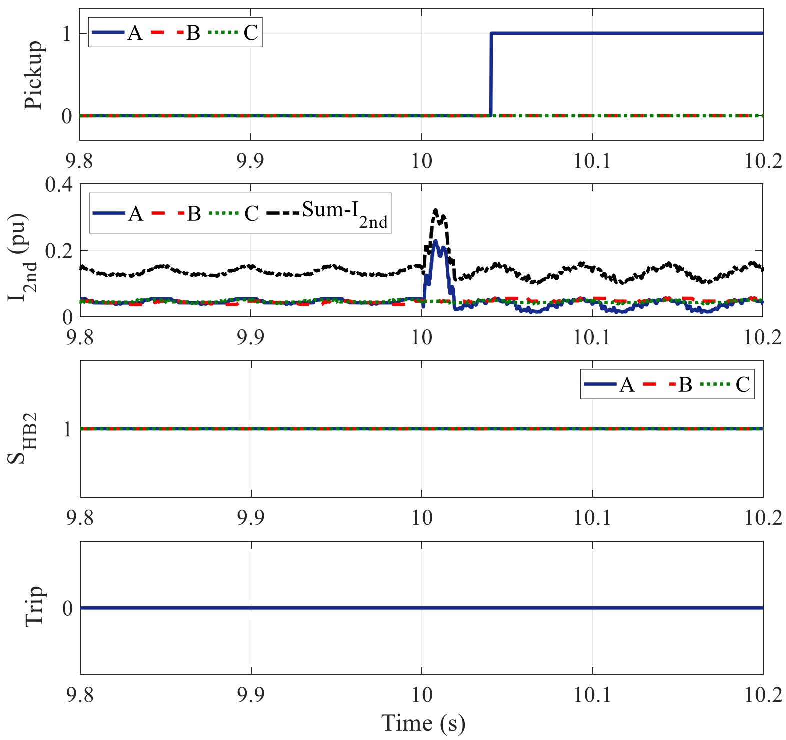

Figure 3.16. The signals of the differential relay employing the SBM for the unbolted phase A to ground fault (at 10 s) on the LV side when it is loaded in the presence of GIC.

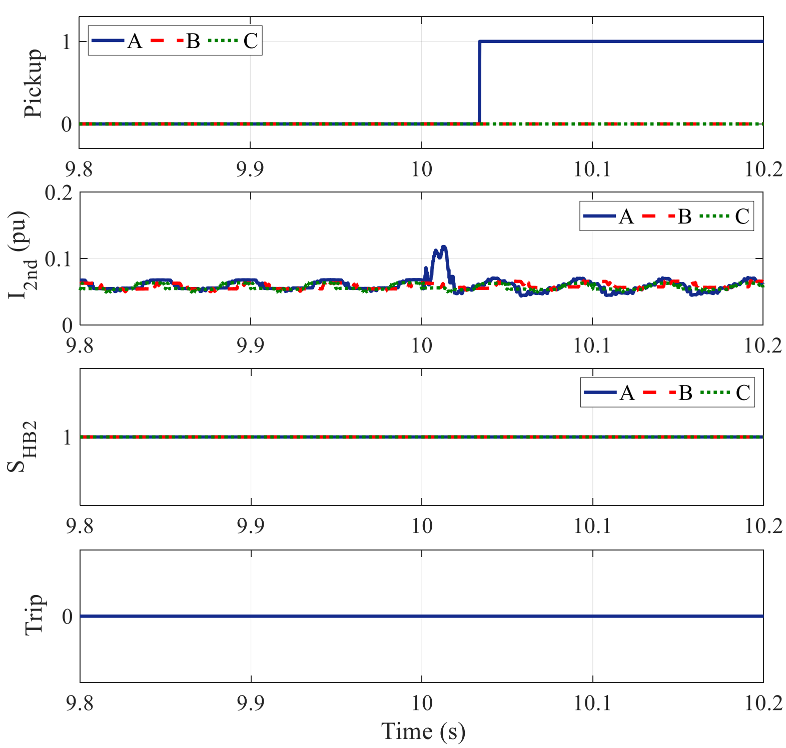

Figure 3.17. The signals of the differential relay employing the PBM for the unbolted phase A to ground fault (at 10 s) on the LV side when it is unloaded in the presence of GIC.

Studies related to the unbolted faults show that the differential protection employing the PBM is more dependable than the one equipped with the SBM during the GIC. However, there are scenarios in which both of these methods cause the relays to fail to trip for the faults in the presence of GIC. It should be noted that, as discussed in Section 2.3, the PBM provides a differential relay with low security for the inrush currents, and therefore, the relay malfunction is likely if this HB method is employed. It is worth mentioning that if there is no GIC, the differential relay operates for the faults in all scenarios investigated in this section, regardless of the type of HB scheme.

3.4 Summary

In this chapter, the performance of HB-based differential relays was studied for different fault types and resistances, HB methods and thresholds, and transformer loading levels. The studies of this chapter showed that regardless of the employed HB method, there are scenarios in which the differential relays fail to operate for the internal faults due to the GIC-related harmonic blocking. Although it was shown that the relays with the independent HB methods are more dependable than the relays employing the common HB methods, the former still lost dependability as the fault resistances exceeded certain levels in the presence of GIC. The HV-side fault resistances in the range of kΩ, for which the PBM- and SBM-based relays failed to trip, may seem less likely to occur in power systems. Nonetheless, such faults lead to the I_{op} values in the approximate ranges of those associated with the LV-side faults in the study system, as analyzed in this chapter, as well as transformer turn faults which are studied in detail in Chapter 7 of this dissertation. A harmonic-based unblocking scheme is introduced in Chapter 4 for the dependability improvement of the relays during the GMDs.

Chapter 4
Harmonic-Based Unblocking Scheme

4.1 Introduction

In Chapter 3, it is revealed that the differential relays employing the common and independent HB methods are incapable of tripping for some in-zone faults under the GIC conditions due to the unwanted harmonic blocking. In order to enhance the differential protection dependability for the internal faults during the GMDs regardless of the type of the HB method, an unblocking scheme is proposed in this chapter. The proposed scheme relies on a harmonic-based GIC detection algorithm and a fault detection logic to unblock the relay solely for the internal faults during the GIC. Available GIC/DC bias monitoring and detection methods are reviewed in the subsection below.

4.1.1 A Review of GIC Monitoring and Detection Approaches

In order to detect the GIC, the general practice is to employ the associated monitoring systems [4, 24, 81-86], in which sensors are installed at the transformers' neutrals or terminals, and the acquired signals are processed for the GIC detection. The GIC monitoring can be done by measuring both phase and neutral currents of the transformers [1, 81]. The authors in [84] utilize a Hall Effect coupler installed at the transformer neutral for the GIC measurements. According to the studies of [84], more gas activities in the transformer's tank, the transformer voltage reduction, and an increase in its reactive power consumption indicate the existence of GIC. In [83, 86], the GIC is estimated and detected based on the monitored transformer reactive power consumption during a GMD. However, in addition to the unavailability risks, the monitoring systems lead to capital, operational, and maintenance costs. Therefore, it is preferable to devise a method that recognizes the GIC based on the available signals of the existing installed equipment, avoiding the extra costs and enhancing the monitoring reliability.

The neutral currents and particularly their DC components correlate with the reactive power losses of the transformers during the GMDs. The current harmonics, which are generated due to the part-cycle core saturation of the transformer, may also represent a GIC condition. Thereby, the harmonics and transformers' reactive power losses are suggested as the GIC indicators in [6]. The authors in [87] propose a method to estimate the GIC or DC current at the transformer's neutral using the harmonic components of the differential currents employed in the transformer differential protection. As transformer energization also leads to the core saturation, and therefore, the differential current harmonics, the proposed scheme of [87] is prone to failure in discrimination between the inrush currents and the GIC conditions.

By measuring the transformer voltage and differential current, the technique proposed in [88] utilizes an extended Kalman filter (EKF) to estimate the GIC flow in transformers during the GMDs. Nevertheless, the accurate parameters of the transformer model are needed to initiate the estimation process using the proposed technique of [88]. Furthermore, the EKF-based estimation methods do not provide a precise estimation unless their covariance matrices are finely tuned, making the implementation of such methods challenging. A machine learning-based scheme for GIC detection in power systems using the currents provided by the CTs is introduced in [89]. Besides the complexity, such schemes require massive data sets for the training process. Moreover, the performance of the method proposed in [89] is not investigated in the transformer energization cases to show its ability to discriminate the GIC conditions from the inrush currents. Additionally, none of the aforementioned references discusses the utilization of the GIC monitoring and detection methods to improve the differential relay performance under the GIC conditions.

4.2 Harmonic-Based Approach

Figure 4.1 shows the proposed approach for transformer differential protection and how it is integrated with the HB module of the differential relay. The goal is to unblock existing differential relays for the internal faults under the GIC conditions. Considering Figure 4.1, the proposed method is comprised of two main modules, i.e., harmonic-based GIC detection and supplementary modules. By overriding S_{HB} signals during an internal fault and a GIC condition, the differential relay becomes able to issue the trip signal if there is a *PKP*. Overriding S_{HB} means that the modified harmonic blocking (MHB) signal (S_{MHB}) of each phase is set to 0, as the former is equal to 1 during a GMD. It is worth mentioning that S_{HB-A}, S_{HB-B}, and S_{HB-C} in Figure 4.1 are similar, provided that a common HB method is employed, and they are different if an independent HB method is utilized.

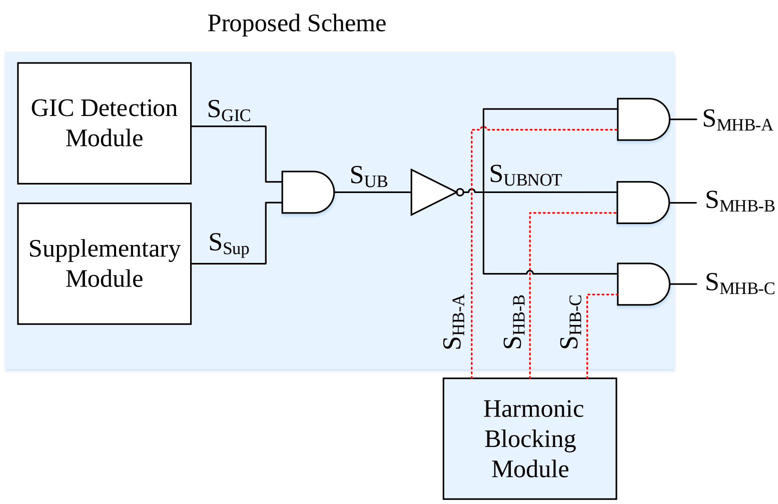

Figure 4.1. The proposed scheme for the transformer differential protection under the GIC conditions.

When a GIC condition is detected, the GIC signal (S_{GIC}) in Figure 4.1 is set to 1, unblocking the differential protection (i.e., S_{HB} is overridden) if there is no supplementary module. This module, however, is needed so that the differential relay is unblocked during a GMD only if there is an internal fault occurrence. Accordingly, in the case of an internal fault, the supplementary module issues a supplementary signal (S_{Sup}) equal to 1. Therefore, S_{UB} is asserted if there is the GIC (S_{GIC} = 1), which unblocks the relay by setting S_{UBNOT} to 0 (Figure 4.1).

4.2.1 Harmonic-Based GIC Detection

Due to the part-cycle saturation of the transformer during the GIC, the odd and even harmonic currents with significant second harmonic components exist in the transformer currents [21, 39]. Hence, a GIC condition can be detected by monitoring the second harmonic components of the differential currents. In fact, the relationship between phase angles of the differential current second harmonic components ($\theta_{I_{2nd}}$) during a GMD is different from the one related to the transformer energization. Two sets of time-domain simulations are carried out on the study system of Figure 3.1 for verification. Figure 4.2(a) depicts $\theta_{I_{2nd}}$ of three phases, passed through low-pass filters (LPFs), denoted as $\theta_{I_{2ndp}}$, when the GIC is applied at 0.1 s. Figure 4.2(b) illustrates $\theta_{I_{2ndp}}$ of the three phases during the transformer energization, when the CB on the HV side of the transformer is closed at 0.1 s. Figure 4.3 compares the phasor arrangements of the second harmonic components at t = 1 s (Figure 4.2) during the GIC and transformer energization. As shown in Figure 4.3, the phasors represent a negative-sequence order (ACB) in the presence of GIC. On the contrary, in the case of energization, they are in a positive-sequence arrangement (ABC).

The aforementioned observation results from the signal processing of differential current waveforms, associated with the GIC and energization conditions, to extract the second harmonic

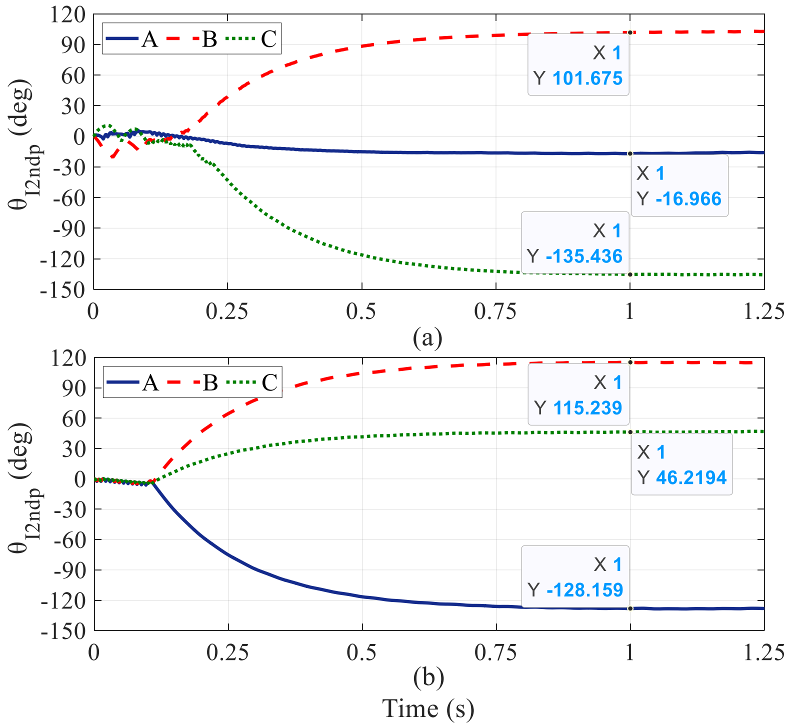

Figure 4.2. The phase angles of the differential current second harmonic components: (a) during the GIC and (b) during the transformer energization.

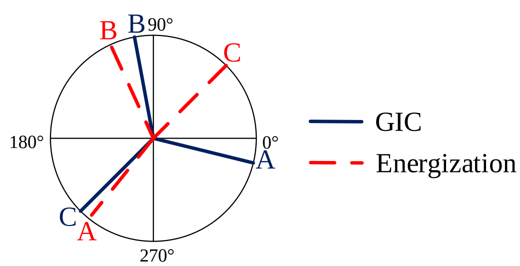

Figure 4.3. Phasor arrangements of the differential current second harmonic components during the GIC and energization, based on the phase angles of Figure 4.2 at t = 1 s.

components using the Fourier transform. Subsequently, a GIC condition can be detected and distinguished from the transformer energization by monitoring $\theta_{I_{2nd}}$ of three phases to check whether the second harmonic components are in a negative-sequence order. In this dissertation, a negative-sequence relationship between the components is detected if $\theta_{I_{2nd}}$ of three phases satisfy *Requirement I*, *II*, or *III* in (4.1). In this equation, θ_{set} is an adjustable threshold, which is considered to be 10° in this chapter. The three requirements in (4.1) include all possible arrangements of the second harmonic components representing a negative-sequence relationship.

$$\begin{cases} I: \quad \theta_{I_{2nd_B}} - \theta_{I_{2nd_A}} > \theta_{set} \ \&\& \ \theta_{I_{2nd_C}} - \theta_{I_{2nd_B}} > \theta_{set} \\ \qquad\qquad\qquad\qquad\qquad || \\ II: \quad \theta_{I_{2nd_A}} - \theta_{I_{2nd_C}} > \theta_{set} \ \&\& \ \theta_{I_{2nd_C}} - \theta_{I_{2nd_B}} > \theta_{set} \\ \qquad\qquad\qquad\qquad\qquad || \\ III: \ \theta_{I_{2nd_A}} - \theta_{I_{2nd_C}} > \theta_{set} \ \&\& \ \theta_{I_{2nd_B}} - \theta_{I_{2nd_A}} > \theta_{set} \end{cases} \tag{4.1}$$

Figure 4.4 illustrates the logic of the harmonic-based GIC detection algorithm. As shown in this figure, the inputs are $\theta_{I_{2nd}}$ and I_{2nd} related to phases A, B, and C, and the output is S_{GIC}. According to Figure 4.4, $\theta_{I_{2nd}}$ of three phases are first passed through the LPFs in order to remove the high-frequency transients. The filtered phase angles, $\theta_{I_{2ndp}}$, are then processed to check whether any of the requirements in (4.1) is met. By satisfying *Requirement I*, *II*, or *III*, S_{GIC} in Figure 4.4 becomes 1, indicating that a GIC condition is detected if at least one of the second harmonic magnitudes (i.e., I_{2nd}) is larger than a pre-specified threshold set at 0.001 pu in this study. This requirement is imposed in order to differentiate a normal condition from a GIC condition such that S_{GIC} is not asserted if I_{2nd} of the three phases are all equal to or smaller than the threshold. This is due to the fact that the second harmonic magnitudes are small when there is no GIC.

In Figure 4.4, the adjustable pickup time ($t_{\text{set-1}}$) is considered to avoid false S_{GIC} during the transients. Moreover, using an adjustable dropout time ($t_{\text{set-2}}$), the algorithm's output S_{GIC} remains asserted for specific time after none of the conditions above is met to ensure that S_{GIC} is available long enough to unblock the relay during an internal fault. This is because shortly after the fault happens in the presence of GIC, $\theta_{I_{2nd}}$ of the three phases may no longer meet the criteria in (4.1).

In this chapter, $t_{set\text{-}1}$ and $t_{set\text{-}2}$ are set at 0 and 3 cycles, respectively.

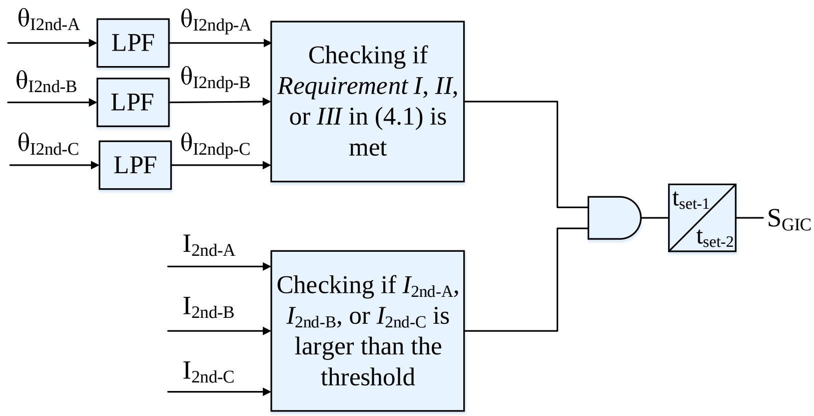

Figure 4.4. The logic of GIC detection module of Figure 4.1.

4.2.2 Supplementary Module

The logic of the supplementary module is shown in Figure 4.5, which operates based on the rate of change of current (RCC). The inputs of this module are the three-phase differential current fundamental components, i.e., I_{op}, and the output is S_{RCC} that is referred to as S_{Sup} in this chapter. As depicted in Figure 4.5, the absolute (ABS) values of the three-phase I_{op} derivatives are passed through the LPFs to remove the high-frequency transients, resulting in the three-phase *RCCs*. *RCC* of each phase is then compared with an adjustable threshold (thr_{RCC}) and S_{Sup} is asserted if one of *RCCs* exceeds the threshold, unblocking the relay provided that S_{GIC} is 1 as well (Figure 4.1). The time settings $t_{set\text{-}3}$ and $t_{set\text{-}4}$ are considered to be 0 and 3 cycles in the studies of this chapter. The dropout time ($t_{set\text{-}4}$) of 3 cycles is to coordinate with the relay's pickup, ensuring that the relay is unblocked and operates for an in-zone fault during the GIC. It should be noted that unlike I_{op}, the I_{op} derivatives in Figure 4.5 remain small in no-fault conditions during a GMD because of the GIC's slow variations. This ensures that the proposed scheme of Figure 4.1 is secure in the absence of faults under the GIC conditions.

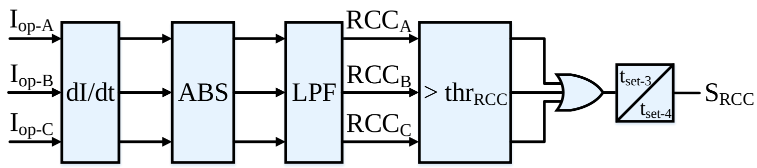

Figure 4.5. The logic of the supplementary module of Figure 4.1.

In order to prevent the supplementary module from issuing a false S_{Sup} for external faults, thr_{RCC} in Figure 4.5 should be high enough to keep this signal at 0 in such cases. On the other hand, it should be low enough to unblock the relay for even low-current internal faults during the GMDs. To achieve such a desired functionality, the bolted external faults are simulated on the HV and LV sides of the transformer in the study system, between the CTs and the corresponding CBs (Figure 3.1). The faults occur at 10 s when the GIC reaches its steady-state level of 200 A. Based on these studies, the largest *RCCs* among the three phases for the HV- and LV-side faults are 5.52 pu/s and 0.584 pu/s, respectively. Thus, thr_{RCC} should be larger than 5.52 pu/s so that there is no malfunction for both HV- and LV-side faults happening outside the zone protected by the differential relay. In this chapter, thr_{RCC} is set at 6 pu/s, with which the supplementary module can detect the internal faults on the HV and LV sides of the transformer in Figure 3.1, with the R_F values as high as around 2000 Ω and 100 Ω, respectively.

4.3 Performance Evaluation

In this section, the performance of the proposed method in Figure 4.1 is investigated in various scenarios. The HB method employed in this section is the SBM. In this chapter, both second and fifth harmonic blocking are enabled. For each phase, if S_{HB2} or S_{HB5} is set to 1, the resulting S_{HB} of that phase is asserted (Figure 2.3). The HB thresholds thr_{2nd} and thr_{5th} are set at 15% and 35% [40], respectively. The differential relay settings are the same as those presented in Table 3.1.

4.3.1 GIC without Faults

Figure 4.6 shows signals of the proposed method, S_{GIC}, S_{Sup}, and S_{UBNOT}, as well as the blocking signals, S_{HB} and S_{MHB}, during the GIC initiated at 0.1 s. Due to similar behaviors of the three-phase signals, only the blocking signals of phase A are shown in Figure 4.6. The GIC condition is detected at 0.423 s, which is when S_{GIC} settles at 1 following a few transitions between 0 and 1. On the other hand, S_{Sup} remains constant and equal to 0; hence, S_{UB} is not asserted, and S_{UBNOT} remains 1. In addition, one can see that the differential relay is blocked after 0.103 s because S_{HB} is asserted. Considering that S_{UBNOT} is 1, S_{MHB} matches S_{HB}, which means that the relay equipped with the proposed method is blocked and does not malfunction in the presence of GIC. The simulation results of this case study are the same for both loaded and unloaded transformer conditions.

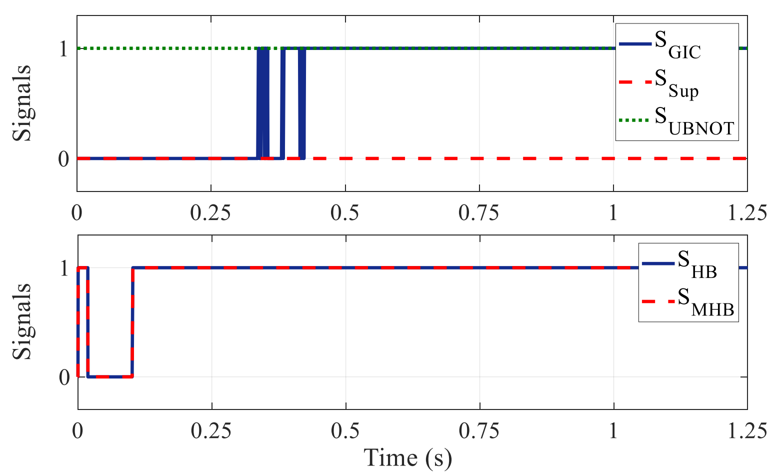

Figure 4.6. The signals of the proposed method and the harmonic blocking signals of phase A during the GIC.

4.3.2 Transformer Energization

The transformer energization is simulated by closing the HV-side CB at 0.1 s while the LV-side CB is open (Figure 3.1). The results are depicted in Figure 4.7. As depicted in this figure, S_{Sup}

changes to 1 at 0.107 s, which does not affect the output because S_{GIC} remains equal to 0, and as a result, S_{UBNOT} is kept at 1. This means that not only the proposed method is able to discriminate the GIC from the energization ($S_{GIC} = 0$) but also there is no malfunction during the energization. Figure 4.7 shows that both S_{HB} and S_{MHB} are set to 1 after the transformer is energized, which blocks the relay and prevents any maloperation.

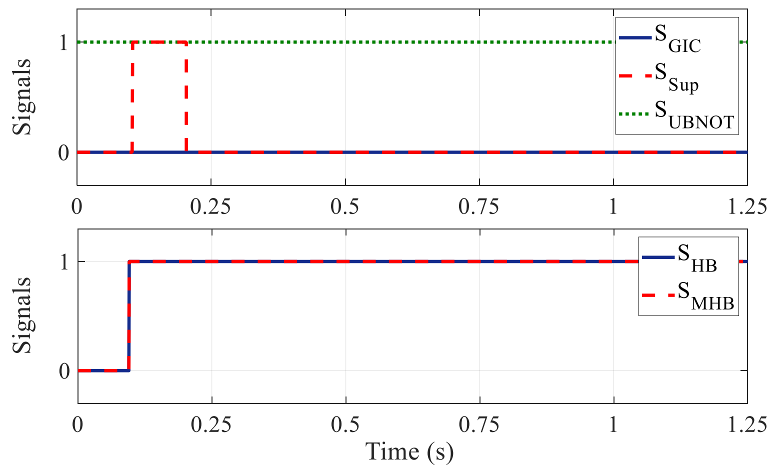

Figure 4.7. The signals of the proposed method and the harmonic blocking signals of phase A during the transformer energization.

The proposed method's performance is also simulated during the transformer energization with the CT saturation. Figure 4.8 shows the results including the phase A differential current waveform (i.e., i_{Diff}) as well as the primary ratio and secondary currents of CT1 (Figure 3.1). The primary ratio current is the CT1's primary current divided by its turns ratio, i.e., 200/5. In Figure 4.8(a), observe that when the CT saturates around 0.3 s, the low-magnitude periods (LMPs) of i_{Diff} become non-flat and depart from zero. Furthermore, as seen in Figure 4.8(b), the CT's secondary current noticeably deviates from the primary ratio current due to the CT saturation. However, based on Figure 4.8(c), the CT saturation during the transformer energization does not cause the proposed method to malfunction since S_{GIC}, and therefore, S_{UB} are not asserted, keeping S_{UBNOT} unchanged and equal to 1.

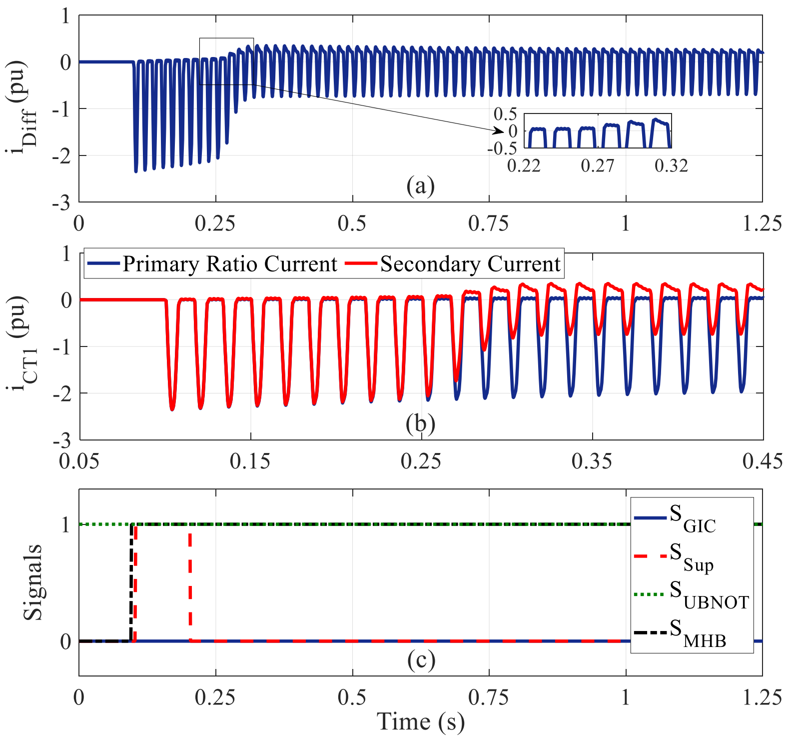

Figure 4.8. Performance of the proposed method during the transformer energization and CT saturation: (a) differential current waveform of phase A, (b) CT1 currents of phase A, and (c) the method signals

4.3.3 A Comparison with Waveform-Based Inrush Detection

Although waveform-based inrush detection methods [47, 48, 90, 91] may represent a high level of dependability for internal faults, the security of such methods needs to be verified when the CTs are saturated. The performance of the gap detection method [90, 91], as a prevalent waveform-based blocking approach, is studied in this subsection during the transformer energization and GIC with the CT saturation. This method monitors the LMPs of i_{Diff} and detects the inrush current if the waveform includes the LMPs lasting more than one-quarter of a cycle [48, 90, 91]. Similar to the HB approach, the gap detection method blocks the relay operation as an energization condition is detected. Here, an LMP is assumed when the i_{Diff} magnitude (the absolute value) is lower than 0.05 pu [90]. In the simulations, the algorithm is disabled if the i_{Diff} magnitude does not exceed the threshold of 0.05 pu for the whole cycle. Figure 4.9 illustrates the results during the transformer energization and CT saturation, as studied in Subsection 4.3.2. In this figure, t_{LMP} is the calculated time related to the LMPs of i_{Diff} in Figure 4.8, and S_{Block} is the output of the gap detection algorithm. It is observed that although the algorithm initially blocks the relay after the energization, it unblocks the relay (S_{Block} = 0) as the CT is saturated, which affects the LMPs (Figure 4.8). This can lead to maloperation since the relay asserts *PKP* (pickup) during the energization. However, the proposed scheme does not unblock the relay in such a condition, as discussed in the previous subsection.

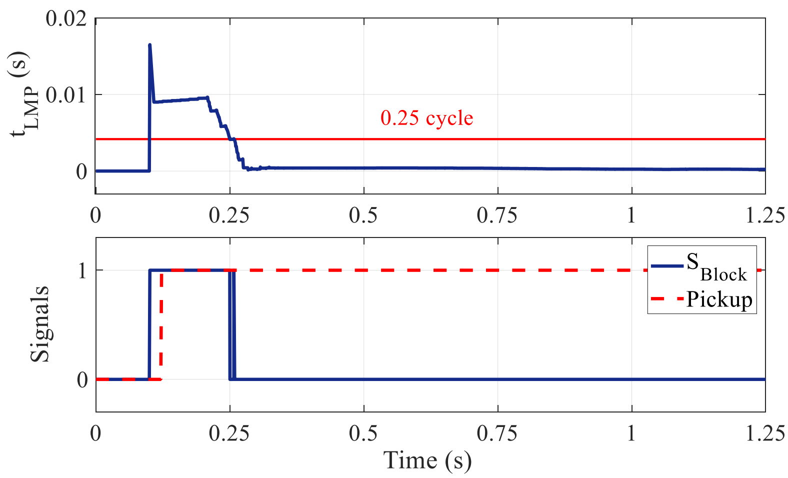

Figure 4.9. The signals of the gap detection method and the pickup signal of phase A during the transformer energization and CT saturation.

Figure 4.10 shows the performance of the gap detection algorithm during the GIC and a severe CT saturation scenario. In this case study, the CT saturation causes t_{LMP} to decrease below the threshold of 0.25 cycle at 0.79 s, which unnecessarily sets S_{Block} to 0 and can result in security issues. On the other hand, as observed in Figure 4.10, S_{MHB} of phase A remains asserted during the GIC and CT saturation. Similar performance is observed for phases B and C in this scenario.

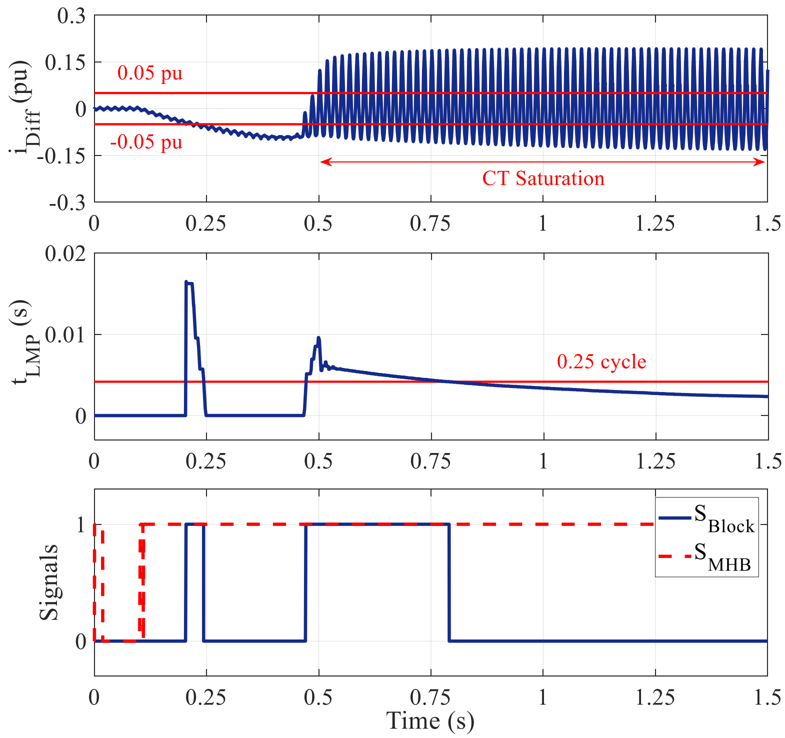

Figure 4.10. The signals of the gap detection method and the modified harmonic blocking signal of phase A during the GIC and severe CT saturation.

4.3.4 Sympathetic Inrush Currents

The proposed method's capability to distinguish the GIC from sympathetic inrush currents is verified in this subsection. While the existing transformer of Figure 3.1 serves the load in steady state, a second similar transformer parallel to the first transformer is energized at 0.1 s, leading to the flow of sympathetic inrush currents in the first transformer. The performance of the proposed scheme in this case study is illustrated in Figure 4.11. In this figure, the phase A differential currents of the first and second transformers are indicated as "sympathetic inrush" and "inrush", respectively. In Figure 4.11, both S_{GIC} and S_{Sup} remain equal to 0 during the second transformer energization, keeping S_{UBNOT} equal to 1. Thus, the proposed protection of the first transformer does not maloperate during the sympathetic inrush currents. Such a performance is also observed with the CT saturation.

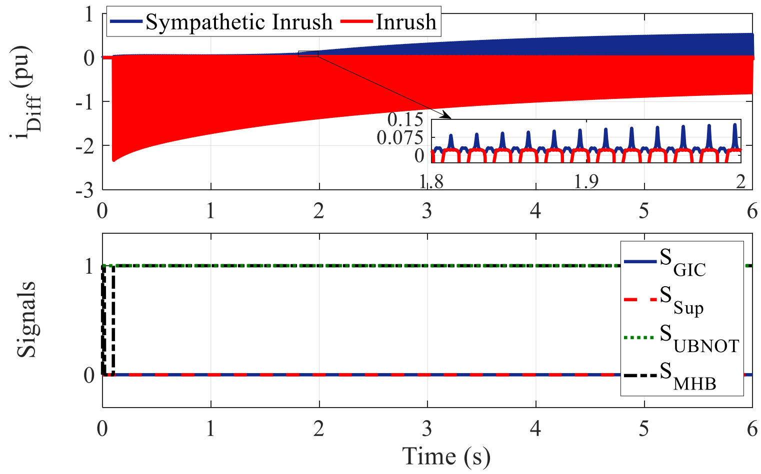

Figure 4.11. The phase A differential currents of the existing and the second parallel transformers and the proposed method performance during the sympathetic inrush currents.

4.3.5 Internal Faults during GIC

The simulated faults are phase A to ground faults with the resistances of 2175 Ω and 110 Ω, respectively, applied on the transformer's HV and LV sides under the GIC condition. According to Subsection 3.3.2, for faults with the resistances higher than these values, the differential relay does not assert a *PKP* under the GIC condition.

The signals of the proposed scheme and the HB signals for the LV-side fault are shown in Figure 4.12. The corresponding signals, related to the HV-side fault, are skipped in view of similarity. The results of Figure 4.12 indicate that S_{Sup} changes from 0 to 1 at 10.016 s, asserting S_{UB} and setting S_{UBNOT} to 0 at this instant since S_{GIC} is also 1. This leads to unblocking the relay as S_{MHB} is set to 0 for 3 cycles, despite the fact that S_{HB} is still asserted. As a result, fault clearance becomes possible under the GIC condition.

Three-phase signals of $\theta_{I_{2ndp}}$ and *RCC*, related to the internal fault at 10 s with the resistance of 110 Ω under the GIC condition, are shown in Figure 4.13. Despite the high resistance value, this fault leads to an *RCC* that exceeds thr_{RCC} of 6 pu/s for the faulted phase. Consequently, the fault is detected by the proposed method ($S_{Sup} = 1$), which results in overriding S_{HB} since the phase angles also satisfy the criteria in (4.1).

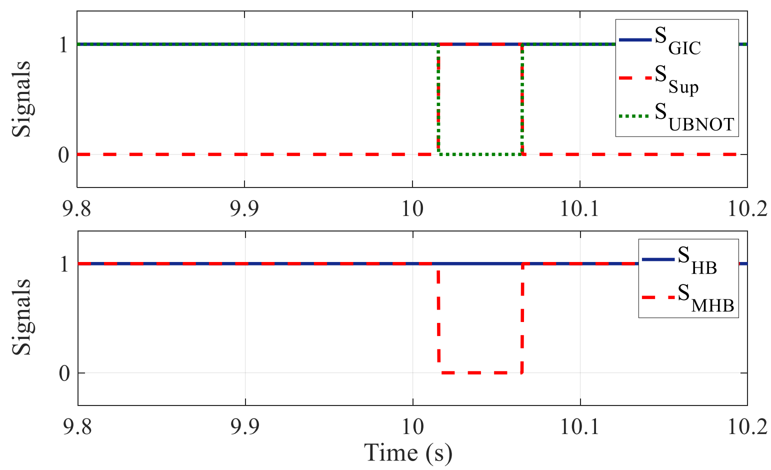

Figure 4.12. The signals of the proposed method and the harmonic blocking signals of phase A for the internal phase A to ground fault at 10 s on the LV side during the GIC.

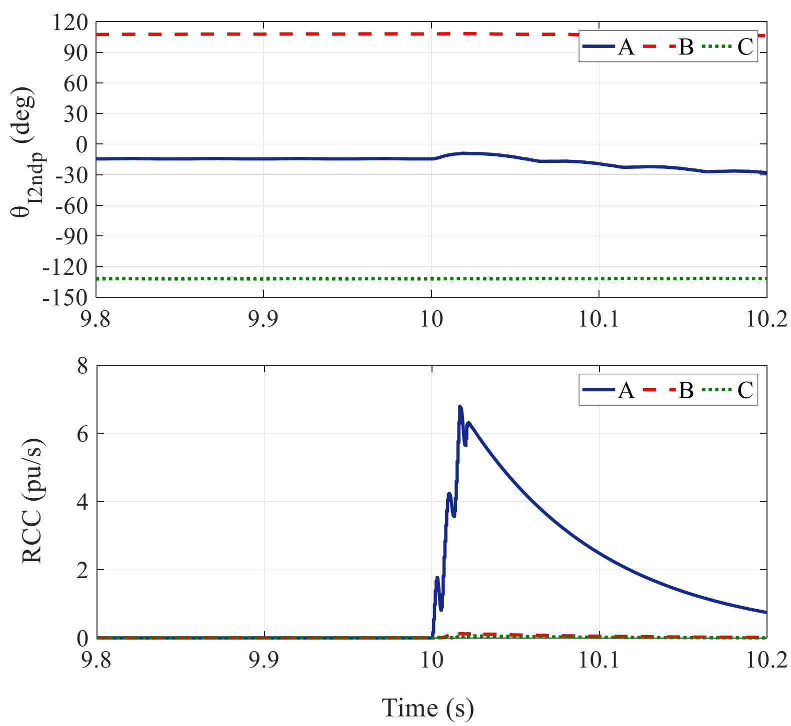

Figure 4.13. The phase angles of the differential current second harmonic components and rate of change of the differential currents for the internal phase A to ground fault at 10 s on the LV side during the GIC.

During the GIC, the behavior of the proposed method is investigated for the above LV-side terminal fault and CT saturation, with the simulation results of Figure 4.14. Before the fault occurrence at 10 s, CT1 is saturated due to the GIC, which leads to the high discrepancy between the primary ratio current and secondary current of the CT and the uneven LMPs of i_{Diff}. When the internal fault occurs, S_{Sup} is successfully issued, and S_{HB} is overridden ($S_{MHB} = 0$), considering that S_{GIC} is equal to 1. This shows the proposed method's capability to unblock the relay for the internal faults during the GIC and CT saturation.

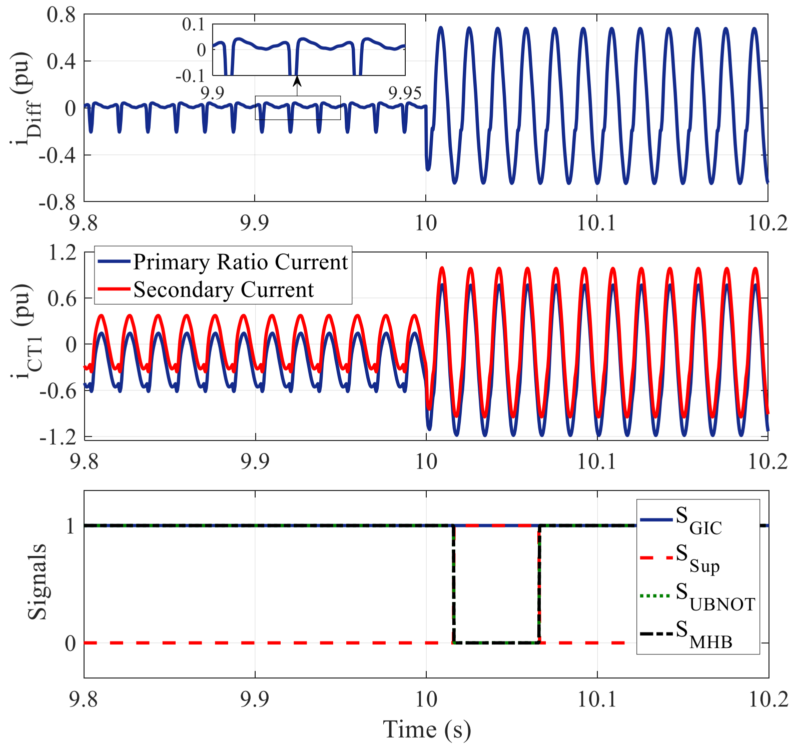

Figure 4.14. The differential current, the CT1 currents of phase A, and the proposed method performance for the internal phase A to ground fault at 10 s on the LV side during the GIC and CT saturation.

4.3.6 External Faults during GIC

Figure 4.15 illustrates the proposed method performance for a bolted external fault on the transformer's LV side (on phase A) at 10 s, under the GIC condition. It is observed that S_{Sup} is not issued for the external fault occurrence, which means that the proposed method can distinguish the internal fault from the external fault. Therefore, the relay remains blocked for the external fault since S_{MHB} is equal to 1. The simulation results also demonstrate a similar behavior for an external fault on the HV side under the GIC condition, and thus, they are not repeated here.

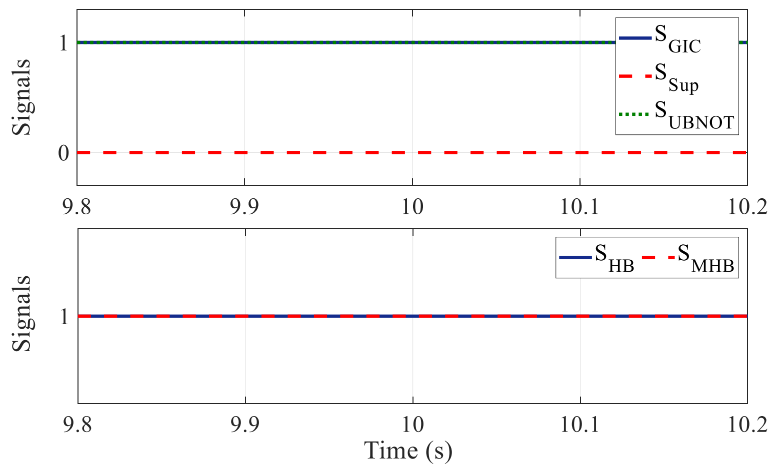

Figure 4.15. The signals of the proposed method and the harmonic blocking signals of phase A for the external phase A to ground fault at 10 s on the LV side during the GIC.

Figure 4.16 shows $\theta_{I_{2ndp}}$ and *RCCs* for the fault mentioned above. In this figure, because of the GIC presence, there is a negative-sequence relationship between the phase angles, and consequently, S_{GIC} is equal to 1 (Figure 4.15). In addition, as *RCCs* are lower than thr_{RCC} of 6 pu/s, S_{Sup} is not triggered.

In the presence of GIC and with the CT saturation, Figure 4.17 illustrates the behavior of the proposed method for the external fault on the LV side. The supplementary module does not issue S_{Sup} for the external fault while the CT1 is saturated due to the GIC; therefore, S_{UBNOT} and S_{MHB} remain unchanged and equal to 1, similar to Figure 4.15.

It is worth mentioning that CT saturation can affect *RCCs* during the faults. Nevertheless, based on the simulations conducted in this section, the CT saturation does not make the proposed

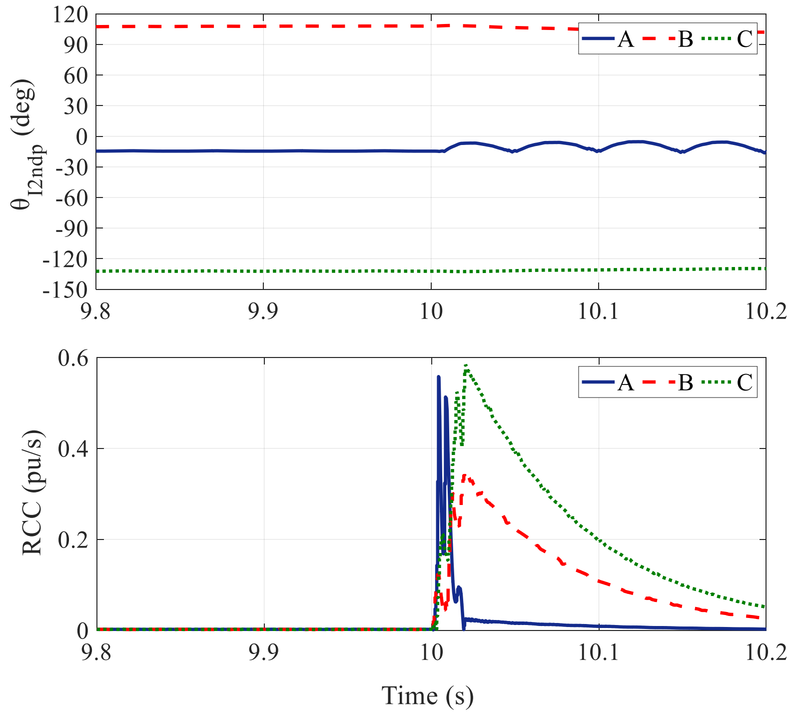

Figure 4.16. The phase angles of the differential current second harmonic components and rate of change of the differential currents for the external phase A to ground fault at 10 s on the LV side during the GIC.

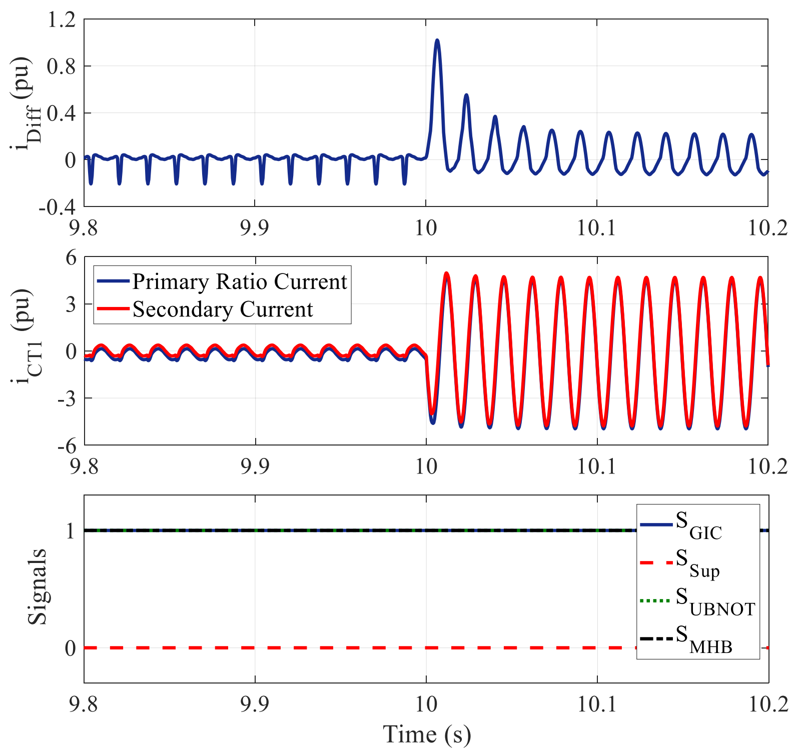

Figure 4.17. The differential current, the CT1 currents of phase A, and the proposed method performance for the external phase A to ground fault at 10 s on the LV side during the GIC and CT saturation.

scheme incapable of detecting the internal faults and differentiating them from the external faults under the GIC conditions.

4.3.7 Transformer Energization with Pre-Existing Faults

The performance of the proposed approach is investigated for the transformer energization while there is a pre-existing internal or external fault in the study system. The bolted phase A to ground faults are assumed to occur on the LV side of the transformer at 0.05 s, and the transformer is energized at 0.1 s. This study is carried out with and without CT saturation. Figure 4.18 shows the results related to the internal fault when CT1 is saturated around 0.12 s and then starts recovering from the saturation. In Figure 4.18, it is observed that for the internal fault, S_{Sup} is issued when the transformer is energized, while S_{GIC} remains 0. Therefore, the proposed approach does not unblock the differential protection (S_{UBNOT} = 1), as expected. It should be noted that in this case study, the differential relay issues a trip signal at 0.118 s since there is a *PKP* at this instant and S_{MHB} is temporarily set to 0, as observed in Figure 4.18. The performance is similar for the energization with a pre-existing internal fault when there is no CT saturation.

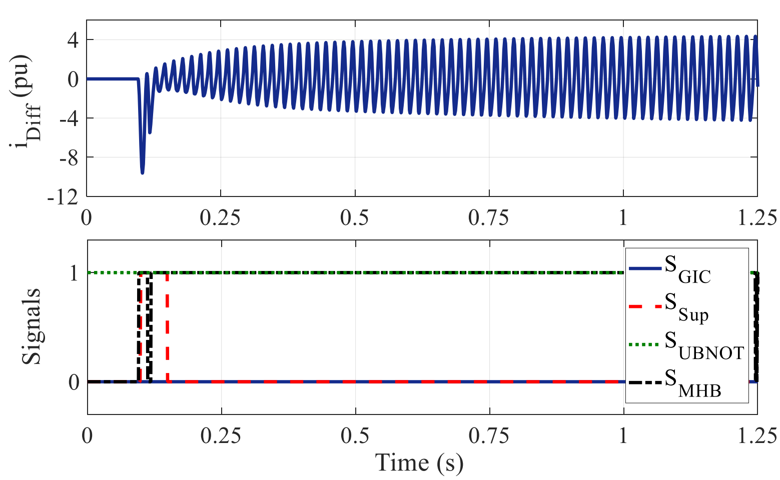

Figure 4.18. The differential current of phase A and the proposed method performance for the transformer energization with the pre-existing internal fault and the CT saturation.

The behavior of the proposed method for the pre-existing external fault with the CT saturation is illustrated in Figure 4.19. Around a cycle after the transformer energization, there is a sudden increase in the differential current of phase A, which is because of the saturation of both CT1 and CT2. This, in turn, makes S_{Sup} change to 1; however, the proposed scheme does not malfunction, and the differential protection is kept blocked ($S_{MHB} = 1$) since S_{GIC} is not asserted. It should be mentioned that without the CT saturation, S_{Sup} is not issued during the transformer energization with the pre-existing fault.

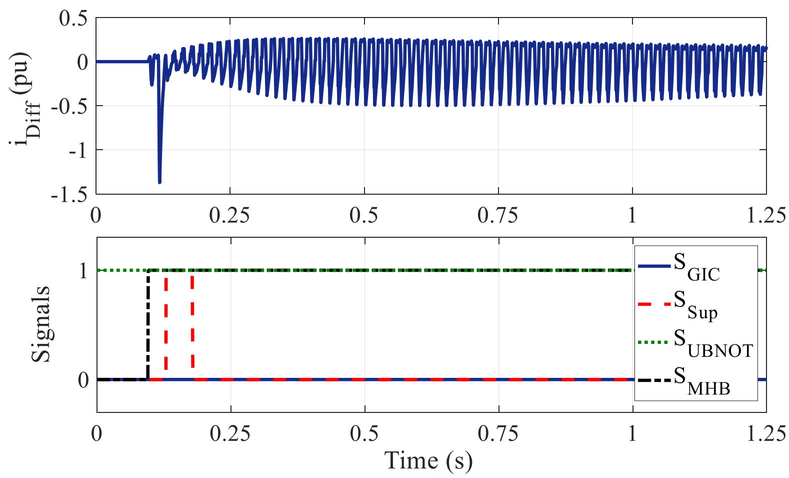

Figure 4.19. The differential current of phase A and the proposed method performance for the transformer energization with the pre-existing external fault and the CT saturation.

4.4 Performance of Relay with Unblocking Scheme

The vulnerability of power transformers to the GIC highly depends on their core constructions. The transformers with different core topologies represent different saturation severities, magnetizing current magnitudes, and harmonic characteristics as subjected to the same GIC level [16, 60]. In this section, the performance of the differential relay equipped with the proposed harmonic-based method is analyzed for different transformer types during the internal faults and the GIC. The CBM and SBM are considered in the studies of this section. The studies are conducted for two transformer types: one is the three-leg transformer (Section 3.1), hereafter referred to as T1, and the other one, T2, is a transformer bank consisting of three single-phase units. Unlike T1, the magnetic cores of the three phases are separate in T2, and therefore, no interphase magnetic coupling exists in T2. These two transformers are subjected to the GIC of 200 A at neutral and assumed to have similar ratings of 125 MVA and 500/115 kV, as well as the same Z_{SC} of 13%. The saturation data of T2 are the same as those provided in Table 3.2.

4.4.1 Three-Leg Transformer

With the integration of the proposed scheme, Figure 4.20 shows the performance of the proposed CBM-based relay for a bolted internal phase A to ground fault occurring at 10 s on the T1's LV side. In addition, the signals of the proposed SBM-based relay for the fault with the resistance of 105 Ω are illustrated in Figure 4.21. Without the proposed unblocking scheme, the original differential relays fail to operate for these two faults during the GIC, as discussed and shown in Chapter 3. According to Figure 4.20, the *PKP* is asserted at 10.022 s, and at the same time, the trip signal is sent to the CBs of T1 to trip the transformer and clear the fault in the system. Figure 4.20 also shows that the relay is unblocked by the proposed scheme at 10.002 s as the three-phase S_{MHB} are set to 0, which is because S_{UBNOT} changes to 0 at this time.

In Figure 4.21, S_{UBNOT} is set to 0 about 0.016 s after the fault occurrence, which leads to unblocking the relay since S_{MHB} of the three phases change to 0 around 10.016 s, while the three-phase S_{HB} are still asserted owing to the GIC flow. This allows the relay to trip when the *PKP* signal is issued at 10.041 s in the presence of GIC.

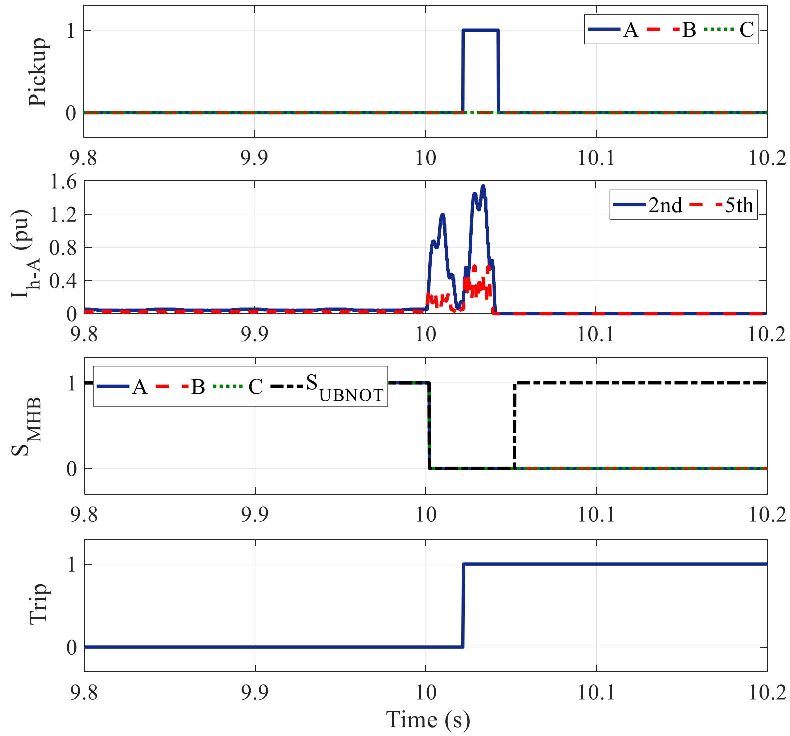

Figure 4.20. The signals of the proposed CBM-based differential relay for the bolted phase A to ground fault at 10 s on the T1's LV side during the GIC.

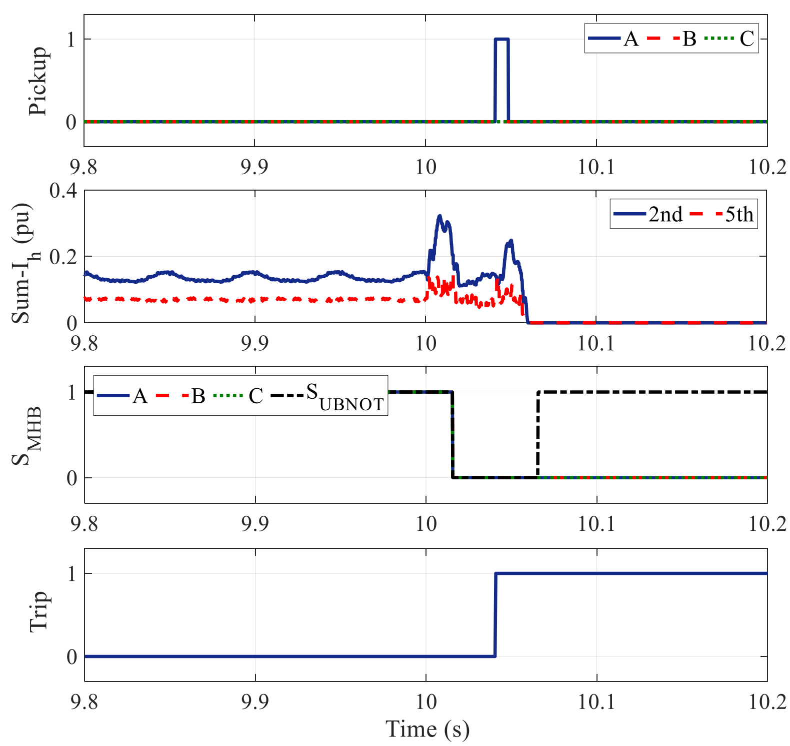

Figure 4.21. The signals of the proposed SBM-based differential relay for phase A to ground fault with the resistance of 105 Ω at 10 s on the T1's LV side during the GIC.

4.4.2 Three Single-Phase Transformer Units

With T2 represented in the study system, Figure 4.22 depicts signals of the proposed CBM-based relay when a bolted phase A to ground fault occurs at 10 s. Furthermore, the simulation results for a fault with R_F of 9 Ω (I_{op} = 4.094 pu) at 10 s are illustrated in Figure 4.23 for the SBM-based relay. Figures 4.22 and 4.23 show that the differential relays, equipped with the proposed unblocking scheme, are able to operate for the aforementioned faults under the GIC condition. This is due to the fact that the S_{HB} signals are overridden as S_{UB} is asserted in both fault cases (S_{UBNOT} = 0); nonetheless, the relays cannot trip for the faults without employing the proposed scheme. The studies of this section show that the proposed scheme significantly improves the differential protection dependability during the GIC, regardless of the transformer type.

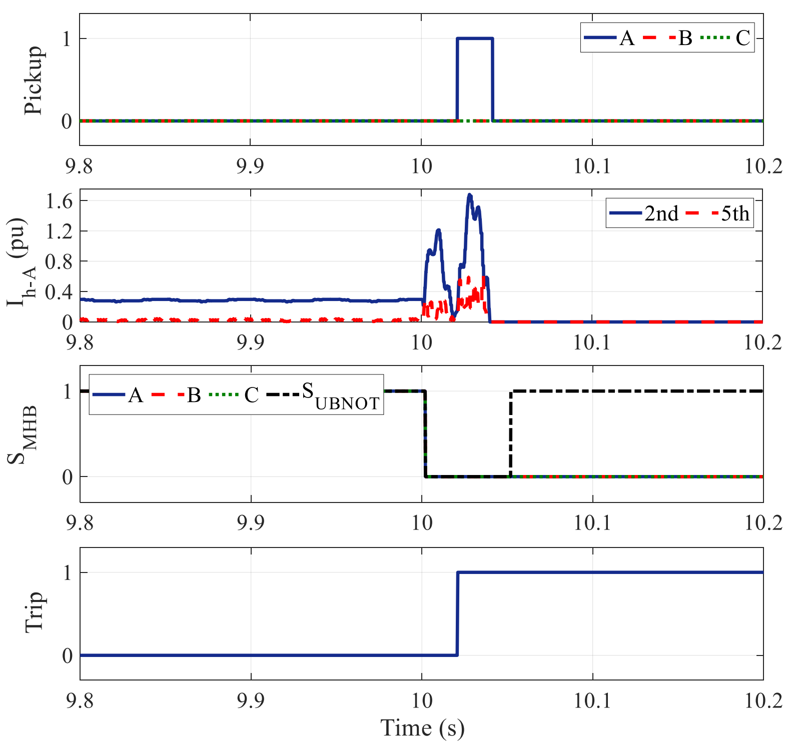

Figure 4.22. The signals of the proposed CBM-based differential relay for the bolted phase A to ground fault at 10 s on the T2's LV side during the GIC.

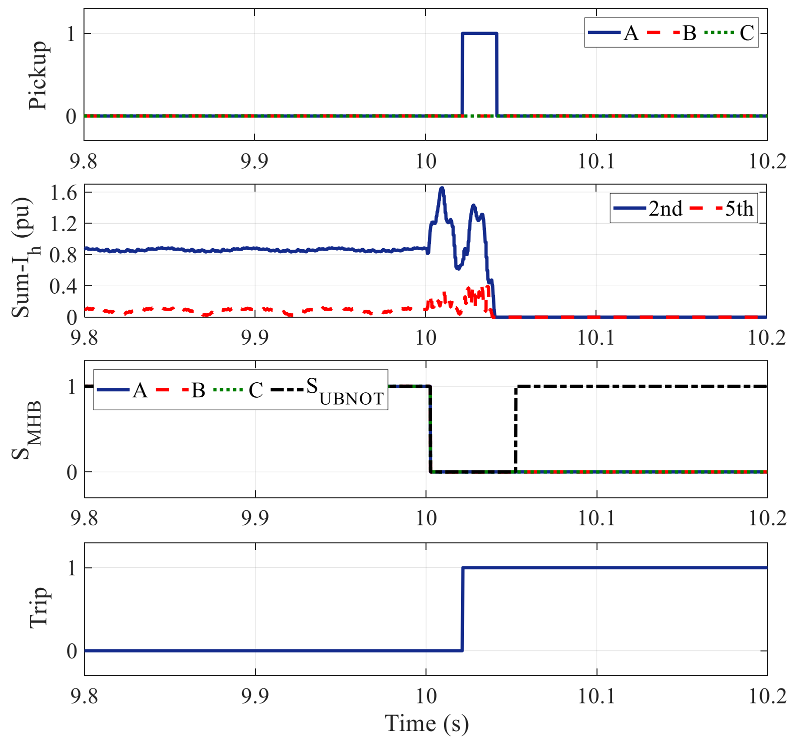

Figure 4.23. The signals of the proposed SBM-based differential relay for phase A to ground fault with the resistance of 9 Ω at 10 s on the T2's LV side during the GIC.

4.5 Summary

An unblocking scheme for transformer differential protection during the GMDs was introduced in this chapter. The scheme utilizes a harmonic-based GIC detection algorithm and an RCC-based fault detection logic to enhance the performance of differential relays during internal faults and GIC. It was shown that the relays, utilizing the proposed scheme, are dependable for the internal faults in the presence of GIC, while they cannot operate for the same faults if the unblocking scheme is not employed. The scheme effectiveness for the internal faults under the GIC condition was verified for different transformer types. Moreover, the scheme security during the inrush currents and external faults was extensively examined with and without considering the CT saturation. Chapter 5 proposes an alternative waveform-based unblocking approach.

Chapter 5
Waveform-Based Unblocking Scheme

5.1 Introduction

This chapter proposes a waveform-based unblocking scheme to enhance the dependability of existing HB-based differential relays under the GIC conditions while maintaining the security level. A GIC detection algorithm is devised that only requires the raw/unfiltered instantaneous differential current waveforms without filtering and extracting the harmonic components, as needed for the GIC detection algorithm of Chapter 4. Furthermore, instead of the RCC detection-based supplementary module in the previous chapter, the proposed waveform-based scheme utilizes the available *PKP* signals of the relay's fault detection module to unblock the relay solely for internal faults during the GIC.

5.2 Waveform-Based Approach

Figure 5.1 shows the logic of the differential protection equipped with the waveform-based unblocking scheme. As discussed in Chapter 4, the goal is to override the HB signals (i.e., S_{HB}) for the internal faults during the GIC flow in the transformer. The unblocking scheme of Figure 5.1 includes a waveform-based GIC detection (WGD) module that sets S_{GIC} to 1 under the GIC conditions by processing the instantaneous differential current waveforms (i_{Diff}). The three-phase

PKP signals, based on the relay's operation-restraint characteristic (Figure 2.2), are employed for unblocking the relay during the internal faults such that S_{PKP} is asserted if at least one phase picks up (PKP = 1). On the other hand, S_{PKP} is expected to remain 0 for the external faults, keeping the unblocking signal (S_{UB}) at 0. Today's advanced transformer differential relays generally utilize more sophisticated logics, including external fault detection logics, to supervise the *PKP* signals and provide further security for the external faults, specifically during CT saturation [67, 68, 92, 93].

In no-fault conditions, especially when the transformer is lightly loaded, significantly high GIC magnitudes can make the operation-restraint differential relays wrongly pick up owing to the elevated differential current fundamental component (I_{op}) stemming from the transformer core saturation [35, 39]. In order to avoid unwanted unblocking in such conditions, the proposed waveform-based approach employs the RCC detection module, with the logic of Figure 4.5, that keeps S_{RCC}, and thereby, S_{UB} at 0 in the absence of faults. In this chapter, however, the RCC detection threshold (i.e., thr_{RCC}) is required to be high enough to maintain security only in no-fault conditions and low enough to trigger S_{RCC} for internal faults. According to Figure 5.1, an S_{UB} = 1 is issued provided that S_{GIC}, S_{PKP}, and S_{RCC} are all asserted, setting S_{MHB} of the three phases to 0, allowing the relay to operate for the in-zone faults under the GIC conditions if S_{HB} is still 1.

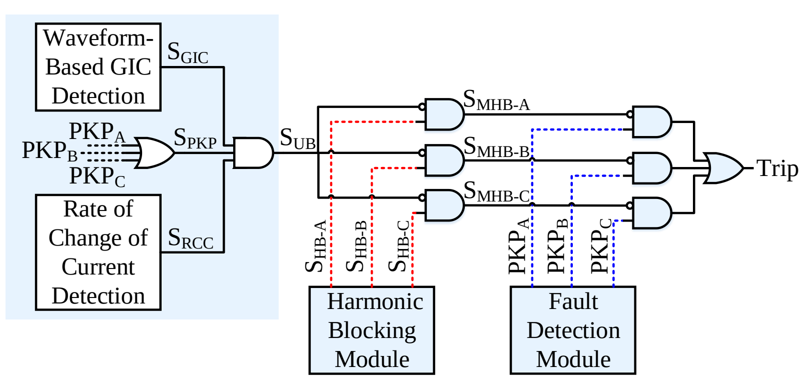

Figure 5.1. Transformer differential protection utilizing the waveform-based unblocking scheme.

5.2.1 Waveform-Based GIC Detection

The part-cycle saturation of the transformer core under the GIC conditions leads to unipolar/asymmetrical three-phase differential current waveforms in one direction. Figure 5.2(a) illustrates the typical i_{Diff} of the three phases during the GIC. In this figure, it can be observed that the asymmetrical waveforms are all in the negative direction in the presence of GIC. Nevertheless, one of the phases has an opposite direction compared to other phases during the transformer energization, as depicted in Figure 5.2(b).

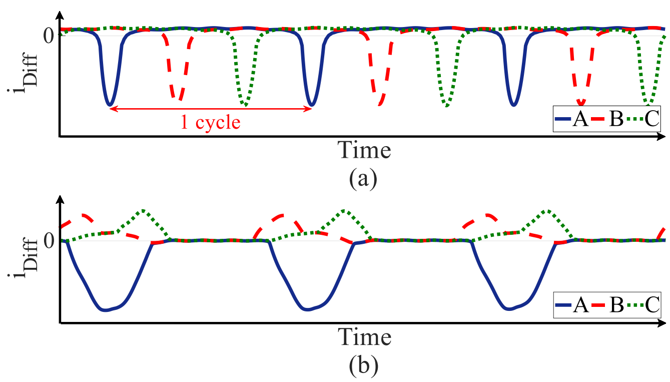

Figure 5.2. Typical differential current waveforms of the three phases: (a) during the GIC and (b) during the transformer energization.

During a GMD, the GIC-caused DC components of the transformer currents have the same magnitudes and polarities in all three phases, and the core is biased and saturated at the same level and in the same direction in the three phases. As a result, the asymmetrical i_{Diff}, representing the transformer's magnetizing currents, possess the same direction under the GIC conditions [8, 16]. During the energization, however, the three-phase core fluxes obtained by the integration of the voltage waveforms lead to both positive and negative core saturation directions in the three phases, regardless of the transformer switching angle and the point on the wave. Thereby, the three-phase i_{Diff} represent different directions in the energization conditions. The waveform-based GIC detection module of Figure 5.1 uses these principles to detect the GIC conditions and distinguish them from the transformer energization cases.

In order to decide whether i_{Diff} of one phase is in a positive or negative direction, the maximum (*MAX*) and minimum (*MIN*) of the waveform in each cycle (T) are tracked. If the *MAX* magnitude (|*MAX*|) is larger than or equal to the *MIN* magnitude (|*MIN*|), i_{Diff} is considered to be in a positive direction; otherwise, it is in a negative direction. Figure 5.3(a) depicts i_{Diff} of phase A ($i_{\mathrm{Diff\text{-}A}}$) and its associated *MAX* and *MIN* values under a GIC condition. In this figure, it is observed that |*MAX*| is smaller than |*MIN*|, and as a result, the waveform is in a negative direction.

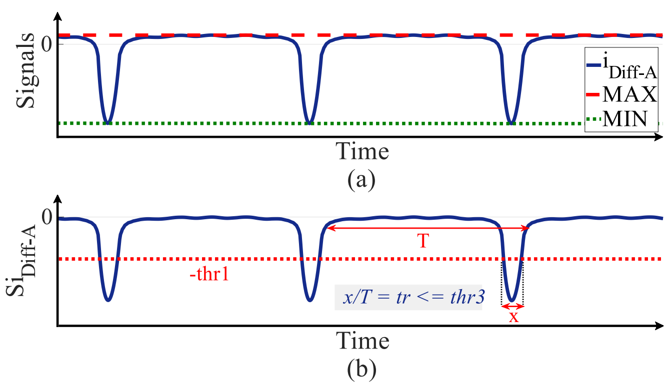

Figure 5.3. Signals during the GIC: (a) differential current waveform of phase A with its *MAX* and *MIN* values and (b) shifted differential current waveform of phase A.

The waveform is first shifted upward or downward depending on its *MAX* and *MIN* values using (5.1) to check the waveform asymmetry. In (5.1), Si_{Diff} is the shifted differential current waveform. The differential current waveform is shifted to obtain a waveform that has a maximum or minimum of 0 in each cycle. In other words, Si_{Diff} is either positive or negative within a cycle. As it takes one cycle to determine *MAX* and *MIN* of i_{Diff} in each cycle, i_{Diff} with a delay of T, i.e., $i_{\mathrm{Diff}}(t\text{-}T)$, is employed in (5.1) to add to its corresponding *MAX* and *MIN* values in each cycle. The positive or negative Si_{Diff} is subsequently compared with an adjustable threshold (*thr1*) or -*thr1*, respectively. Figure 5.3(b) illustrates $Si_{\text{Diff-A}}$ that is compared with -*thr1* as the shifted waveform is negative. In each cycle, the period of time in which Si_{Diff} is lower (or higher) than -*thr1* (or *thr1*) is calculated, which is shown by *x* in Figure 5.3(b). If the ratio of *x* to *T*, referred to as *tr*, meets the criteria in (5.2), i_{Diff} is considered asymmetric.

$$Si_{\text{Diff}}(t) = \begin{cases} i_{\text{Diff}}(t-T) - MIN & \begin{array}{c} MAX > 0, MIN < 0, \& \\ MAX \geq |MIN| \end{array} \\ i_{\text{Diff}}(t-T) - MAX & \begin{array}{c} MAX > 0, MIN < 0, \& \\ MAX < |MIN| \end{array} \\ i_{\text{Diff}}(t-T) - MIN & MAX > 0 \ \& \ MIN > 0 \\ i_{\text{Diff}}(t-T) - MAX & MAX < 0 \ \& \ MIN < 0 \end{cases} \tag{5.1}$$

$$thr2 \leq \ tr \leq thr3 \tag{5.2}$$

In (5.2), *thr2* and *thr3* are the adjustable thresholds. The threshold *thr2* is to prevent false GIC detection stemming from transients and noise, and *thr3* is to distinguish between the asymmetrical and symmetrical waveforms. For example, as indicated in Figure 5.3(b), the *x*-to-*T* ratio (i.e., *tr*) of $Si_{\text{Diff-A}}$ does not exceed *thr3*, and hence, the waveform is considered asymmetric. On the other hand, i_{Diff} is assumed to be bipolar/symmetric, provided that *tr* is larger than *thr3*. As an example, Figure 5.4 shows an $Si_{\text{Diff-A}}$ during a short-circuit fault. In this figure, the *x*-to-*T* ratio of $Si_{\text{Diff-A}}$ is larger than *thr3*; thus, the associated $i_{\text{Diff-A}}$ is considered symmetric.

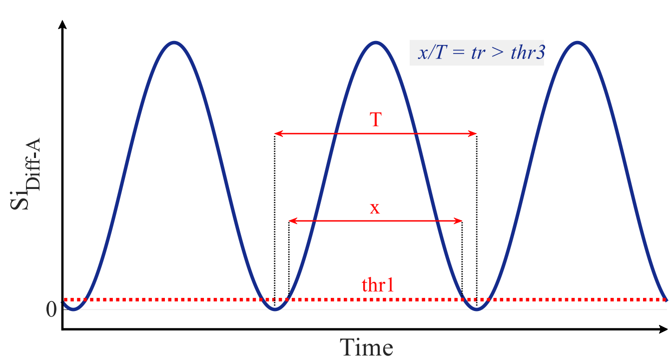

Figure 5.4. The shifted differential current waveform of phase A during a short-circuit fault.

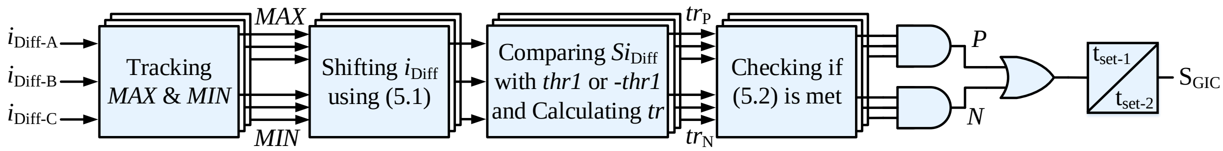

Figure 5.5. The logic of the waveform-based GIC detection module of Figure 5.1.

The logic of the WGD module is depicted in Figure 5.5. The *MAX* and *MIN* values associated with i_{Diff} of the three phases are tracked for upward or downward shifting of the differential current waveforms. For each phase, if the associated i_{Diff} is shifted upward, the resulting positive Si_{Diff} is compared with *thr1*. In this case, tr_{N} is 0, and tr_{P} is larger than 0 if Si_{Diff} exceeds the threshold. Otherwise, $tr_{\text{N}} > 0$ if the waveform is shifted downward and Si_{Diff} is smaller than -*thr1* for a portion of a cycle. According to Figure 5.5, if tr_{P} or tr_{N} of the three phases meet the criteria in (5.2), *P* or *N* is set to 1, representing that the three-phase i_{Diff} are all asymmetric in a positive or negative direction, respectively. The GIC is detected, and S_{GIC} changes to 1 if either *P* or *N* remains asserted for more than $t_{\text{set-1}}$. This pickup time is set to avoid issuing the wrong S_{GIC} during the transients. *P* or *N* may immediately change from 1 to 0 after the fault occurrence as i_{Diff} of at least one phase becomes symmetric. In this regard, S_{GIC} is maintained at 1 for $t_{\text{set-2}}$ after *P* or *N* changes to 0 to ensure that the differential relay is unblocked under the GIC conditions.

5.3 Performance Evaluation

In this section, the performance of the proposed protection scheme of Figure 5.1 is examined, considering numerous scenarios. The threshold *thr1* of the WGD algorithm (Figure 5.5) is set at 0.1 pu. This value ensures that *tr* of each phase, and subsequently, S_{GIC} remain 0 in the normal operating conditions of the study system of Figure 3.1. In addition, *thr1* of 0.1 pu is adequate to trigger *tr* in abnormal cases, such as the GIC conditions. The threshold *thr3* is obtained based on the *tr* values of various asymmetrical and symmetrical differential current waveforms corresponding to the GIC conditions, inrush currents, and short-circuit faults. According to these studies, *thr3* of 75% (of *T*) provides the WGD algorithm with an acceptable capability to differentiate between asymmetrical and symmetrical differential current waveforms. The threshold *thr2* is considered to be 5% in this study. Furthermore, $t_{\text{set-1}}$ and $t_{\text{set-2}}$ in Figure 5.5 are set at 2 and 3 cycles, respectively.

The RCC detection threshold (i.e., thr_{RCC}) is set at 2 pu/s, that is high enough to keep S_{RCC} at 0 in the no-fault conditions during the GIC, while ensuring dependability for the in-zone faults in the study system. In the studies of this chapter, the settings of the differential relay's operation-restraint characteristic are based on those provided in [66] and presented in Table 5.1. Moreover, it is assumed that the HB module of Figure 5.1 employs the CBM with thr_{2nd} and thr_{5th} of 15% and 35%, respectively.

TABLE 5.1. THE DIFFERENTIAL RELAY SETTINGS

I_{pkp}	0.3 (pu)
I_{bkp}	3 (pu)
s_1	25 (%)
s_2	60 (%)
t_{pkp}	0.02 (s)

5.3.1 GIC without Faults

Figure 5.6 depicts the proposed differential relay behavior when the GIC flow in the transformer is initiated at 0.1 s. After the early transitions, $S_{\text{HB-ABC}}$ (i.e., S_{HB} of phases A, B, and C) and $S_{\text{MHB-ABC}}$ settle at 1 owing to the GIC-caused second and fifth harmonics, and the relay is blocked. Observe that the GIC flow is detected by the WGD module of Figure 5.1 at 1.84 s as S_{GIC} is set to 1. Since S_{RCC} and S_{PKP} are equal to 0, S_{UB} is not asserted, and the relay remains blocked. Therefore, the relay malfunction is not likely in this condition. It is worth mentioning that the performance is similar in the no-load condition.

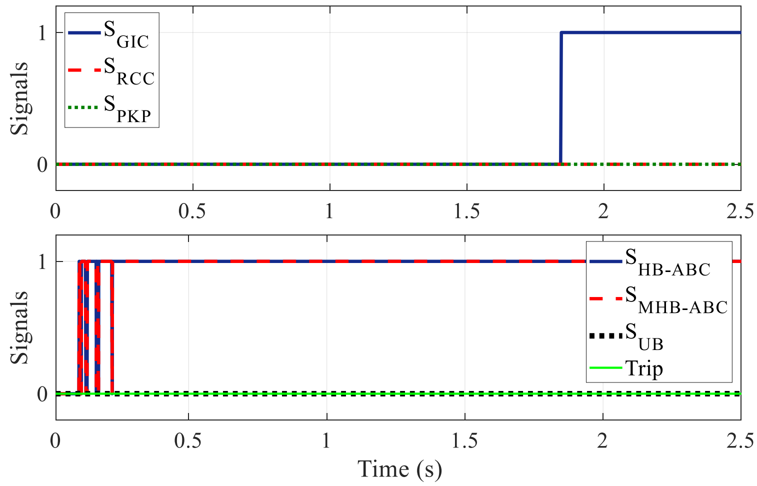

Figure 5.6. The proposed differential protection performance under the GIC condition.

The differential protection performance is also studied when CT1 (Figure 3.1) is saturated due to the GIC. In this scenario, the relay response is the same as the one depicted in Figure 5.6. Figure 5.7 illustrates the behavior of the WGD algorithm during the GIC and CT saturation. In Figure 5.7, before the CT saturation occurs around 1.5 s, both *MAX* and *MIN* values of $i_{\text{Diff-A}}$ are negative; therefore, the waveform is shifted upward with the magnitude of *MAX*, according to (5.1). In the CT saturation state, *MAX* is positive, while *MIN* is negative with a larger magnitude than *MAX*, resulting in the downward shifting of $i_{\text{Diff-A}}$ with the amount of *MAX*. Consequently, $Si_{\text{Diff-A}}$ (also $Si_{\text{Diff-B}}$ and $Si_{\text{Diff-C}}$) is a completely negative waveform during the GIC and compared with -*thr1*, as depicted in Figure 5.7. In this figure, the non-flat LMPs of $Si_{\text{Diff-A}}$ stem from the CT saturation.

As observed in Figure 5.7, *N* (Figure 5.5) is asserted at 2.08 s when tr_{N} of the three phases are all above *thr2*. This sets S_{GIC} to 1 around 2.11 s, which is two cycles ($t_{\text{set-1}}$) after *N* is asserted. Thereby, the WGD algorithm can successfully detect the GIC condition during the CT saturation.

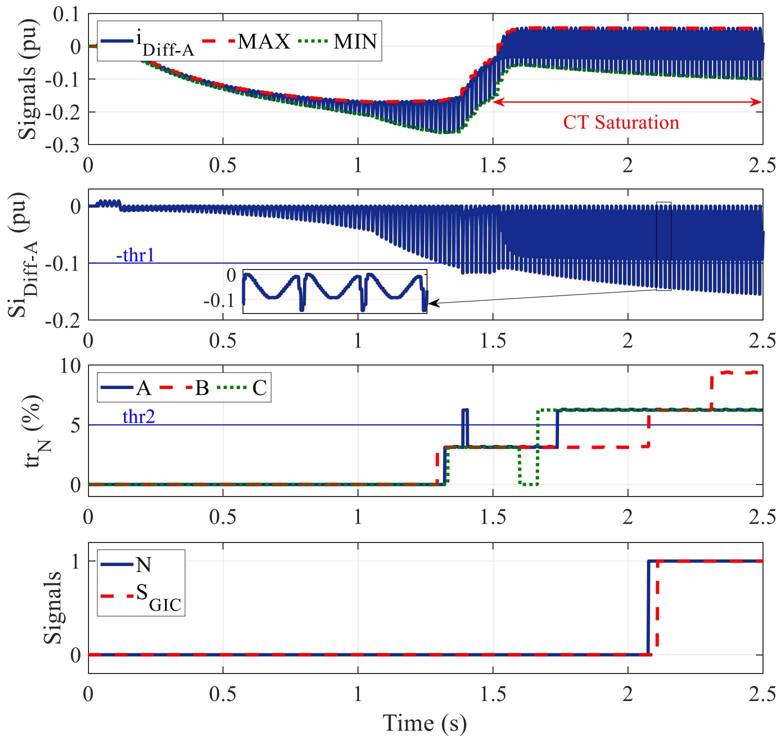

Figure 5.7. Performance of the waveform-based GIC detection algorithm under the GIC condition and CT saturation.

5.3.2 GIC with Faults

The behavior of the differential relay equipped with the waveform-based approach is investigated for the internal and external faults when the GIC exists. The bolted faults occur on the HV and LV sides of the transformer at 10 s when the GIC is 200 A. The results for the internal fault on the LV side are shown in Figure 5.8. Because of the similarity, the results related to the HV-side faults are skipped here. In Figure 5.8, before the occurrence of phase A to ground fault at 10 s, the three-phase i_{Diff} are asymmetric in the negative direction; as a result, tr_N of the three phases are between *thr2* and *thr3*, asserting S_{GIC}. After the fault, i_{Diff-A} becomes symmetric, which makes tr_{N-A} exceed *thr3* at 10.03 s, changing N to 0. Nonetheless, S_{GIC} is maintained at 1 for three cycles (t_{set-2}) after N becomes 0. In Figure 5.8, S_{RCC} is issued at 10.001 s when RCC_A exceeds thr_{RCC}, as depicted in Figure 5.9. S_{PKP} in Figure 5.8 is asserted due to a pickup for the faulty phase A at 10.022 s (i.e.,

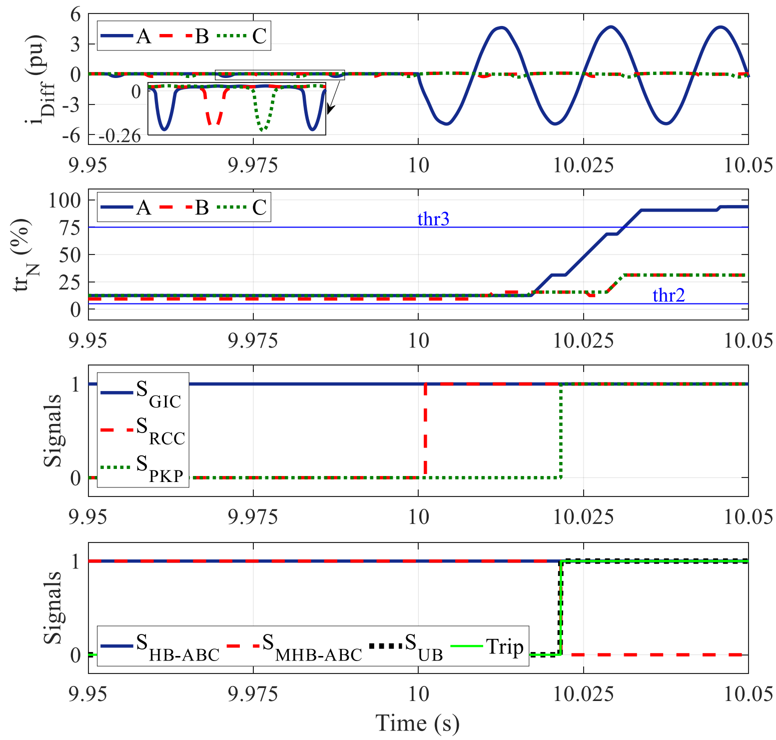

Figure 5.8. The proposed differential protection performance for the internal fault during the GIC.

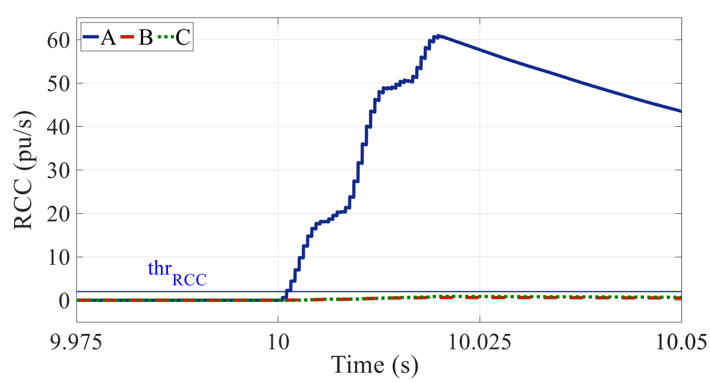

Figure 5.9. *RCCs* of the three phases for the internal fault during the GIC.

PKP_A = 1). This is 0.02 s (t_{PKP} in Table 5.1) after $I_{op\text{-}A}$ surpasses RES_A at 10.002 s, as shown in Figure 5.10. Consequently, S_{UB} is set to 1 at 10.022 s and unblocks the differential relay by making $S_{MHB\text{-}ABC}$ change to 0; hence, the relay can issue the trip signal for the fault. In the studies of this chapter, the CBs in the study system (Figure 3.1) are kept closed in the simulations after the trip signal is issued by the relay for post-fault demonstration purposes.

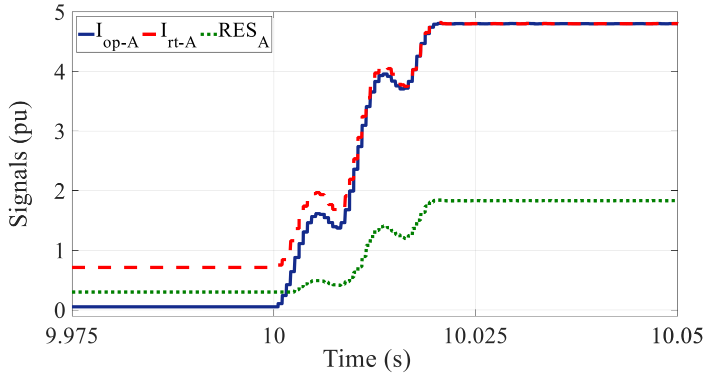

Figure 5.10. I_{op}, I_{rt}, and *RES* of the faulty phase A for the internal fault during the GIC.

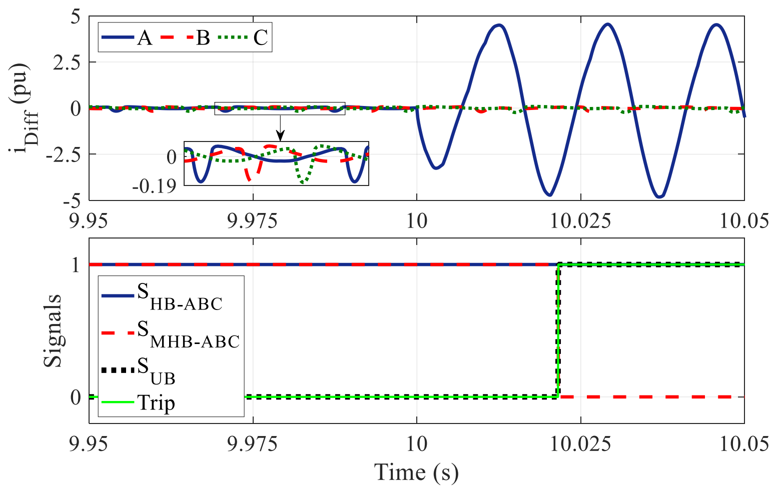

Figure 5.11. The proposed differential protection performance for the internal fault during the GIC and CT saturation.

It should be noted that without the proposed approach, the relay cannot operate for the aforementioned fault during the GIC since $S_{HB\text{-}ABC}$ is still asserted after the fault inception at 10 s (Figure 5.8). Although the fault on phase A forces $S_{HB\text{-}A}$ to 0 owing to an increase in $I_{op\text{-}A}$, S_{HB} of phases B and C, and thus, $S_{HB\text{-}ABC}$ remain asserted (Figure 2.4).

Figure 5.11 illustrates the proposed differential protection performance for the internal fault under the GIC condition and the saturation of CT1. In Figure 5.11, the three-phase i_{Diff} include the non-flat LMPs because of the CT saturation, unlike the waveforms shown in Figure 5.8 with the flat LMPs. The relay is effectively unblocked during the fault and CT saturation as S_{UB} changes to

1, causing $S_{MHB\text{-}ABC}$ to become 0. Subsequently, the trip signal can be issued, although $S_{HB\text{-}ABC}$ is still asserted. The proposed relay behavior for the external phase A to ground fault (on the LV side) at 10 s under the GIC condition and CT1 saturation is shown in Figure 5.12. It can be observed that after the fault occurs, S_{UB} is not asserted due to S_{PKP} = 0. Hence, the relay remains blocked ($S_{MHB\text{-}ABC}$ = 1) and does not malfunction for the external fault during the CT saturation.

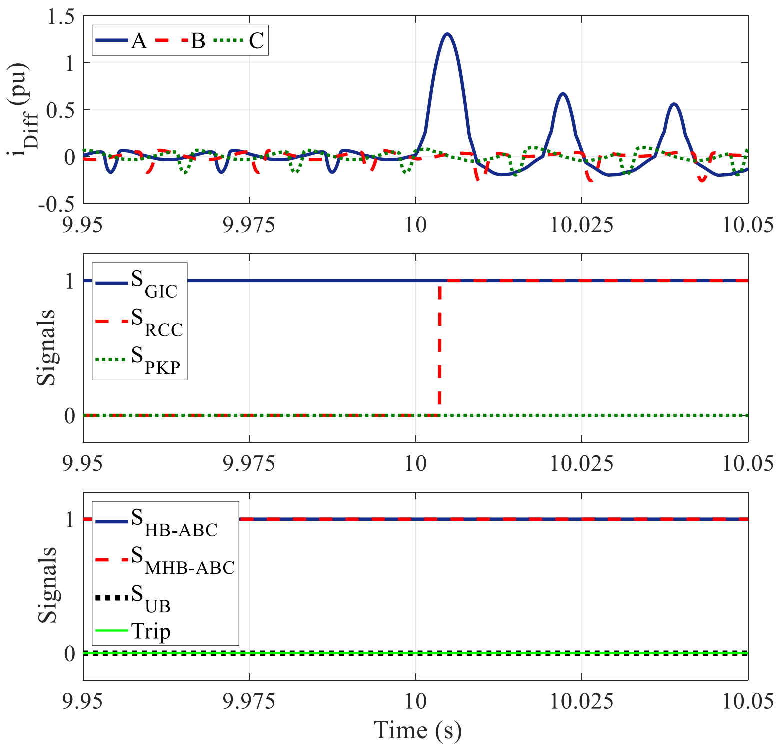

Figure 5.12. The proposed differential protection performance for the external fault during the GIC and CT saturation.

5.3.3 Inrush Currents

In this subsection, the performance of the proposed differential protection is investigated for the inrush currents that occur by energizing the transformer at 0.1 s. Figure 5.13 shows the relay behavior in this case study. The relay remains blocked ($S_{MHB\text{-}ABC}$ = 1) during the energization as

S_{GIC}, and consequently, S_{UB} are not asserted, although S_{RCC} and S_{PKP} are set to 1. As a result, there is no maloperation for the inrush currents.

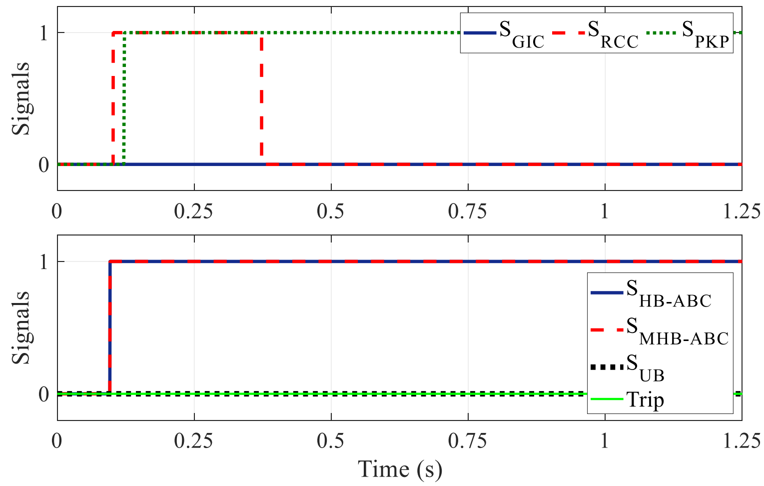

Figure 5.13. The proposed differential protection performance during the transformer energization.

The proposed relay performance during the energization and CT saturation is depicted in Figure 5.14. In this figure, $i_{Diff\text{-}A}$ is in the negative direction (shifted downward), while $i_{Diff\text{-}B}$ and $i_{Diff\text{-}C}$ are in the positive direction (shifted upward). The CT saturation occurs around 0.5 s for phase A, leading to a temporary increase in $tr_{N\text{-}A}$. Observe that in this case study, only $tr_{N\text{-}A}$, $tr_{P\text{-}B}$, and $tr_{P\text{-}C}$ have values between *thr2* and *thr3*, and $tr_{P\text{-}A}$, $tr_{N\text{-}B}$, and $tr_{N\text{-}C}$ are 0; therefore, neither *P* nor *N* is asserted, keeping S_{GIC} equal to 0. Similar to Figure 5.13, although both S_{RCC} and S_{PKP} are set to 1, S_{UB} is not asserted because of $S_{GIC} = 0$. Hence, the relay is kept blocked ($S_{MHB\text{-}ABC} = 1$) and does not issue a false trip signal for the inrush currents during the CT saturation. It is worth mentioning that in Figure 5.14, S_{RCC} is temporarily re-asserted at 0.5 s due to the CT saturation, but it does not cause maloperation.

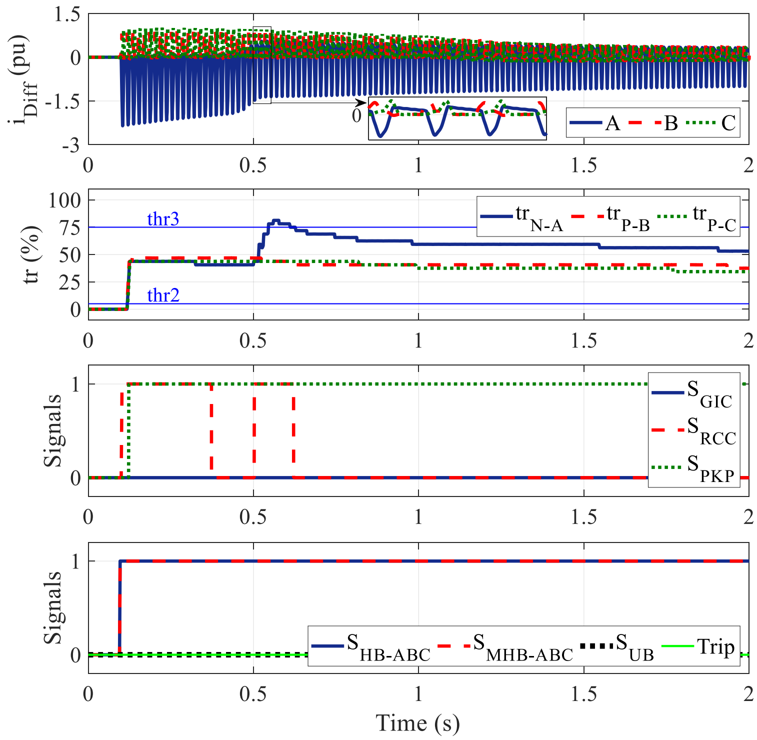

Figure 5.14. The proposed differential protection performance during the transformer energization and CT saturation.

5.3.4 Remnant Flux Effect during Energization

Since the core remnant flux affects the transformer inrush currents, and thus, the differential current waveforms, the remnant flux effect during the energization is also studied here. The transformer energization is simulated for the following different sets of three-phase remnant fluxes as the percentage of the rated operating flux of the transformer:

- *Set I*: ϕ_A = 80%, ϕ_B = -40%, and ϕ_C = -40%
- *Set II*: ϕ_A = -60%, ϕ_B = 10%, and ϕ_C = 50%

Figures 5.15(a) and (b) illustrate the three-phase i_{Diff} and the corresponding *tr* values for *Set I* and *Set II* of the remnant fluxes, respectively. In these figures, it is observed that once the transformer is energized at 0.1 s, the remnant fluxes result in different magnitudes of i_{Diff}, compared to the three-phase i_{Diff} shown in Figure 5.14 related to the energization without the remnant flux. However, in Figure 5.15 (similar to Figure 5.14), the $i_{Diff\text{-}A}$ waveforms have opposite directions with respect to phases B and C, keeping $tr_{P\text{-}A}$, $tr_{N\text{-}B}$, and $tr_{N\text{-}C}$ at 0 for both sets of the remnant fluxes. Consequently, S_{GIC} is not asserted by the WGD algorithm, and thereby, the remnant fluxes do not affect the performance of the waveform-based unblocking approach during the energization (S_{UB} = 0). Since i_{Diff} of one phase is in a different direction than the other phases during the transformer energization, the malfunction of the proposed approach is unlikely for the inrush currents, regardless of the remnant flux.

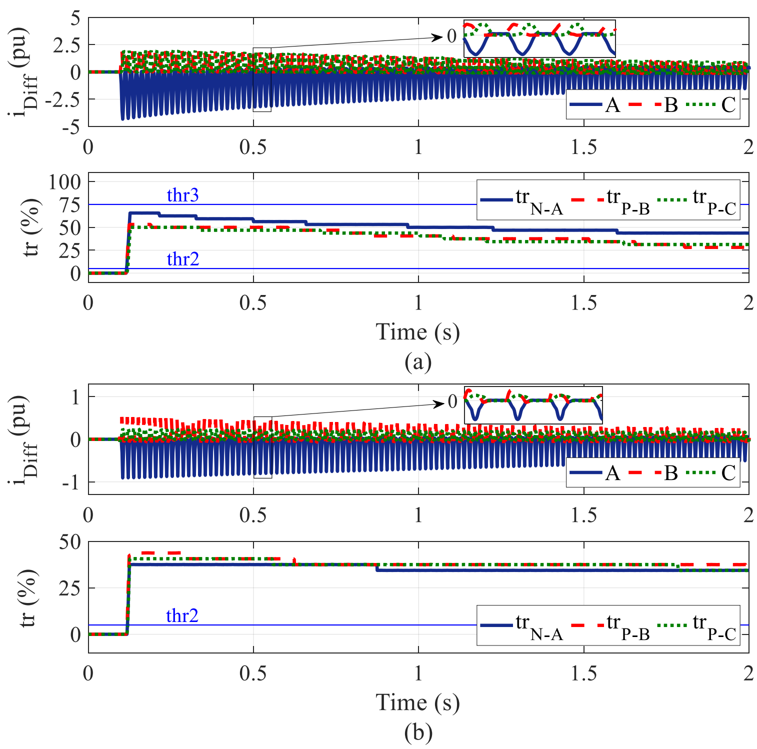

Figure 5.15. The three-phase differential current waveforms and the associated *tr* values during the transformer energization with different remnant fluxes: (a) *Set I* of remnant fluxes and (b) *Set II* of remnant fluxes.

5.3.5 Sympathetic Inrush Currents

In order to show that the differential protection, utilizing the waveform-based approach, does not malfunction during the parallel transformer energization, the energization of a second transformer is simulated in the study system, as described in Subsection 4.3.4. Figure 5.16 depicts the performance of the relay, protecting the original transformer, in this scenario. In this figure, it can be observed that the sympathetic inrush current of phase A ($i_{\text{Diff-A}}$) is in the positive direction, and those of phases B and C are in the negative direction. Hence, P and N are not triggered, similar to the transformer energization conditions discussed in Subsections 5.3.3 and 5.3.4, and S_{GIC} remains equal to 0. This shows that the WGD algorithm can successfully discriminate between the sympathetic inrush currents and the GIC. Moreover, S_{RCC} and S_{PKP} are not asserted in this case study. According to Figure 5.16, the relay is blocked after energizing the second transformer since $S_{\text{MHB-ABC}}$ is set to 1. Therefore, no maloperation is likely in such a condition. It should be added

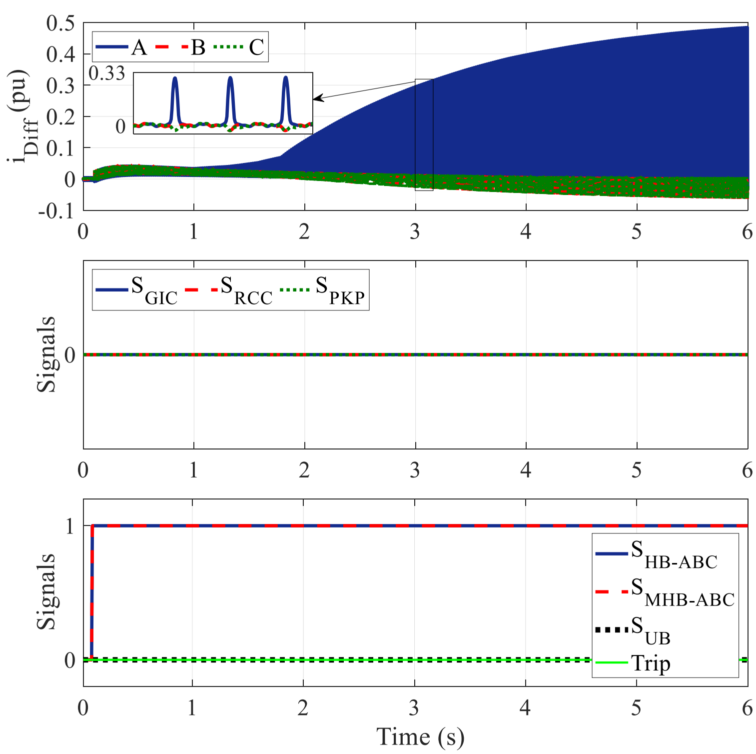

Figure 5.16. The proposed differential protection performance during the parallel transformer energization.

that the relay behavior is the same as in Figure 5.16 if the CT saturation occurs during the parallel transformer energization.

5.3.6 Measurement Noise

The robustness of the WGD module of the proposed waveform-based approach is studied for the noisy differential current waveforms. In this regard, the white Gaussian noise [94, 95] is added to the three-phase i_{Diff}, as the inputs of the WGD algorithm of Figure 5.5, resulting in a signal-to-noise ratio (SNR) of 30 dB [94] for each phase. The noise study is conducted in the GIC and transformer energization scenarios with the CT saturation, which are considered in Subsections 5.3.1 and 5.3.3, respectively. Figure 5.17 shows the results under the GIC condition. In this figure, the variations in the three-phase tr_{N} are due to the noise. However, these variations are insignificant, and the tr_{N} values remain between *thr2* and *thr3* (75%) after the initial transients. In the noise condition, the GIC flow in the transformer is detected at 2.13 s (S_{GIC} = 1), which is close to the GIC detection instant of 2.11 s in Figure 5.7, where the three-phase i_{Diff} are not noisy. It should be mentioned that N becomes 0 at 2.14 s for less than a cycle as $tr_{\text{N-B}}$ temporarily decreases below *thr2* at this time; nonetheless, S_{GIC} is not affected because of the dropout time of $t_{\text{set-2}}$ (3 cycles) in Figure 5.5.

In Figure 5.18, the WGD algorithm response is depicted during the transformer energization. In this figure, observe that except for the noise-caused variations in the *tr* values, there is no considerable difference between their behavior and that of *tr* values illustrated in Figure 5.14 associated with the no-noise condition. Thus, both P and N signals are not asserted, keeping S_{GIC} at 0 during the energization when the three-phase i_{Diff} are noisy. The results of this subsection prove that the WGD module of the waveform-based approach is immune to noise.

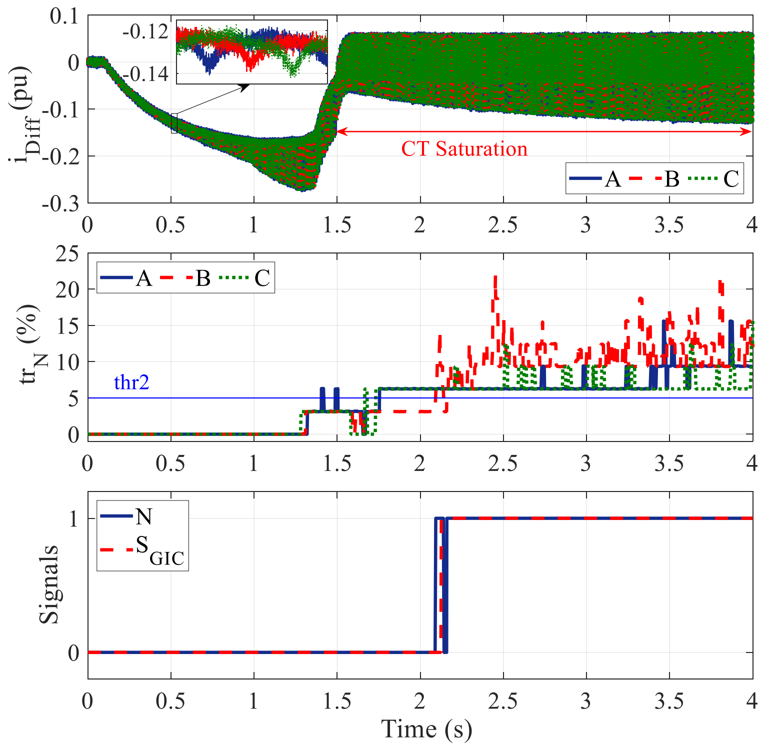

Figure 5.17. Performance of the waveform-based GIC detection algorithm for the noisy differential current waveforms under the GIC condition and CT saturation.

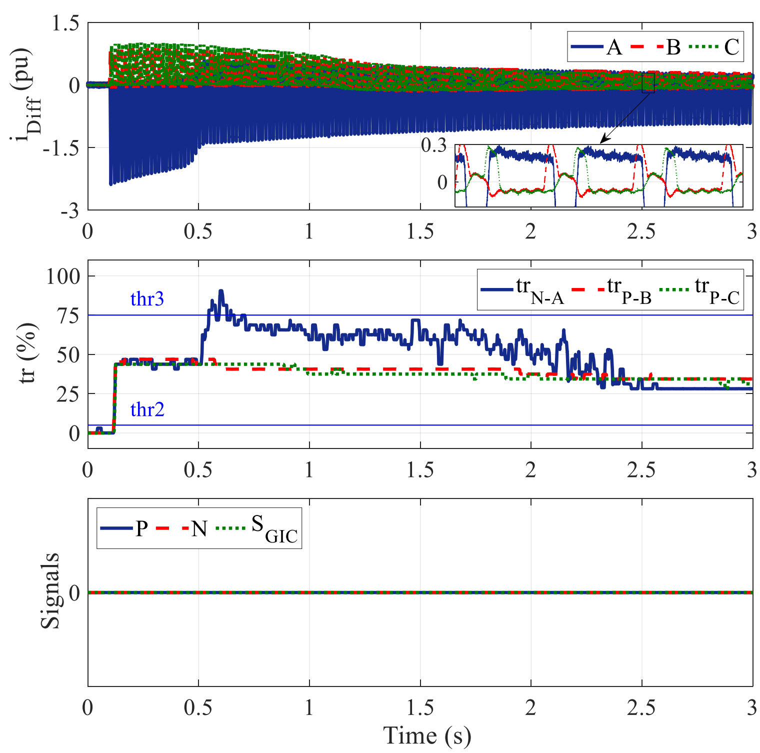

Figure 5.18. Performance of the waveform-based GIC detection algorithm for the noisy differential current waveforms during the transformer energization and CT saturation.

5.3.7 Single-Phase Transformer Units

Similar to Section 4.4, in order to verify that the effectiveness of the waveform-based approach is independent of the transformer type, the three-leg transformer in the system of Figure 3.1 is replaced with a transformer bank of three single-phase units. Figure 5.19 illustrates the relay performance for an internal single-phase fault (on phase A) during the GIC. The bolted fault is simulated on the LV side of the transformer bank at 10 s. In Figure 5.19, the three-phase i_{Diff} are asymmetric in the negative direction before the fault is applied, which leads to successful GIC detection. After the fault, the relay is unblocked and issues the trip signal since S_{UB} is asserted, causing $S_{\mathrm{MHB\text{-}ABC}}$ to become 0. It should be noted that without the proposed approach, the relay cannot trip for this fault as $S_{\mathrm{HB\text{-}ABC}}$ is maintained at 1 due to the GIC.

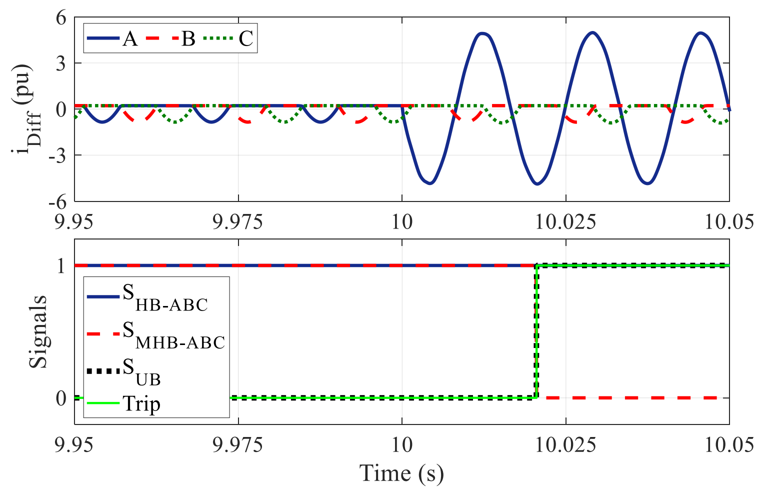

Figure 5.19. The proposed differential protection performance for the internal fault during the GIC when the transformer is modeled as three single-phase units.

5.3.8 Wye-Delta Transformer

In high-voltage transmission systems, the common practice is to ground the transformers on both HV and LV sides effectively. Nonetheless, in order to show the effectiveness of the WGD algorithm for different transformer winding connections/vector groups, the winding connection of the transformer is changed to delta on the LV side, leading to the vector group of YD1. Similar to the previous subsection, the transformer is modeled as the transformer bank of three single-phase units. Figure 5.20 shows the response of the WGD algorithm when the wye-delta transformer is subjected to the GIC with the steady-state magnitude of 200 A at the HV-side neutral.

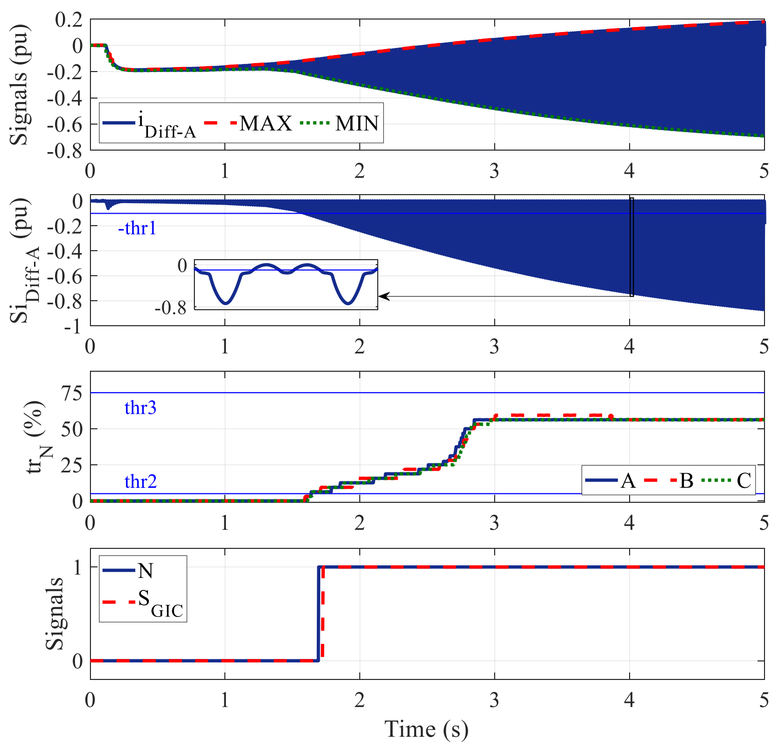

Figure 5.20. Performance of the waveform-based GIC detection algorithm under the GIC condition when the transformer is modeled as three single-phase units with a wye-delta connection.

In Figure 5.20, the initial offset in $i_{\text{Diff-A}}$ is due to the GIC, which is gradually removed by the CTs. The behavior is the same for $i_{\text{Diff-B}}$ and $i_{\text{Diff-C}}$. The $Si_{\text{Diff-A}}$ magnitude (also $Si_{\text{Diff-B}}$ and $Si_{\text{Diff-C}}$) goes below *–thr1* around 1.6 s, making the tr_{N} values depart from 0 and surpass *thr2* at 1.69 s, which sets N to 1 at this instant. Subsequently, the GIC flow in the wye-delta transformer is successfully detected around 1.73 s. It should be noted that in Figure 5.20, the increase in tr_{N} of the three phases around 2.7 s is due to the partial crossing of the LMPs of the Si_{Diff} waveforms from the threshold of –*thr1*. The Si_{Diff}'s uneven LMP stems from the LV-side delta connection and the associated phase angle compensation to obtain the differential current, as discussed in Section 2.1. The results are similar to Figure 5.20 if the CT saturation is also considered.

5.4 Summary

An alternative waveform-based unblocking approach was introduced in this chapter. The approach employs a GIC detection algorithm that identifies the GIC flow in the transformer based on the unfiltered instantaneous differential current waveforms. Additionally, it discriminates the internal faults from the external faults using the differential protection's pickup signals. The waveform-based approach's dependability and security were investigated during the GIC without and with the faults considering different transformer core topologies, inrush and sympathetic inrush currents, and different remnant fluxes during the energization. In addition, the performance of the WGD algorithm was analyzed for the noisy differential current waveforms and different transformer winding connections. The next chapter represents a hybrid unblocking scheme incorporating the capabilities of both harmonic- and waveform-based GIC detection algorithms and proposes an external fault detection logic to further improve the scheme security during external faults.

Chapter 6
Hybrid Unblocking Scheme

6.1 Introduction

To improve the GIC detection reliability and capability, compared to the individual harmonic- and waveform-based GIC detection algorithms introduced in the previous chapters, this chapter proposes a hybrid GIC detection approach consisting of harmonic- and waveform-based methods that detect the GIC utilizing the differential current second harmonic phasors and instantaneous differential current waveforms, respectively. In addition, a GIC detection algorithm is devised based on the average, maximum, and minimum values of the differential current waveforms to enhance the performance of the waveform-based part of the hybrid GIC detection method. The GIC detection capabilities of the proposed algorithms are investigated for different GIC magnitudes. Compared to the unblocking approach of Chapter 5, the unblocking scheme of this chapter also utilizes an external fault detection logic to enhance security for the external faults and CT saturation, especially during extreme GMDs leading to significantly high GICs.

6.2 Test System

The test system of Figure 6.1 is used for the offline simulations in this chapter and the real- tests, as described in Chapter 7. Compared to the system of Figure 3.1, a 50 km line connects the transformer's LV side to the 115 kV grid with an SCL of 20 kA. Both lines are modeled with their constant parameters, and the grids are modeled by their Thevenin equivalent circuits. The 115 kV

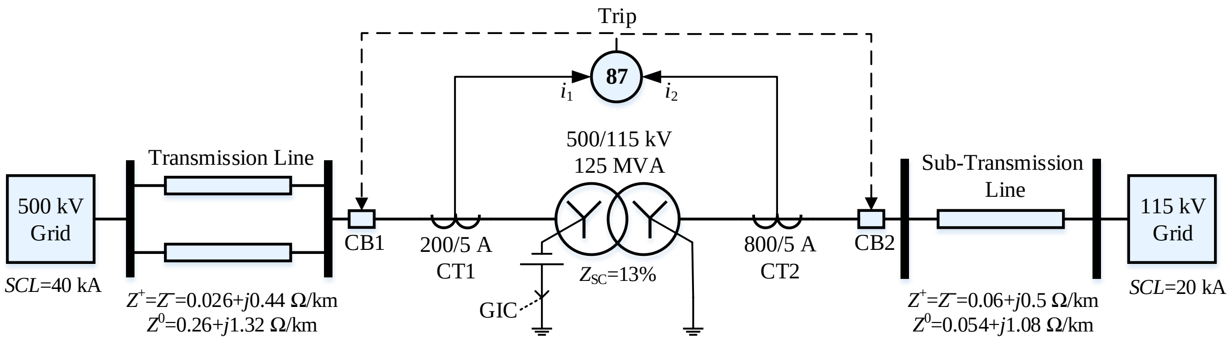

Figure 6.1. Single-line diagram of the test system.

grid in Figure 6.1 receives the power of 62.5 MVA at the unity power factor under normal conditions in the absence of GIC. A GIC magnitude of 200 A is considered in the majority of the studies and tests conducted in this chapter and Chapter 7, respectively. However, to create different GIC magnitudes at the transformer's HV-side neutral, the DC voltage source is accordingly adjusted.

In Figure 6.1, the C200 CTs have a burden of 0.5 Ω, and the differential relay calculates the restraint current (i.e., I_{rt}) using (2.4). Table 6.1 presents the relay settings in the studies of this chapter, which are based on the default settings of the commercial relay under test in Chapter 7.

TABLE 6.1. THE DIFFERENTIAL RELAY SETTINGS

I_{pkp}	0.1 (pu)
I_{bkp}	2 (pu)
s_1	25 (%)
s_2	90 (%)
t_{pkp}	0 (s)

6.3 Hybrid Approach

Figure 6.2 depicts the hybrid unblocking scheme employing both harmonic-based (Chapter 4) and waveform-based methods in the GIC detection module. The waveform-based GIC detection algorithm of Chapter 5 is retrofitted with an average-based algorithm that monitors 1-cycle average values of differential current waveforms alongside their maximum and minimum values to identify the GIC. As discussed in Section 5.2, the unblocking module utilizes the *PKP* signals to unblock the relay for the internal faults under the GIC conditions. Moreover, the RCC detection is to avoid possible unblocking by keeping S_{RCC} at 0 during the extreme GMDs, with the likelihood of S_{PKP} = 1 [39], in the absence of faults.

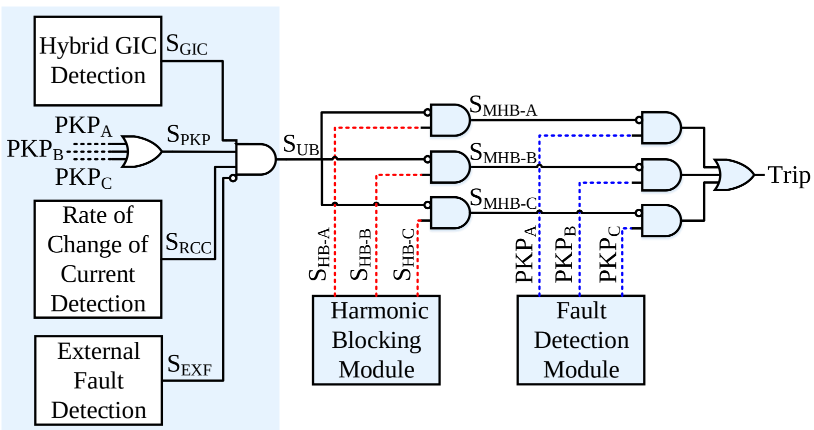

Figure 6.2. Transformer differential protection utilizing the hybrid unblocking scheme.

The unblocking scheme in Figure 6.2 also employs an RCC-based external fault detection logic to ensure that the relay remains blocked for external faults, specifically when S_{PKP} is asserted before the fault occurrence due to a considerably high GIC. Without the external fault detection in such conditions, the unblocking signal (i.e., S_{UB}) is wrongly set to 1 if S_{RCC} is asserted and S_{PKP} is still 1 after the external fault inception. The external fault detection module can prevent such malfunctions by setting S_{EXF} to 1 before the assertion of S_{RCC} during the external faults. Hence, based on the external fault detection's response time, the pickup time $t_{set\text{-}3}$ for the RCC detection (Figure 4.5) is set such that S_{RCC} is asserted after S_{EXF} is issued. Provided that S_{EXF} remains 0 during the internal faults under the GIC conditions, an S_{UB} = 1 is issued if $S_{GIC,}$ S_{PKP}, and S_{RCC} are all asserted.

It should be noted that since the majority of the modern differential relays [67, 68, 92, 93] employ external fault detection logics, such logics' outputs can be alternatively utilized as S_{EXF} in the proposed scheme of Figure 6.2.

6.3.1 Hybrid GIC Detection

Figure 6.3 depicts the logic of the hybrid GIC detection approach. In this figure, the output of the waveform-based method (S_{W}) is combined with the harmonic-based method's output, referred to as S_{H}, using an "OR" gate to improve the reliability of the GIC detection. The details of the harmonic-based method are already provided in Subsection 4.2.1. The waveform-based part consists of shift- and average-based algorithms. The GIC detection algorithm, introduced in Subsection 5.2.1, is referred to as the shift-based algorithm in this chapter.

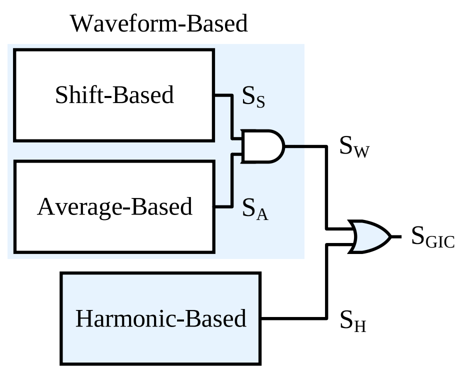

Figure 6.3. The logic of the hybrid GIC detection module of Figure 6.2.

The shift-based method may misidentify some severe external faults with the GIC and issue a false S_{S} (Figure 6.3) for the faults. When there is no GIC, Figure 6.4 illustrates the three-phase Si_{Diff} and the algorithm's output for a bolted single-phase fault on phase A that occurs on the bus between CB2 and the 115 kV line of the test system (Figure 6.1) at 0.1 s. In Figure 6.4, it is observed that the algorithm asserts S_{S} despite the symmetry of the three-phase Si_{Diff} during the fault. In this external fault scenario, the magnitudes of the three-phase Si_{Diff} are high enough to exceed the threshold (i.e., *thr1* = 0.1 pu) and low enough to be categorized by the shift-based method as asymmetrical waveforms (5.2).

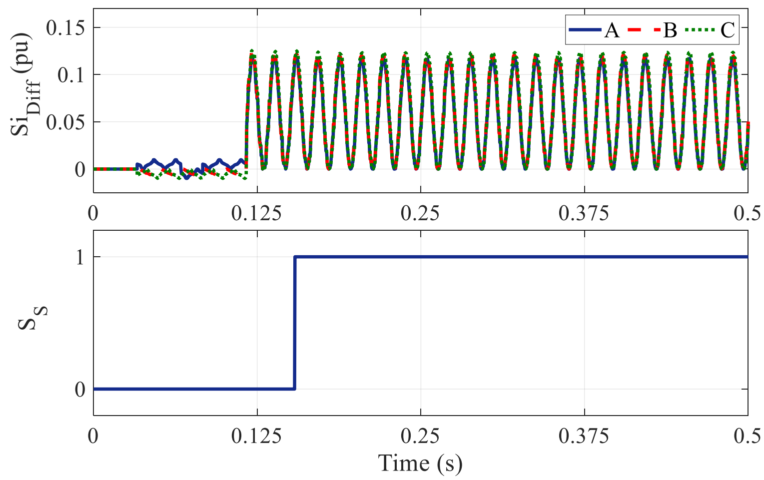

Figure 6.4. Performance of the shift-based algorithm for the external fault at 0.1 s in the absence of GIC.

6.3.2 Average-Based Algorithm

The previous subsection shows that the shift-based algorithm is prone to malfunction in the case of external faults in the absence of GIC. In order to address this issue and keep S_{W}, and subsequently, S_{GIC} at 0 for the external faults without GIC, an average-based algorithm (ABA) is proposed to supervise the shift-based method's output using an "AND" gate (Figure 6.3). Figure 6.5 depicts the logic of the proposed ABA. In this figure, the "AVG" function calculates the average value (*AVG*) of i_{Diff} over one cycle for each phase. The maximum (*MAX*) and minimum (*MIN*) values of i_{Diff} of each phase are tracked in each cycle by the "MAX & MIN" function. The *D* index in Figure 6.5 is calculated using (6.1) for each phase and is the difference between the *AVG* magnitude (i.e., |*AVG*|) of i_{Diff} and the average magnitude of the waveform's *MAX* and *MIN* values in each cycle. If *D* associated with i_{Diff} of one phase exceeds an adjustable threshold

$$D = \left| \left| AVG_{i_{Diff}} \right| - \frac{\left| MAX_{i_{Diff}} + MIN_{i_{Diff}} \right|}{2} \right| \tag{6.1}$$

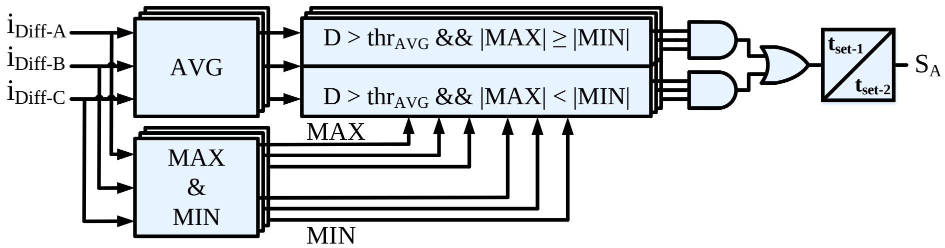

Figure 6.5. The logic of the average-based GIC detection algorithm of Figure 6.3.

(thr_{AVG}), the differential current waveform of that phase is considered to be asymmetric; otherwise, the waveform is symmetric. As an example, Figure 6.6 shows an asymmetrical i_{Diff} with its *AVG* and *D* index.

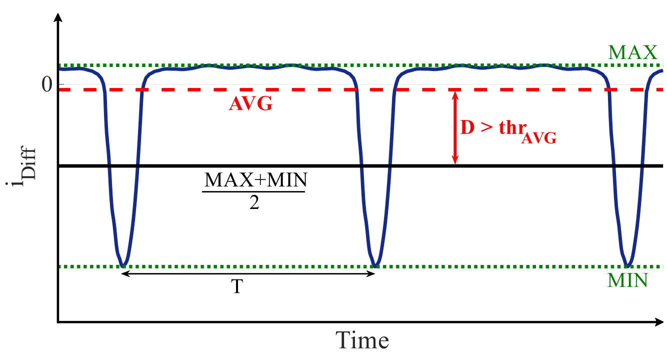

Figure 6.6. Example of an asymmetrical differential current waveform with the associated average value and *D* index.

According to Figure 6.5, if for the three phases, *D* exceeds thr_{AVG} and either the criterion $|MAX| \geq |MIN|$ or $|MAX| < |MIN|$ is met for more than a pickup time ($t_{\text{set-1}}$), S_{A} is asserted. It should be mentioned that $|MAX| \geq |MIN|$ denotes a positive direction of i_{Diff}, and vice versa. In Figure 6.5, thr_{AVG} is set at 0.01 pu that is determined based on several transformer core saturation conditions and fault scenarios conducted in the test system in order to differentiate asymmetrical waveforms from symmetrical ones. The pickup time of t_{set-1} is considered equal to 2 cycles to prevent spurious S_A in the case of transients. The dropout time t_{set-2} is to ensure that $S_A = 1$ remains available long enough after the fault for the relay unblocking during the GIC as i_{Diff} of a faulted phase tends to become symmetric and/or change its direction. In this study, t_{set-2} is set at 5 cycles.

Figure 6.7 shows the performance of the ABA for the same external fault as Figure 6.4. In this figure, i_{Diff} of phase A and its *AVG*, *MAX*, and *MIN* values are depicted. The signals are similar for phases B and C. As observed in Figure 6.7, after a few spikes during the fault, D remains well below thr_{AVG} since i_{Diff} is symmetric; thereby, S_A is not asserted. This keeps S_W in Figure 6.3 at 0 for the external fault despite $S_S = 1$, as illustrated in Figure 6.4. In Figure 6.7, although D exceeds thr_{AVG} for a fraction of a cycle, S_A is not affected owing to the considered 2-cycle pickup time. It should be noted that the $|AVG|$ value in (6.1) is zero in the long run, owing to the DC removal by the CTs. However, employing the $|AVG|$ value in (6.1) is essential for distinguishing between the asymmetrical waveforms from the symmetrical ones such as i_{Diff} in the external fault case shown in Figure 6.7. Otherwise, the D index would be large and exceeding the threshold of thr_{AVG} due to the temporary DC component of the waveform during the fault, resulting in unequal *MAX* and $|MIN|$ values.

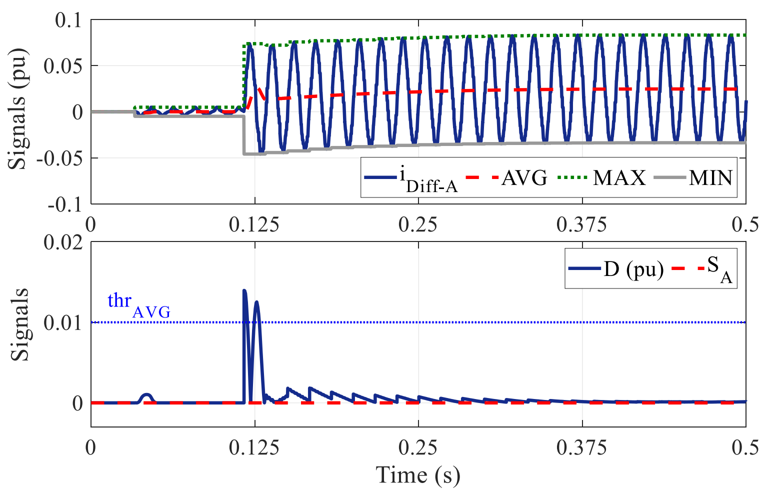

Figure 6.7. Performance of the average-based algorithm for the external fault at 0.1 s in the absence of GIC.

6.3.3 External Fault Detection

The logic of the proposed external fault detection for phase A is shown in Figure 6.8. The corresponding logics of phases B and C are similar. This logic is based on the principle that during an external fault, the restraint current (I_{rt}) changes more than the operation current (I_{op}) when the CT(s) is not saturated [67, 68]. In Figure 6.8, RCC_{rt} is the rate of change of restraint current calculated in the same way as *RCC*, which is the rate of change of operation current (Figure 4.5). For any phase, if RCC_{rt} is larger than *RCC* and the latter exceeds thr_{RCC}, *EXF* of that phase and S_{EXF} are asserted after an adjustable pickup time ($t_{\text{set-5}}$), declaring an external fault and preventing the assertion of S_{UB} (Figure 6.2).

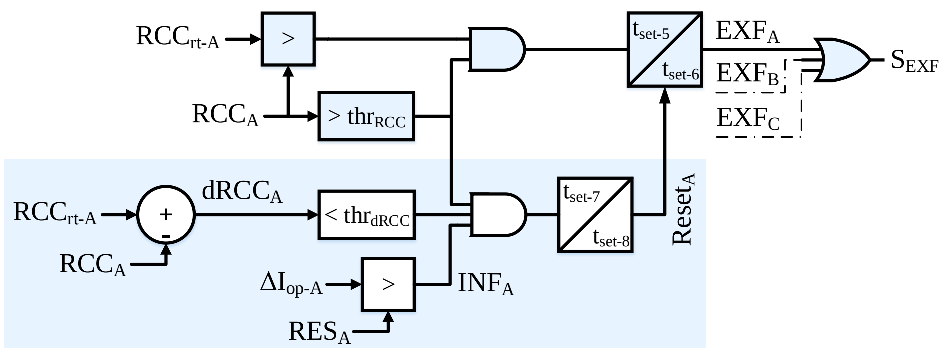

Figure 6.8. The logic of the external fault detection module of Figure 6.2.

Based on the analysis conducted in [30], the transient CT saturation persists for around a half cycle after the fault inception during the GIC. This indicates that *RCC* is likely to be high during the first half cycle due to the GIC-caused CT saturation, and therefore, RCC_{rt} can assertively surpass *RCC* in the second half cycle when the transient CT saturation is over. Accordingly, the developed logic is able to detect an external fault within one cycle after the fault occurrence during the GMDs. In the studies of this chapter, $t_{\text{set-5}}$ is set at 0.25 cycle to avoid spurious S_{EXF}, and the adjustable dropout time $t_{\text{set-6}}$ is considered to be 120 cycles (i.e., 2 s) to keep S_{EXF} asserted long enough after the external fault inception during the GMDs.

The proposed external fault detection logic also includes a reset logic, as shown in Figure 6.8. This logic is to ensure the relay unblocking for the low-current internal faults, especially during the extreme GMDs. In such conditions, the resulting RCC_{rt} is prone to exceed RCC by a small margin, which may unwantedly assert S_{EXF}. For each phase, the reset logic checks the following criteria to declare an internal fault and reset the *EXF* and S_{EXF} signals by overriding $t_{\text{set-6}}$: (i) the difference between RCC_{rt} and RCC, referred to as $dRCC$, is lower than an adjustable threshold (thr_{dRCC}), (ii) RCC is above thr_{RCC}, and (iii) ΔI_{op} exceeds RES (2.5), asserting *INF* in Figure 6.8. The variable ΔI_{op} is the change of differential current fundamental component in a time window with the duration of a few cycles, e.g., two cycles in this study. Instead of I_{op}, ΔI_{op} is employed in the operation-restraint characteristic since ΔI_{op} is small and remains below the pickup threshold (i.e., RES) in no-fault conditions, regardless of the GIC magnitude. The reset logic also facilitates the relay unblocking if an external fault evolves into an internal fault [67, 68, 92]. In the studies, thr_{dRCC} is considered 0.5 pu/s that is determined by conducting numerous simulations, including different fault currents and GIC magnitudes, on the test system of Figure 6.1 to achieve the desired performance during both internal and external faults. Furthermore, the time settings $t_{\text{set-7}}$ and $t_{\text{set-8}}$ are set at 0.5 cycle and 1 cycle, respectively, to confirm an internal fault condition and keep the *Reset* signal (Figure 6.8) asserted long enough for the relay unblocking.

6.4 Performance Evaluation

This section evaluates the response of the proposed scheme of Figure 6.2 to extensive scenarios based on time-domain simulations. The HB method is assumed to be the CBM with thr_{2nd} of 20%. The same pickup ($t_{\text{set-1}}$) and dropout ($t_{\text{set-2}}$) time settings as the ABA are considered for the shift-and harmonic-based algorithms. Moreover, the phase angle threshold of θ_{set} in (4.1) is set at 60° to prevent any possible false S_H (Figure 6.3) during the external faults in the absence of GIC, such as the fault example in subsection 6.3.1, without affecting the GIC detection capability level. In addition, thr_{RCC} is 2 pu/s (similar to Chapter 5), and $t_{set\text{-}3}$ is set at 1 cycle to ensure that S_{RCC} is asserted after S_{EXF} during the external faults, as discussed at the beginning of Section 6.3.

6.4.1 GIC without Faults

Figure 6.9 illustrates the three-phase I_{op} and signals of the proposed scheme of Figure 6.2 during the GIC initiated at 0.1 s. As observed in Figure 6.9, there is an increase in the I_{op} magnitudes after applying the GIC, while the differential relay is blocked by its HB module ($S_{HB\text{-}ABC} = 1$). Moreover, the proposed scheme does not unblock the relay ($S_{UB} = 0$), as S_{PKP} and S_{RCC} are not asserted during the GIC. Hence, $S_{MHB\text{-}ABC}$ is kept at 1, preventing any malfunction under the GIC conditions. According to Figure 6.9, the GIC condition is successfully detected by the hybrid GIC detection method of Figure 6.3 since S_{GIC} is set to 1 at 0.35 s, which is when S_H is asserted. The proposed ABA asserts S_A and identifies the GIC at 0.783 s; however, because of the "AND" gate in Figure 6.3, S_W is set to 1 at 1.12 s when the shift-based algorithm also detects the GIC flow ($S_S = 1$).

The signals of the average-based algorithm during the GIC are depicted in Figure 6.10. In this figure, around 1.2 s after applying the GIC at 0.1 s, $|AVG|$ of $i_{Diff\text{-}A}$ gradually decreases to zero as the waveform's DC-bias, caused by the GIC, is removed by the CTs. Due to the similarity, $i_{Diff\text{-}B}$ and $i_{Diff\text{-}C}$ and their AVG, MAX, and MIN values are not shown in Figure 6.10. According to this figure, the calculated D indices of the three phases are all above thr_{AVG} at 0.75 s owing to the waveform asymmetry. In this scenario, i_{Diff} of the three phases are in the negative direction ($|MAX| < |MIN|$); thus, S_A is asserted two cycles ($t_{set\text{-}1}$) after 0.75 s, as illustrated in Figure 6.9.

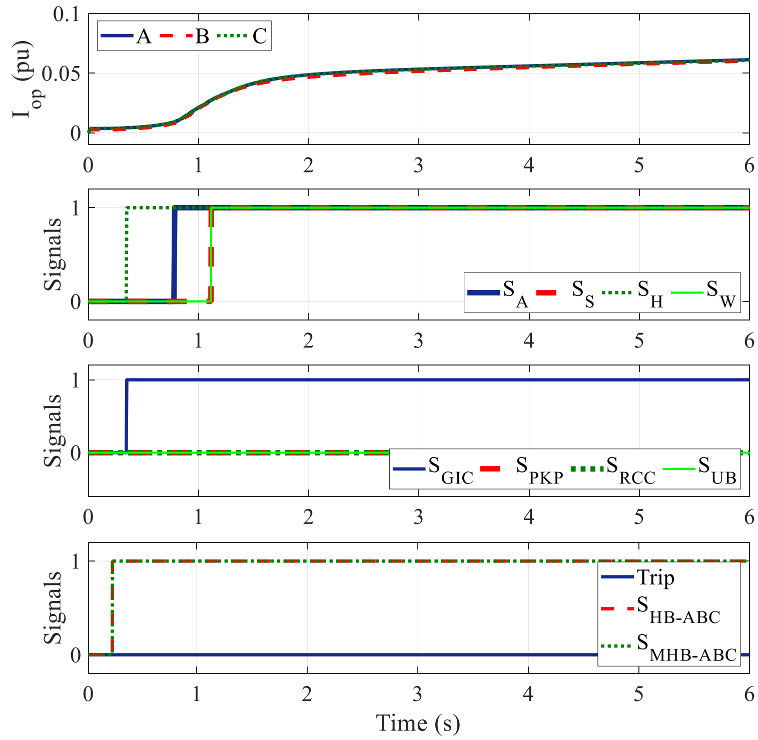

Figure 6.9. The three-phase I_{op} and signals of the proposed protection scheme during the GIC initiated at 0.1 s.

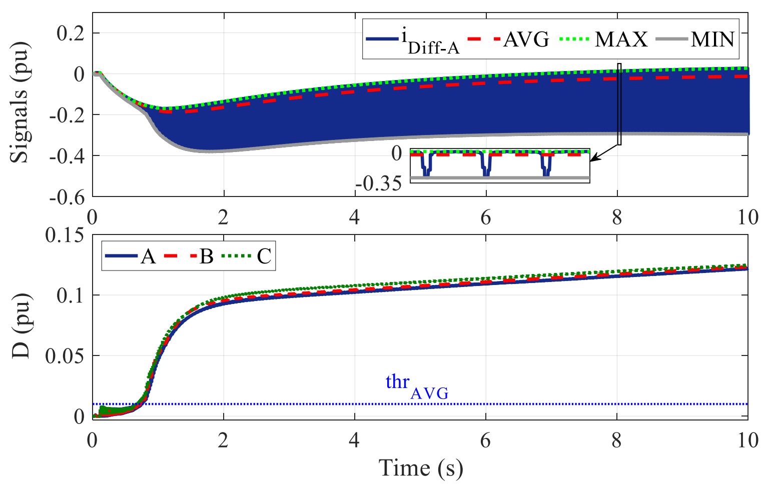

Figure 6.10. Performance of the average-based algorithm during the GIC initiated at 0.1 s.

Figure 6.11 illustrates the performance of the ABA under the GIC condition while CT1 in the test system is saturated at 1.5 s owing to the GIC flow in the transformer. As observed in this figure, the CT saturation causes $|AVG|$ of $i_{\text{Diff-A}}$ to quickly decrease to zero (the same behavior is observed for the *AVG* values of $i_{\text{Diff-B}}$ and $i_{\text{Diff-C}}$). Moreover, after the CT saturation, the *D* indices suddenly decrease, which indicates the lower asymmetry levels in the differential current waveforms, compared to Figure 6.10 with no CT saturation. Nonetheless, the *D* indices are still well above thr_{AVG} to identify the GIC flow during the CT saturation. It should be noted that the performance of the proposed protection scheme during the GIC in the absence of faults is not affected by the CT saturation and remains the same as the one shown in Figure 6.9.

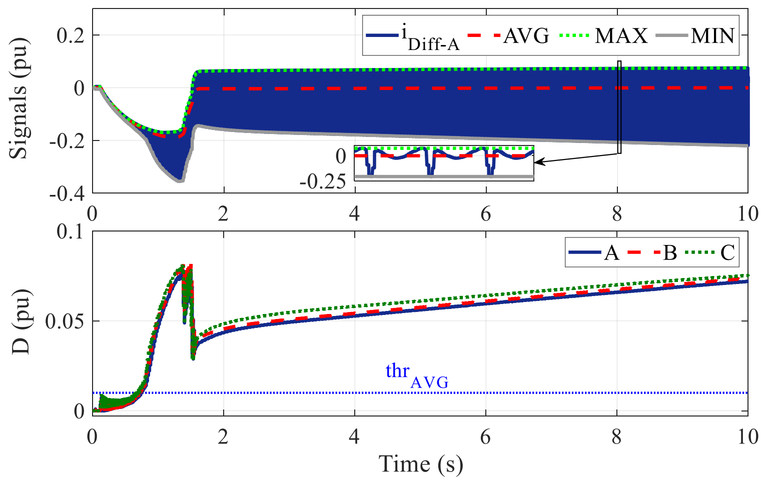

Figure 6.11. Performance of the average-based algorithm during the GIC initiated at 0.1 s and CT saturation at 1.5 s.

6.4.2 Comparison of GIC Detection Methods during GICs

In this subsection, the performance of the GIC detection algorithms employed in the hybrid method of Figure 6.3 is studied for different GIC magnitudes in order to compare their capabilities to identify the GIC conditions. The study results are summarized in Table 6.2. In this table, the minimum steady-state GIC magnitudes that can be detected by each algorithm are provided, considering the abovementioned settings for each algorithm. In Table 6.2, the proposed ABA is able to detect the GIC levels equal to or higher than 120 A at the transformer's neutral in the test system of Figure 6.1. As a result, it surpasses the shift-based algorithm with the minimum GIC detection capability of 150 A. However, combining the shift-based algorithm with the ABA using the "AND" gate in Figure 6.3 provides more GIC detection accuracy for the waveform-based part.

TABLE 6.2. GIC DETECTION CAPABILITY COMPARISON

Method	Minimum Detectable GIC (A)
Average-Based	120
Shift-Based	150
Harmonic-Based	60
Hybrid	60

According to Table 6.2, the harmonic-based algorithm can detect the GICs as low as 60 A, which is also the minimum detectable GIC of the hybrid method, considering the "OR" gate in Figure 6.3. The reason for the best GIC detection capability of the harmonic-based algorithm is that the negative-sequence relationship (Subsection 4.2.1) among the differential current second harmonic phasors can be formed at very low GIC magnitudes. Nevertheless, in terms of reliability, the hybrid GIC detection is superior to the individual harmonic-based or waveform-based method since it does not rely solely on the second harmonic phasors or the differential current waveforms to identify the GIC. Due to the three-leg core construction of the transformer in the test system, the core is not saturated with the neutral GIC of lower than 60 A, and thus, an unwanted relay blocking during the internal faults is unlikely in such GIC conditions because of low I_{2nd}-to-I_{op} ratio(s).

6.4.3 Internal Faults during GIC

Figure 6.12 shows the proposed scheme signals for an internal phase A to ground fault with R_F of 90 Ω (I_{op} = 0.57 pu). The fault is simulated on the transformer's LV side (Figure 6.1) at 10 s when the GIC is at the steady-state magnitude of 200 A. In this figure, observe that all the signals of the hybrid GIC detection are asserted during the GIC before the fault occurrence. Around 5.5 cycles after the fault occurs on phase A, S_A is set to 0 since i_{Diff-A} becomes symmetric and changes its direction from negative to positive, which leads to $S_W = 0$ at 10.09 s, despite $S_S = 1$. Nevertheless, S_{GIC} remains asserted because S_H is equal to 1. It can be seen in Figure 6.12 that S_{UB} is asserted at 10.02 s when S_{GIC}, S_{PKP}, and S_{RCC} are all equal to 1; consequently, the relay is unblocked as $S_{MHB-ABC}$ is set to 0 and issues the trip signal for the fault during the GIC, in spite of $S_{HB-ABC} = 1$.

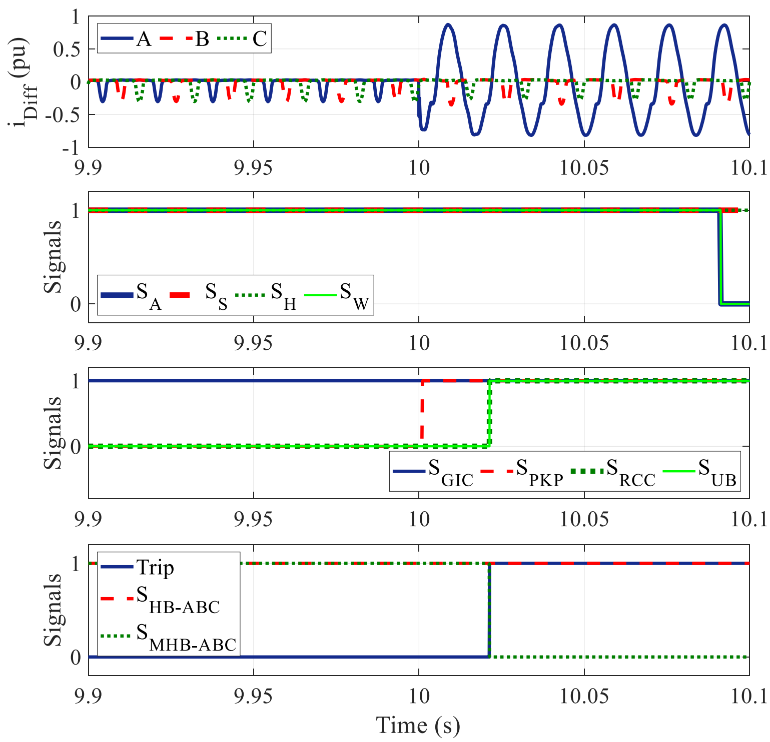

Figure 6.12. The signals of the proposed protection scheme for the internal fault at 10 s during the GIC.

The signals of the external fault detection logic for the faulted phase A are depicted in Figure 6.13. In this figure, observe that *RCC* is above RCC_{rt} during the internal fault; therefore, *dRCC* is negative (Figure 6.8), and S_{EXF} is not asserted, as expected. On the other hand, ΔI_{op} is almost 0 before the fault occurrence despite the GIC existence, and it exceeds *RES* during the fault, setting *INF* to 1. Since *RCC* and *dRCC* are above 2 pu/s and below 0.5 pu/s, respectively, while *INF* is asserted, *Reset* is issued at 10.015 s for the studied internal fault. The results are similar to Figures 6.12 and 6.13 during the CT saturation.

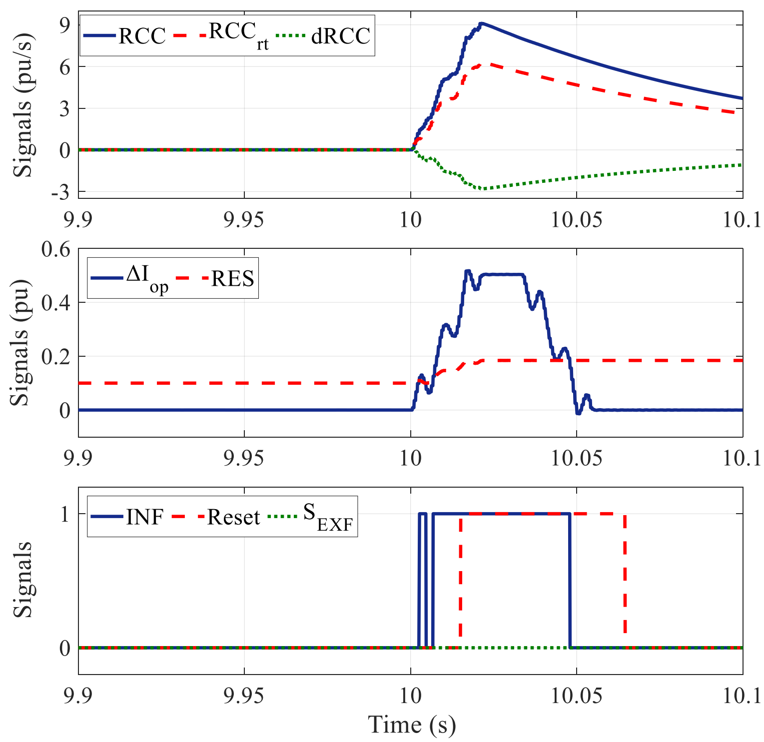

Figure 6.13. The phase A signals of the external fault detection logic for the internal fault at 10 s during the GIC.

6.4.4 External Faults during GIC

The response of the proposed scheme is analyzed for a phase A bolted external fault at 10 s on the transformer's LV side in the GIC existence. The results are depicted in Figure 6.14, where it is observed that both S_{PKP} and S_{RCC} are not asserted for the fault, keeping S_{UB} at 0. Thereby, the relay is kept blocked ($S_{MHB\text{-}ABC} = 1$) and does not malfunction during the fault and GIC. In Figure 6.14, the symmetry and change in the direction of $i_{Diff\text{-}A}$ during the fault lead to setting S_A, and subsequently, S_W to 0 (similar to Figure 6.12). Furthermore, S_{EXF} is not asserted in this case study since the three-phase *RCCs* remain below the threshold of thr_{RCC} ($S_{RCC} = 0$). Regarding the hybrid unblocking scheme of Figure 6.2, this does not lead to any security issue; nonetheless, a smaller threshold (thr_{RCC}) can be exclusively selected for the external fault detection logic to enable the logic for lower *RCCs*, if required.

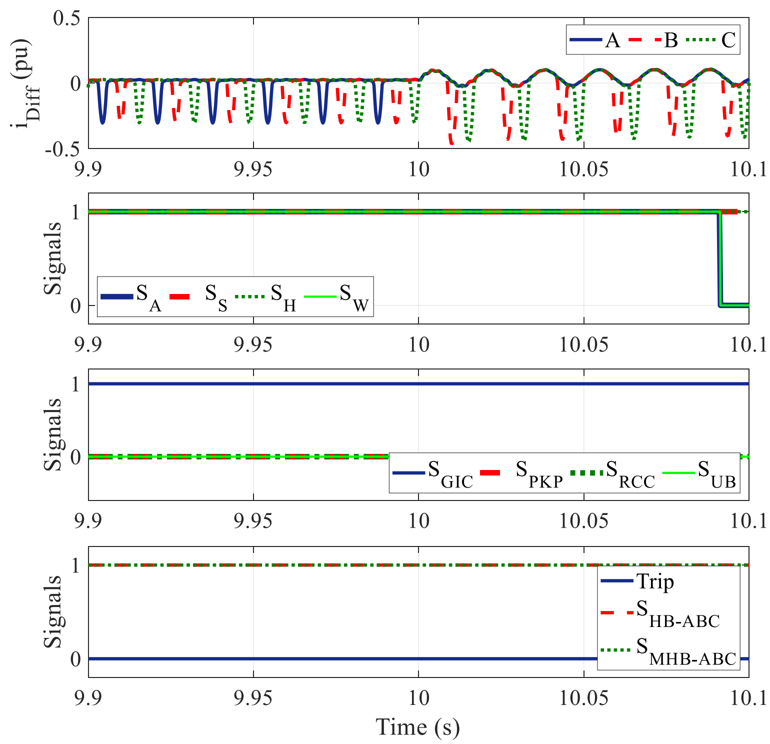

Figure 6.14. The signals of the proposed protection scheme for the external fault at 10 s during the GIC.

The scheme performance is also examined for the external faults on the LV and HV sides of the transformer during the GIC and CT saturation. The studies are conducted for different fault angles, including 0°, -90°, and +90° associated with the peak, upward zero-crossing, and downward zero-crossing points on the phase A voltage waveform, respectively. Figure 6.15 shows the scheme behavior for an LV-side fault on phase A with the inception angle of 0° during the CT saturation caused by the GIC. The fault angle of 0° is equivalent to the fault instant of 10 s. The performance for other fault angles and HV-side faults remains similar to Figure 6.15.

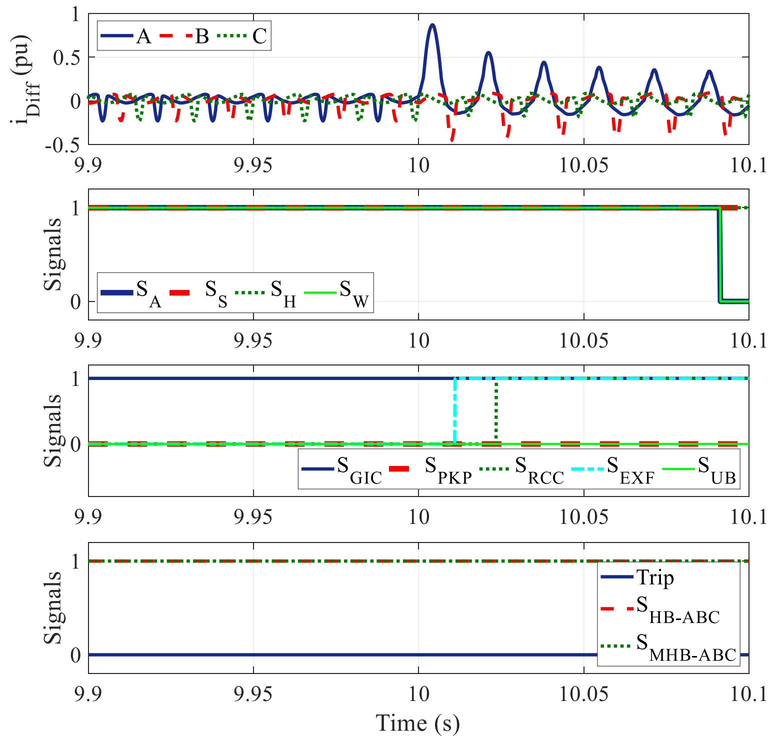

Figure 6.15. The signals of the proposed protection scheme for the external fault at 10 s during the GIC and CT saturation.

In Figure 6.15, observe that the i_{Diff} magnitude of the faulted phase A is higher compared to i_{Diff-A} in Figure 6.14, due to the CT saturation. However, the differential relay does not pick up (S_{PKP} = 0) since the relay is restrained during the external fault, based on the relay's operation-restraint characteristic. Unlike the case shown in Figure 6.14, the CT saturation in this scenario leads to setting S_{RCC} to 1 at 10.023 s. Nevertheless, the relay remains blocked during the external fault and CT saturation as S_{PKP} is not asserted, and further, S_{EXF} is issued by the external fault detection logic at 10.011 s. Figure 6.16 depicts the logic signals of phase A for the studied fault scenario. The *INF* and *Reset* signals are not shown in this figure since they are not asserted for the external fault, as expected. In Figure 6.16, RCC_{rt} exceeds *RCC* after the external fault inception, which results in a significant, positive *dRCC*. Subsequently, the external fault is detected, and S_{EXF} (Figure 6.15) is asserted at 10.011 s that is 0.25 cycle (t_{set-5}) after *RCC* surpasses 2 pu/s.

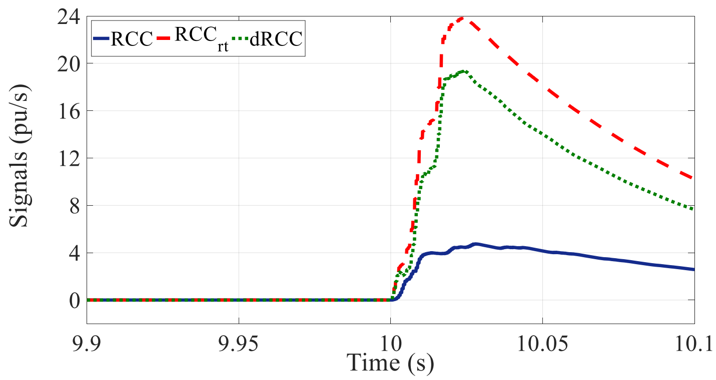

Figure 6.16. The phase A signals of the external fault detection logic for the external fault at 10 s during the GIC and CT saturation.

6.4.5 Inrush Currents

The behavior of the proposed scheme is examined for the inrush currents, and the results are shown in Figure 6.17. The ABA's output (i.e., S_A) as well as S_S and S_H securely remain 0 during the transformer energization initiated at 0.1 s; therefore, S_{GIC} is not asserted for the inrush currents, revealing that the hybrid GIC detection approach can discriminate the GIC from the inrush currents. In this scenario, S_{PKP} and S_{RCC} are set to 1; nonetheless, S_{UB} is not asserted owing to S_{GIC} of 0. Therefore, no trip is issued for the inrush currents since $S_{MHB\text{-}ABC}$ is 1 and the relay is blocked. It should be noted that the external fault detection performance does not affect the results associated with the inrush currents since S_{GIC} is 0 in such conditions, and thereby, S_{UB} is not asserted, regardless of S_{EXF}. Figure 6.18 shows the ABA response to the inrush currents. It is observed that during the transformer energization, the D indices of the three phases are above thr_{AVG} of 0.01 pu because of the asymmetrical differential current waveforms. However, $i_{Diff\text{-}A}$ is in the negative direction ($|MAX| < |MIN|$), while $i_{Diff\text{-}B}$ and $i_{Diff\text{-}C}$ are in the positive direction ($|MAX| > |MIN|$). As a result, considering Figure 6.5, the criteria to issue $S_A = 1$ are not met, and S_A is not asserted for the inrush currents. According to this analysis, the ABA is capable of discriminating between the GIC and inrush currents.

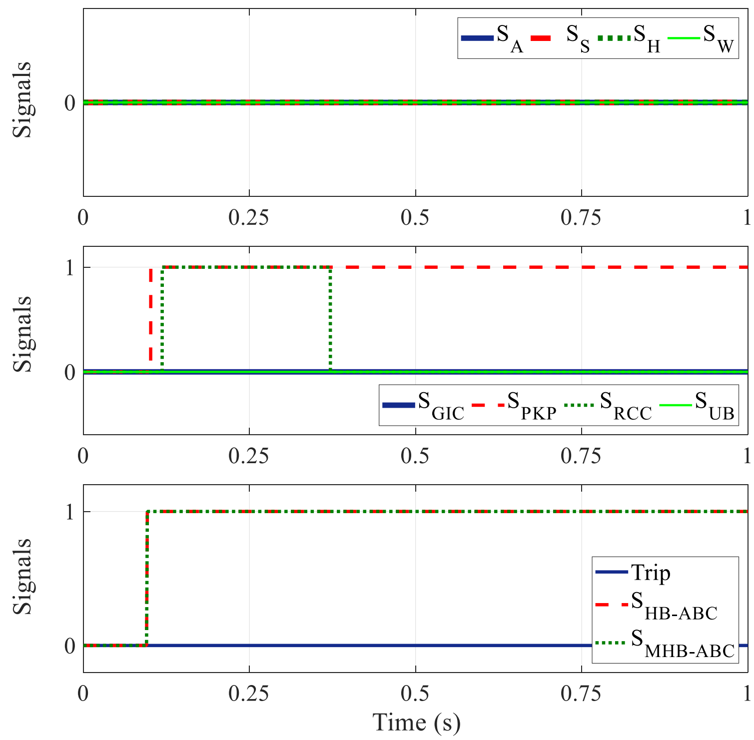

Figure 6.17. The signals of the proposed protection scheme during the transformer energization.

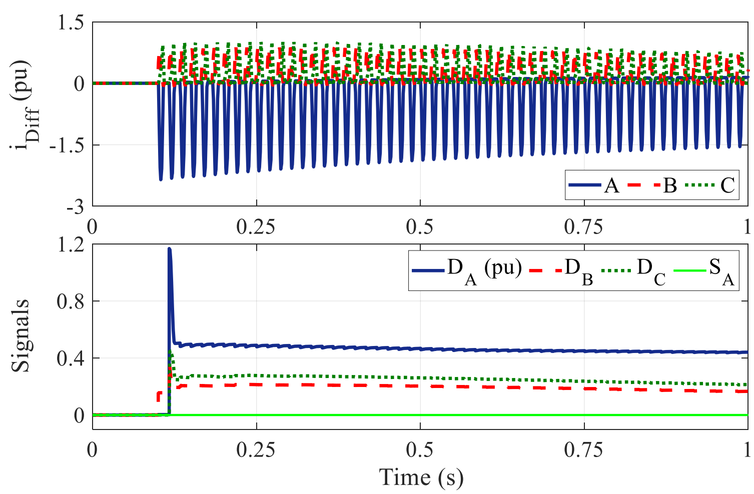

Figure 6.18. Performance of the average-based algorithm during the transformer energization.

In order to show that the performance of the hybrid GIC detection module of Figure 6.3 is not affected by the transformer switching angle, the three-phase i_{Diff} and θ_{I2ndp} during the inrush currents, associated with different switching angles of -90°, 0°, and +90°, are illustrated in Figures

6.19(a) to (c), respectively. The switching angle of -90° is equivalent to the energization instant of 0.1 s, as studied above. As observed in Figure 6.19, regardless of the transformer switching angle, i_{Diff} of one phase has an opposite direction than the other phases, and hence, S_{A} and S_{S} in Figure 6.3 are not asserted. Considering that the three-phase θ_{I2ndp} in Figure 6.19 represent a positive-sequence order (ABC) for the studied switching angles, S_{H} is kept at 0 (Subsection 4.2.1). Therefore, the hybrid GIC detection module does not assert S_{GIC} under different transformer switching angle conditions.

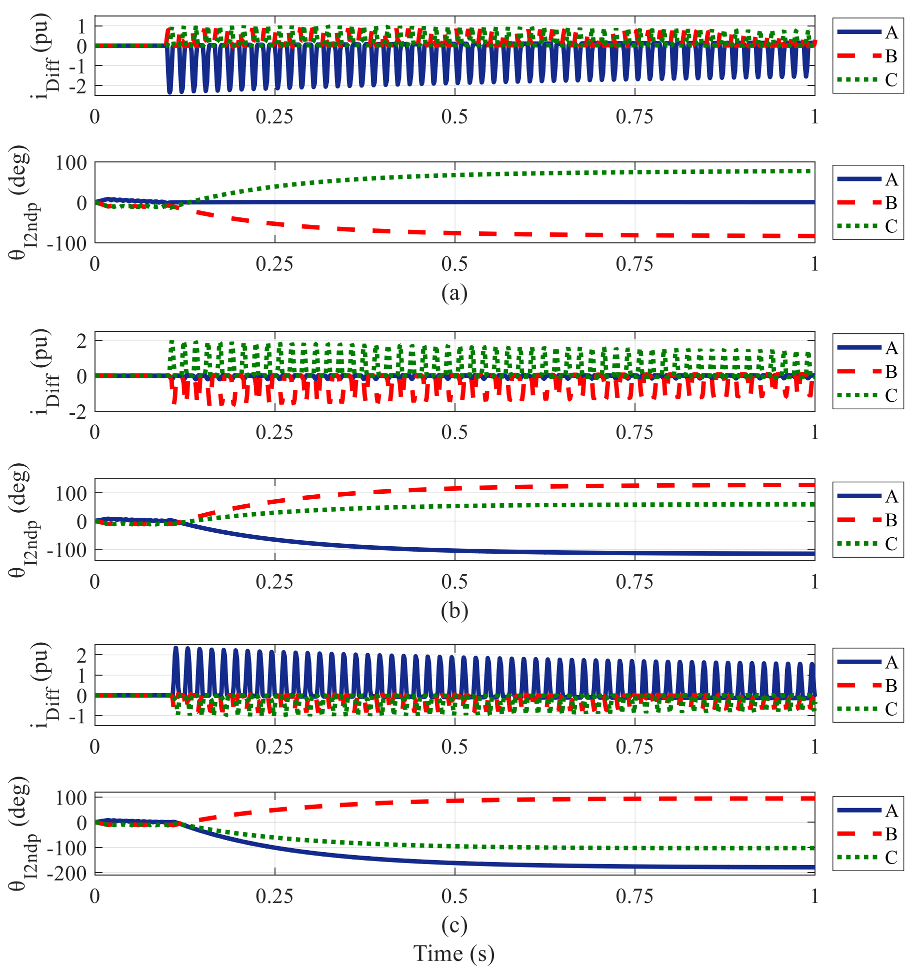

Figure 6.19. The three-phase i_{Diff} and θ_{I2ndp} during the transformer energization: (a) the switching angle of -90°, (b) the switching angle of 0°, and (c) the switching angle of +90°.

Figure 6.20 depicts the performance of the proposed scheme for the transformer energization at 0.1 s, where the CT1 of phase A is saturated around 0.5 s and those of phases B and C are saturated around 1.2 s. In this figure, observe that neither of the waveform-based (including the ABA) and the harmonic-based GIC detection algorithms asserts during the energization, regardless of the CT saturation, and hence, S_{GIC} and S_{UB} remain 0.

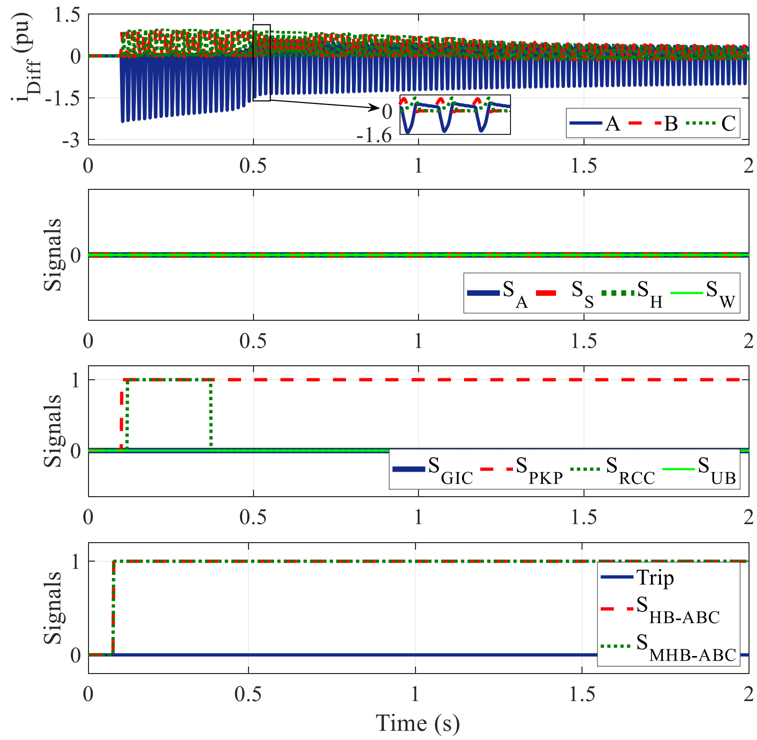

Figure 6.20. The signals of the proposed protection scheme during the transformer energization and CT saturation.

6.4.6 Inrush Currents during GMD

The performance of the proposed protection scheme is scrutinized for the inrush currents with the pre-existing GMD condition. In this case, the GIC starts flowing in the transformer once CB1 is closed at 0.1 s while CB2 is open (Figure 6.1). The results are depicted in Figures 6.21 and 6.22.

In Figure 6.21, CT1 of phase A is saturated around 0.4 s, reasserting S_{RCC}, as observed in Figure 6.22.

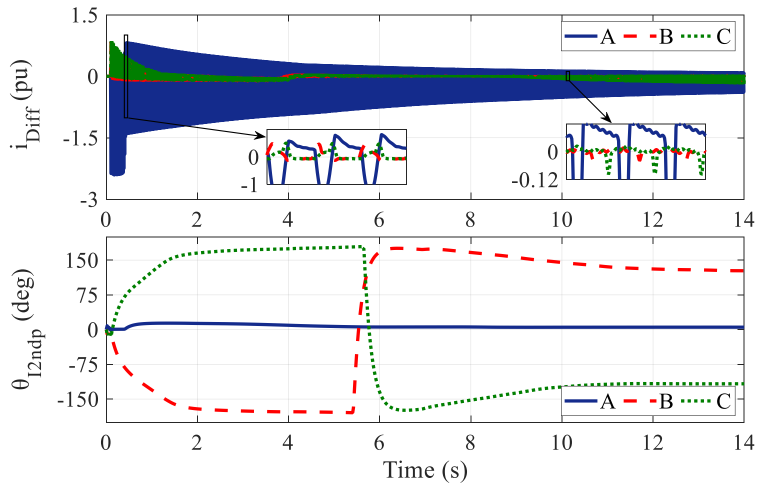

Figure 6.21. The three-phase i_{Diff} and θ_{I2ndp} for the inrush currents during the GMD and CT saturation.

However, since S_{GIC} in Figure 6.22 is not asserted while S_{RCC} = 1, S_{UB} remains 0, which keeps the relay blocked and avoids any malfunction during the simultaneous occurrence of the inrush currents and GIC. In Figure 6.22, the proposed ABA and shift-based method temporarily assert S_A and S_S, respectively, owing to the GIC flow in the transformer. Nevertheless, for the simultaneous occurrence of the energization and GIC, (i) it takes time for the energization signature to disappear from the differential currents, and (ii) it also takes time for the GIC signature to fully appear in the three-phase i_{Diff} and θ_{I2ndp} (as seen in Figure 6.21), based on which the hybrid GIC detection identifies the GIC. In this case study, S_A, S_S, and S_H are continuously set to 1 at 10.14 s, 12.21 s, and 5.84 s, respectively, and hence, the GIC condition is assertively detected at 5.84 s (S_{GIC} = 1). The results of this subsection prove that the proposed scheme maloperation is unlikely for the inrush currents during the pre-existing GMDs.

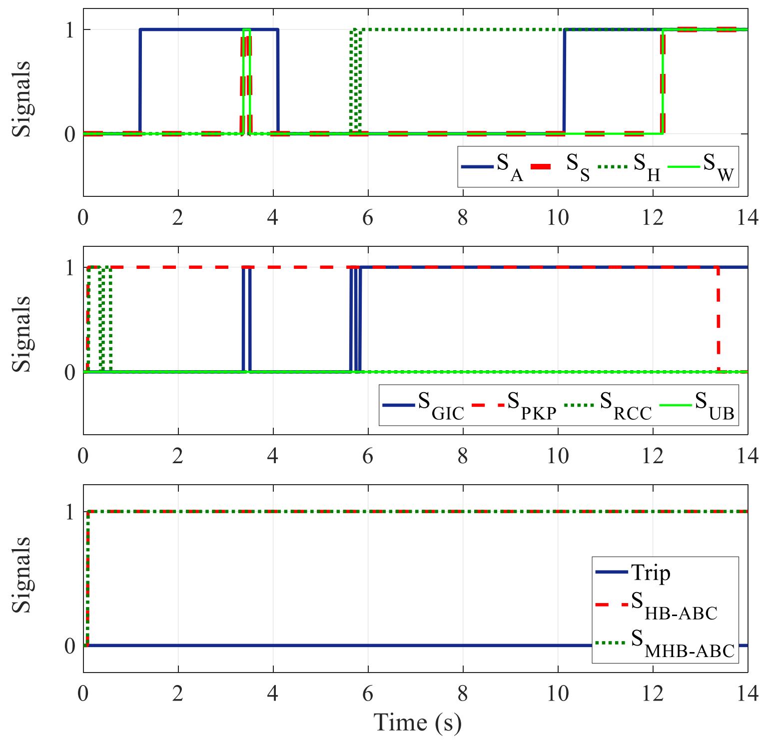

Figure 6.22. The signals of the proposed protection scheme for the inrush currents during the GMD and CT saturation.

6.4.7 External Fault during Extreme GMD

In Subsection 6.4.4, the scheme performance is analyzed for the external faults during the observed high neutral GIC of 200 A [79]. This subsection demonstrates the scheme response to a phase A to ground LV-side external fault at 10 s during an extreme GMD, generating a GIC magnitude of 400 A. Figure 6.23 presents the results, where the GIC leads to an I_{op} of 0.18 pu, asserting S_{PKP} before the fault initiation. In this figure, one can observe that the i_{Diff} magnitudes in the pre-fault period are significantly larger than the corresponding currents shown in Figure 6.15 associated with the GIC of 200 A. After the fault occurrence in this case study, although the *PKP* of the faulted phase A is set to 0, the *PKP* of the healthy phase B remains 1 because of the severe GIC magnitude of 400 A. However, the relay remains blocked (S_{UB} = 0 and $S_{MHB-ABC}$ = 1) since S_{EXF} is asserted at 10.013 s before S_{RCC} is set to 1 at 10.02 s, as illustrated in Figure 6.23. The external fault detection logic signals are depicted in Figure 6.24. In this figure, observe that RCC_{rt} is temporarily below RCC ($dRCC$ < 0) within the first half cycle, and shortly thereafter, it exceeds RCC, leading to the external fault detection after the pickup time ($t_{set\text{-}5}$) is passed.

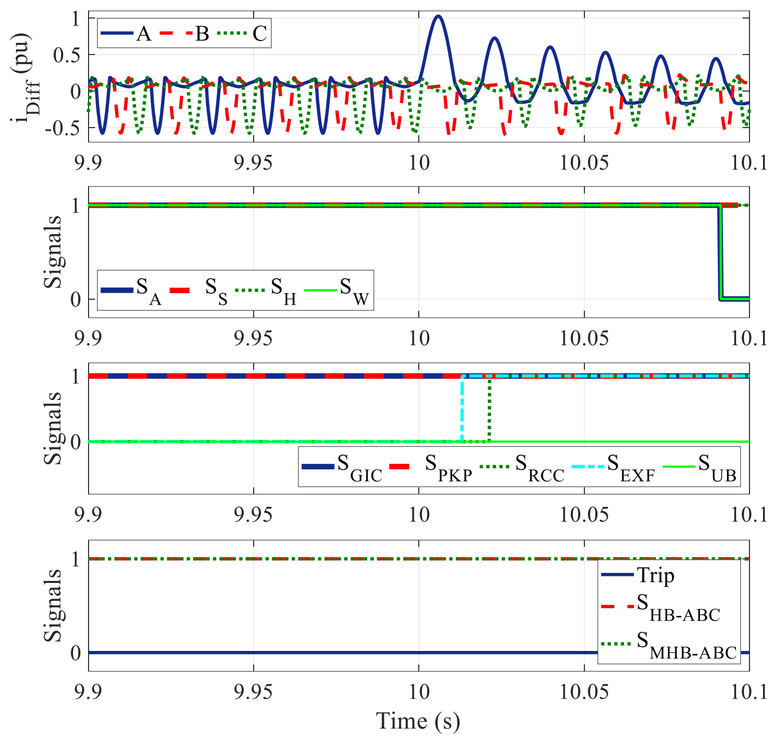

Figure 6.23. The signals of the proposed protection scheme for the external fault at 10 s during the extreme GMD and CT saturation.

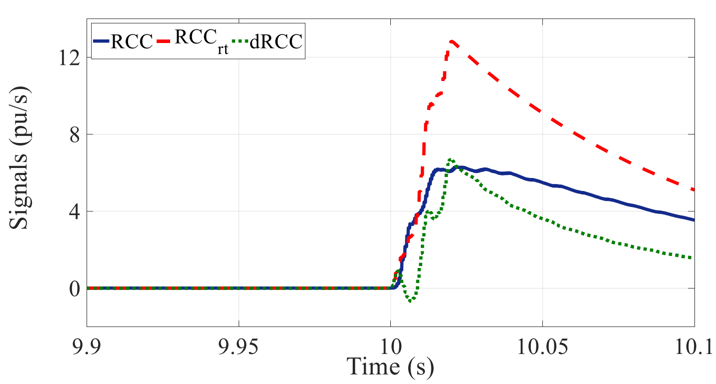

Figure 6.24. The phase A signals of the external fault detection logic for the external fault at 10 s during the extreme GMD and CT saturation.

6.5 Summary

In this Chapter, a hybrid unblocking scheme based on both harmonic- and waveform-based GIC detection methods was introduced. An average-based GIC detection algorithm was developed to enhance the accuracy of the waveform-based part. The performance of the GIC detection algorithms proposed in this research was compared for different GIC magnitudes. Moreover, an external fault detection logic was introduced to enhance the security of the unblocking scheme during the external faults and CT saturation, even under severe GIC magnitudes. The effectiveness of the differential relay equipped with the hybrid unblocking scheme was examined in numerous GIC- and non-GIC-based case studies. Chapter 7 represents the real-time validation test results including a real-world differential relay response to the in-zone faults occurring during the GIC and the real-time performance of the hybrid unblocking scheme for the internal faults in the presence of GIC.

Chapter 7
Real-Time Validation Tests

7.1 Introduction

In this chapter, first, the performance of an advanced commercial transformer differential relay is tested in real time during the GIC, without and with the CT saturation. Both terminal and turn faults as well as different HB logics and thresholds are included in the tests. Afterward, the effectiveness of the protection scheme of Chapter 6 is validated in real time. It is shown that the relay employing the unblocking module can successfully operate during the internal faults for which the commercial relay fails to trip due to unwanted harmonic blocking during the GIC.

7.2 HIL Setup and Test Procedure

Figure 7.1 illustrates the HIL setup for the differential protection testing. In this setup, the simulated secondary currents of CT1 and CT2 in the test system of Section 6.2 are sent to the commercial differential relay in real time using the RTDS. The relay response to each fault scenario is recorded for detailed analysis using the SynchroWAVe Event software [96].

The hybrid unblocking scheme introduced in Chapter 6 is implemented in RSCAD, which is the RTDS's interface, for the real-time performance validation of the relay equipped with the unblocking scheme during the internal faults under the GIC conditions. In this regard, the relay recorded signals (as COMTRADE files), including the HV- and LV-side CT currents, *PKP*, and

S_{HB} signals, are played back to the implemented protection scheme using the RTDS to monitor the scheme behavior for different in-zone faults during the GIC.

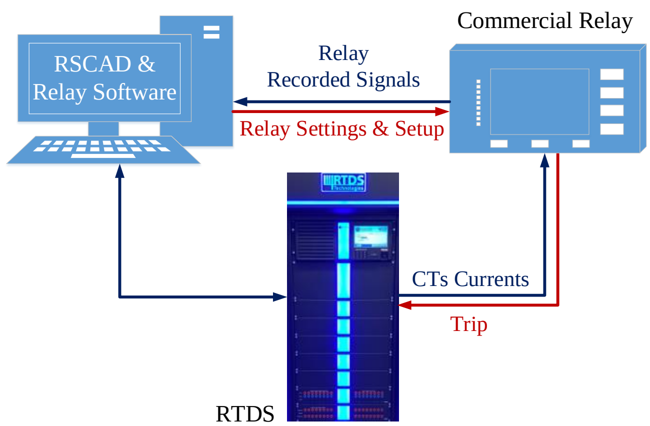

Figure 7.1. HIL setup for the transformer differential protection tests.

7.3 HIL Testing of Commercial Relay

In this section, the performance of the real-world differential relay in extensive internal fault scenarios under the GIC condition is tested and analyzed. The CBM (Figure 2.4) and PBM (Figure 2.6) logics associated with the second harmonic blocking are considered in the tests. The relay performance is evaluated for the typical thr_{2nd} values of 20% and 15%. The settings of the relay under test are provided in Table 6.1 in the previous chapter.

7.3.1 Terminal Faults

In this subsection, the commercial relay behavior is tested for the internal terminal faults during the GIC using the HIL setup of Figure 7.1. The phase A to ground faults are applied on the LV and HV sides of the transformer when the GIC is equal to the steady-state value of 200 A. The resistances of the LV- and HV-side faults (i.e., R_F) are increased by the steps of 10 Ω and 100 Ω, respectively, and the relay response to each fault scenario is recorded. The test results are summarized in Table 7.1, providing the fault resistance and I_{op} ranges in which the relay fails to operate or remains blocked during the GIC. The I_{op} values in Table 7.1 are related to the faulted phase A.

TABLE 7.1. THE OPERATION CURRENT AND FAULT RESISTANCE FAILURE RANGES OF THE COMMERCIAL RELAY

LV-Side Faults			
Logic	thr_{2nd}	I_{op}	R_F
CBM	20%	≤ 0.61 pu	≥ 80 Ω
	15%	≤ 1.01 pu	≥ 50 Ω
PBM	20%	≤ 0.33 pu	≥ 160 Ω
	15%	≤ 0.44 pu	≥ 120 Ω
HV-Side Faults			
Logic	thr_{2nd}	I_{op}	R_F
CBM	20%	≤ 0.75 pu	≥ 1300 Ω
	15%	≤ 0.98 pu	≥ 1000 Ω
PBM	20%	≤ 0.32 pu	≥ 3100 Ω
	15%	≤ 0.47 pu	≥ 2100 Ω

As a case in Table 7.1, one can observe that with the CBM and thr_{2nd} of 20%, the relay does not operate for the LV-side faults with R_F equal to and larger than 80 Ω that correspond to I_{op} of 0.61 pu and lower. Figure 7.2 illustrates the relay recorded signals for the fault with the resistance of 80 Ω during the GIC. In this figure, I_1 and I_2 are the secondary currents of CTs in amp (A) on the HV and LV sides, respectively. The three-phase *PKP* denote the relay's pickup signals, and the three-phase S_{HB} are the outputs of the relay's HB module. In Figure 7.2, the reference time is the fault occurrence instant, and the dashed red line shows the instant at which the relay's event recorder is triggered by *PKP* of phase A. In this figure, observe that the currents of the CTs are distorted because of the transformer core saturation caused by the GIC, and the three-phase S_{HB} are asserted before the fault occurrence owing to the significant differential current second harmonics. The relay picks up around 7 ms after the fault inception; however, S_{HB} of the three phases are asserted due to the GIC, which prevents the relay from issuing the trip signal, as seen in Figure 7.2. As a result, the fault remains uninterrupted during the GIC.

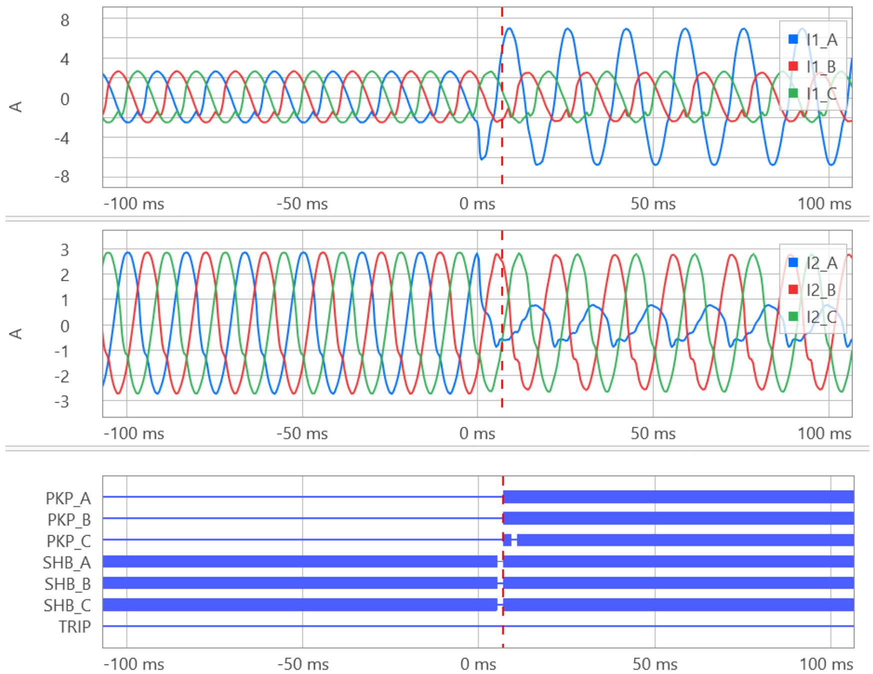

Figure 7.2. The relay recorded signals for the fault with R_F of 80 Ω on phase A during the GIC. The logic is the CBM and thr_{2nd} is 20%.

Figure 7.3 depicts the operation currents (I_{op}), restraint currents (I_{rt}), and I_{2nd}-to-I_{op} ratios, referred to as second harmonic ratios (*SHR*), of the three phases before and after the fault occurrence under the GIC condition. It is observed that during the fault, *SHR* of the faulted phase A is below thr_{2nd} of 20%; nonetheless, the relay is blocked for the three phases (Figure 7.2) as *SHR* of the healthy phases B and C do not decrease below the HB threshold during the fault in the presence of GIC. Compared to the studies of Chapter 3, the CBM-based relay under test does not remain blocked for the bolted faults because of the relay's zero-sequence removal function, as discussed in Section 3.1. Considering Figure 7.3, the zero-sequence removal leads to an increase in I_{op} of the healthy phases B and C during the phase A to ground fault, which decreases the likelihood of the relay blocking for significantly high fault currents under the GIC condition.

Based on Table 7.1, the relay with the PBM also fails to operate for specific ranges of fault resistances under the GIC condition, although it outperforms the CBM-based relay. As an example,

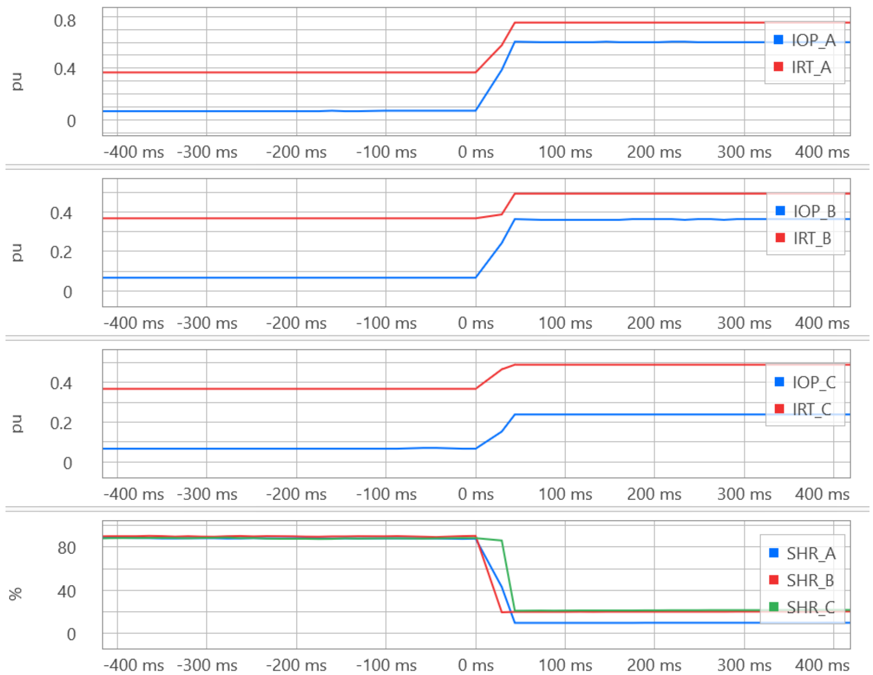

Figure 7.3. Recorded I_{op}, I_{rt}, and SHR of the three phases for the fault with R_F of 80 Ω on phase A during the GIC.

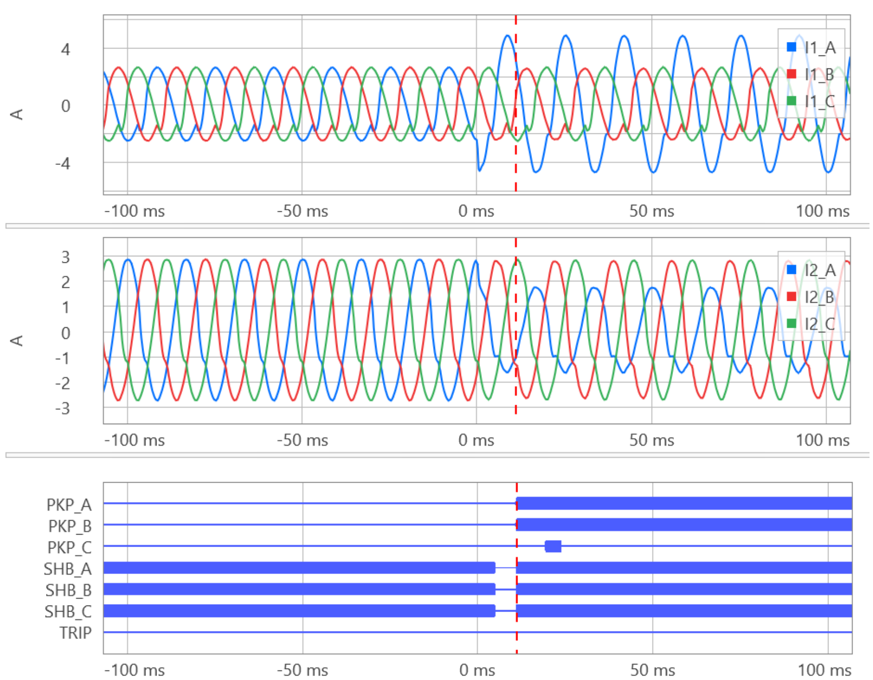

Figure 7.4. The relay recorded signals for the fault with R_F of 160 Ω on phase A during the GIC. The logic is the PBM and thr_{2nd} is 20%.

consider Figure 7.4 showing the recorded signals of the relay with the PBM and thr_{2nd} of 20% for the LV-side fault with the resistance of 160 Ω (I_{op} = 0.33 pu). In this figure, the relay asserts the *PKP* signals for phases A and B at 11.22 ms and temporarily for phase C at 19.56 ms. However, in addition to S_{HB-B} and S_{HB-C}, S_{HB} of the faulted phase A is asserted during the fault because of the GIC; consequently, the relay with the PBM fails to operate for the fault.

According to Table 7.1, by decreasing thr_{2nd} from 20% to 15%, the relay's ability to operate for the faults during the GIC is considerably reduced. For instance, the relay with the CBM and thr_{2nd} of 15% remains blocked for the LV-side faults with R_F of 50 Ω and above, causing I_{op} equal to and smaller than 1.01 pu. Comparing the I_{op} values during the HV-side faults with those related to the LV-side faults for a specific HB logic and threshold in Table 7.1, it is observed that the relay performance is not significantly different for the HV-side faults than the faults on the transformer's LV side in the presence of GIC.

7.3.2 Double-Phase Faults

As discussed in Section 3.3, the differential relays are more likely to remain blocked under the GIC conditions for the single-phase faults compared to other fault types, considering both common and independent HB methods. Moreover, the phase to ground faults are more frequent and likely to occur in the transformer differential protection zone than other fault types. Nonetheless, this subsection examines the performance of the commercial relay for the phase-to-phase or double-phase faults in the presence of GIC. This fault type does not contribute to the zero-sequence current, and thereby, it may not be detected by the REF protection [63, 67].

Figure 7.5 shows an example of the relay performance for a terminal phase A-to-phase B fault with R_F of 200 Ω during the GIC while the HB logic is the CBM with thr_{2nd} of 20%, resulting in I_{op-A} = 0.61 pu and I_{op-B} = 0.68 pu during the fault. As seen in Figure 7.5, PKP_A and PKP_B are asserted at 15.6 ms while the relay is blocked; consequently, the double-phase fault remains uninterrupted during the GIC. It should be noted that regardless of the zero-sequence removal function, the relays employing the CBM are prone to failure to operate even for bolted double-phase faults under the GIC conditions.

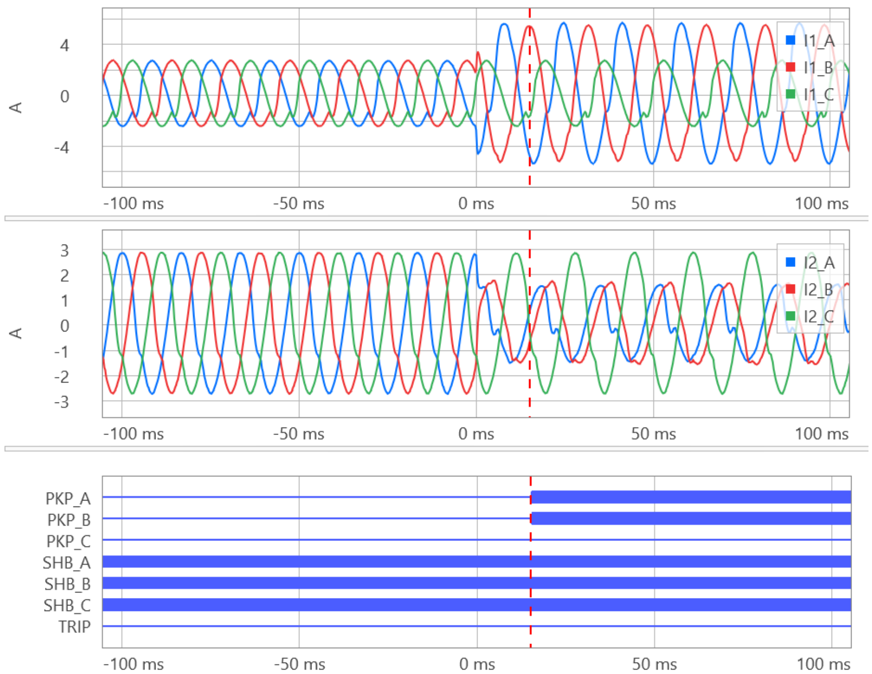

Figure 7.5. The relay recorded signals for the double-phase fault on phases A and B during the GIC. The logic is the CBM and thr_{2nd} is 20%.

7.3.3 Turn Faults

In this subsection, the response of the real-world relay to turn faults under the GIC of 200 A is analyzed. The LV phase A winding-to-ground faults are simulated using the detailed topological transformer model discussed in Section 3.1. The fault turns ratio, i.e., the number of shorted turns divided by the total number of turns, is increased by the steps of 1%, and the relay signals for each turn fault scenario are recorded. Table 7.2 summarizes the results for the CBM and PBM with both thr_{2nd} of 20% and 15%. As observed in this table, the relay remains blocked and stops

TABLE 7.2. THE OPERATION CURRENT AND TURNS RATIO FAILURE RANGES OF THE COMMERCIAL RELAY

Logic	thr_{2nd}	I_{op}	Turns Ratio
CBM	20%	≤ 0.62 pu	≤ 12%
	15%	≤ 0.90 pu	≤ 14%
PBM	20%	≤ 0.31 pu	≤ 8%
	15%	≤ 0.38 pu	≤ 9%

asserting the trip signal for the turn faults causing the I_{op} values around those presented in Table 7.1, associated with the terminal faults.

For instance, the relay with the CBM cannot issue the trip signal for the faults with the turns ratios lower than 12% during the GIC when thr_{2nd} is set at 20%. Regarding the PBM with the same HB threshold, the faults with the turns ratios lower than 8% remain uninterrupted during the GIC. Figure 7.6 illustrates the relay recorded signals for the fault with the turns ratio of 12%. As illustrated in this figure, the relay does not trip for the fault due to the harmonic blocking in the presence of GIC, while the three-phase *PKP* are asserted at 6.26 ms.

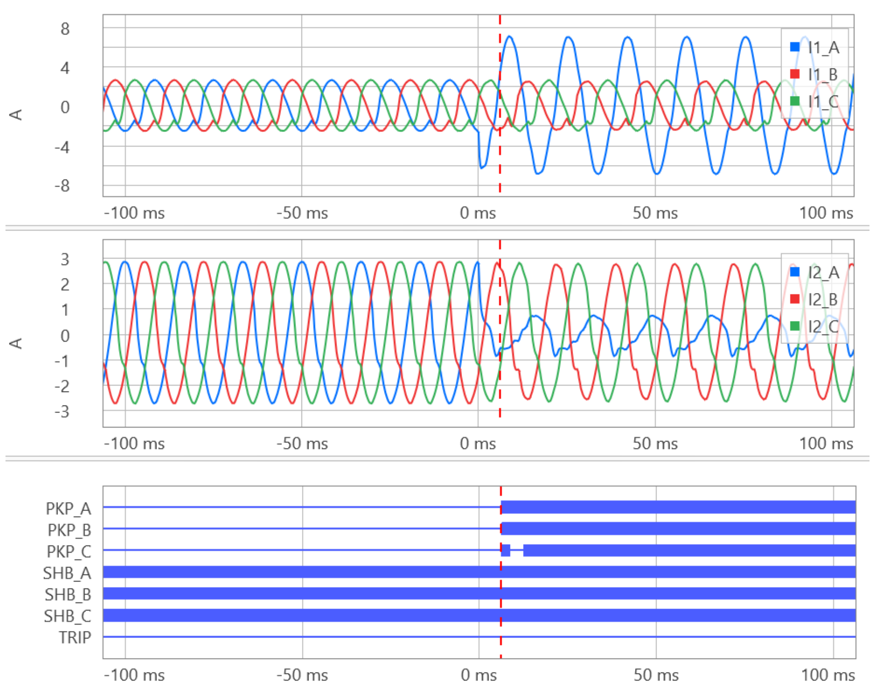

Figure 7.6. The relay recorded signals for the turn fault on phase A with the turns ratio of 12% during the GIC. The logic is the CBM and thr_{2nd} is 20%.

7.3.4 CT Saturation Effect

In the previous subsections, the tests are conducted without considering the CT saturation to examine the commercial relay performance solely under the transformer core saturation caused by the GIC. In this subsection, the relay response to the terminal faults in the presence of GIC is tested during the CT saturation. Table 7.3 summarizes the results for the LV-side faults. By comparing Table 7.3 with the corresponding results in Table 7.1, it can be concluded that the relay dependability level under the GIC conditions is not significantly affected by the CT saturation.

TABLE 7.3. THE OPERATION CURRENT AND LV-SIDE FAULT RESISTANCE FAILURE RANGES OF THE COMMERCIAL RELAY, CONSIDERING THE CT SATURATION

Logic	thr_{2nd}	I_{op}	R_F
CBM	20%	≤ 0.69 pu	≥ 70 Ω
	15%	≤ 0.96 pu	≥ 50 Ω
PBM	20%	≤ 0.27 pu	≥ 170 Ω
	15%	≤ 0.36 pu	≥ 130 Ω

Figure 7.7 shows the recorded signals of the relay for one of the cases in Table 7.3, where the relay employing the CBM with thr_{2nd} of 20% fails to operate for the 70 Ω fault during the GIC and CT1 saturation in the test system (Figure 6.1). In Figure 7.7, observe that the HB signals are not asserted before the fault occurrence. This is because the GIC-caused CT saturation in the tests prevents the operation currents from exceeding the relay's hard-coded cutoff threshold, which forces I_{op} and I_{2nd} to 0 and disables the relay's HB logic, as seen in Figure 7.8. However, in Figure 7.7, 4.43 ms after the fault inception, the three-phase S_{HB} are asserted and remain 1 during the fault since *SHR* of phase B is above 20%, as observed in Figure 7.8. Hence, the relay remains blocked and does not operate for the fault, although PKP_A is asserted at 6.52 ms.

It should be added that depending on several factors in the test system, including the GIC magnitude and the severity of the CT saturation, the GIC-caused CT saturation does not necessarily result in the decrease of the operation currents and unblocking the relay in the pre-fault period, as observed in Figure 7.7.

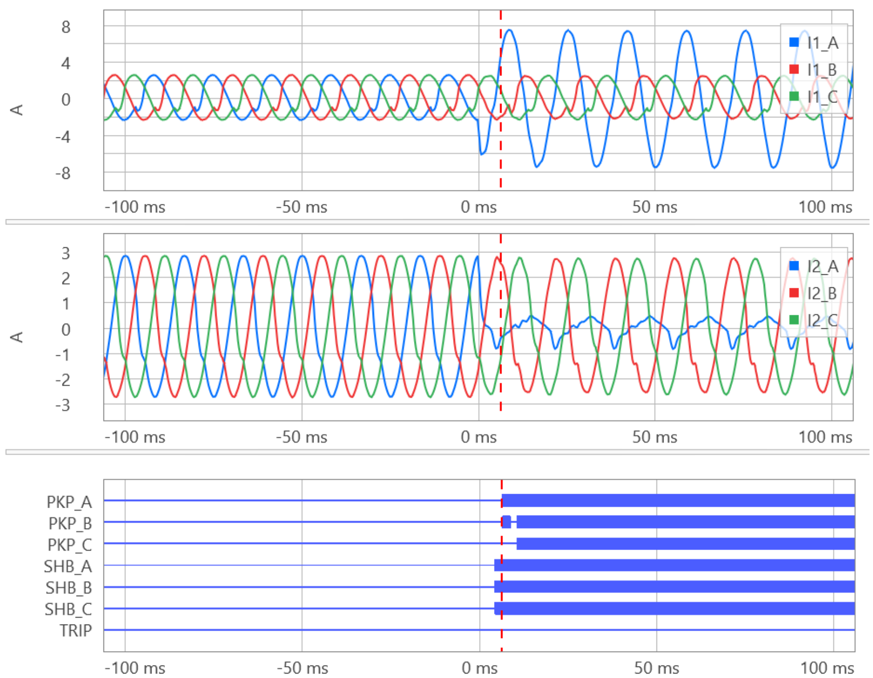

Figure 7.7. The relay recorded signals for the fault with R_F of 70 Ω on phase A during the GIC and CT saturation. The logic is the CBM and thr_{2nd} is 20%.

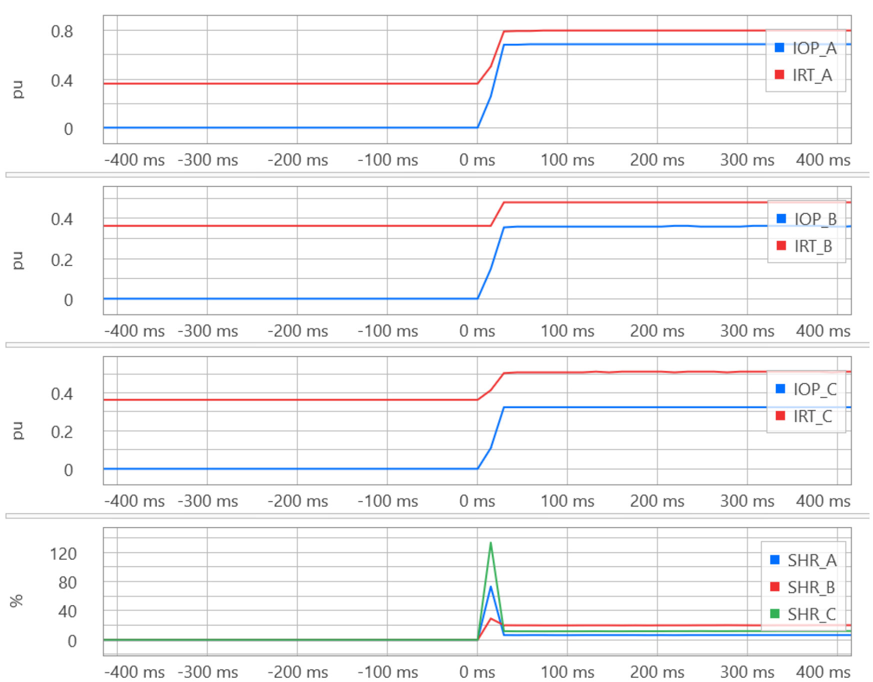

Figure 7.8. Recorded I_{op}, I_{rt}, and *SHR* of the three phases for the fault with R_F of 70 Ω on phase A during the GIC and CT saturation.

7.4 Unblocking Scheme Real-Time Performance

Section 7.3 shows that a real-world transformer differential relay is not able to operate for some internal faults under the GIC condition. This is due to the unwanted harmonic blocking of the relay during the GIC, regardless of the adopted HB logic and threshold, and the CT saturation. This section investigates the real-time response of the proposed unblocking scheme of Figure 6.2 to the internal faults under the GIC condition using the RTDS, with the results shown in Figures 7.9 to 7.12. The following cases are selected from the previous section to demonstrate the scheme's effectiveness in unblocking the relay during the GIC:

- *Case I*: The terminal fault with R_F of 80 Ω when the logic is the CBM.
- *Case II*: The terminal fault with R_F of 160 Ω when the logic is the PBM.
- *Case III*: The turn fault with the turns ratio of 12% when the logic is the CBM.
- *Case IV*: The terminal fault with R_F of 70 Ω during the CT saturation when the logic is the CBM.

In all cases mentioned above, thr_{2nd} is 20%. In Figure 7.9, the three-phase *PKP* and $S_{HB\text{-}ABC}$ as well as the CT currents on the HV (I_1) and LV (I_2) sides, are the real-world relay recorded signals related to *Case I* (Figure 7.2). The fault inception time is shown by a red line at 0 s in Figure 7.9. It is observed that S_{GIC} is 1, showing that the GIC condition is successfully detected by the hybrid GIC detection method (Figure 6.3). S_{PKP} is asserted around 7 ms after the fault, and S_{RCC} is issued at 24 ms; subsequently, S_{UB} is set to 1, unblocking the relay by changing $S_{MHB\text{-}ABC}$ from 1 to 0. This leads to issuing the trip signal at 24 ms for the fault with R_F of 80 Ω. It should be noted that since the external fault detection output, i.e., S_{EXF}, is not asserted in the internal fault cases of this section, it is not shown in the figures below.

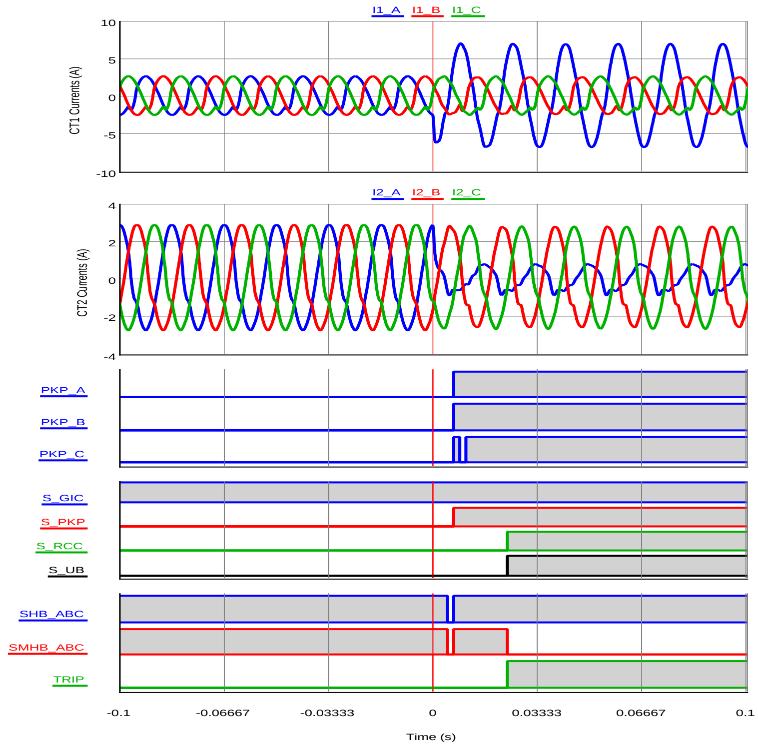

Figure 7.9. Real-time performance of the proposed protection scheme in *Case I*.

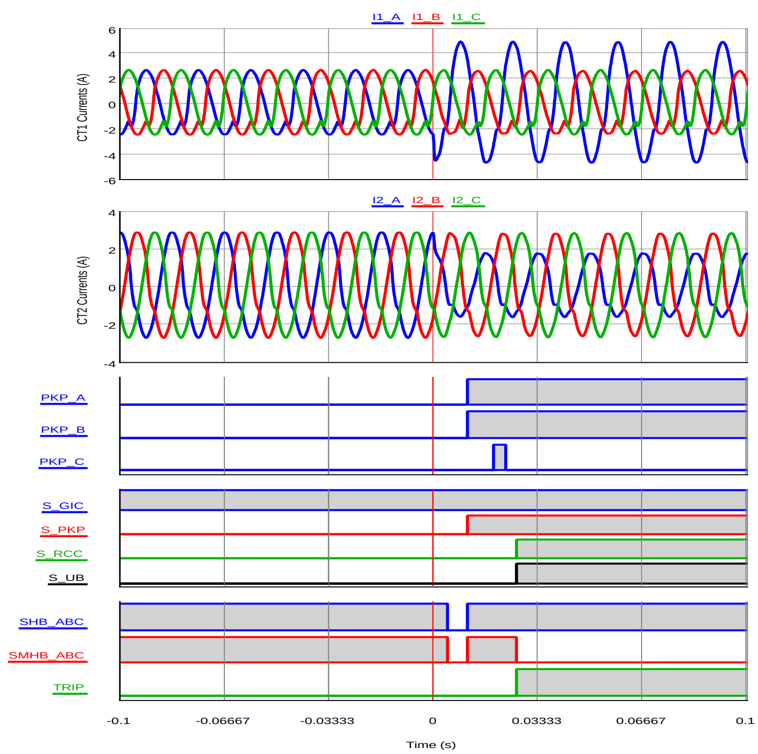

Figure 7.10. Real-time performance of the proposed protection scheme in *Case II*.

In Figure 7.10, although the logic is the PBM, S_{HB} of the three phases are shown as one signal of $S_{HB\text{-}ABC}$ since the HB signals are the same in *Case II*, as observed in Figure 7.4. In Figure 7.10, S_{PKP} is set to 1 around 11 ms after the fault occurrence, and the relay is unblocked (S_{UB} = 1) at 27 ms when S_{RCC} is 1. Hence, $S_{MHB\text{-}ABC}$ is set to 0, allowing the relay to operate for the 160 Ω fault in the presence of GIC.

According to Figure 7.11, related to the real-time behavior of the proposed scheme in *Case III*, the relay is unblocked at 23.7 ms when S_{RCC} is asserted after S_{PKP} and S_{GIC} are set to 1. This allows the relay to operate for the 12% turn fault under the GIC condition since $S_{MHB\text{-}ABC}$ is 0.

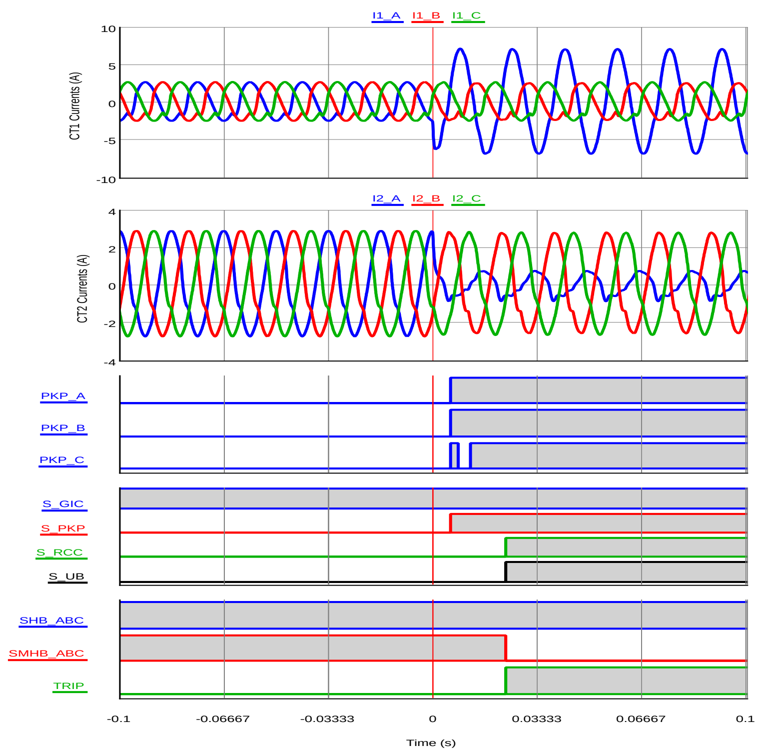

Figure 7.11. Real-time performance of the proposed protection scheme in *Case III*.

Figure 7.12 depicts the real-time response of the proposed scheme in *Case IV*. In this figure, S_{PKP} and S_{RCC} are asserted at 6.52 ms and 19.8 ms after the fault, respectively; hence, S_{UB} is set to

1 at 19.8 ms, unblocking the relay by setting $S_{MHB\text{-}ABC}$ to 0. As a result, the proposed scheme can issue the trip signal for the 70 Ω fault during the GIC and CT saturation, unlike the commercial relay performance shown in Figure 7.7

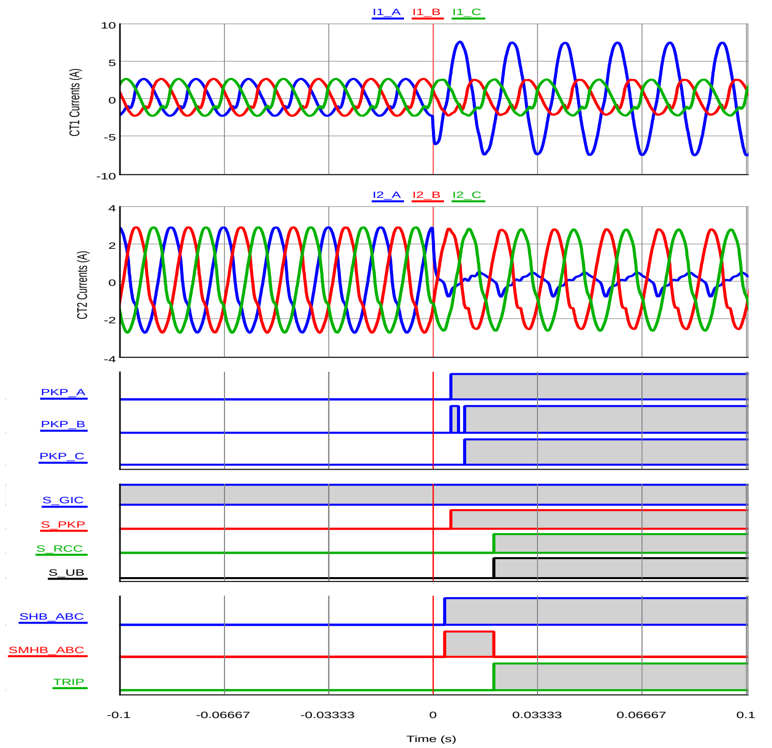

Figure 7.12. Real-time performance of the proposed protection scheme in *Case IV*.

7.5 Summary

In this chapter, the performance of an advanced real-world transformer differential relay was extensively tested using an HIL setup for terminal and turn faults during the GIC, considering both common and independent HB logics with different HB thresholds. It was proven that there are internal fault scenarios in which the commercial relay fails to operate, regardless of the CT saturation. Using the RTDS, the relay recorded signals associated with different fault cases were played back to the hybrid unblocking scheme of Chapter 6, implemented in RSCAD, to verify the scheme's effectiveness in real time. It was shown that the proposed scheme is able to unblock the differential relay, leading to operation for the faults for which the real-world relay fails to trip. The conclusions and topics for future work are presented in the next chapter.

Chapter 8
Conclusions and Future Work

8.1 Conclusions

8.1.1 Summary

The studies and findings of this research can be summarized in four parts, as presented below.

1. The performance of a CBM-based transformer differential relay was investigated for different types of internal short-circuit faults, such as single-phase, two-phase, and three-phase to ground faults, in the presence of GIC using time-domain simulations in EMTP. A detailed and accurate transformer model, pertained to the GIC studies, was employed in the investigations. It was revealed that the relay equipped with the HB module has difficulty operating for the single-phase to ground faults due to the elevated differential current second harmonics caused by the transformer core saturation exposed to the GIC. Furthermore, the effects of factors, such as fault resistance, HB threshold, and transformer loading, on the relay performance during the two-phase to ground faults and GMD were studied. According to the studies, the CBM-based relay is more likely to remain blocked, even for the two-phase to ground faults, under the GIC conditions if (i) the fault resistance increases, (ii) the HB threshold decreases, and (iii) the transformer loading is reduced.
2. The performance of the differential relays, equipped with the common and independent HB approaches, was examined and compared during the bolted and unbolted single-phase faults in

the presence of GIC under loaded and unloaded transformer conditions. It was shown that the relays, employing the independent HB methods of the PBM and SBM, outperform the ones equipped with the common HB methods, i.e., the CBM and ABM. Similar to the ABM, the CBM can keep the relay blocked even for the bolted faults during the GIC. Regarding the unbolted faults, the PBM is superior to the SBM since the former provides a higher level of dependability in the presence of GIC, specifically when the transformer serves a load. Nonetheless, in the unloaded condition, both the PBM- and SBM-based relays lose dependability as the fault resistances and the post-fault differential/operation currents increase above and decrease below certain levels, respectively. The results highlight the necessity of modifying the differential protection logic, regardless of the deployed HB approach, in order to improve the dependability and reduce the chance of unwanted blocking for the in-zone faults under the GIC conditions.

3. The unblocking schemes were devised to address the shortcomings pinpointed in the previous parts by overriding the HB signals during the internal faults and GIC. The devised schemes utilize the GIC detection algorithms and fault detection logics, which function based on the differential relay's available signals. The proposed unblocking schemes are as follows: (i) harmonic-based scheme that employs a GIC detection algorithm, based on the differential current second harmonic phasors, and an internal fault detection logic utilizing the RCCs of the differential current fundamental components, (ii) waveform-based scheme, which detects the GIC flow in the transformer using the unfiltered differential current waveforms and employs the relay's pickup signals, associated with the operation-restraint characteristic, for the relay unblocking solely during the internal faults, and (iii) hybrid scheme that combines the harmonic- and waveform-based GIC detection capabilities to achieve a more reliable and

accurate GIC detection method while employing an external fault detection logic for further security during the external faults and GMDs. Besides verifying the effectiveness of the schemes in the relay unblocking during the internal faults for both three-leg and single-phase transformer core topologies, extensive time-domain simulations were conducted to examine the security of the unblocking schemes in scenarios such as the external faults during the GIC, inrush currents, parallel transformer energization, and the CT saturation. The studies revealed that the developed unblocking schemes significantly improve the dependability of the operation-restraint differential protection for the in-zone faults while maintaining security in the abovementioned GIC- and non-GIC-based scenarios.

4. First, the results of parts 1 and 2 were validated by the HIL testing of a commercial differential relay response to numerous internal fault scenarios during the GIC using the RTDS. The fault scenarios included both terminal single-phase and double-phase/phase-to-phase faults as well as turn faults, with and without considering the GIC-caused CT saturation. Moreover, both the CBM and PBM with the typical HB thresholds of 20% and 15% were considered in the tests. According to the HIL test results, there are terminal and turn faults for which the advanced real-world relay fails to operate due to the unwanted harmonic blocking in the presence of GIC, regardless of the CT saturation and the employed HB logic. Afterward, the real-time performance of the hybrid unblocking scheme, implemented in RSCAD, was analyzed using the RTDS-based playback of the commercial relay recorded signals associated with different fault scenarios. It was shown in real time that the unblocking scheme can successfully detect the GIC condition and override the commercial relay's HB signals to allow the operation for the internal faults that remain uninterrupted by the real-world relay with the CBM and PBM logics.

8.1.2 Contributions

The followings highlight the dissertation contributions:

- Detailed time-domain performance analysis and comparison of the transformer differential relays equipped with the CBM, ABM, PBM, and SBM for the internal faults in the presence of GIC. A three-leg transformer model, representing the magnetic coupling among phases and the accurate off-core flux paths that are necessary to be modeled under GIC-caused core saturation conditions, was considered in the studies. The studies pinpointed the differential protection failures in operating for some in-zone faults because of unwanted harmonic blocking during the GIC, regardless of the employed HB method.
- Proposing different unblocking approaches to ensure the dependability of the transformer differential relays for the in-zone faults during the GIC, as follows:

  i. *Harmonic-based approach*: This approach identifies the GIC flow if the differential current second harmonic phasors represent a negative-sequence order and I_{2nd} in any phase exceeds an adjustable threshold. The principle of this GIC detection method is that the elevated second harmonic phasors, caused by the transformer core saturation during the GIC with the same magnitude and direction in each phase, form a negative-sequence relationship, while they are in a positive-sequence order during the inrush currents. The approach also employs an internal fault detection logic that detects the internal faults if *RCC* in any phase is larger than an adjustable threshold thr_{RCC}. In this unblocking scheme, thr_{RCC} is required to be set such that the RCC-based fault detection logic does not assert during the external faults and GIC, while maintaining sensitivity for the internal faults. The scheme's effectiveness in unblocking the differential relays was verified for different transformer core topologies. Moreover, it was shown that the harmonic-based approach is more secure than a typical waveform-based inrush detection/blocking scheme, i.e., gap detection technique, in both GIC and energization cases while there is the CT saturation.

ii. *Waveform-based approach*: This approach employs an alternative GIC detection algorithm based on the unfiltered differential current waveforms. During the GIC-caused core saturation, the three-phase i_{Diff} are all asymmetric and have the same positive or negative direction, unlike the transformer energization cases resulting in the waveforms with both positive and negative directions. Because of using the unfiltered waveforms, the performance of the WGD algorithm was investigated while the three-phase i_{Diff} were polluted with white Gaussian measurement noise, and it was verified that the algorithm performance is immune to the noise. Furthermore, the algorithm effectiveness was investigated for different transformer core topologies and winding connections in order to show that the abovementioned i_{Diff} behavior is independent of transformer specifications. Unlike the harmonic-based unblocking scheme, the waveform-based approach utilizes the differential relay's pickup signals, based on the operation-restraint characteristic, to unblock the relay solely for the internal faults under the GIC conditions. This alleviates the possible complexity of the threshold selection for the RCC-based logic, as employed in the harmonic-based approach for internal fault detection. Additionally, utilizing the pickup signals can provide superior security during external faults and CT saturation, considering the fact that such signals are generally supervised by more sophisticated logics, e.g., external fault detection logics.

iii. *Hybrid approach*: This approach utilizes both harmonic- and waveform-based GIC detection methods to recognize the GIC conditions, which provides superior reliability than the individual harmonic-based or waveform-based method. This is because the hybrid GIC detection approach does not rely solely on the second harmonic phasors or the differential current waveforms to identify the GIC. The waveform-based GIC detection algorithm is supervised by an average-based algorithm to prevent possible false GIC detection for severe external faults in the absence of GIC. Using a D index, calculating the difference between the i_{Diff}'s 1-cycle average and the average of the waveform's MAX and MIN values, the ABA is able to more accurately decide whether the waveform is asymmetric, considering the fact that the D index of a symmetrical waveform is small. The GIC detection capabilities of the hybrid method as well as the individual harmonic- and waveform-based algorithms were compared for different GIC magnitudes. An external fault detection logic is developed to enhance the unblocking scheme security for the external faults and CT saturation, specifically during the extreme GMDs, which may cause the differential protection to pick up before the fault inception due to the elevated I_{op}. The logic declares an external fault if RCC of the restraint current I_{rt} in any phase is higher than the corresponding RCC of I_{op}, while the latter also exceeds thr_{RCC}. To ensure dependability and the relay unblocking, the external fault detection logic is equipped with a reset mechanism to reset any unwanted S_{EXF} in some low-current internal fault conditions. The reset mechanism asserts for the internal faults by checking the pickup criterion based on a ΔI_{op}-I_{rt} characteristic, in addition to other RCC-based criteria. The variable ΔI_{op} is not affected by the GIC magnitude, and therefore, its utilization in the operation-restraint characteristic (instead of I_{op}) prevents any wrong pickup during the extreme GMDs, prior to the faults. The dependability and security of the hybrid unblocking scheme were verified in numerous scenarios.

- Conducting real-time verification tests that included: (i) HIL testing of a commercial differential relay with the CBM and PBM during the internal faults and GIC, and showing that the commercial relay fails to operate for the terminal and turn faults with the specific R_F/turns ratio and I_{op} ranges, regardless of the deployed HB logic and threshold and (ii) real-time performance verification of the hybrid unblocking scheme based on the real-world relay recorded signals and proving that the relay equipped with the unblocking scheme can issue trip for the internal faults for which it remains blocked without the unblocking scheme. The real-time test results verify the feasibility of real-world implementation of the proposed GIC detection algorithms and fault detection logics to improve the dependability of existing differential relays during in-zone faults and GMDs.

8.2 Future Work

The future research on the power equipment protection under the GIC conditions could include the following topics:

- Detailed time-domain performance analysis of other transformer protection elements during the GMDs, such as the REF and negative-sequence differential relays, as well as transmission line and generator protection schemes.
- Performance evaluation of transformer and line differential relays in converter-based power systems under the GIC conditions, including the high voltage direct current (HVDC) systems and wind farms such as doubly fed induction generator (DFIG)-based wind farms.
- Investigating the behavior of available external fault detection approaches employed in the differential protection in the presence of GIC.

List of Publications

The publications during the Ph.D. studies are listed below.

1. B. Ahmadzadeh-Shooshtari and A. Rezaei-Zare, “Transformer differential protection during geomagnetic disturbances: A hybrid protection scheme and real-time validation tests,” *IEEE Trans. Power Del.*, Accepted for Publication, Oct. 2023.
2. B. Ahmadzadeh-Shooshtari and A. Rezaei-Zare, “Transformer DC bias detection using differential current waveforms,” *IEEE Ind Appl. Magazine*, Accepted for Publication, Jul. 2023.
3. B. Ahmadzadeh-Shooshtari and A. Rezaei-Zare, “Real-time performance verification of a commercial transformer differential relay under GIC conditions,” *IEEE Kansas Power and Energy Conf. (KPEC)*, Manhattan, Kansas, Apr. 2023.
4. B. Ahmadzadeh-Shooshtari and A. Rezaei-Zare, “A waveform-based approach for transformer differential protection under GIC conditions,” *IEEE Trans. Power Del.*, vol. 37, no. 6, pp. 5366-5375, Dec. 2022.
5. B. Ahmadzadeh-Shooshtari and A. Rezaei-Zare, “Advanced transformer differential protection under GIC conditions,” *IEEE Trans. Power Del.*, vol. 37, no. 3, pp. 1433–1444, Jun. 2022.
6. B. Ahmadzadeh-Shooshtari and A. Rezaei-Zare, “A method to detect DC bias in transformers using differential current waveforms,” *IEEE Int. Conf. Environment and Electrical Engineering*, Prague, Czech Republic, Jun. 2022.
7. A. Rezaei-Zare and B. Ahmadzadeh-Shooshtari, “System and method for differential protection under geomagnetically induced current,” *US Patent App. Publication*, Feb. 2022.
8. B. Ahmadzadeh-Shooshtari and A. Rezaei-Zare, “Comparison of harmonic blocking methods in transformer differential protection under GIC conditions,” *IEEE Electr. Power and Energy Conf. (EPEC)*, Toronto, ON, Oct. 2021.
9. B. Ahmadzadeh-Shooshtari and A. Rezaei-Zare, “Analysis of transformer differential protection performance under geomagnetically induced current conditions,” *Electr. Power Syst. Research*, vol. 194, pp. 1–8, May 2021.

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