

STACKED-SWITCHED ELECTROLYTIC
CAPACITOR-LESS AC/DC POWER
CONVERTERS

SIAMAK DERAKHSHAN

A DISSERTATION SUBMITTED TO
THE FACULTY OF GRADUATE STUDIES
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

GRADUATE PROGRAM IN
ELECTRICAL ENGINEERING AND COMPUTER SCIENCE
YORK UNIVERSITY
TORONTO, ONTARIO

September 2025

© Siamak Derakhshan, 2025

Abstract

The growing adoption of Electric Vehicles (EVs) has increased the demand for compact, efficient, and reliable On-Board Chargers (OBCs) capable of interfacing directly with the AC grid. Conventional single-phase AC/DC converters often depend on bulky electrolytic capacitors, diode bridges, and hard-switching circuits, leading to reduced reliability, increased losses, and limited power density. Additionally, the need for bidirectional energy flow—such as Vehicle-to-Grid (V2G) and Vehicle-to-Home (V2H)—requires grid-compliant converters with enhanced functionality and robust control strategies.

This dissertation presents novel single-phase AC/DC converter topologies and control systems designed to eliminate electrolytic capacitors while enabling efficient bidirectional power transfer and robust grid-forming capabilities. The work is organized around three primary contributions.

First, a unidirectional bridgeless AC/DC converter is proposed, utilizing a stacked-switch configuration to reduce voltage stress and operating in Discontinuous Conduction Mode (DCM) to achieve inherent power factor correction. Closed-loop control based on Variable Frequency Modulation (VFM) is used for voltage regulation, and a secondary-side duty modulation strategy minimizes low-frequency ripple, enabling the use of compact, long-life capacitors. Experimental validation on a 1.1 kW prototype confirms high power factor (>0.99), low THD ($<2.5\%$), and soft-switching operation.

Second, a bidirectional converter is introduced, combining a half-bridge dual stacked-switch AC/DC stage and a CLLC resonant DC/DC stage. A dq-

frame-based controller ensures low harmonic injection and effective grid synchronization in both power flow directions. Ripple reduction is again achieved through duty modulation, validated on a 1 kW prototype.

Finally, a robust grid-forming control scheme is developed using $\mathcal{H}_\infty$ synthesis with Linear Matrix Inequalities (LMIs), ensuring voltage stability under uncertainty and distortion. Experimental results confirm dynamic performance and low output distortion.

Together, these contributions support next-generation EV charging systems with high reliability, bidirectional capability, and electrolytic capacitorless design.

To my parents

Acknowledgements

First and foremost, I would like to express my deepest gratitude to my supervisor, Dr. John Lam, for his unwavering support, insightful guidance, and incredible patience throughout my Ph.D. journey. His technical expertise and mentorship have shaped not only the direction of my research but also the way I think as an engineer and a scholar. I truly appreciate the many conversations—both technical and personal—that helped me stay grounded and motivated during the most challenging phases of this work.

I am also sincerely thankful to the members of my dissertation examination committee, Dr. Afshin Rezaei-Zare and Dr. Ping Wang, for their valuable time, constructive feedback, and continuous encouragement over the years. Their thoughtful input helped refine the quality of this dissertation and has been instrumental in shaping the final outcome.

I would like to extend my heartfelt appreciation to my parents, whose love and sacrifices have been the foundation of everything I have achieved. Their belief in my potential and their constant encouragement have been a powerful source of strength throughout this journey. This accomplishment is as much theirs as it is mine.

Contents

Abstract	ii
Dedication	iv
Acknowledgments	v
Table of Contents	vi
List of Tables	viii
List of Figures	ix
List of Abbreviations	xiv
Chapter 1: Introduction	1
1.1 Introduction	1
1.2 Electric Vehicles and Charging Infrastructure	2
1.2.1 Off-Board Battery Chargers	8
1.2.2 On-Board Battery Chargers	11
1.3 AC/DC Power Converters for EV Charging	14
1.3.1 Single-Phase Unidirectional Converters	15
1.3.2 Recent Unidirectional AC/DC Converter Topologies	21
1.3.3 Single-Phase Bidirectional Converters	23
1.4 Recent Bidirectional AC/DC Converter Topologies	29
1.5 Storage Capacitance Reduction in AC/DC Power Converters ...	31
1.5.1 Different Types of Capacitors	32
1.5.2 Voltage Ripple Reduction	34
1.6 Control Principles in AC/DC Power Converters	40
1.6.1 PFC Control	41
1.6.2 Voltage Regulation	45
1.6.3 Grid-Forming Control	47
1.6.4 Grid-Following Control	50
1.7 Recent Grid-Connected Control designs for Bidirectional AC/DC Converters	52
1.8 Technical Challenges and Possible Solutions	54
1.8.1 Achieving High Efficiency Without Compromising Sim- plicity	54
1.8.2 Managing Large Storage Capacitance Requirements	54
1.8.3 Supporting Bidirectional Power Flow and Grid Services ..	55
1.8.4 Robust GFM Control with Improved Transient Perfor- mance	55
1.8.5 Summary	56
1.9 Research Objectives	56
1.10 Dissertation Outline	57
Chapter 2: Unidirectional Bridgeless, Stacked Switch-Pair-Based AC/DC Power Converter with Minimal Storage Capacitance	59
2.1 Introduction	59
2.2 Description and Operation of the Converter	60
2.3 Converter Analysis	66
2.3.1 PFC Boost Converter	66
2.3.2 Maximum and RMS Switch Currents	69
2.3.3 Voltage Gain	71

2.4	Control System Design	74
2.4.1	Input Current Control	75
2.4.2	Output Voltage Regulation	77
2.4.3	Output Voltage Ripple Reduction	80
2.5	Experimental Validation	82
2.5.1	Design Procedure	84
2.5.2	Steady-State Experimental Results	85
2.5.3	Dynamic Response Experimental Results	92
2.5.4	Comparison	93
2.6	Chapter Summary	96
Chapter 3: Bidirectional Half-Bridge/Dual Stacked-Switches Structured Electrolytic Capacitor-Less AC/DC Power Con- verter		99
3.1	Introduction	99
3.2	Description and Operation of the Converter	100
3.3	Converter Analysis	106
3.3.1	Half-Bridge PFC Converter	106
3.3.2	Ripple Reduction Method	110
3.4	Control System Design	114
3.4.1	PFC Current Controller	115
3.4.2	Output Voltage Regulation	118
3.4.3	Ripple Reduction Controller	121
3.5	Experimental Validation	125
3.5.1	AC to DC Mode Experimental Results	126
3.5.2	DC to AC Mode Experimental Results	133
3.5.3	Dynamic Response Experimental Results	136
3.5.4	Comparison	138
3.6	Chapter Summary	141
Chapter 4: Linear Matrix Inequality-Based Robust H_∞ AC- Grid-Forming Control System		143
4.1	Introduction	143
4.2	State-Space Dynamic Modeling	144
4.2.1	Integral Augmentation for Zero Steady-State Error	145
4.2.2	Polytopic Uncertainty Modeling	148
4.3	Robust H_∞ GFM Controller Design	150
4.4	Experimental Validation	152
4.5	Chapter Summary	163
Chapter 5: Conclusion and Future Work		165
5.1	Contributions	165
5.2	Future Work	166
Bibliography		168
Appendix A: List of Publications		177
Appendix B: Printed Circuit Board (PCB) Layouts		179
Appendix C: PSIM Schematics		182

List of Tables

1.1	Charging stations classification	7
1.2	Comparative analysis of electrolytic, film, and ceramic capacitors.	35
2.1	Parameter Values of the Designed Prototype	83
2.2	Comparison with the State-of-the-Art EV OBCs.....	90
3.1	Parameter Values of the Designed Prototype	126
3.2	Comparison with the State-of-the-Art EV OBCs.....	142
4.1	Parameter Values of the Designed Prototype	153

List of Figures

1.1	Carbon dioxide emissions from energy-related activities, categorized by economic sector in the United States in the year 2024 [14].	3
1.2	U.S. energy-related carbon dioxide emissions by sector, 2020-2024 [15].	4
1.3	Global EV sales by region from 2015 to 2024. Data based on reported sales volumes from China, Europe, the U.S., and other global markets [18].	5
1.4	Power connections and off-board charging system for HV battery system in EV.	9
1.5	Power connections and on-board charging system for HV battery system in EV.	12
1.6	Types of PFC: (a) Passive PFC, (b) Active PFC using a boost converter.	16
1.7	Diode Rectifier with Two-Level Boost Converter.	17
1.8	Diode Rectifier with Three-Level Boost Converter.	17
1.9	Full-bridge rectifier with isolated resonant circuit.	18
1.10	AC/DC converter with bridge-less topology.	19
1.11	AC/DC converter based on totem-pole bridge-less topology.	19
1.12	A diode-clamp five-level AC/DC converter.	20
1.13	Half-bridge PWM converter as PFC.	24
1.14	Full-bridge PWM converter as PFC.	25
1.15	Three-Level converter as PFC.	26
1.16	Dual active bridge bi-directional converter.	26
1.17	Three-level bi-directional converter.	27
1.18	Four-switch string structure bi-directional converter.	27
1.19	Ripple characteristics of the four-switch string converter in rectifier mode.	28
1.20	Bi-directional DAB-based matrix converter.	28
1.21	Totem-pole bi-directional AC/DC converter.	29
1.22	Electrolytic Capacitor [77].	33
1.23	Film Capacitor [78].	33
1.24	Ceramic Capacitor [79].	34
1.25	Popular voltage ripple reduction circuits: (a) low-pass filter, (b) common mode choke filter, (c) capacitance multiplier.	36
1.26	AC/DC converter employing synchronous rectification.	37
1.27	Output waveforms from a synchronous rectification converter synchronized to double-line frequency.	38
1.28	Harmonic injection-based control strategy for ripple mitigation [65].	39
1.29	PFC based on peak current control implemented on boost converter.	42
1.30	Current waveform while implementing peak current control technique.	42

1.31	PFC based on average current control implemented on boost converter.	43
1.32	Current waveform while implementing average current control technique.	43
1.33	PFC based on hysteresis current control implemented on boost converter.	44
1.34	Current waveform while implementing hysteresis current control technique.	44
1.35	Pulse Width Modulation scheme.	46
1.36	Block diagram of duty ratio control based on PI controller.	46
1.37	Phase-Shifted full-bridge converter.	47
1.38	PSM-based waveforms of a phase-shifted full-bridge converter. ..	47
1.39	CLL-based resonant converter.	48
1.40	CLL resonant circuit gain waveform.	48
1.41	Block diagram of VFM control based on PI controller.	48
1.42	GFM control.	49
1.43	GFM control using LCL filter interface.	50
1.44	GFM control structure.	50
1.45	GFL control.	51
1.46	GFL inverter with LCL filter.	52
1.47	GFL control structure.	52
2.1	Single-stage stacked switches-based bridgeless AC/DC converter.	60
2.2	Key operating waveforms of the AC/DC converter.	62
2.3	Operational stages of the bridgeless AC/DC converter within a switching period in the positive half cycle.	63
2.4	Conditions for DCM and CCM operation of the front-end PFC boost rectifier.	68
2.5	Input current example of the DCM PFC converter operating in CCM at the peak of the input voltage.	69
2.6	Equivalent circuit of the CLLC resonant circuit in the AC/DC converter.	72
2.7	Overall voltage gain plot of the converter for $D_s = 0$ for $m = 10$ and $k = 0.8$	73
2.8	Overall voltage gain plot of the converter for $D_s > 0$	74
2.9	Block diagram of the developed input current controller for the converter.	75
2.10	Block diagram of the developed VFM-based output voltage regulation controller for the converter.	78
2.11	Bode diagram of the closed-loop system for the developed VFM-based controller.	78
2.12	Block diagram of the developed ripple reduction controller for the converter.	79
2.13	Ripple Reduction Control key waveforms.	79
2.14	Bode diagram of the closed-loop system for the developed ripple reduction controller.	80
2.15	Picture of the Proof-of-concept Prototype.	82
2.16	Soft-switching region of the designed converter.	83
2.17	Input and Output waveforms of the converter at rated power.	85
2.18	Input voltage, input current, and boost inductor current waveforms.	86
2.19	Voltage over and current flowing through S_1 at line frequency. ..	87
2.20	Voltage over and current flowing through S_1 at switching frequency.	87
2.21	Voltage over and current flowing through S_2 at line frequency. ..	88

2.22	Voltage over and current flowing through S_2 at switching frequency.	89
2.23	Voltage over and current flowing through S_6 at line frequency. ..	91
2.24	Voltage over and current flowing through S_6 at switching frequency.	91
2.25	Dynamic performance of the system against output voltage reference change.	93
2.26	Dynamic performance of the system against input voltage variation.	94
2.27	Dynamic performance of the system without and with the closed-loop control systems.	95
2.28	Efficiency Curve of the designed converter for different input voltages.	96
2.29	Power Factor Curve of the designed converter for different input voltages.	96
2.30	Harmonic distortion captured from the hardware experimental prototype showing first to seventh harmonics.	97
2.31	Harmonic distortion captured from the hardware experimental prototype showing seventh to thirteenth harmonics.	97
2.32	Harmonic distortion captured from the hardware experimental prototype showing thirteenth to nineteenth harmonics.	98
3.1	Half-bridge/dual-stacked switched-structured bridgeless bidirectional AC/DC converter.	100
3.2	Key operating waveforms of the designed bidirectional AC/DC converter.	103
3.3	Operational stages of the designed bridgeless bidirectional AC/DC converter within a switching period in the positive half cycle. ...	105
3.4	Operational stages of the employed bidirectional HB PFC converter.	106
3.5	LCL filter connected to the bidirectional HB PFC converter.	108
3.6	Visualization of dq and $\alpha\beta$ reference frame with corresponding vectors.	108
3.7	Soft-switching condition, (a) ZVS turn ON, (b) ZCS turn ON and, (c) hard-switching.	110
3.8	Active rectification for both modes of the designed bidirectional converter. (a) Converter's operation in AC to DC mode, (b) Converter's operation in DC to AC mode.	111
3.9	Equivalent circuit of the CLLC resonant circuit connected to leg A of the designed converter.	113
3.10	Overall voltage gain plot of the designed converter for $D_s > 0$. ..	115
3.11	Block diagram of the developed PFC controller for the designed bidirectional converter.	117
3.12	Bode diagram of the closed-loop system for the developed dq -based PFC controller.	118
3.13	Block diagram of the developed VFM-based output voltage regulation controller for the designed converter.	119
3.14	Bode diagram of the closed-loop system for the developed VFM-based controller.	119
3.15	Block diagram of the developed ripple reduction controller for the designed converter.	121
3.16	Bode diagram of the closed-loop system for the developed ripple reduction controller.	122
3.17	Unified block diagram representation of all the developed control systems.	123

3.18	Picture of the Proof-of-concept prototype.	125
3.19	Input and Output waveforms of the converter at rated power in AC to DC mode.	127
3.20	Voltage over and current flowing through S_1 at line frequency in AC to DC mode.	127
3.21	Voltage over and current flowing through S_1 at switching frequency in AC to DC mode.	128
3.22	Voltage over and current flowing through S_3 at line frequency in AC to DC mode.	129
3.23	Voltage over and current flowing through S_3 at switching frequency in AC to DC mode.	130
3.24	Voltage over and current flowing through S_4 at line frequency in AC to DC mode.	130
3.25	Voltage over and current flowing through S_4 at switching frequency in AC to DC mode.	131
3.26	Voltage over and current flowing through S_8 at line frequency in AC to DC mode.	132
3.27	Voltage over and current flowing through S_8 at switching frequency in AC to DC mode.	132
3.28	Voltage over the DC-link capacitors C_{i1} (V_{ci1}) and C_{i2} (V_{ci1}), and overall DC-link voltage in AC to DC mode.	133
3.29	Input and Output waveforms of the converter at rated power in DC to AC mode.	134
3.30	Voltage over and current flowing through S_1 at switching frequency in DC to AC mode.	134
3.31	Voltage over and current flowing through S_7 at switching frequency in DC to AC mode.	135
3.32	Voltage over and current flowing through S_8 at switching frequency in DC to AC mode.	136
3.33	Dynamic performance of the system against input voltage variation in AC to DC mode.	137
3.34	Dynamic performance of the system against input current reference change in DC to AC mode.	138
3.35	Efficiency Curve of the designed converter for different input voltages.	138
3.36	Power Factor Curve of the designed converter for different input voltages.	139
3.37	Harmonic distortion captured from the hardware experimental prototype.	139
4.1	Block diagram of the designed AC-GFM controller for an OBC connected to unknown load through LCL filter.	146
4.2	Unified Block diagram of all the controllers implemented in the OBC in Chapter 3 during V2H operation.	147
4.3	Picture of the Proof-of-concept prototype.	153
4.4	Input and Output waveforms of the converter at rated power in DC to AC mode with AC-GFM controller.	154
4.5	Experimental voltage and current waveforms of switch S_1 at line frequency, confirming ZVS behavior.	155
4.6	Switch S_1 waveforms at switching frequency showing ZVS turn-on during high-frequency operation (case 1).	155
4.7	Switch S_1 waveforms at switching frequency showing ZVS turn-on during high-frequency operation (case 2).	156
4.8	Experimental THD and output voltage waveform for $L_{in} = 350 \mu\text{H}$, showing 1.96% THD.	157

4.9	Experimental THD and output voltage waveform for nominal case $L_{in} = 550 \mu\text{H}$, showing 2.20% THD.	157
4.10	Experimental THD and output voltage waveform for $L_{in} = 1 \text{ mH}$, showing 2.94% THD.	158
4.11	Experimental validation of dq reference tracking performance. The d - and q -axis voltage references are changed from (1.0, 0.0) p.u. to (0.8, 0.6) p.u..	159
4.12	Experimental load voltage and current waveforms at 750 W load.	161
4.13	Experimental load voltage and current waveforms at 850 W load.	162
4.14	Experimental dynamic response under load change.	162
B.1	PCB layout of the proposed AC/DC bidirectional converter.	179
B.2	3-D view of the PCB layout of the proposed AC/DC bidirectional converter.	180
B.3	PCB layout of the measurement board designed for the proposed AC/DC bidirectional converter.	180
B.4	3-D view of the PCB layout of the measurement board designed for the proposed AC/DC bidirectional converter.	181
C.1	Diagram of a proposed unidirectional AC/DC converter topology and its control blocks from PSIM.	182
C.2	Diagram of a proposed bidirectional AC/DC converter topology in AC to DC mode and its control blocks from PSIM.	183
C.3	Diagram of a proposed bidirectional AC/DC converter topology in DC to AC mode and its control blocks from PSIM.	183
C.4	Diagram of a proposed bidirectional AC/DC converter topology in DC to AC mode and the developed AC-GFM control block from PSIM.	184

List of Abbreviations

ADC	Analog-to-Digital Converter
AI	Artificial Intelligence
BMS	Battery Management System
CCM	Continuous Conduction Mode
CLL	Capacitor-Inductor-Inductor (Resonant Circuit)
CLLC	Capacitor-Inductor-Inductor-Capacitor
DC	Direct Current
DCM	Discontinuous Conduction Mode
DPT	Double Pulse Test
DSP	Digital Signal Processor
dq	Direct-Quadrature (Reference Frame)
EMI	Electromagnetic Interference
EV	Electric Vehicle
FB	Full-Bridge
FFT	Fast Fourier Transform
G2V	Grid-to-Vehicle
GFM	Grid-Forming
GFL	Grid-Following
HB	Half-Bridge
HV	High Voltage
ICE	Internal Combustion Engine
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
LCL	Inductor-Capacitor-Inductor Filter
LMI	Linear Matrix Inequality
MPPT	Maximum Power Point Tracking
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
OBC	On-Board Charger
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PFC	Power Factor Correction
PLL	Phase-Locked Loop
PSM	Phase Shift Modulation
PWM	Pulse Width Modulation
RMS	Root Mean Square

SiC	Silicon Carbide
SoC	State of Charge
SR	Synchronous Rectification
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
V2G	Vehicle-to-Grid
V2H	Vehicle-to-Home
V2L	Vehicle-to-Load
VDC	DC-Link Voltage
VFM	Variable Frequency Modulation
VRRC	Voltage Ripple Reduction Circuit
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Chapter 1

Introduction

1.1 Introduction

The global shift toward sustainable transportation has accelerated the adoption of Electric Vehicles (EVs), driven by advancements in battery technology, environmental concerns, and supportive governmental policies. As the number of EVs continues to grow, so does the demand for efficient, reliable, and cost-effective charging infrastructure. At the core of this infrastructure lie power electronic converters, which facilitate the critical energy conversion processes required for EV charging [1], [2].

In particular, AC/DC power converters play a fundamental role in connecting EVs to the electric grid. These converters are responsible for rectifying grid-supplied Alternating Current (AC) into the Direct Current (DC) required by EV batteries. Depending on their location within the charging system, these converters may be integrated into the vehicle itself—known as On-Board Chargers (OBCs) or be part of external charging stations, referred to as off-board chargers. Each configuration presents distinct design challenges and performance requirements, particularly in terms of size, efficiency, power density, and control complexity [3], [4].

Furthermore, the emergence of bidirectional charging systems has introduced new paradigms such as Vehicle-to-Grid (V2G) and Vehicle-to-Home (V2H), enabling EVs to act not only as energy consumers but also as dynamic storage resources. These applications necessitate the development of advanced bidirectional converters capable of handling power flow in both directions while

ensuring grid compliance and system stability [5], [6].

One of the key technical challenges in the design of EV chargers, especially for single-phase systems, is the bulky storage capacitance traditionally required to meet ripple requirements. Reducing or eliminating this capacitance without compromising performance is an ongoing research focus, with implications for converter size, reliability, and cost [7]–[9]. Additionally, the development of robust control strategies is essential for ensuring stability, fast dynamic response, and accurate power regulation under varying grid and load conditions [10]–[12].

This dissertation investigates the design, modeling, control, and implementation of single-phase AC/DC converters for EV charging applications, with a particular emphasis on storage capacitance reduction, bidirectional operation and robust performance. It aims to contribute novel design methodologies and control strategies that improve performance while reducing component stress, size, and cost. The following sections outline the relevant background, highlight key technical challenges, and present the research objectives that guide this work.

1.2 Electric Vehicles and Charging Infrastructure

Climate change is caused by the buildup of greenhouse gases in the atmosphere, with carbon dioxide (CO_2) being the most common of these gases. The combustion of fossil fuels such as coal, oil, and natural gas, as well as their derivatives like gasoline and diesel fuel, leads to the release of carbon dioxide into the atmosphere [13]. As illustrated in Fig. 1.1, the transportation sector was responsible for approximately 39% of the total U.S. energy-related carbon dioxide emissions in 2024. This makes it the largest contributor among all economic sectors, followed by electric power generation (30%) and the industrial sector (20%) [14], [15]. The continued dominance of transportation in emissions has heightened environmental concerns and underscored the urgency of transitioning to cleaner mobility technologies.

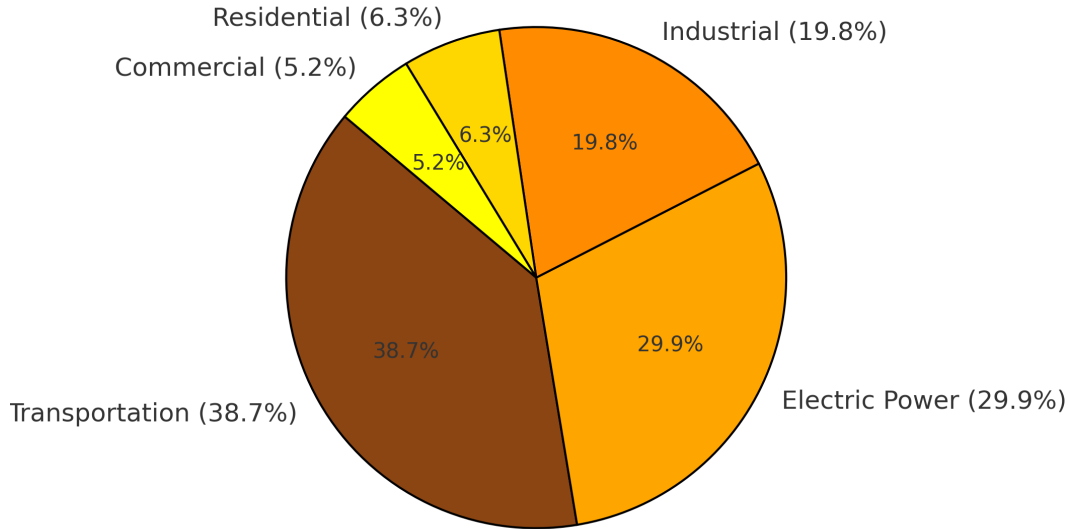


Figure 1.1: Carbon dioxide emissions from energy-related activities, categorized by economic sector in the United States in the year 2024 [14].

Figure 1.2 presents a sector-wise breakdown of U.S. energy-related CO_2 emissions from 2020 to 2024. Over this five-year period, total CO_2 emissions peaked in 2022 at nearly 5,000 million metric tons, before declining modestly in the subsequent years. This trend reflects a partial rebound in emissions following the COVID-19 pandemic and a gradual transition toward cleaner energy sources.

Among all sectors, the transportation sector consistently accounted for the largest share of emissions, with a steady rise from approximately 1,630 million metric tons in 2020 to around 1,848 million metric tons in 2024. This persistent dominance highlights the sector’s significant environmental footprint, primarily driven by gasoline and diesel consumption in road vehicles and aviation.

The electric power sector, which ranked second in emissions, saw a gradual decline from its 2021 peak of approximately 1,553 million metric tons to 1,427 million metric tons in 2024. This drop may be attributed to the increased penetration of renewable energy sources and improved grid efficiency.

Industrial emissions remained relatively stable, averaging close to 950–960 million metric tons throughout the period, while residential and commercial

emissions fluctuated slightly year over year but stayed within the 300–340 and 230–260 million metric ton ranges, respectively. These lower values reflect their relatively smaller contributions, likely influenced by seasonal heating demand and changes in energy efficiency practices.

Overall, the figure demonstrates a modest but observable effort in reducing power sector emissions, while transportation continues to be a key challenge in the U.S. decarbonization pathway.

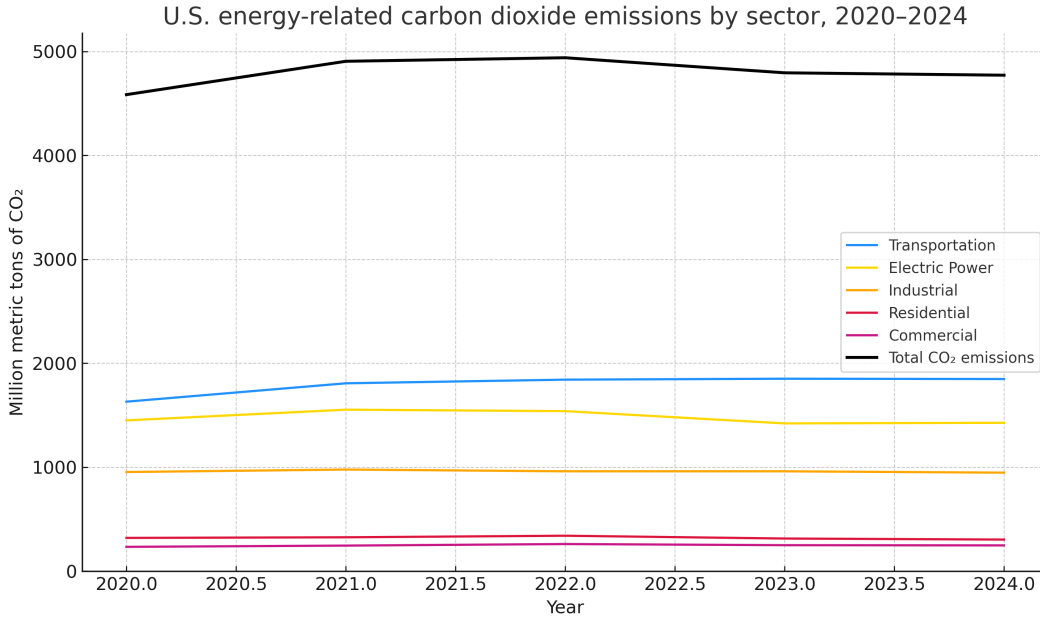


Figure 1.2: U.S. energy-related carbon dioxide emissions by sector, 2020-2024 [15].

To address this issue, development of a grid-connected EV transportation system has been considered as one of the best solutions to help significantly reduce fossil fuel consumption [16], [17]. Therefore, there is a rapid increase in EV sales across the globe that can be attributed to a confluence of factors, including government policy support, improvement in battery technology, more charging infrastructure and new compelling models from EV manufactures. As illustrated in Fig. 1.3, global EV sales have experienced remarkable growth over the past decade, rising from fewer than 1 million units in 2015 to over 17 million units in 2024 [18]. This rapid expansion reflects the growing adoption of EVs across key regions, driven by government incentives, technological

advances, and tightening emissions regulations.

China has remained the dominant market throughout the period, accounting for approximately 65% of global EV sales in 2024 with over 11 million units sold. This growth is largely due to robust domestic policy support and a highly competitive manufacturing ecosystem. Europe’s EV market grew steadily until 2022 and then plateaued at around 3 million units annually. In contrast, the U.S. market showed modest but consistent growth, reaching 1.8 million units in 2024. The rest of the world, including Southeast Asia, Latin America, and the Middle East, collectively saw a sharp rise to 1.3 million units in 2024, indicating an increasingly global shift toward electrified transportation.

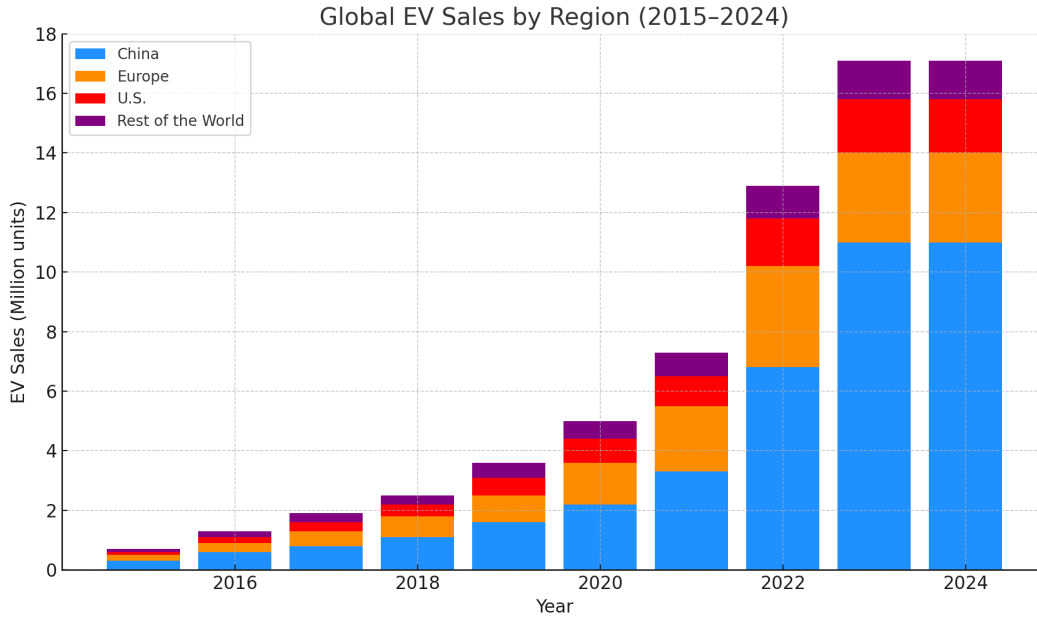


Figure 1.3: Global EV sales by region from 2015 to 2024. Data based on reported sales volumes from China, Europe, the U.S., and other global markets [18].

DC fast and ultra-fast charging infrastructure are being developed to match the driving range of internal combustion engine-based vehicles, and plugging to the power grid facilitates reactive power support, load balance, and integration of renewable energy resources. Moreover, High-Voltage (HV) battery systems are emerging as an attractive power solution for EVs due to their ability to provide ultra-fast charging, and recent commercial EVs such as the Porsche

Taycan and Aston Martin Rapide Type E have revealed their 800Vdc battery technology. Given Canada’s ambitious commitment to reducing greenhouse gas emissions (GHG) by 30% from 2005 levels under the Paris Agreement by 2030, and its goal of achieving net-zero emissions by 2050 in the fight against climate change [19], investigation on recent trends in EV systems and power electronic technology utilized in them becomes of paramount importance.

As EVs continue to gain traction worldwide, the importance of a fast, reliable, and efficient charging infrastructure has grown in parallel. A key enabler in closing the performance gap between EVs and traditional internal combustion engine (ICE) vehicles is the emergence of DC fast and ultra-fast charging technologies. These advanced charging systems have significantly improved the practicality of EVs, allowing for quicker refueling times and extended travel ranges, thereby addressing one of the major barriers to widespread adoption. Beyond simply recharging the battery, modern charging stations also provide additional grid services such as reactive power support, peak load reduction, load balancing, and even integration with renewable energy resources, transforming EVs into dynamic elements of the broader energy ecosystem [20].

Central to the effectiveness of these charging systems is the continued advancement of battery technology. The battery is not only the most expensive component of an EV but also the heaviest, meaning improvements in battery energy density and cost have a direct impact on overall vehicle performance and market competitiveness [21], [22]. As battery capacities have increased, so too has the demand for high-power charging systems capable of replenishing energy quickly and efficiently. Early generations of EVs were limited in both range and charging speed, but today’s models are designed with significantly larger battery packs, requiring the support of high-performance charging infrastructure that can keep pace with user expectations and transportation needs [23].

To meet these evolving requirements, modern EV chargers must be designed with a number of critical performance attributes in mind. High efficiency is essential to reduce energy loss and thermal management requirements. A high power factor and low total harmonic distortion (THD) are necessary

Table 1.1: Charging station classification based on power level.

Type	Location	Input	Power Level	Charging Time
Level-1 (AC)	On-board	120/230 V_{ac}	1.44–1.92kW	11–36 hours
Level-2 (AC)	On-board	208/240 V_{ac}	3.1–19.2kW	2–6 hours
Level-3 (DC)	Off-board	300–600 V_{dc}	50–350kW	<30 min.
Next Gen. (DC)	Off-board	800 V_{dc}	Up to 400kW	$\approx$ 10 min.

to ensure compatibility with grid standards and minimize negative impacts on the electrical supply network. For instance, widely adopted standards such as IEEE 1547-2018 [24] and SAE J2894-1 [25] mandate that the THD of the input current must remain below 5%, and the charger must draw current from the grid at a near-unity power factor. Furthermore, these systems should be compact, lightweight, cost-effective, and reliable, making them suitable for a wide range of applications in both residential and commercial environments.

Broadly, EV chargers can be categorized into two main types: on-board and off-board. OBCs are integrated into the vehicle and allow users to connect directly to the grid using standard AC outlets. These chargers are ideal for home use or locations where low-to-moderate charging speeds are acceptable. Off-board chargers, on the other hand, are standalone external units, typically found in public or commercial locations, that can deliver significantly higher power levels, enabling fast or even ultra-fast charging capabilities.

Charging systems are also often classified by power level, which directly affects charging time, infrastructure requirements, and user experience. Table 1.1 summarizes the typical specifications for each category of charger based on location, input voltage, power delivery, and expected charging duration [22].

As shown in Table 1.1, Level-1 and Level-2 chargers are typically associated with on-board systems. Level-1 charging represents the most basic and widely accessible form, suitable for overnight use in residential settings. However, its slow charging speed, often requiring over a full day for a complete charge, limits its practicality for users with longer daily driving requirements. Level-2 chargers, by contrast, offer a significant improvement in power delivery, making them well-suited for home garages, workplaces, and public parking

areas. These systems can fully recharge most EVs within a few hours and are compatible with standard connector types, such as SAE J1772 in North America and IEC 62196 Type 2 in Europe [26]–[28].

Despite the utility of Level-1 and Level-2 chargers for routine charging needs, their limited power output is insufficient to support the rapid energy replenishment needed for long-distance travel or high-demand commercial applications. This has led to the development and widespread deployment of Level-3 DC fast chargers. These off-board systems are capable of delivering power in the range of 50–350kW, drastically reducing charging times to under 30 minutes in most cases. In addition to speed, off-board chargers reduce the size and thermal burden on the vehicle itself, since the bulky and heavy components required for fast conversion and power handling are housed externally.

Pushing the envelope further, next-generation ultra-fast chargers operating at 800V and above are already entering the market. These systems can deliver up to 400kW of power, potentially recharging compatible EVs in approximately 10 minutes. This level of performance is a crucial step toward matching or even exceeding the refueling speed of conventional gasoline vehicles, making EVs far more appealing for time-sensitive users and fleet operators.

In conclusion, the charging infrastructure supporting EV is becoming increasingly diverse, both in terms of technological capability and application scenarios. OBCs offer flexibility and independence, while off-board systems bring speed and power for demanding situations. As battery technology continues to improve and standards evolve, the synergy between vehicle hardware, charging systems, and the power grid will play a vital role in shaping the future of electric mobility.

1.2.1 Off-Board Battery Chargers

Off-board battery chargers play a vital role in the broader EV charging ecosystem, particularly when it comes to delivering high power for fast and ultra-fast charging applications. Unlike OBCs that are physically integrated into the vehicle, off-board chargers are located externally and typically installed in public spaces, commercial areas, or highway charging stations. This exter-

nal placement allows these systems to overcome the size, weight, and thermal limitations imposed on vehicle-mounted hardware, enabling the delivery of significantly higher power levels. An example of a typical off-board charging configuration is illustrated in Fig. 1.4.

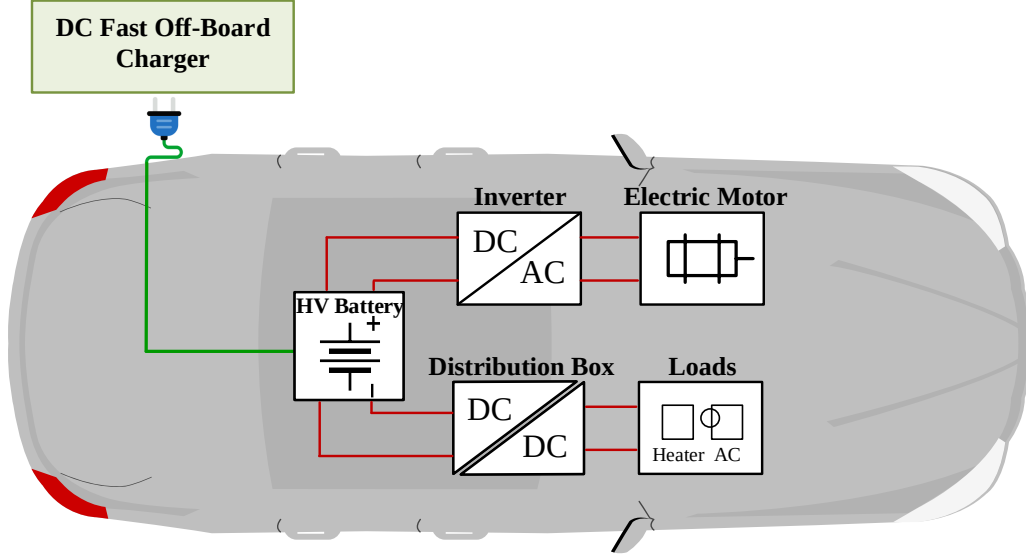


Figure 1.4: Power connections and off-board charging system for HV battery system in EV.

One of the most compelling advantages of off-board chargers is their ability to drastically reduce charging time. These systems are capable of delivering power in the range of 50 kW to over 350 kW, making it possible to recharge most EVs in under 30 minutes. This capability is particularly beneficial in scenarios where time is critical, such as during long road trips, in ride-sharing and taxi fleets, or at high-traffic urban charging hubs. By enabling rapid energy replenishment, off-board chargers significantly reduce one of the most common concerns associated with EV ownership: range anxiety. The availability of fast charging infrastructure gives drivers confidence in their ability to travel longer distances without extensive downtime, making EVs a more practical alternative to ICE vehicles [29].

Off-board chargers also support the deployment of high-voltage battery systems, which are becoming increasingly common in next-generation EVs. Vehicles with 800V architectures, for example, require charging systems ca-

pable of handling higher voltages and currents safely and efficiently. Because these components are housed outside the vehicle, engineers have more design freedom to implement advanced cooling systems, larger magnetic components, and robust control algorithms, without compromising vehicle packaging or weight distribution. As a result, off-board chargers can offer superior thermal performance and higher reliability, particularly under heavy-duty usage.

Strategically placing off-board chargers in public spaces, such as shopping centers, office complexes, and transportation corridors, greatly enhances accessibility and convenience for EV users. This widespread availability also plays a critical role in encouraging EV adoption, particularly among users who do not have access to home charging infrastructure. In densely populated cities where parking is limited or in apartment complexes without dedicated electrical systems, off-board chargers provide a much-needed solution to the logistical challenges of EV ownership. Moreover, many of these public charging stations are equipped with digital interfaces that offer user-friendly features like smart payment systems, real-time availability updates, and V2G communication protocols [22].

Despite their advantages, off-board chargers are not necessarily the ideal solution for every EV owner. For users with predictable driving patterns and the ability to charge at home overnight, the convenience and cost-effectiveness of on-board Level-1 or Level-2 chargers may be more suitable. Off-board chargers often require significant infrastructure investments and can be more expensive to use, especially when operated by third-party charging networks. Additionally, because these systems are exposed to outdoor environments and used by a wide range of vehicles, they must meet stringent reliability, safety, and interoperability standards. Factors that can add to their design and deployment complexity.

In summary, off-board battery chargers are an indispensable component of modern EV infrastructure. Their ability to deliver high power over short periods makes them ideal for fast charging in public and commercial settings. As EV adoption continues to grow and user expectations shift toward faster and more flexible charging options, the role of off-board systems will become

increasingly prominent. Coupled with smart grid capabilities and renewable energy integration, these chargers will not only serve the immediate needs of EV users but also contribute to the development of a more resilient and sustainable energy landscape.

1.2.2 On-Board Battery Chargers

OBCs are a central component in EV powertrain systems, designed to provide the convenience of charging from virtually any standard electrical outlet or AC charging station. As these chargers are physically integrated into the vehicle, they travel with it wherever it goes, enabling flexibility and ease of use. This built-in functionality allows EV owners to recharge their vehicles at home, at work, or in public locations without requiring specialized infrastructure beyond a basic AC power supply. For everyday use, especially for users with predictable daily driving routines and access to overnight charging, OBCs offer a practical, cost-effective, and user-friendly solution [30].

While OBCs generally operate at lower power levels compared to their off-board counterparts, they are more than adequate for typical daily charging needs. Depending on the vehicle and regional power grid, most OBCs offer between 3.3 kW and 22 kW of charging capacity, which can fully recharge a battery over the course of several hours. This aligns well with overnight charging at home or long parking durations at the workplace. In fact, many EV users rarely require fast charging for daily commutes, and therefore prioritize reliability and affordability over speed. As such, OBCs remain the default choice for most EV models and continue to be refined for higher power density, improved efficiency, and greater compatibility with emerging battery systems [22], [30].

A typical OBC power interface consists of two main stages: an AC/DC conversion stage for Power Factor Correction (PFC), and a DC/DC isolated conversion stage for regulating output to the battery pack. This configuration, shown in Fig. 1.5, is designed to operate across a wide range of AC input voltages and frequencies, delivering high-voltage DC output suitable for modern EV battery systems [31]. The need for high voltage gain, compact

size, and thermal efficiency in this dual-stage design poses unique challenges for circuit design, magnetic component optimization, and control algorithm implementation.

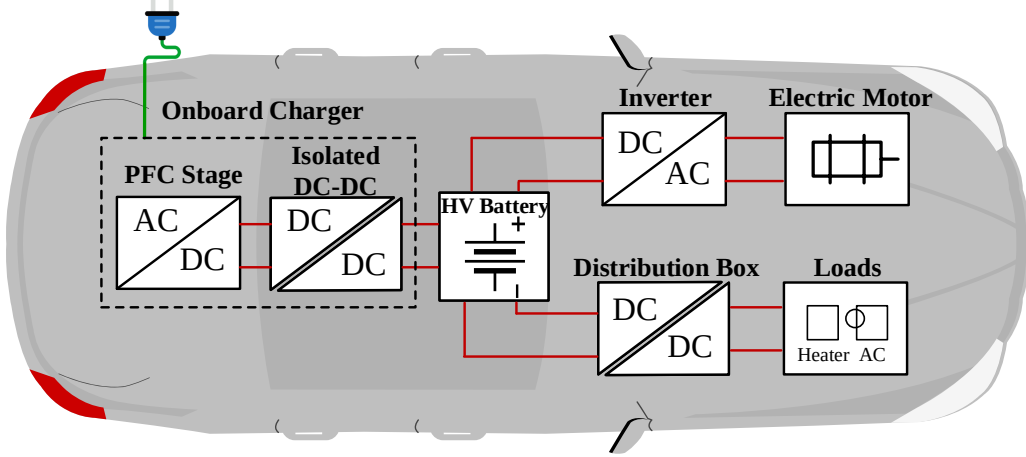


Figure 1.5: Power connections and on-board charging system for HV battery system in EV.

In the context of single-phase AC charging, common in residential applications, the choice between single-stage and two-stage converter architectures becomes particularly relevant. Single-stage converters aim to simplify the system by combining PFC and DC regulation into a single power stage. This approach can offer benefits in terms of compactness and cost, but it introduces design complexity in meeting strict grid compliance standards, especially in maintaining low THD and high input power factor. Two-stage topologies, while slightly larger and more complex, offer better modularity and performance, enabling independent optimization of the AC/DC and DC/DC stages. These systems are generally better suited for high-power OBCs or where grid standards like IEEE Std 1547-2018 or SAE J2894-1 must be rigorously met [24], [25].

Regardless of the architecture, modern OBCs must produce a high-quality sinusoidal input current with very low harmonic distortion, typically less than 5% THD, and maintain a near-unity power factor to minimize stress on the electrical grid. These performance metrics not only ensure compliance with international standards but also improve energy efficiency and reduce interfer-

ence with other grid-connected devices. Output voltage ripple is another key consideration, with typical design targets keeping this below 5% to protect battery health and support stable operation.

Given these demanding requirements, the selection of suitable power converter topologies and control strategies becomes critical. Traditional front-end PFC converters, such as diode bridge rectifiers followed by boost converters, are well-understood but suffer from relatively high losses, particularly at low input voltage conditions. These configurations often require multiple sensors and Phase-Locked Loop (PLL) systems for grid synchronization, adding complexity and cost [32], [33]. To address these limitations, recent developments have explored bridgeless topologies that eliminate the diode bridge, reducing conduction losses and improving overall efficiency.

As EV batteries grow in capacity and voltage, and as user expectations shift toward faster and more efficient charging even at home, OBC design must continue to evolve. Engineers are now developing high-frequency switching techniques, soft-switching resonant topologies, and digital control methods to further enhance performance and minimize system size. In some cases, bidirectional OBCs are being introduced to support emerging applications such as V2G and V2H, which require the charger to reverse power flow and operate safely in both directions [34], [35].

In conclusion, OBCs remain a cornerstone of the EV charging landscape, offering everyday utility, flexibility, and portability. While they are inherently limited in maximum power delivery compared to off-board chargers, their design sophistication, reliability, and seamless user experience make them indispensable for the majority of EV users. The ongoing evolution of AC/DC converter technologies, topologies, and control strategies will be key to enhancing the performance and versatility of OBCs in the years to come. The next sections will examine these converter designs in more depth, focusing on both unidirectional and bidirectional topologies, along with the control methods necessary for stable and efficient operation.

1.3 AC/DC Power Converters for EV Charging

AC/DC power converters constitute a fundamental component of the EV charging infrastructure, acting as the critical interface between the utility grid and the EV's onboard energy storage system. Their principal role is to convert the AC supplied by the grid into DC suitable for charging the high-voltage battery within the vehicle. This energy conversion must be performed with high efficiency, power quality, and reliability to meet the performance demands of modern EVs and to support large-scale grid integration.

The topology and control strategy of the AC/DC converter vary depending on the specific charging architecture. In conventional charging stations, unidirectional converters are typically employed, where power flows solely from the grid to the vehicle. These systems are simpler and more cost-effective but limit functionalities such as grid support or V2G applications. In contrast, bidirectional AC/DC converters enable power flow in both directions, allowing the EV to not only receive energy from the grid but also to return stored energy back to it. This bidirectional capability supports advanced energy management features such as peak shaving, frequency regulation, and the integration of renewable energy sources, contributing to the development of smart grid ecosystems.

Therefore, the design of AC/DC converters is pivotal not only for efficient and safe battery charging but also for enabling future-oriented functionalities that enhance grid flexibility and resilience in an increasingly electrified transportation landscape.

Unidirectional converters facilitate one-way power flow from the grid to the EV, making them suitable for conventional charging systems. In contrast, bidirectional converters support energy flow in both directions, enabling advanced functionalities such as V2G and V2H. These capabilities are vital for future smart grid integration, allowing EVs to act as distributed energy storage units.

This section explores the two primary categories of single-phase AC/DC

converters used in EV charging: unidirectional and bidirectional. Each subsection delves into their respective topologies, operational principles, advantages, and challenges in the context of modern EV charging requirements.

1.3.1 Single-Phase Unidirectional Converters

Single-phase unidirectional AC/DC converters are among the most fundamental components in modern power electronic systems. Their primary role is to convert sinusoidal AC from a single-phase source into regulated DC suitable for a wide range of downstream applications, including battery charging, industrial drives, uninterruptible power supplies (UPS), and renewable energy interfaces [36], [37]. Although often associated with EV charging systems, their applicability extends well beyond that domain. The focus of this section is to analyze the key topologies, operational principles, and performance trade-offs involved in the design of single-phase uni-directional converters, with particular attention to power factor correction, efficiency, harmonic reduction, and control complexity.

Power Factor Correction

A critical requirement in single-phase AC/DC converter design is maintaining high power quality at the interface with the electrical grid. This is typically achieved through PFC, which ensures that the input current is sinusoidal and in phase with the voltage. Poor power factor and high THD can lead to increased losses in the transmission system, over-dimensioned infrastructure, and regulatory non-compliance [38].

PFC techniques can be categorized into passive and active methods. Passive PFC uses fixed inductive and capacitive components to filter harmonics, offering simplicity and ruggedness at the cost of increased size, weight, and limited dynamic response [39]. Active PFC, in contrast, employs high-frequency switching and feedback control to dynamically shape the input current waveform. This method achieves superior power quality, higher efficiency, and better performance under varying load conditions but introduces complexity in both control and hardware design [40]. Illustrations of these two categories

are shown in Fig. 1.6.

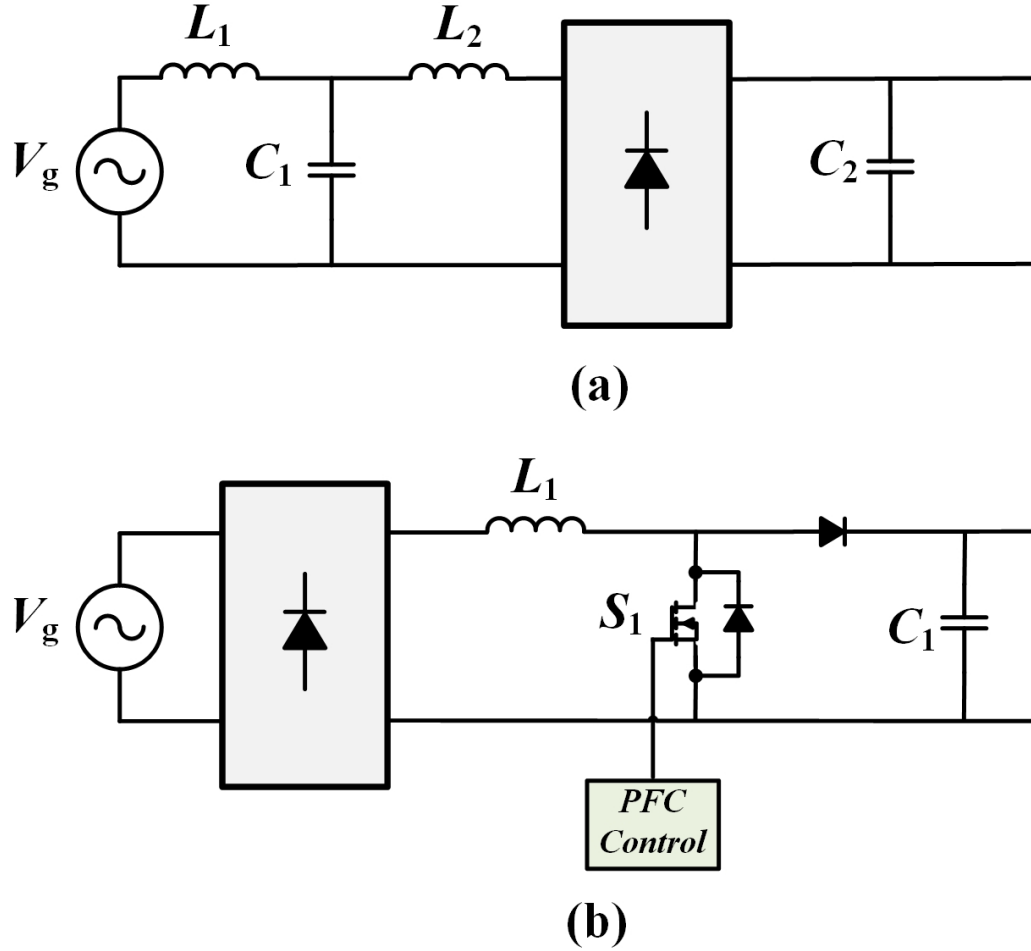


Figure 1.6: Types of PFC: (a) Passive PFC, (b) Active PFC using a boost converter.

Diode Bridge with Two-Level Boost Converter

One of the most common topologies for single-phase AC/DC conversion is the combination of a full-bridge diode rectifier and a two-level boost converter. The diode bridge performs the initial rectification, producing a pulsating DC voltage, while the boost stage regulates the output to a desired level and incorporates active PFC through controlled switching. Fig. 1.7 illustrates the configuration.

This topology is relatively simple and cost-effective and can achieve high efficiency under nominal operating conditions. The boost converter ensures

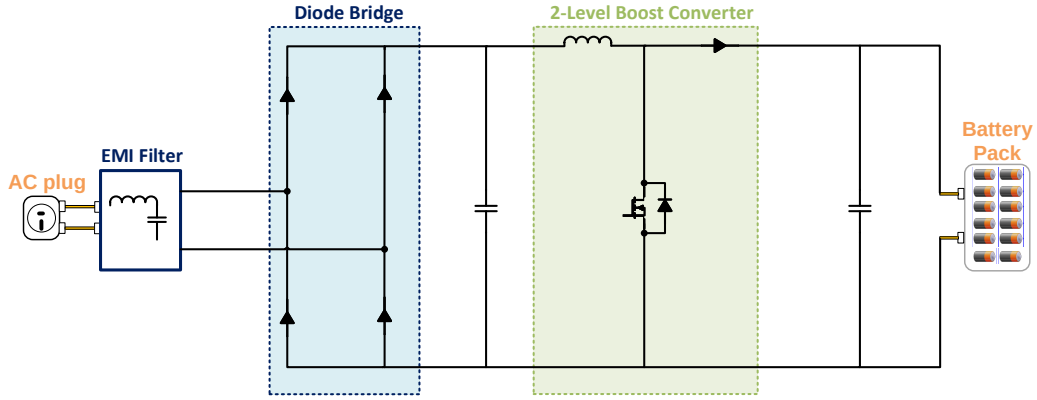


Figure 1.7: Diode Rectifier with Two-Level Boost Converter.

low input current distortion and unity power factor by shaping the current through modulation techniques such as average current mode control. However, the diode bridge introduces conduction losses due to forward voltage drops and contributes to harmonic distortion. Moreover, the two-level boost stage places high voltage stress on switches and requires large passive components, especially under low-line conditions [41], [42].

Diode Bridge with Three-Level Boost Converter

To improve upon the limitations of two-level converters, three-level boost converters are employed. As shown in Fig. 1.8, this topology adds an intermediate voltage node and additional switching devices to divide the voltage stress across components.

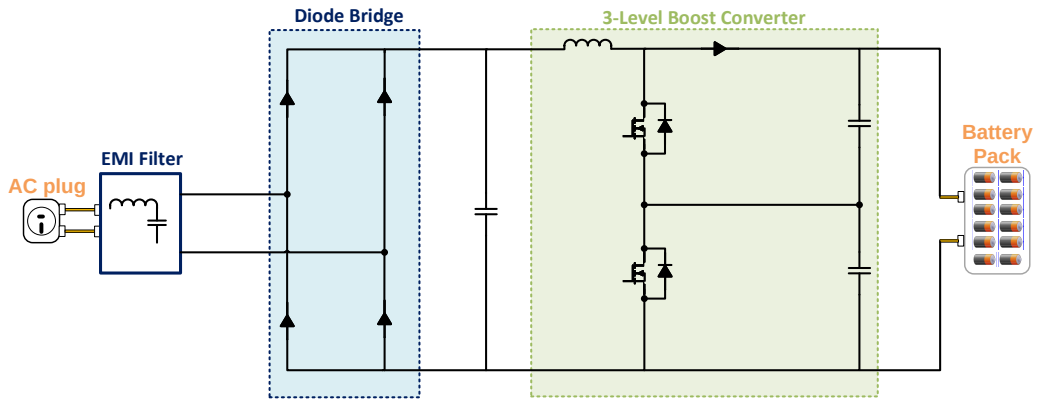


Figure 1.8: Diode Rectifier with Three-Level Boost Converter.

The three-level design reduces the voltage stress on each switch and allows the use of devices with lower voltage ratings, which typically exhibit lower conduction and switching losses. It also improves output voltage quality and reduces electromagnetic interference (EMI) due to smoother voltage transitions. However, these benefits come at the cost of increased circuit complexity, more sophisticated gate driver requirements, and the need for precise voltage balancing and timing control [43], [44].

Isolated Resonant Converters

Isolated resonant converters introduce galvanic isolation between the input and output stages and utilize soft-switching principles to minimize switching losses. Fig. 1.9 illustrates a typical implementation with a full-bridge rectifier followed by a resonant DC/DC stage.

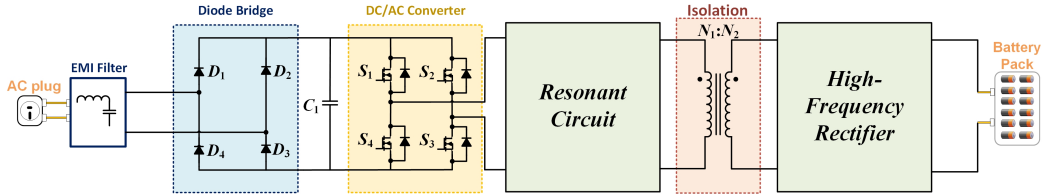


Figure 1.9: Full-bridge rectifier with isolated resonant circuit.

Resonant topologies such as LLC or CLLC enable zero-voltage or zero-current switching, which significantly improves efficiency at high frequencies and reduces the size of magnetic and filter components. Additionally, the isolation helps meet safety standards and supports bidirectional extension in more advanced applications. However, resonant converters require careful tuning and can be sensitive to parameter variation and load changes, making their control more complex than conventional pulse-width modulated converters [45], [46].

Bridge-less Topologies

Bridge-less PFC converters aim to improve efficiency by eliminating the front-end diode bridge and reducing the number of conduction paths. Fig. 1.10

shows a basic implementation where active switches handle the full rectification and boost operation.

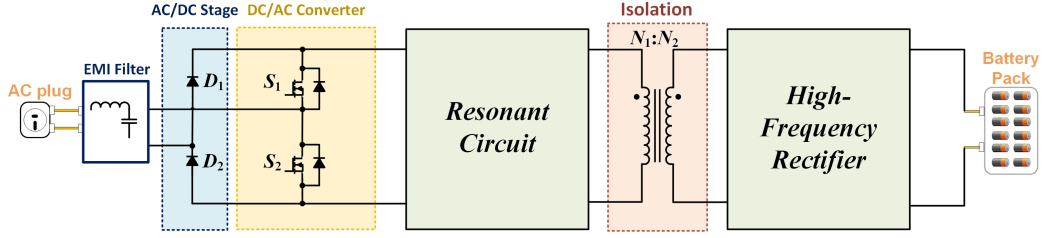


Figure 1.10: AC/DC converter with bridge-less topology.

These topologies reduce conduction losses and heat generation, allowing for improved thermal management and higher power density. However, the elimination of passive diodes introduces control challenges. Current paths are more complex, and timing must be precisely managed to prevent shoot-through and discontinuities in current flow. Furthermore, these converters are more sensitive to parasitic elements in layout and require careful electromagnetic compatibility (EMC) design [47], [48].

Totem-Pole PFC Converter

An evolution of the bridge-less topology is the totem-pole PFC converter, which uses synchronous switches to perform rectification and boost operations in a highly efficient and compact form. A simplified configuration is shown in Fig. 1.11.

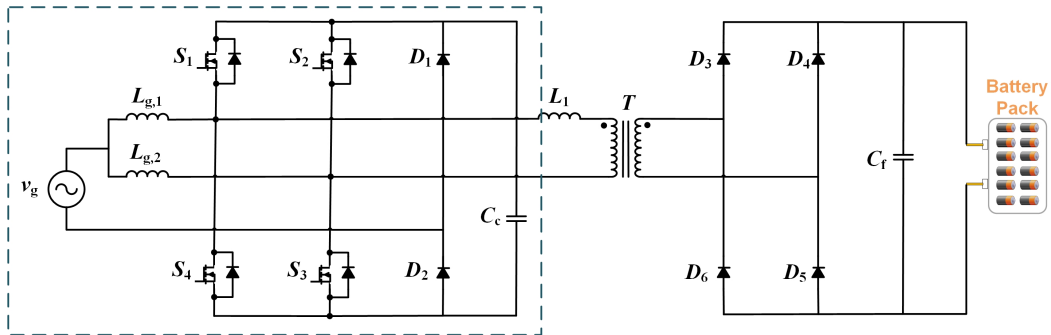


Figure 1.11: AC/DC converter based on totem-pole bridge-less topology.

Totem-pole converters are particularly well suited to wide-bandgap devices such as GaN and SiC MOSFETs, which support high-speed switching with low

losses. These converters can operate in continuous conduction mode (CCM) or critical conduction mode (CRM), achieving very high efficiency and near-unity power factor across a wide load range [49], [50]. Despite their performance, the fast switching and strict timing requirements demand sophisticated controllers, precise dead-time management, and highly optimized PCB layouts [51].

Multi-Level Converters

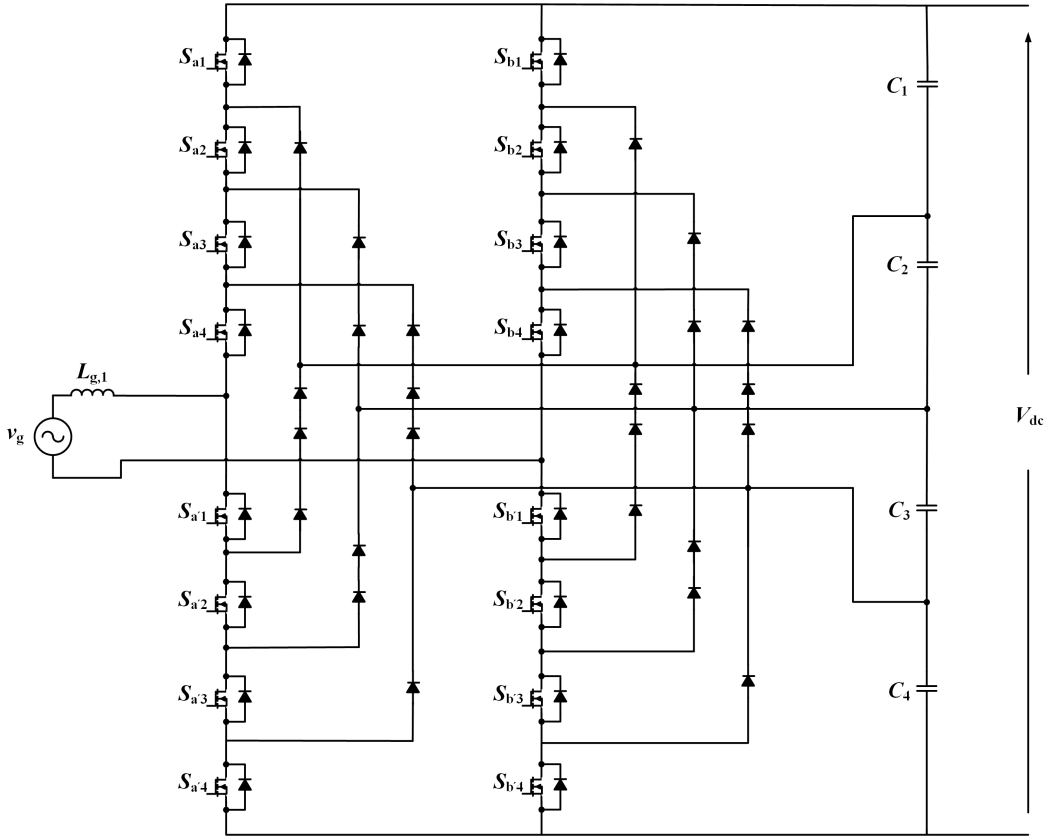


Figure 1.12: A diode-clamp five-level AC/DC converter.

Multi-level converters offer another approach for improving efficiency and power quality by generating stepped output voltages that approximate a sine wave. Fig. 1.12 illustrates a diode-clamped five-level converter as one representative topology.

By dividing the voltage across multiple switching stages, multi-level converters reduce voltage stress, switching losses, and filter requirements. They are particularly attractive in high-power, high-voltage systems where grid com-

patibility and waveform fidelity are critical [52], [53]. However, they involve a large number of components and require advanced modulation techniques, such as space vector modulation or phase-shifted pulse-width modulation, increasing the control burden and cost.

1.3.2 Recent Unidirectional AC/DC Converter Topologies

Beyond the foundational converter architectures introduced in the preceding sections, including two-level and three-level boost converters, isolated resonant stages, bridgeless configurations, and totem-pole topologies, recent research has focused on enhancing performance, reducing component count, and improving compatibility with evolving EV charging standards. These investigations build upon conventional designs but aim to address persistent limitations such as high conduction losses, poor soft-switching, bulky passive components, and challenges in high-voltage scalability.

In the context of single-phase OBCs, AC/DC conversion is generally realized using either two-stage [54], [55] or single-stage architectures [56], [57]. Regardless of the approach, adherence to standards such as IEEE 1547-2018 [24] and SAE J2894-1 [25] necessitates a high-quality sinusoidal input current with high power factor and minimal harmonic distortion.

Boost-type PFC converters are widely used as front-end stages in EV chargers due to their straightforward structure and effective current shaping capability. Traditional implementations often include a diode bridge rectifier followed by a boost converter; however, this structure introduces high conduction losses, particularly at low line conditions, where the diode bridge alone can account for 30–50% of total losses [31]. Furthermore, these converters typically operate in Continuous Conduction Mode (CCM), which necessitates a Phase-Locked Loop (PLL) for proper control [32], [33].

To address these limitations, various bridgeless topologies have been proposed in the literature. These designs aim to eliminate the diode bridge to reduce losses and improve efficiency, while still achieving compliance with power quality standards. In the isolated DC-DC stage, resonant topologies such as

LLC and CLLC are commonly employed due to their ability to achieve soft-switching and high efficiency [58], [59]. Among these, the CLLC topology is often preferred for its superior voltage regulation and lower output ripple due to its dual inductor structure.

Several single-stage OBC architectures have also been proposed to reduce component count and improve power density. For example, [60] introduced a full-bridge diode rectifier with active clamp and interleaved resonant circuits, while [34] proposed a PFC OBC without an intermediate DC-link that achieves soft-switching across the AC line. A bridgeless Cuk-type converter with a series ripple compensator was presented in [61], though it lacked soft-switching capability. A resonant single-stage OBC with inherent PFC was discussed in [57]. While many of these topologies are tailored for 300–400 V_{dc} battery systems, HV battery applications around 800 V_{dc} demand greater voltage gain and introduce higher voltage stress across components.

A persistent design challenge in all these systems is the use of large electrolytic capacitors for DC-link and output filtering to suppress low-frequency voltage ripple. While effective, these capacitors suffer from poor reliability, short life span, and thermal sensitivity. To reduce capacitance requirements, advanced ripple reduction techniques have been investigated, including Voltage Ripple Reduction Circuits (VRRCs) [62], [63], Synchronous Rectification (SR) [64], and harmonic injection methods [65]. However, these techniques often come with trade-offs such as increased complexity, additional conduction losses, and open-loop control dependence.

The VRRC approach typically introduces extra inductors, HV capacitors, and semiconductor switches to absorb ripple energy, but adds conduction loss. SR techniques rely on precise synchronization with the AC line via PLLs and are often implemented as open-loop controllers, increasing sensitivity and control difficulty. Harmonic injection strategies deliberately introduce counter-acting harmonics into the control signal, which requires accurate sensing and can increase both design complexity and cost.

In summary, although numerous unidirectional AC/DC converter designs have been proposed for EV OBCs, many still suffer from significant limita-

tions: high voltage stress on semiconductors, poor soft-switching performance, reliance on lossy diode bridges, use of bulky electrolytic capacitors, and insufficient compatibility with HV battery systems. These challenges motivate the need for a new converter topology that reduces switch stress, eliminates the bridge rectifier, ensures soft-switching, and operates with minimal capacitance through an integrated closed-loop ripple reduction strategy, all while delivering high efficiency and grid-compliant performance.

1.3.3 Single-Phase Bidirectional Converters

Single-phase bidirectional AC/DC converters are essential in modern power systems that demand controlled energy flow in both directions between AC and DC domains. Unlike conventional unidirectional converters, these systems are capable of operating in rectification mode (AC to DC) as well as inversion mode (DC to AC), enabling dynamic interaction with the grid and local loads. This bidirectional capability is particularly valuable in applications such as battery energy storage systems, grid-integrated renewable generation, and uninterruptible power systems (UPS), where energy must be both consumed and delivered depending on system requirements. This section examines various converter architectures, including both two-stage and single-stage configurations, with a focus on their topological structures, functional characteristics, performance benefits, and inherent trade-offs.

Two-stage Bidirectional Converter Structures

In the two-stage configuration, the first stage typically performs AC/DC conversion with PFC, while the second stage handles DC/DC conversion. This approach enables better control, isolation, and adaptability over a wide input/output voltage range.

Bidirectional AC/DC Power Factor Correction

Half-Bridge PWM Converter The half-bridge pulse-width modulation (PWM) converter offers a simple solution for bidirectional PFC. In rectification mode, when gate signals are deactivated, the converter utilizes body diodes of

switches S_1 and S_2 for passive conduction. For instance, when the AC voltage is positive, current flows through S_1 's body diode and charges capacitor C_1 . Conversely, for negative AC voltage, S_2 's diode conducts, charging capacitor C_2 . In inversion mode, active modulation of the switches generates a sinusoidal output current in phase with the AC voltage.

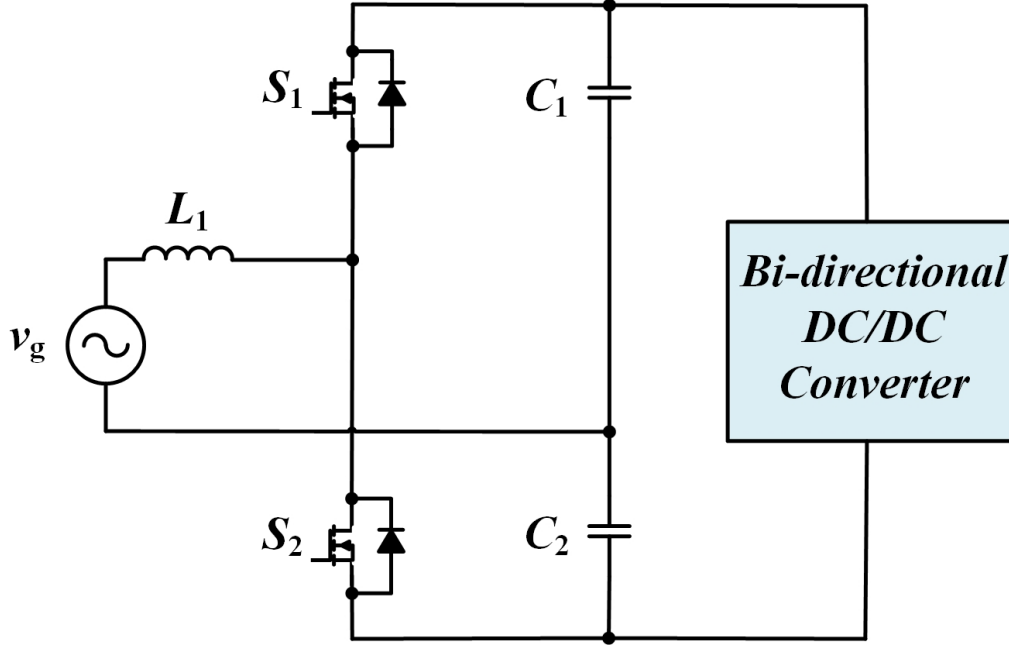


Figure 1.13: Half-bridge PWM converter as PFC.

This topology is cost-effective and easy to implement but suffers from higher input current distortion and greater component stress, necessitating larger filter components.

Full-Bridge PWM Converter The full-bridge PWM converter consists of four switches (S_1 to S_4). During passive rectification, the body diodes of opposing switch pairs conduct, charging the output capacitor. Under active control, the converter modulates the switches to synchronize input current with grid voltage, improving the power factor and current waveform.

Although more complex than the half-bridge, this configuration reduces component stress and harmonic distortion, leading to better performance at higher power levels.

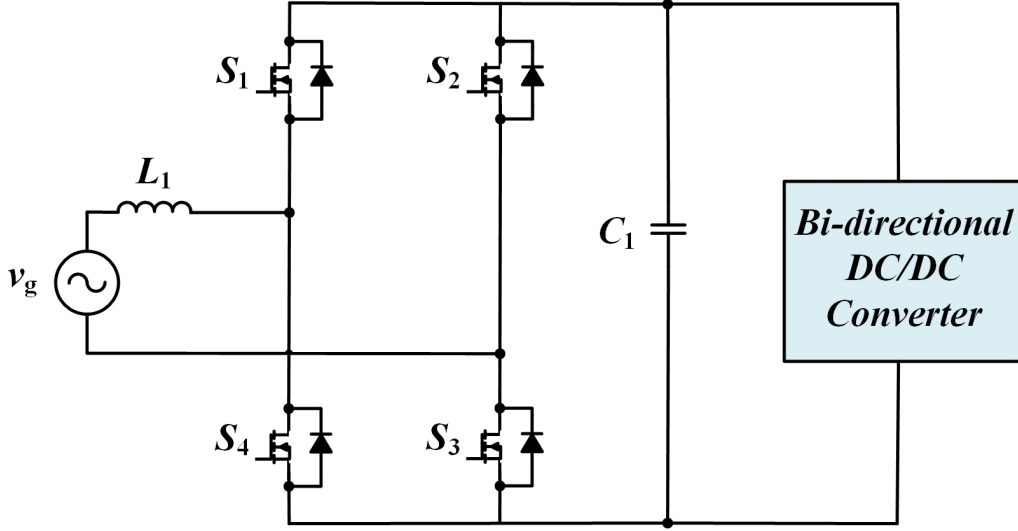


Figure 1.14: Full-bridge PWM converter as PFC.

Three-Level PWM Converter The three-level (TL) PWM converter enhances performance by synthesizing multiple voltage levels at its output. It employs additional switches and diodes, enabling intermediate voltage steps and improving the quality of the AC waveform. In rectification mode, it operates similarly to the full-bridge but with reduced voltage stress on components.

The TL structure supports reduced filtering requirements and improved electromagnetic compatibility (EMC), though it increases circuit complexity and control demands.

Bidirectional DC/DC Converter Topologies

In two-stage converter systems, the bidirectional DC/DC stage is responsible for regulating voltage between the rectified DC bus and the EV battery. It ensures proper charging voltage, enhances power quality, and allows controlled discharging back to the grid or load during V2G or V2H operations. Several topologies have been developed to meet these goals.

Dual Active Bridge (DAB) The DAB converter comprises two full-bridge inverters connected via a high-frequency transformer. In forward mode, the first bridge produces a high-frequency AC waveform, which is transformed and rectified by the second bridge. The process is reversed in the opposite direction

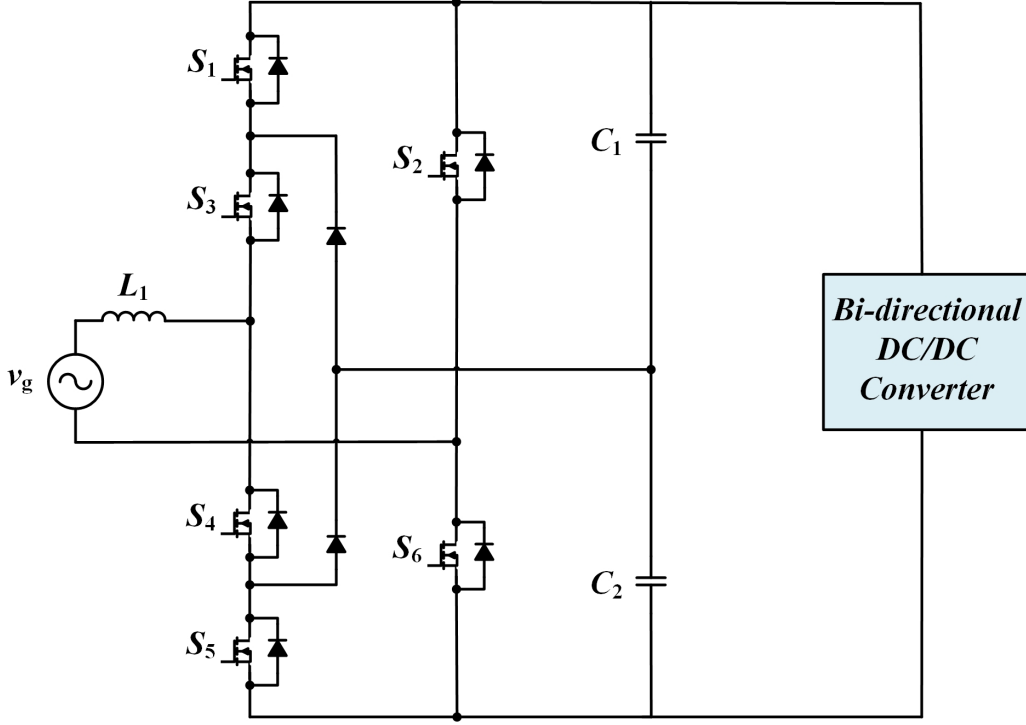


Figure 1.15: Three-Level converter as PFC.

for power flow reversal.

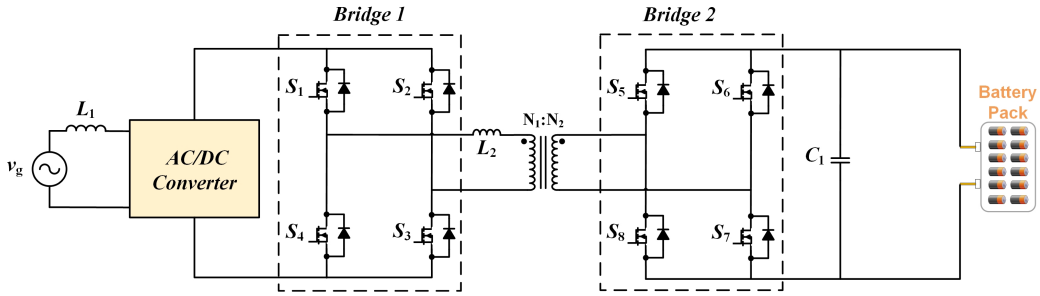


Figure 1.16: Dual active bridge bi-directional converter.

DABs allow for galvanic isolation and soft-switching operation, which minimizes losses. However, reactive power circulation and limited ZVS range at low load conditions are challenges in their design.

Three-Level Bidirectional Converter The TL bidirectional converter reduces switch voltage stress and improves output voltage ripple characteristics. The topology uses six switches and can be designed to incorporate active neutral-point balancing techniques for stable operation.

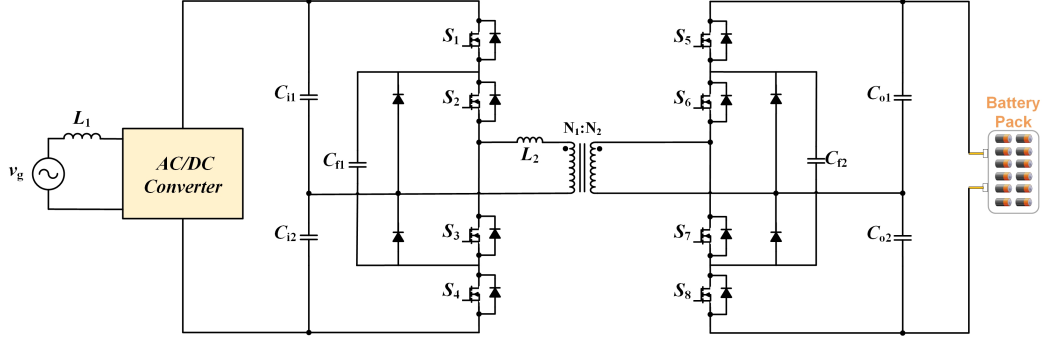


Figure 1.17: Three-level bi-directional converter.

It is more complex than traditional two-level converters but offers improved efficiency and control, especially in medium voltage applications.

Four-Switch String Structure This topology splits the input voltage stress between switch pairs, reducing the requirement for HV-rated devices. It operates in half-wave rectification under one polarity and switches current through a resonant tank during the other half.

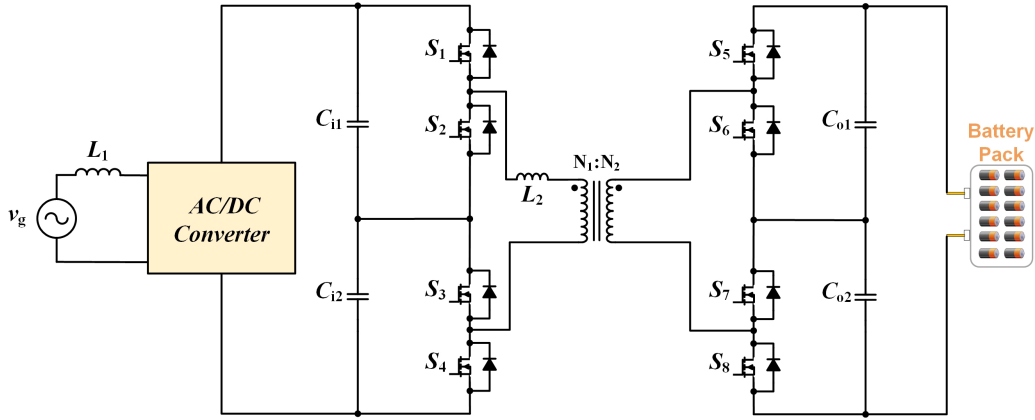


Figure 1.18: Four-switch string structure bi-directional converter.

A drawback is the appearance of high-frequency ripple on the load side, which may require more elaborate filtering strategies.

Single-Stage Bidirectional Converter Structures

Single-stage bidirectional converters offer a compact solution by integrating PFC and DC/DC conversion into a unified architecture. While advantageous

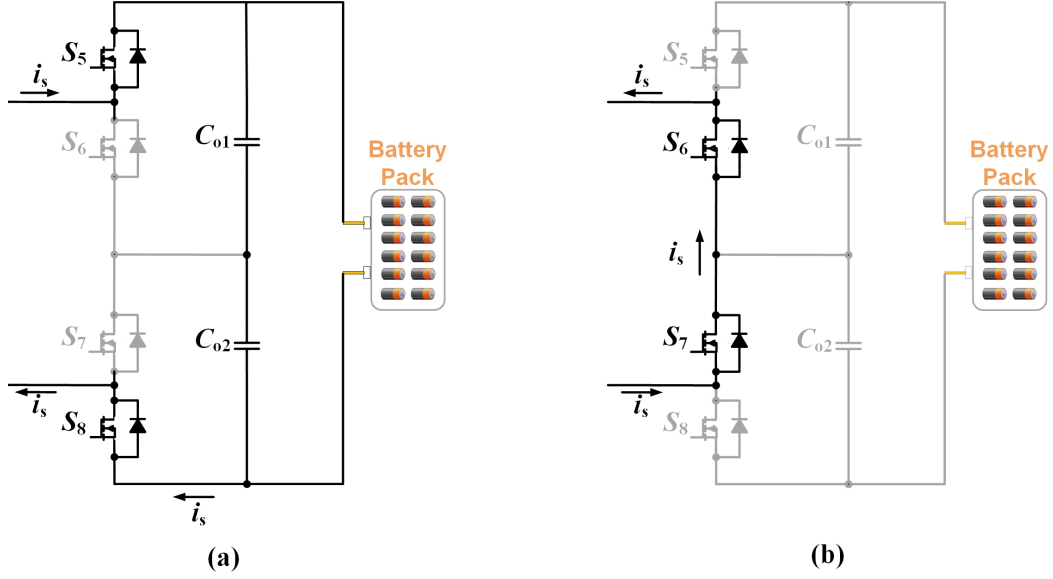


Figure 1.19: Ripple characteristics of the four-switch string converter in rectifier mode.

in size and cost, they often require advanced modulation and control schemes to achieve efficiency comparable to two-stage systems.

DAB-based Matrix Converter This architecture performs direct AC-AC conversion via high-frequency modulation and uses transformer isolation. It allows soft-switching and achieves compactness by avoiding the need for a bulky DC-link.

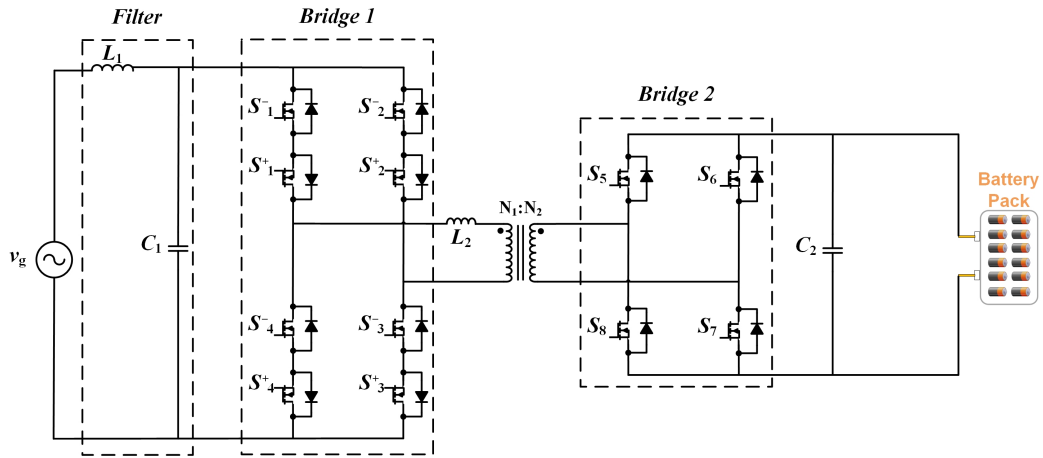


Figure 1.20: Bi-directional DAB-based matrix converter.

Despite high power density, the matrix converter demands complex gate

driving and synchronization control, making it suitable for systems where high performance justifies the design complexity.

Totem-Pole Bi-directional AC/DC Converter A totem-pole topology uses active switches to replace the conventional diode bridge, resulting in improved conduction efficiency. Its symmetrical design facilitates bi-directional operation and enhances performance in continuous conduction mode (CCM).

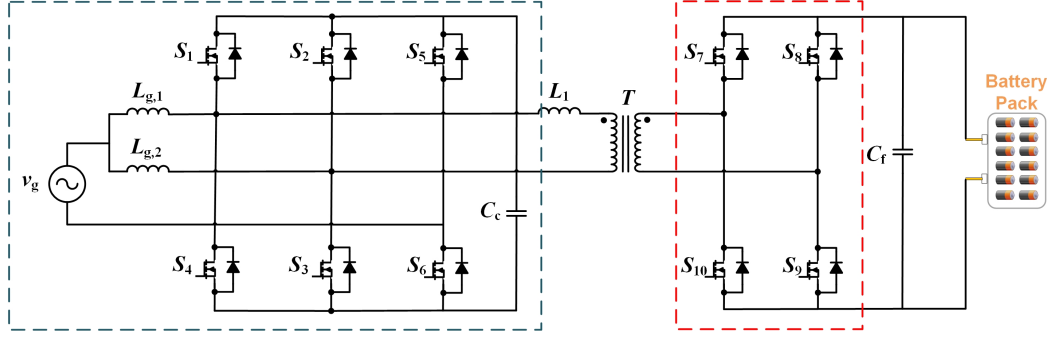


Figure 1.21: Totem-pole bi-directional AC/DC converter.

While simpler in control compared to matrix converters, the totem-pole design must still manage the bi-directional current path and switching transitions carefully to maintain high efficiency and reliability.

1.4 Recent Bidirectional AC/DC Converter Topologies

In addition to the fundamental bidirectional AC/DC converter topologies discussed earlier, a growing body of research has explored more advanced architectures tailored specifically for EV charging applications. While conventional two-stage and single-stage converters form the basis for bidirectional power flow, recent literature introduces a range of innovative designs that aim to improve efficiency, reduce component count, enhance control flexibility, and support grid-interactive features such as V2G and V2H. These studies address critical challenges including wide voltage gain requirements, soft-switching across operating modes, high-frequency isolation, and compliance with grid power quality standards. This section reviews notable developments in the

field, highlighting both the evolution of established configurations and the emergence of novel solutions optimized for bidirectional EV charging infrastructure.

Bidirectional OBCs are typically implemented using either single-stage or two-stage converter topologies. Single-stage designs offer benefits such as higher power density and reduced component count, but often suffer from increased output voltage ripple and more complex control due to the tight coupling of PFC and isolation [57], [66]. In contrast, two-stage designs decouple the AC/DC and DC/DC functions, allowing for optimized control and improved power quality, albeit at the cost of increased size and complexity [66]. The front-end AC/DC PFC stage is responsible for shaping the input current and reducing THD, while the isolated DC/DC stage provides galvanic isolation and voltage regulation. To enhance performance, modern designs frequently employ active PFC configurations such as half-bridge, full-bridge, and three-level structures [31], [67], [68]. Resonant DC/DC stages, particularly those using the CLLC topology, are widely favored for their soft-switching characteristics and high efficiency.

Several bidirectional converter topologies have been explored in recent literature. For example, a boost-inductor-less, electrolytic-capacitor-less single-stage converter based on Dual Active Bridge (DAB) was proposed in [69]. A two-stage interleaved bridgeless buck-boost PFC converter was developed in [70] to improve efficiency and reduce ripple, although it required a complex control system. A Zero-Current Switching (ZCS) current-fed full-bridge (CFFB) converter was introduced in [71] as a compact high-efficiency solution.

Further designs include a single-stage interleaved totem-pole AC/DC converter with high-frequency isolation and minimal component count [64], and a DCM-based single-stage converter with active ripple reduction tailored for HV applications [72]. In [73], an electrolytic capacitor-less bidirectional charger for V2G/V2H was proposed, improving reliability through ZCS operation. Adaptive modulation for improved power density and reliability was discussed in [74], while [75] proposed a charger with multistep constant current charging to improve efficiency and flexibility. An isolated wide-output-range bidirectional

converter was introduced in [76], though it posed challenges in control and consistency across varying voltage levels.

Despite these advances, several limitations persist. Many existing designs rely on electrolytic capacitors, which reduce system lifespan and reliability. Some topologies are optimized for 300–400 V_{dc} systems, making them unsuitable for newer HV EV platforms. Other challenges include high voltage stress on components, hard-switching operation, complicated control strategies, and large low-frequency output ripple.

These challenges underscore the need for a new bidirectional converter architecture that supports HV operation, minimizes component stress, eliminates electrolytic capacitors, ensures soft-switching in both directions, and simplifies ripple reduction without added circuitry. Such advancements are critical for enabling robust, compact, and reliable EV OBC systems with full grid-interactive functionality.

1.5 Storage Capacitance Reduction in AC/DC Power Converters

Optimizing storage capacitance in AC/DC power converters is critical in high-performance, space-constrained applications such as EVs, aerospace systems, and compact industrial equipment. Traditionally, large electrolytic capacitors are used to buffer energy, suppress low-frequency voltage ripple, and stabilize the DC output. However, despite their functional utility, these capacitors introduce several drawbacks that limit converter reliability, compactness, and longevity.

Electrolytic capacitors are often the bulkiest components in the system, constraining the physical design and adding significant weight, an issue especially problematic in mobile platforms like EVs. They also suffer from poor thermal performance and short operational lifespans, particularly under elevated temperatures, making them one of the most failure-prone elements in a converter. Over time, degradation due to electrolyte evaporation leads to increased ESR and reduced capacitance, resulting in worsened ripple suppression

and greater stress on other components.

From a sustainability perspective, the production and disposal of electrolytic capacitors involve hazardous materials, contributing to electronic waste and environmental concerns. As a result, there is growing interest in reducing or eliminating them from converter designs.

Replacing electrolytic capacitors with film capacitors or using advanced ripple reduction techniques, such as active ripple cancellation, harmonic injection, or interleaved control, can significantly improve thermal stability, reliability, and system lifetime. Although film capacitors are more expensive, they offer superior performance in demanding conditions.

Minimizing storage capacitance not only enhances power density and reliability but also supports broader economic and environmental goals. For EV charging systems, where space, efficiency, and durability are paramount, this design strategy offers a compelling path toward more resilient and sustainable power electronics.

1.5.1 Different Types of Capacitors

AC/DC power converters incorporate a diverse range of capacitors, each optimized for distinct roles based on their characteristics. Among the most common are electrolytic, film, and ceramic capacitors, each offering trade-offs in terms of capacitance density, reliability, and frequency performance.

Electrolytic Capacitors

Electrolytic capacitors are favored for their high capacitance in a relatively compact form, making them suitable for buffering and smoothing voltage ripples in high-power systems. These capacitors utilize an electrolyte to maximize energy storage per volume, often positioning them in the input/output stages of converters.

Despite their advantages, electrolytic capacitors are limited by thermal sensitivity, aging effects, and drift in capacitance values over time. These issues necessitate regular maintenance and create challenges in high-reliability



Figure 1.22: Electrolytic Capacitor [77].

applications. Thus, while they are practical for bulk capacitance, their use in advanced systems is increasingly scrutinized.

Film Capacitors

Film capacitors utilize thin plastic dielectric films and are recognized for their long operational life, stability, and robustness. With low ESR and high dielectric strength, they are well-suited for environments demanding thermal resilience and low-loss energy delivery.

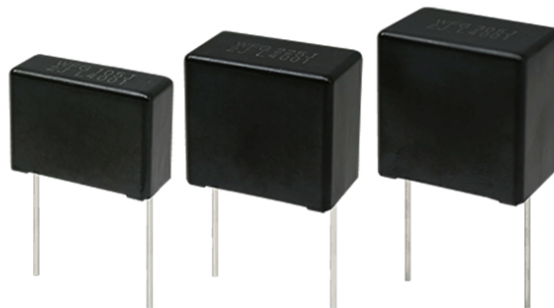


Figure 1.23: Film Capacitor [78].

Although they offer superior reliability compared to electrolytics, film capacitors generally require more physical space to deliver equivalent capacitance. This makes them ideal for applications prioritizing endurance over miniaturization, such as long-lifespan energy systems.

Ceramic Capacitors

Ceramic capacitors, built from dielectric ceramics, offer compact size and excellent high-frequency characteristics. They are non-polarized and stable over wide temperature ranges, making them valuable for noise suppression, bypassing, and filtering.



Figure 1.24: Ceramic Capacitor [79].

Their lower capacitance compared to electrolytic types limits them in bulk energy storage applications, but they are unmatched in surface-mount applications requiring minimal parasitic effects and long-term stability.

1.5.2 Voltage Ripple Reduction

Minimizing voltage ripple is a critical goal in the design of AC/DC converters, especially in high-efficiency systems like EVs, where stability and long-term reliability are paramount. Ripple refers to the unwanted AC component superimposed on the DC output, which can lead to increased stress on circuit elements, reduced power quality, and potential degradation of downstream components such as batteries or sensitive electronics.

Traditionally, large electrolytic capacitors have been deployed to attenuate these ripples. However, these components are bulky, temperature-sensitive, and prone to aging—traits that limit their effectiveness in compact, long-lasting power systems. As such, new strategies are being adopted to reduce

Parameter	Electrolytic Capacitors	Film Capacitors	Ceramic Capacitors
Lifespan (hours at rated temperature)	2,000 to 5,000 hours	10,000 to 100,000 hours or more	Often lasts the lifetime of the device
Cost (per unit) HV application	Relatively low; \$0.10 to \$5.00	Average; around \$50.00	Generally High; above \$100.00
Capacitance Range	0.1 μF to several Farads	up to few hundred μF	Few pF to μF
Voltage Rating	Up to 500V or more	Up to 1000V or more	Usually below 250V
Temperature Stability	Decreases over time/temperature	Good across a wide range	Decrease over temperature
Size	Larger for high values	Larger for high capacity/voltage	Smaller for low values
Tolerance	$\pm 20\%$ or worse	$\pm 5\%$ or better	$\pm 0.1\%$ to $\pm 20\%$
Frequency Response	Poor at high frequencies	Good at high frequencies	Excellent at high frequencies
ESR	Higher; varies with type	Lower; varies with type	Generally very low

Table 1.2: Comparative analysis of electrolytic, film, and ceramic capacitors.

reliance on electrolytics by minimizing ripple through alternative circuit techniques. These approaches also enable the use of more robust capacitor technologies like ceramics or films.

Some of the most widely used methods include voltage ripple reduction circuits (VRRCs), synchronous rectification, harmonic injection, and advanced switching strategies. These solutions contribute not only to ripple suppression but also enable smaller form factors and higher power densities, key enablers for EV applications and other power-sensitive systems.

Voltage Ripple Reduction Circuits

VRRCs are auxiliary circuits integrated into power converters to suppress voltage fluctuations at the DC output. These designs often incorporate passive components, like inductors and capacitors, as well as active elements such as transistors, arranged in ways that enhance filtering effectiveness.

Figure 1.25 illustrates three popular VRRC topologies: a simple low-pass

filter (a), a common mode choke-based filter (b), and a capacitance multiplier circuit (c). Each design achieves ripple reduction through different principles. The low-pass filter relies on its natural impedance characteristics to block high-frequency ripple. The common mode choke suppresses noise shared across lines. Meanwhile, the capacitance multiplier emulates a much larger capacitance at the output by leveraging a transistor and a small capacitor.

In the capacitance multiplier shown in Fig. 1.25.c, transistor S_1 modulates the current drawn from the input capacitor C_1 , effectively reducing the ripple current seen by the output. The apparent capacitance is multiplied by the current gain factor (β) of the transistor, offering ripple attenuation comparable to that of much larger capacitors, without the added bulk.

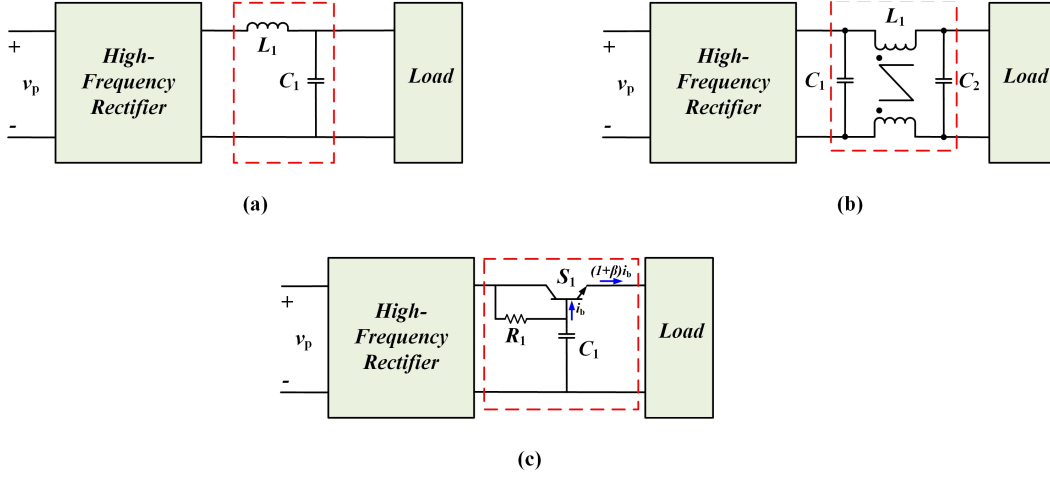


Figure 1.25: Popular voltage ripple reduction circuits: (a) low-pass filter, (b) common mode choke filter, (c) capacitance multiplier.

Despite their benefits, VRRCs introduce trade-offs. Incorporating additional filtering elements increases system size and may marginally reduce efficiency due to passive losses. Furthermore, at higher switching frequencies, designers must mitigate parasitic inductance and capacitance, which can degrade performance or introduce unwanted resonances. Nonetheless, VRRCs remain a cost-effective and widely accepted solution for improving DC output quality in converter designs.

Synchronous Rectification

Synchronous rectification (SR) enhances converter efficiency and reduces voltage ripple by replacing traditional diodes with actively controlled switching devices such as MOSFETs or IGBTs. While diodes conduct unidirectionally with a forward voltage drop, synchronous switches exhibit far lower conduction losses, especially at high currents and low voltages.

In SR, the switching devices are precisely synchronized with the AC input waveform. During the appropriate conduction interval, a MOSFET is turned on in place of a diode, significantly reducing forward losses. This also allows for more continuous and predictable current flow, minimizing ripple in the resulting DC output.

The benefits of SR are best illustrated in high-frequency applications or low-output voltage systems, where diode drops account for a larger proportion of overall power loss. Additionally, SR circuits allow better control over the timing and shape of the output waveform, yielding smoother voltage profiles and improving overall power quality.

Figures 1.26 and 1.27 show a sample SR-based topology and corresponding waveforms. The switching duty cycle is often modulated based on the double-line frequency ripple, enabling dynamic correction of voltage deviations and further reduction in ripple amplitude.

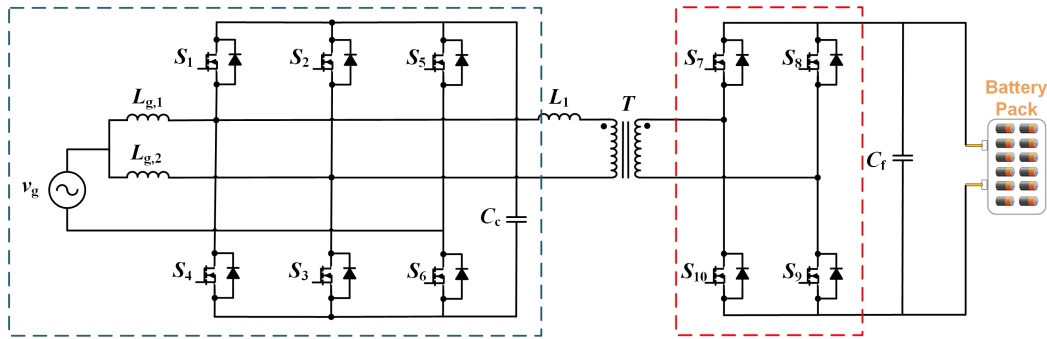


Figure 1.26: AC/DC converter employing synchronous rectification.

However, implementing SR increases circuit complexity. It requires precise gate timing and may necessitate advanced digital control, especially in systems with variable load or supply conditions. Still, the reduction in ripple and

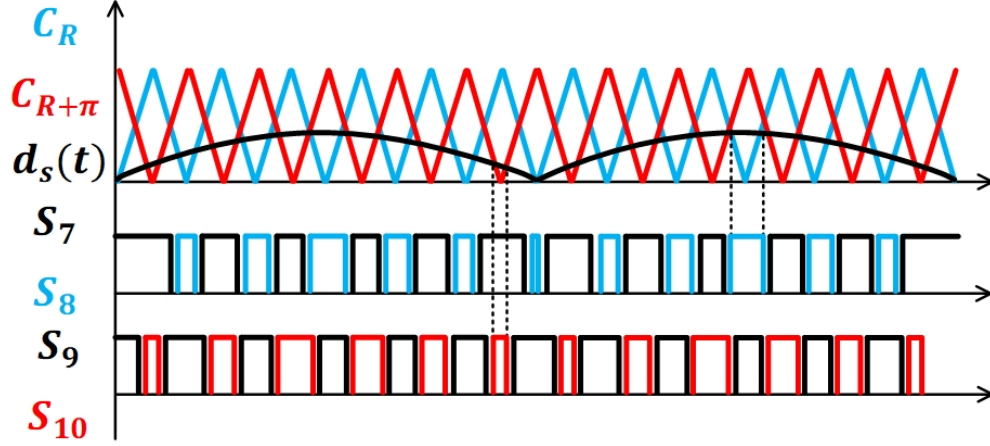


Figure 1.27: Output waveforms from a synchronous rectification converter synchronized to double-line frequency.

conduction losses makes SR an attractive option in modern high-performance converter designs.

Harmonic Injection

Harmonic injection is a control-based ripple reduction technique wherein specific harmonic components are intentionally added to the switching control signal. These injected harmonics are phase-shifted to oppose and cancel the dominant harmonics responsible for output ripple. This form of active filtering is particularly effective in converters with low storage capacitance, where traditional filtering alone may not suffice.

The concept is illustrated in Fig. 1.28, which shows the control block diagram of a harmonic injection setup. A digital controller analyzes the output waveform, identifies the harmonic content, especially those near the second harmonic of the line frequency, and synthesizes an opposing waveform to be injected into the modulator. This targeted cancellation suppresses voltage ripple and enhances output stability.

Advantages of this method include the ability to reduce output ripple without increasing component size or cost. It is also suitable for digital implementation, making it compatible with modern DSP- or microcontroller-based converter platforms.

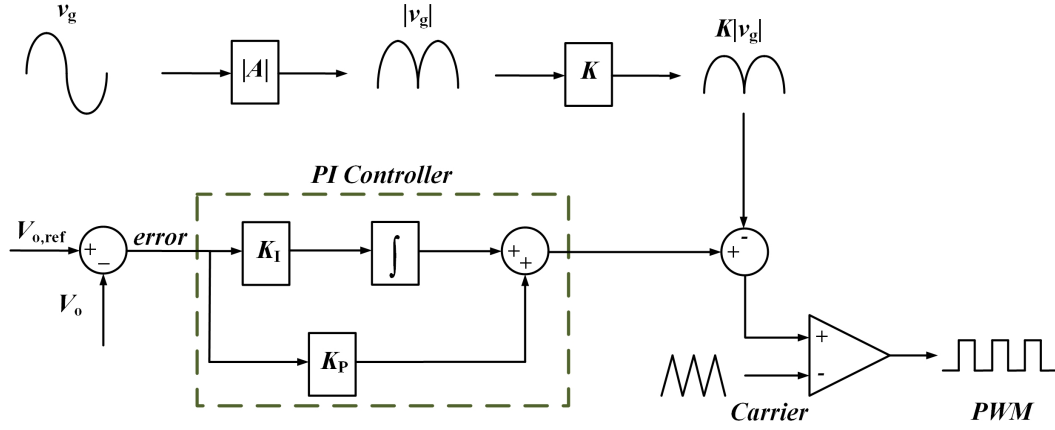


Figure 1.28: Harmonic injection-based control strategy for ripple mitigation [65].

However, harmonic injection requires accurate real-time analysis and modulation, which increases control complexity. Poor implementation can introduce unwanted spectral content or interfere with other system components. Nonetheless, when properly designed, harmonic injection is a powerful tool for reducing voltage ripple in compact AC/DC converters.

Additional Strategies

Besides dedicated filtering and control techniques, other ripple reduction strategies include:

- Switching Frequency Optimization: Increasing the switching frequency can decrease ripple amplitude and reduce the size of filter components. However, it may increase switching losses and EMI, requiring careful trade-off analysis.

- Advanced Control Methods: Implementing sophisticated modulation techniques like interleaved PWM, variable duty-cycle modulation, or predictive control can reduce ripple by improving the converter's dynamic response and output precision.

- Load Balancing: In multi-phase or multi-level converters, distributing the load evenly across phases reduces peak current stress, leading to smoother current profiles and reduced voltage ripple.

These strategies, when used in combination with the techniques discussed

earlier, contribute to a holistic approach to ripple mitigation. By minimizing output ripple, designers can reduce storage capacitance requirements, lower cost, and enhance the size, weight, and efficiency characteristics of the overall AC/DC converter system.

1.6 Control Principles in AC/DC Power Converters

Control systems are an essential component of AC/DC power converters, ensuring stable, efficient, and reliable operation across a wide range of applications. These systems govern how power is processed, regulate output voltage, shape input current for compliance with grid standards, and manage dynamic behavior under varying load and line conditions.

In general, AC/DC converters require precise coordination between current and voltage control loops. Current control which is often implemented to achieve PFC, aims to ensure that the input current is sinusoidal and in phase with the grid voltage. Voltage regulation, on the other hand, maintains the desired output level and adjusts power delivery based on the load or system requirements.

Depending on the converter architecture and its specific role within a larger system, different control strategies may be employed. These include peak current mode control, average current control, hysteresis control, duty ratio (PWM) control, phase-shift modulation, and variable frequency techniques. Each has its advantages and trade-offs in terms of complexity, response time, and efficiency.

In systems that interact with the grid, additional elements such as PLL are used to synchronize with the grid frequency and phase. Furthermore, in applications requiring bidirectional power flow or support during grid disturbances, grid-following (GFL) and grid-forming (GFM) control strategies are essential.

The following sections explore key control techniques used in AC/DC power converters, outlining their operating principles, design considerations, and

practical implications in real-world systems.

1.6.1 PFC Control

PFC is a fundamental function in AC/DC power converters that are connected to the grid. Its main purpose is to ensure that the input current waveform closely follows the shape and phase of the input voltage waveform, thereby improving the overall power quality and reducing harmonic distortion. An ideal PFC system shapes the input current to be sinusoidal and in phase with the grid voltage, mimicking the behavior of a purely resistive load.

Various control strategies are employed to achieve PFC, each with its own advantages, limitations, and suitability for different converter topologies and power levels. The most common techniques include peak current control, average current control, and hysteresis control.

Peak Current Control: In this method, a reference current is generated by scaling the rectified input voltage and multiplying it by the output of a voltage error amplifier. The switch turns off when the sensed current plus an external compensation ramp reaches the reference level. This control method maintains fixed switching frequency and requires only current sensing at the switch, but it may suffer from sub-harmonic oscillation at duty cycles above 50%. The general scheme and current waveform for peak current control are shown in Figures 1.29 and 1.30, respectively.

Average Current Control: This technique improves upon peak current control by using the average value of the inductor current to track the reference. The current is sensed, filtered, and then compared with a reference to modulate the duty cycle via a PWM modulator. This method eliminates the need for a compensation ramp and offers improved noise immunity. However, it adds complexity due to the requirement of a current error amplifier. Figures 1.31 and 1.32 illustrate the implementation and current waveform of average current control.

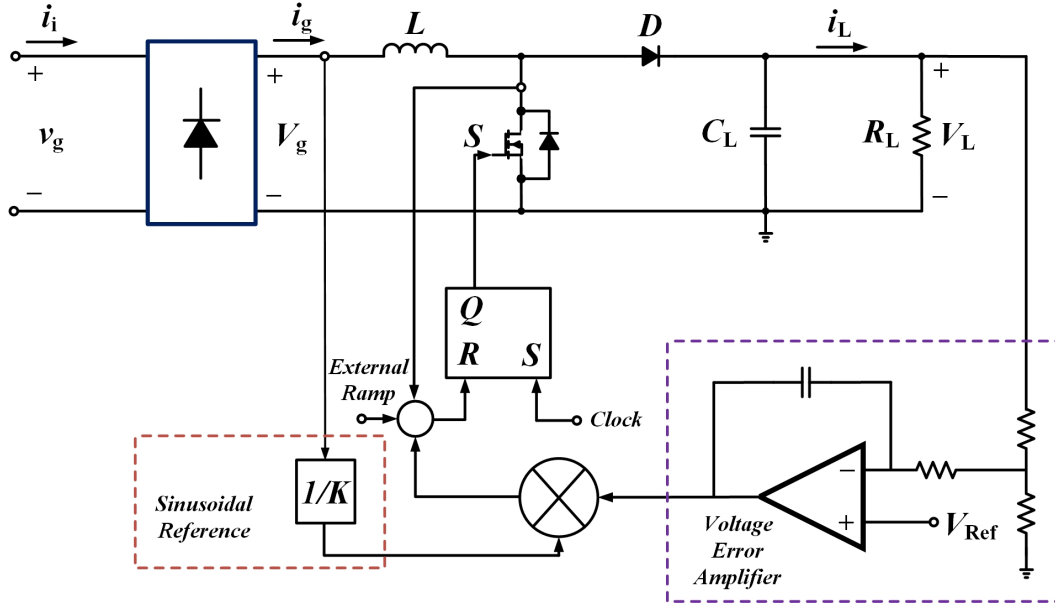


Figure 1.29: PFC based on peak current control implemented on boost converter.

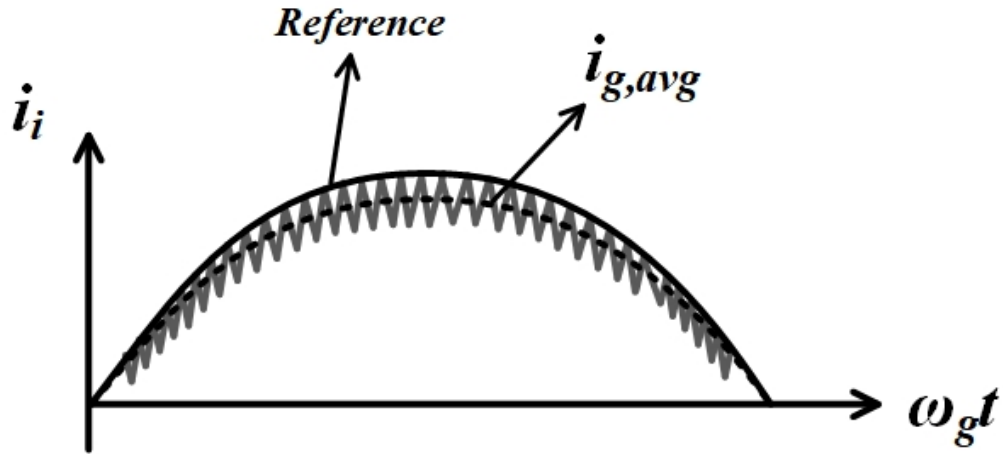


Figure 1.30: Current waveform while implementing peak current control technique.

Hysteresis Control: In this approach, two sinusoidal reference signals define the upper and lower bounds for the current waveform. The switch is turned on when the inductor current drops below the valley reference and turned off when it exceeds the peak reference. This leads to a variable switching frequency. While simple and capable of producing low-distortion current waveforms, hysteresis control is sensitive to noise and requires current sensing

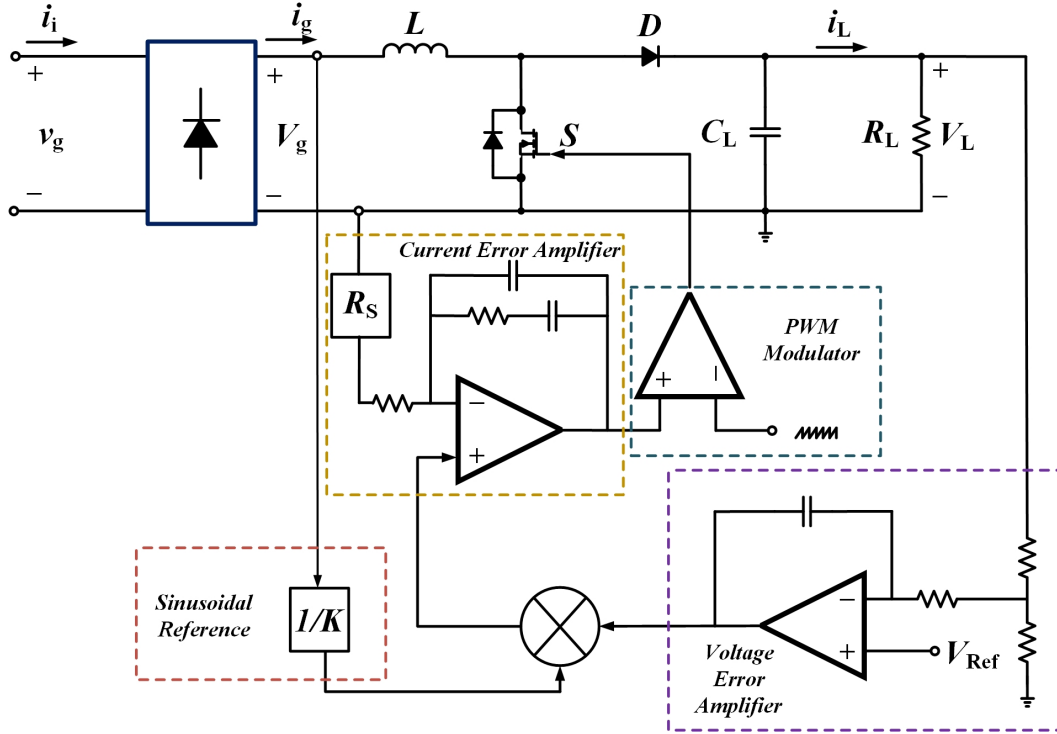


Figure 1.31: PFC based on average current control implemented on boost converter.

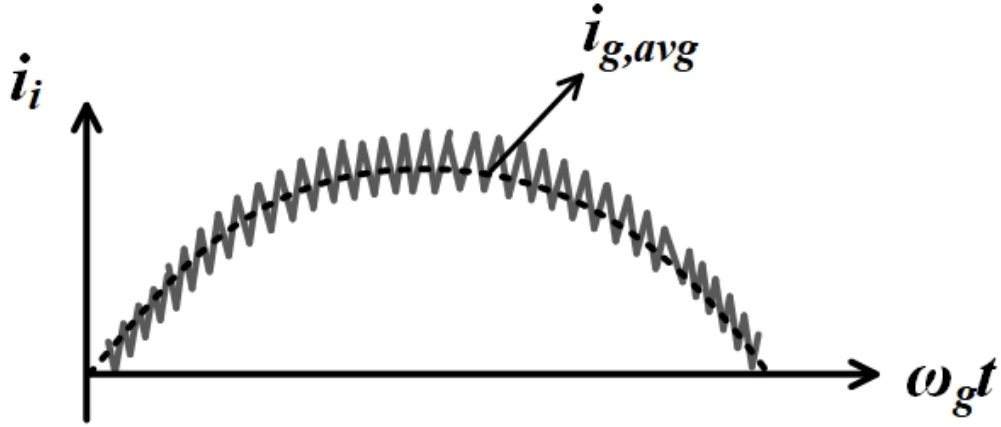


Figure 1.32: Current waveform while implementing average current control technique.

hardware. Figures 1.33 and 1.34 show the schematic and resulting waveforms for hysteresis control.

Each PFC technique involves trade-offs between complexity, efficiency, switching noise, and response time. The appropriate method is typically se-

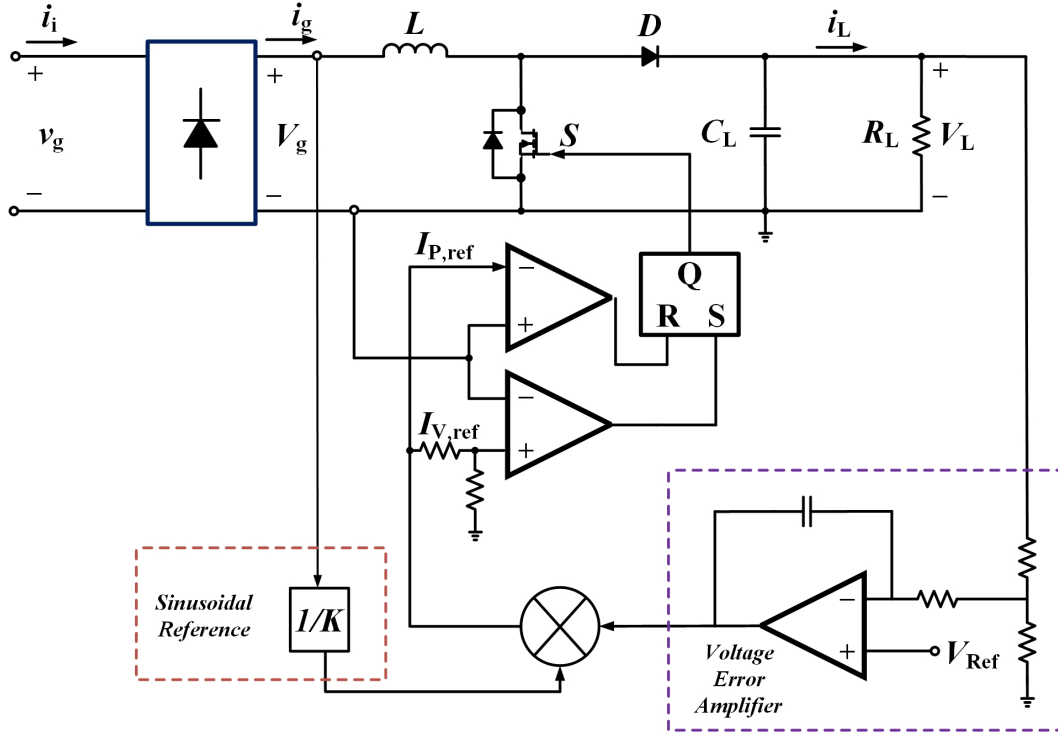


Figure 1.33: PFC based on hysteresis current control implemented on boost converter.

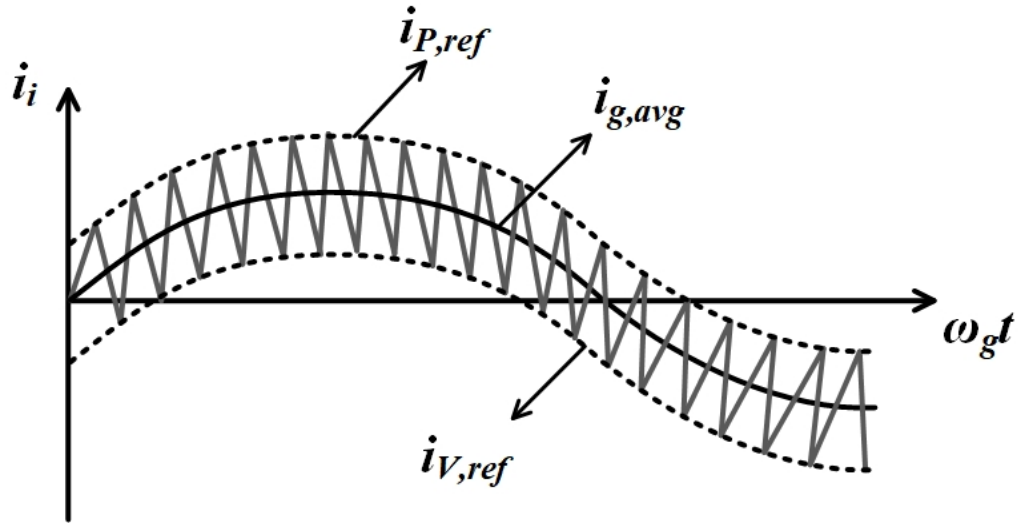


Figure 1.34: Current waveform while implementing hysteresis current control technique.

lected based on the converter's topology, power level, and specific application requirements.

1.6.2 Voltage Regulation

Voltage regulation is a critical function in AC/DC power converters, responsible for maintaining a stable and controlled output voltage despite fluctuations in input voltage or load conditions. This ensures proper operation of downstream systems and protects sensitive components connected to the converter's output. Effective voltage regulation improves efficiency, enhances reliability, and allows the converter to adapt to varying power demands.

Several modulation techniques are used for voltage regulation, each suited to different converter topologies and application requirements. Common methods include duty ratio control, phase shift modulation (PSM), and variable frequency modulation (VFM).

Duty Ratio Control: In this method, also known as PWM control, the output voltage is regulated by adjusting the duty cycle of the switching signal. A typical implementation uses a PI controller to generate a control signal that is compared with a carrier waveform (such as a ramp) to produce the PWM signal. This technique is straightforward and widely used due to its ease of implementation and good dynamic response. However, it can introduce ripple current, which must be filtered using large capacitors. The PWM waveform and block diagram are shown in Figures 1.35 and 1.36.

Phase Shift Modulation: PSM is typically used in full-bridge or dual-active-bridge converters, where the phase difference between gate signals is varied to control power flow. This technique enables soft switching, which reduces switching losses and improves efficiency, especially valuable in high-power systems. Figures 1.37 and 1.38 illustrate the converter structure and corresponding waveforms for phase-shift modulation.

Variable Frequency Modulation: VFM is often applied in resonant converters, where the switching frequency is varied relative to the circuit's resonant frequency to regulate output voltage. This approach enables zero-voltage or zero-current switching, significantly reducing switching losses. The CLL

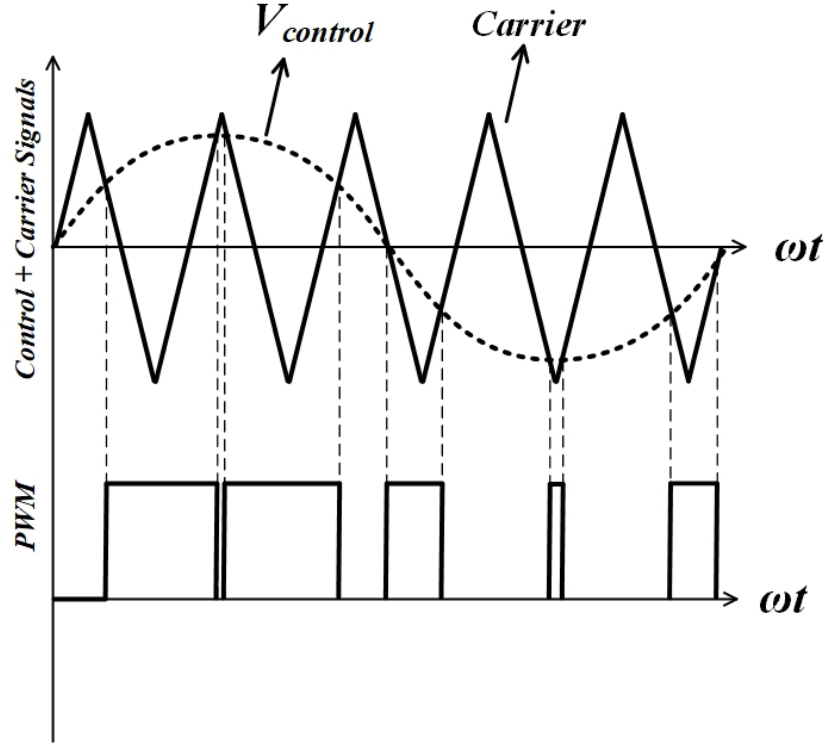


Figure 1.35: Pulse Width Modulation scheme.

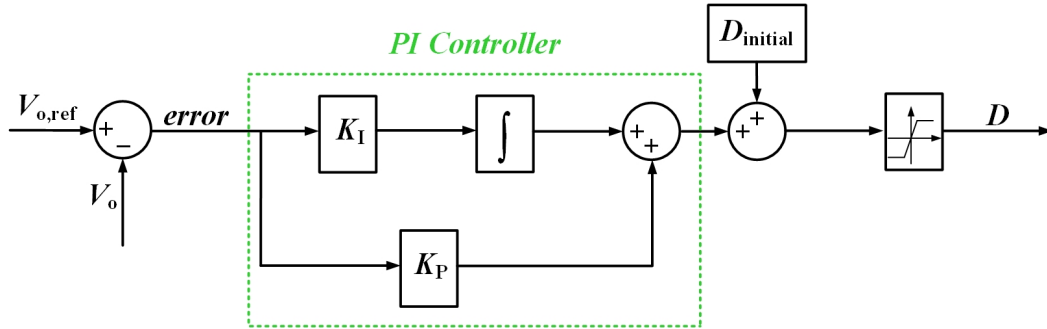


Figure 1.36: Block diagram of duty ratio control based on PI controller.

resonant converter, shown in Figure 1.39, serves as an example of such an application. The gain characteristics and control block for this method are depicted in Figures 1.40 and 1.41.

Each voltage regulation technique presents trade-offs between complexity, efficiency, control bandwidth, and hardware requirements. The choice of modulation method depends on the specific design objectives, including power level, converter topology, and desired efficiency.

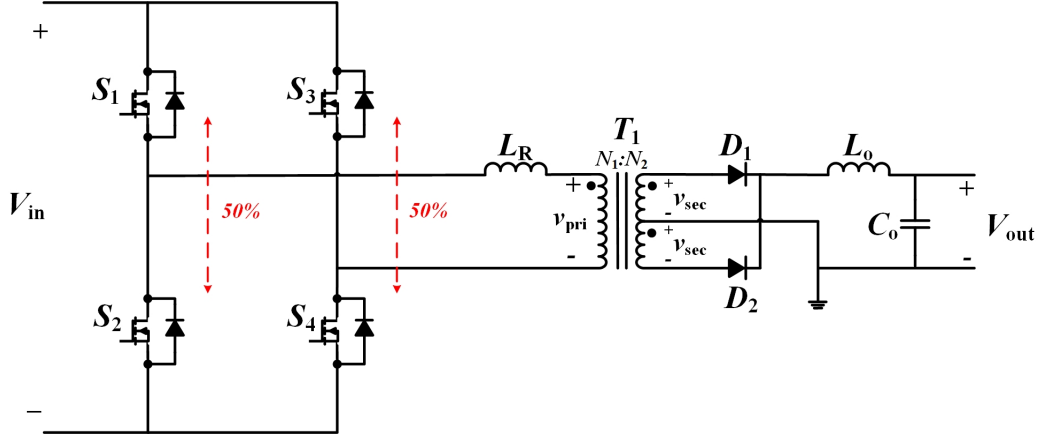


Figure 1.37: Phase-Shifted full-bridge converter.

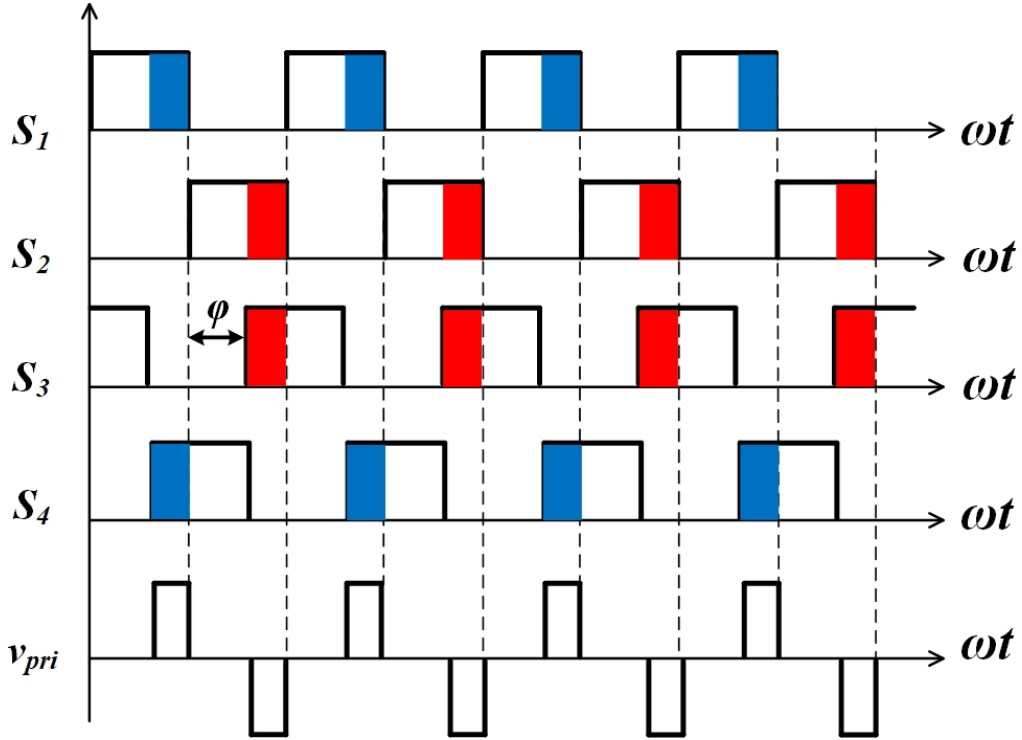


Figure 1.38: PSM-based waveforms of a phase-shifted full-bridge converter.

1.6.3 Grid-Forming Control

GFM control is a strategy employed in AC/DC power converters that enables them to operate as voltage sources capable of establishing and regulating the local grid voltage and frequency. Unlike GFL converters, which synchronize with an existing grid, GFM converters set their own reference, making them particularly valuable in islanded systems or weak grid scenarios.

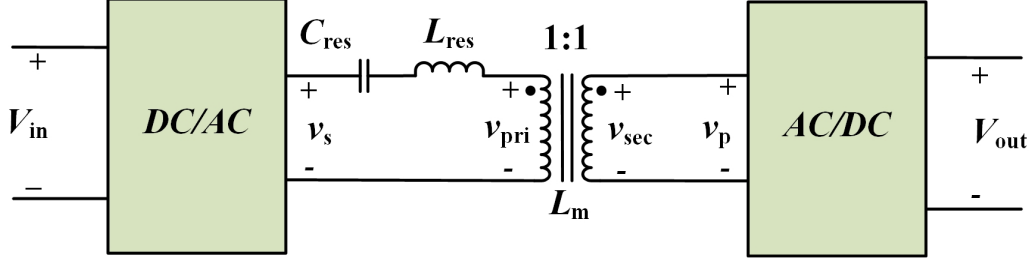


Figure 1.39: CLL-based resonant converter.

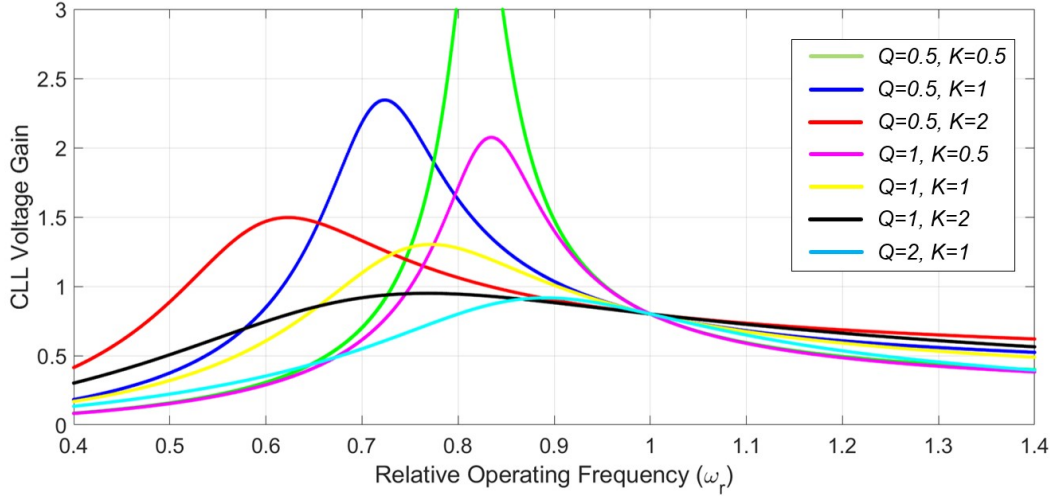


Figure 1.40: CLL resonant circuit gain waveform.

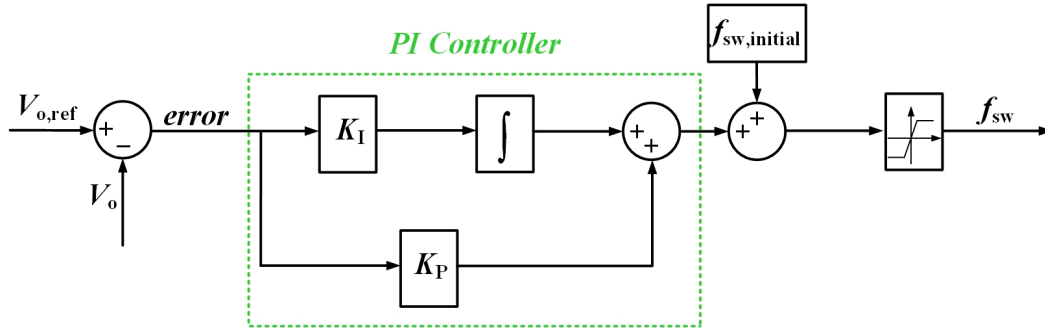


Figure 1.41: Block diagram of VFM control based on PI controller.

In this control mode, the converter plays a proactive role in shaping the electrical environment. It is responsible for generating a stable voltage waveform with predefined amplitude and frequency, which other converters and loads can follow. This autonomous behavior allows the converter to maintain operation even in the absence of a strong external grid reference.

The key characteristic of GFM control is its ability to enhance system re-

silience and stability, especially during grid disturbances or outages. These systems are designed with robust control algorithms that dynamically regulate output voltage and frequency in response to load variations and system conditions.

Figure 1.42 illustrates the basic concept of a GFM converter operating as a voltage source.

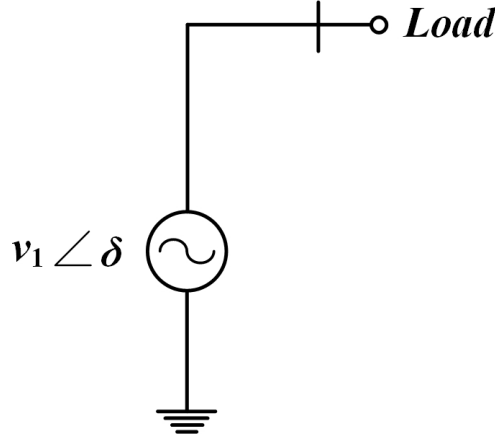


Figure 1.42: GFM control.

To implement GFM behavior, detailed modeling of the converter and its interfacing components is essential. For example, when using an LCL filter between the converter and the grid or load, the control system must be carefully designed based on the filter's dynamic characteristics. The circuit diagram of such a system is shown in Figure 1.43, and a corresponding block diagram of the GFM control strategy is shown in Figure 1.44.

While GFM control offers enhanced grid support, autonomy, and resilience, it comes with certain challenges. These include increased complexity in control design, the need for high-performance digital controllers, and careful coordination in systems where multiple converters operate in GFM mode simultaneously. Furthermore, ensuring system stability under dynamic loading conditions requires precise tuning and sometimes communication between multiple units.

Despite these challenges, GFM converters are gaining prominence in modern power systems, particularly in scenarios demanding improved grid stability,

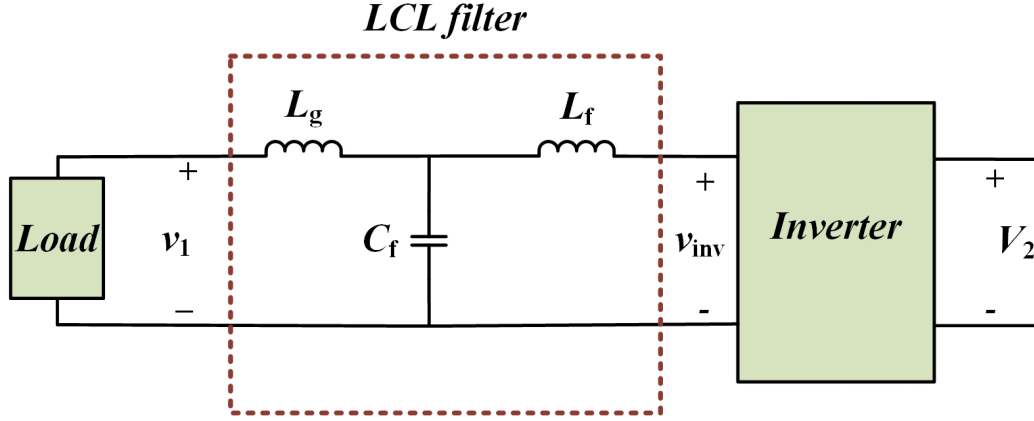


Figure 1.43: GFM control using LCL filter interface.

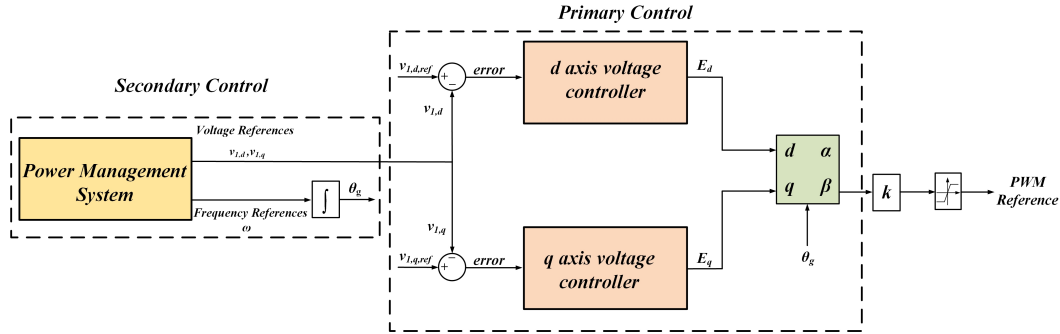


Figure 1.44: GFM control structure.

support for renewable integration, and autonomous operation in microgrids or decentralized energy networks.

1.6.4 Grid-Following Control

GFL control is a widely used strategy in AC/DC power converters that are connected to a stable grid. In this mode, the converter operates as a current source, injecting current into the grid while synchronizing its operation with the voltage and frequency of the existing grid. This synchronization is typically achieved using a Phase-Locked Loop (PLL), which tracks the grid's phase and provides the necessary reference signals for the control system.

GFL converters regulate their output current based on the grid voltage waveform, ensuring that the injected current is sinusoidal and in phase with the voltage, thereby supporting power quality and stability. This control method is essential for systems where the grid is the dominant source of voltage and

frequency reference, and the converter's role is to deliver power in a controlled and responsive manner.

Figure 1.45 shows the conceptual model of a converter operating in GFL mode, where the converter acts as a controlled current source.

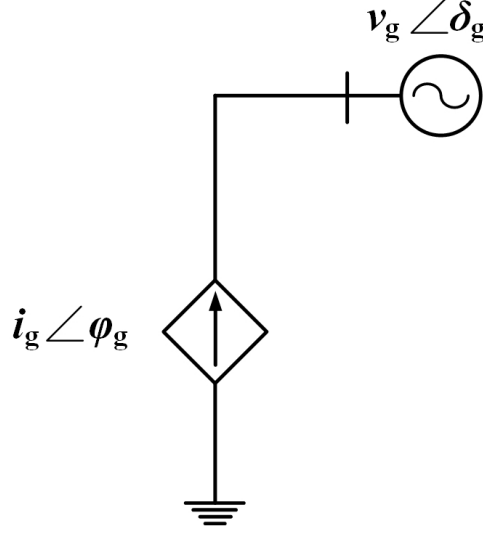


Figure 1.45: GFL control.

The implementation of GFL control typically involves current control loops that are designed based on the dynamics of the converter's output filter. For converters interfaced with the grid through LCL filters, precise modeling is necessary to achieve stable and accurate current regulation. Figure 1.46 presents a grid-connected inverter using an LCL filter, and Figure 1.47 shows the corresponding control block diagram.

GFL control offers several advantages, including fast dynamic response, relatively simple implementation, and compatibility with established grid infrastructure. It is especially effective when the external grid is strong and stable, allowing the converter to maintain synchronization and inject power with high accuracy.

However, this method also presents some limitations. Its performance is heavily dependent on the availability of a stable external voltage reference. In the event of a grid disturbance or outage, GFL converters may lose synchronization and cease proper operation. Additionally, these systems are less

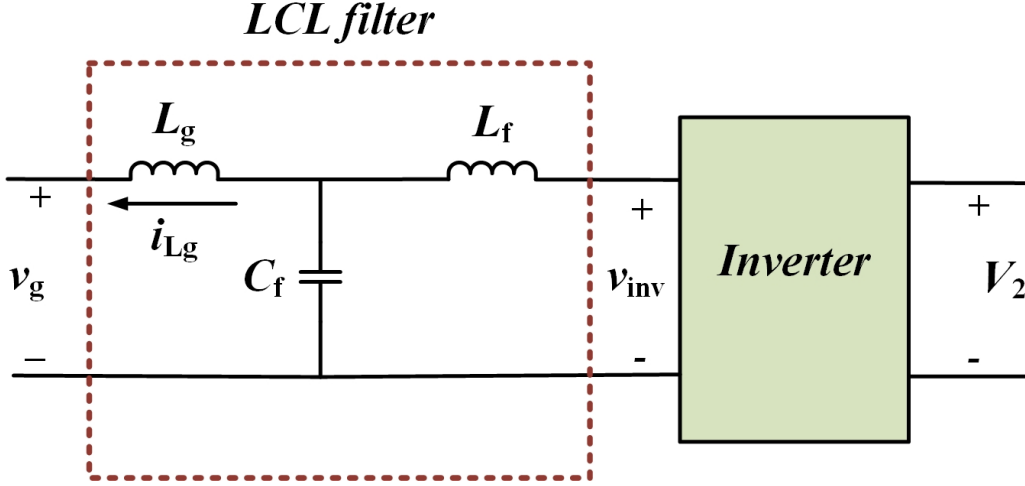


Figure 1.46: GFL inverter with LCL filter.

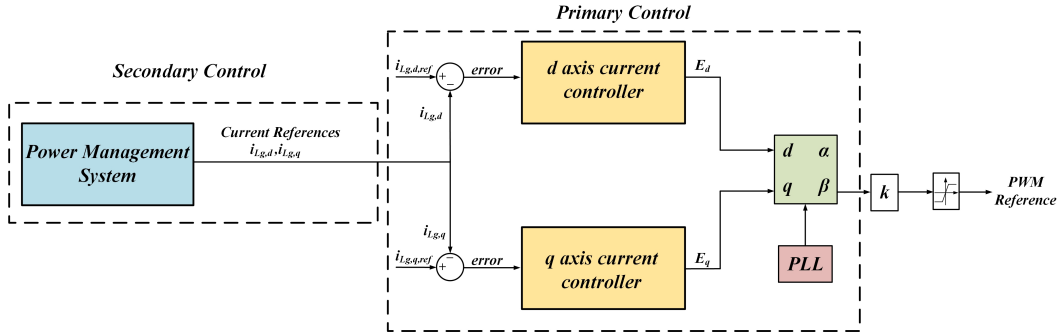


Figure 1.47: GFL control structure.

effective in supporting voltage and frequency stability during transients or weak-grid conditions, where a more autonomous approach such as GFM control may be necessary.

Despite its limitations, GFL control remains the dominant method in grid-connected power converter applications due to its simplicity and effectiveness under nominal operating conditions.

1.7 Recent Grid-Connected Control designs for Bidirectional AC/DC Converters

While significant progress has been made in converter topologies and hardware-level optimization, the design of robust controllers for bidirectional AC/DC converters, particularly in V2G and V2H contexts, remains an open challenge.

These applications demand stable performance under a wide range of uncertainties, including grid disturbances, component tolerances, load transients, and weak or islanded grid conditions. Conventional control strategies often fail to maintain performance in the face of such dynamic operating scenarios, highlighting the need for advanced robust control techniques.

Recent studies have proposed various robust control frameworks aimed at enhancing converter stability and disturbance rejection. Zhao et al. [80] introduced a GFM control method based on active susceptance injection, which improves system damping across a wide range of short-circuit ratios. Chakraborty et al. [81] proposed a generalized μ -synthesis-based framework to manage uncertainties in load and grid dynamics, demonstrating strong robust stability margins. Huang et al. [82] developed a decentralized H_∞ control approach that emphasizes scalability and local robustness in multi-converter systems. Similarly, Afshari et al. [83] explored low-gain feedback control techniques effective for islanded microgrids under communication uncertainty, while Babazadeh et al. [84] applied convex optimization techniques for structured robust control in multi-DG islanded systems.

Although these strategies show promising results in microgrid and general inverter contexts, their application to bidirectional OBCs for V2H scenarios remains limited. Residential environments introduce unique control challenges such as frequent load transients, nonlinear appliance behavior, and the absence of large passive filters. Moreover, the use of HV battery systems and space-constrained embedded controllers imposes additional complexity and design constraints.

Current gaps in the literature include: **1)** Limited controller designs explicitly tailored for bidirectional OBCs in V2H mode, **2)** Insufficient robustness against nonlinear and rapidly changing residential loads, **3)** Dependence on high-order or computationally intensive algorithms unsuitable for EV-grade embedded systems, and **4)** Weak performance under ripple and steady-state voltage variations induced by parameter mismatch or model drift.

These gaps motivate the need for scalable, efficient, and resilient robust control strategies specifically engineered for automotive V2H applications, bal-

ancing real-time performance with hardware feasibility.

1.8 Technical Challenges and Possible Solutions

Designing high-performance AC/DC converters for EV charging systems involves navigating several technical challenges, especially as the demand for higher power, better efficiency, and more compact designs continues to grow. This section outlines the main issues encountered in developing single-phase AC/DC converters and introduces the strategies this thesis explores to address them in later chapters.

1.8.1 Achieving High Efficiency Without Compromising Simplicity

Single-phase AC/DC converters are widely used in charging applications due to their simplicity and lower cost. However, many conventional topologies, such as the full-bridge boost converter, struggle to maintain high efficiency across a wide load range. These converters also face switching losses at high frequencies, which can significantly degrade performance.

In this Chapter, several uni-directional converter topologies were examined in detail. Among them, the bridgeless boost and totem-pole configurations emerge as promising candidates for improving efficiency while reducing conduction losses. By eliminating the input diode bridge and using synchronized switches instead, these topologies offer a more efficient path for current flow, especially during low-load conditions.

1.8.2 Managing Large Storage Capacitance Requirements

One of the biggest physical and reliability bottlenecks in single-phase converters is the requirement for bulky storage capacitors to filter the low-frequency (120 Hz) ripple. These capacitors are not only large but also often electrolytic, which can reduce system lifespan due to their limited temperature and aging tolerance.

In Chapter 1, this issue is addressed by exploring multiple strategies for storage capacitance reduction. Both passive and active techniques are discussed, including:

- The use of film capacitors in conjunction with current ripple compensation,
- Integration of voltage ripple reduction controller (VRRC) for active ripple reduction.

Hardware results throughout the report demonstrate how the proposed method significantly reduce voltage ripple while maintaining output voltage regulation, even under dynamic loading conditions.

1.8.3 Supporting Bidirectional Power Flow and Grid Services

With the growing interest in V2G applications, enabling bidirectional power flow is becoming increasingly important. However, incorporating bidirectionality adds complexity in both control and hardware, especially when also aiming for high power density and low harmonic distortion.

Chapter 3 introduces a stacked-switch bidirectional converter architecture tailored for EV applications. This design not only supports reverse power flow but also distributes voltage stress across multiple switches, enabling the use of lower-voltage-rated devices with better efficiency. The chapter also covers the associated control strategies for synchronizing PFC and grid interactivity.

1.8.4 Robust GFM Control with Improved Transient Performance

In Chapter 4, a robust GFM control strategy is developed for operation under islanded grid conditions. A polytopic state-space model of the grid-side connection is constructed, and an $\mathcal{H}_\infty$ controller is synthesized using Linear Matrix Inequalities (LMIs). This approach ensures robust voltage and frequency regulation in the presence of parameter variations and external disturbances.

Hardware validation confirms stable GFM operation with low output voltage distortion and fast dynamic response.

1.8.5 Summary

Across the design of AC/DC converters for EV charging, several persistent challenges arise: achieving high efficiency, minimizing bulky passive components, supporting grid interaction, and managing ripple. The following chapters of this thesis systematically address each of these issues through careful topology selection, Hardware-backed design, and proposed control enhancements. In doing so, the work aims to contribute practical solutions for more compact, efficient, and grid-friendly charging systems.

1.9 Research Objectives

This dissertation addresses three key challenges in single-phase AC/DC power conversion for EV charging systems: reducing storage capacitance, enabling bidirectional power flow, and achieving robust GFM control.

1. Development of a Unidirectional Bridgeless AC/DC Converter with Minimal Storage Capacitance: Design a high-performance unidirectional converter that eliminates the diode bridge and reduces voltage stress through a stacked-switch architecture. The topology operates in Discontinuous Conduction Mode (DCM) for natural power factor correction and integrates a CLLC resonant stage for soft-switching. Closed-loop controllers regulate output voltage, suppress low-frequency ripple, and maintain compliance with grid standards while minimizing reliance on electrolytic capacitors.

2. Design of a Bidirectional Electrolytic-Capacitor-Less AC/DC Converter for Grid-Interactive EV Applications: Develop a bidirectional converter supporting both G2V and V2G modes using a dual-stacked-switch structure and resonant CLLC stage. The system enables capacitor-less operation through active ripple reduction control and dq-frame-based grid synchronization, ensuring high efficiency, fault tolerance, and compatibility with HV EV batteries.

3. Implementation of a Robust GFM Control Scheme for V2H

Operation: Implement an $\mathcal{H}_\infty$ -based GFM controller using Linear Matrix Inequalities (LMIs) to ensure robust voltage and frequency regulation under islanded or uncertain grid conditions. The controller is validated experimentally and tailored for V2H applications, ensuring low harmonic distortion, fast dynamic response, and reliable standalone performance.

1.10 Dissertation Outline

This dissertation is organized into five chapters, covering the design, control, and validation of capacitor-less, stacked-switch-based single-phase AC/DC converters for EV charging applications. The work spans unidirectional and bidirectional converter development, robust control strategies, and hardware evaluation.

Chapter 1 – Introduction: Presents the motivation for developing compact and reliable AC/DC converters in EV systems, driven by environmental goals and the limitations of conventional designs. It outlines key technical challenges, such as reliance on electrolytic capacitors, and introduces the main research objectives addressed in this work.

Chapter 2 – Unidirectional Bridgeless AC/DC Converter with Minimal Storage Capacitance: Introduces a single-stage unidirectional AC/DC converter for HV EV charging, featuring a bridgeless stacked-switch architecture. The design operates in DCM for inherent power factor correction and incorporates a ripple reduction loop to minimize storage capacitance. Experimental validation confirms high efficiency, soft-switching, and compliance with grid standards.

Chapter 3 – Bidirectional Capacitor-Less AC/DC Converter for Grid-Interactive EV Applications: Presents a bidirectional converter with a dual-stacked-switch half-bridge structure and a CLLC resonant stage. A dq-frame PFC controller ensures sinusoidal current in both G2V and V2G modes. A closed-loop ripple reduction strategy enables capacitor-less operation. Hardware results demonstrate effective bidirectional power flow and low harmonic

distortion.

Chapter 4 – Robust $\mathcal{H}_\infty$ GFM Control under Uncertainty: Develops an $\mathcal{H}_\infty$ -based GFM control strategy using LMIs, designed for uncertain grid and load conditions. The controller ensures voltage/frequency stability, includes integral action, and is validated through hardware tests under V2H conditions.

Chapter 5 – Conclusion and Future Work: Summarizes the dissertation’s contributions in converter design and control, and suggests future research directions such as three-phase extensions, renewable integration, and AI-assisted adaptive control for enhanced grid interaction.

Chapter 2

Unidirectional Bridgeless, Stacked Switch-Pair-Based AC/DC Power Converter with Minimal Storage Capacitance

2.1 Introduction

This chapter presents the development of a novel unidirectional single-phase AC/DC converter tailored for EV applications. The converter architecture addresses the key limitations of conventional designs, including reliance on bulky electrolytic capacitors, lack of soft-switching, high voltage stress on semiconductor devices, and poor conduction efficiency due to diode bridge rectification.

In the first part of this chapter, a new bridgeless, stacked-switch-based boost-type AC/DC converter topology is introduced. This topology eliminates the input diode bridge, reduces switch voltage stress by half through a stacked-switch configuration, and operates in Discontinuous Conduction Mode (DCM) to inherently shape the input current for high power factor operation.

The second part of this chapter focuses on the closed-loop control system development, which includes input current shaping, output voltage regulation using VFM, and low-frequency voltage ripple reduction using a secondary-side duty ratio modulation strategy. This coordinated control allows the converter to operate with minimal film or ceramic capacitance while still meeting grid compliance standards.

Finally, this chapter concludes with simulation and experimental results obtained from a 1.1 kW hardware prototype. These results validate the performance of the converter in terms of efficiency, power factor, THD, and voltage ripple performance under various operating conditions.

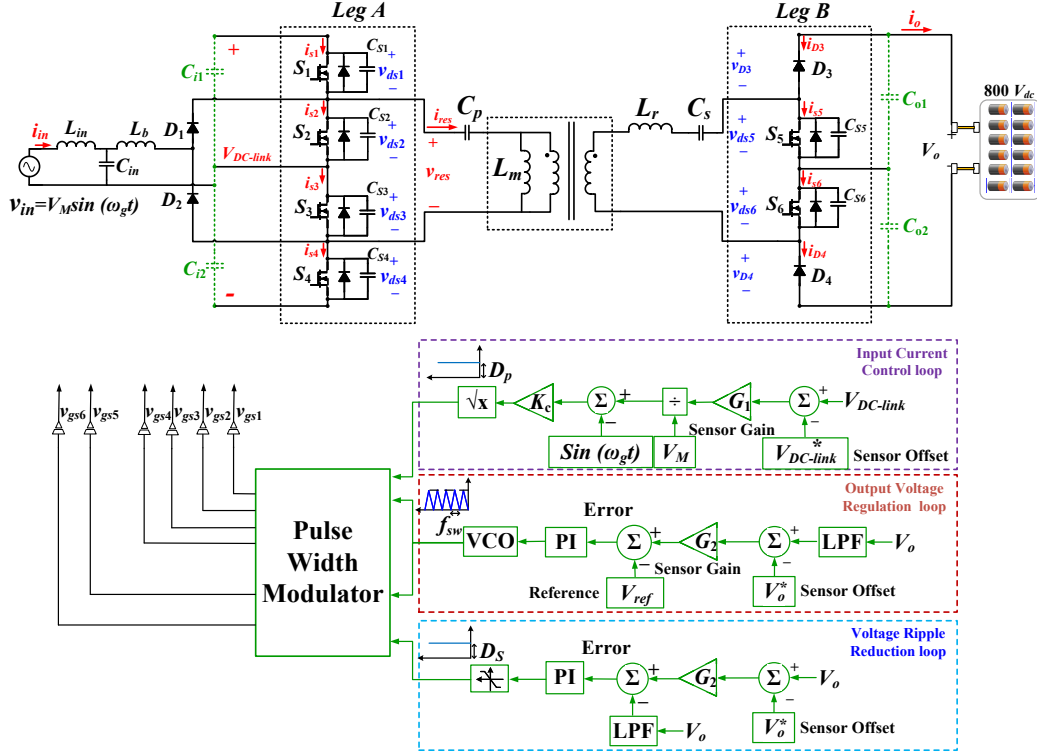


Figure 2.1: Single-stage stacked switches-based bridgeless AC/DC converter.

2.2 Description and Operation of the Converter

Fig 2.1 illustrates the AC/DC converter and the designed control system developed for HV OBCs in EV systems. The converter consists of a bridgeless PFC boost rectifier connected to an isolated CLLC resonant circuit through stacked switches configuration marked as leg A. Moreover, the output of the isolated CLLC resonant circuit is connected to High-Frequency (HF) half-wave rectifier. In leg A of the converter, two middle switches S_2 and S_3 operate together with the same duty ratio D_p , while switches S_1 and S_4 operate with a duty ratio of $1 - D_p$. Moreover, two middle switches S_5 and S_6 in leg B operate together with the same duty ratio D_s generated from the closed-loop

oscillation control system. Due to the stacked switches configuration of the switches in both leg A and leg B, the voltage stress across each switch in leg A is half of the DC-link voltage and the voltage stress across each switch in leg B is half of the output voltage, making the converter suitable for HV EV application. Furthermore, the CLLC resonant circuit module consists of a resonant inductor L_r , a HF transformer with magnetizing inductance L_m , and two resonant capacitor C_p and C_s . It is worth mentioning that while leg A's functionality aligns with recognized practices, leg B's operation marks a deviation from traditional methods that generally leverage only leg A for their operation. Therefore, a comprehensive analysis of leg B's integration with leg A and their synchronized operation and the achievement of soft-switching across all semiconductor devices becomes of paramount importance in the converter.

In leg A of the converter, each switch is shared between the resonant converter stage and the input PFC boost stage. Therefore, each switch current consists of the resonant current i_{res} and the PFC current i_b . As the result of the presence of the resonant circuit, all the switches in the converter are able to achieve soft-switching operation. Key operating waveforms of the AC/DC converter is illustrated in Fig. 2.2. Since the converter operates symmetrically during both positive and negative half-cycles, only the positive half-cycle is addressed in this analysis. Moreover, the switching frequency of leg A and leg B of the converter has been consider identical as f_{sw} . For steady-state analysis of the converter, the switching period T_{sw} is divided into nine operating modes. The operational stages of the AC/DC converter within the switching period T_{sw} is illustrated in Fig. 2.3.

Interval $t_0 < t < t_1$

During this interval, the gate signals are applied to the switches S_1 and S_4 in leg A, and the the boost current is discharging through D_1 . As the result, the currents $i_{D1} + i_{res}$ and i_{res} forces the antiparallel diode of S_1 and S_4 to conduct, respectively. This is why S_4 current reaches zero sooner than S_1 current. During this interval, the voltage stress across switches S_2 and S_3 is half of the DC-link voltage $V_{DC-link}/2$. Moreover, the lagging resonant current

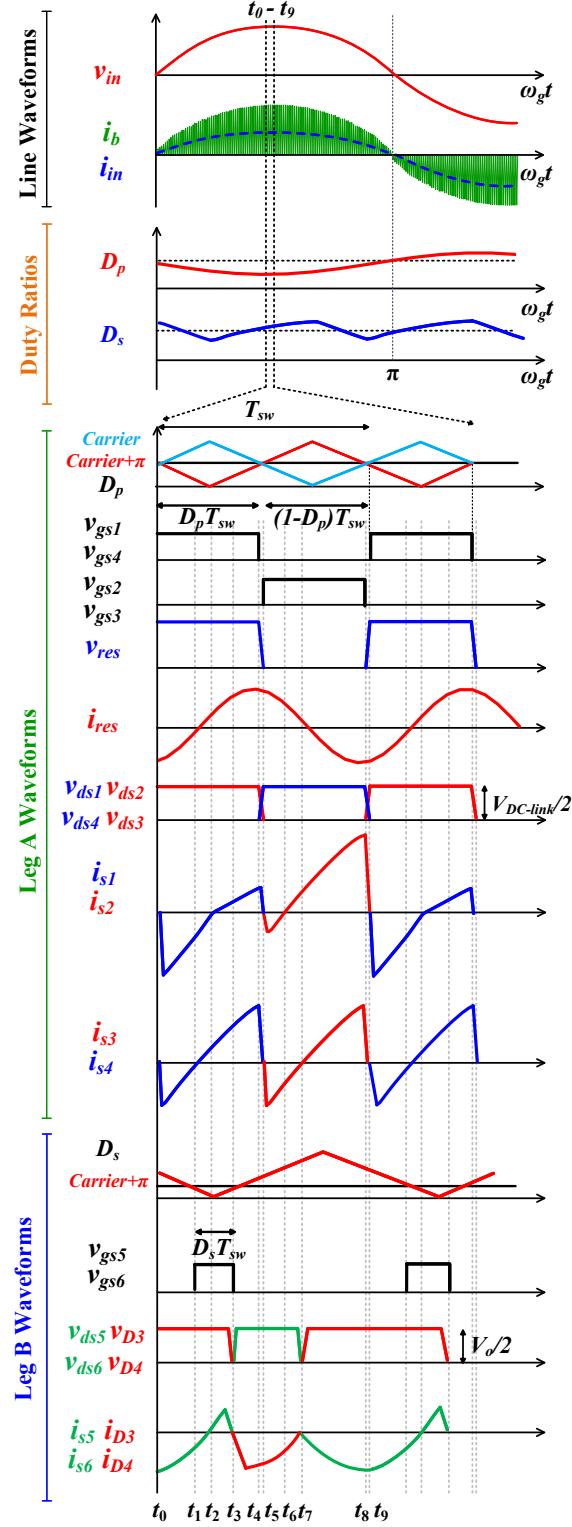


Figure 2.2: Key operating waveforms of the AC/DC converter.

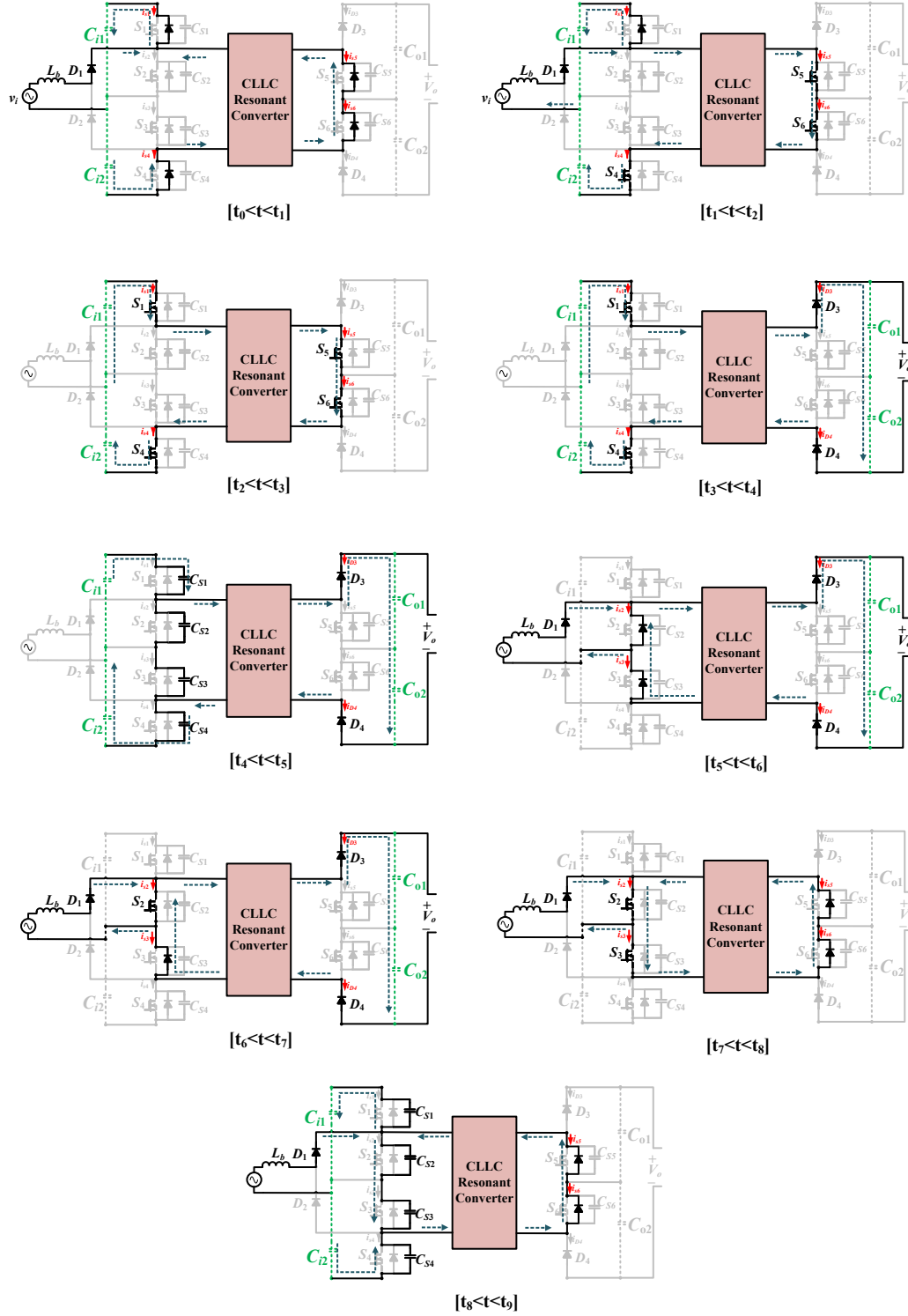


Figure 2.3: Operational stages of the bridgeless AC/DC converter within a switching period in the positive half cycle.

i_{res} forces the antiparallel diodes of switches S_5 and S_6 in leg B to conduct. The current flowing through the switches S_1 , S_4 , S_5 , and S_6 in this interval are shown below:

$$\begin{aligned} i_{s_1} &= \frac{\sqrt{2}V_{DC-link}}{\pi|Z_{in}|} \sqrt{1 - \cos(2\pi D_p)} - \frac{V_M}{L_b} D_p T_{sw} \\ i_{s_4} &= \frac{\sqrt{2}V_{DC-link}}{\pi|Z_{in}|} \sqrt{1 - \cos(2\pi D_p)} \\ i_{s_5} = i_{s_6} &= \frac{\sqrt{2}V_{DC-link}}{\pi|Z_{in}|} \sqrt{1 - \cos(2\pi D_p)} \end{aligned} \quad (2.1)$$

Interval: $t_1 < t < t_2$

During this interval, the gate signals are still applied to the switches S_1 and S_4 in leg A. At this point, the switch S_4 changes its polarity as the boost current stops flowing through S_4 and turns ON with Zero Voltage Switching (ZVS). Moreover, the gate signals are applied to the switches S_5 and S_6 in leg B and since the lagging resonant current is now positive, S_5 and S_6 turn ON under ZVS to reduce the ripple by changing the gain of the converter using variable duty ratio D_s .

Interval: $t_2 < t < t_3$

In this interval, the gate signals are still applied to the switches S_1 and S_2 in leg A. At $t = t_2$, the boost current becomes zero and the switch S_1 changes its polarity and turns ON under ZVS. At this point, the boost current stops flowing through the switch S_1 and the S_1 current is the resonant current. Moreover, depending on the duty ratio D_s , the switches S_5 and S_6 remain on for a while and then turn OFF.

Interval: $t_3 < t < t_4$

The switches S_1 and S_4 are still conducting, while the gate signal of the switches S_5 and S_6 are removed. At the same time, the snubber capacitors C_{S_5} and C_{S_6} start to charge. As the result, the voltages across the switches S_5 and S_6 charge gradually, which results in near Zero Current Switching (ZCS)

turn OFF for S_5 and S_6 . Moreover, the resonant current flows through the diodes D_3 and D_4 and charges the output capacitors C_{o1} and C_{o2} .

$$\begin{aligned} i_{D_3} &= \frac{\sqrt{2}V_{DC-Link}}{\pi|Z_{in}|} \sqrt{1 - \cos(2\pi(1 - D_p))} \\ i_{D_4} &= \frac{\sqrt{2}V_{DC-link}}{\pi|Z_{in}|} \sqrt{1 - \cos(2\pi(1 - D_p))} \end{aligned} \quad (2.2)$$

Interval: $t_4 < t < t_5$

During this interval, the gate signals of the switches S_1 and S_4 are removed and the snubber capacitors C_{S1} and C_{S4} start to charge. As the result, the voltages across the switches S_1 and S_4 charge gradually, which results in near ZCS turn OFF for S_5 and S_6 .

Interval: $t_5 < t < t_6$

During this interval, the gate signals are applied to the switches S_2 and S_3 , and the the boost current begins to charge which will result in ZCS turn ON for D_1 . At the same time, the currents $i_{D1} + i_{res}$ and i_{res} forces the antiparallel diode of S_2 and S_3 to conduct, respectively. Since $i_{res} > i_{D1} + i_{res}$, the current going through the antiparallel diode of S_3 is higher than S_2 . This is why S_3 current will reach zero sooner than S_2 current. During this interval, the voltage stress across switches S_1 and S_4 is half of the DC-link voltage $V_{DC-link}/2$. The current flowing through the antiparallel diodes of the switches S_2 and S_3 are as below:

$$\begin{aligned} i_{s2} &= \frac{\sqrt{2}V_{DC-link}}{\pi|Z_{in}|} \sqrt{1 - \cos(2\pi(1 - D_p))} + \frac{V_M}{L_b} D_p T_{sw} \\ i_{s3} &= \frac{\sqrt{2}V_{DC-link}}{\pi|Z_{in}|} \sqrt{1 - \cos(2\pi(1 - D_p))} \end{aligned} \quad (2.3)$$

Interval: $t_6 < t < t_7$

At $t = t_6$, the gate signals are still applied to the switches S_2 and S_3 , and the current that were flowing through the antiparallel diode of S_2 becomes zero, resulting in ZVS turn ON for S_2 . However, since i_{res} is still positive and $i_{res} < i_{D1}$, the antiparallel diode of S_3 is still ON.

Interval: $t_7 < t < t_8$

At $t = t_7$, the gate signals are still applied to the switches S_2 and S_3 , and the current that were flowing through the antiparallel diode of S_3 becomes zero too, resulting in ZVS turn ON for S_3 . Moreover, the negative resonant current i_{res} start flowing through the antiparallel diodes of the switches S_5 and S_6 in leg B.

Interval: $t_8 < t < t_9$

At $t = t_8$, the gate signals of the switches S_2 and S_3 are removed and the snubber capacitors C_{S_2} and C_{S_3} start to charge. As the result, the voltages across the switches S_2 and S_3 start to rise slowly, which allows a near ZCS turn OFF for S_2 and S_3 .

2.3 Converter Analysis

2.3.1 PFC Boost Converter

The bridgeless AC/DC rectifier operates in DCM operational mode. As the result, the input voltage v_{in} and input current i_{in} are in-phase with near unity power factor. The input voltage and current of the converter can be given as below, where R_e is the emulated resistance and ω_g is the grid angular frequency.

$$i_{in} \cong \frac{v_{in}}{R_e} \quad (2.4)$$

$$v_{in} = V_M \sin(\omega_g t) \quad (2.5)$$

$$R_e = \frac{v_{in,rms}^2}{P_{av}} \quad (2.6)$$

Since the PFC boost converter operates in DCM operational mode, the average boost inductor current should be less than the current ripple. Therefore, the condition for DCM operation of the front-end PCF boost converter is as below:

$$\langle i_b(t) \rangle_{T_{sw}} < \frac{\Delta i_b(t)}{2} \quad (2.7)$$

where $\langle i_b(t) \rangle_{T_{sw}}$ is the average current flowing through the PFC boost inductor (L_b) and $\langle i_b(t) \rangle_{T_{sw}}$ is it's current ripple which are given below:

$$\langle i_b(t) \rangle_{T_{sw}} = \frac{|v_{in}(t)|}{R_e} \quad (2.8)$$

$$\Delta i_b(t) = \frac{|v_{in}(t)|}{L_b} D_p T_{sw} \quad (2.9)$$

this is while for the CCM operation of the converter, where the average inductor current is higher than its current ripple, the duty ratio should vary as below:

$$D_p(t) = 1 - \frac{|v_{in}(t)|}{0.5V_{DC-link}} \quad (2.10)$$

substituting (2.8)-(2.10) into (2.7) leads to the condition for the DCM operation of the PFC inductor as below:

$$L_b < \frac{(1 - \frac{2V_M}{V_{DC-link}} R_e)}{2f_{sw}} \quad (2.11)$$

Based on the steady-state equivalent model of the boost converter [85], the voltage gain of the boost converter during DCM operation is as below:

$$G_B(t) = \frac{0.5V_{DC-link}}{|v_{in}(t)|} = 1 + \frac{D_p^2}{\frac{4L_b f_{sw}}{V_{DC-link}} i_{in}(t)} \quad (2.12)$$

Considering $i_{in,norm} = (4L_b f_{sw}/V_{DC-link}) i_{in}(t)$, the normalized gain of the boost converter during DCM operation can be shown as below:

$$G_B(t) = \frac{0.5V_{DC-link}}{|v_{in}(t)|} = 1 + \frac{D_p^2}{i_{in,norm}} \quad (2.13)$$

Fig. 2.4 shows a 3-D diagram that illustrates the relationship between the normalized gain ($G_{B,norm}$), duty ratio (D_p), and normalized input current of the PFC boost inductor ($i_{in,norm}$). The white separating surface in Fig 2.4 shows the Boundary Conduction Mode (BCM) of the front-end PFC boost converter. In BCM, the DCM gain of the converter in (2.13) is equal to CCM gain of the converter which is $1/(1 - D_p(t))$. Therefore, the condition for BCM operation of the front-end PFC boost converter is as below:

$$i_{in,norm} G_B^2 - G_B + 1 = 0 \quad (2.14)$$

From Fig. 2.4, it can be seen that using the duty ratio of $D_p = 0.5$, the converter remains in DCM operational mode with the widest range of input current. According to Fig. 2.4, when the sinusoidal input voltage $v_{in}(t)$ nears zero ($G_B(t)$ becoming infinite), the converter is more likely to operate in DCM. Conversely, as $v_{in}(t)$ reaches its maximum value (V_M) ($G_B(t)$ converging to 1), the converter is inclined to operate in CCM. This indicates that at the peak of the input AC voltage, the boost rectifier can operate in CCM. In the scenario where the bridgeless boost converter is designed to operate in DCM, encountering CCM at the voltage peak can lead to spikes in current and harmonic distortion. An instance of this scenario is depicted in Fig. 2.5 [86]. Such conditions might also arise under situations of output overload. Furthermore, it is important to recognize that while employing DCM in the converter can ensure PFC, this method introduces challenges, including heightened peak currents in DCM and the requirement for extra filtering to manage the high-frequency fluctuating input currents. Nonetheless, the advantages of reduced inductance, zero-current activation for the switch, and the absence of reverse recovery in the diode during DCM occasionally make DCM a preferred operation mode for step-up DC-DC converters [86], [87].

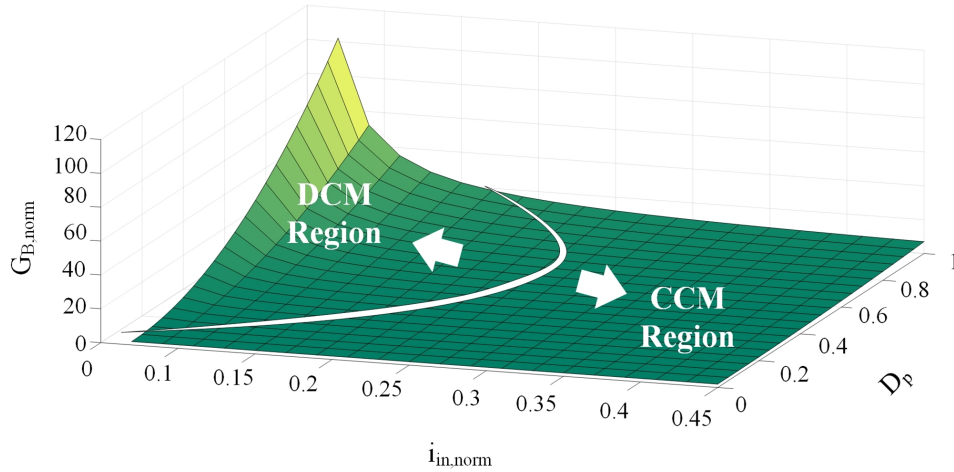


Figure 2.4: Conditions for DCM and CCM operation of the front-end PFC boost rectifier.

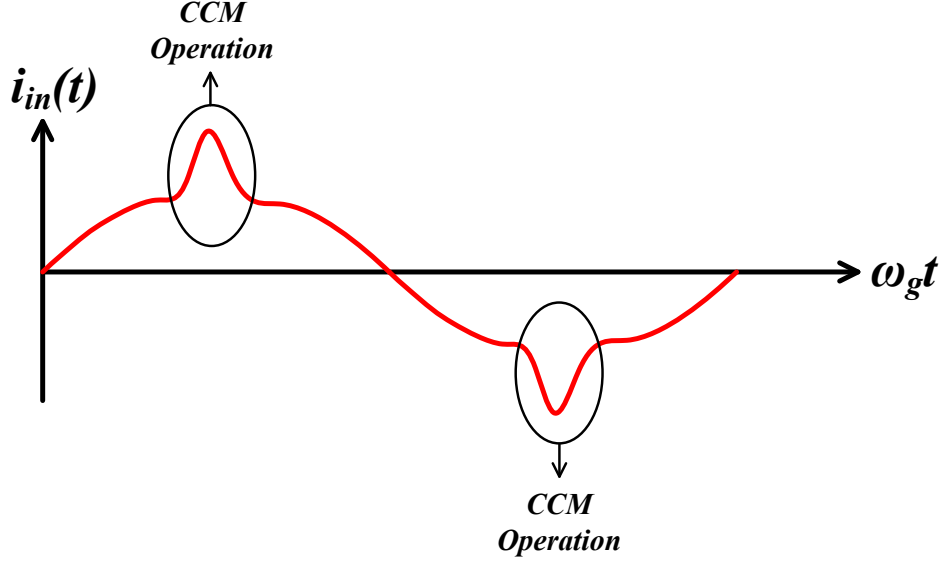


Figure 2.5: Input current example of the DCM PFC converter operating in CCM at the peak of the input voltage.

2.3.2 Maximum and RMS Switch Currents

During the positive half-cycle of the input voltage v_{in} , switches S_1 and S_2 are responsible for carrying both the boost inductor current and the resonant current, while S_3 and S_4 only carry the resonant current. This operational characteristic can be observed in Fig. 2.3. Specifically, the antiparallel diode of S_1 in the interval $[t_0 < t < t_2]$ and the switch S_2 in the interval $[t_5 < t < t_8]$ must handle both the boost inductor current and the resonant current. A similar situation occurs for the antiparallel diode of S_4 and the MOSFET S_3 during the negative cycle of the input voltage. This means that the peak currents of the antiparallel diodes of S_1 and S_4 , and the peak currents of S_2 and S_3 must be considered during the design of the bridgeless boost converter. Because of the converter's symmetrical operation, $i_{S2,max} = i_{S3,max}$ and $i_{S1,min} = i_{S4,min}$. As shown in Fig. 2.3, the maximum current going through S_2 is the sum of $i_{res,max}$ and $i_{b,max}$.

To perform steady-state analysis of the topology, the following assumptions are made: (1) all components, including semiconductor switches and diodes, are ideal, (2) the delay between the switches gating signals is neglected, and (3) the effect of snubber capacitors is ignored. The Fourier series representation

of the input voltage to the resonant circuit v_{res} is given by (2.15). Due to the DC blocking function of C_p , only the AC components of v_{res} are applied to the resonant circuit, where $V_{DC-link}$ is the DC-link voltage.

$$v_{res} = V_{DC-link}D_p + \sum_{h=1}^{\infty} \left(\frac{\sqrt{2}V_{DC-link}}{h\pi} \sqrt{1 - \cos(2h\pi D_p)} \sin(2\pi h f_{sw} t + \theta_h) \right) \quad (2.15)$$

$$\theta_h = \tan^{-1} \left(\frac{\sin(2\pi h D_p)}{1 - \cos(2\pi h D_p)} \right) = \frac{\pi}{4} - \pi D_p \quad (2.16)$$

in (2.15) and (2.16), harmonic order is shown by h . Moreover, the relative angular frequency (ω_r) is given by (2.17), where ω_{sw} , ω_0 , and Q represent angular switching frequency, angular resonant frequency, and quality factor, respectively.

$$\omega_r = \frac{\omega_{sw}}{\omega_0} \quad (2.17)$$

$$\omega_0 = \frac{1}{\sqrt{L_m C_p}} \quad (2.18)$$

$$Q = \frac{R_{ac}}{L_m \omega_0} \quad (2.19)$$

The resonant current i_{res} can be calculated from v_{res} in (2.15) as below:

$$i_{res} = \sum_{h=1}^{\infty} \left(\frac{\sqrt{2}V_{DC-link}}{h\pi |Z_{i,h}|} \sqrt{1 - \cos(2h\pi D_p)} \sin(2\pi h f_{sw} t + \theta_h) \right) \quad (2.20)$$

where $Z_{i,h}$ can be calculated as below:

$$|Z_{i,h}| = R_{ac} \sqrt{\frac{(k + 1 + \frac{1}{m}(1 - \frac{1}{h^2 \omega_r^2}) - k\omega_r^2)^2 + (hQ\omega_r(1 - \frac{1}{h\omega_r^2}))^2}{Q^4 + (hQ\omega_r(k + 1 - \frac{1}{mh\omega_r^2}))^2}} \quad (2.21)$$

$$\begin{aligned} \phi_{Z_{i,h}} &= \tan^{-1} \left(\frac{hQ\omega_r \left(1 - \frac{1}{h\omega_r^2}\right)}{k + 1 + \frac{1}{m} \left(1 - \frac{1}{h^2 \omega_r^2}\right) - k\omega_r^2} \right) \\ &= -\tan^{-1} \left(\frac{h\omega_r \left(k + 1 - \frac{1}{mh\omega_r^2}\right)}{Q} \right) \end{aligned} \quad (2.22)$$

where $k = L_r/L_m$ is defined as the ratio between secondary-side and magnetizing inductance, and $m = C_s/C_p$ is defined as the ratio between secondary-side and primary-side capacitances. Moreover, R_{ac} is the equivalent resistance seen by the resonant circuit and considering $D_s = 0$, where leg B act like a half-wave rectifier, R_{ac} can be defined as (2.23) where R_L is the load.

$$R_{ac} = \frac{8}{\pi^2} R_L \quad (2.23)$$

However, since two middle switches S_5 and S_6 in leg B are switching at the same frequency of the switches in leg A (f_{sw}), the equivalent resistance (R_{ac}) varies based on the secondary-side duty ratio (D_s) which can later help to control the gain of the converter. The equivalent resistance (R_{ac}) in this case can be approximated as below:

$$R_{ac} = \frac{8}{\pi^2} (1 - D_s)^2 R_L \quad (2.24)$$

As a result, the peak currents of the switches S_2 and S_1 based on first harmonic approximation ($h = 1$) can be calculated as shown in (2.25).

$$\begin{aligned} i_{S_2,max} &= -i_{S_1,max} = i_{res,max} + i_{b,max} \\ &= \frac{\sqrt{2}V_{DC-link}}{\pi|Z_{in}|} \sqrt{1 - \cos(2\pi d)} + \frac{V_M}{L_b} D_p T_{sw} \end{aligned} \quad (2.25)$$

Moreover, the peak currents of the switches S_5 and S_6 based on first harmonic approximation ($h = 1$) can be calculated as shown in (2.26).

$$\begin{aligned} i_{S_5,max} &= i_{S_6,max} = i_{res,max} \\ &= \frac{\sqrt{2}V_{DC-link}}{\pi|Z_{in}|} \sqrt{1 - \cos(2\pi d)} \end{aligned} \quad (2.26)$$

2.3.3 Voltage Gain

The overall voltage gain of the bridgeless single-stage AC/DC converter is the multiplication of the gains of the front-end PFC boost converter, stacked switch converter, CLLC resonant circuit, and HF half-wave rectifier. Since the switching frequency of the converter is much higher than the input voltage frequency, the input voltage (v_{in}) can be considered constant during each

switching period T_{sw} . Therefore, the gain of the PFC boost converter operating in DCM can be calculated as (2.27).

$$\frac{V_{DC-link}}{V_M} = 1 + \sqrt{1 + \frac{2D_p^2 R_e}{L_B f_{sw}}} \quad (2.27)$$

Based on (2.15), the RMS value of the input voltage to the resonant circuit (v_{res}) can be calculated as (2.28).

$$\frac{v_{res}}{V_{DC-link}} = \frac{1}{\pi} \sqrt{\sum_{n=1}^{\infty} \frac{1 - \cos(2n\pi D_p)}{n^2}} \quad (2.28)$$

Based on the designed control system shown in section IV, the duty ratio of the stacked switches in leg A will be slightly changing around $D_p = 0.5$, following the input voltage frequency ($f_g = 60Hz$). Therefore, considering the average value of $D_p = 0.5$ to further simplify the voltage gain equation, the RMS value give in (2.28) can be simplified as shown in (2.29).

$$\frac{v_{res}}{V_{DC-link}} = \frac{\sqrt{2}}{\pi} \sqrt{\sum_{n=1,3,5,\dots}^{\infty} \frac{1}{n^2}} = \frac{1}{2} \quad (2.29)$$

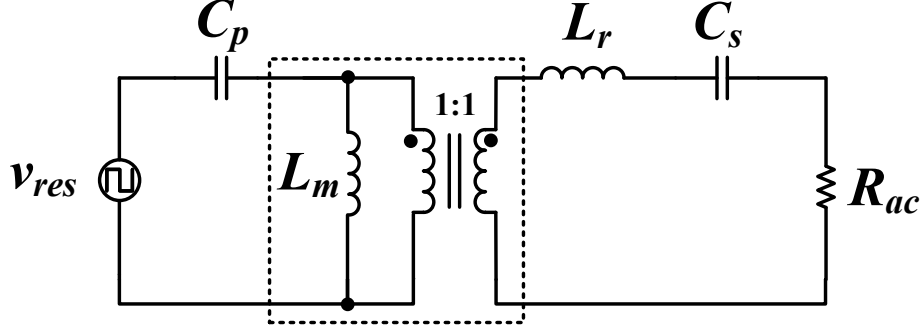


Figure 2.6: Equivalent circuit of the CLLC resonant circuit in the AC/DC converter.

The equivalent circuit of the CLLC resonant circuit is given in Fig. 2.6. By ignoring the higher order harmonics, the voltage gain of the CLLC resonant circuit can be calculated as (2.30).

$$\frac{v_p}{v_{res}} = \frac{\omega_r^2}{\sqrt{(\omega_r^2 - 1)^2 + \frac{1}{Q^2} \left(k\omega_r^3 - \frac{\omega_r}{m} - k\omega_r + \frac{1}{m\omega_r} - \omega_r \right)^2}} \quad (2.30)$$

As the result, total voltage gain of the converter considering an average value of 0.5 for the duty ratio of the switches in leg A (D_p) is given in (2.31).

$$\frac{v_o}{V_M} = \frac{\omega_r^2 \left[1 + \sqrt{1 + \frac{2D_p^2 R_e}{L_b f_{sw}}} \right]}{2 \sqrt{(\omega_r^2 - 1)^2 + \frac{1}{Q^2} \left(k\omega_r^3 - \frac{\omega_r}{m} - k\omega_r + \frac{1}{m\omega_r} - \omega_r \right)^2}} \quad (2.31)$$

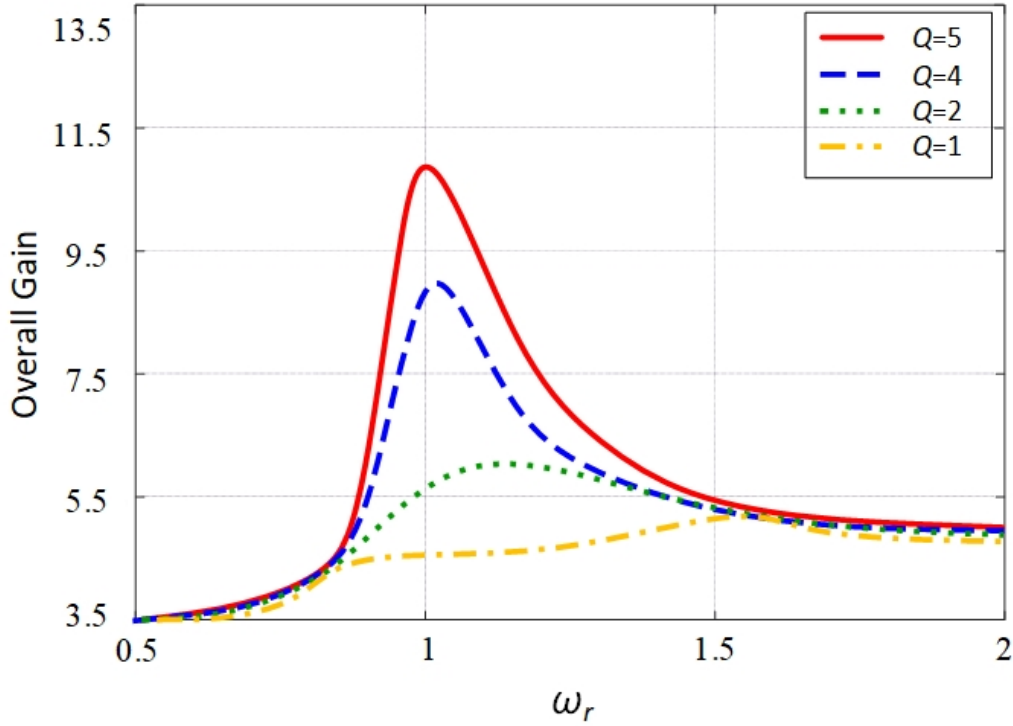


Figure 2.7: Overall voltage gain plot of the converter for $D_s = 0$ for $m = 10$ and $k = 0.8$.

The overall voltage gain of converter in the absence of the HF switches in leg B (i.e. $D_s = 0$) is illustrated in Fig. 2.7 for $k = 10$ and $m = 0.8$ and different quality factors (Q). On the other hand, in the bridgeless rectifier where the two switches S_5 and S_6 in leg B are switching with the same frequency as the switches in leg A (f_{sw}) and with $D_s > 0$; R_{ac} (see (2.24)), and therefore, quality factors changes below:

$$Q = \frac{R_{ac}}{L_m \omega_0} (1 - D_s)^2 = Q(1 - D_s)^2 \quad (2.32)$$

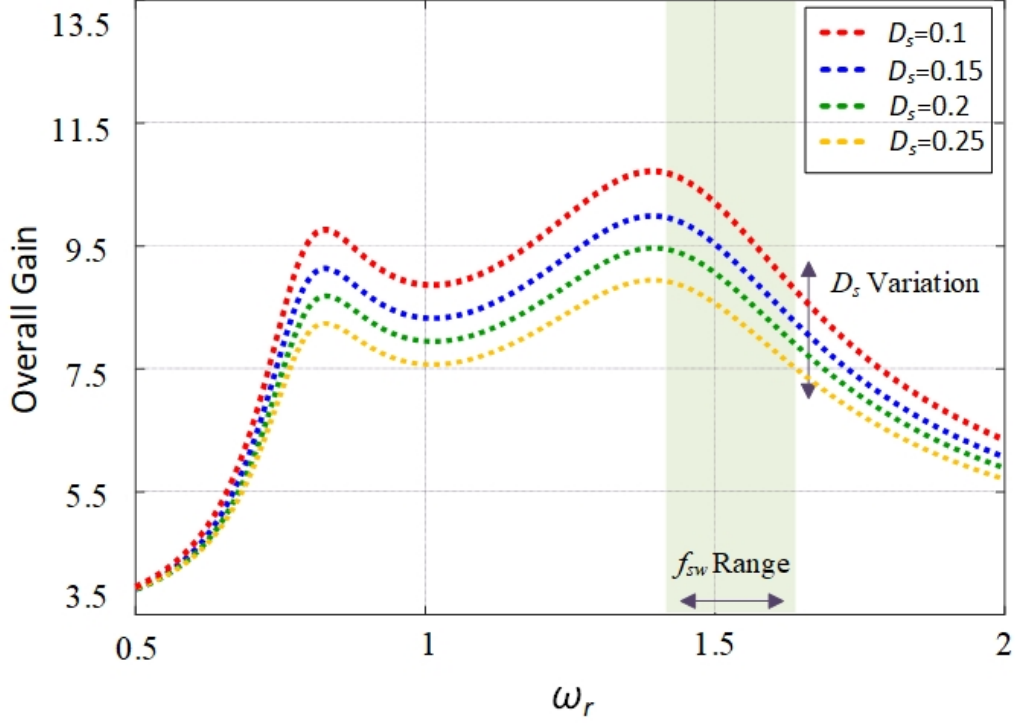


Figure 2.8: Overall voltage gain plot of the converter for $D_s > 0$.

As the result, the overall gain of the converter becomes dependant to the duty ratio of the switches in leg B (D_s) as presented in (2.33).

$$\frac{v_o}{V_M} = \frac{\omega_r^2 \left[1 + \sqrt{1 + \frac{2D_s^2 R_e}{L_b f_{sw}}} \right]}{2 \sqrt{(\omega_r^2 - 1)^2 + \frac{1}{Q^2(1-D_s)^4} \left(k\omega_r^3 - \frac{\omega_r}{m} - k\omega_r + \frac{1}{m\omega_r} - \omega_r \right)^2}} \quad (2.33)$$

Fig. 2.8 demonstrates the overall gain plot of the converter when $D_s > 0$. It can be seen that in this way, the overall gain of the converter can be controlled using D_s and independent of leg A, which later will be used in the controller to help the converter to achieve a reduced output voltage ripple. Details of the designed controller is explained in Section IV.

2.4 Control System Design

As mentioned in the pervious sections, achieving high-quality sinusoidal input current, having a reduced output voltage ripple while critically reducing the

converter's storage capacitances, and ensuring voltage regulation are crucial for efficient and reliable operation of EV systems. These factors greatly influence the performance, longevity, and overall functionality of EV systems. This section presents the designed control system that will help the converter achieve the aforementioned objectives.

Moreover, it is worth mentioning that each of these objectives is addressed through distinct and independently developed control loops within our system. This approach ensures that the input current shaping, output voltage ripple control, and voltage regulation are not only individually optimized but also function cohesively without interference from one another.

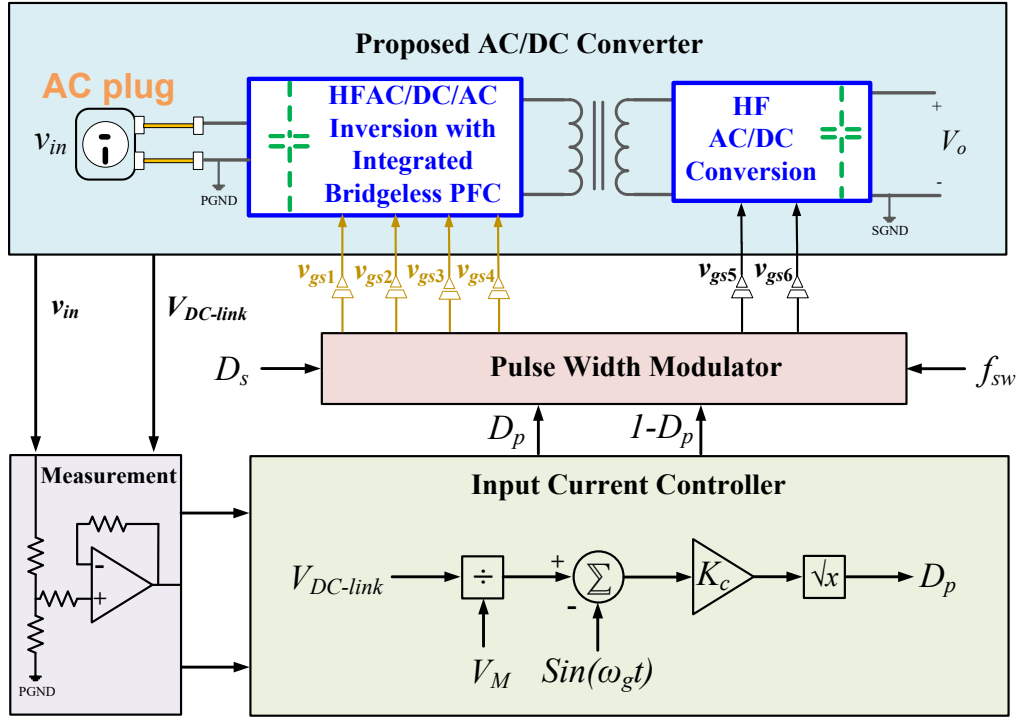


Figure 2.9: Block diagram of the developed input current controller for the converter.

2.4.1 Input Current Control

As stated throughout the paper, the PFC boost stage in the bridgeless AC/DC converter operates in DCM operational mode. In this mode, the AC line voltage and current are in phase and have a near unity power factor. From

(2.12), the average input current of the PFC boost converter can be calculated as below:

$$i_{in} = \frac{V_{DC-link} T_p D_p^2 \sin(\omega_g t)}{2L_b \left(\frac{V_{DC-link}}{v_{in}} - \sin(\omega_g t) \right)} \quad (2.34)$$

The input current shown in (2.34) indicates that the average input current of the converter will not be purely sinusoidal. However, as it is clear in (2.34), it is possible to achieve a high-quality sinusoidal input current (i_{in}) by properly controlling the primary-side duty ratio D_p so that the destructive term $V_{DC-link}/v_{in} - \sin(\omega_g t)$ in the denominator of (2.34) be eliminated. To that end, the primary-side duty ratio (D_p) is chosen as (2.35).

$$D_p = \sqrt{\frac{V_{DC-link}}{v_{in}} - \sin(\omega_g t)} \quad (2.35)$$

In this way, by implementing a closed-loop control system as shown in Fig. 2.9, the denominator term in (2.34) will be canceled-out and the input current will become purely sinusoidal.

However, in this converter that the bulky DC-link capacitors are replaced with smaller ones, the DC-link voltage has more fluctuation which results in higher voltage ripple in the output of the converter. Moreover, since the converter is designed to operate in DCM, CCM operation of the converter at the peak of the input current can result in current spikes, harmonic distortion, and hard-switching operation of the switches in leg A. Therefore, as the duty ratio of the primary-side switches (D_p) is set to vary based on (35), it should be also controlled to counteract the fluctuations in DC-link voltage as a result of using reduced DC-link capacitances which negatively impact the input current and prevent the converter from going to CCM operation considering the conditions described in Section III.A. As the result, for a better duty ratio control and to further weaken DC-link voltage fluctuation and maintain the input current quality and DCM operation of the converter, the duty ratio of the primary-side switches has been considered to be as (2.36).

$$D_p = \sqrt{K_c \left(\frac{V_{DC-link}}{v_{in}} - \sin(\omega_g t) \right)} \quad (2.36)$$

The parameter K_c in (2.36) is tuned properly to lower the DC-link voltage ripple, increasing input current quality, and maintain the DCM operation of the converter and to guarantee soft-switching by forcing D_p to change in a pre-defined interval. Using the (D_p) defined in (2.36) the input current of the converter (i_{in}) can be re-defined as presented in (2.37), which is purely sinusoidal as the result of using the closed-loop control system. Moreover, it is clear from (2.36) and (2.37) that the input current is shaped independent from other control loops.

$$i_{in} = \frac{V_{DC-link} K_c T_p}{2L_b} \sin(\omega_g t) \quad (2.37)$$

2.4.2 Output Voltage Regulation

As shown in Fig. 2.10, to provide output voltage regulation for the AC/DC converter during its operation, Variable Frequency Modulation (VFM) technique has been utilized. Moreover, the designed VFM-based controller is developed to be solely responsible for output voltage regulation to avoid a never-ending frequency variation (which can cause stability issues) due to the high output voltage ripple of the converter as a result of using small DC-link and output filter capacitors. To that end, the output voltage of the converter is first fed to a Low-Pass Filter (LPF) to remove the low-frequency ripples and then the filtered voltage is compared with a reference value ($V_{o,ref} = 800V_{dc}$) to generate the error signal (see Fig. 2.10). In this way, the output voltage ripple does not affect this control loop, and therefore, the switching frequency of the converter.

Then the generated error signal is fed to a PI controller to generate the required control signal which is in this case, is the switching frequency (f_{sw}). Moreover, the PI controller gains (K_{io} and K_{po}) shown in (2.38) are calculated based on the fundamental harmonic approximation (FHA) and using Control System Analysis Toolbox in MATLAB.

It is worth to mention that there exist two subsystems in the overall close-loop system that have different operating frequencies: 1) the designed bridgeless AC/DC converter that is working with a very high frequency ($f_{sw} \approx$

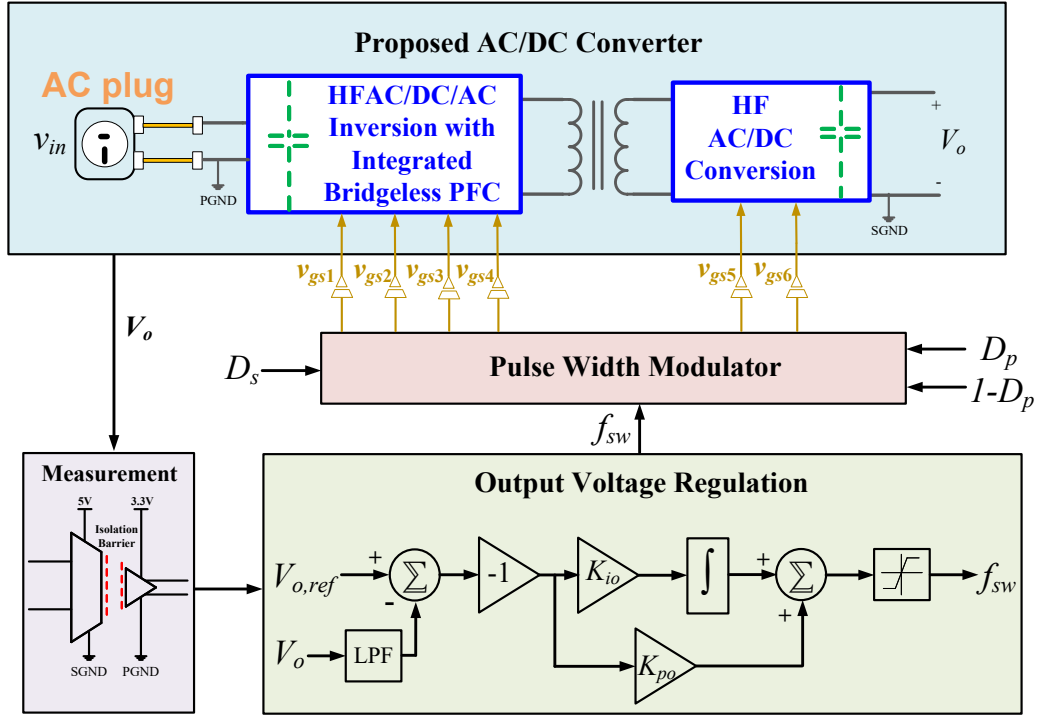


Figure 2.10: Block diagram of the developed VFM-based output voltage regulation controller for the converter.

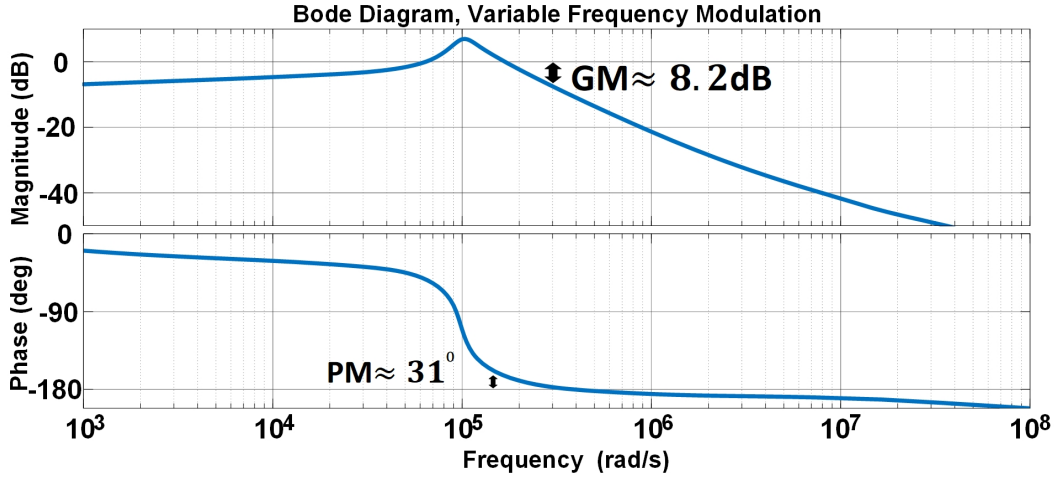


Figure 2.11: Bode diagram of the closed-loop system for the developed VFM-based controller.

100kHz), 2) the designed VFM-based PI controller which is working with low frequency. In control systems theory, when there exist subsystems interacting with each other and are working with different operating frequencies; using the complete model of the subsystem that is working with high operating fre-

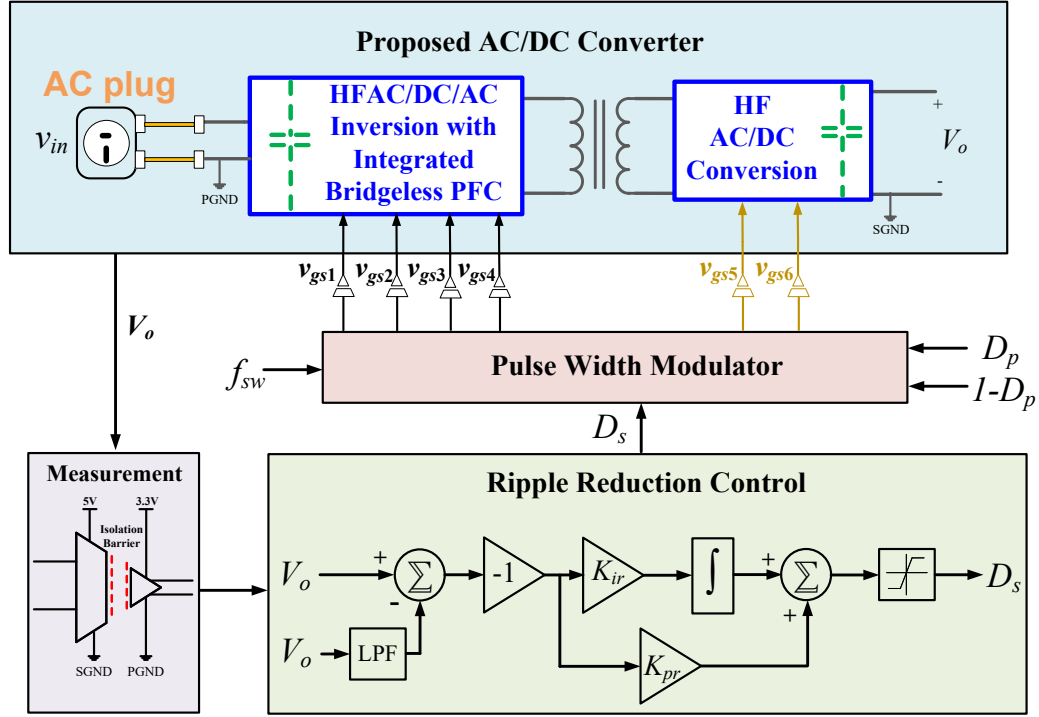


Figure 2.12: Block diagram of the developed ripple reduction controller for the converter.

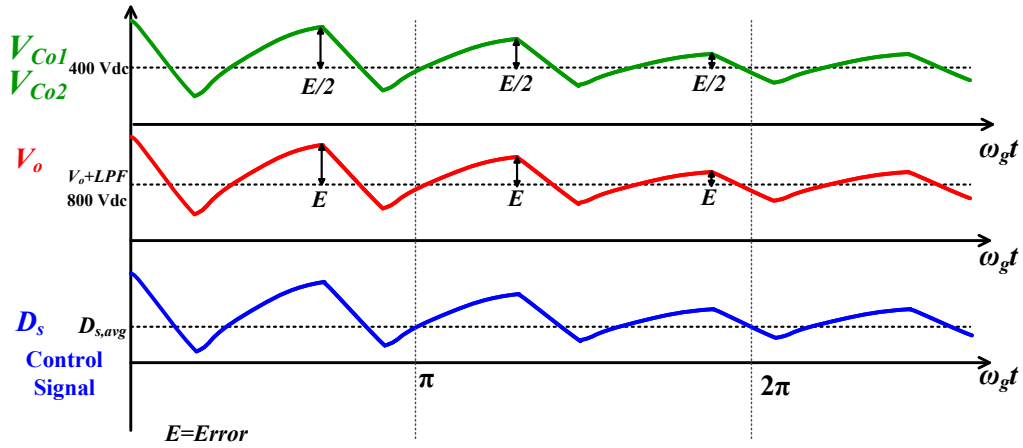


Figure 2.13: Ripple Reduction Control key waveforms.

quency only complicates the overall model of the closed-loop system and using an average model of the system is sufficient for designing the low frequency (PI) controller . [88]-[89]. Therefore, using FHA model is sufficient to design the PI controllers for output voltage regulation of the designed converter.

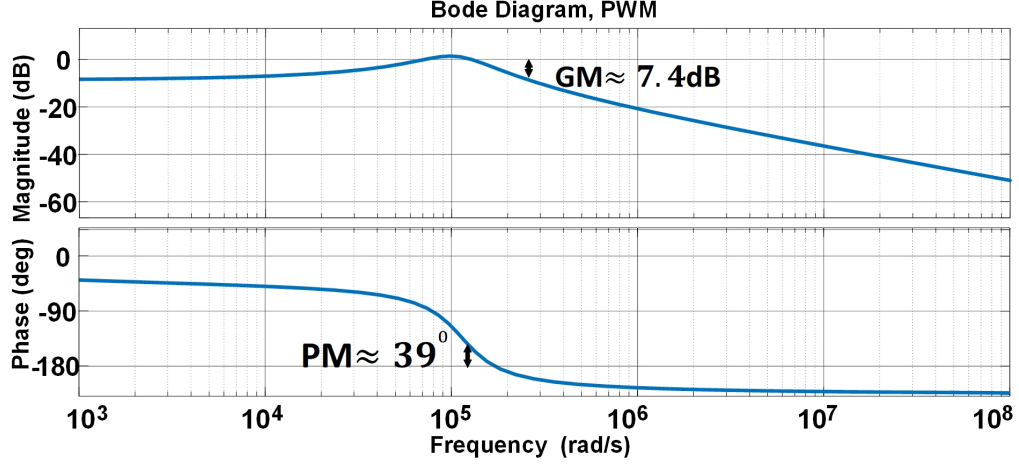


Figure 2.14: Bode diagram of the closed-loop system for the developed ripple reduction controller.

To that end, a PI controller in the form of (2.38) is developed for output voltage regulation. First, to cancel-out the destructive effect of the PI's pole at zero, PI's zero should be considered close to the origin. Therefore, $K_{io}/K_{po} = 125 \times 10^{-6}$ has been considered. Moreover, considering the output range of the VFM controller ($f_{sw} \approx 100kHz$), the proportional gain of the PI controller is considered as $K_{po} = 800$. As the result, $K_{io} = 0.1$ can be calculated. The bode diagram of the closed-loop system is illustrated in Fig. 2.11, where phase margin and gain margin are 31° and 2.8dB, respectively.

$$C_o(s) = K_{po} + \frac{K_{io}}{s} \quad (2.38)$$

2.4.3 Output Voltage Ripple Reduction

As shown in Fig. 2.12, to reduce the high output voltage ripple of the designed converter which occurs as a result of using low storage capacitances, a closed-loop controller based on Pulse Width Modulation (PWM) technique has been utilized. The designed PWM-based controller is developed to be solely responsible for output voltage ripple reduction using the switches S_5 and S_6 in leg B of the designed topology. To design the output voltage ripple reduction controller independent of the designed VFM controller, it is important to make an error signal solely as a result of output voltage ripple. To that end, the actual output of the converter is compared with the LPF fed output of the converter

as illustrated in Fig. 2.12 and Fig. 2.13. As the result, this loop operates independently, focusing solely on ripple minimization. Then, the calculated error signal is fed to a PI controller to generate the required control signal which in this case, is the duty ratio (D_s) of the switches S_5 and S_6 in leg B of the converter. Moreover, the PI controller gains (K_{ir} and K_{pr}) shown in (2.39) are calculated based on the fundamental harmonic approximation (FHA) and using Control System Analysis Toolbox in MATLAB.

$$C_o(s) = K_{pr} + \frac{K_{ir}}{s} \quad (2.39)$$

Considering the fact that the error signal in this case is the output voltage ripple ($E = Ripple$), the control signal (D_s) generated by (2.39) can be defined in (2.40).

$$D_s(t) = K_{pr}Ripple(t) + K_{ir} \int_0^t Ripple(\tau)d\tau \quad (2.40)$$

Now combining the time-varying D_s and equivalent resistance (R_{ac}) defined in (2.24) results in (2.41).

$$R_{ac} = \frac{8}{\pi^2} \left(1 - \left[K_{pr}Ripple(t) + K_{ir} \int_0^t Ripple(\tau)d\tau \right]^2 \right) R_L \quad (2.41)$$

As a result, by properly choosing the PI controller gains (K_{pr} and K_{ir}), the equivalent resistance (R_{ac}), and therefore, the overall gain of the converter can be controlled to minimize the output voltage ripple enabling the converter to utilized low storage capacitances.

Similar to the designed VFM controller, there exist two subsystems in the overall close-loop system with different operating frequencies: 1) the designed bridgeless AC/DC converter that is working with a very high frequency ($f_{sw} \approx 100kHz$), 2) the designed PWM-based PI controller which is working with low frequency. Similar to the discussion in VFM controller design, using an average model of the system is sufficient for designing the low frequency (PI) controller used for output voltage ripple reduction [88]-[89]. Therefore, using FHA model is sufficient to design the PI controllers.

To that end, a PI controller in the form of (2.38) is developed for output voltage regulation. First, to cancel-out the destructive effect of the PI's pole at zero, PI's zero should be considered close to the origin. Therefore, $K_{io}/K_{po} = 10^{-3}$ has been considered. Moreover, considering the output range of the PWM-based controller, the proportional gain of the PI controller is considered as $K_{pr} = 0.01$. As the result, $K_{ir} = 0.00001$ can be calculated. The bode diagram of the closed-loop system is illustrated in Fig. 2.14, where phase margin and gain margin are 39° and 7.4dB, respectively.

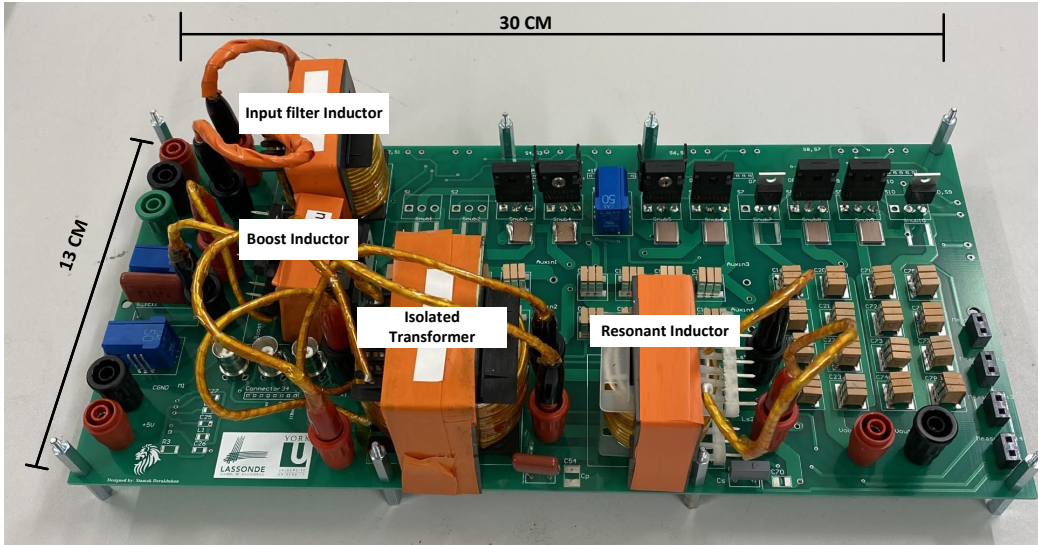


Figure 2.15: Picture of the Proof-of-concept Prototype.

2.5 Experimental Validation

To verify the performance of the designed bridgeless AC/DC converter and the effectiveness of the designed control system, a proof-of-concept hardware prototype has been developed and tested in the laboratory using a $1.1kW$, $120V_{rms}/800V_{dc}$, $100 - 120kHz$ SiC-based design. Moreover, PLECS RT Box 1 is used as the controller unit. Fig. 2.15 shows a picture of the hardware prototype, while Table I shows the system specification and system parameters.

Table 2.1: Parameter Values of the Designed Prototype

Parameters	Values
Rated Power (P_o)	$1.1kW$
Output Voltage (V_o)	$800V_{dc}$
Input AC Voltage (v_{in})	$90 - 135V_{ac,rms}$
Switching Frequency (f_{sw})	$\geq 100kHz$
Input Filter Inductance (L_{in})	$550\mu H$
Input Filter Capacitance (C_{in})	$0.8\mu F$
Boost Inductance (L_b)	$20\mu H$
DC-link Capacitances (C_{i1}, C_{i2})	$25\mu F$
Primary Resonant Capacitance (C_p)	$0.068\mu F$
Secondary Resonant Capacitance (C_s)	$0.68\mu F$
Resonant Inductance (L_r)	$260\mu H$
Magnetizing Inductance (L_m)	$270\mu H$
Output Filter Capacitances (C_{o1}, C_{o2})	$25\mu F$
Switches ($S_1 - S_6$)	IMW65R030M1HXKSA1
Diodes ($D_1 - S_4$)	GP3D005A170B

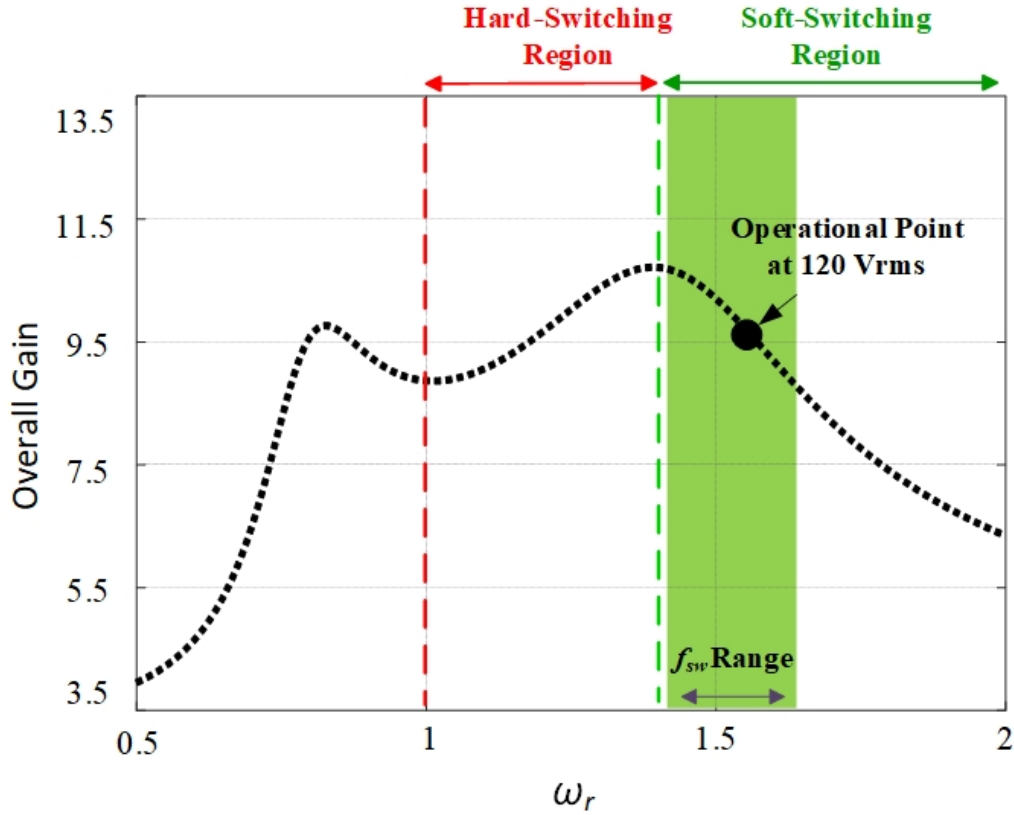


Figure 2.16: Soft-switching region of the designed converter.

2.5.1 Design Procedure

Since the drain-source breakdown voltage of the IMW65R030M1HXKSA1 switches is 650V and the stress of voltage across switches is half of the DC-link voltage, The maximum switch voltage is designed to be 500V, making DC-link voltage $V_{DC-link} = 1000$. According to Fig. 2.16, the bottom limit for the switching frequency happens around $\omega_r = 1.45$. Therefore, to design the converter to operate with the switching frequency $f_{sw} \geq 100kHz$, the base frequency of the resonant circuit is set to $f_0 = 70kHz$. The specification and parameters of the prototype are given in Table I based on the following:

$$R_e = \frac{V_M^2}{2P_o} = 40\Omega \quad (2.42)$$

$$L_b < \frac{(1 - \frac{V_M}{V_{DC-link}})R_e}{2f_{sw}} \Rightarrow L_b < 30\mu H \Rightarrow L_b = 20\mu H \quad (2.43)$$

$$R_{load} = \frac{V_o^2}{P_o} = 640\Omega \quad (2.44)$$

$$R_{ac} = \frac{8}{\pi^2} R_{load} = 519.29\Omega \quad (2.45)$$

$$L_m = \frac{R_{ac}}{Q2\pi f_0} \approx 270\mu H \quad (2.46)$$

$$L_s = kL_m \approx 260\mu H \quad (2.47)$$

$$C_p = \frac{1}{L_m \omega_0^2} \approx 0.068\mu H \quad (2.48)$$

$$C_s = mC_p \approx 0.68\mu H \quad (2.49)$$

$$f_{sw} = 1.45 \times f_0 \approx 100kHz \quad (2.50)$$

The soft-switching region of the converter, as outlined by the design procedure, is depicted in Fig. 2.16. The frequency range within which switches operate under soft-switching conditions is highlighted in light green in Fig. 2.16. Furthermore, the operational point of the converter, with an input voltage of 120Vrms, is marked on the converter's voltage gain curve within Fig. 2.16. Variations in input voltage or load conditions may cause this operational point to shift either left or right. Such shifts result from alterations in

the switching frequency, as adjusted by the output voltage controller to maintain the voltage at its reference value. Excessive shifting towards the right may lead to inefficiency due to increased negative current, while shifting too far to the left, beyond the converter's operational range, may induce hard-switching conditions. It is important to note that the designated soft-switching region is based on a specific operational range considered for the converter, which can be adjusted to accommodate different operational ranges as required by the user.

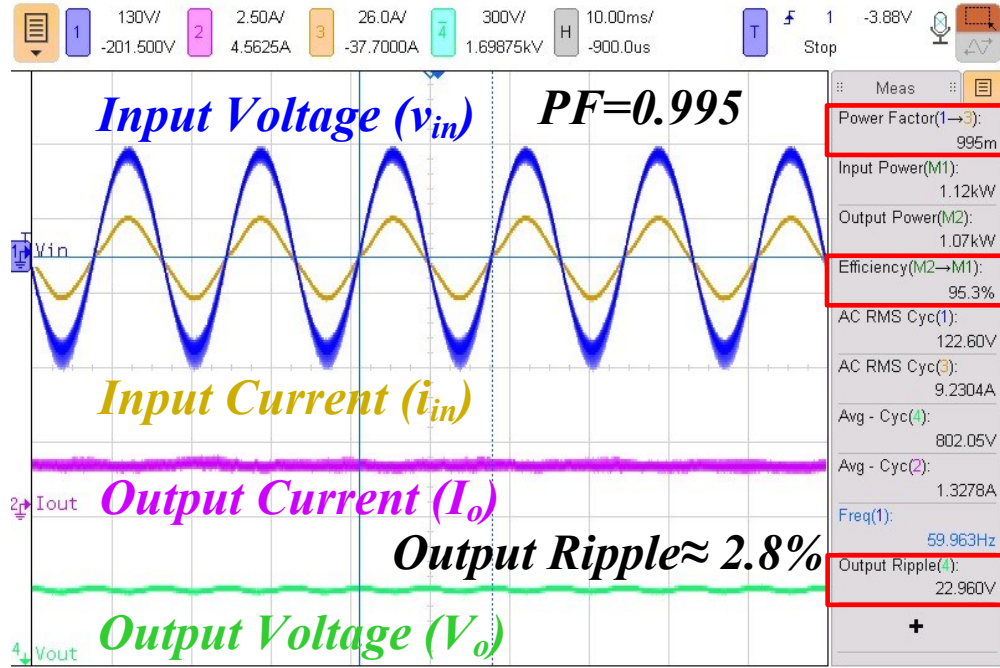


Figure 2.17: Input and Output waveforms of the converter at rated power.

2.5.2 Steady-State Experimental Results

The steady-state experimental waveforms obtained from the prototype are shown in Figs. 3.19–2.24. Fig. 3.19 illustrates input voltage (v_{in}), input current (i_{in}), output voltage (V_o), and output current (I_o) waveforms at $120V_{ac,rms}$ input and $800V_{dc}$ output voltage. As can be seen in Fig. 3.19, the input power factor is $PF = 0.993$ and the developed converter achieved efficiency of 95.6 at around 1.1kW power which was measured by “power analysis tool” from the

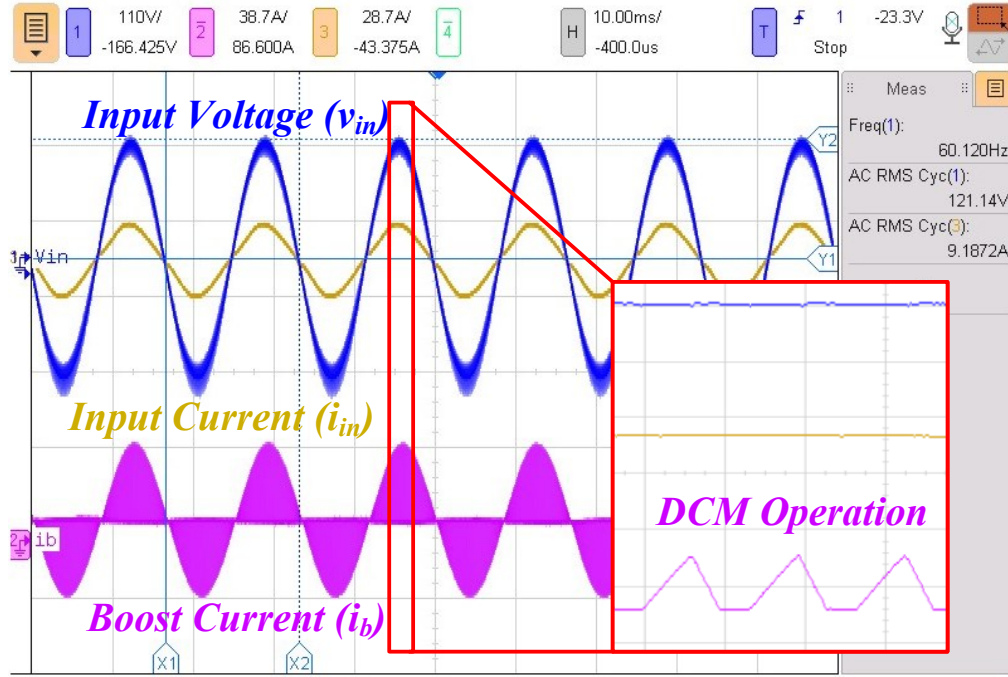


Figure 2.18: Input voltage, input current, and boost inductor current waveforms.

KEYSIGHT MSOX6004A oscilloscope.

Moreover, Fig. 2.18 illustrates the boost inductors current (i_b) of the designed front-end PFC circuit along with input voltage (v_{in}) and input current (i_{in}). It can be seen that using the calculated boost inductance at the chosen switching frequency and power level, the PFC circuit operates in DCM as desired.

The switches S_1 , S_2 , and S_6 voltage and current waveforms at line and switching frequency are shown in Figs. 3.20-2.24. Each switch current in the designed bridgeless converter has a low-frequency envelope and therefore, the soft-switching operation of each switch needs to be verified in both positive and negative line cycles. Due to the similar operation of the switches S_1 and S_4 , S_2 and S_3 , and S_5 and S_6 , showing the switching waveforms for S_1 , S_2 , and S_6 would be sufficient to confirm the soft-switching performance of the converter.

The voltage and current waveforms of switch S_1 at line frequency are shown

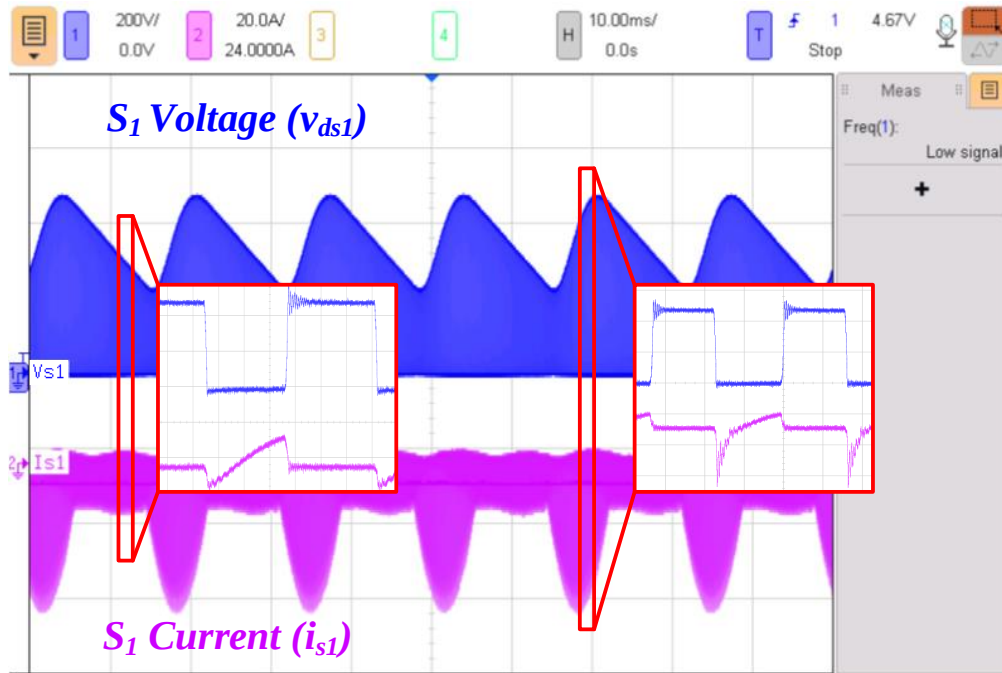


Figure 2.19: Voltage over and current flowing through S_1 at line frequency.

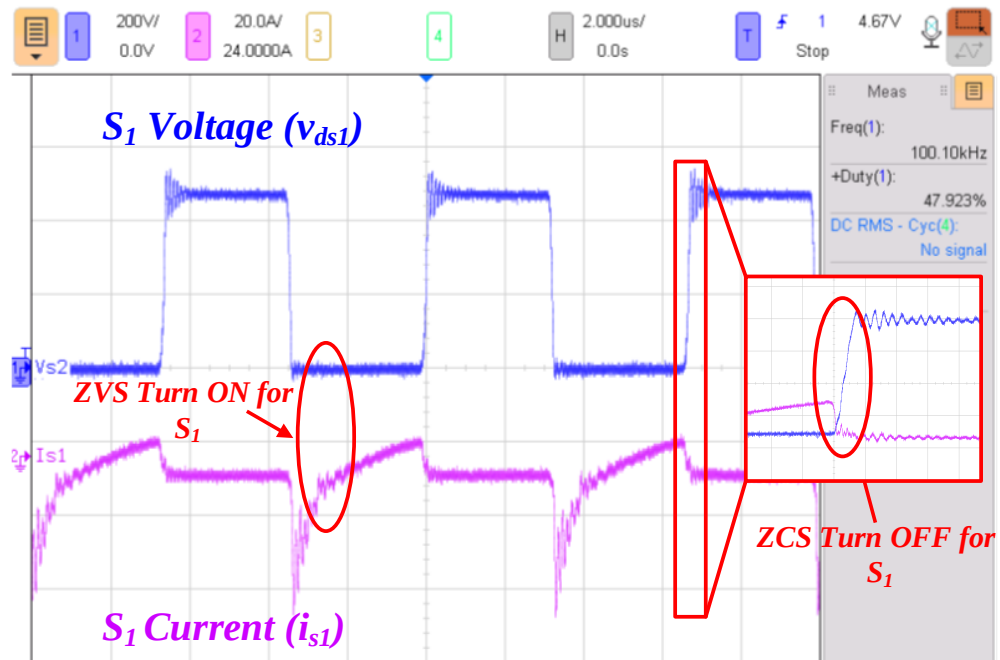


Figure 2.20: Voltage over and current flowing through S_1 at switching frequency.

in Fig. 3.20. Moreover, the soft-switching operation of the switch S_1 in both positive and negative line cycles are shown in Fig. 3.20. To further verify the soft-switching operation of switch S_1 , voltage and current waveforms of switch S_1 at switching frequency are illustrated in Fig. 3.21. Since the resonant current is lagging behind the resonant voltage due to the presence of CLLC resonant converter, switch S_1 current first flows through its antiparallel diode. This is why as shown in Fig. 3.21, S_1 current is negative at the moment that it turns ON, resulting in ZVS Turn ON for Switch S_1 . Moreover, due to the presence of snubber capacitors, voltage across S_1 slowly rises from zero proving ZCS turn OFF for this switch as shown in Fig. 3.21.

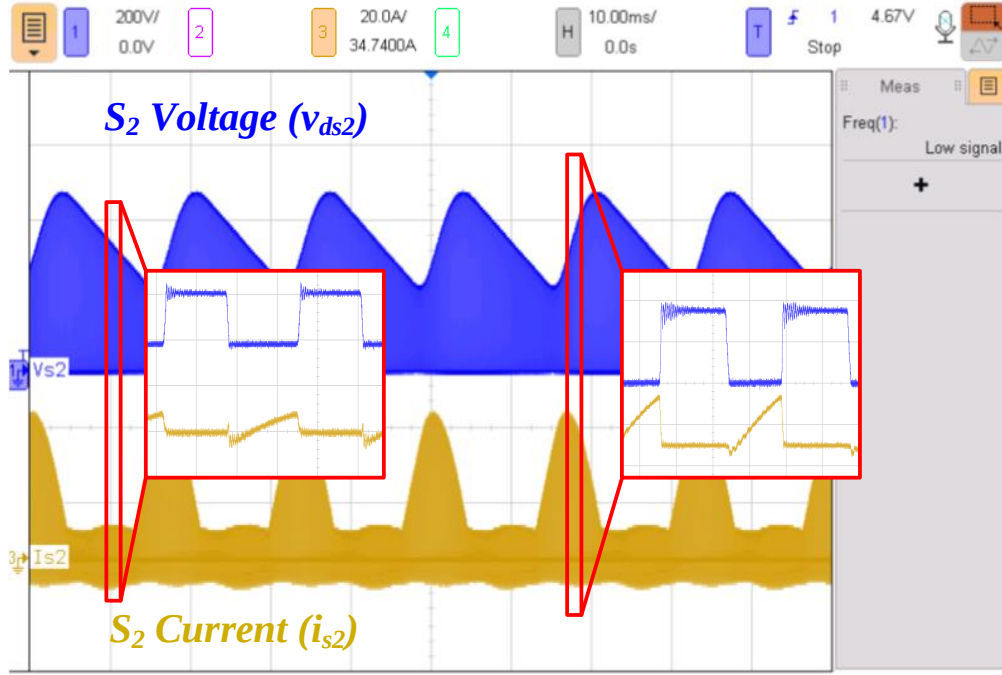


Figure 2.21: Voltage over and current flowing through S_2 at line frequency.

Similarly, the voltage and current waveforms of switch S_2 at line frequency are shown in Fig. 2.21. Moreover, the soft-switching operation of the switch S_2 in both positive and negative line cycles are shown in Fig. 2.21. To further verify the soft-switching operation of switch S_2 , voltage and current waveforms of S_2 at switching frequency are illustrated in Fig. 2.22. Similar to the switch S_1 , switch S_2 current first flows through its antiparallel diode resulting in

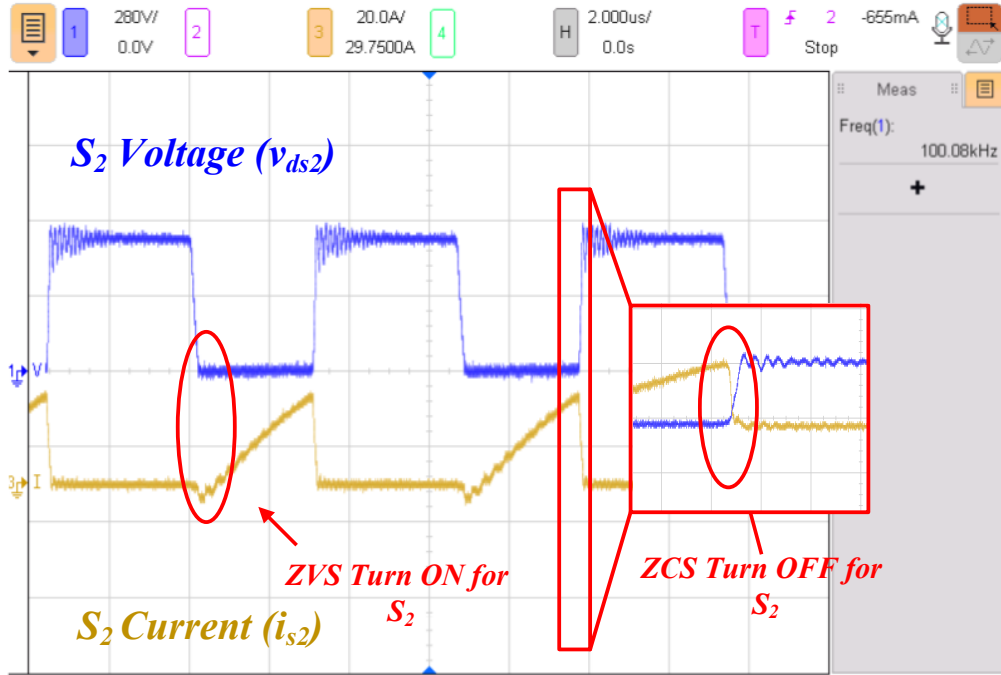


Figure 2.22: Voltage over and current flowing through S_2 at switching frequency.

ZVS Turn ON for Switch S_2 as illustrated in Fig. 2.22. Moreover, due to the presence of snubber capacitors, voltage across S_2 slowly rises from zero proving ZCS turn OFF for this switch as shown in Fig. 2.22.

Similar to the switches S_1 and S_2 , to show the soft-switching operation of the switch S_6 , its voltage and current waveforms at line frequency are shown in Fig. 2.23. Moreover, the soft-switching operation of the switch S_6 in both positive and negative line cycles are shown in Fig. 2.23. To further verify the soft-switching operation of switch S_6 , voltage and current waveforms of S_6 at switching frequency are illustrated in Fig. 2.24. Similar to the switches S_1 and S_2 , switch S_6 current first flows through its antiparallel diode resulting in ZVS Turn ON as illustrated in Fig. 2.24. Moreover, due to the presence of snubber capacitors, voltage across S_6 slowly rises from zero proving ZCS turn OFF for this switch as shown in Fig. 2.24.

Table 2.2: Comparison with the State-of-the-Art EV OBCs

Paper	Number of Semiconductors		Switching Frequency	DC-link Capacitors	Filter Capacitors	Peak Efficiency	Output Voltage
	Switches	Diodes					
Abbasi <i>et al.</i> [31]	8	8	100kHz	$2 \times 220\mu F$	$2 \times 10\mu F$	97.9%	800V
Nguyen <i>et al.</i> [55]	9	4	75kHz	$2 \times 50\mu F$	$1 \times 50\mu F$	96.1%	430V
Kwon <i>et al.</i> [90]	8	-	100kHz	$2 \times 100\mu F$	$1 \times 100\mu F$	95.7%	410V
Xue <i>et al.</i> [91]	10	-	50kHz	$1 \times 70\mu F$	$1 \times 70\mu F$	91%	366V
Zhang <i>et al.</i> [41]	6	-	100kHz	$1 \times 200\mu F$	$1 \times 50\mu F$	95.2%	200V
Designed Converter	6	4	100-120kHz	$2 \times 25\mu F$	$2 \times 25\mu F$	95.3%	800V

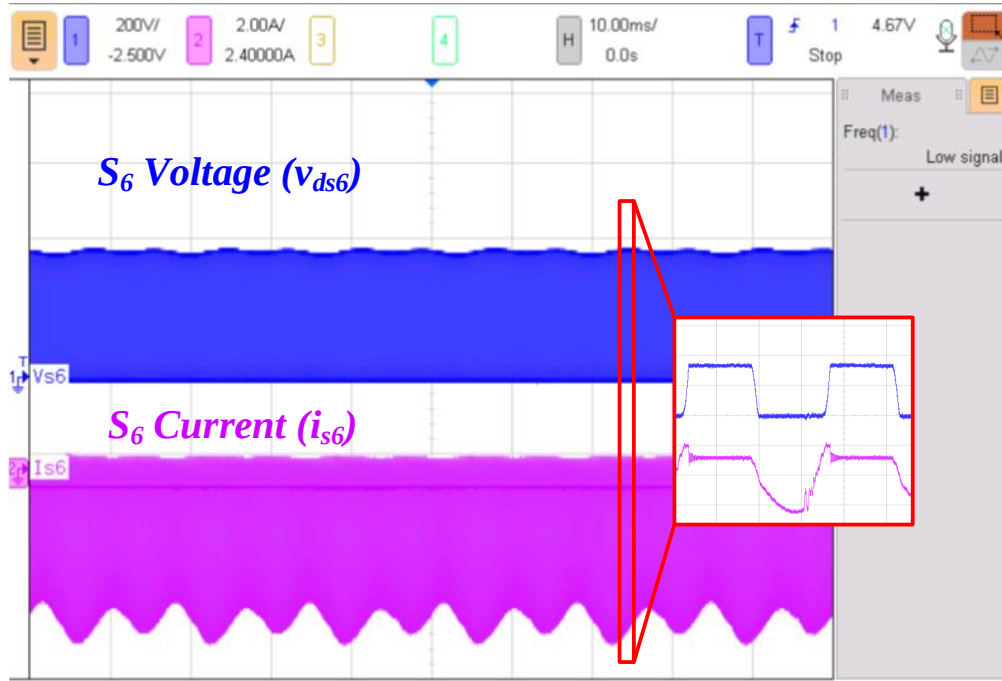


Figure 2.23: Voltage over and current flowing through S_6 at line frequency.

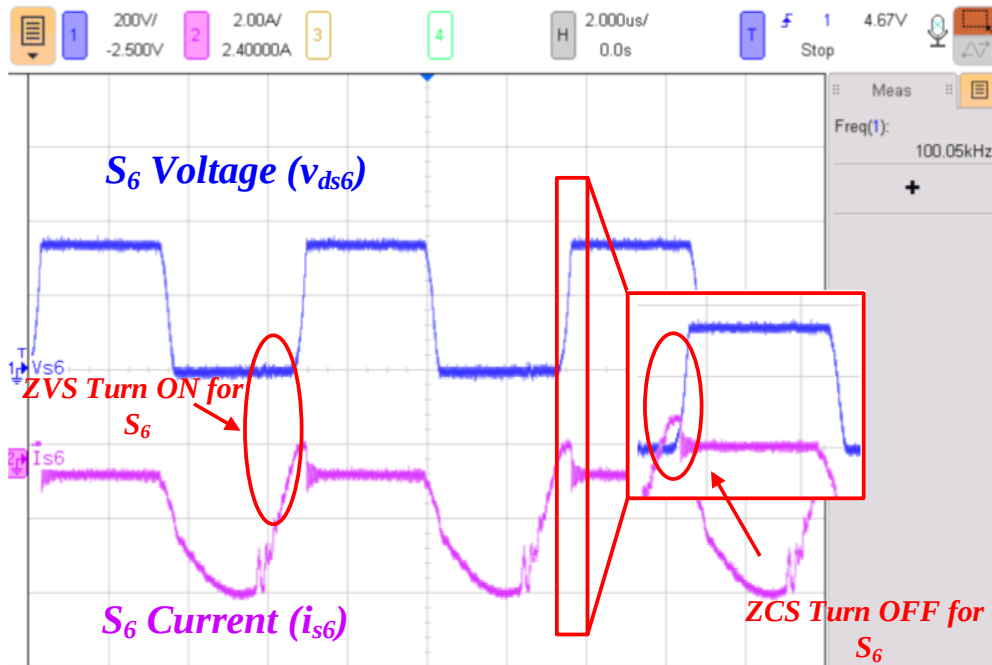


Figure 2.24: Voltage over and current flowing through S_6 at switching frequency.

2.5.3 Dynamic Response Experimental Results

To further validate the performance of the developed closed-loop control systems, several dynamic responses are captured in case of reference tracking, input voltage variation and transition between open loop and closed loop control system. The dynamic responses of the designed converter are shown in Figs. 2.25–2.27.

To validate the performance of the developed VFM-based controller regarding reference voltage tracking, reference voltage of the converter is changed from the nominal $800V_{dc}$ to $750V_{dc}$ during the normal operation of the converter. Fig. 2.25 illustrates the dynamic performance of the converter to this reference variation. Input voltage (v_{in}), input current (i_{in}), DC-link voltage ($V_{DC-link}$), and output voltage (V_o) of the converter are shown in Fig. 2.25. It can be seen in Fig. 2.25 that the closed-loop control system was able to track the new reference voltage with zero steady-state error and fast transient response.

To further validate that developed control system is able to regulate the output voltage of the designed converter (V_o) for different input voltages (v_{in}), the input voltage of the converter is changed from $120V_{rms}$ to $135V_{rms}$ and the dynamic response the converter is illustrated in Fig. 2.26. As can be seen in Fig. 2.25, the closed-loop control system was able to maintain the $800V_{dc}$ output of the system despite the change in the input voltage of the converter with zero steady-state error and fast transient response.

Finally, to show the effectiveness of the designed closed-loop controllers in terms of ripple reduction, the ripple reduction and VFM-based controller are turn off and the converter is operated with open-loop controller with a fixed switching frequency. Then, using a C block in PLECS RT Box1, both feedback loops are manually activated to see the effect of the closed-loop controllers in terms of reducing the output voltage ripple and regulating the voltage at $800V_{dc}$. The dynamic response of the converter is presented in Fig. 2.27. As can be seen in Fig. 2.27, the closed-loop control system successfully reduced the voltage ripple and regulated the output voltage to $800V_{dc}$ with zero steady-

state error and fast transient response.

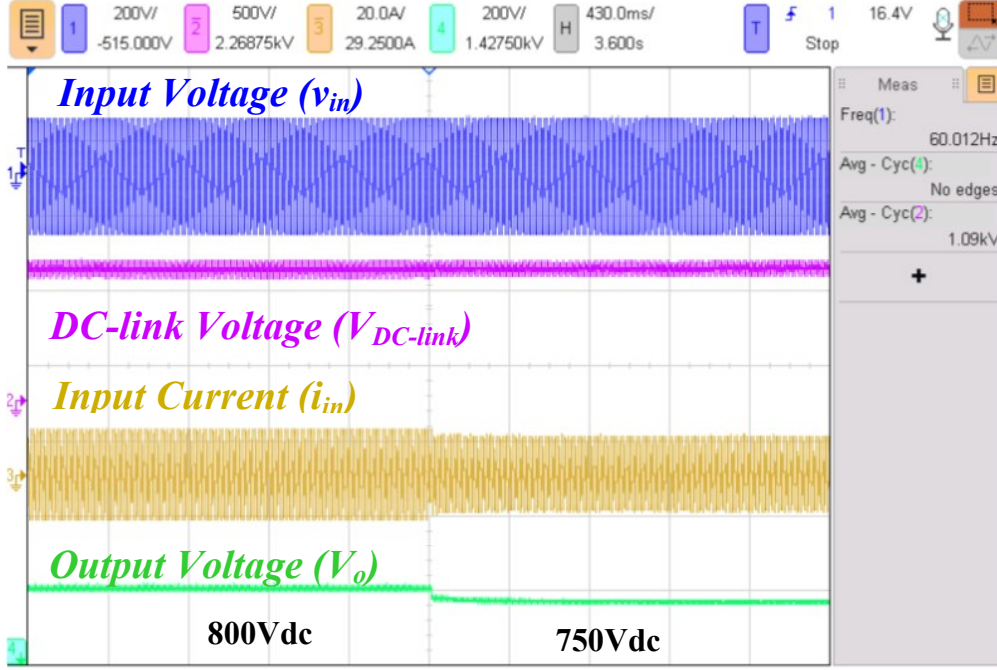


Figure 2.25: Dynamic performance of the system against output voltage reference change.

2.5.4 Comparison

To show the superiority of the designed topology and the designed closed-loop controller, the converter was compared with several other state-of-the-art EV OBC topologies with reduced storage units. The result of this comparison is summarized in Table 3.2. With similar switching frequency range and comparable efficiency, the designed converter was able to reduce the voltage ripple while utilizing the lowest storage capacitances with reduced number of semi-conductor devices. Moreover, it is worth mentioning that the designed converter distinguishes itself from existing designs in the literature through a stacked switch configuration, reducing semi-conductor voltage stress to half, thereby enabling the use of lower-rated, more cost-effective semiconductors. This design not only cuts down initial and replacement costs but also makes the components more accessible. Additionally, it incorporates lower-value DC-

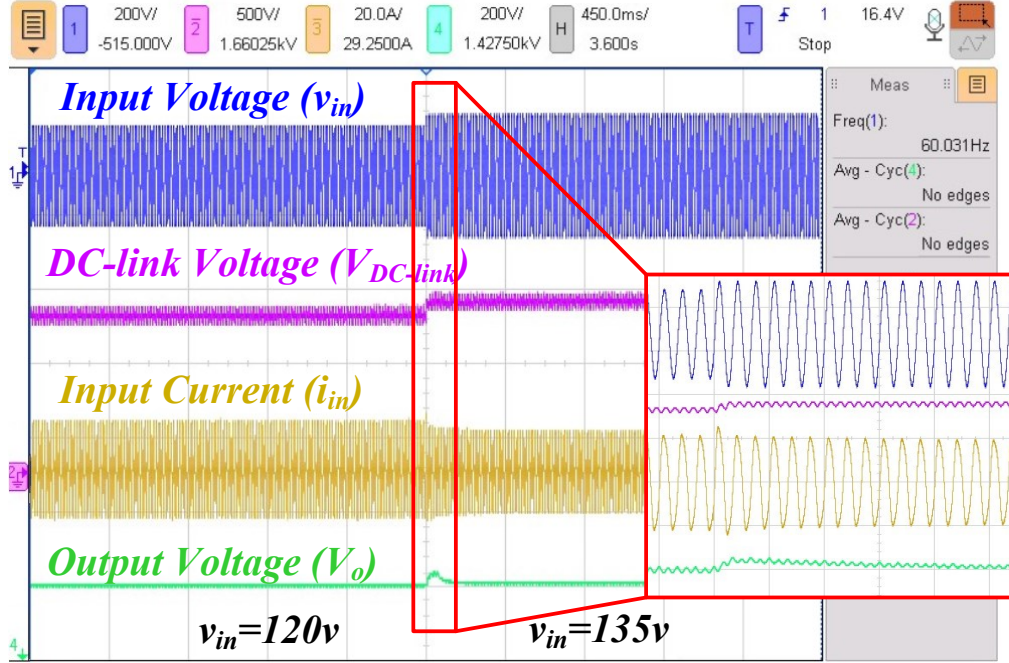


Figure 2.26: Dynamic performance of the system against input voltage variation.

link and filter capacitors, effectively reducing the overall material costs without sacrificing performance. The converter also requires fewer semi-conductor devices compared with most of the designs in the literature, simplifying the design, reducing hardware costs, and enhancing system reliability due to fewer potential failure points. Collectively, these strategic component selections position the converter as a cost-effective solution for high-voltage EV systems, despite the challenges in direct cost comparison due to variability in voltage levels.

Fig. 3.35 illustrates the measured efficiency for a range of an input voltages. It can be observed that the maximum efficiency of 95.3% was achieved at $v_{in} = 120V_{rms}$. Moreover, Fig. 3.36 shows the measured power factor of the converter for a range of an input voltages. It can be observed that using the closed-loop duty ratio controller, the quality of the input current remains high for different input voltages. Moreover, the detailed harmonics ranging from the first to the nineteenth harmonics captured from the hardware prototype using “Power

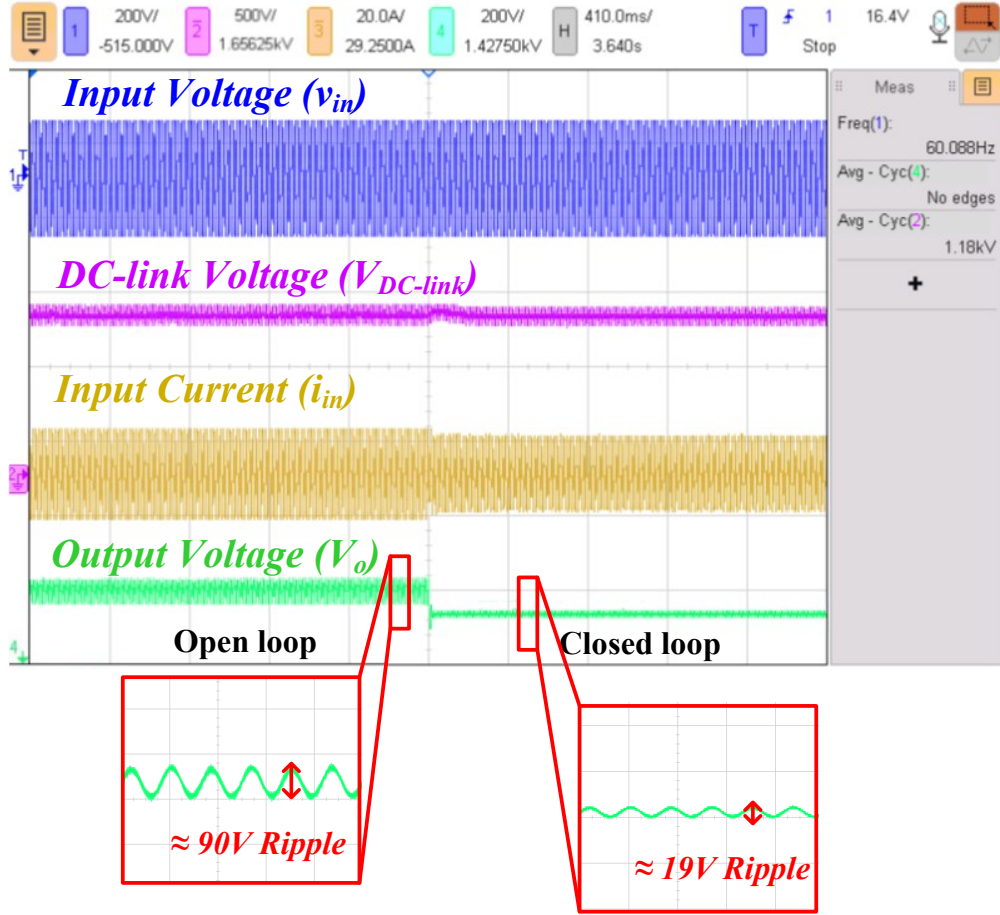


Figure 2.27: Dynamic performance of the system without and with the closed-loop control systems.

Analysis Tool” from the KEYSIGHT MSOX6004A oscilloscope are presented in Fig. 2.30 through Fig. 2.32. The Total Harmonic Distortion (THD) value of 2.23% has been captured and the captured harmonic values are compared with IEC 6000-3-2 [92], which shows maximum allowable harmonics for class A battery chargers (with input current $\leq 16A$). The results validate that the developed input current controller successfully conforms to these stringent standards, despite the minimized DC-link capacitance value.

Furthermore, the designed converter with dimensions of $30 \times 139 \times 5.2cm^3$, achieves a volumetric power density of approximately $0.532W/cm^3$. When considering its weight of $2.32kg$, the gravimetric power density is around $474.14W/kg$. This performance places our converter within the range observed

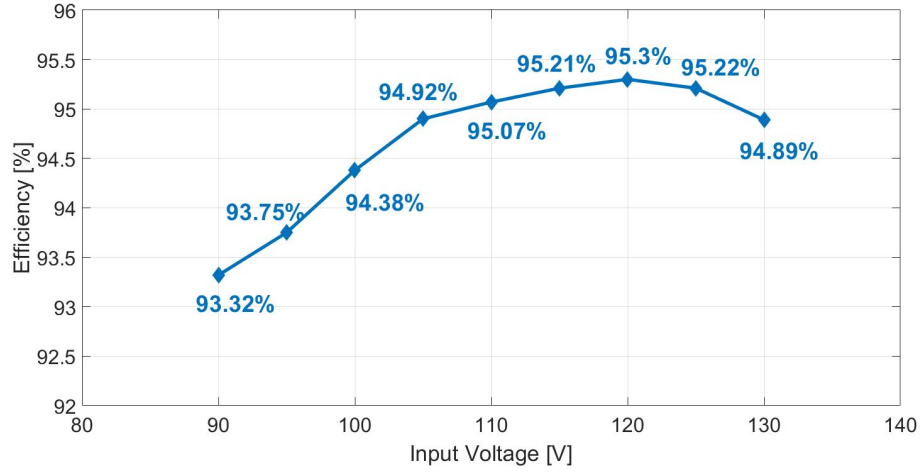


Figure 2.28: Efficiency Curve of the designed converter for different input voltages.

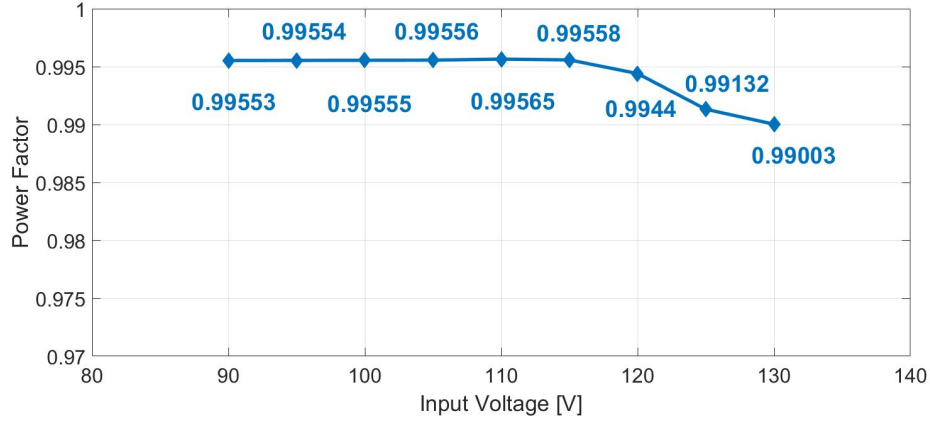


Figure 2.29: Power Factor Curve of the designed converter for different input voltages.

in existing literature, where reported power densities vary from $0.333W/cm^3$ [55] to $0.8W/cm^3$ [31] for similar devices.

2.6 Chapter Summary

This chapter presented the design, control, and validation of a novel unidirectional bridgeless AC/DC converter tailored for EV on-board charging applications. The designed topology eliminates the conventional input diode bridge, thereby reducing conduction losses and improving overall efficiency. By employing a stacked-switch configuration, the voltage stress across each active



Figure 2.30: Harmonic distortion captured from the hardware experimental prototype showing first to seventh harmonics.

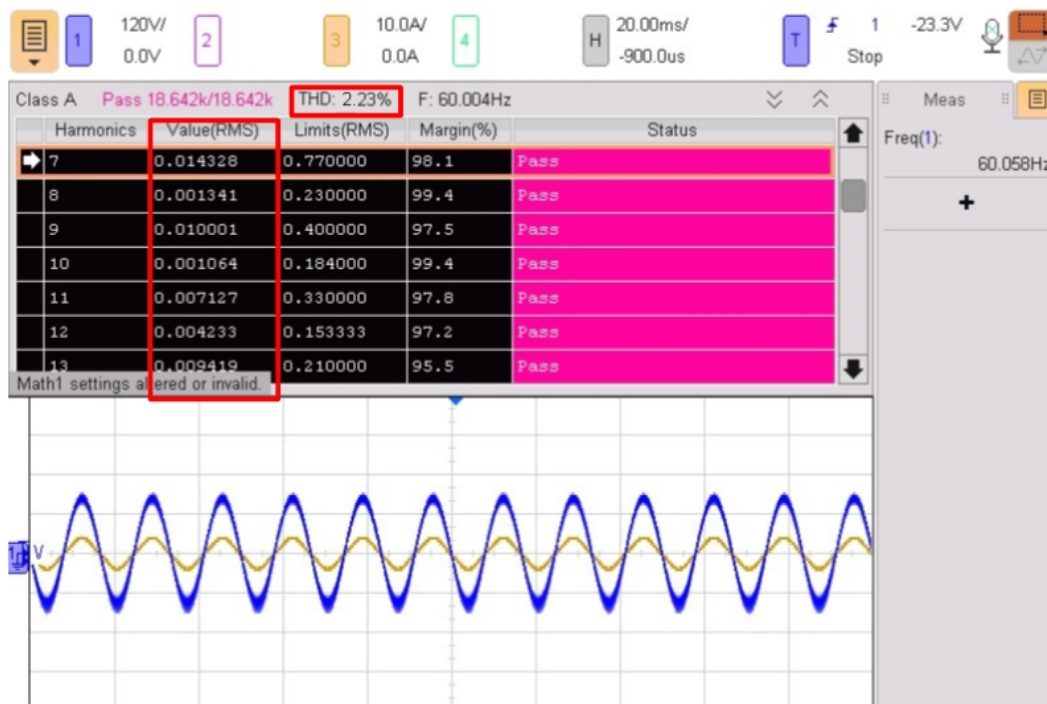


Figure 2.31: Harmonic distortion captured from the hardware experimental prototype showing seventh to thirteenth harmonics.



Figure 2.32: Harmonic distortion captured from the hardware experimental prototype showing thirteenth to nineteenth harmonics.

switch is reduced to half of the output voltage, making the design suitable for high-voltage battery systems.

To meet stringent grid standards while minimizing storage capacitance, the converter is designed to operate in DCM, allowing natural shaping of the input current for high power factor and low THD. A closed-loop control architecture was developed to regulate the output voltage using VFM, and a secondary-side duty ratio control was introduced to actively suppress the low-frequency voltage ripple. This coordinated control strategy enables the use of compact, high-reliability film capacitors instead of bulky electrolytic types.

The performance of the designed converter and control system was verified through simulation and experimental testing on a 1.1 kW, 120 V_{rms} to 800 V_{dc} prototype. The results confirmed high efficiency, unity power factor, effective ripple suppression, and fully soft-switched operation across the entire line cycle. The success of this design provides a promising solution for compact, efficient, and reliable unidirectional EV chargers, addressing key industry challenges related to size, reliability, and grid compliance.

Chapter 3

Bidirectional Half-Bridge/Dual Stacked-Switches Structured Electrolytic Capacitor-Less AC/DC Power Converter

3.1 Introduction

This chapter introduces the development of a novel bidirectional single-phase AC/DC converter designed to support both charging (G2V) and discharging (V2G) operations in EV systems. The designed topology addresses the major limitations of conventional bidirectional converters, such as high voltage stress, lack of soft-switching, bulky passive components, and limited ripple mitigation capability.

In the first part of this chapter, a dual stacked-switch half-bridge PFC structure is presented for the AC-side stage, enabling reduced voltage stress across the switches. The DC-side employs a bidirectional CLLC resonant stage to provide galvanic isolation and ensure soft-switching during both AC/DC and DC/AC operation modes. The overall architecture is optimized for HV EV battery systems and bidirectional power flow with minimal component count.

The second part of this chapter focuses on the control system design. A dq-frame-based closed-loop PFC controller is implemented to ensure sinusoidal input current, unity power factor, and grid synchronization. Additionally,

a ripple reduction controller is introduced by dynamically modulating the secondary-side duty ratio, significantly reducing the low-frequency output voltage ripple without requiring large electrolytic capacitors.

In the final section, the designed converter and control strategy are validated through simulation and experimental testing on a 1 kW laboratory prototype. The results highlight the converter's ability to operate efficiently and reliably in both directions of power flow, maintaining high performance under various grid conditions and load scenarios.

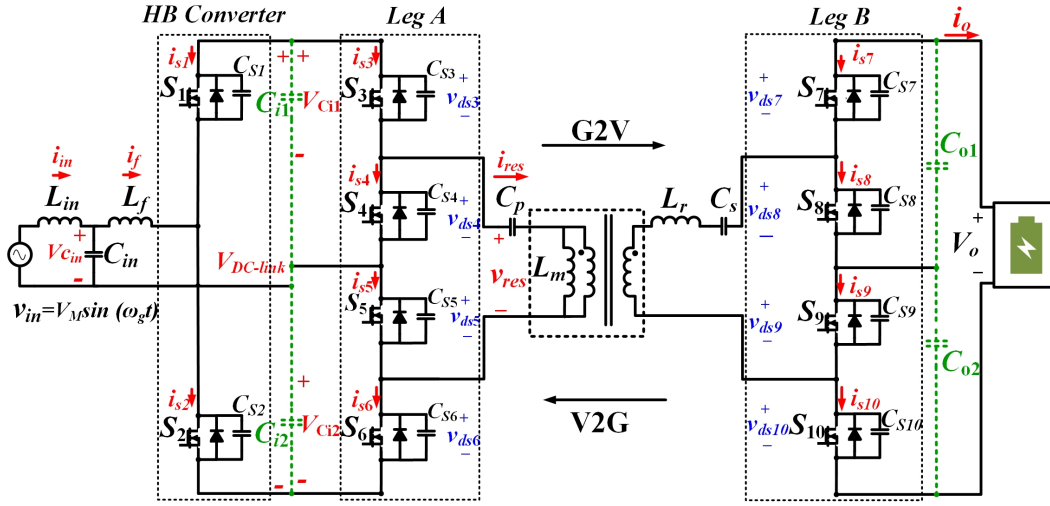


Figure 3.1: Half-bridge/dual-stacked switched-structured bridgeless bidirectional AC/DC converter.

3.2 Description and Operation of the Converter

Fig. 3.1 illustrates the designed bidirectional AC/DC converter topology developed as an OBC for HV EV systems. The designed converter consists of a HB converter as a PFC circuit and dual-stacked-switches configurations in leg A and B that are connected using a CLLC resonant circuit. In the HB PFC converter, switches S_1 and S_2 operate with D_I and $1 - D_I$ duty ratios, respectively. In leg A (leg B) of the designed converter, two middle switches S_4 and S_5 (S_8 and S_9) operate together with the same duty ratio D_p (D_s), while switches S_3 and S_6 (S_7 and S_{10}) operate with a duty ratio of $1 - D_p$ ($1 - D_s$) with a similar switching frequency f_{sw} .

In AC to DC mode (DC to AC mode), switches S_7 and S_{10} (S_3 and S_6) are turned off, and only switches S_8 and S_9 (S_4 and S_5) operate to minimize the voltage ripple following the command from the ripple reduction control system. Due to the stacked switches configuration in both Leg A and Leg B, the voltage stress across each switch is effectively divided, enhancing the converter's suitability for HV EV applications. In Leg A, the voltage stress across each switch is half of the DC-link voltage, as the stacked configuration allows the voltage to be shared evenly between the switches in the leg. This significantly reduces the voltage rating requirements for the individual switches while maintaining overall system performance. Similarly, in Leg B, the voltage stress across each switch is half of the output voltage. This configuration not only reduces the stress on individual switches but also ensures reliable operation under high-voltage output conditions. By reducing the voltage stress, the design enables the use of lower-voltage-rated switches, which are typically more efficient and cost-effective. This not only improves the converter's overall reliability and efficiency but also makes it particularly well-suited for high-voltage onboard charging applications, where managing voltage stress is critical to performance and longevity.

Furthermore, the CLLC resonant circuit module consists of a resonant inductor L_r , an isolated High-Frequency (HF) transformer with magnetizing inductance L_m , and two resonant capacitors C_p and C_s . It is worth mentioning that while leg A's (leg B's) functionality in AC to DC mode (DC to AC mode) aligns with recognized practices, leg B's (leg A's) operation marks a deviation from traditional methods that generally leverage only leg A (leg B) for their operation. Therefore, a comprehensive analysis of both legs and their synchronized operation, along with the achievement of soft-switching across all semiconductor devices, becomes of paramount importance in the designed converter.

Key operating waveforms of the designed bidirectional AC/DC converter are illustrated in Fig. 3.2. Since the converter operates similarly in both AC to DC and DC to AC modes and symmetrically during both positive and negative half-cycles, only the positive half-cycle of the converter during its AC

to DC mode is addressed in this analysis. Moreover, the switching frequency of leg A and leg B of the converter is considered identical, denoted as f_{sw} , and the switching frequency of the HB PFC converter is denoted by f_{hb} . Also, during AC to DC (DC to AC) mode, duty ratio of leg A (B) is assumed to be fixed at $D_p = 0.5$ ($D_s = 0.5$). Moreover, in the analysis of the designed converter, it is assumed that the primary and secondary resonant currents are equal, and the magnetizing current is neglected. This assumption is made to simplify the analysis and focus on the operation of the resonant tank. While the contribution of the magnetizing current to the overall behavior of the converter is acknowledged, it is considered negligible for the purposes of this study. The details of the operation of legs A and B are given below:

Interval $t_0 < t < t_1$

During this interval, gate signals are applied to switches S_3 and S_6 in leg A. Due to the above resonance operation of the CLLC resonant circuit, the resonant current i_{res} causes the antiparallel diodes of S_3 and S_6 to conduct. The voltage stress across switches S_4 and S_5 is half of the DC-link voltage, $V_{DC-link}/2$. Additionally, the lagging resonant current i_{res} forces the antiparallel diodes of switches S_8 and S_9 in leg B to conduct.

Interval: $t_1 < t < t_2$

During this interval, gate signals remain applied to switches S_3 and S_6 in leg A. At this point, switches S_3 and S_6 switch polarity and turn ON with Zero Voltage Switching (ZVS). Additionally, gate signals are applied to switches S_8 and S_9 in leg B following the command from ripple reduction control unit. As the lagging resonant current becomes positive, switches S_8 and S_9 turn ON under ZVS to minimize ripple by adjusting the converter's gain through a variable duty ratio D_s .

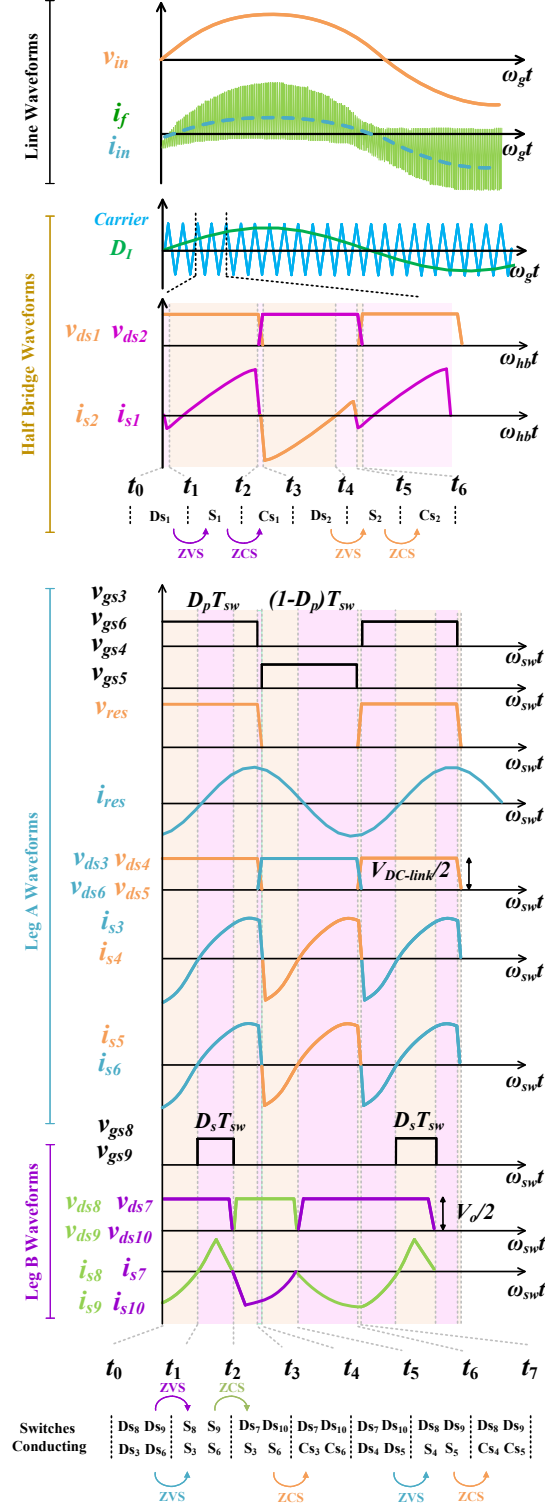


Figure 3.2: Key operating waveforms of the designed bidirectional AC/DC converter.

Interval: $t_2 < t < t_3$

During this interval, switches S_3 and S_6 in leg A continue to conduct. At $t = t_2$, following the command from the ripple reduction control unit with duty ratio D_s , switches S_8 and S_9 turn OFF with near Zero Current Switching (ZCS) due to the presence of snubber capacitors C_{S_8} and C_{S_9} . Moreover, the resonant current flows through the antiparallel diodes of S_7 and S_{10} and charges the output capacitors C_{o_1} and C_{o_2} .

Interval: $t_3 < t < t_4$

The gate signals for switches S_3 and S_6 are removed. Simultaneously, the snubber capacitors C_{S_3} and C_{S_6} begin to charge. As a result, the voltages across switches S_3 and S_6 increase gradually, leading to a near ZCS turn OFF. It is also important to mention that the resonant current (i_{res}) flows entirely through the conducting switch (S_3 or S_4), while the current through the non-conducting switch is zero. This complementary operation ensures compliance with Kirchhoff's Current Law (KCL), as the resonant current always equals the current in the active switch.

Interval: $t_4 < t < t_5$

During this interval, gate signals are applied to switches S_4 and S_5 . Simultaneously, the resonant current i_{res} forces the antiparallel diodes of S_4 and S_5 to conduct. During this period, the voltage stress across switches S_3 and S_6 is half of the DC-link voltage $V_{DC-link}/2$.

Interval: $t_5 < t < t_6$

At $t = t_5$, gate signals remain applied to switches S_4 and S_5 . The current flowing through the antiparallel diodes of S_4 and S_5 drops to zero at $t = t_5$, resulting in ZVS turn ON.

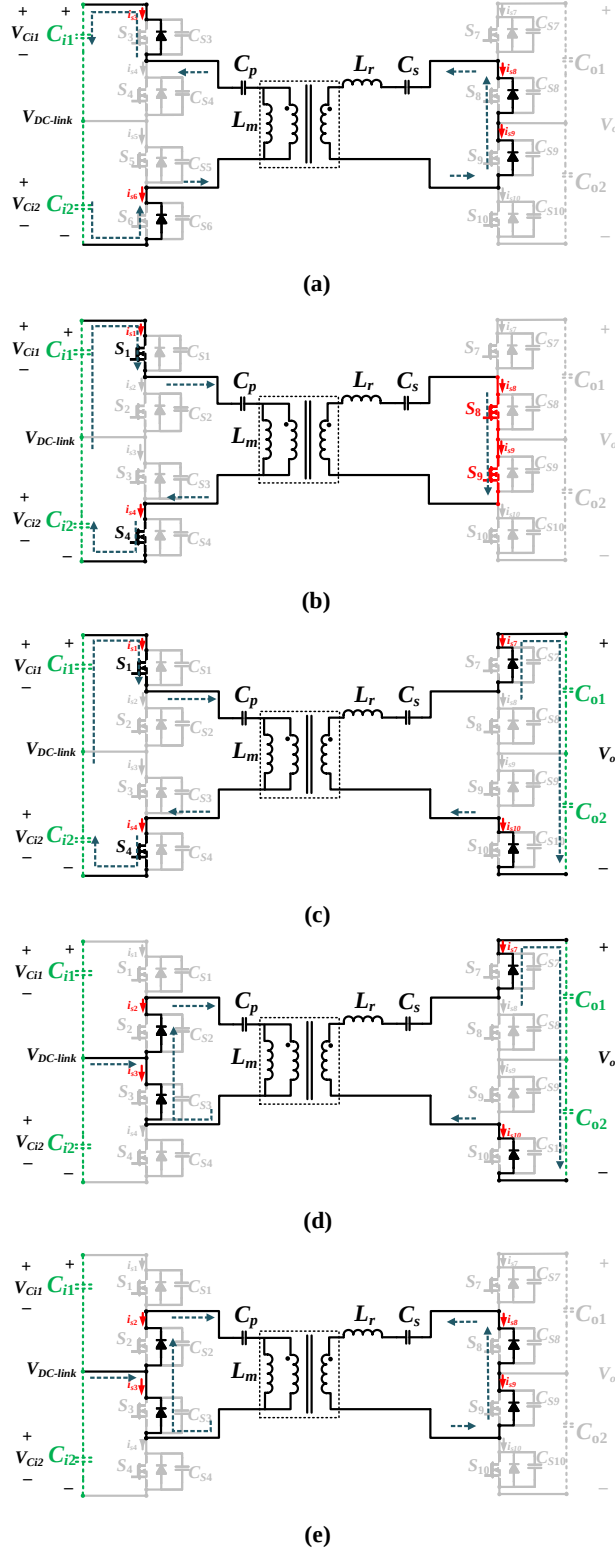


Figure 3.3: Operational stages of the designed bridgeless bidirectional AC/DC converter within a switching period in the positive half cycle.

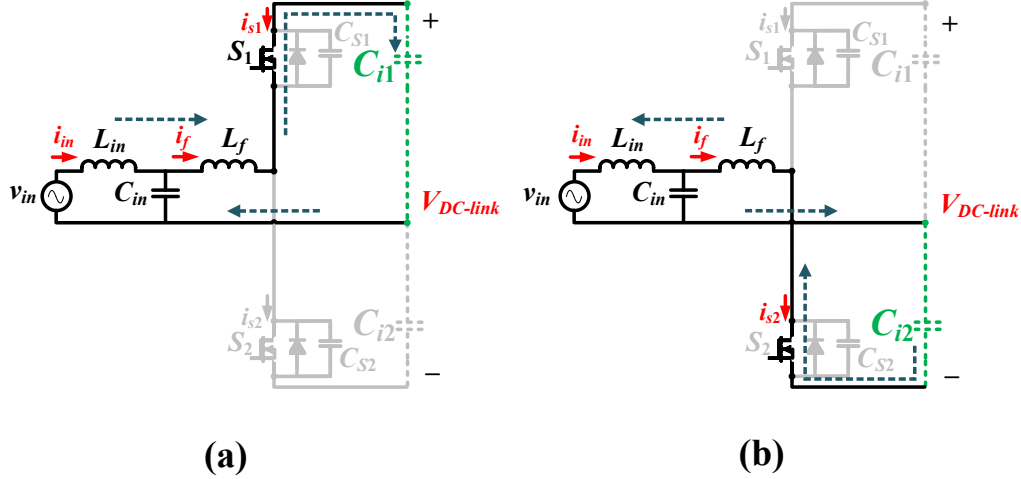


Figure 3.4: Operational stages of the employed bidirectional HB PFC converter.

Interval: $t_6 < t < t_7$

At $t = t_6$, the gate signals of the switches S_4 and S_5 are removed and the snubber capacitors C_{S4} and C_{S5} start to charge. As the result, the voltages across the switches S_4 and S_5 start to rise slowly, which allows a near ZCS turn OFF for S_2 and S_3 .

3.3 Converter Analysis

3.3.1 Half-Bridge PFC Converter

The HB converter in the designed bidirectional AC/DC converter serves as an active PFC circuit. The diagram presented in Fig 3.5. provides an overview of its components and connections. Switches S_1 and S_2 in the HB converter operate with duty cycles D_I and $D_I - 1$. Their switching ensures the PFC operation by shaping the input current to follow the input voltage waveform, using the implemented PLL and the designed controller, achieving a high power factor. The input voltage (v_{in}) and input current (i_{in}) of the designed converter can be given as below, where ω_g is the grid angular frequency.

$$v_{in} = V_M \sin(\omega_g t) \quad (3.1)$$

$$i_{in} \cong \frac{v_{in}}{R_e} \quad (3.2)$$

The input current (i_{in}) is controlled to follow the input voltage waveform for achieving PFC. In (3.2), R_e is the emulated resistance which is given below:

$$R_e = \frac{v_{in,rms}^2}{P_{av}} \quad (3.3)$$

The dq modelling of single-phase grid-connected HB PFC Converter with LCL filter

To design the controller for the HB PFC converter connected to the grid via LCL filter (see Fig. 3.5) and for simplifying control and analysis, transformation of the single phase LCL filter equations into the dq (direct-quadrature) reference frame is needed (see Fig. 3.6). This transformation is typically used for three-phase systems, but for a single-phase system, a virtual second phase that is 90 degrees out of phase with the actual phase is required to apply the transformation. The general approach for this transformation is as below:

1. Select a rotating frame of reference: This frame of reference rotates at the grid's angular frequency (ω_g), which is 2π times the grid frequency (in Hz).
2. Define the grid voltage and current: The grid voltage (v_{in}) is typically the reference and is represented as a purely d -axis quantity because the q -axis component would be zero for a single-phase grid. The grid current (i_{in}), however, would have both d -axis and q -axis components depending on its phase angle relative to v_{in} .

In the dq frame synchronized with the grid voltage shown in (3.1), v_{in} would be represented as:

$$\begin{aligned} v_{in,d} &= V_M \\ v_{in,q} &= 0 \end{aligned} \quad (3.4)$$

For the grid current, assuming a phase shift of ϕ with the grid voltage, if we have:

$$i_{in} = I_{in,M} \sin(\omega_g t + \phi) \quad (3.5)$$

Its d - q components would be:

$$\begin{aligned} i_{in,d} &= I_{in,M} \cos(\phi) \\ i_{in,q} &= I_{in,M} \sin(\phi) \end{aligned} \quad (3.6)$$

3. Apply the dq transformation to the filter equations: Now, the dq transformation is applied to the original differential equations.

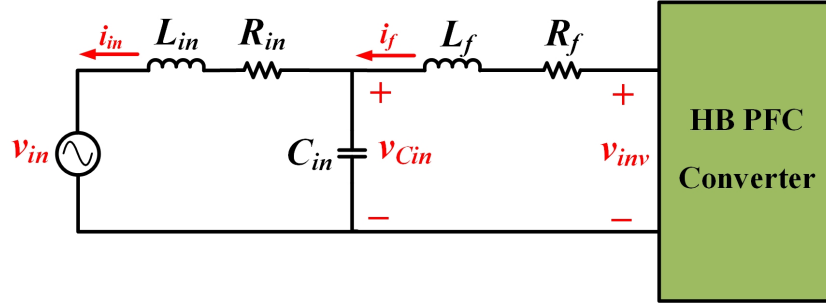


Figure 3.5: LCL filter connected to the bidirectional HB PFC converter.

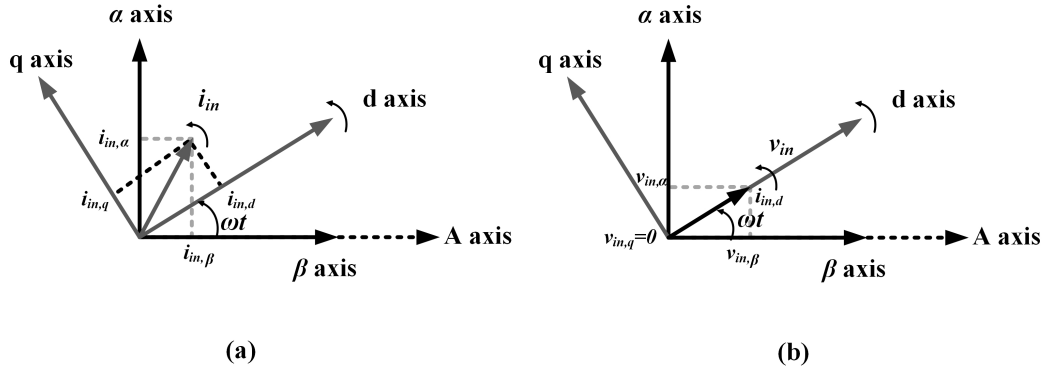


Figure 3.6: Visualization of dq and $\alpha\beta$ reference frame with corresponding vectors.

The differential equations of the LCL filter in the dq reference frame be-

come:

$$\begin{aligned}
L_f \left(\frac{di_{f,d}}{dt} - \omega_g i_{f,q} \right) + R_f i_{f,d} &= v_{inv,d} - v_{Cin,d} \\
L_f \left(\frac{di_{f,q}}{dt} + \omega_g i_{f,d} \right) + R_f i_{f,q} &= v_{inv,q} - v_{Cin,q} \\
L_{in} \left(\frac{di_{in,d}}{dt} - \omega_g i_{in,q} \right) + R_{in} i_{in,d} &= v_{Cin,d} - v_{in,d} \\
L_{in} \left(\frac{di_{in,q}}{dt} + \omega_g i_{in,d} \right) + R_{in} i_{in,q} &= v_{Cin,q} \\
C_{in} \left(\frac{dv_{Cin,d}}{dt} - \omega_g v_{Cin,q} \right) &= i_{f,d} - i_{in,d} \\
C_{in} \left(\frac{dv_{Cin,q}}{dt} + \omega_g v_{Cin,d} \right) &= i_{f,q} - i_{in,q}
\end{aligned} \tag{3.7}$$

In these equations, $(v_{inv,d}, v_{inv,q})$, $(v_{Cin,d}, v_{Cin,q})$, $(i_{in,d}, i_{in,q})$, and $(i_{f,d}, i_{f,q})$ are the d and q components of the HB PFC converter voltage, LCL filter capacitor voltage, input current, and filter inductance current, respectively.

HB PFC Converter Soft-Switching Operation

To illustrate the soft-switching condition for the switches S_1 and S_2 in HB PFC converter, the concept described in [64] was followed. For analysis, the operation of the switch S_2 has been considered as its analysis can be applied to the switch S_1 as well. Considering an input power of 1kW, and S_2 turns ON at $t = t_0$, as shown in Fig. 3.6, three scenarios can be considered based on the value of the filter inductance (L_f).

1. ZVS turn ON: In Fig. 7(a), for $L_f < 190\mu H$, ZVS turn-ON is always achieved as the filter current i_f will become negative at the moment the switch S_2 turn ON at $t = t_0$.
2. ZCS turn ON: In Fig. 7(b), with the filter inductor $L_f = 190\mu H$, the PFC converter enters its boundary condition and i_f becomes zero at the moment the switch S_2 turn ON at $t = t_0$, resulting in S_2 turning ON with ZCS.
3. ZVS Failure: In Fig. 7(c), for $L_f > 190\mu H$, the PFC converter inductor current is always positive and therefore, i_f never reaches zero, resulting in hard-switching operation of S_2 . Utilizing any filter inductance (L_f) with values greater than $190\mu H$ will result in hard-switching operation of the switches S_1 and S_2 .

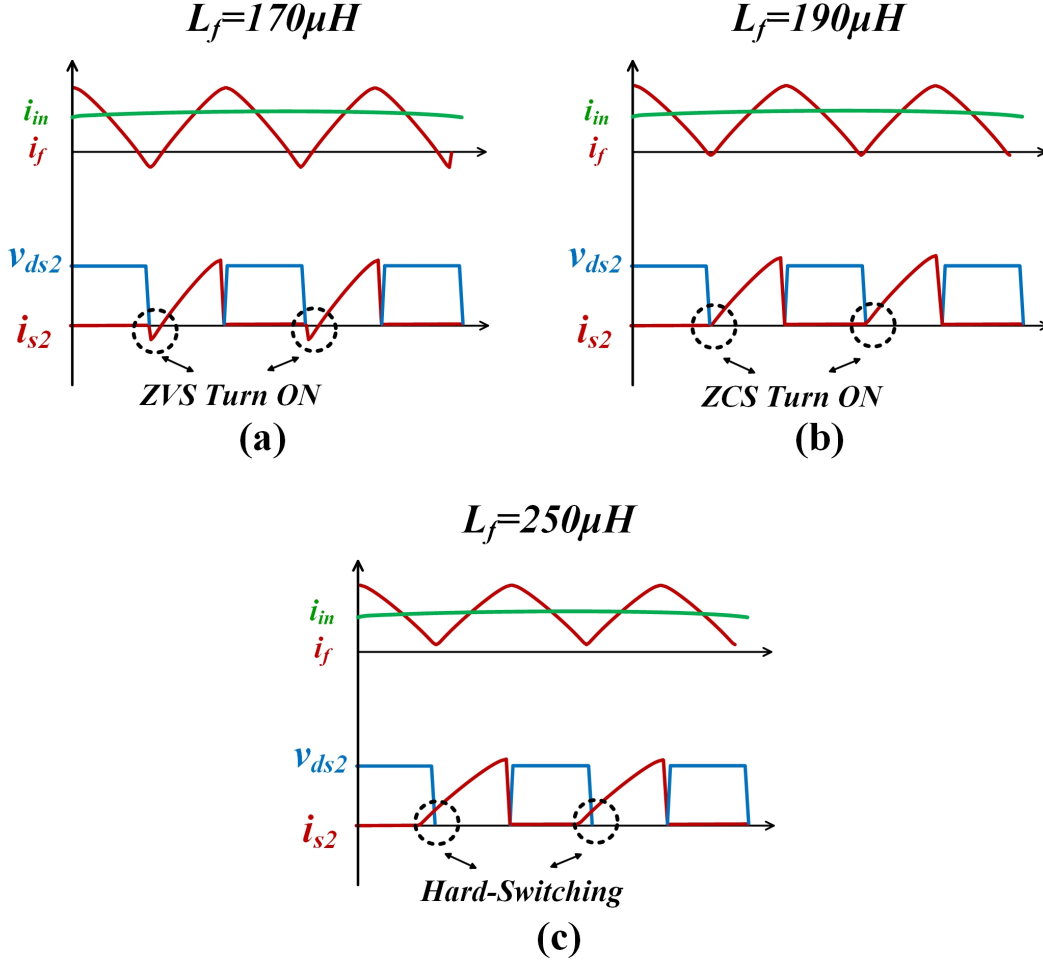


Figure 3.7: Soft-switching condition, (a) ZVS turn ON, (b) ZCS turn ON and, (c) hard-switching.

In summary, the ZVS condition of the switches in the HB PFC converter is influenced by the value of L_f . Using a very small filter inductors increases the ZVS range but also raises the circulating current. Therefore, L_f must be designed to balance switching and conduction losses.

3.3.2 Ripple Reduction Method

In the designed bidirectional AC/DC converter, the bulky and unreliable electrolytic-type DC-link and output filter capacitors are replaced with small and reliable film capacitors. As a result, higher voltage ripple is expected at the output of the converter, which can be harmful to the EV's battery. To mitigate this, as shown in Fig. 3.8, two switches (S_8 and S_9 in AC to DC

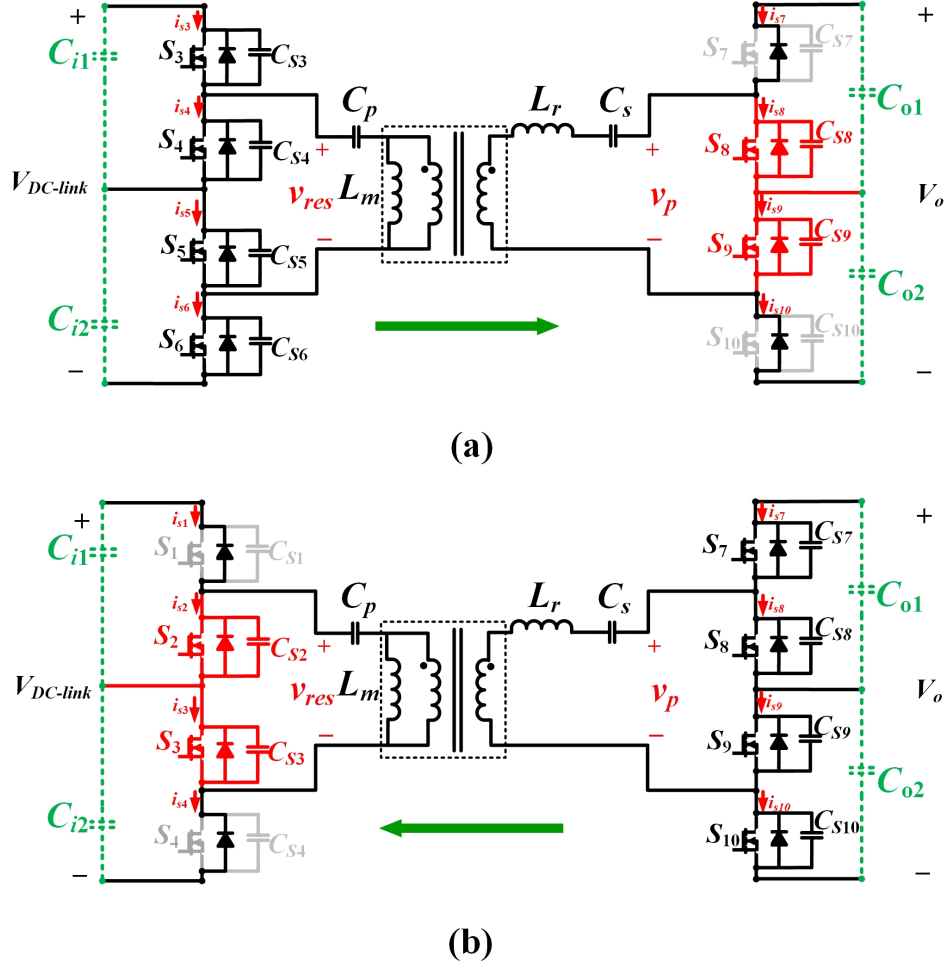


Figure 3.8: Active rectification for both modes of the designed bidirectional converter. (a) Converter's operation in AC to DC mode, (b) Converter's operation in DC to AC mode.

mode and S_4 and S_5 in DC to AC mode) in the rectifying stage of the DC/DC stage of the bidirectional converter are actively switched to cancel out the ripple by controlling the voltage gain of the converter. To show how controlling the duty ratio of these switches affect the voltage gain of the converter, steady-state analysis of the converter is necessary.

To analyze the steady-state performance of the designed topology, the following assumptions are made: (1) all components, including semiconductor switches and diodes, are considered ideal, (2) the delay between the gating signals of the switches is ignored, and (3) the effect of snubber capacitors is disregarded. The Fourier series representation of the input voltage to the res-

onant circuit, v_{res} , is given by (3.8). Due to the DC blocking function of C_p , only the AC components of v_{res} are applied to the resonant circuit, where $V_{DC-link}$ is the DC-link voltage.

$$v_{res} = V_{DC-link}D_p + \sum_{h=1}^{\infty} \left(\frac{\sqrt{2}V_{DC-link}}{h\pi} \sqrt{1 - \cos(2h\pi D_p)} \sin(2\pi h f_{sw}t + \theta_h) \right) \quad (3.8)$$

$$\theta_h = \tan^{-1} \left(\frac{\sin(2\pi h D_p)}{1 - \cos(2\pi h D_p)} \right) = \frac{\pi}{4} - \pi D_p \quad (3.9)$$

in (3.8) and (3.9), the harmonic order is denoted by h . Additionally, the relative angular frequency ω_r is defined by (3.10), where ω_{sw} , ω_0 , and Q represent the angular switching frequency, the angular resonant frequency, and the quality factor, respectively.

$$\omega_r = \frac{\omega_{sw}}{\omega_0} \quad (3.10)$$

$$\omega_0 = \frac{1}{\sqrt{L_m C_p}} \quad (3.11)$$

$$Q = \frac{R_{ac}}{L_m \omega_0} \quad (3.12)$$

The resonant current i_{res} can be calculated from v_{res} in (3.8) as below:

$$i_{res} = \sum_{h=1}^{\infty} \left(\frac{\sqrt{2}V_{DC-link}}{h\pi |Z_{i,h}|} \sqrt{1 - \cos(2h\pi D_p)} \sin(2\pi h f_{sw}t + \theta_h) \right) \quad (3.13)$$

where $Z_{i,h}$ can be calculated as below:

$$|Z_{i,h}| = R_{ac} \sqrt{\frac{(k + 1 + \frac{1}{m}(1 - \frac{1}{h^2\omega_r^2}) - k\omega_r^2)^2 + (hQ\omega_r(1 - \frac{1}{h\omega_r^2}))^2}{Q^4 + (hQ\omega_r(k + 1 - \frac{1}{mh\omega_r^2}))^2}} \quad (3.14)$$

$$\begin{aligned} \phi_{Z_{i,h}} &= \tan^{-1} \left(\frac{hQ\omega_r \left(1 - \frac{1}{h\omega_r^2}\right)}{k + 1 + \frac{1}{m} \left(1 - \frac{1}{h^2\omega_r^2}\right) - k\omega_r^2} \right) \\ &= -\tan^{-1} \left(\frac{h\omega_r \left(k + 1 - \frac{1}{mh\omega_r^2}\right)}{Q} \right) \end{aligned} \quad (3.15)$$

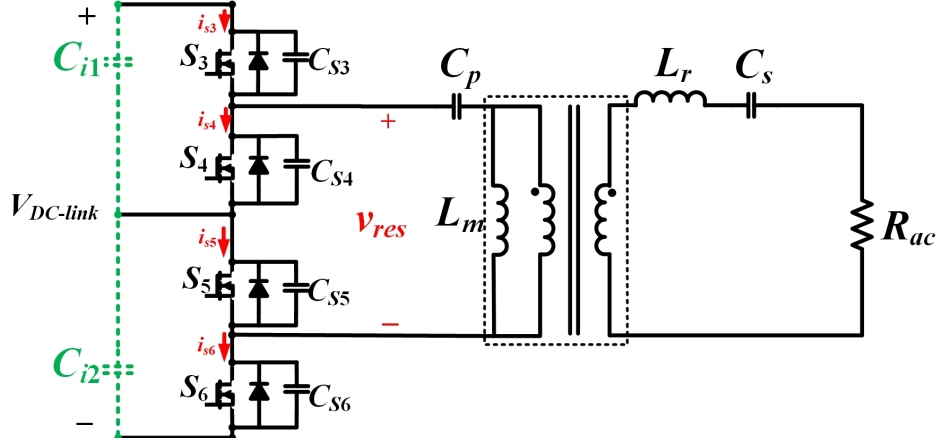


Figure 3.9: Equivalent circuit of the CLLC resonant circuit connected to leg A of the designed converter.

where $k = L_r/L_m$ is defined as the ratio between secondary-side and magnetizing inductance, and $m = C_s/C_p$ is defined as the ratio between secondary-side and primary-side capacitances. Moreover, R_{ac} is the equivalent resistance seen by the resonant circuit as shown in Fig. 3.8. Switching the two middle switches in the leg B (leg A) in AC to DC (DC to AC) mode, R_{ac} can be described as below:

$$R_{ac} = \frac{8}{\pi^2}(1 - D_s)^2 R_L \quad (3.16)$$

as a result, quality factor can be redefined as below:

$$Q = \frac{R_{ac}}{L_m \omega_0}(1 - D_s)^2 = Q(1 - D_s)^2 \quad (3.17)$$

The effect of the active rectification on the voltage gain of the DC/DC stage of the designed converter during both AC to DC and DC to AC operation of the bidirectional converter is discussed below.

Based on (3.8), the RMS value of the input voltage to the resonant circuit (v_{res}) can be calculated as (3.18).

$$\frac{v_{res}}{V_{DC-link}} = \frac{1}{\pi} \sqrt{\sum_{n=1}^{\infty} \frac{1 - \cos(2n\pi D_p)}{n^2}} \quad (3.18)$$

The duty ratio of the stacked switches in leg A will be fixed at $D_p = 0.5$. Therefore, for further simplification, the RMS value give in (3.18) can be

simplified as given in (3.19).

$$\frac{v_{res}}{V_{DC-link}} = \frac{\sqrt{2}}{\pi} \sqrt{\sum_{n=1,3,5,\dots}^{\infty} \frac{1}{n^2}} = \frac{1}{2} \quad (3.19)$$

Disregarding the higher-order harmonics, considering the voltage gain of the CLLC resonant circuit, and the redefined quality factor shown in (3.17), overall voltage gain of the DC/DC stage of the converter in AC to DC mode can be determined as shown in (3.20).

$$\frac{v_o}{V_{DC-link}} = \frac{\omega_r^2}{2\sqrt{(\omega_r^2 - 1)^2 + \frac{1}{Q^2} \left(k\omega_r^3 - \frac{\omega_r}{m} - k\omega_r + \frac{1}{m\omega_r} - \omega_r\right)^2}} \quad (3.20)$$

Following the same procedure, overall voltage gain of the DC/DC stage of the converter in DC to AC mode can be determined as shown in (3.21).

$$\frac{V_{DC-link}}{v_o} = \frac{\omega_r}{2\sqrt{\left(\omega_r - \frac{1}{m\omega_r} + k\omega_r\right)^2 + \frac{1}{Q^2} \left(1 + \frac{1}{m} - \frac{1}{m\omega_r^2}k(1 - \omega_r^2)\right)^2}} \quad (3.21)$$

Following (3.20) and (3.21), the overall gain of the converter becomes dependant to the duty ratio of the switches in leg B (D_s) (leg A (D_p)) during AC to DC (DC to AC) mode.

Fig. 3.9 illustrates the overall gain plot of the designed converter with active rectification. It shows that the converter's overall gain can be controlled independently using D_s . This approach will later be utilized in the controller to help the converter achieve reduced output voltage ripple.

3.4 Control System Design

As mentioned in the pervious sections, high input current quality, output voltage regulation, and low output voltage ripple are critical performance metrics in the design of the bidirectional AC/DC converter, especially when using low storage capacitances. Ensuring high input current quality minimizes harmonics, thereby reducing EMI and enhancing the overall efficiency of the power

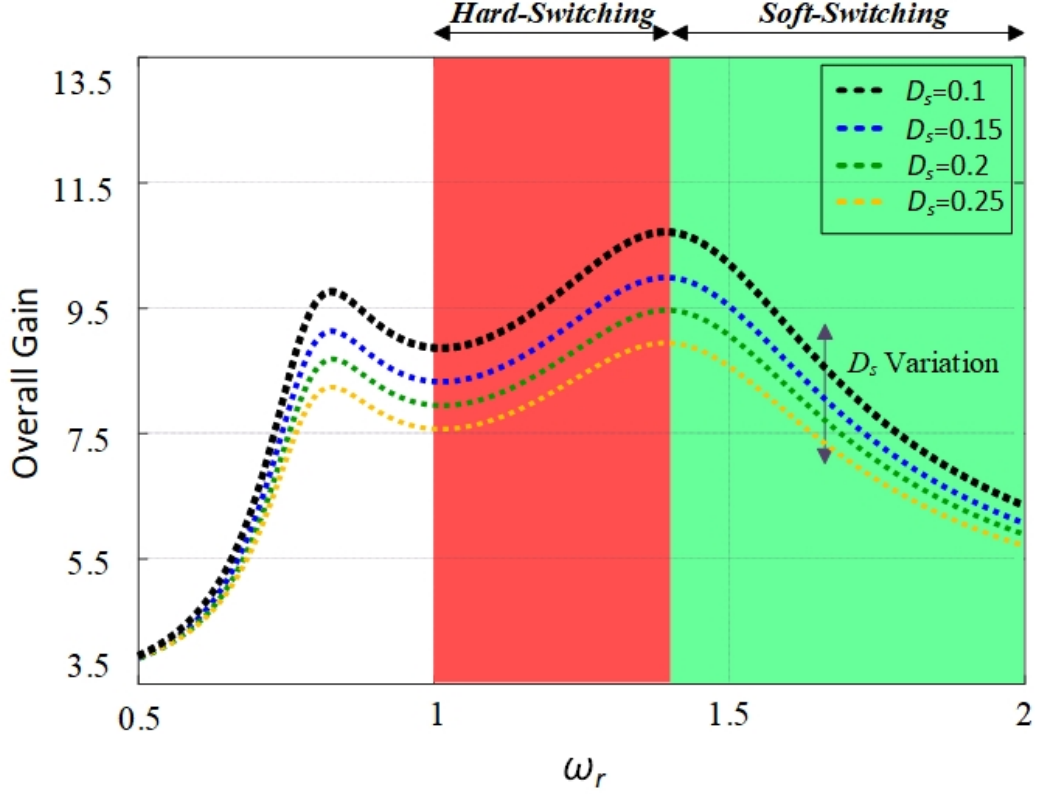


Figure 3.10: Overall voltage gain plot of the designed converter for $D_s > 0$.

system. Precise output voltage regulation is vital for maintaining stable operation, and low output voltage ripple is essential for providing a clean and stable DC output to the battery. This allows the elimination of bulky electrolytic-type capacitors and use of more reliable film capacitors in the converter design that not only reduces the physical size and cost of the system but also makes the converter more efficient and reliable. In the following, the detailed design of the developed controllers is discussed to illustrate how these performance metrics are achieved.

3.4.1 PFC Current Controller

As stated throughout the paper, a dq -based PFC control system has been developed for designed bidirectional AC/DC converter to provide high-quality grid current for both AC to DC and DC to AC modes of operation. To that end, the dq model presented in section III-A has been utilized to derive the transfer function of the system. Laplace transformation of (3.7) results in

(3.22) as shown below.

$$\begin{aligned}
si_{f,d} &= \frac{v_{inv,d}}{L_f} - \frac{v_{Cin,d}}{L_f} + \omega_g i_{f,q} - \frac{R_f}{L_f} i_{f,d} \\
si_{f,q} &= \frac{v_{inv,q}}{L_f} - \frac{v_{Cin,q}}{L_f} - \omega_g i_{f,d} - \frac{R_f}{L_f} i_{f,q} \\
si_{in,d} &= \frac{v_{Cin,d}}{L_{in}} - \frac{v_{in,d}}{L_{in}} + \omega_g i_{in,q} - \frac{R_{in}}{L_{in}} i_{in,d} \\
si_{in,q} &= \frac{v_{Cin,q}}{L_{in}} - \omega_g i_{in,d} - \frac{R_{in}}{L_{in}} i_{in,q} \\
sv_{Cin,d} &= \frac{i_{f,d}}{C_{in}} + \omega_g v_{Cin,q} - \frac{i_{in,d}}{C_{in}} \\
sv_{Cin,q} &= \frac{i_{f,q}}{C_{in}} - \omega_g v_{Cin,d} - \frac{i_{in,q}}{C_{in}}
\end{aligned} \tag{3.22}$$

Considering $i_{in,d}$ and $i_{in,q}$ as outputs and $v_{inv,d}$ and $v_{inv,q}$ as inputs of the system, the mathematical model presented in (3.22) can be re-written as shown in (3.23) where $v_{Cin,d}$, $v_{Cin,q}$, $i_{f,d}$ and $i_{f,q}$ are replaced with their equivalent values.

$$\begin{aligned}
si_{in,d} &= \frac{1}{L_{in}} \left(\frac{1}{s} \left(\frac{1}{C_{in}} \left(\frac{1}{s} \left(\frac{v_{inv,d}}{L_f} - \frac{v_{Cin,d}}{L_f} - \frac{R_f}{L_f} i_{f,d} \right) \right) \right. \right. \\
&\quad \left. \left. - \frac{i_{in,d}}{C_{in}} \right) \right) - \frac{v_{in,d}}{L_{in}} - \frac{R_{in}}{L_{in}} i_{in,d} \\
si_{in,q} &= \frac{1}{L_{in}} \left(\frac{1}{s} \left(\frac{1}{C_{in}} \left(\frac{1}{s} \left(\frac{v_{inv,q}}{L_f} - \frac{v_{Cin,q}}{L_f} - \frac{R_f}{L_f} i_{f,q} \right) \right) \right. \right. \\
&\quad \left. \left. - \frac{i_{in,q}}{C_{in}} \right) \right) - \frac{R_{in}}{L_{in}} i_{in,d}
\end{aligned} \tag{3.23}$$

since $i_{in,d}$ and $i_{in,q}$, and $v_{inv,d}$ and $v_{inv,q}$ are outputs and inputs of the system, respectively, (3.23) can be re-defined as shown in (3.24), where $d_d(s)$ and $d_q(s)$ are considered as disturbances to the system as shown in (3.25).

$$\begin{aligned}
\left(s + \frac{1}{sL_{in}C_{in}} + \frac{R_{in}}{L_{in}} \right) i_{in,d} &= \frac{1}{s^2 L_{in} C_{in} L_f} v_{inv,d} + d_d(s) \\
\left(s + \frac{1}{sL_{in}C_{in}} + \frac{R_{in}}{L_{in}} \right) i_{in,q} &= \frac{1}{s^2 L_{in} C_{in} L_f} v_{inv,q} + d_q(s)
\end{aligned} \tag{3.24}$$

$$\begin{aligned}
d_d(s) &= -\frac{v_{in,d}}{L_{in}} - \frac{1}{s^2 L_{in} C_{in}} \left(\frac{v_{Cin,d}}{L_f} + \frac{R_f}{L_f} i_{f,d} \right) \\
d_q(s) &= -\frac{1}{s^2 L_{in} C_{in}} \left(\frac{v_{Cin,q}}{L_f} + \frac{R_f}{L_f} i_{f,q} \right)
\end{aligned} \tag{3.25}$$

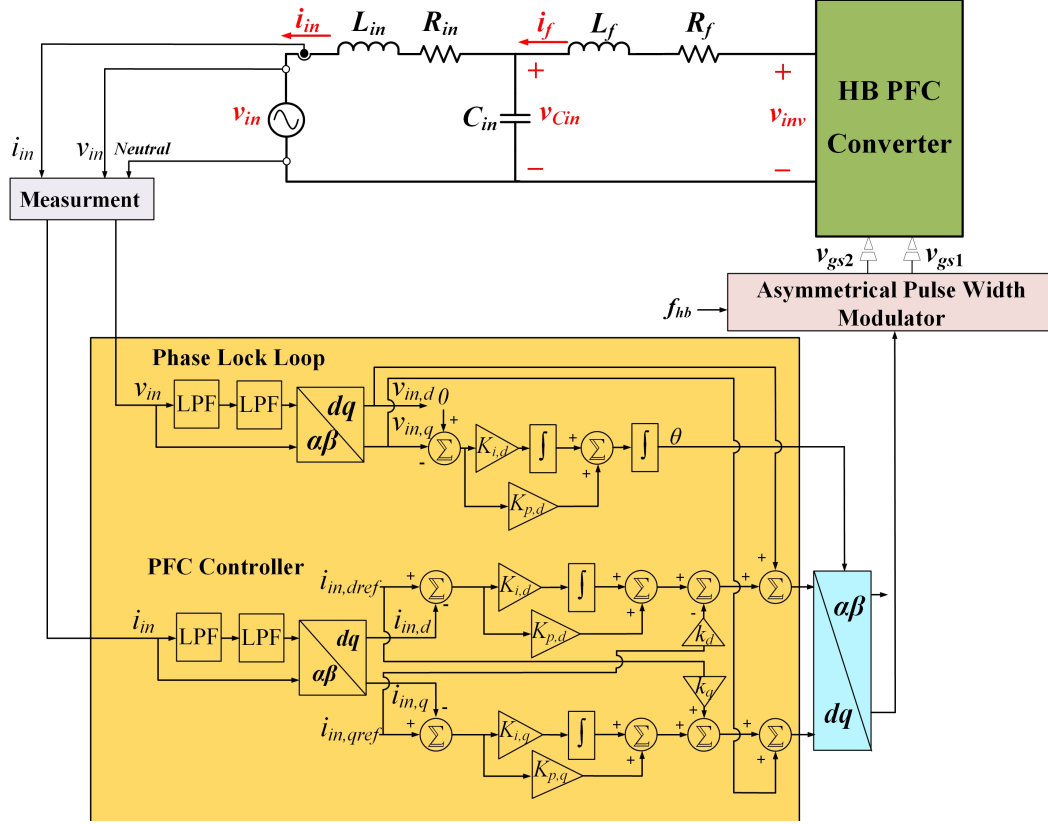


Figure 3.11: Block diagram of the developed PFC controller for the designed bidirectional converter.

as a result, d and q transfer functions of the system can be calculated as shown in (3.26).

$$\begin{aligned} \frac{i_{in,d}}{v_{inv,d}} = G_d(s) &= \frac{L_{in}/L_f}{s(s^2 L_{in}^2 C_{in} + s R_{in} L_{in} C_{in} + L_{in})} \\ \frac{i_{in,q}}{v_{inv,q}} = G_q(s) &= \frac{L_{in}/L_f}{s(s^2 L_{in}^2 C_{in} + s R_{in} L_{in} C_{in} + L_{in})} \end{aligned} \quad (3.26)$$

Using the transfer functions $G_d(s)$ and $G_q(s)$ calculated in (3.26), two PI controllers in the form of (3.27) can be designed for closed-loop stability of the system. To that end, Control Systems Analysis Toolbox in MATLAB has been utilized to calculate the proportional and integral gains of the PI controllers implemented for the dq PFC current controller in the designed controller following the the converter specifications presented in Section V.

$$\begin{aligned} C_{i,d}(s) &= K_{p,id} + \frac{K_{i,id}}{s} \\ C_{i,q}(s) &= K_{p,iq} + \frac{K_{i,iq}}{s} \end{aligned} \quad (3.27)$$

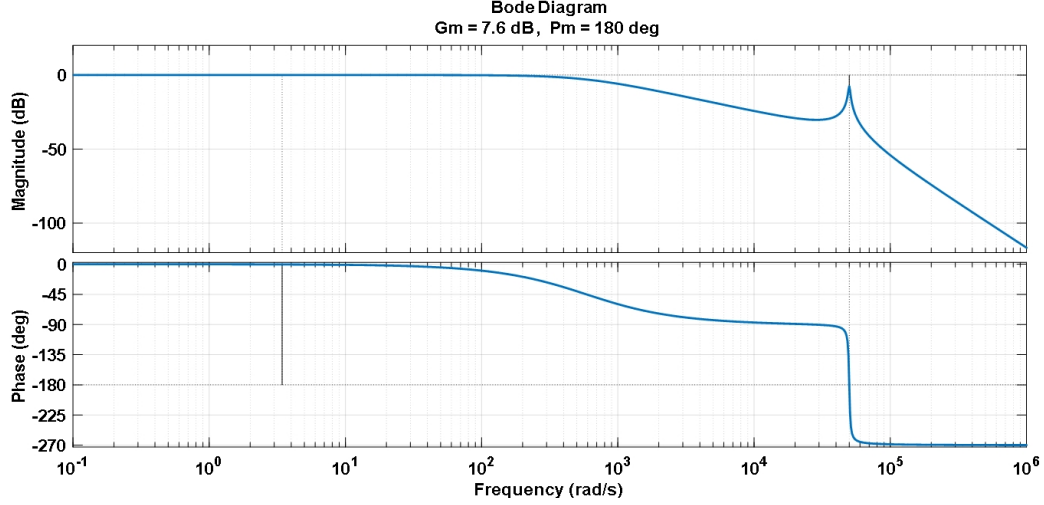


Figure 3.12: Bode diagram of the closed-loop system for the developed dq -based PFC controller.

In (3.27), to cancel-out the destructive effect of the PI's pole at zero, PI's zero should be considered close to the origin. Therefore, $K_{i,id}/K_{p,id} = K_{i,iq}/K_{p,iq} = 0.1$ has been considered. Moreover, the proportional gain of the $K_{p,id} = K_{p,iq} = 70$, and therefore, $K_{i,id} = K_{i,iq} = 7$ has been chosen for the controllers. The bode diagram of the closed-loop system is illustrated in Fig. 12, where phase margin and gain margin are 180° and 7.6dB, respectively.

3.4.2 Output Voltage Regulation

As illustrated in Fig. 3.12, VFM has been employed to regulate the output voltage of the designed bidirectional AC/DC converter during operation. The VFM-based controller is designed specifically for output voltage regulation and independent from ripple reduction controller, ensuring stability by avoiding continuous frequency variation due to high output voltage ripple, which results from the use of small DC-link and output filter capacitors. To achieve this, the average of the converter's output voltage was utilized to eliminate the low-frequency ripples. Then the measured voltage is compared with a reference value (i.e. $V_{o,ref} = 750V_{dc}$ for this design) to generate an error signal (see Fig. 3.12). This approach ensures that the output voltage ripple does not influence the output voltage regulation control loop and, consequently, the switching

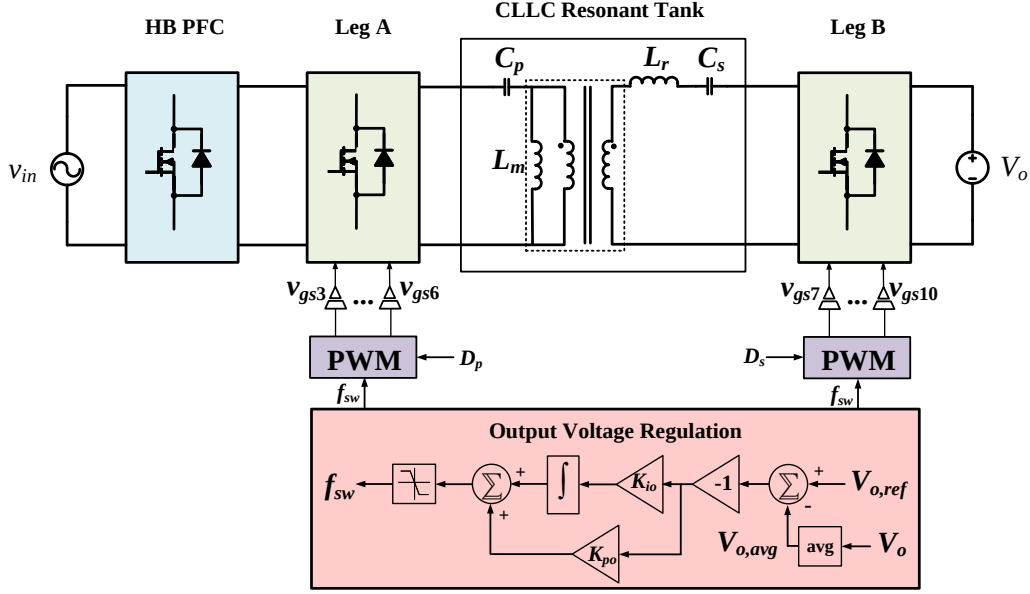


Figure 3.13: Block diagram of the developed VFM-based output voltage regulation controller for the designed converter.

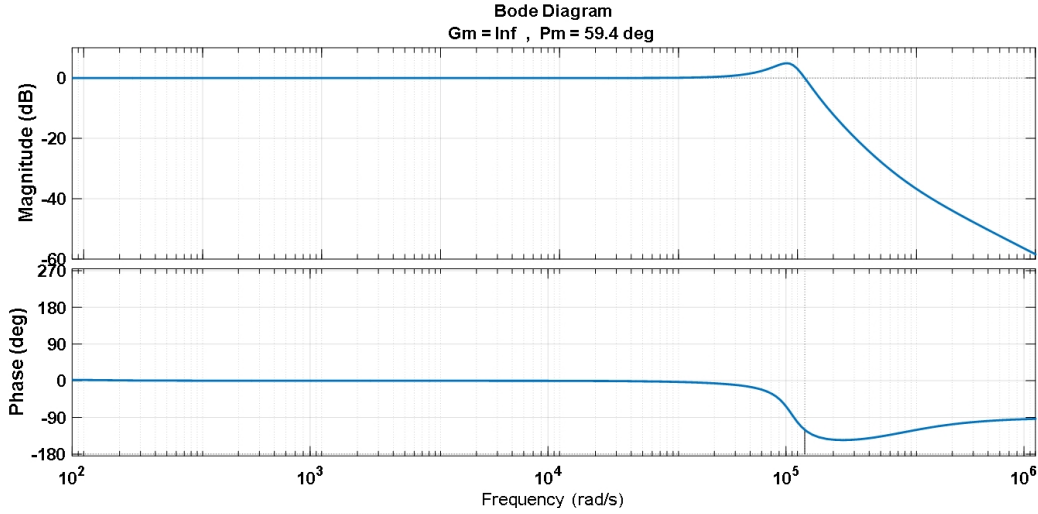


Figure 3.14: Bode diagram of the closed-loop system for the developed VFM-based controller.

frequency of the converter.

The error signal is subsequently fed into a PI controller to produce the required control signal, which in this case is the switching frequency (f_{sw}). The gains of the PI controller ($K_{i,o}$ and $K_{p,o}$), as shown in (3.28), are determined based on the fundamental harmonic approximation (FHA) and utilizing the

$$C_o(s) = K_{p,o} + \frac{K_{i,o}}{s} \quad (3.28)$$

The mechanism of the designed VFM-based output voltage regulation control system can be summarized in the following steps:

1. The control loop continually compares the average of the actual output voltage (V_o) with a reference voltage ($V_{o,\text{ref}}$, e.g., 750Vdc). In this way, the output ripple will have no effect on this loop.
2. Any deviation from $V_{o,\text{ref}}$ generates an error signal, which is processed by a PI controller presented in Fig. 3.12.
3. The PI controller dynamically adjusts the switching frequency (f_{sw}) to influence the voltage gain of the resonant converter based on the voltage gain curve of the converter presented in Fig. 3.9:
 - When V_o exceeds $V_{o,\text{ref}}$, f_{sw} increases to reduce the voltage gain.
 - When V_o falls below $V_{o,\text{ref}}$, f_{sw} decreases to increase the voltage gain.
4. Then, the switching frequency (f_{sw}) is applied to the switches in both leg A and leg B of the converter as shown in Fig. 3.12.

It's important to note that the overall closed-loop system comprises two subsystems operating at different frequencies: 1) the designed bridgeless bidirectional AC/DC converter, which operates at a very high frequency ($f_{\text{sw}} \approx 100\text{kHz}$), and 2) the VFM-based PI controller, which operates at a lower frequency. In control system theory, when subsystems interact at different operating frequencies, using the full model of the high-frequency subsystem can unnecessarily complicate the overall closed-loop system. Instead, employing an average model of the high-frequency subsystem is sufficient for designing the low-frequency (PI) controller [88]-[89]. Therefore, the FHA model is adequate for designing the PI controllers for output voltage regulation in the designed converter.

Accordingly, a PI controller as described in (3.28) is developed for output voltage regulation. To counteract the PI's pole at zero, the PI's zero is positioned close to the origin, setting $K_{io}/K_{po} = 133 \times 10^{-7}$. Considering the output range of the VFM controller ($f_{sw} \approx 100kHz$), the proportional gain of the PI controller is set at $K_{po} = 750$. Consequently, $K_{io} = 0.01$ is calculated. The Bode diagram of the closed-loop system is given in Fig. 3.13. The bode diagram in Fig. 3.13 indicates a phase margin of 59.7° and a gain margin of infinity that shows very stable system.

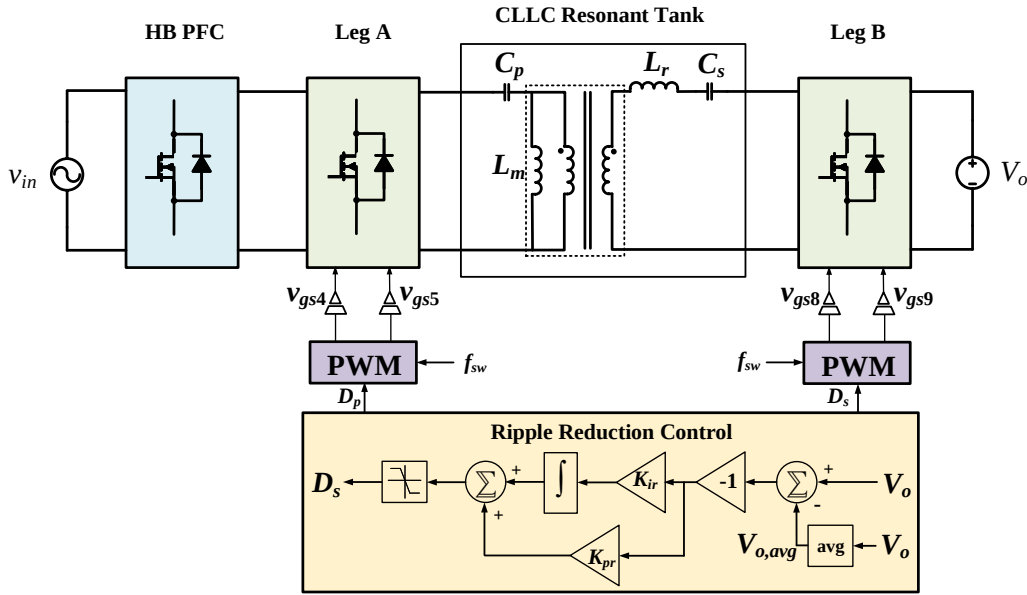


Figure 3.15: Block diagram of the developed ripple reduction controller for the designed converter.

3.4.3 Ripple Reduction Controller

As illustrated in Fig. 3.14, the designed converter employs a closed-loop controller based on Pulse Width Modulation (PWM) to address the high output voltage ripple caused by the use of low storage capacitances. This PWM-based controller is designed specifically to reduce output voltage ripple by controlling switches S_8 and S_9 in leg B of the converter during AC to DC mode and S_4 and S_5 in leg A of the converter during DC to AC mode. The ripple reduction controller, as shown in Fig. 5, extracts the ripple component of the

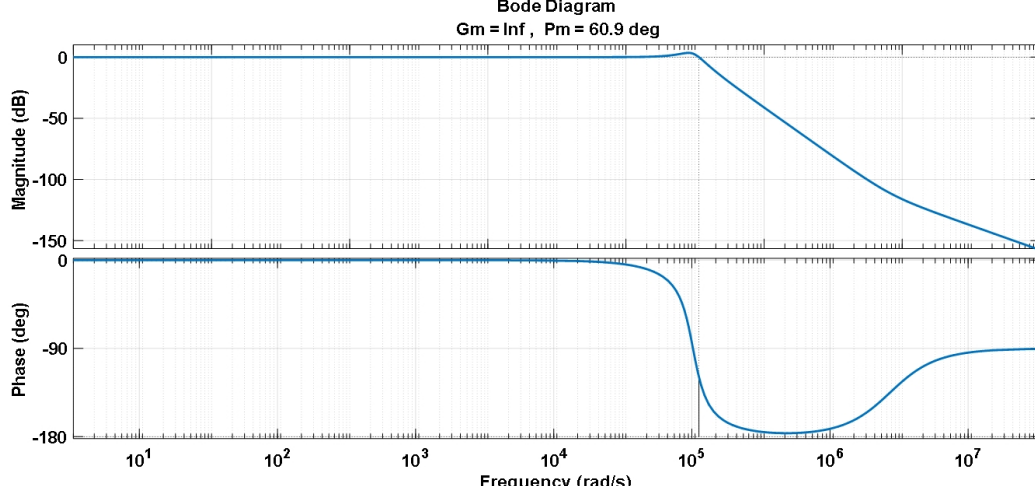


Figure 3.16: Bode diagram of the closed-loop system for the developed ripple reduction controller.

output voltage (V_o) by subtracting the average output voltage ($V_{o,avg}$) from the instantaneous voltage. This isolated ripple is then processed to dynamically adjust the secondary-side duty ratio (D_s) for effective ripple minimization. By operating independently of the voltage regulation and PFC loops, the ripple controller ensures stable system performance without interference from other control mechanisms.

$$C_r(s) = K_{p,r} + \frac{K_{i,r}}{s} \quad (3.29)$$

Considering the fact that the error signal in this case is the output voltage ripple ($E = Ripple$), the control signal (D_s) generated by (3.29) can be defined in (3.30).

$$D_s(t) = K_{p,r}Ripple(t) + K_{i,r} \int_0^t Ripple(\tau)d\tau \quad (3.30)$$

Now combining the time-varying D_s and equivalent resistance (R_{ac}) defined in (3.16) results in (3.31).

$$R_{ac} = \frac{8}{\pi^2} \left(1 - \left[K_{p,r}Ripple(t) + K_{i,r} \int_0^t Ripple(\tau)d\tau \right]^2 \right) R_L \quad (3.31)$$

By appropriately selecting the PI controller gains ($K_{p,r}$ and $K_{i,r}$), the equivalent resistance (R_{ac}), quality factor (Q) and, consequently, the overall gain

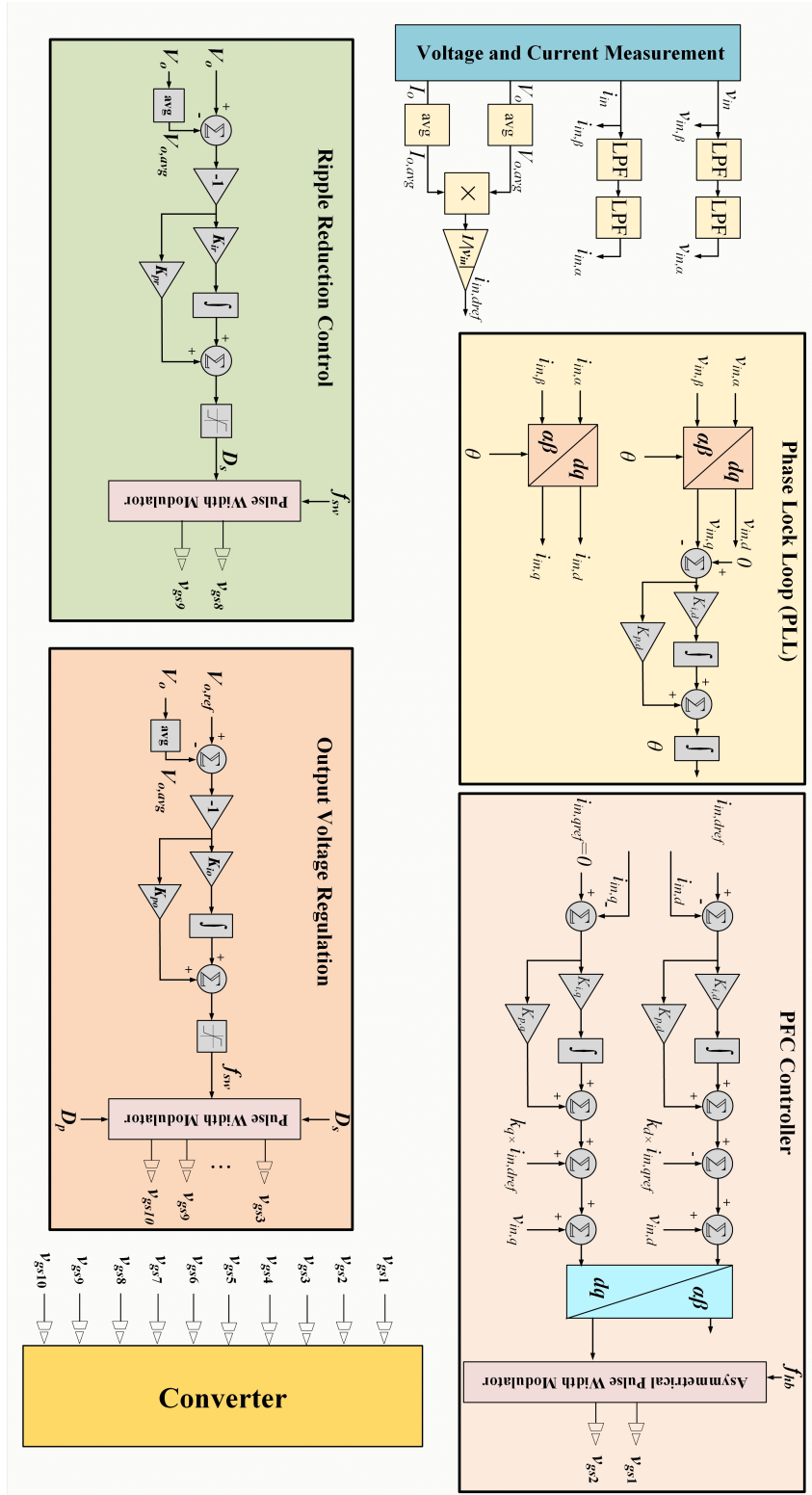


Figure 3.17: Unified block diagram representation of all the developed control systems.

of the converter can be controlled by the PI controller to minimize the output voltage ripple, allowing the use of low storage capacitances.

Similar to the VFM controller design, the overall closed-loop system includes two subsystems with different operating frequencies: 1) the designed bridgeless AC/DC converter operating at a high frequency ($f_{sw} \approx 100kHz$), and 2) the PWM-based PI controller operating at a lower frequency. As discussed in the VFM controller design, using an average model of the system suffices for designing the low-frequency (PI) controller for output voltage ripple reduction [88]-[89]. Therefore, the FHA model is adequate for PI controller design.

To this end, a PI controller as described in (3.29) is developed for output voltage regulation. To mitigate the PI's pole at zero, the PI's zero is placed near the origin, resulting in $K_{i,r}/K_{p,r} = 10^{-3}$. Given the output range of the PWM-based controller, the proportional gain is set to $K_{p,r} = 0.01$, and consequently, $K_{i,r} = 0.00001$. The Bode diagram of the closed-loop system is shown in Fig. 3.16, with phase and gain margins of 60.9° and infinity, respectively.

For simplicity and practicality, this unified control block diagram has been presented as Fig. 3.17 to consolidate the previously separated control systems into a single integrated structure. The diagram demonstrates the interconnections between the PFC controller, output voltage regulation loop, and ripple reduction control, streamlining the implementation while maintaining robust functionality. The input current controller dynamically adjusts the input current reference ($i_{in,dref}$) based on load demand and input voltage measurements, ensuring proper power factor correction (PFC) and matching input power with output power. The output voltage regulation loop utilizes the switching frequency (f_{sw}) to stabilize the output voltage (V_o) at its reference value ($V_{o,ref}$) under varying load conditions, while the ripple reduction control dynamically adjusts the secondary-side duty ratio (D_s) to minimize ripple independently of the voltage regulation loop. This unified approach enhances practicality by reducing complexity and ensuring efficient and autonomous operation of each subsystem.

It is important to note that the ripple reduction controller operates by targeting the low-frequency ripple component (120 Hz) in the output voltage. With a fast sampling time of 1 μ s, the controller accurately measures and processes the ripple, adjusting the duty cycle (D_s) of Leg B at the ripple frequency to achieve effective cancellation. This process is robust against high-frequency noise due to proper signal filtering and operates independently of high-frequency switching dynamics, ensuring precise ripple minimization without impacting other control loops.

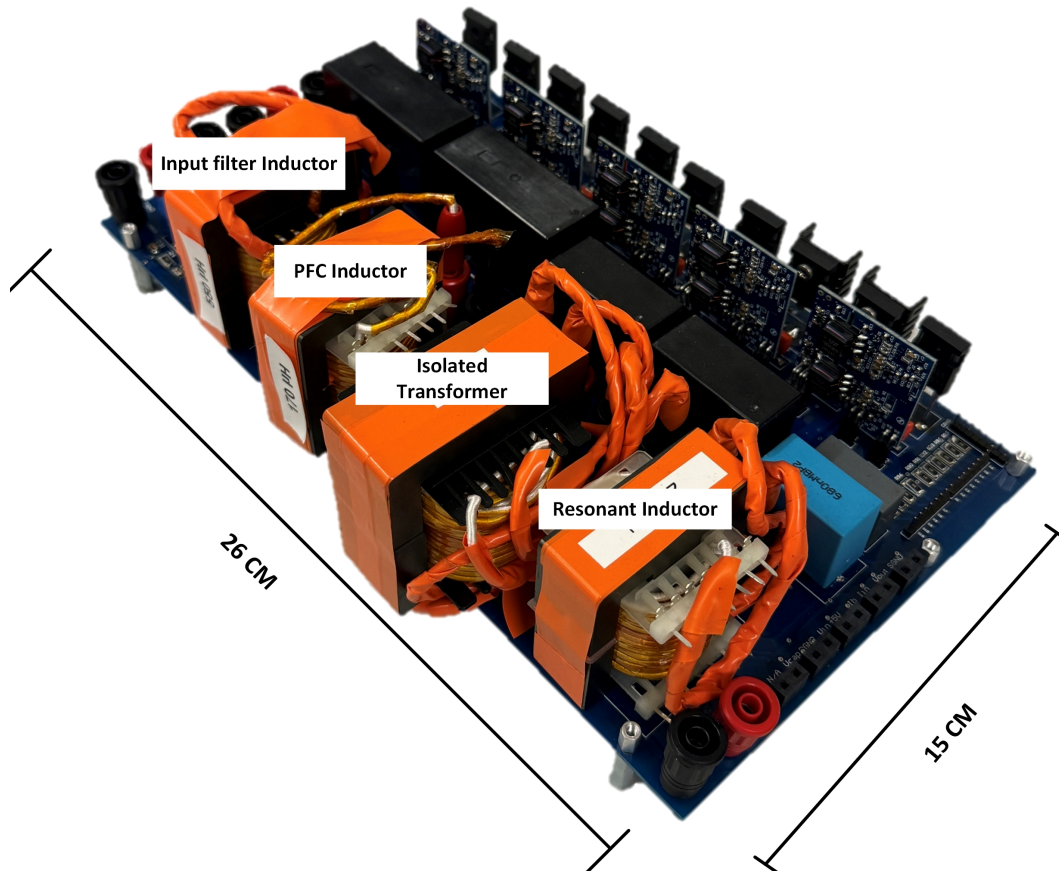


Figure 3.18: Picture of the Proof-of-concept prototype.

3.5 Experimental Validation

To validate the performance of the designed bidirectional AC/DC converter and the efficacy of the designed control systems, a proof-of-concept hardware

Table 3.1: Parameter Values of the Designed Prototype

Parameters	Values
Rated Power (P_o)	$1kW$
Output Voltage (V_o)	$750V_{dc}$
Input AC Voltage (v_{in})	$90 - 135V_{ac,rms}$
Leg A and B Switching Frequency (f_{sw})	$\geq 100kHz$
HB Switching Frequency (f_{hb})	$70kHz$
Input Filter Inductance (L_{in})	$550\mu H$
Input Filter Capacitance (C_{in})	$0.8\mu F$
PFC Inductance (L_f)	$170\mu H$
DC-link Capacitances (C_{i1}, C_{i2})	$50\mu F$
Primary Resonant Capacitance (C_p)	$0.068\mu F$
Secondary Resonant Capacitance (C_s)	$0.68\mu F$
Resonant Inductance (L_r)	$260\mu H$
Magnetizing Inductance (L_m)	$270\mu H$
Output Filter Capacitances (C_{o1}, C_{o2})	$25\mu F$
Switches ($S_1 - S_2$)	IMW120R020M1HXKSA1
Switches ($S_3 - S_{10}$)	IMW65R030M1HXKSA1
Snubber Capacitors ($C_{s1} - C_{s10}$)	$200pF$
Dead-time (t_{dt})	$30ns$

prototype was developed and tested in the laboratory. The prototype employs a $1kW$, $120V_{rms}/750V_{dc}$, $90 - 120kHz$ SiC-based design. Additionally, the PLECS RT Box 1 was utilized as the controller unit. Fig. 3.17 presents a photograph of the developed hardware prototype, and Table I provides the system specifications and parameters. Moreover, the design procedure of the parameters presented in Table I is provided in the Appendix.

3.5.1 AC to DC Mode Experimental Results

The experimental waveforms obtained from the prototype in its AC to DC operational mode are displayed in Figs. 3.19–3.27. Fig. 3.19 shows the input voltage (v_{in}), input current (i_{in}), output voltage (V_o), and output current (I_o) waveforms at an input of $120V_{ac,rms}$ and an output voltage of $750V_{dc}$. As illustrated in Fig. 3.19, the input power factor is $PF = 0.994$, and the developed converter achieved an efficiency of 94.4% at approximately 1kW power, as measured by the "power analysis tool" from the KEYSIGHT MSOX6004A oscilloscope.

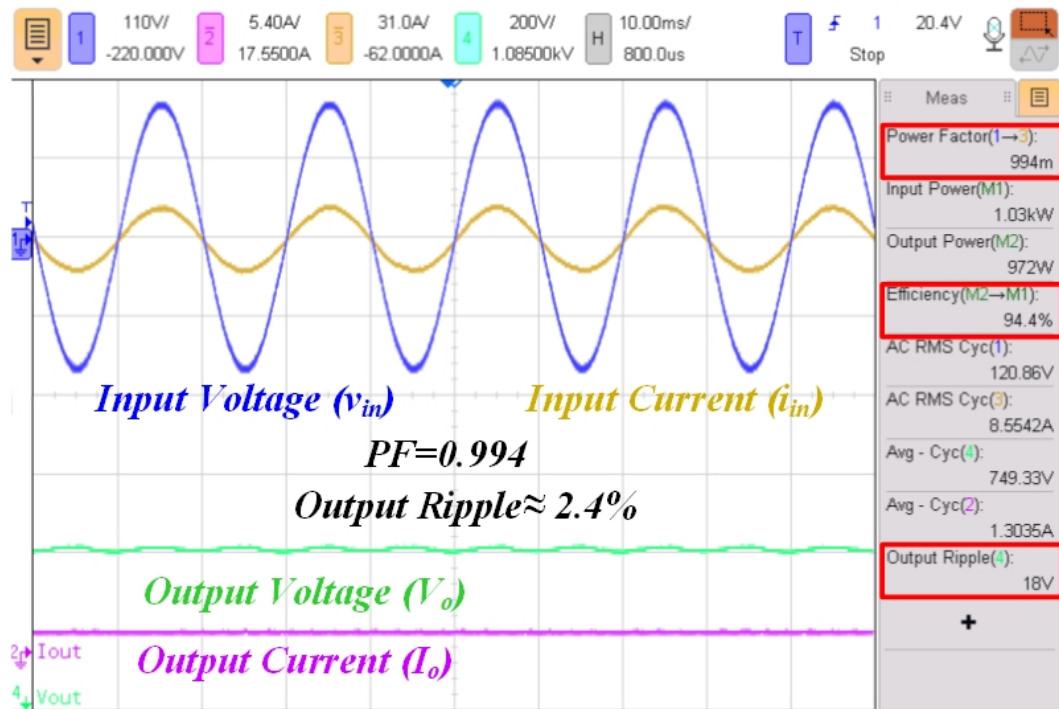


Figure 3.19: Input and Output waveforms of the converter at rated power in AC to DC mode.

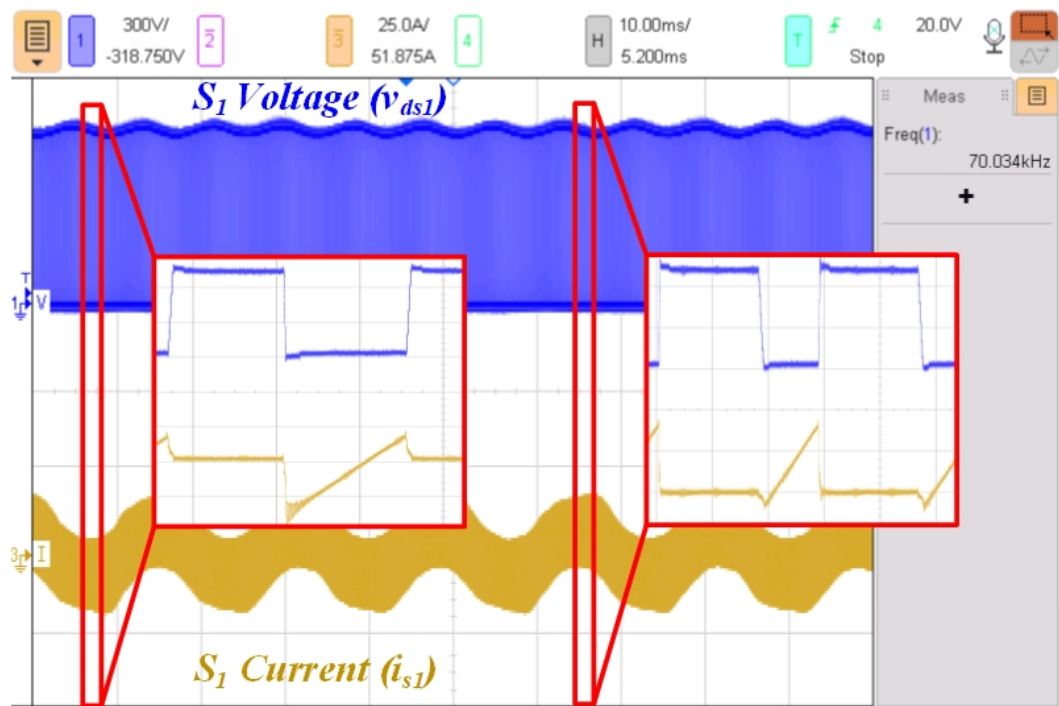


Figure 3.20: Voltage over and current flowing through S_1 at line frequency in AC to DC mode.

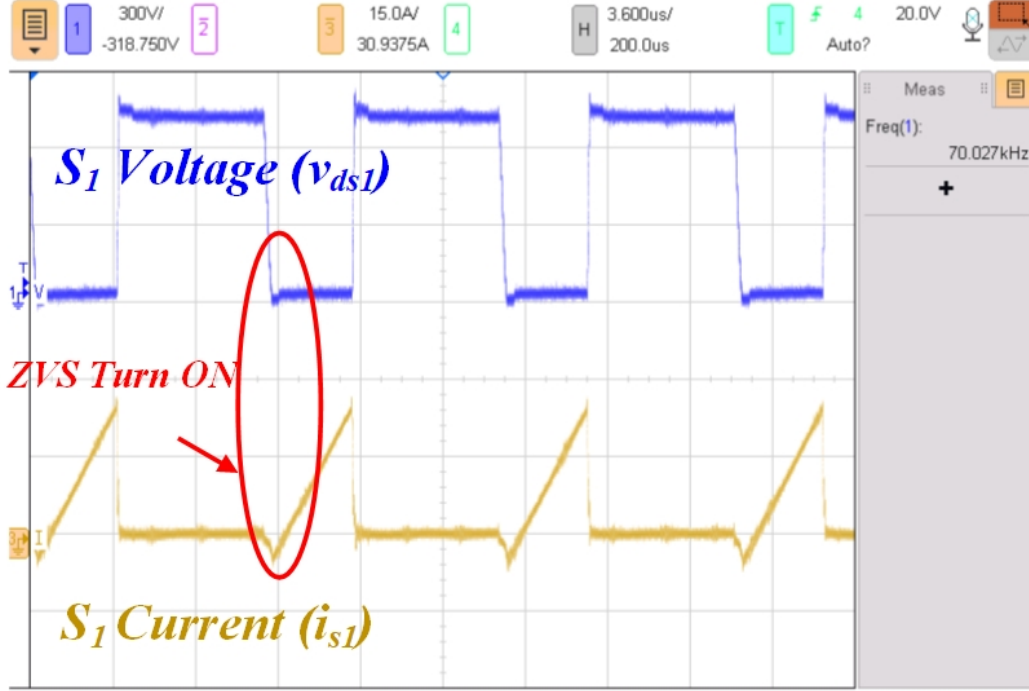


Figure 3.21: Voltage over and current flowing through S_1 at switching frequency in AC to DC mode.

The switches S_1 , S_3 , S_4 , and S_8 voltage and current waveforms at line and switching frequency are shown in Figs. 3.20-3.27. Each switch current in the designed converter has a low-frequency envelope and therefore, the soft-switching operation of each switch needs to be verified in both positive and negative line cycles. Due to the similar operation of the switches S_1 and S_2 , S_3 and S_6 , S_4 and S_5 , and S_8 and S_9 , showing the switching waveforms for S_1 , S_3 , S_4 , and S_8 would be sufficient to confirm the soft-switching performance of the converter.

The voltage and current waveforms of switch S_1 at line frequency are shown in Fig. 3.20. Moreover, the soft-switching operation of the switch S_1 in both positive and negative line cycles are shown in Fig. 3.20. To further verify the soft-switching operation of switch S_1 , voltage and current waveforms of switch S_1 at switching frequency are illustrated in Fig. 3.21. ZVS turn ON and ZCS turn off can be observed in Fig. 3.21, which occurs due to the design of the LCL filter and PFC stage of the converter.

The voltage and current waveforms of switch S_3 at line frequency are shown

in Fig. 3.22. Moreover, the soft-switching operation of the switch S_3 is shown in Fig. 3.22. To further verify the soft-switching operation of switch S_3 , voltage and current waveforms of switch S_3 at switching frequency are illustrated in Fig. 3.23. Since the resonant current is lagging behind the resonant voltage due to the presence of CLLC resonant converter, switch S_3 current first flows through its antiparallel diode. This is why as shown in Fig. 3.23, S_3 current is negative at the moment that it turns ON, resulting in ZVS Turn ON for Switch S_3 . Moreover, due to the presence of snubber capacitors, voltage across S_3 slowly rises from zero proving near ZCS turn OFF for this switch as shown in Fig. 3.23.

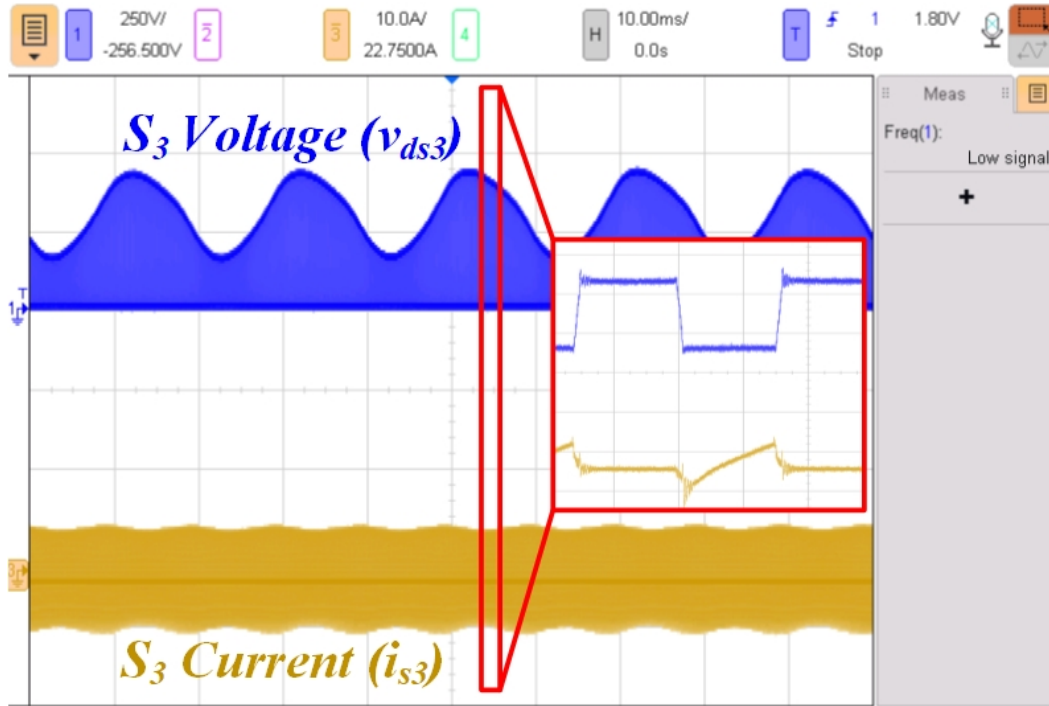


Figure 3.22: Voltage over and current flowing through S_3 at line frequency in AC to DC mode.

Similarly, the voltage and current waveforms of switch S_4 at line frequency are shown in Fig. 3.24. Moreover, the soft-switching operation of the switch S_4 is shown in Fig. 3.24. To further verify the soft-switching operation of switch S_4 , voltage and current waveforms of S_4 at switching frequency are illustrated in Fig. 3.25. Similar to the switch S_3 , switch S_4 current first flows through its antiparallel diode resulting in ZVS Turn ON for Switch S_4 as illustrated in

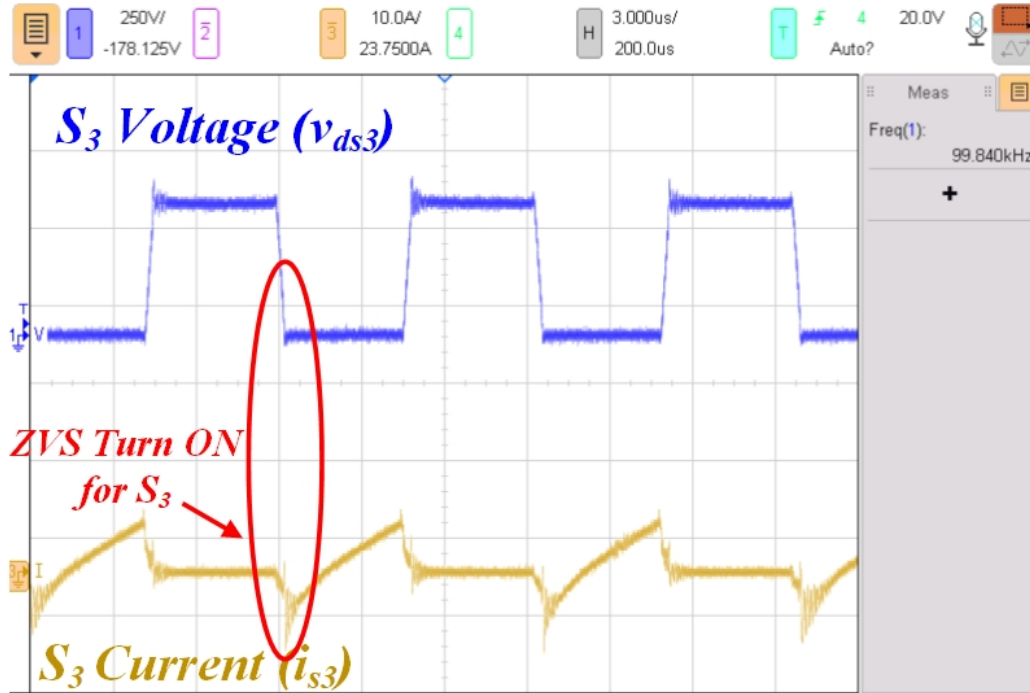


Figure 3.23: Voltage over and current flowing through S_3 at switching frequency in AC to DC mode.

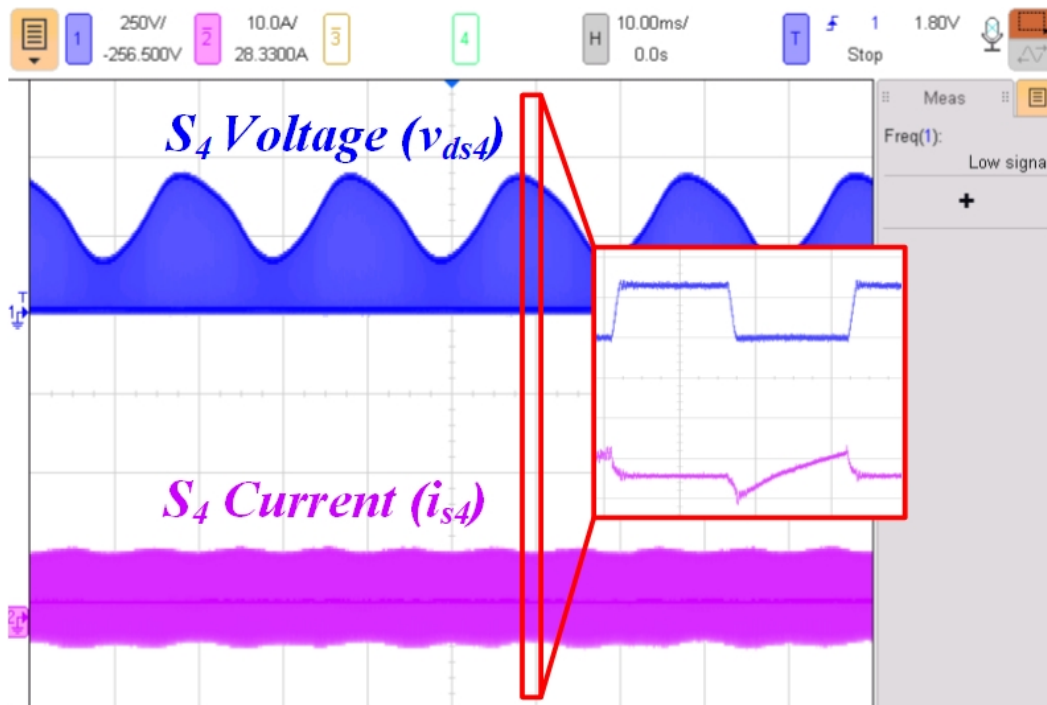


Figure 3.24: Voltage over and current flowing through S_4 at line frequency in AC to DC mode.

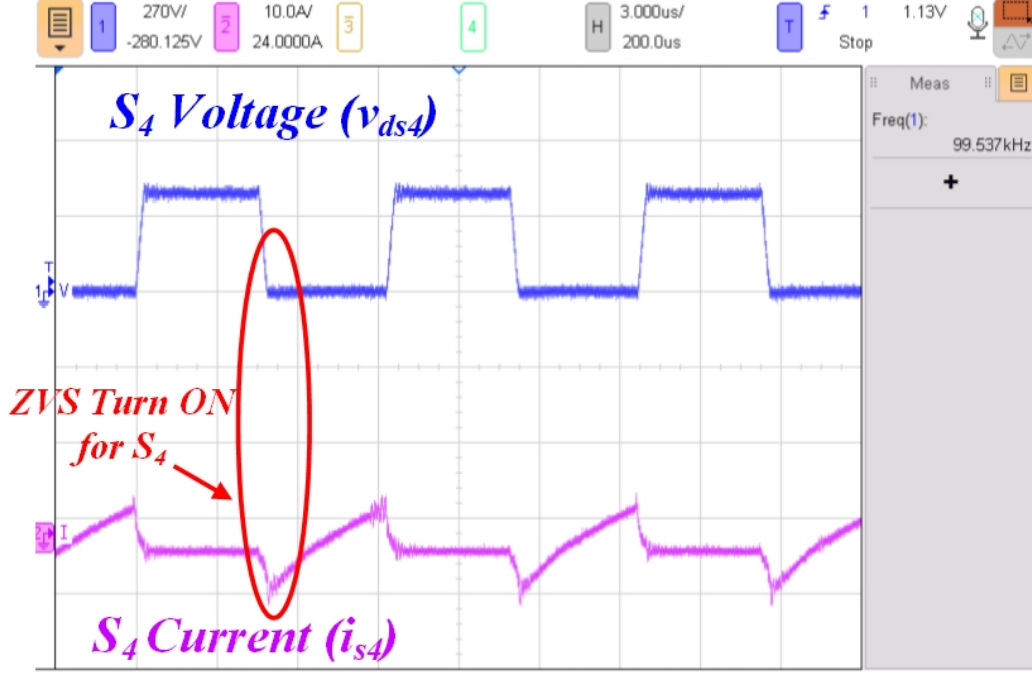


Figure 3.25: Voltage over and current flowing through S_4 at switching frequency in AC to DC mode.

Fig. 3.25. Moreover, due to the presence of snubber capacitors, voltage across S_4 slowly rises from zero proving near ZCS turn OFF for this switch as shown in Fig. 3.25.

Similar to the switches S_3 and S_4 , to show the soft-switching operation of the switch S_8 , its voltage and current waveforms at line frequency are shown in Fig. 3.26. Moreover, the soft-switching operation of the switch S_8 is shown in Fig. 3.26. To further verify the soft-switching operation of switch S_8 , voltage and current waveforms of S_8 at switching frequency are illustrated in Fig. 3.27. Similar to the switches S_3 and S_4 , switch S_8 current first flows through its antiparallel diode resulting in ZVS Turn ON as illustrated in Fig. 3.27. Moreover, due to the presence of snubber capacitors, voltage across S_8 slowly rises from zero proving near ZCS turn OFF for this switch as shown in Fig. 3.27.

Furthermore, the voltage waveforms of the DC-link capacitors C_{i1} and C_{i2} (V_{ci1} and V_{ci2}) and the overall DC-link voltage $V_{DC-link}$ are presented in Fig. 3.28 at line frequency. The voltage balance and stable voltage across DC-link

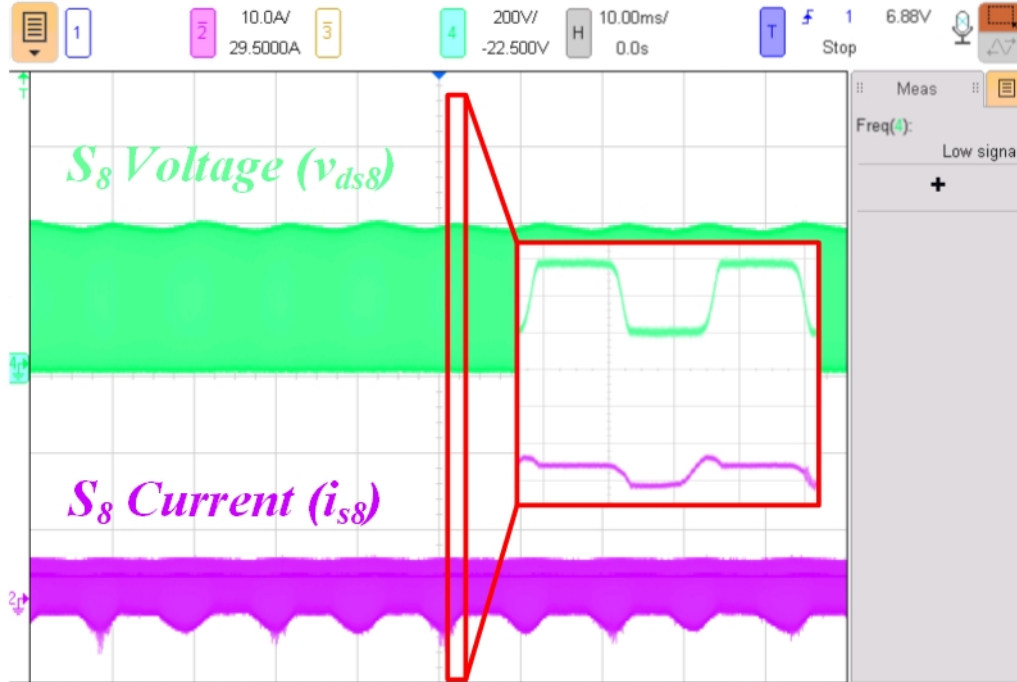


Figure 3.26: Voltage over and current flowing through S_8 at line frequency in AC to DC mode.

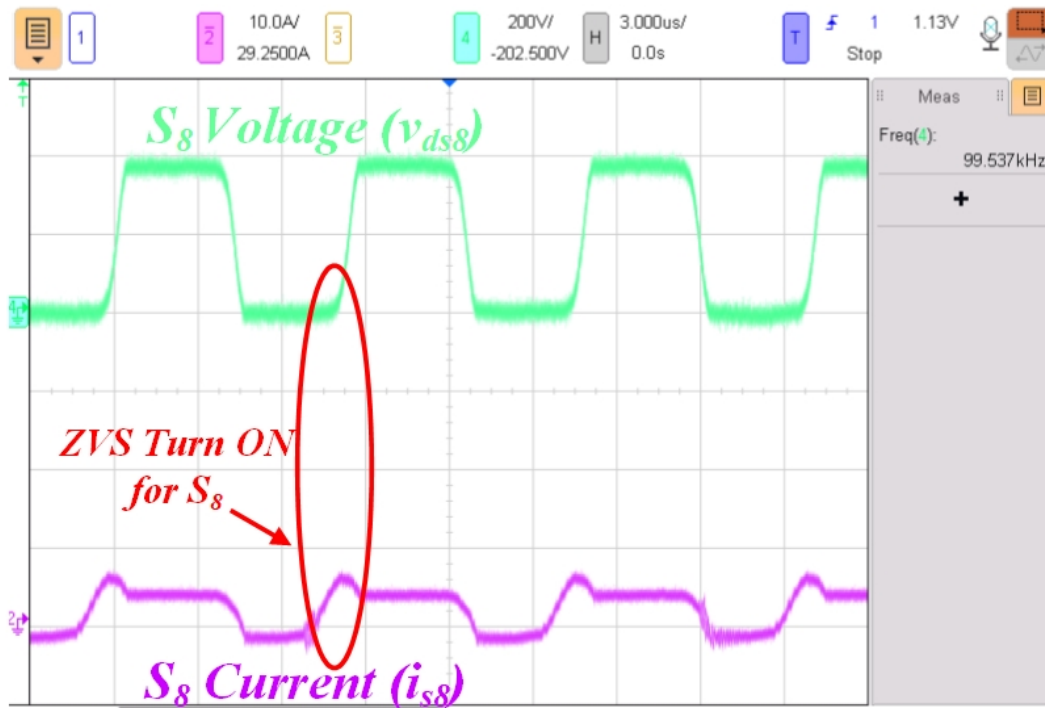


Figure 3.27: Voltage over and current flowing through S_8 at switching frequency in AC to DC mode.

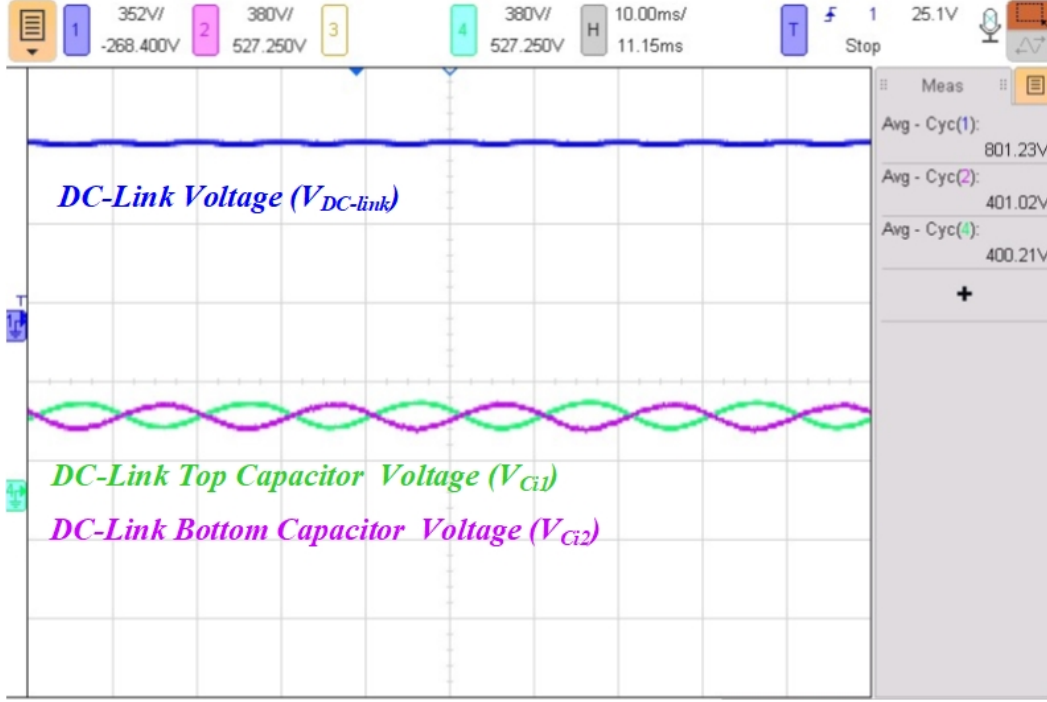


Figure 3.28: Voltage over the DC-link capacitors C_{i1} (V_{Ci1}) and C_{i2} (V_{Ci1}), and overall DC-link voltage in AC to DC mode.

capacitors can be seen in this figure.

3.5.2 DC to AC Mode Experimental Results

The experimental waveforms obtained from the prototype in its DC to AC operational mode are displayed in Figs. 3.29–3.32. Fig. 3.19 shows the grid voltage (v_{in}), injected grid current (i_{in}), DC-side voltage (V_o), and DC-side current (I_o) waveforms at the grid voltage of $120V_{ac,rms}$ and an DC-side voltage of $750V_{dc}$. As illustrated in Fig. 3.29, the input power factor is $PF = 0.976$, and the developed converter achieved an efficiency of 96.2% at approximately 1kW power, as measured by the "power analysis tool" from the KEYSIGHT MSOX6004A oscilloscope.

The switches S_1 , S_7 and S_8 voltage and current waveforms at switching frequency are shown in Figs. 3.30-3.32. Each switch current in the designed converter has a low-frequency envelope and therefore, the soft-switching operation of each switch needs to be verified. The operation of the switches S_1 and S_2 , S_4 and S_5 , S_7 and S_{10} , and S_8 and S_9 are similar. Moreover, the operation

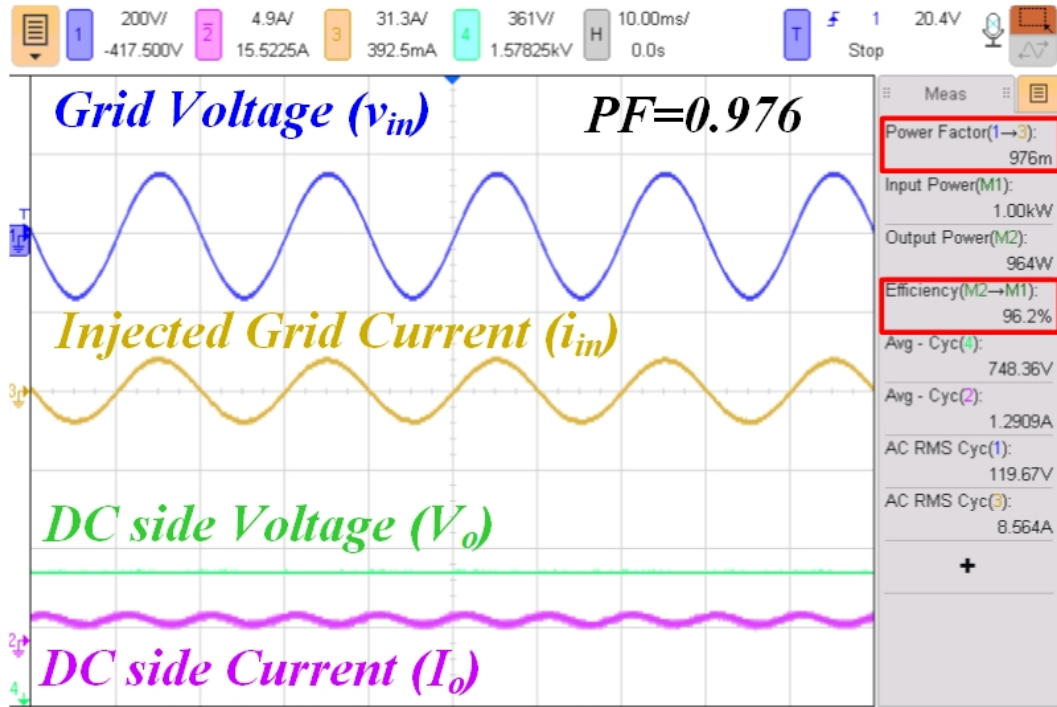


Figure 3.29: Input and Output waveforms of the converter at rated power in DC to AC mode.

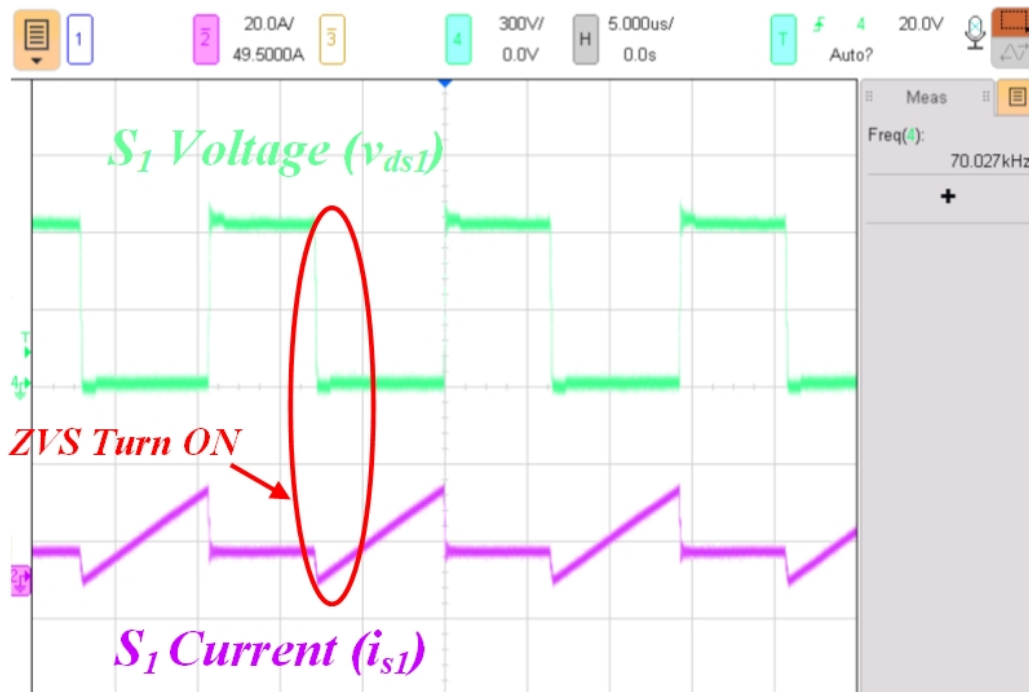


Figure 3.30: Voltage over and current flowing through S_1 at switching frequency in DC to AC mode.

of switch S_4 in DC to AC mode is similar to the operation of switch S_8 in AC to DC mode. Therefore, showing the switching waveforms for S_1 , S_7 and S_8 would be sufficient to confirm the soft-switching performance of the converter in DC to AC mode.

To show the soft-switching operation of switch S_1 in DC to AC mode, voltage and current waveforms of switch S_1 at switching frequency are illustrated in Fig. 3.30. Due to the specific design of the HB converter and the PFC inductor, switch S_1 current first flows through its antiparallel diode. This is why as shown in Fig. 3.30, S_1 current is negative at the moment that it turns ON, resulting in ZVS Turn ON for Switch S_1 . Moreover, due to the presence of snubber capacitors, voltage across S_1 slowly rises from zero proving near ZCS turn OFF for this switch as shown in Fig. 3.30.



Figure 3.31: Voltage over and current flowing through S_7 at switching frequency in DC to AC mode.

Moreover, to verify the soft-switching operation of switch S_7 in DC to AC mode, voltage and current waveforms of S_7 at switching frequency are illustrated in Fig. 3.31. Due to the presence of the CLLC resonant converter, switch S_7 current first flows through its antiparallel diode resulting in ZVS

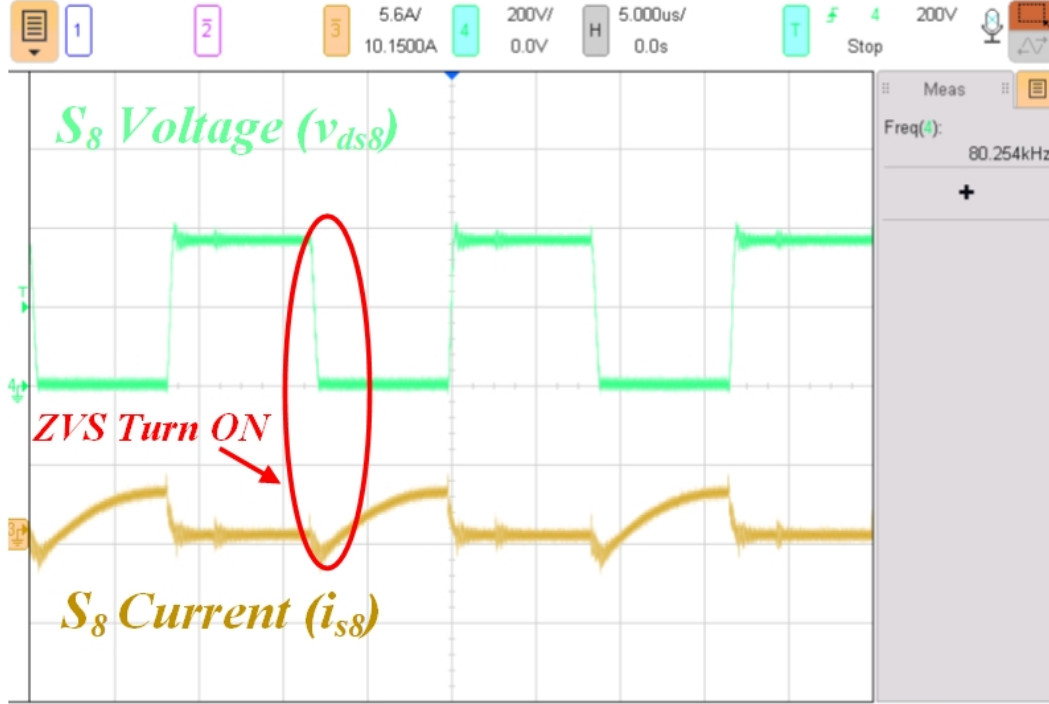


Figure 3.32: Voltage over and current flowing through S_8 at switching frequency in DC to AC mode.

Turn ON for Switch S_7 as illustrated in Fig. 3.31. Moreover, due to the presence of snubber capacitors, voltage across S_7 slowly rises from zero proving near ZCS turn OFF for this switch as shown in Fig. 3.31.

Similar to the switch S_7 , switch S_8 current first flows through its antiparallel diode resulting in ZVS Turn ON for Switch S_8 as illustrated in Fig. 3.32. Moreover, due to the presence of snubber capacitors, voltage across S_8 slowly rises from zero proving near ZCS turn OFF for this switch as shown in Fig. 3.32.

3.5.3 Dynamic Response Experimental Results

To further validate the performance of the developed closed-loop control systems, dynamic responses are captured in case of voltage reference tracking in AC to DC mode and current reference tracking in DC to AC mode. The dynamic responses of the designed converter are shown in Figs. 3.33 and 3.34.

To validate that developed VFM-based output voltage control system in AC to DC mode is able to regulate the output voltage of the designed converter

(V_o) for different input voltages (v_{in}), the input voltage of the converter is changed from $120V_{rms}$ to $100V_{rms}$ and the dynamic response the converter is illustrated in Fig. 3.33. As can be seen in Fig. 3.33, the closed-loop control system was able to maintain the $750V_{dc}$ output of the system despite the change in the input voltage of the converter with zero steady-state error and fast transient response.

To validate the performance of the developed dq -based PFC current controller regarding reference current tracking, reference current of the converter is decreased by 15% during the DC to AC operation of the converter. Fig. 3.34 illustrates the dynamic performance of the converter to this reference variation. Grid voltage (v_{in}), injected grid current (i_{in}) and DC side voltage (V_o) of the converter are shown in Fig. 3.34. It can be seen in Fig. 3.33 that the dq -based PFC control system was able to track the new reference current with zero steady-state error and fast transient response.

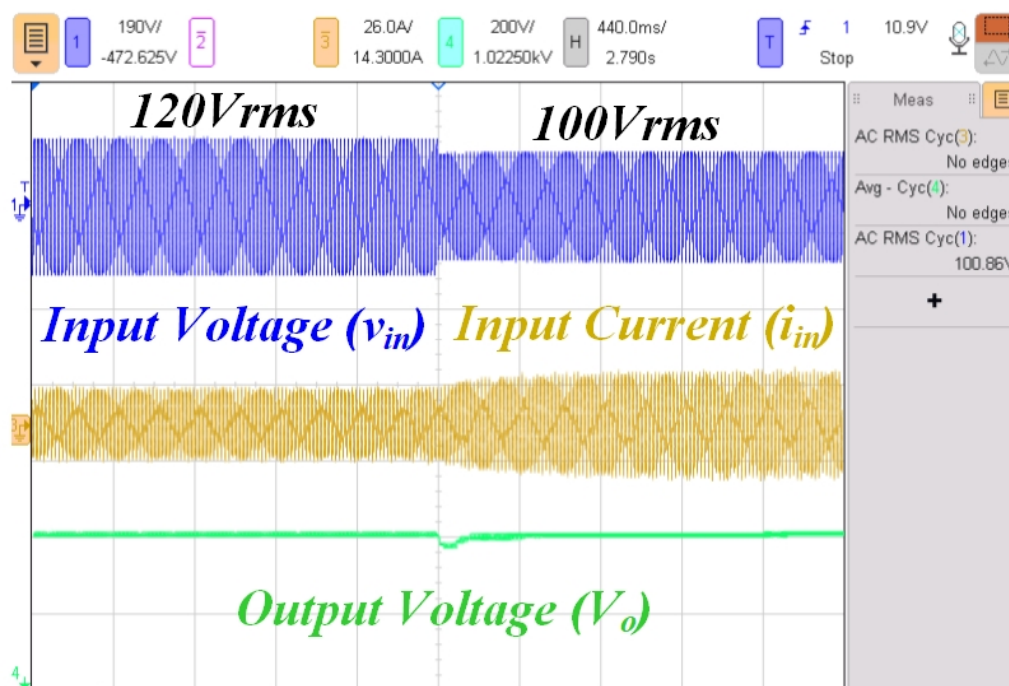


Figure 3.33: Dynamic performance of the system against input voltage variation in AC to DC mode.

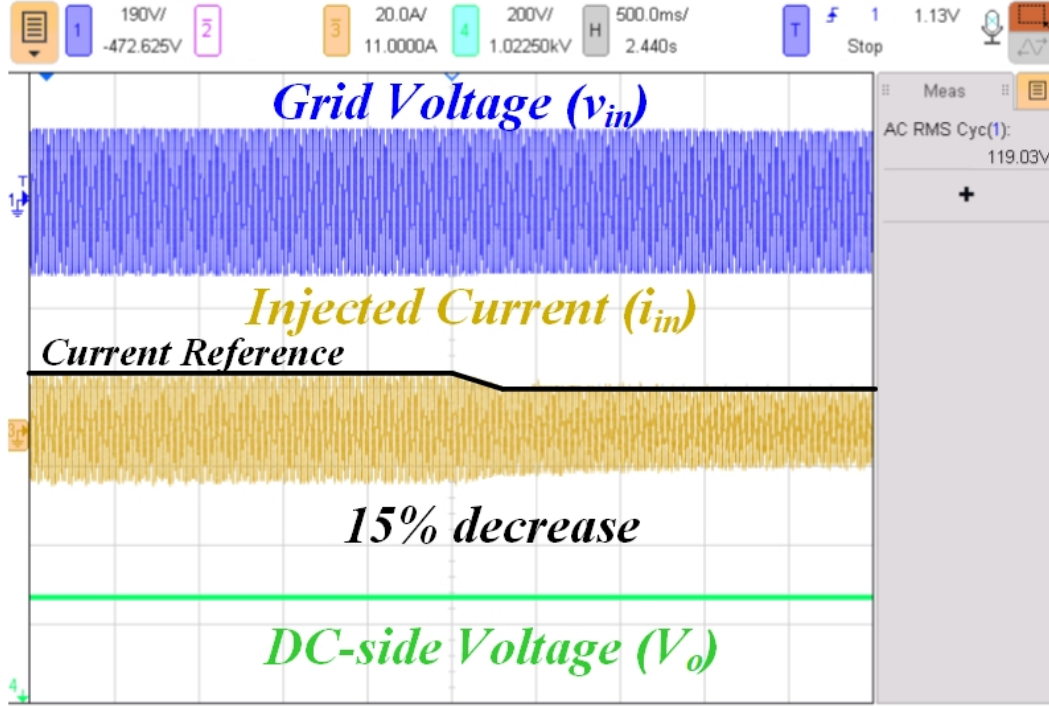


Figure 3.34: Dynamic performance of the system against input current reference change in DC to AC mode.

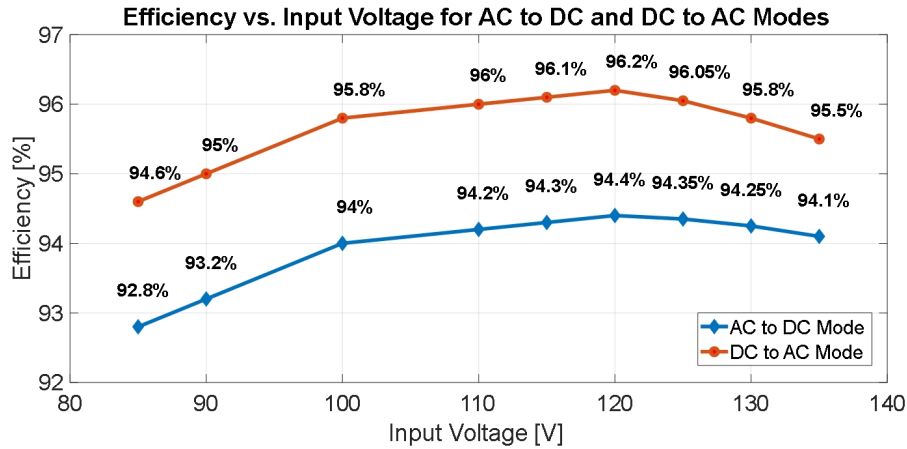


Figure 3.35: Efficiency Curve of the designed converter for different input voltages.

3.5.4 Comparison

Table 3.2 provides a comprehensive comparison of the designed converter with several state-of-the-art OBCs presented in the literature, highlighting key parameters such as the number of semiconductor devices, switching frequency, DC-link and filter capacitances, peak efficiency, and output voltage.

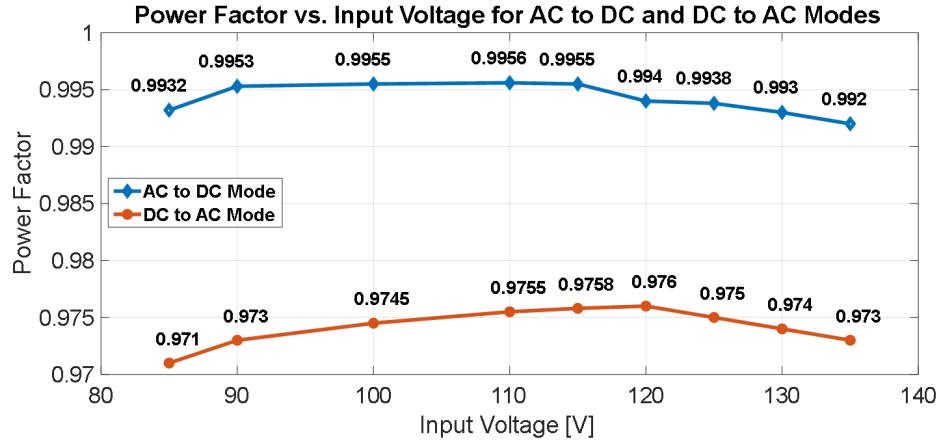


Figure 3.36: Power Factor Curve of the designed converter for different input voltages.



Figure 3.37: Harmonic distortion captured from the hardware experimental prototype

A standout feature of the designed design is the complete elimination of bulky electrolytic capacitors, which are commonly used in other designs but suffer from limited lifespan and larger volume. Instead, the designed converter uses $2 \times 25 \mu F$ film capacitors for both the DC-link and filter stages, significantly reducing size, cost, and reliability concerns. The converter achieves a peak ef-

efficiency of 96.2% and operates at a switching frequency range of 100–120 kHz, enabling reduced passive component sizes and enhanced power density. Moreover, due to the stack-switched-based design of the converter, the designed topology effectively reduces the voltage stress across individual switches, making it more suitable for high-voltage (HV) applications compared to the other designs. With support for an output voltage of up to 750 V, the converter is well-suited for modern HV EV applications, while minimizing the component count to just 10 switches and completely eliminating discrete diodes. This design strikes a balance between performance, compactness, and reliability, offering advantages over existing solutions.

Fig. 3.35 illustrates the measured efficiency for a range of input voltages for both AC to DC and DC to AC modes of operation. It can be observed that the maximum efficiency of 94.4% (96.2%) was achieved at $v_{in} = 120V_{rms}$ in AC to DC (DC to AC) mode. Moreover, Fig. 3.36 shows the measured power factor of the converter for a range of input voltages in both modes of operation. It can be observed that using the closed-loop duty ratio controller, the quality of the input current remains high for different input voltages. It is important to mention that switches S_8 and S_9 in Leg B in AC to DC mode (switches S_4 and S_5 in Leg A in DC to AC mode) are the primary contributors to the voltage ripple reduction, as their duty ratios D_s in AC to DC mode (D_p in DC to AC mode) are dynamically adjusted to control the gain curve and ensure effective ripple cancellation. This design aligns with the theoretical framework and experimental results presented in Sections V. While S_7 and S_{10} in AC to DC mode (S_4 and S_5 in DC to AC mode) were not utilized in the current design to maintain simplicity and adhere to the theoretical focus, they could potentially be employed as synchronous rectifiers to complement S_8 and S_9 (S_3 and S_6), reducing conduction losses and improving overall efficiency.

The detailed harmonic analysis, covering the first to the seventh harmonics, was obtained from the hardware prototype using the "Power Analysis Tool" of the KEYSIGHT MSOX6004A oscilloscope, as illustrated in Fig. 3.37 during DC to AC operation at $v_{in} = 120V_{rms}$. The THD was measured at 2.42%, and these harmonic values were compared with the IEC 61000-3-2 standard [92],

which specifies the maximum allowable harmonics for class A battery chargers (with input current ≤ 16 A). The results confirm that the developed PFC current controller successfully meets these stringent standards.

3.6 Chapter Summary

This chapter presented the design and implementation of a high-performance bidirectional single-phase AC/DC converter for EV charging systems capable of operating in both charging (G2V) and discharging (V2G) modes. The designed topology integrates a dual stacked-switch half-bridge PFC stage on the AC side and a CLLC resonant stage on the DC side to achieve galvanic isolation, soft-switching, and reduced voltage stress across the semiconductor devices. This architecture addresses critical challenges in conventional bidirectional converter designs, including excessive voltage stress, poor soft-switching capability, and the reliance on bulky electrolytic capacitors.

A comprehensive control system was developed to support bidirectional power flow with high power quality and ripple suppression. A dq-frame-based PFC controller was implemented to synchronize with the grid and ensure sinusoidal input/output current in both AC/DC and DC/AC modes. Furthermore, a secondary-side duty modulation control technique was introduced to reduce low-frequency output voltage ripple, enabling the use of compact and reliable film-type capacitors.

The designed topology and control framework were validated through detailed simulation and experimental testing on a 1 kW prototype. The results confirmed the converter's ability to operate with high efficiency, maintain unity power factor, achieve low THD, and perform soft-switching in both directions of power transfer. These outcomes demonstrate the feasibility of the designed system as a compact, efficient, and reliable bidirectional EV charger suitable for future grid-interactive mobility applications.

Table 3.2: Comparison with the State-of-the-Art EV OBCs

Paper	Number of Semiconductors		Switching Frequency	DC-link Capacitors	Filter Capacitors	Peak Efficiency	Output Voltage
	Switches	Diodes					
Shi <i>et al.</i> [54]	5	9	200kHz	$1 \times 2000\mu F$	$1 \times 10\mu F$	93.5%	100–420V
Nguyen <i>et al.</i> [55]	12	0	90–150kHz	$2 \times 50\mu F$	$1 \times 200\mu F$	96.1%	400V
Kwon <i>et al.</i> [73]	8	0	100kHz	$2 \times 100\mu F$	$1 \times 100\mu F$	95.7%	410V
Yuan <i>et al.</i> [74]	10	0	100kHz	$1 \times 2.5\mu F$	$1 \times 900\mu F$	95.3%	800V
Sharma <i>et al.</i> [75]	6	0	100kHz	$1 \times 12, 1 \times 10\mu F$	$1 \times 1100\mu F$	90.18%	250–410V
Designed Converter	10	0	100–120kHz	$2 \times 50\mu F$	$2 \times 25\mu F$	96.2%	750V

Chapter 4

Linear Matrix Inequality-Based Robust H_∞ AC-Grid-Forming Control System

4.1 Introduction

This chapter focuses on the design and implementation of a robust GFM control strategy for single-phase bidirectional AC/DC converters used in EV charging systems. As EVs evolve into active grid participants through V2G and V2H capabilities, the ability of onboard chargers to autonomously establish voltage and frequency references under islanded conditions becomes increasingly critical.

In the first part of this chapter, a comprehensive state-space model of the bidirectional AC/DC converter is developed, incorporating polytopic uncertainty to account for variations in grid parameters and system loading. This model serves as the foundation for robust controller synthesis.

The second part presents the design of an $\mathcal{H}_\infty$ controller using LMIs, ensuring robust voltage and frequency regulation across a range of operating conditions. Integral action is embedded in the control structure to eliminate steady-state error, while maintaining low THD and fast transient response.

In the final part of the chapter, the designed control strategy is implemented and validated experimentally. The performance of the controller is evaluated under dynamic loading, disturbances, and transition scenarios. The results demonstrate the controller's effectiveness in maintaining grid-forming

operation with high stability, low harmonic distortion, and reliable dynamic behavior, confirming its suitability for future EV grid-supportive infrastructures.

4.2 State-Space Dynamic Modeling

To enable robust control synthesis for the AC-GFM operation of the bidirectional OBC, a state-space model of the system is developed in the synchronous dq reference frame. This modeling approach transforms sinusoidal AC variables into DC quantities, greatly simplifying the analysis and control of the system. In particular, the dq transformation facilitates decoupling of active and reactive power control, enhances disturbance rejection, and allows for straightforward integration of integral action to eliminate steady-state error.

The modeling process begins by projecting the single-phase signals into the two-phase stationary $\alpha\beta$ frame using the Clarke transformation, followed by the Park transformation to convert the signals into the rotating dq frame. This methodology is consistent with the framework introduced in Chapter 3. The inverter is connected to the load through an LCL filter, and the state variables are defined as the filter inductor current i_f , the filter capacitor voltage v_{cf} , and the load current i_L as shown in Fig. 3.4. The load voltage v_L is treated as a disturbance to enable robustness against load changes and load side perturbations.

The resulting linear time-invariant (LTI) state-space model of the system in the dq frame is described by the following equations:

$$\begin{aligned}\dot{x}(t) &= Ax(t) + B_u u(t) + B_d d(t), \\ y(t) &= C_y x(t)\end{aligned}\tag{4.1}$$

where the state vector is defined as $x(t) = [i_{f,d}, i_{f,q}, i_{L,d}, i_{L,q}, v_{cf,d}, v_{cf,q}]^T$, the control input vector as $u(t) = [v_{inv,d}, v_{inv,q}]^T$, and the disturbance input as $d(t) = [v_{in,d}, v_{in,q}]^T$. The corresponding system matrices are presented at the bottom of this page.

$$\begin{aligned}
A &= \begin{bmatrix} -\frac{R_f}{L_f} & \omega_g & 0 & 0 & -\frac{1}{L_f} & 0 \\ -\omega_g & -\frac{R_f}{L_f} & 0 & 0 & 0 & \frac{1}{L_f} \\ 0 & 0 & -\frac{R_{in}}{L_{in}} & \omega_g & \frac{1}{L_{in}} & 0 \\ 0 & 0 & -\omega_g & -\frac{R_{in}}{L_{in}} & 0 & \frac{1}{L_{in}} \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 & 0 & \omega_g \\ 0 & \frac{1}{C_f} & 0 & -\frac{1}{C_f} & -\omega_g & 0 \end{bmatrix}, \\
B_u &= \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & \frac{1}{L_f} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad B_d = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{L_{in}} & 0 \\ 0 & \frac{1}{L_{in}} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \\
C_y &= \begin{bmatrix} 0 & 0 & R_{in} + \omega_g L_{in} & 0 & 1 & 0 \\ 0 & 0 & 0 & R_{in} + \omega_g L_{in} & 0 & 1 \end{bmatrix}.
\end{aligned} \tag{4.2}$$

The matrix A captures the dynamics of the LCL filter and rotating reference frame through ω_g , while B_u relates to inverter control inputs and B_d models the effect of load-side voltage disturbances. The output matrix C selects the capacitor voltages $v_{cf,d}$ and $v_{cf,q}$ as the controlled outputs, which serve as the grid-forming reference voltages.

4.2.1 Integral Augmentation for Zero Steady-State Error

To ensure zero steady-state error in tracking the reference voltage during GFM operation, the system is augmented with integral action. This augmentation is particularly important in AC-GFM control, where accurate voltage regulation is critical for maintaining power quality and load stability in V2H applications.

To ensure zero steady-state error in regulating the output voltage during V2H operation, the system is augmented with integrator states that track the error between the load voltage and its reference. Based on the corrected output model, the error dynamics are defined as:

$$\dot{v}(t) = v_{ref,dq}(t) - C_y x(t), \tag{4.3}$$

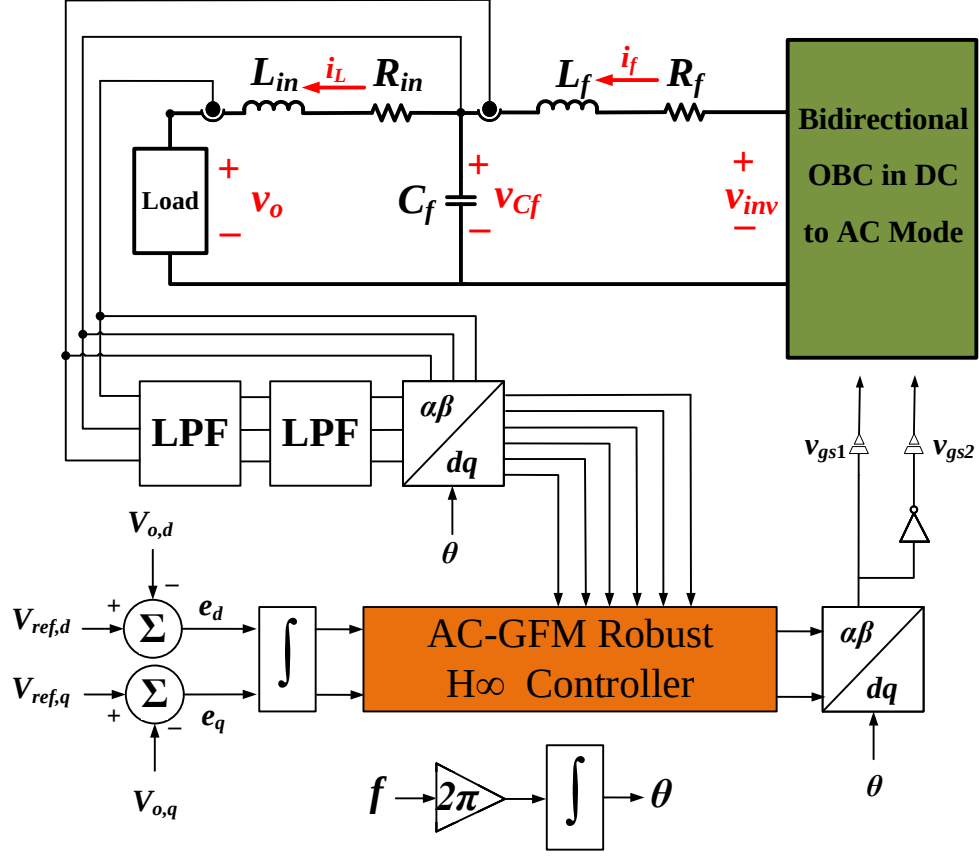


Figure 4.1: Block diagram of the designed AC-GFM controller for an OBC connected to unknown load through LCL filter.

where $\vartheta(t)$ denotes the integrator states. As a result, the augmented state vector becomes:

$$\hat{x}(t) = \begin{bmatrix} x(t) \\ \vartheta(t) \end{bmatrix} \quad (4.4)$$

and the augmented system dynamics are given by:

$$\begin{aligned} \dot{\hat{x}}(t) &= \hat{A}\hat{x}(t) + \hat{B}_u u(t) + \hat{B}_d \hat{d}(t), \\ \hat{y}(t) &= \hat{C}_y \hat{x}(t) \end{aligned} \quad (4.5)$$

with the augmented system matrices defined as:

$$\begin{aligned} \hat{A} &= \begin{bmatrix} A & \mathbf{0}_{6 \times 2} \\ -C_y & \mathbf{0}_{2 \times 2} \end{bmatrix}, \quad \hat{B}_u = \begin{bmatrix} B_u \\ \mathbf{0}_{2 \times 2} \end{bmatrix}, \\ \hat{B}_d &= \begin{bmatrix} B_d & \mathbf{0}_{6 \times 2} \\ \mathbf{0}_{2 \times 2} & I_2 \end{bmatrix}, \quad \hat{C}_y = \begin{bmatrix} C_y & \mathbf{0}_{2 \times 2} \\ \mathbf{0}_{2 \times 6} & I_2 \end{bmatrix} \end{aligned} \quad (4.6)$$

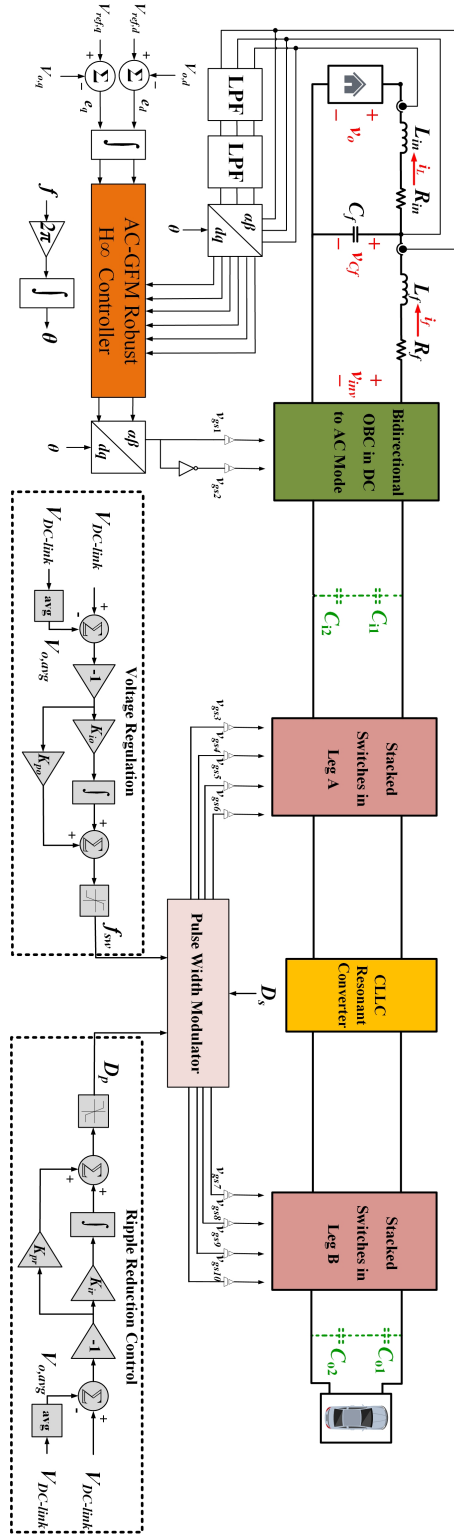


Figure 4.2: Unified Block diagram of all the controllers implemented in the OBC in Chapter 3 during V2H operation.

where $\hat{x}(t) = [x(t), \vartheta_d(t), \vartheta_q(t)]^T$ is the integrator state vector, $u(t) = [v_{inv,d}, v_{inv,q}]^T$ is the control input, $\hat{d}(t) = [d(t), v_{ref,d}(t), v_{ref,q}(t)]^T$ is the disturbance input, and $\hat{y}(t) = [y(t), \vartheta_d(t), \vartheta_q(t)]^T$ is the regulated output voltage at the load terminals.

This augmented model serves as the basis for robust state-feedback controller synthesis, ensuring both transient performance and zero steady-state error in the face of disturbances and uncertainties.

4.2.2 Polytopic Uncertainty Modeling

To ensure robust stability and performance under parameter deviations, the AC-GFM system is modeled using a polytopic uncertainty framework. This approach enables the representation of uncertain system matrices as convex combinations of vertex matrices, each corresponding to boundary values of the uncertain parameters.

In this study, the uncertainty arises from variations in the load-side inductance L_{in} and resistance R_{in} , which are subject to change due to fluctuating load conditions or environmental factors. These parameters significantly affect the dynamic behavior of the system and must therefore be explicitly considered during controller design.

Specifically, the variations in $L_{in} \in [L_{in}^{\min}, L_{in}^{\max}]$ and $R_{in} \in [R_{in}^{\min}, R_{in}^{\max}]$ propagate through multiple matrices in the model, including the state matrix A , the disturbance input matrix B_d , and the output matrix C_y . As a result, their augmented counterparts, $\hat{A}$, $\hat{B}_d$, and $\hat{C}_y$, also inherit this uncertainty and are treated accordingly within the polytopic structure.

All possible realizations of the uncertain polytopic matrix lie within a convex hull. This convex hull represents the smallest convex set that encompasses every admissible configuration of the matrix under parameter variation. For a system matrix affected by n independent uncertain parameters, the convex hull is defined by 2^n vertex matrices, each corresponding to an extreme combination of the parameter bounds. The uncertain matrix can then be expressed as a convex combination of these vertices, as shown below for a given matrix E :

$$\begin{aligned}
E(q_1, q_2, \dots, q_n) &\in \text{conv} \{E^v\}, \\
E(q_1, q_2, \dots, q_n) &= \sum_{v=1}^{2^n} \lambda_v E^v, \\
\sum_{v=1}^{2^n} \lambda_v &= 1, \quad \lambda_v \geq 0
\end{aligned} \tag{4.7}$$

where E^v represents the vertex matrix associated with the v^{th} combination of parameter extremes, and n denotes the number of uncertain parameters.

Similarly, for matrices $\hat{A}$, $\hat{B}_d$, and $\hat{C}_y$, we have:

$$\begin{aligned}
\hat{A}(q_1, q_2) &= \sum_{v=1}^4 \lambda_1^v \hat{A}^{(v)}, \\
\hat{B}_d(q_3) &= \sum_{v=1}^2 \lambda_2^v \hat{B}_d^{(v)}, \\
\hat{C}_y(q_4) &= \sum_{v=1}^2 \lambda_3^v \hat{C}_y^{(v)},
\end{aligned} \tag{4.8}$$

where $q_1 = 1/L_{in}$, $q_2 = R_{in}/L_{in}$, $q_3 = -1/L_{in}$, $q_4 = R_{in} + L_{in}$. As a result, the augmented matrices $\hat{A}$, $\hat{B}_d$, and $\hat{C}_y$ have a permissible range of changes within a defined bounded range, described as follows:

$$\begin{cases} q_1^{\min} \leq q_1 \leq q_1^{\max}, \\ q_2^{\min} \leq q_2 \leq q_2^{\max}, \\ q_3^{\min} \leq q_3 \leq q_3^{\max}, \\ q_4^{\min} \leq q_4 \leq q_4^{\max} \end{cases} \tag{4.9}$$

Accordingly, the vertices of the uncertain augmented matrices $\hat{A}$, $\hat{B}_d$, and $\hat{C}_y$ corresponding to the extreme combinations of uncertainties can be given as below:

$$\begin{aligned}
\hat{A}^{(1)} &= \hat{A}(q_1^{\min}, q_2^{\min}), \quad \hat{A}^{(2)} = \hat{A}(q_1^{\min}, q_2^{\max}), \\
\hat{A}^{(3)} &= \hat{A}(q_1^{\max}, q_2^{\min}), \quad \hat{A}^{(4)} = \hat{A}(q_1^{\max}, q_2^{\max})
\end{aligned} \tag{4.10}$$

$$\hat{B}_d^{(1)} = \hat{B}_d(q_3^{\min}), \quad \hat{B}_d^{(2)} = \hat{B}_d(q_3^{\max}), \tag{4.11}$$

$$\hat{C}_y^{(1)} = \hat{C}_y(q_4^{\min}), \quad \hat{C}_y^{(2)} = \hat{C}_y(q_4^{\max}), \tag{4.12}$$

$$\begin{bmatrix} W^{(i,j)} + \bar{A}^\nu X + X(\bar{A}^\nu)^T + Z^T \bar{B}_u^{\nu^T} + \bar{B}_u^\nu Z & * & * \\ \xi X(\bar{A}^\nu)^T + \xi Z^T \bar{B}_u^\nu & -W^{(i,j)} - \xi \bar{A}^\nu X - \xi \bar{B}_u^\nu Z - \xi Z^T (\bar{A}^\nu)^T - \xi Z^T \bar{B}_u^{\nu^T} & * \\ \bar{B}_d^\nu & -\bar{B}_d^\nu & -I \\ C_z X + D_z Z & \xi C_z X + \xi D_z Z & D_d \quad -\gamma I \end{bmatrix} < 0 \quad (4.13)$$

This structure allows the use of LMI-based robust control synthesis over the entire range of uncertainties by ensuring the closed-loop performance and stability at all vertex cases. Since the polytopic model includes all possible variations of the uncertain parameters, the controller designed over this set guarantees robust performance for all admissible values of R_{in} and L_{in} .

4.3 Robust H_∞ GFM Controller Design

To achieve robust voltage regulation and stability in the presence of load-side disturbances and parameter uncertainties, a state-feedback control strategy is developed based on the H_∞ optimization framework. The designed controller operates under the control law $u(t) = K_s \hat{x}(t)$, where K_s is the state feedback gain matrix to be synthesized.

The first step in the controller synthesis process is to derive the closed-loop representation of the uncertain system. By substituting the control input $u(t) = K_s \hat{x}(t)$ into the state-space model of the augmented system in (4.5), the resulting closed-loop dynamics of the augmented system can be expressed as:

$$\begin{aligned} \dot{\hat{x}}(t) &= \left(\hat{A}(\lambda_1) + \hat{B}_u K_s \right) \hat{x}(t) + \hat{B}_d(\lambda_2) \hat{d}(t), \\ \hat{y}(t) &= \hat{C}_y(\lambda_3) \hat{x}(t), \\ z(t) &= (C_z + D_z K_s) \hat{x}(t) + D_d \hat{d}(t), \end{aligned} \quad (4.14)$$

where $\hat{x}(t)$, $\hat{d}(t)$, and $z(t)$ are the state, disturbance, and controlled output vectors of the augmented system respectively, and the matrices $\hat{A}$, $\hat{B}_u$, $\hat{B}_d$, and $\hat{C}_y$ follow the definitions provided in the section II.C. The controlled output vector $z(t)$ is considered to include error and control input vectors to make

sure the disturbances have minimum effect on these vectors. This closed-loop model forms the foundation for formulating the robust H_∞ control problem and deriving appropriate LMI conditions to ensure system performance and stability across all admissible uncertainty realizations.

To guarantee closed-loop stability and ensure that the induced H_∞ norm from disturbance $d(t)$ to controlled output $z(t)$ is less than a prescribed performance level γ , the following theorem provides a sufficient condition:

Theorem 1. *Assume scalar parameters $\epsilon > 0$, $\xi \in (-1, 1)$, and $\gamma > 0$. For each vertex realization v of the uncertain system, suppose there exist matrices $W^{(i,j)} = (W^{(i,j)})^T > 0$, $X = X^T > 0 \in R^{n_x \times n_x}$, and $Z \in R^{n_u \times n_x}$ such that the LMI (4.13) shown at the top of the page holds, where the transformed matrices are defined as:*

$$\begin{aligned}\tilde{A}^v &= \epsilon A^v - I, \\ \bar{B}_d^v &= \epsilon B_d^v, \\ \bar{B}_u^v &= \epsilon B_u.\end{aligned}$$

Then, the state feedback gain

$$K_s = ZX^{-1} \tag{4.15}$$

ensures that the closed-loop system is quadratically stable with an H_∞ guaranteed cost less than $\sqrt{\gamma}$ for all admissible uncertainties in the polytopic set $(\left\| \frac{z}{d} \right\|_\infty = \sqrt{\gamma})$ [93].

Remark. In cases where the system matrices such as $\hat{A}^v$, $\hat{B}_d^v$, or $\hat{B}_u^v$ have different numbers of polytopic vertices, the overall uncertainty must be represented using the *Cartesian product* of these vertex sets. This results in a total of $4 \times 2 = 8$ combined vertex combinations for the uncertain closed-loop system. To ensure robust $\mathcal{H}_\infty$ performance under all admissible combinations, the LMIs in Theorem 1 must be enforced for *each* of these 8 vertex pairs. That is, a separate Lyapunov matrix $W^{(ij)} \succ 0$ is used for each combination (i, j) , where $i \in \{1, 2, 3, 4\}$, $j \in \{1, 2\}$. This approach guarantees that the controller

is robust with respect to the full range of structured uncertainty across all system matrices.

The robust controller design follows a systematic three-step procedure:

1. **Step 1: Vertex Construction.** Construct the vertex matrices of the uncertain system $\hat{A}^v$, $\hat{B}_d^v$, and $\hat{C}_y^v$, corresponding to the extreme values of the uncertain parameters R_{in} and L_{in} , as detailed in the polytopic uncertainty modeling section.
2. **Step 2: LMI-Based Synthesis.** Solve the convex optimization problem defined by the LMI in (4.13) for each vertex v , using chosen scalars $\epsilon > 0$, $\xi \in (-1, 1)$, and $\gamma > 0$, to find feasible matrices X and Z . This step ensures that the closed-loop system meets robust stability and performance requirements across the full uncertainty range.
3. **Step 3: Gain Extraction.** Compute the final controller gain $K_s = ZX^{-1}$. This gain guarantees minimized steady-state error, optimal transient response, and robust voltage regulation under V2H operation.

4.4 Experimental Validation

To experimentally validate the performance of the designed robust H_∞ AC-GFM control strategy for V2H operation, a proof-of-concept hardware prototype of the electrolytic capacitor-less bidirectional AC/DC converter was developed and tested under laboratory conditions. The prototype is rated for 1 kW, with input/output specifications of 120 V_{rms}/750 V_{dc}, and operates within a 90–120 kHz switching frequency range using SiC-based semiconductor devices. The PLECS RT Box 1 platform was used to implement the real-time performance of the designed AC-GFM controller. A photograph of the assembled prototype is shown in Fig. 4.3, and the key system specifications and electrical parameters are summarized in Table 4.1.

Fig. 4.4 shows the experimentally measured steady-state waveforms of the load voltage v_L and load current i_L when the converter operates in the DC-to-

Table 4.1: Parameter Values of the Designed Prototype

Parameters	Values
Rated Power (P_o)	$1kW$
DC-Side Voltage (V_{DC})	$750V_{dc}$
Load Voltage (v_L)	$120V_{ac,rms}$
Leg A and B Switching Frequency (f_{sw})	$\geq 100kHz$
HB Switching Frequency (f_{hb})	$70kHz$
Load-Side Filter Inductance (L_{in})	$550\mu H$
Load-Side Filter Capacitance (C_f)	$0.8\mu F$
Inverter-Side Filter Inductance (L_f)	$170\mu H$
DC-link Capacitances (C_{i1}, C_{i2})	$50\mu F$
Primary Resonant Capacitance (C_p)	$0.068\mu F$
Secondary Resonant Capacitance (C_s)	$0.68\mu F$
Resonant Inductance (L_r)	$260\mu H$
Magnetizing Inductance (L_m)	$270\mu H$
Output Filter Capacitances (C_{o1}, C_{o2})	$25\mu F$
Switches ($S_1 - S_2$)	IMW120R020M1HXKSA1
Switches ($S_3 - S_{10}$)	IMW65R030M1HXKSA1

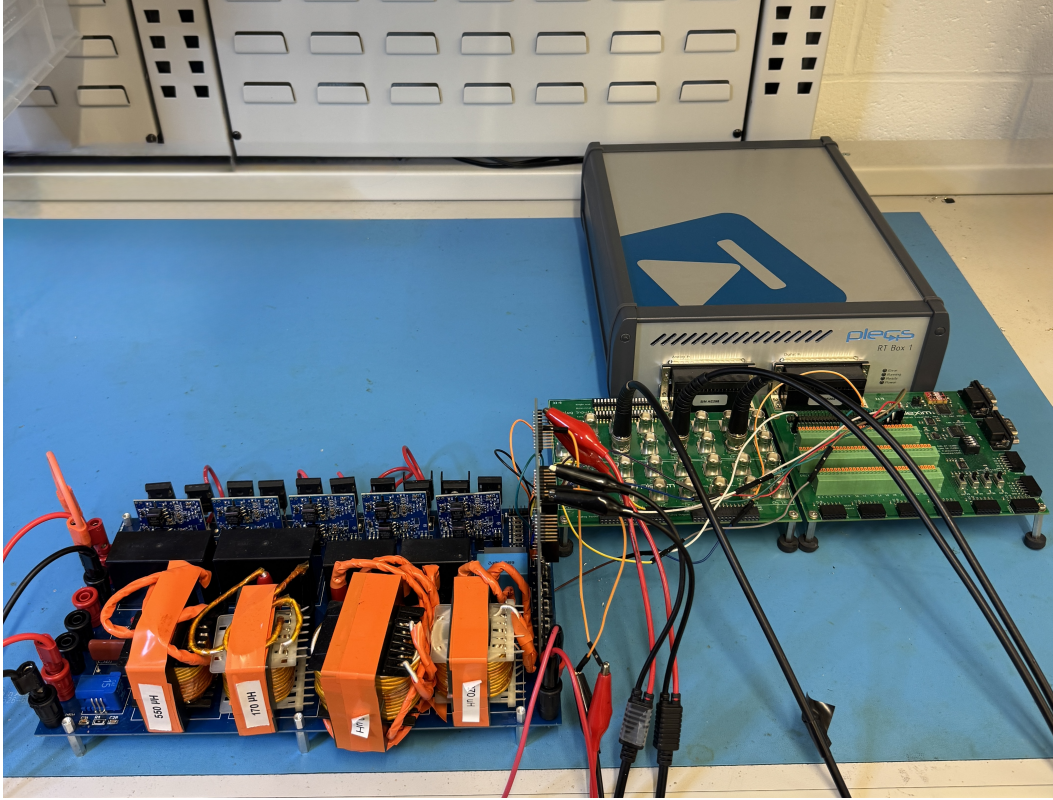


Figure 4.3: Picture of the Proof-of-concept prototype.

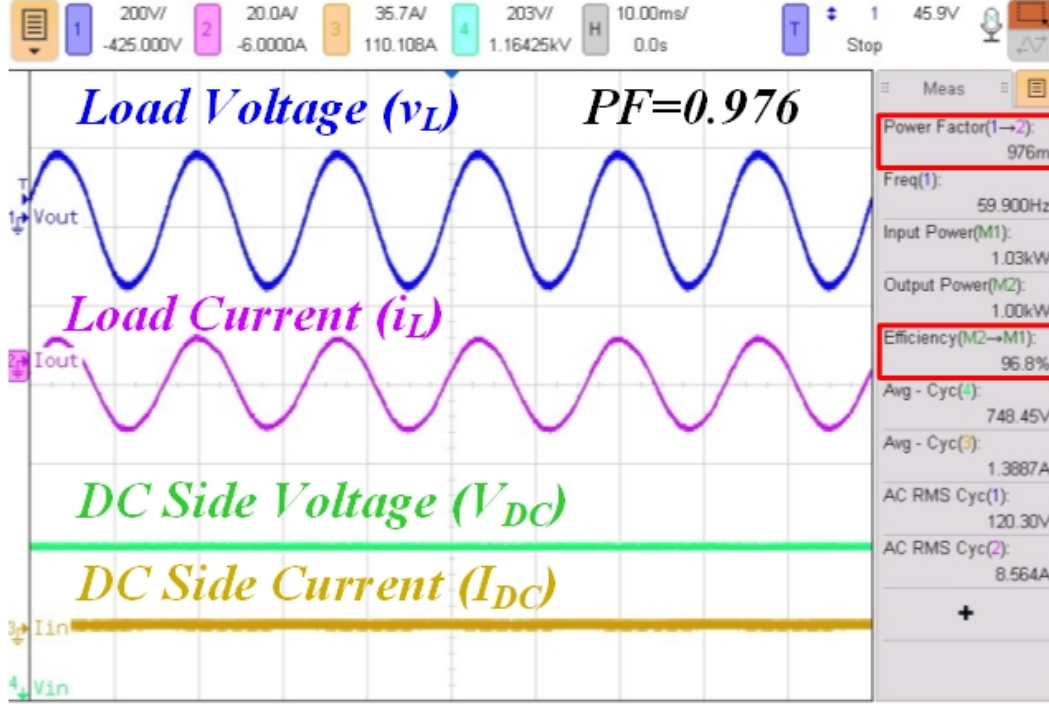


Figure 4.4: Input and Output waveforms of the converter at rated power in DC to AC mode with AC-GFM controller.

AC (V2H) mode at full load. The output voltage waveform exhibits a near-perfect sinusoidal shape with an RMS amplitude of approximately $120 V_{\text{rms}}$, indicating high-quality voltage synthesis. The output current i_L is also sinusoidal and closely aligned in phase with the output voltage, resulting in a measured power factor of 0.976.

This result verifies the effectiveness of the designed AC-GFM controller in providing tight voltage regulation, minimal harmonic distortion, and accurate synchronization with the load. The converter delivers a measured output power of 1.00 kW, confirming the system's ability to maintain stable and high-performance operation under nominal V2H conditions.

To validate the soft-switching behavior of the designed bidirectional AC-GFM converter under the robust control framework, the experimental waveforms of switch S_1 are captured and shown in Figs. 4.5–4.7. While detailed operation and soft-switching performance of all half-bridge switches (such as S_1 – S_2 , S_3 – S_6 , S_4 – S_5 , and S_8 – S_9) are presented in Chapter 3, this section focuses on the performance of switch S_1 to confirm that, even under the designed

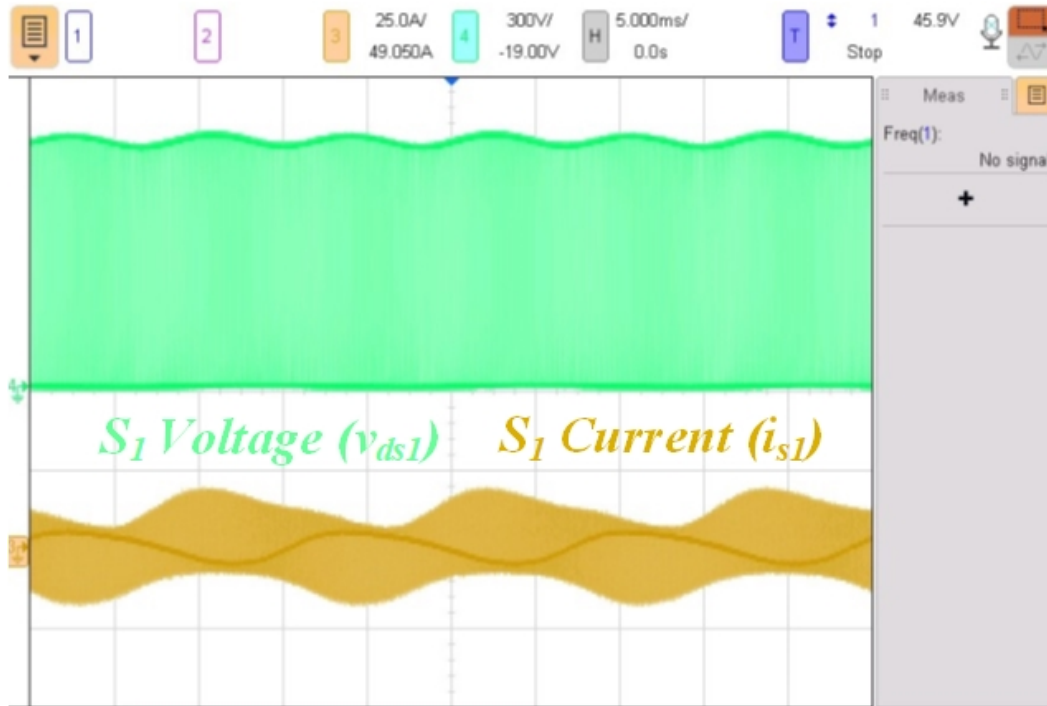


Figure 4.5: Experimental voltage and current waveforms of switch S_1 at line frequency, confirming ZVS behavior.

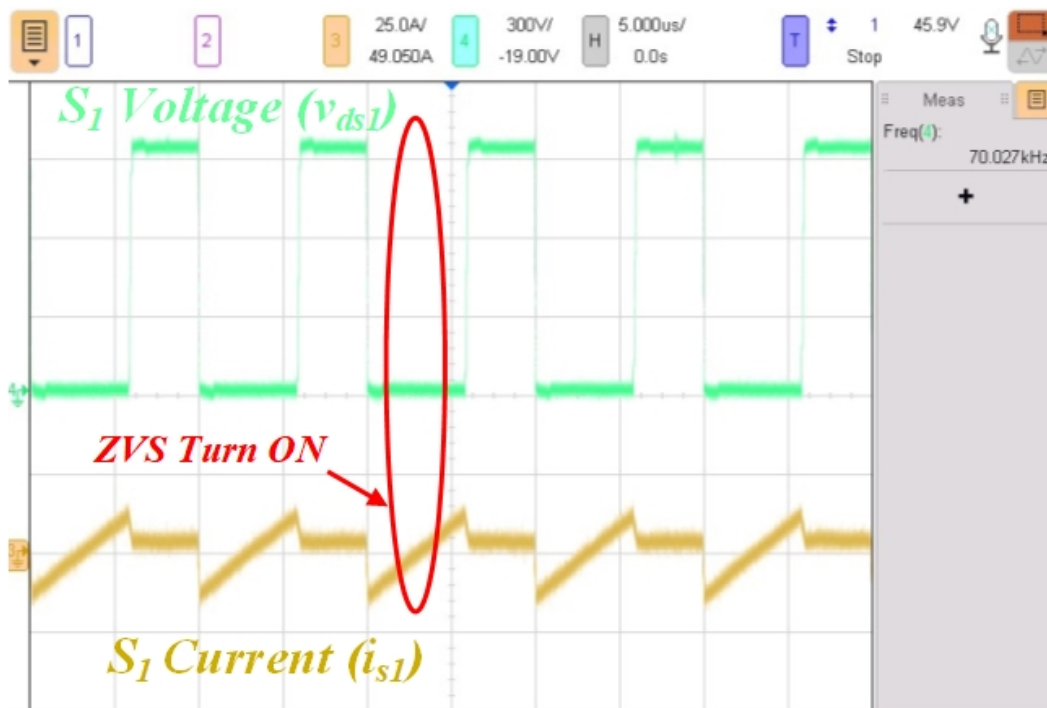


Figure 4.6: Switch S_1 waveforms at switching frequency showing ZVS turn-on during high-frequency operation (case 1).

AC-GFM robust controller, soft-switching is maintained. Due to the symmetrical behavior of switches S_1 and S_2 , only the results for S_1 are shown for brevity.

Fig. 4.5 illustrates the voltage (v_{ds1}) and current (i_{s1}) waveforms of switch S_1 at the line frequency. It can be observed that S_1 transitions at zero voltage, confirming successful ZVS operation during both positive and negative line cycles. This ZVS performance is essential for reducing switching losses and ensuring thermal efficiency.

Figs. 4.6 and 4.7 show the high-frequency switching behavior of switch S_1 at approximately 70 kHz. The voltage waveform clearly drops to zero just before the switch turns ON, while the current builds up afterwards, confirming ZVS turn-on events. The sinusoidal nature of the switch current further confirms the resonant operation of the converter. These results collectively verify that the half-bridge switch S_1 maintains full soft-switching functionality even under closed-loop robust AC-GFM operation.



Figure 4.7: Switch S_1 waveforms at switching frequency showing ZVS turn-on during high-frequency operation (case 2).

To experimentally validate the robustness of the designed AC-GFM con-

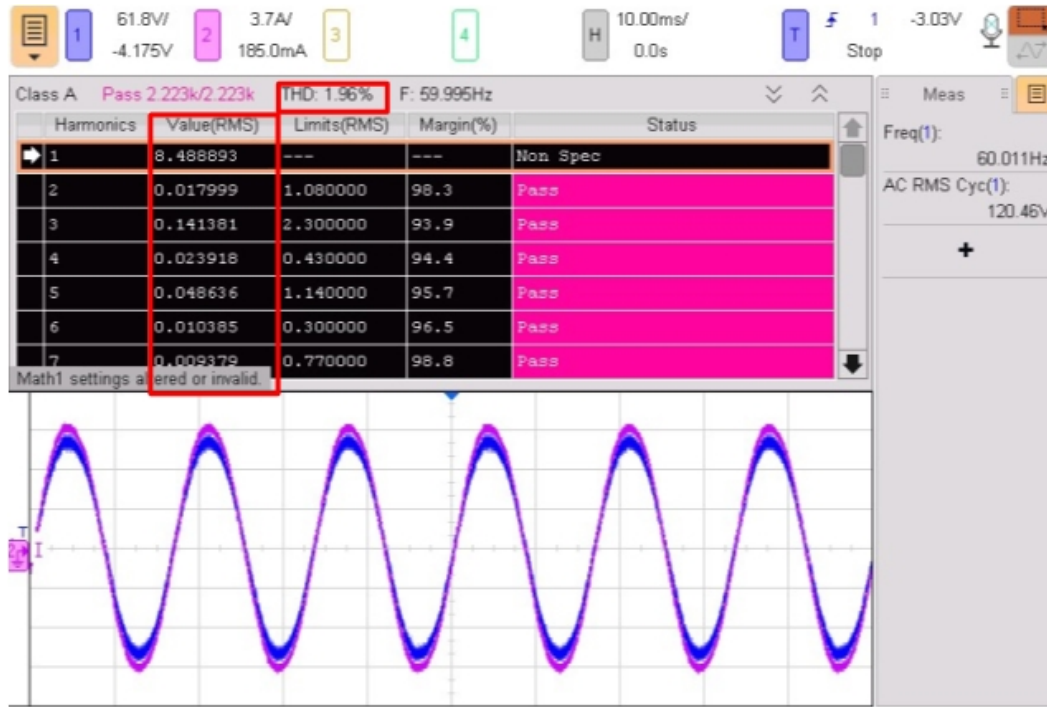


Figure 4.8: Experimental THD and output voltage waveform for $L_{in} = 350 \mu\text{H}$, showing 1.96% THD.



Figure 4.9: Experimental THD and output voltage waveform for nominal case $L_{in} = 550 \mu\text{H}$, showing 2.20% THD.



Figure 4.10: Experimental THD and output voltage waveform for $L_{in} = 1$ mH, showing 2.94% THD.

troller against variations in the load-side inductance, three different inductance values were tested: $350 \mu\text{H}$, $550 \mu\text{H}$ (nominal), and 1 mH. The corresponding output voltage waveforms and harmonic distortion measurements are shown in Figs. 4.8–4.10. The detailed harmonic analysis, covering the first to the seventh harmonics, was obtained from the hardware prototype using the "Power Analysis Tool" of the KEYSIGHT MSOX6004A oscilloscope. These results highlight the controller's capability to maintain acceptable output voltage quality and low harmonic distortion despite significant plant uncertainties.

Fig. 4.8 presents the experimental results for $L_{in} = 350 \mu\text{H}$, where the total harmonic distortion (THD) is measured to be 1.96%. This result demonstrates excellent voltage quality even when the inductance is smaller than the nominal value, reflecting the fast dynamic response enabled by the controller.

In the nominal case shown in Fig. 4.9, with $L_{in} = 550 \mu\text{H}$, the THD slightly increases to 2.20%, remaining well within the acceptable Class A limits. This confirms the controller's baseline performance and optimal design under nominal parameters.

As the inductance is further increased to $L_{in} = 1$ mH, the results in Fig. 4.10 show a THD of 2.94%. Although the harmonic content increases slightly due to slower current dynamics associated with higher inductance, the output voltage remains sinusoidal and the THD still satisfies international standards.

Notably, all measured THD values comply with the Class A requirements specified in IEC 61000-3-2:2018 [92], which limits harmonic current emissions for equipment with input current ≤ 16 A per phase. This compliance further affirms the suitability of the designed AC-GFM controller for practical applications with varying load-side conditions.

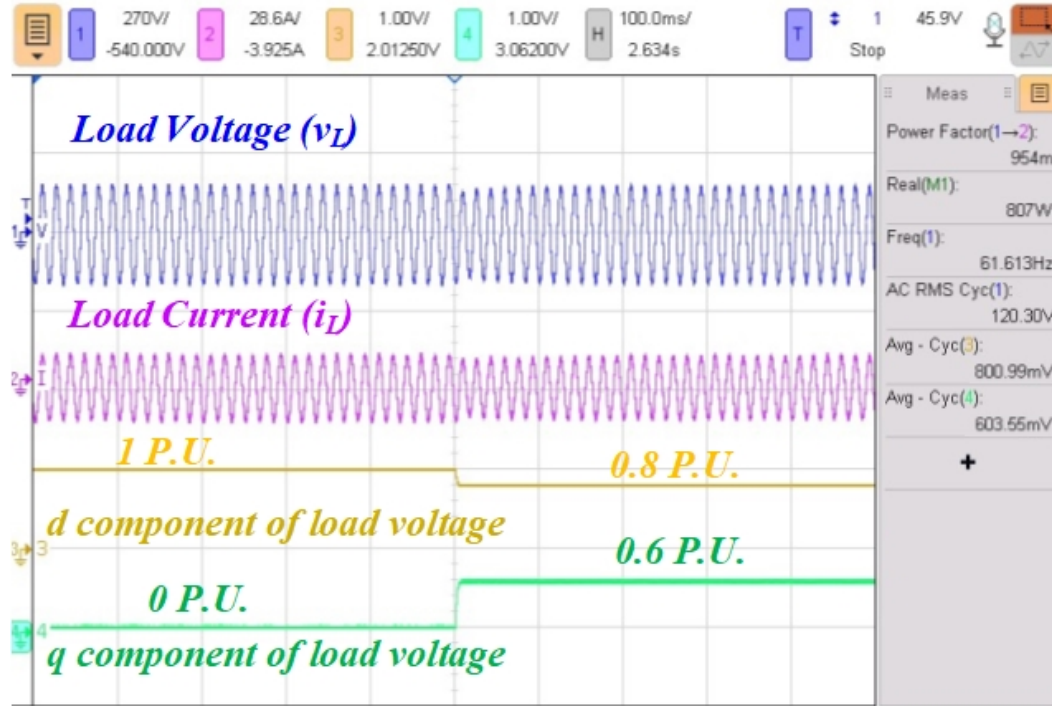


Figure 4.11: Experimental validation of dq reference tracking performance. The d - and q -axis voltage references are changed from (1.0, 0.0) p.u. to (0.8, 0.6) p.u..

To demonstrate the effectiveness of the designed robust AC-GFM controller in tracking time-varying dq -frame voltage references and its impact on active power injection, Fig. 4.11 shows the experimental waveforms of the load voltage, load current, and the applied d - and q -axis reference setpoints. Initially, the voltage reference is set to $v_{ref,d} = 1.0$ p.u. and $v_{ref,q} = 0.0$ p.u., correspond-

ing to the conventional scenario where the output voltage is fully aligned with the d -axis. At this operating point, the system injects approximately 1 kW of active power into the grid with negligible reactive power, as evidenced by the high power factor.

At $t = 2.6$ s, the voltage reference is changed to $v_{ref,d} = 0.8$ p.u. and $v_{ref,q} = 0.6$ p.u.. Despite the change in phase and magnitude of the voltage reference, the controller successfully regulates the output voltage to follow the new dq setpoints, as shown by the transitions in the yellow and green channels. Importantly, the load current remains sinusoidal, confirming that the converter continues to supply a clean output waveform.

As expected, the active power measured on the oscilloscope decreases to ≈ 800 W due to the reduction in the d -axis voltage component. This validates the theoretical prediction that active power is directly proportional to v_d when the current vector remains aligned with the d -axis. The system maintains stable operation and high voltage quality despite the change in power setpoints, confirming the capability of the designed controller in dynamically regulating voltage vectors under varying operating conditions.

To further evaluate the effectiveness of the designed robust AC-GFM controller under varying load conditions, Fig. 4.12 and Fig. 4.13 present experimental results for two different power levels: 750 W and 850 W. These tests were conducted to assess the controller's ability to maintain voltage regulation and waveform quality against different load power demand by changing the load value.

Fig. 4.12 illustrates the output voltage and current waveforms when the load draws approximately 750 W. The load current remains sinusoidal and well-aligned with the output voltage, resulting in a high power factor of 0.990. The RMS output voltage is measured to be 120.32 V, indicating tight voltage regulation despite the moderate load.

In Fig. 4.13, the load is increased to approximately 850 W. Despite the higher power transfer, the AC-GFM controller continues to regulate the voltage effectively, maintaining an RMS output voltage of 120.59 V. The power factor remains high at 0.962, and the current waveform continues to exhibit low

distortion and proper phase alignment with the voltage.

These results confirm that the designed robust controller ensures stable operation and consistent voltage regulation across different load levels. The controller dynamically adjusts the internal voltage generation to meet varying power demands while preserving output waveform quality and minimizing phase shift, validating its suitability for real-world Vehicle-to-Home (V2H) applications.

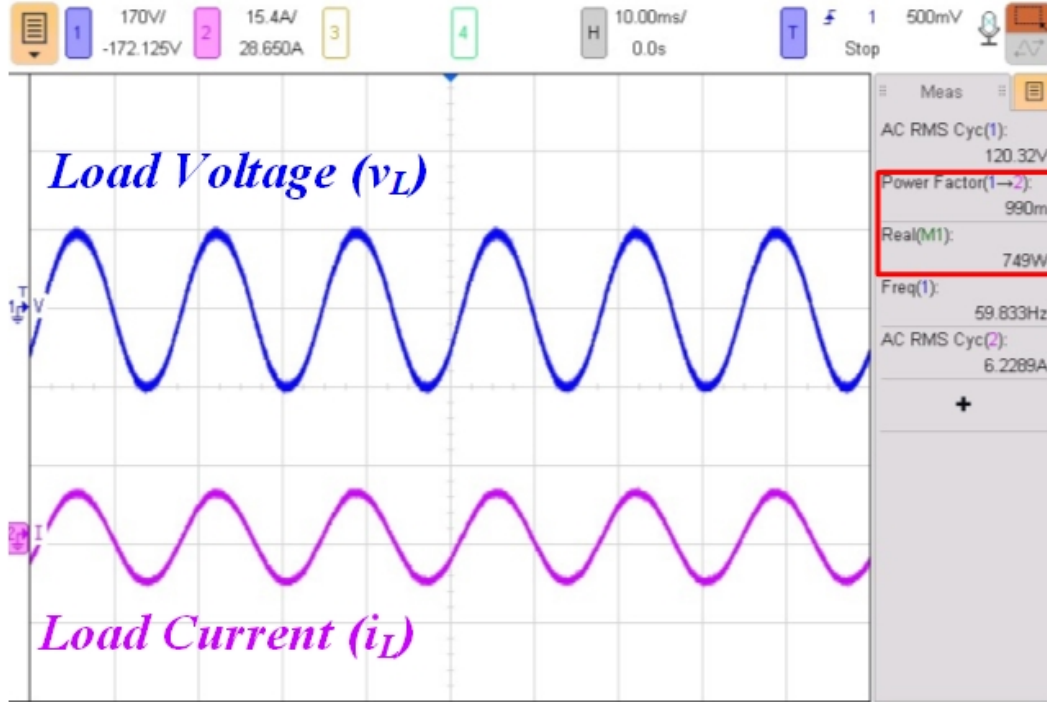


Figure 4.12: Experimental load voltage and current waveforms at 750 W load.

To validate the transient performance and robustness of the designed AC-GFM controller under dynamic loading conditions, Fig. 4.14 presents the experimental results where the load was suddenly changed during operation. The waveforms display the load voltage v_L and current i_L responses during the disturbance event. Initially, the system is operating under steady-state conditions with a constant load. Then, the load is abruptly changed, which introduces a step disturbance in the system's power demand.

As shown in the figure, the controller responds promptly to the load change, effectively regulating the output voltage. Despite the transient disturbance,

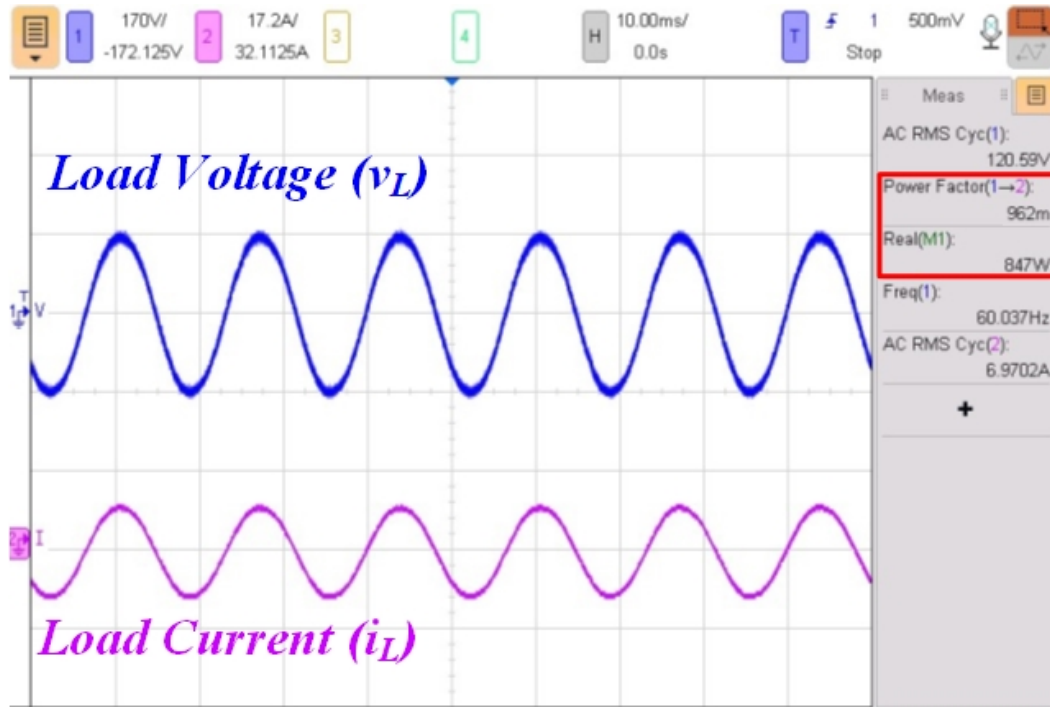


Figure 4.13: Experimental load voltage and current waveforms at 850 W load.

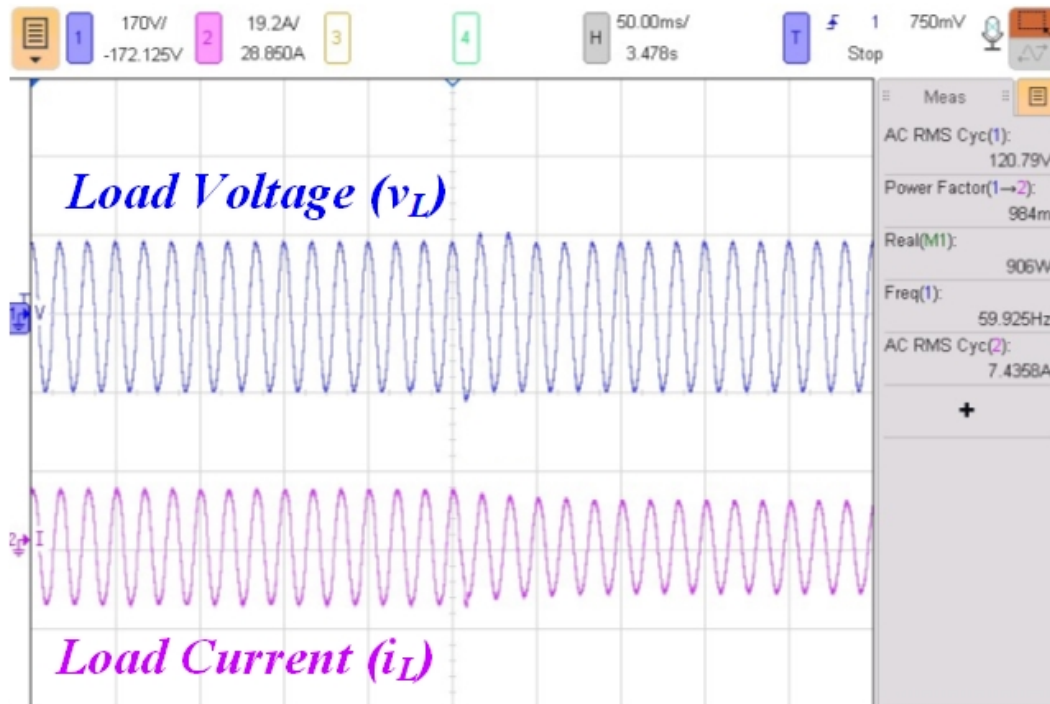


Figure 4.14: Experimental dynamic response under load change.

the RMS output voltage remains tightly controlled at approximately 120.79 V with no significant overshoot or undershoot. The voltage waveform maintains

sinusoidal shape throughout the event, and the recovery to steady state occurs within approximately 1.5 cycles (i.e., ~ 25 ms), indicating fast settling time.

Furthermore, the measured power factor of 0.984 and the active power of 906 W confirm that the controller successfully regulated the load voltage at its reference value. These results demonstrate the disturbance rejection, stability, and voltage regulation performance of the designed robust H_∞ -based controller in practical V2H scenarios involving load changes.

4.5 Chapter Summary

This chapter presented the development and experimental validation of a robust GFM control strategy for bidirectional single-phase AC/DC converters in EV applications. The designed control framework enables stable operation of the converter under weak-grid and islanded conditions, transforming the EV charger into an active voltage and frequency source suitable for V2G and V2H scenarios.

To address the challenges associated with uncertain grid parameters and load disturbances, a polytopic state-space model of the bidirectional converter was developed to capture system variability. An $\mathcal{H}_\infty$ controller was then synthesized using LMIs to guarantee robust stability and performance across a range of operating conditions. Integral augmentation was incorporated into the controller design to eliminate steady-state errors in voltage and frequency tracking.

The designed GFM controller was implemented in a hardware testbed and evaluated under various dynamic loading and grid disturbance scenarios. Experimental results confirmed the controller's ability to maintain voltage and frequency regulation, suppress THD, and ensure fast dynamic response. These findings validate the practicality and reliability of the control approach for grid-supportive EV charging applications.

By enabling resilient, autonomous operation and enhancing grid interactivity, the designed GFM control strategy represents a significant step toward the realization of intelligent, bidirectional, and capacitor-less EV chargers that

can actively participate in modern smart grid infrastructures.

Chapter 5

Conclusion and Future Work

This dissertation explored the design, control, and experimental validation of advanced single-phase AC/DC power converters for EV charging systems, with emphasis on eliminating electrolytic capacitors, enabling bidirectional operation, and ensuring robust grid interactivity. Motivated by the growing need for compact, efficient, and reliable on-board chargers, the work proposed innovative converter architectures and control strategies to address key challenges related to power factor correction, voltage ripple suppression, soft-switching, and operation under uncertain grid conditions.

The research was structured into three core areas: the development of a unidirectional bridgeless converter topology with minimal storage capacitance; the extension of this topology to a bidirectional, grid-interactive architecture; and the implementation of a robust $\mathcal{H}_\infty$ grid-forming control strategy suitable for islanded environments. All proposed solutions were validated through hardware prototypes and experimental testing, demonstrating the feasibility of high-performance, electrolytic capacitor-less EV chargers that meet modern efficiency and reliability requirements.

5.1 Contributions

- **Unidirectional Converter Design:** Developed a bridgeless, stacked-switch AC/DC converter operating in DCM with high power factor and low THD. A variable-frequency control system and ripple reduction strategy enabled elimination of electrolytic capacitors, validated on a 1.1 kW

prototype.

- **Bidirectional Capacitor-Less Architecture:** Proposed a bidirectional converter with dual-stacked switches and a CLLC resonant stage for galvanic isolation and soft-switching. Integrated dq-based PFC and active ripple reduction control for G2V/V2G operation, verified through hardware testing.
- **Robust Grid-Forming Control:** Designed an $\mathcal{H}_\infty$ -based controller using LMIs for stable and robust voltage regulation under uncertain and islanded conditions. The controller demonstrated low THD and fast dynamic response in V2H scenarios.
- **Electrolytic-Capacitor Elimination Strategy:** Across all designs, demonstrated the feasibility of using closed-loop ripple mitigation to eliminate bulky capacitors without compromising performance, improving reliability and system lifetime.
- **Hardware Validation:** All proposed converter topologies and control schemes were validated using laboratory-scale prototypes, confirming their effectiveness under practical operating conditions.

5.2 Future Work

- **Three-Phase Topologies:** The proposed converter architectures and ripple reduction strategies can be extended to three-phase systems, which are more suitable for high-power EV charging infrastructure. This would offer benefits such as improved power scalability, reduced per-phase ripple, and better thermal and electromagnetic performance.
- **Renewable Integration:** Integrating the proposed bidirectional converters with renewable sources such as photovoltaic (PV) or wind systems can enable smart, decentralized energy management for homes and microgrids. This could position EVs as active energy assets, contributing to load balancing and renewable smoothing.

- **Battery-Aware Control:** Future control strategies could incorporate real-time battery models to better manage charging profiles based on parameters like state-of-charge, internal resistance, and aging. This would enhance battery safety, prolong battery lifespan, and improve overall system efficiency.
- **Modular Design:** Developing modular and interleaved converter units could allow flexible scaling for commercial EV fleets, DC microgrids, or fast-charging stations. Such designs would also support redundancy, fault tolerance, and parallel operation for improved system robustness.

In summary, this research establishes a robust foundation for the next generation of compact, high-efficiency, grid-interactive EV chargers with strong potential for real-world deployment in sustainable transportation and smart energy systems.

Bibliography

- [1] D. Kessler and J. Bauer, “Design and implementation of a multilevel on-board charger for electric vehicles,” *IEEE Trans. Ind. Electron.*, vol. 67, no. 5, pp. 4048–4057, 2020.
- [2] N. Sundarka *et al.*, *Optimizing the topology of electrical powertrain for plug-in hybrid and electric vehicles*, http://ipindia.gov.in/writereaddata/Portal/IP0Journal/1_474_1/Part-1.pdf, India Patent 201811047973 [Online], 2018.
- [3] H. Sanchez, G. Lucca, R. Jiménez, and P. Gaona, “Differential-power processing on-board charger for 400/800-v battery architectures using 650-v super junction mosfets,” in *Proc. IEEE Appl. Power Electron. Conf. and Expo. (APEC)*, 2021, pp. 564–568.
- [4] J. Y. Kim, B. S. Lee, D. H. Kwon, D. W. Lee, and J. K. Kim, “Low voltage charging technique for electric vehicles with 800 v battery,” *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 7890–7896, Aug. 2022.
- [5] M. Momayyezani, B. Hredzak, and V. G. Agelidis, “Integrated reconfigurable converter topology for high-voltage battery systems,” *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1968–1979, Mar. 2016.
- [6] I. Aghaebrahimi, J. Bauman, P. J. Kollmeyer, Y. Wang, B. Bilgin, and A. Emadi, “800-v electric drive powertrains: Review and analysis of benefits, challenges, and future trends,” *IEEE Trans. Transport. Electrification*, vol. 7, no. 3, pp. 927–948, Sep. 2021.
- [7] S. Li, G. Zhu, S. C. Tan, and S. Y. Hui, “Direct ac/dc rectifier with mitigated low-frequency ripple through waveform control,” in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Pittsburgh, PA, 2014, pp. 2691–2697.
- [8] R. Chen, Y. Liu, and F. Z. Peng, “Dc capacitor-less inverter for single-phase power conversion with minimum voltage and current stress,” *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5499–5507, Oct. 2015.
- [9] A. Tausif, H. Jung, and S. Choi, “Single-stage isolated electrolytic capacitor-less ev onboard charger with power decoupling,” *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 1, pp. 30–39, Mar. 2019. DOI: 10.24295/CPSSSTPEA.2019.00004.

- [10] H. Esmaili and M. Asadi, “A sliding mode controller based on robust model reference adaptive proportional-integral control for stand-alone three-phase inverter,” *J. Mod. Power Syst. Clean Energy*, vol. 9, no. 3, pp. 668–678, May 2021. DOI: 10.35833/MPCE.2019.000077.
- [11] J. C. Moreno, J. M. E. Huerta, R. G. Gil, and S. A. Gonzalez, “A robust predictive current control for three-phase grid-connected inverters,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1993–2004, Jun. 2009. DOI: 10.1109/TIE.2009.2016513.
- [12] Y. Xu, Z. Li, J. Zhao, and J. Zhang, “Distributed robust control strategy of grid-connected inverters for energy storage systems’ state-of-charge balancing,” *IEEE Trans. Smart Grid*, vol. 9, no. 6, pp. 5907–5917, Nov. 2018. DOI: 10.1109/TSG.2017.2698641.
- [13] U. S. C. B. Office, “Emissions of carbon dioxide in the transportation sector,” Dec. 2022. [Online]. Available: <https://www.cbo.gov/publication/58566>.
- [14] U.S. Energy Information Administration, *Monthly energy review, march 2025*, Table 11.1–11.6, 2025. [Online]. Available: <https://www.eia.gov/totalenergy/data/monthly/>.
- [15] U.S. Environmental Protection Agency, *Sources of greenhouse gas emissions*, 2025. [Online]. Available: <https://www.epa.gov/ghgemissions/sources-greenhouse-gas-emissions>.
- [16] B. MacInnis and J. A. Krosnick, “Climate insights 2020: Electric vehicles. resources for the future (rff),” Oct. 2020. [Online]. Available: <https://www.rff.org/publications/reports/climateinsights2020-electric-vehicles>.
- [17] U. S. E. P. Agency, “Inventory of u.s. greenhouse gas emissions and sinks,” Apr. 2021. [Online]. Available: <https://www.epa.gov/ghgemissions/inventory-us-greenhouse-gasemissions-and-sinks>.
- [18] International Energy Agency, *Global ev outlook 2025: Trends in electric car markets*, Accessed: July 13, 2025, 2025. [Online]. Available: <https://www.iea.org/reports/global-ev-outlook-2025>.
- [19] S. Dion, “Reducing greenhouse gas emissions in canada,” Mar. 2018. [Online]. Available: https://www.international.gc.ca/country_news-pays_nouvelles/2018-03-23-germany-allemagne.aspx?lang=eng.
- [20] M. Yilmaz and P. T. Krein, “Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles,” *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2151–2169, May 2013.

- [21] A. König, L. Nicoletti, D. Schröder, S. Wolff, A. Waclaw, and M. Lienkamp, "An overview of parameter and cost for battery electric vehicles," *World Electric Vehicle Journal*, vol. 12, no. 1, Feb. 2021.
- [22] M. Safayatullah, M. T. Elrais, S. Ghosh, R. Rezaii, and I. Batarseh, "A comprehensive review of power converter topologies and control methods for electric vehicle fast charging applications," *IEEE Access*, vol. 10, pp. 40 753–40 793, Apr. 2022.
- [23] S. Srdic and S. Lukic, "Toward extreme fast charging: Challenges and opportunities in directly connecting to medium-voltage line," *IEEE Electrification Magazine*, vol. 7, no. 1, pp. 22–31, Mar. 2019.
- [24] "Ieee standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces," *IEEE Standard 1547-2018 (Revision of IEEE Std 1547-2003)*, pp. 1–138, 2018.
- [25] "Sae j2894-1: Power quality requirements for plug-in electric vehicle chargers—part 1: Requirements," *SAE International Standard*, 2019.
- [26] "Sae electric vehicle and plug-in hybrid electric vehicle conductive charge coupler," *SAE International Standard*, 2010.
- [27] "Plugs, socket-outlets, vehicle connectors and vehicle inlets-conductive charging of electric vehicles-part 1, 2, 3, standard," *IEC 62196*, 2014.
- [28] "Plug-on around the ev world," Dec. 2017. [Online]. Available: http://www.%20ev-institute.com/images/media/Plug_World_map_v4.pdf.
- [29] G. Rajendran, C. A. Vaithilingam, N. Mison, K. Naidu, and M. R. Ahmed, "A comprehensive review on system architecture and international standards for electric vehicle charging stations," *Journal of Energy Storage*, vol. 42, p. 103 099, Oct. 2021.
- [30] A. Khaligh and M. D'Antonio, "Global trends in high-power on-board chargers for electric vehicles," *IEEE Transactions on Vehicular Technology*, vol. 68, no. 4, pp. 3306–3324, Apr. 2019.
- [31] M. Abbasi, K. Kanathipan, and J. Lam, "An interleaved bridgeless single-stage ac/dc converter with stacked switches configurations and soft-switching operation for high-voltage ev battery systems," *IEEE Transactions on Industry Applications*, vol. 58, no. 5, pp. 5533–5545, Mar. 2022.
- [32] F. Musavi, W. Eberle, and W. G. Dunford, "A high-performance single-phase bridgeless interleaved pfc converter for plug-in hybrid electric vehicle battery chargers," *IEEE Trans. Ind. App.*, vol. 47, no. 4, pp. 1833–1843, Jul. 2021.
- [33] A. Dixit, K. Pande, S. Gangavarapu, and A. K. Rathore, "Dcm-based bridgeless pfc converter for ev charging application," *IEEE J. Emerg. Sel. Top. Ind. Electron.*, vol. 1, no. 1, pp. 57–66, Jul. 2020.

- [34] D. Zinchenko, A. Blinov, A. Chub, D. Vinnikov, I. Verbytskyi, and S. Bayhan, "High-efficiency single-stage on-board charger for electrical vehicles," *IEEE Trans. Veh. Technol.*, vol. 70, no. 12, pp. 12 581–12 592, Dec. 2021.
- [35] A. U. Rehman, H. Park, A. Ahmed, M. Kim, and J.-W. Jung, "An improved nonlinearities mitigation based control of a bridgeless single-stage ac/dc converter with enhanced reliability," *IEEE Trans. Ind. Electron.*, vol. 72, no. 1, pp. 318–329, Jan. 2025. DOI: 10.1109/TIE.2024.3406849.
- [36] A. E. L. da Costa, C. B. Jacobina, N. Rocha, E. R. C. da Silva, and A. V. d. M. Lacerda Filho, "A single-phase ac–dc–ac unidirectional three-leg converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 5, pp. 3876–3886, May 2021. DOI: 10.1109/TIE.2020.2987261.
- [37] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality ac–dc converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003. DOI: 10.1109/TIE.2003.817609.
- [38] O. Garcia, J. Cobos, R. Prieto, P. Alou, and J. Uceda, "Power factor correction: A survey," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, vol. 1, 2001, 8–13 vol. 1.
- [39] B. Singh, B. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. Kothari, "A review of single-phase improved power quality ac-dc converters," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 5, pp. 962–981, Oct. 2003.
- [40] F. Musavi and W. Eberle, "Overview of wireless power transfer technologies for electric vehicle battery charging," *IET Power Electronics*, vol. 7, no. 1, pp. 60–66, Jan. 2014.
- [41] J. Zhang, B. Su, and Z. Lu, "Single inductor three-level bridgeless boost power factor correction rectifier with nature voltage clamp," *IET Power Electronics*, vol. 5, no. 3, pp. 358–365, Mar. 2012.
- [42] V. Yaramasu, B. Wu, P. C. Sen, S. Kouro, and M. Narimani, "High-power wind energy conversion systems: State-of-the-art and emerging technologies," *Proceedings of the IEEE*, vol. 103, no. 5, pp. 740–788, May 2015.
- [43] J.-M. Kwon, B.-H. Kwon, and K.-H. Nam, "Three-phase photovoltaic system with three-level boosting mppt control," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2319–2327, Sep. 2008.
- [44] S. Yang, Q. Lei, F. Z. Peng, and Z. Qian, "A robust control scheme for grid-connected voltage-source inverters," *IEEE transactions on Industrial Electronics*, vol. 58, no. 1, pp. 202–212, Jan. 2010.

- [45] V. K. Goyal and A. Shukla, "Isolated dc–dc boost converter for wide input voltage range and wide load range applications," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 10, pp. 9527–9539, Oct. 2021.
- [46] S. Deshmukh, A. Iqbal, S. Islam, *et al.*, "Review on classification of resonant converters for electric vehicle application," *Energy Reports*, vol. 8, pp. 2352–4847, Nov. 2022.
- [47] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance evaluation of bridgeless pfc boost rectifiers," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1381–1390, May 2008.
- [48] Y. Jeong, J.-K. Kim, and G.-W. Moon, "A bridgeless dual boost rectifier with soft-switching capability and minimized additional conduction loss," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 2226–2233, Aug. 2018.
- [49] Z. Yu, Y. Xia, and R. Ayyanar, "A simple zvt auxiliary circuit for totem-pole bridgeless pfc rectifier," *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 2868–2878, May 2019.
- [50] Q. Huang, R. Yu, Q. Ma, and A. Q. Huang, "Predictive zvs control with improved zvs time margin and limited variable frequency range for a 99% efficient, 130-w/in³ mhz gan totem-pole pfc rectifier," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 7079–7091, Oct. 2019.
- [51] M. Abbasi and J. Lam, "A bridgeless ac/dc high voltage gain converter with three-phase modular series-output connected configuration for mvdc grid applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10 323–10 337, Mar. 2020.
- [52] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509–517, May 1996.
- [53] M. A. Perez, S. Ceballos, G. Konstantinou, J. Pou, and R. P. Aguilera, "Modular multilevel converters: Recent achievements and challenges," *IEEE Open Journal of the Industrial Electronics Society*, vol. 2, pp. 224–239, Feb. 2021.
- [54] C. Shi, H. Wang, S. Dusmez, and A. Khaligh, "A sic-based high-efficiency isolated onboard pev charger with ultrawide dc-link voltage range," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 501–511, Jan. 2017.
- [55] H. V. Nguyen, D.-C. Lee, and F. Blaabjerg, "A novel sic-based multi-functional onboard battery charger for plug-in electric vehicles," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5635–5646, May 2021.
- [56] C. Oh, D. Kim, D. Woo, W. Sung, Y. Kim, and B. Lee, "A high-efficient nonisolated single-stage on-board battery charger for electric vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5746–5757, Dec. 2013.

- [57] S. Li, J. Deng, and C. C. Mi, "Single-stage resonant battery charger with inherent power factor correction for electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 62, no. 9, pp. 4336–4344, Nov. 2013.
- [58] J. Wu, S. Li, S.-C. Tan, and S. Y. R. Hui, "Capacitor-clamped llc resonant converter operating in capacitive region for high-power-density ev charger," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 456–468, Oct. 2021.
- [59] S. Derakhshan and J. Lam, "A single-stage ac/dc bridge-less converter with an adaptive control scheme and reduced dc-link and output capacitances for high voltage ev systems," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 2037–2042.
- [60] S. Jeong, Y. Jeong, J. Kwon, and B. Kwon, "A soft-switching single-stage converter with high efficiency for a 3.3-kw on-board charger," *IEEE Trans. Ind. Electron.*, vol. 66, no. 9, pp. 6959–6967, Sep. 2019.
- [61] D. Patil and V. Agarwal, "Compact onboard single-phase ev battery charger with novel low-frequency ripple compensator and optimum filter design," *IEEE Trans. Veh. Technol.*, vol. 65, no. 4, pp. 1948–1956, Apr. 2016.
- [62] N. Spode, M. A. D. Costa, G. Z. Abdelmessih, J. M. Alonso, and R. R. Duarte, "Reducing low-frequency ripple using alternative output capacitor connection on integrated converters for led drivers," *IEEE Trans. Ind. App.*, vol. 59, no. 4, pp. 5158–5168, Jul. 2023.
- [63] J. V. Missula, R. Adda, and P. Tripathy, "Ripple reduction in the dc-link capacitor voltages of single-phase anpc inverter using external chopper circuit," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, Singapore, 2020, pp. 2436–2441.
- [64] H. K. H. Belkamel and S. Choi, "Interleaved totem-pole zvs converter operating in ccm for single-stage bidirectional ac–dc conversion with high-frequency isolation," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3486–3495, Mar. 2021.
- [65] Y.-T. Huang, C.-C. Yang, T.-S. Li, and Y.-M. Chen, "A feedforward voltage control strategy for reducing the output voltage double-line-frequency ripple in single-phase ac–dc converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 6, pp. 6605–6612, Dec. 2021.
- [66] J. Yuan, L. Dorn-Gomba, A. D. Callegaro, J. Reimers, and A. Emadi, "A review of bidirectional on-board chargers for electric vehicles," *IEEE Access*, vol. 9, pp. 51 501–51 518, Mar. 2021.
- [67] L. Sih-Yi, J. Jynu-Jhe, L. Jing-Yuan, H. Yao-Ching, and C. Haung-Jen, "High-voltage bi-directional half-bridge three-level series resonant converter with frequency modulation control," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, 2018, pp. 645–650.

- [68] S. Derakhshan and J. Lam, “A bridge-less, stacked switch-pair based ac/dc on-board high voltage ev charger with minimal storage capacitance featuring continuous secondary-side high frequency rectifier control,” *IEEE J. Emerg. Sel. Top. Ind. Electron.*, 2024.
- [69] Y. Z. et al., “A boost-inductorless electrolytic-capacitorless single-stage bidirectional isolated ac–dc converter,” *IEEE Tran. Power Electron.*, vol. 38, no. 4, pp. 5496–5478, Apr. 2023.
- [70] G. K. N. Kumar and A. K. Verma, “A single-phase interleaved buck-boost pfc based on-board ev charger,” *IEEE Tran. Ind. App.*, vol. 59, no. 6, pp. 7163–7174, Nov. 2023.
- [71] N. Patel, L. A. C. Lopes, A. Rathore, and V. Khadkikar, “A soft-switched single-stage single-phase pfc converter for bidirectional plug-in ev charger,” *IEEE Trans. Ind. App.*, vol. 59, no. 4, pp. 5123–5135, Jul. 2023.
- [72] S. Derakhshan and J. Lam, “A new bridge-less ac-dc stacked-switches structured bi-directional on-board high voltage ev charger with minimal storage capacitances,” in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA., 2024*, pp. 1700–1705.
- [73] M. Kwon and S. Choi, “An electrolytic capacitorless bidirectional ev charger for v2g and v2h applications,” *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6792–6799, Sep. 2017.
- [74] J. Yuan, A. Poorfakhraei, Y. Zhang, G. Fang, C. Liu, and A. Emadi, “An improved adaptive sinusoidal single phase shift modulation for bidirectional single-stage onboard ev chargers,” *IEEE Trans. Transport. Electrific.*, Oct. 2023.
- [75] U. Sharma and B. Singh, “A bidirectional onboard charger with multi-step constant current charging capability,” *IEEE Trans. Transport. Electrific.*, vol. 9, no. 1, Mar. 2023.
- [76] M. Su *et al.*, “A natural bidirectional isolated single-phase ac/dc converter with wide output voltage range for aging test application in electric vehicle,” *IEEE J. Emerg. Sel. Top. Ind. Electron.*, vol. 9, no. 3, pp. 3489–3500, Jun. 2021.
- [77] M. Global, “Aluminium electrolytic and film capacitors,” [Online]. Available: <https://www.mersen.com/products/solutions-power-management/aluminium-electrolytic-and-film-capacitors>.
- [78] Panasonic, “Ecw-fg series metallized polypropylene film capacitors 700v and 800v,” [Online]. Available: <https://na.industrial.panasonic.com/whats-new/ecw-fg-series-metallized-polypropylene-film-capacitors-700v-and-800v>.

- [79] kyocera, “Multilayer ceramic chip capacitors (mlcc),” [Online]. Available: <https://ele.kyocera.com/en/product/capacitor/mlcc/>.
- [80] F. Zhao, X. Wang, Z. Zhou, Y. Sun, L. Harnefors, and T. Zhu, “Robust grid-forming control with active susceptance,” *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 2872–2875, Mar. 2023.
- [81] S. Chakraborty, S. Patel, and M. V. Salapaka, “ μ -synthesis-based generalized robust framework for grid-following and grid-forming inverters,” *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3163–3176, Mar. 2023.
- [82] L. Huang, H. Xin, and F. Dörfler, “ H_∞ -control of grid-connected converters: Design, objectives and decentralized stability certificates,” *IEEE Trans. Smart Grid*, vol. 11, no. 5, pp. 3805–3817, Sep. 2020.
- [83] A. Afshari, M. Karrari, H. R. Baghaee, G. B. Gharehpetian, and J. M. Guerrero, “Robust cooperative control of isolated ac microgrids subject to unreliable communications: A low-gain feedback approach,” *IEEE Syst. J.*, vol. 16, no. 1, pp. 55–66, Mar. 2022.
- [84] M. Babazadeh and A. Nobakhti, “Robust decomposition and structured control of an islanded multi-dg microgrid,” *IEEE Trans. Smart Grid*, vol. 10, no. 3, pp. 2463–2473, May 2019.
- [85] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd. Boston, MA, USA: Kluwer, 2001.
- [86] M. Abbasi and J. Lam, “A bridgeless ac/dc high voltage gain converter with three-phase modular series-output connected configuration for mvdc grid applications,” *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10 323–10 337, Oct. 2020.
- [87] K. Yao, L. Li, H. Tang, C. Mao, and K. Chen, “Optimum boundary inductance control concerning limited pf for a dcm boost pfc converter,” *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 443–454, Jan. 2020.
- [88] H. K. Khalil, *Nonlinear Systems*, 3rd. Upper Saddle River: Prentice Hall, 2002.
- [89] J. Schiffer, D. Efimov, and R. Ortega, “Global synchronization analysis of droop-controlled microgrids—a multivariable cell structure approach,” *Automatica*, vol. 109, 2019.
- [90] M. Kwon and S. Choi, “An electrolytic capacitorless bidirectional ev charger for v2g and v2h applications,” *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6792–6799, Sep. 2017.
- [91] L. Xue, Z. Shen, D. Boroyevich, P. Mattavelli, and D. Diaz, “Dual active bridge-based battery charger for plug-in hybrid electric vehicle with charging current containing low frequency ripple,” *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7299–7307, Dec. 2015.

- [92] *Electromagnetic Compatibility (EMC) – Part 3-2: Limits – Limits for Harmonic Current Emissions (equipment input current ≤ 16 A per phase*, 2018.
- [93] L. A. Rodrigues, E. C. L. F. Oliveira, and J. F. Camino, “Parameterized limits for robust h_2 and h_∞ state feedback control of continuous-time polytopic systems,” *Int. J. Robust Nonlinear Control*, vol. 28, no. 3, pp. 840–952, Feb. 2018.

Appendix A

List of Publications

Peer-Reviewed Journal Papers

- J1 **S. Derakhshan** and J. Lam, "Linear Matrix Inequality-Based Robust H_∞ AC-Grid-Forming Control of an Electrolytic Capacitor-Less On-Board Charger for V2H Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, (submitted June 2025).
- J2 **S. Derakhshan** and J. Lam, "A Bridgeless, A Half-Bridge/Dual Stacked-Switches Structured AC/DC Electrolytic Capacitor-Less Bidirectional Converter with Soft-Switching for High-Voltage EV Charger," in IEEE Transactions on Power Electronics, vol. 40, no. 8, pp. 10912-10930, Aug. 2025.
- J3 **S. Derakhshan** and J. Lam, "A Bridgeless, Stacked Switch-Pair-Based AC/DC On-Board High-Voltage EV Charger With Minimal Storage Capacitance Featuring Continuous Secondary-Side High-Frequency Rectifier Control," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 12, no. 4, pp. 3439-3455, Aug. 2024.
- J4 **S. Derakhshan**, K. Kanathipan, M. Abbasi, M. A. M. Cheema and J. Lam, "A Robust H_∞ State Feedback Controller Enabling a Medium Voltage Five-Level Grid-Connected Inverter for Grid Code Compliance," in IEEE Transactions on Power Delivery, vol. 39, no. 1, pp. 647-660, Feb. 2024.

Peer-Reviewed Conference Papers

- C1 **S. Derakhshan** and J. Lam, "Robust H_∞ AC-Grid-Forming Electrolytic Capacitor-Free Fully Soft-Switched AC/DC On-Board Charger for Vehicle-to-Home Application," 2025 IEEE Energy Conversion Congress and Exposition (ECCE), Philadelphia, PA, USA, 2025.
- C2 **S. Derakhshan** and J. Lam, "A New Half-Bridge/Dual-Stacked-Switches Structured Electrolytic Capacitor-less AC/DC Bi-Directional On-Board Charger for High-Voltage EV Battery," 2024 IEEE Energy Conversion Congress and Exposition (ECCE), Phoenix, AZ, USA, 2024, pp. 3188–3194.
- C3 **S. Derakhshan** and J. Lam, "A New Bridge-Less AC-DC Stacked-Switches Structured Bi-Directional On-Board High Voltage EV Charger with Minimal Storage Capacitances," 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2024, pp. 1700–1705.
- C4 **S. Derakhshan** and J. Lam, "A Bridgless Stacked Switches-Based AC-DC Converter with Reduced Storage Capacitances and Low-Frequency Voltage Ripple for HV EV Systems," 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA, 2023, pp. 6577–6579.
- C5 **S. Derakhshan** and J. Lam, "A Single-Stage AC/DC Bridge-Less Converter with an Adaptive Control Scheme and Reduced DC-Link and Output Capacitances for High Voltage EV Systems," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 2037–2042.
- C6 **S. Derakhshan** and J. Lam, "A Multi-Mode Hybrid CCM/DCM Three-Phase Step-Up AC/DC Soft-Switched Converter with an Adaptive Active-Controlled Auxiliary Circuit and Constant Output Voltage," 2022 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2022, pp. 1–7.

Appendix B

Printed Circuit Board (PCB) Layouts

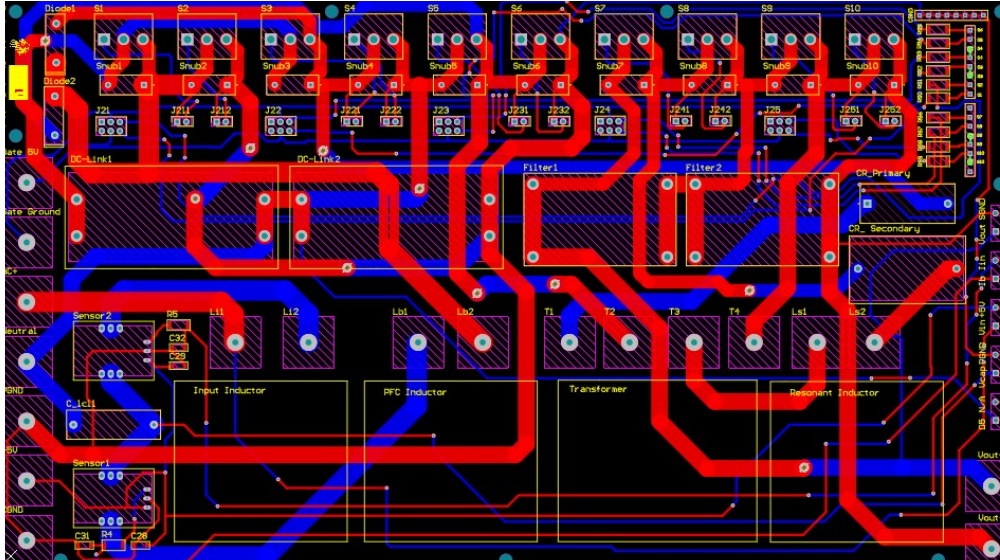


Figure B.1: PCB layout of the proposed AC/DC bidirectional converter.

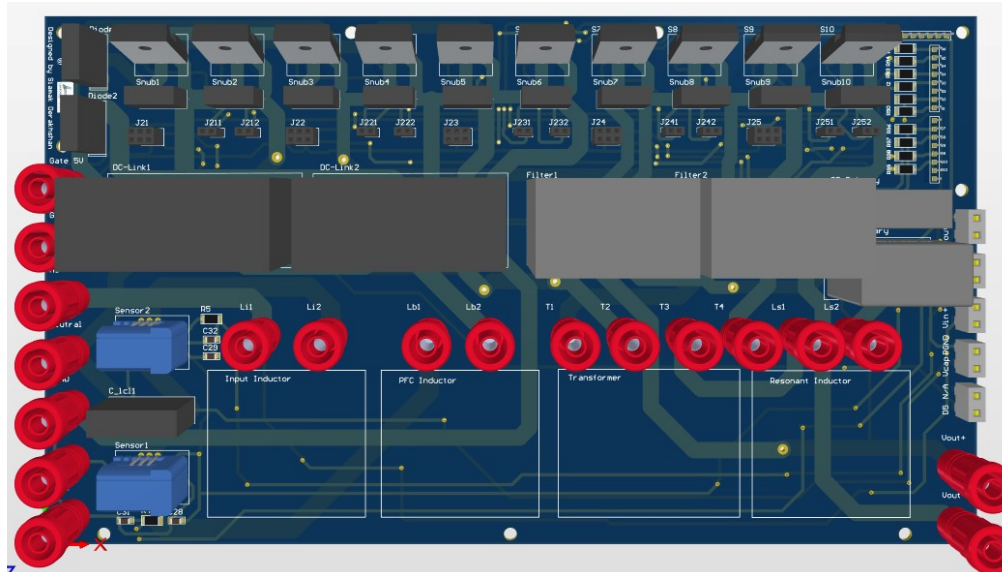


Figure B.2: 3-D view of the PCB layout of the proposed AC/DC bidirectional converter.

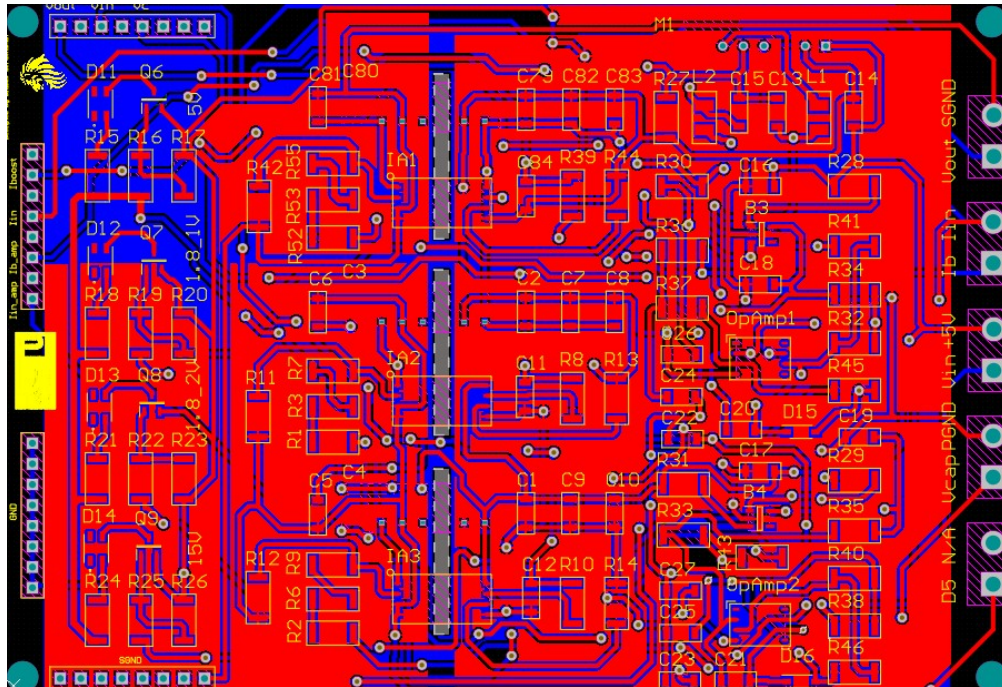


Figure B.3: PCB layout of the measurement board designed for the proposed AC/DC bidirectional converter.

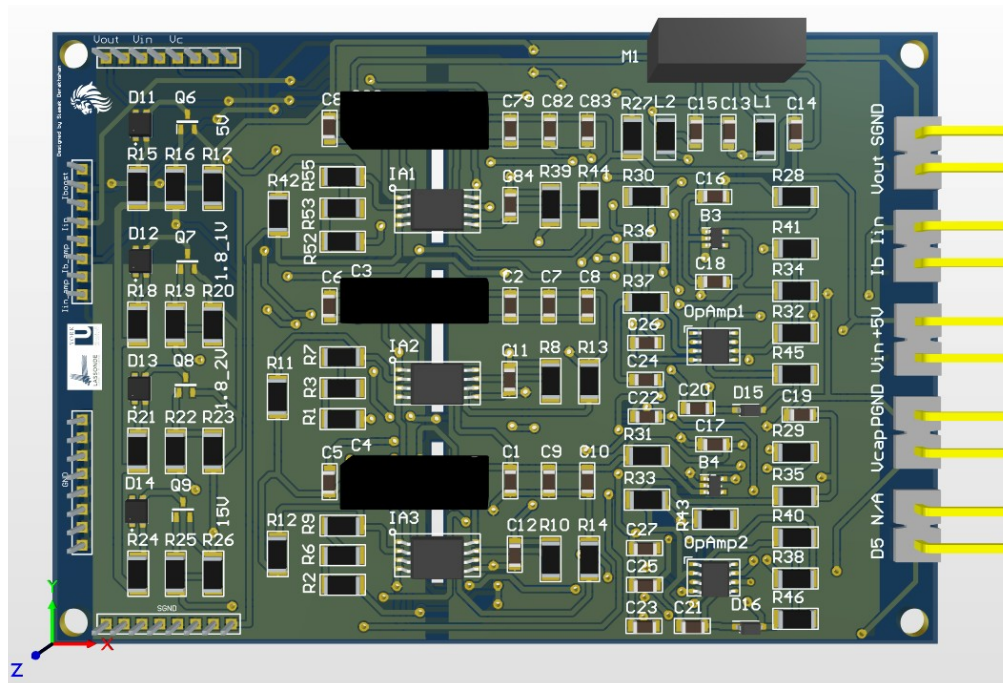


Figure B.4: 3-D view of the PCB layout of the measurement board designed for the proposed AC/DC bidirectional converter.

Appendix C

PSIM Schematics

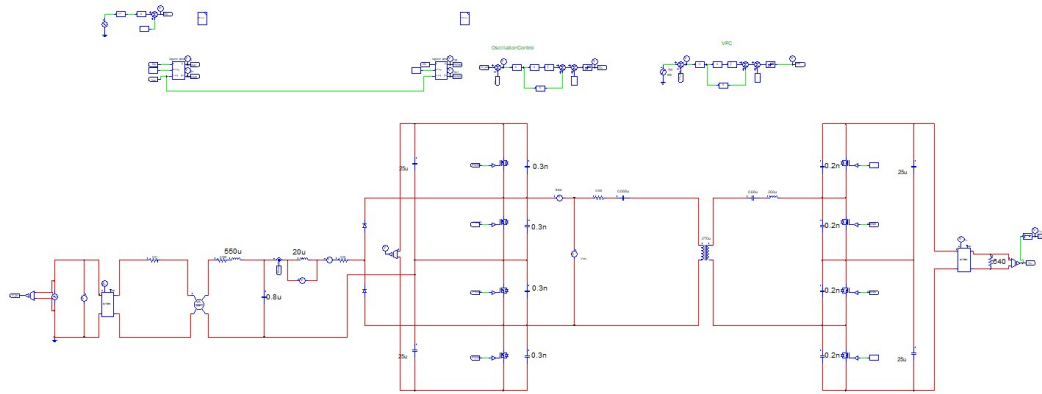


Figure C.1: Diagram of a proposed unidirectional AC/DC converter topology and its control blocks from PSIM.

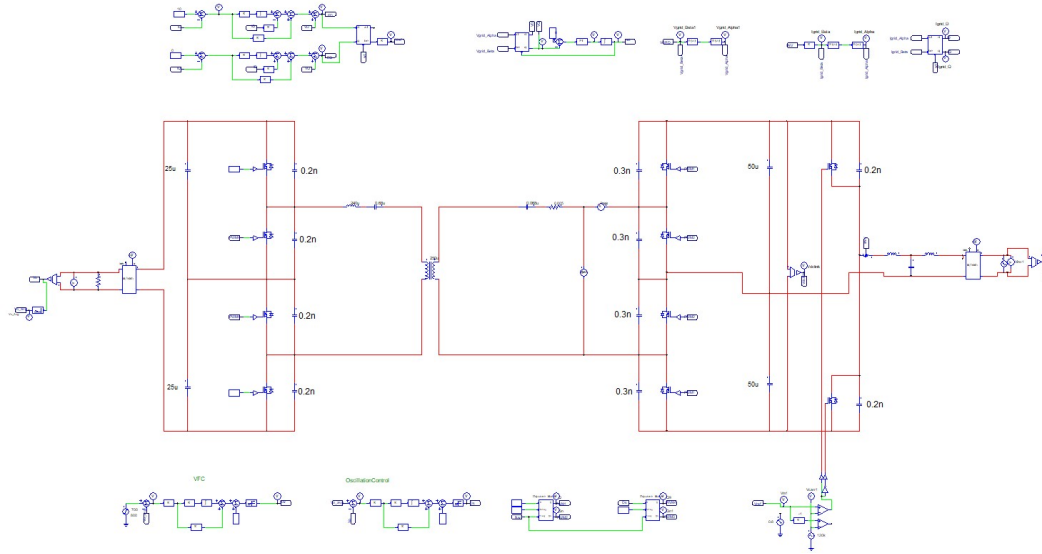


Figure C.2: Diagram of a proposed bidirectional AC/DC converter topology in AC to DC mode and its control blocks from PSIM.

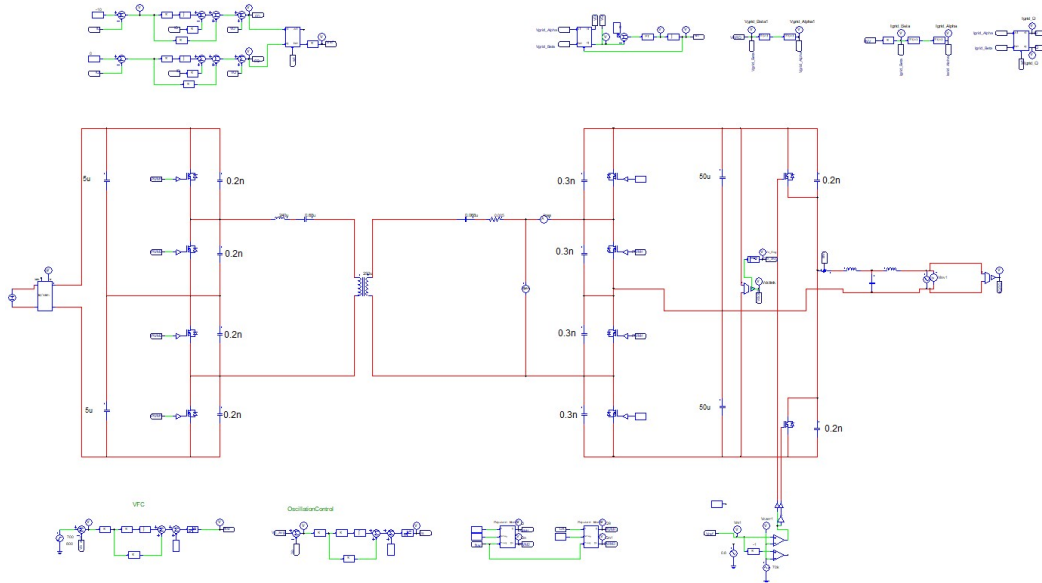


Figure C.3: Diagram of a proposed bidirectional AC/DC converter topology in DC to AC mode and its control blocks from PSIM.

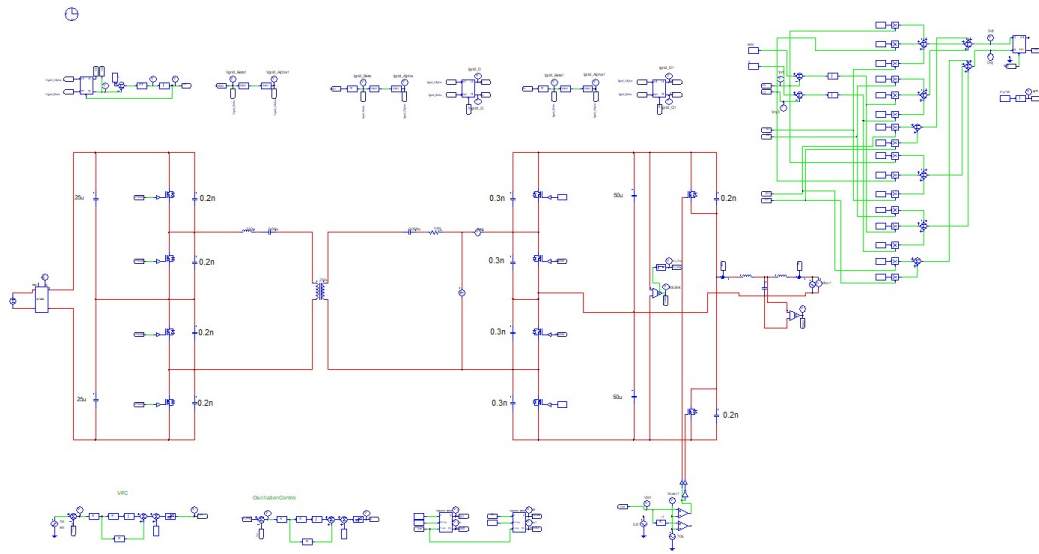


Figure C.4: Diagram of a proposed bidirectional AC/DC converter topology in DC to AC mode and the developed AC-GFM control block from PSIM.