ULTRA-LOW POWER WIRELESS SENSOR CIRCUITS FOR IOT APPLICATIONS

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ABSTRACT

Wireless sensors, which are responsible for local data acquisition, processing and communication, play an important role in Internet of Things (IoT) applications. This research focuses on two basic components in wireless sensors, i.e., the low-power frequency tunable wireless receiver and the power management unit (PMU) for autonomous operation.

In IoT applications, different sensors may need to operate in different frequency bands in order to meet environment constraints and industrial/medical standards. Thus, it is highly desirable to design a frequency configurable wireless receiver that provides flexibility in operation frequency. A 4-path filter based frequency shift keying (FSK) receiver is proposed to meet such a need, where the carrier frequency can be adjusted without changing the circuit. In addition, the proposed receiver requires no low-noise amplifier (LNA), which boosts the power efficiency. Frequency synthesizer is critical in FSK transceiver as it provides an accurate reference frequency. Based on 4-path mixer, a novel two-step calibration frequency synthesizer structure is proposed for low power consumption and wide locking range. Measurement results show that the proposed receiver achieves an energy per bit as 74pJ/bit with 2.5Mbps data rate and 184μW power consumption. Post-layout simulation results show that the proposed frequency synthesizer has a figure of merit (FOM) value as 1.4μW/MHz with 220MHz tuning bandwidth and 305μW power consumption.

Autonomous operation is another requirement for the sensors in many IoT applications, such as wearable sensors. Energy harvester is commonly used for autonomous sensors, where a PMU with low start-up voltage is necessary. To meet such a requirement, a novel controller for PMU is proposed to boost the power efficiency under very low load current. The proposed PMU can be started up with input voltage as low as several tens of millivolts. The novel controller costs little power and the overall efficiency is increased. Also, a hardware efficient maximum power point tracking (MPPT) algorithm which is suitable for energy source with fixed internal resistance is proposed. Measurement results show that the proposed system has a low controller power as 3.6μW and the overall conversion efficiency is 83.9%.

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AFC	Automatic Frequency Calibration
ASK	Amplitude Shift Keying
BB	Base Band
BER	Bit Error Rate
BGR	Band Gap Reference
CP	Charge Pump
D2S	Differential-to-Single-ended
DCM	Discontinuous Conduction Mode
DCO	Digital Controlled Oscillator
DMD	Dual-Mode Demodulator
DTCMOS	Dynamic Threshold CMOS
FAC	Frequency-to-Amplitude Converter
FSK	Frequency Shift Keying
FSPSM	Folded Semi-Passive Sub-harmonic Mixer
I/Q	In phase/Quadrature
ILCM	Injection Locked Clock Multiplier
IL-DCO	Injection-Locking Digitally Controlled Oscillator

ILO	Injection-Locked Oscillator
ILRO	Injection Locked Ring Oscillator
IoT	Internet of Things
ISM	Industrial Scientific and Medical
ITU	International Telecommunication Union
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass Filter
LR	Locking Range
LTI	Linear Time-Invariant
MCB	Mode Change Block
MGLNA	Multiple-Gated Low-Noise Amplifier
MPPT	Maximum Power Point Tracking
OOB	Out-Of-Band
OOK	On-Off Keying
OTC-PSM	On-Time Calibration Pulse Skipping Modulation
PA	Power Amplifier
PFD	Phase-Frequency Detector
PFM	Pulse Frequency Modulation
PLL	Phase-Locked Loop

PMU	Power Management Unit
PVT	Process Voltage and Temperature
PWM	Pulse Width Modulation
RF	Radio Frequency
RMS	Root-Mean-Square
SAW	Surface Acoustic Wave
SC	Switch Capacitor
SDC	Single-to-Differential Circuit
SNR	Signal Noise Ratio
TEG	Thermoelectric Generator
VCO	Voltage-Controlled Oscillator
VGA	Variable Gain Amplifier
WBAN	Wireless Body Area Network
WSN	Wireless Sensor Network
WUC	Wake-Up Circuit
WURX	Wake-up Receiver
ZCS	Zero Current Switching

Chapter 1

Introduction

1.1 Research Motivation

Thanks to the rapid development of the Internet, the Internet of Things (IoT) emerged in 21st century and starts changing our daily life. Currently there are already more connected things than people in the world. It is calculated that around 28.4 billion IoT devices were in use in 2017, which was up by 24 percent from that in 2016, and this will likely reach 50.1 billion by the end of 2020 as shown in Fig. 1-1-1 [1]. The IoT market size also exhibits tremendous development currently. The global IoT market is estimated to reach $1,599T by 2024, from $346.1B in 2016, attaining a compound annual growth rate of 21.1% from 2016 to 2024 as shown in Fig. 1-1-2 [2].

Extending internet connectivity to everyday objects transforms industry and people's daily life and creates tremendous cost savings. For companies, the IoT technology may provide benefits in several aspects such as improving customer experience, collecting new data, reducing the cost of labour and improving the efficiency. For individuals, IoT can provide them with a more convenient life by connecting more and more things together. For example, thanks to the connected household appliances, people can do the housework by simply touching their smartphones. And IoT can even save people's life by monitoring the vital signs in real time, which means that not only things, but human beings can also be incorporated into the IoT [3][4].

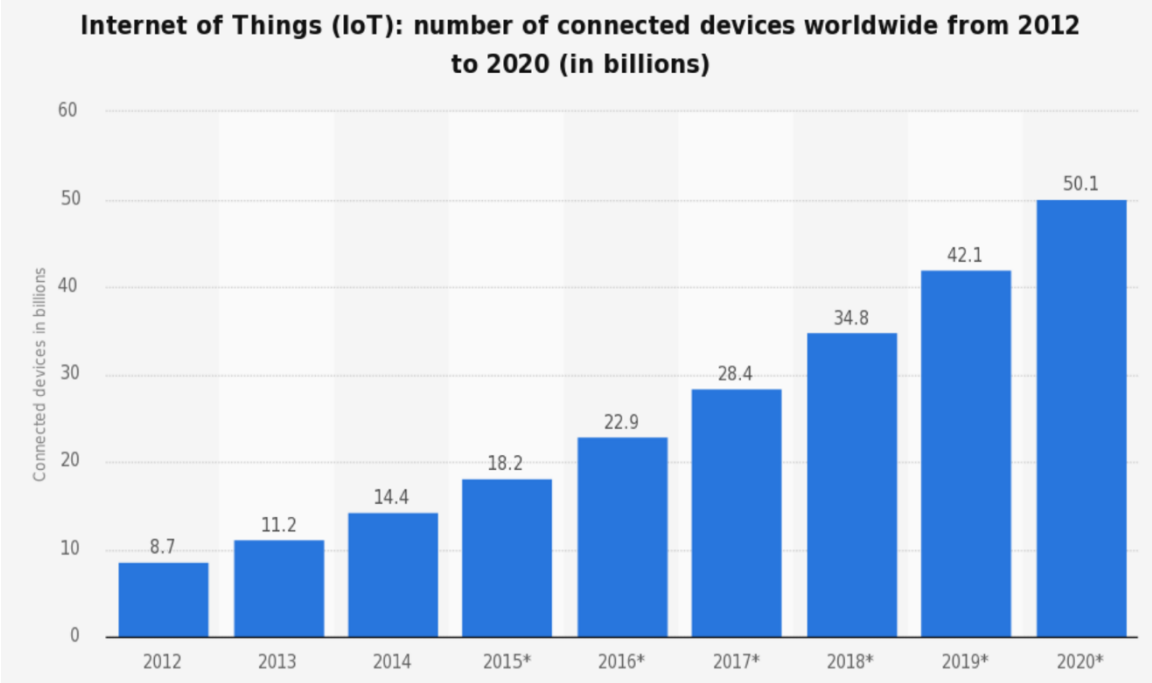


Fig. 1-1-1 Tendency of the number of connected devices worldwide [1]

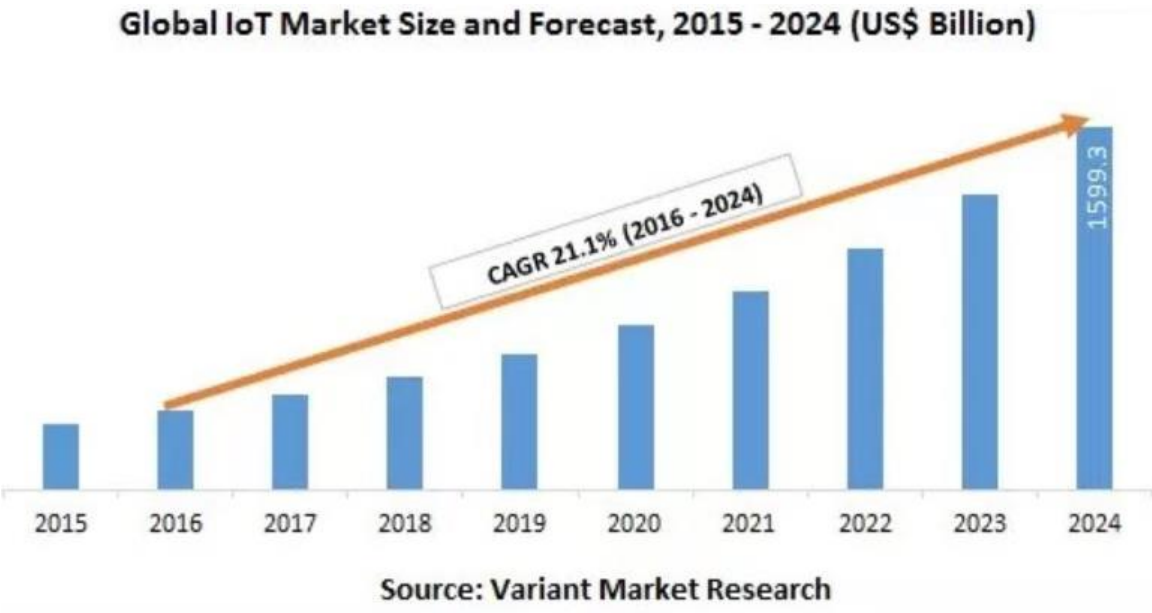


Fig. 1-1-2 Tendency of the global market size of IoT [2]

There are many kinds of technology involved in IoT applications, such as addressability, secured wireless communication, data processing, software development, etc. Among the different technology categories, hardware takes the biggest part and it costs $239 billion on modules and sensors, which takes about 50% of the overall IoT market value [5]. Without good sensors, most IoT applications would not exist. This fact makes sensors the critical design component when developing most new IoT applications. Individuals and organizations can use wireless sensors to enable many different kinds of smart applications. From interconnected homes to smart cities, from military to bioengineering, from industry to education, wireless sensors create the infrastructure upon which the IoT comes alive [6][7].

In IoT applications, tons of sensors are distributed across large geographic areas and they together with the central gateway form a wireless sensor network (WSN). Fig. 1-1-3 gives a detailed range of applications of the WSN based IoT and we can see that it covers every aspect in our life [8]. Generally, such network should have some critical characteristics to be considered as a well-designed network, such as the ability to cope with node failures, the scalability to large scale of deployment, the ability to withstand harsh environmental conditions, etc. Some of the characteristics are guaranteed by the network (for example, how to choose among mesh topology or star topology or the combination of them, how to choose the communication protocol between sensor nodes), while others are determined by the sensor node. In this research, we focus on the design of important circuit blocks for wireless sensor nodes.

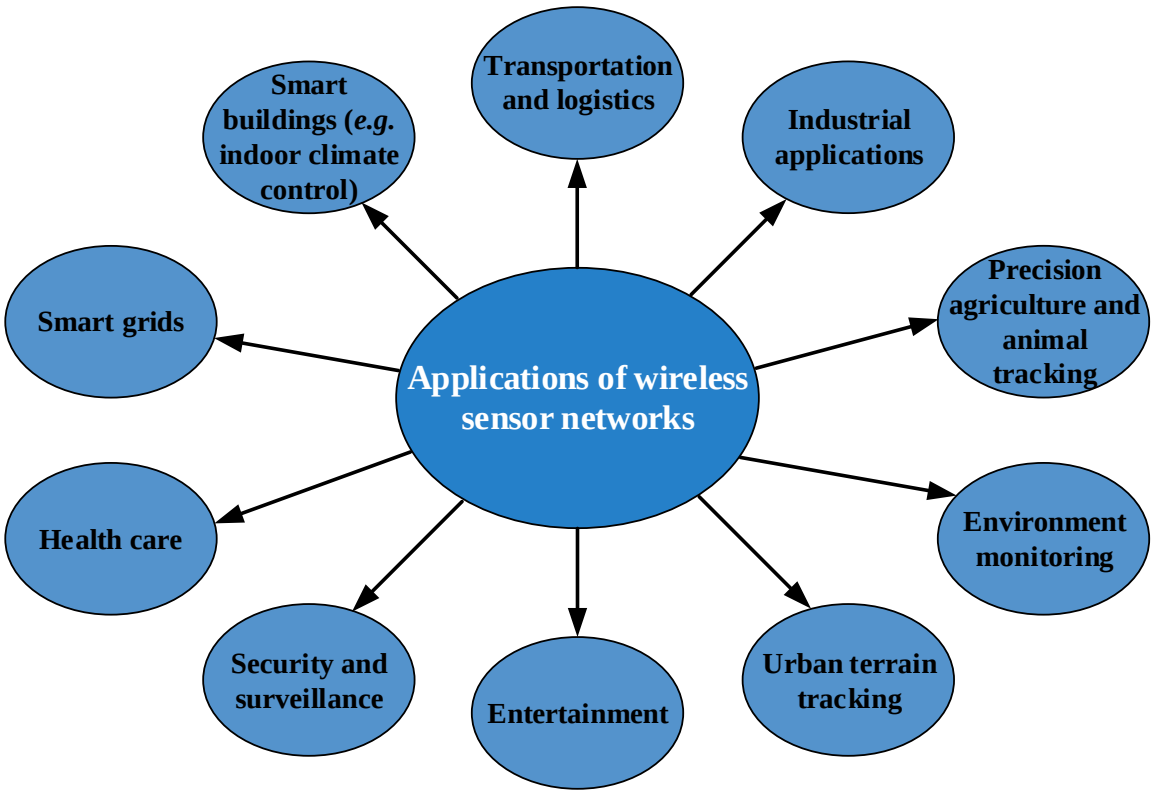


Fig. 1-1-3 Different applications for the WSN based IoT [8]

The basic functions of a wireless sensor in IoT applications include obtaining information, processing it, and communicating it to its neighbors. And all the functional blocks should be powered by batteries or an energy harvester. For a better understanding of how these functions are realized, Fig. 1-1-4 gives a typical architecture of a wireless sensor used in IoT applications. As can be seen, it is composed of four basic functional blocks, power unit, sensing unit, processing unit and communication unit [9].

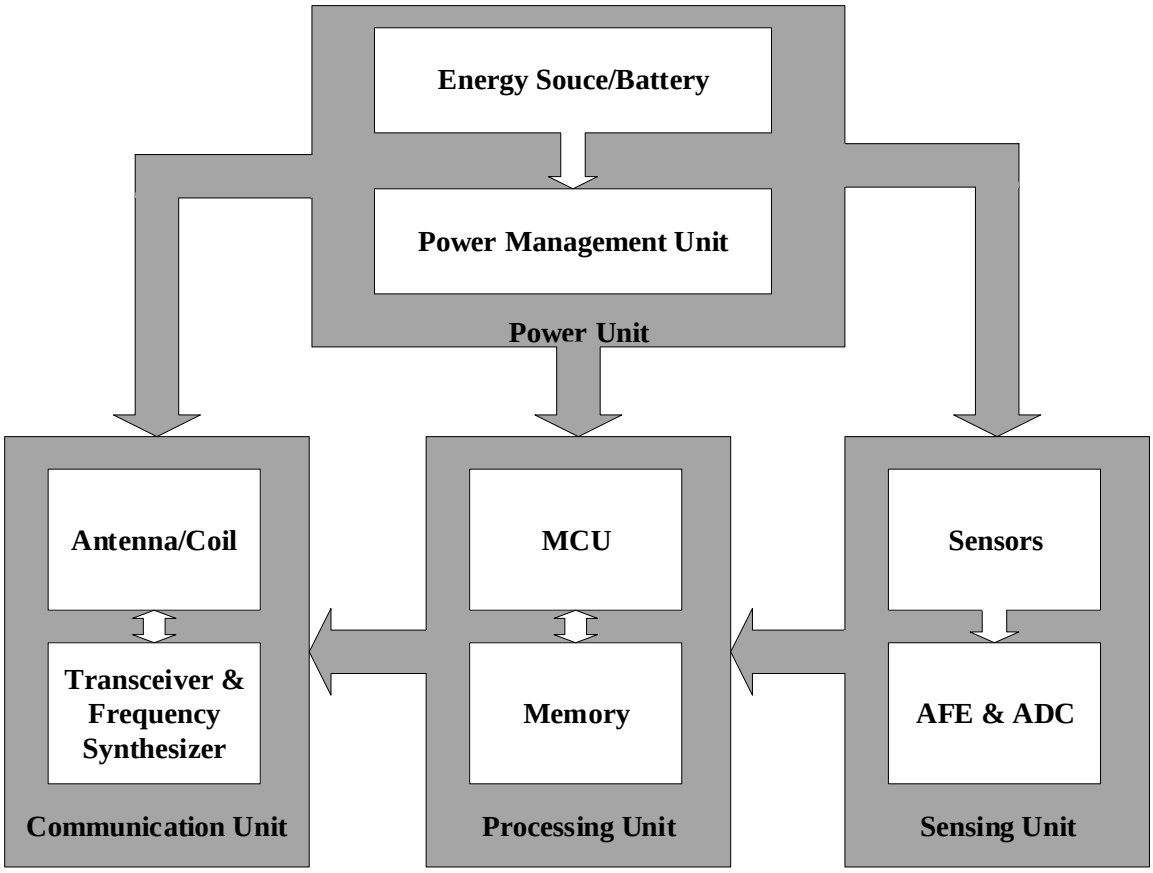


Fig. 1-1-4 Typical architecture of a wireless sensor

Power unit is responsible to supply the other functional blocks with regulated supply voltage and required power. The most common choice for power unit is battery or super-capacitor with high energy density. However, as the wireless sensors in some IoT applications are deployed in a hard-to-reach location, changing the battery or charging the super-capacitor regularly can be costly and inconvenient. So either we extend the lifetime of batteries and super-capacitors by power saving techniques, such as dynamic power management or dynamic voltage scaling to reduce the power consumption of the system [10], or we make the sensor be autonomous by harvesting the surrounding environmental

energy [11][12]. Possible energy sources are photovoltaic energy, vibration energy, radio frequency (RF) energy and thermoelectric energy. Each source has its own characteristics and design challenges for the corresponding power management unit, and we will illustrate them in detail in the following sections.

Sensing unit is used to capture data from the environment and to convert the sensed analog signal to digital signal after proper filtering and amplification. Sensors measure physical data such as temperature, pressure, human vital signs, and etc. Analog front end (AFE) is an interface between sensors and analog-digital-converter (ADC) and it is usually composed of filters and amplifiers. ADC is used to convert the AFE processed analog signal to digital signal for the processing unit with proper resolution.

Processing unit processes data and it is usually composed of a microcontroller unit (MCU) and a memory. As the data processing task required within the wireless sensor is usually less complicated, the main considerations for the MCU are low cost and low power consumption, while providing adequate computation power.

Communication unit is used for data exchange with the gateways in the WSN. A transceiver is necessary to modulate/demodulate the digital signal, but it usually consumes the main part of the power budget in wireless sensor, e.g., in [13], the transceiver takes 762μW out of the total 942.9μW power consumption of the wireless sensor SoC. Thus, energy efficient architecture and modulation techniques should be taken into consideration for the design. Also, the carrier frequency of the modulated signal may differ among sensors due to different standard requirement. For example, the industrial, scientific,

medical (ISM) band is commonly used in IoT applications and it differs in different countries, i.e., 433.05MHz to 434.79MHz band is only used in ITU region 1 countries and 902MHz to 928MHz band is only used in region 2 countries [14]. Thus, it's desirable to have a frequency tunable transceiver so that we don't need to customize the transceiver for different frequency bands. A frequency synthesizer is also needed in the communication unit to provide an accurate local oscillation frequency for the transceiver. As the transceiver is supposed to be frequency tunable, the synthesizer shall be able to cover a large frequency range so that it's compatible with the transceiver. Also, the power consumption of the frequency synthesizer should be low.

In general, the wireless sensor should be able to deliver data with high power efficiency. Currently, there are some exciting achievements regarding the wireless sensor design in different IoT applications [13][15]-[21]. In [13], a CMOS multi-sensor SoC capable of reconfiguration, self powering, signal processing and wireless communication is presented for real-time human vital sign monitoring. The proposed SoC can monitor four physiological parameters (temperature, glucose/protein concentration and pH value) simultaneously and it consumes only 942.9μW. Despite the AFE, ADC and wireless transmitter, the SoC has an embedded energy harvesting interface which can gather light energy and RF energy. However, its energy conversion efficiency is only 73% and its wireless carrier frequency is fixed. In [15], the authors proposed a single-chip sensor node IC for continuous and real-time ECG monitoring. The authors focused on the design of the AFE, $\Delta\sum$ADC and on-off keying (OOK) transmitter. The AFE has a programmable gain

from 38 to 58dB, a bandwidth from 0.1 to 300Hz and a total integrated input referred noise as 18.7μV. The ADC has an ENOB as 10bits and it consumes 71μA with 0.7V voltage supply. The OOK transmitter consumes 670μW at 433.92MHz carrier frequency and 19.2kbps to 1Mbps data rate. However, a critical component is missing from this design, i.e. no wireless receiver is integrated in the sensor chip. Without a receiver, the sensor won't be able to collaborate with other sensor nodes in the WSN. In [20], a 70μW 1.19mm^2 wireless sensor SoC with 32 channels of resistive and capacitive sensors is presented, which can be applied in various IoT scenarios, such as environmental monitoring, wearable and human-computer interaction. A novel CDMA-like resistance/capacitance-to-voltage converter and a single-slope ADC form the sensing unit in the SoC and its communication unit applies an edge-encoded PWM UWB transceiver for low power consumption. However, the SoC lacks power unit and the UWB transceiver occupies a large bandwidth despite of the low power feature.

By reviewing the state-of-art wireless sensor SoCs, we see that there is less motivation to focus on the processing unit as the local data processing load is not heavy. While all the other three functional blocks of the wireless sensor draw attention of the researchers, the sensing unit may have different requirements according to the sensed parameter. For example, the required AFE bandwidth for ECG in [15] is different from that for other physiological parameters in [13]. In contrast, the power and communication units can be designed to be generally suited for different wireless sensors. And such universality can reduce the cost comparing to the customized design. Therefore, in this research, we

will focus on the design for power and communication units. Note that even the transmitter and receiver are both important for wireless sensor, we focus on the receiver design in this research mainly because that the it is considered more challenging than transmitter design, especially for low power design.

There are many researchers focusing on the receiver [22]-[30] and frequency synthesizer [31]-[36] design and good performances have been achieved. In recent studies, frequency shift keying (FSK) shows a high-transmission efficiency. Meanwhile, it is less susceptible to frequency pulling due to its constant envelop nature, thus, it has better noise immunity at very low power levels [22][23]. By combining sliding-IF based low-power down-conversion and relative-power-detection based FSK demodulation, the proposed receiver in [25] achieves -102dBm sensitivity with 0.6V supply voltage and 466μW power consumption. In [28], a dual injection locked FSK-to-ASK conversion technique is proposed and the FSK receiver achieves -78dBm sensitivity for 8Mbps data rate while consuming 639μW power. A ring-type voltage-controlled oscillator based frequency synthesizer is proposed in [33]. Thanks to the injection locking and frequency tracking loop techniques, the frequency synthesizer achieves -115dBc/Hz in-band phase noise and 370μW power consumption. However, despite the achievements, there are still some challenges in the design of the communication unit.

First, frequency tunability is highly desired for the receiver to adapt different IoT application scenarios and standards, but it's challenging to design a low power frequency tunable receiver [37]-[42]. The core component for tunable receivers is bandpass filter

whose center frequency can be easily changed. One solution is to use an array of dedicated, bulky, off-chip and non-tunable filters such as surface acoustic wave (SAW) filters [43]-[45]. However, such off-chip solution may take considerable amount of area. State-of-the-art research proposes some on-chip solutions such as LC filters [46]-[49] and G_m-C filters [50]-[53]. However, LC filters suffer from low quality factor due to the inductor and limited tunability due to the varactor, while G_m-C filters need to trade off among power consumption, quality factor and center frequency and they usually require additional tuning circuitry. Thus, direct tunable integrated bandpass filter with high *Q* factor is critical for the tunable receiver design.

Second, it's hard to design a frequency synthesizer achieving low power consumption and large locking range simultaneously. As the frequency synthesizer needs to provide local oscillation frequency to the tunable receiver, it needs to cover a large frequency range based on the receiver requirement. There are two commonly used techniques for the frequency synthesizer, i.e., phase locked loop (PLL) and injection locking (IL). The PLL based synthesizer has the potential to cover a larger frequency range at the cost of more complicated structure as well as more power consumption [54]-[57]. On the other hand, the IL based synthesizer is easier to implement but it suffers from limited locking range [58]-[60]. Recently, multi-phase injection technique is proposed to enlarge the locking range [61]-[65] and a 23.6% locking range with center frequency at 14.85GHz has been achieved, but it requires accurate phase control of the injected signal, which in turn needs more sophisticated control circuits and higher power consumption, i.e.,

1.56mW [63]. Thus, a frequency synthesizer with low power consumption and large locking range is desired.

Except the two specific requirements for the communication unit of IoT wireless sensor, other general requirements shall also be taken into consideration, i.e., high sensitivity for the FSK receiver and low phase noise for the frequency synthesizer.

Another aspect for the wireless sensor which we will focus on and try to make it generally adaptive is the power management unit (PMU). As discussed, batteries are the conventional choice, but it requires charge or change regularly and occupies large area, which translates to high cost in some IoT applications as the location of the sensors are widely spread and hard to reach. As the power consumption of the sensor interfaces have been reduced dramatically thanks to the recent advance in CMOS technology, powering the sensors by environmental energy harvesters becomes possible [66]-[68].

To harvest environmental surrounding energy, several different kinds of energy harvesters have been applied, such as photovoltaic energy harvester, vibration energy harvester, RF energy harvester and thermoelectric energy harvester [69]-[72]. The features are concluded in Table 1-1-1, including the typical output impedance of the energy source, the typical output voltage and power as well as the main design challenges [73]-[76]. The energy source shall be selected according to the application requirement, such as the availability of the energy, the chip area and power budget, etc. In [77], a multi-input dual-output architecture is proposed to harvest energy from photovoltaic, thermoelectric and piezoelectric all at the same time with a single inductor. Even though such system is more

reliable due to multiple energy sources, the sharing inductor and complicated control block limits the overall energy efficiency. Actually, most of the researchers focus on the harvester design and optimization for a single energy source.

Table 1-1-1. Features for different types of energy harvester [73]-[76]

Energy Source	Challenges	Typical Electrical Impedance	Typical Voltage	Typical Power Output
Light/Solar	Conform to small surface area; Wide input voltage range	Varies with light input: Low kΩ to tens of kΩ	DC: 0.5V to 5V (Depends on number of cells in array)	10μW – 15mW (Outdoors: 0.15mW – 15mW Indoors: <500μW)
Vibrational	Variability of vibrational frequency	Constant impedance tens of kΩ to hundreds of kΩ	AC: tens of volts	1 μW – 20mW
Thermal	Small thermal gradients; Efficient heat sinking	Constant impedance: 1Ω to hundreds of Ω	DC: tens of millivolts to volts	0.5mW – 10mW (20ºC gradient)
RF & Inductive	Coupling & rectification	Constant impedance Low kΩ	AC: Varies with distance and power 0.5V – 5V	Wide range

After the selection of energy source, a regulator, usually a DC-DC converter, is needed to regulate the output voltage and power so that provides stable voltages to different units in a sensor. According to different energy source, there are various requirements for the regulator. For example, for vibrational and RF energy, a rectifier is necessary before the DC-DC converter [78][79], while for thermoelectric energy, a low voltage start up

circuit is mandatory [80]-[82]. And there are also some common considerations regardless the energy sources, such as maximum power point tracking (MPPT), reducing conduction loss, switching loss and power optimization for the control block [83][84].

In summary, this research will focus on the design of wireless communication circuits, i.e., receiver and frequency synthesizer, and autonomous power management unit for wireless sensor in IoT applications, aiming to solve the challenges described above.

1.2 Research Objectives and Dissertation Outline

The objectives of this research are set as follows based on the discussion in Section 1.1.

For the communication unit, a low-power, frequency tunable FSK receiver shall be implemented with the help of a fully integrated, center frequency tunable band-pass filter. This filter will make our receiver be able to handle the RF input signals located in different frequency bands, especially for FSK modulation schemes. Secondly, we need to design a low-power low-phase-noise frequency synthesizer with large locking range to provide an accurate reference clock signal to the receiver.

For the power unit, we need to design a power management unit (PMU) which can provide a regulated stable output voltage. Meanwhile, it should have MPPT function and the energy conversion efficiency should be optimized.

In this research, we proposed several techniques to achieve these goals, and the rest of the dissertation is organized as follows.

The literature review and current research progress on FSK receivers, frequency synthesizers and energy harvesters are presented in Chapter 2.

In Chapter 3, a novel 4-path filter based tunable FSK receiver is presented. We have derived the transient response of the 4-path filter with two-tone inputs and this can help us to determine the maximum achievable data-rate. A fully integrated tunable FSK receiver based on 4-path filter has been implemented in 0.13μm CMOS process. The chip occupies 300 x 700μm^2, achieves data rate of 2.5Mbps, and 74pJ/bit Energy per Bit at -65 dBm sensitivity [85].

In Chapter 4, we present a novel frequency synthesizer based on 4-path mixer and injection-locking. The proposed frequency synthesizer has a two-step tracking mechanism. The first step (coarse tracking) is accomplished by the 4-path mixer and the second step (fine tracking) is done by the injection-locking technique. The tracking ranges of the two steps are also analyzed. This design is implemented in 0.18μm CMOS process. The core circuit occupies 220μm x 190μm. The simulation results show that it can successfully lock the output frequency at 4440MHz of a free-running 3 stage ring oscillator with a power consumption as 305μW. The phase noise at 1MHz offset is -124.86dBc/Hz and it is -97.45dBc/Hz at 100kHz offset. And the integrated RMS jitter from 10kHz to 40MHz is 2.5ps.

In Chapter 5, a boost converter with high efficiency for thermo-electrical energy generator (TEG) is presented as an example for the energy harvester PMU design for wireless sensor. An on-time calibration based pulse skipping modulation (OTC-PSM) scheme is proposed to reduce the power of the controller. A hardware-efficient maximum power point tracking (MPPT) circuit is introduced for the constant internal resistance

source of TEG. The proposed design has been implemented in a standard 180nm CMOS process, achieving a high efficiency of 83.9% at 120mV input voltage and output power of 600μW. The proposed OTC-PSM scheme saves considerable power in achieving 83.9% efficiency as well as low output ripple as 5mV. Also, the proposed MPPT is simple and easy to implement for low cost [86].

The conclusion and considerations for future works are given in Chapter 6.

Chapter 2
Literature Review

In this chapter, we present the literature reviews of the communication unit and power management unit for IoT wireless sensors. In Section 2.1, reviews for receiver and frequency synthesizer are given. In Section 2.2, thermoelectric energy harvesting systems are reviewed. The summary is given in Section 2.3.

2.1 Reviews of the Wireless Communication Unit

The objectives in section 1.2 indicate that we need to design an FSK receiver and a frequency synthesizer for the communication unit of the wireless sensor. We present literature reviews for receiver and frequency synthesizer in this section.

2.1.1 Wireless Receivers for IoT Sensors

The first consideration for receiver design in IoT wireless sensors is reducing the power consumption. Therefore, simple modulation schemes are widely used in such applications, like OOK and FSK. The demodulators for them need less functional blocks and are easier to save power [87]-[92]. Meanwhile, the sensitivity and data rate of the receiver should also be optimized while maintaining low power consumption. Comparing to OOK, FSK shows better transmission efficiency and noise immunity. Thus, it attracts more and more attention from the researchers. Several novel techniques are proposed to save power of the FSK receiver while keeping a good sensitivity and data rate, such as injection-locking

frequency-to-amplitude converter [93]-[96], wake-up mechanism [97]-[101], digitally calibrated injection locking oscillator [102][103], etc. In this section, we review some state-of-the-art techniques for FSK receiver.

In [93], an ultra-low power ISM band RF receiver for IoT devices is proposed. Its overall architecture is shown in Fig. 2-1-1.

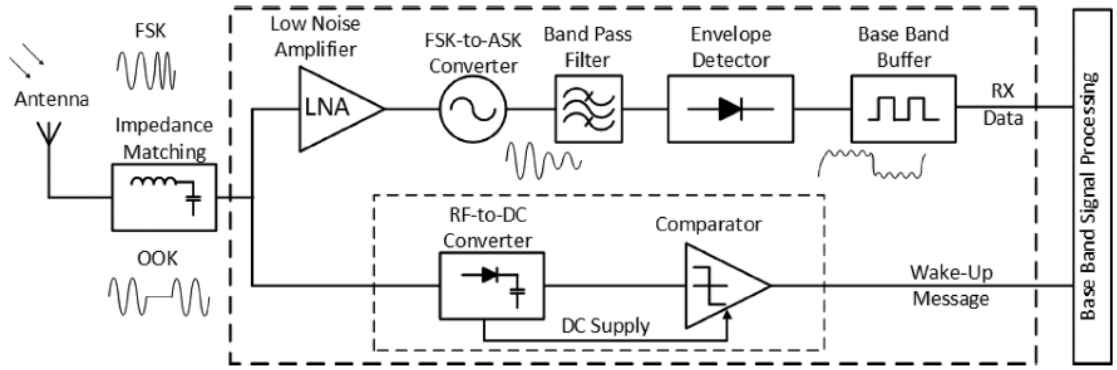


Fig. 2-1-1 Architecture of 902-928 MHz ISM band RF receiver [93]

The receiver is composed of two channels, a primary communication channel and a secondary wake-up receiver channel. During standby period when no data is communicated, the primary channel is disabled, and the ultra-low-power secondary channel will wake up the primary channel when a wake-up message is detected. The primary receiver demodulates FSK signal. The received FSK signal is firstly amplified by the low-noise-amplifier (LNA) and then the amplified signal is fed into the frequency-to-amplitude converter (FAC). Through the FAC, the frequency difference is converted to amplitude difference and the signal is now amplitude shift keying (ASK) modulated. Challenges for ISM receivers are mainly the noise and the interferences, thus, a narrow

BPF is used to further remove the out-of-band blockers and to improve the frequency selectivity of the receiver. Envelope detector and baseband buffer are applied to obtain a demodulated data. The proposed receiver can handle FSK signals with high data-rate of several mega bits per second (bps). Thanks to the FAC, an easily implemented ASK receiver can be used. And such topology successfully eliminates the need of a local oscillator and I/Q signal path, which requires more circuit components and more power. In addition, the FAC also provides additional gain to the signal and this can relax the design requirement for the LNA.

In [97], a 0.45V low-power receiver which utilizes a wake-up mechanism to adjust its power consumption automatically is proposed. The receiver architecture is shown in Fig. 2-1-2.

This receiver consists of a multiple-gated low-noise amplifier (MGLNA), a wake-up circuit (WUC), a folded semi-passive sub-harmonic mixer (FSPSM), a variable-gain amplifier (VGA), a dual-mode demodulator (DMD) and a single-to-differential circuit (SDC).

Because the receiver works under 0.45V supply, which is lower than the normal threshold voltage of the CMOS transistor, the forward body biasing is applied to every transistor in order to lower the threshold voltage. WUC is used to detect the RF signal amplitude and to further control SCM to adjust the power consumptions of other blocks automatically. The noise figure of the overall receiver is mainly determined by the MGLNA, which is the first stage. In addition to the high gain for the purpose of good noise

performance, the MGLNA also adopts a linearity-improving technique, which is important because poor linearity may lead to the WUC to generate wrong control signal. Besides, the gain of the MGLNA can help to improve sensitivity of the WUC. The output of FSPSM is fed into the VGA, whose voltage gain is adjusted by an off-chip ADC and an MCU. After amplification by the VGA, the signal can be demodulated by the DMD.

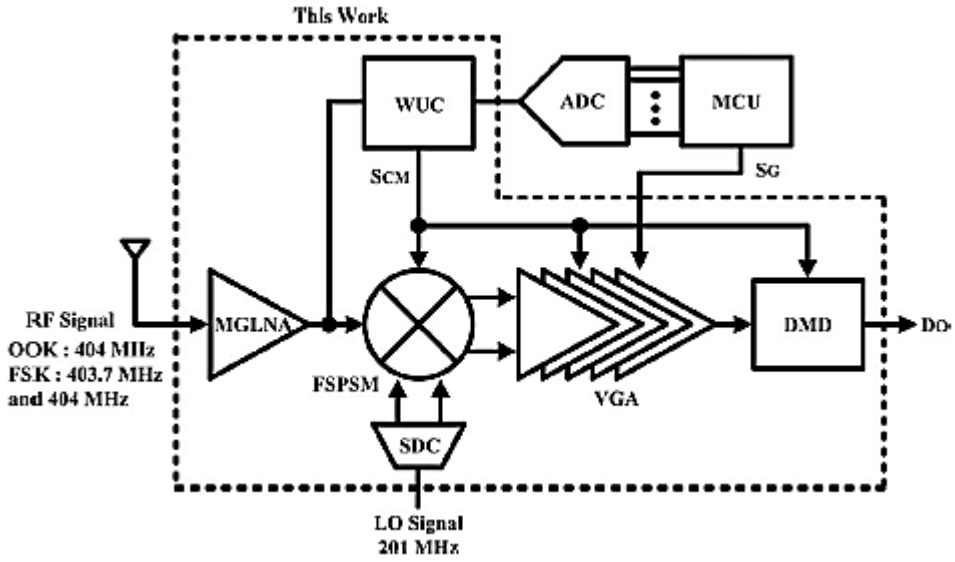


Fig. 2-1-2 The block diagram of 0.45V OOK/FSK receiver [97]

A dedicated ultra-low power fully integrated FSK wake-up receiver (WuRx) for wireless body area network is proposed in [102]. Fig. 2-1-3 shows its overall architecture.

The core blocks of this WuRx are front-end circuits, an injection-locking digitally controlled oscillator (IL-DCO), an envelope detector, baseband circuits and an auto-calibration loop with a successive approximated register (SAR) controller. The IL-DCO is most critical as it can convert the frequency difference to the amplitude difference and

provide some amplification gain at the same time. In addition, by locating it between the front-end circuits and the envelop detector, it acts as an isolator to reduce the noise effect from the envelope detector to the front-end. The receiver operates in two modes, i.e., receiving mode and calibrating mode, according to whether the received signal is FSK modulated or not and whether the closed loop for frequency calibration is activated or not.

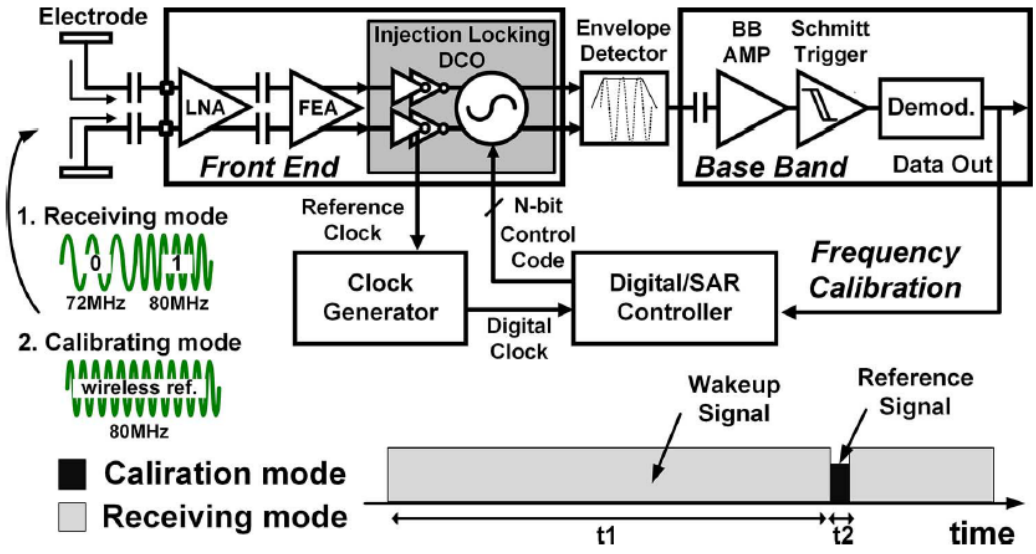


Fig. 2-1-3 Architecture for 45μW injection-locked FSK WuRx [102]

As depicted in Fig. 2-1-3, the receiving mode happens during the time period of t_1. The input signal is FSK modulated, whose frequencies are 72 MHz and 80 MHz with a data rate as 312 kb/s. The input signal is firstly amplified by the front-end circuits and then is fed into the IL-DCO. The locking range of the IL-DCO is centered at 80 MHz and therefore, it will be injection-locked by the 80 MHz and be injection-pulled by the 72 MHz. As a result, the two frequencies will have different amplitude and the signal is now like an

ASK signal. Then, the envelope detector takes the ASK signal as input and remove the carrier frequencies. The baseband circuits further amplify the amplitude difference, and as a result, a demodulated RX signal can be obtained. In this mode, the calibration signal is not valid, and the digital/SAR controller doesn't work.

On the other hand, in the calibrating mode during the time period of t_2, the input signal is an accurate 80 MHz sinusoidal signal. And the frequency calibration loop is enabled to tune the oscillation frequency by changing the control code of the IL-DCO. Ideally, the IL-DCO should be locked at 80 MHz after the calibration is finished.

From above review, we noted that the core block for an FSK receiver is the frequency-to-amplitude converter. [93] and [102] implement such converter with injection locking oscillator, however, the limited locking range of the oscillator requires that the two carrier frequencies should be located at a distance, otherwise, the carrier frequencies will be both injection locked and no data can be extracted. And this means more bandwidth occupancy for FSK modulation. [97] achieves the frequency-to-amplitude conversion by using mixer, however, such approach needs further processing by the VGA and ADC.

Actually, the most convenient way of converting the frequency difference to amplitude difference for FSK demodulation is to use a high-*Q* bandpass filter centered at one of the carrier frequencies. However, such method is less attractive for integrated solution due to the limitations of the bandpass filter, either off-chip (SAW filter) or on-chip (LC filter and G_m-C filter), as discussed in Chapter 1. Fortunately, N-path filter, which is composed of multiple identical low-pass filters and switches, is a promising candidate

to satisfy the requirements for on-chip band-pass filter to serve as the frequency-to-amplitude converter in FSK demodulation. N-path filters have interesting features such as direct tunability with the switching frequency, potential higher *Q*-factors, high linearity and graceful scaling with process [104]-[115].

The concept of N-path configuration was firstly proposed by [116] in 1960 and its architecture is shown in Fig. 2-1-4.

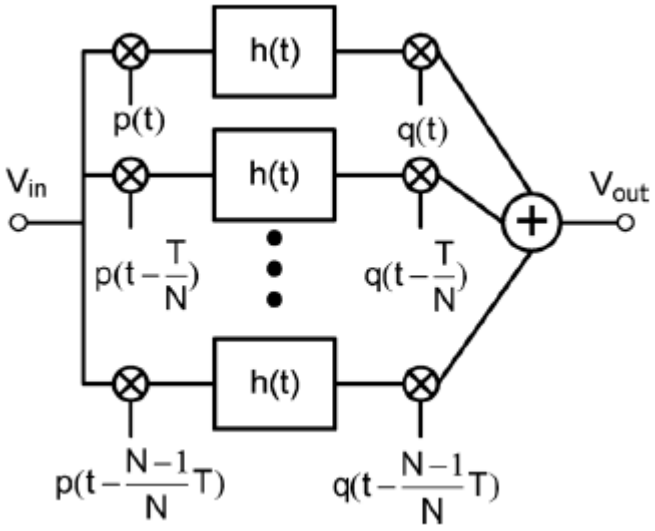


Fig. 2-1-4 Architecture of N-path filter [116]

The N-path filter is composed of *N* identical linear time-invariant (LTI) blocks whose impulse response is $h(t)$ and $2N$ frequency mixers, which are driven by time shifted clocks $p(t)$ and $q(t)$. For two adjacent branches, the shifted time is N/T, where T is the period of mixer clock.

Let the LTI block be a low-pass filter, the general N-path filter will behave as a band-pass filter with center frequency as mixing frequency. Actually, the first series of mixers who are driven by $p(t)$, $p(t\text{-}T/N)$, …, $p(t\text{-}(N\text{-}1)T/N)$ are used to down-convert the input signal to baseband from its original band, which can be at a high frequency. Then the LTI block or low-pass filter will process this signal and another series of mixers driven by $q(t)$, $q(t\text{-}T/N)$, …, $q(t\text{-}(N\text{-}1)T/N)$ will up-convert it back to its original band. The combination of a high mixing frequency and a narrow low-pass filter bandwidth will return a very high Q of this kind of N-path band-pass filter.

In Fig. 2-1-5(a), we replace the LTI block and mixer with RC low-pass filter and MOS switches respectively. Fig. 2-1-5(c) shows the multi-phase clocking scheme for the switches, and it's clear that the on-time for switches in different branches should be non-overlapping. Ideally, there should not be any moment in which the capacitors can share charge. Due to this fact as well as the memory-less property of resistors, we can simplify the circuit in Fig. 2-1-5(a) to Fig. 2-1-5(b), where only one resistor is used and shared with all the N branches. Moreover, since the clocks for switches S_{n1} and S_{n2}, where $1 \leq n \leq N$, are the same, so we can use only one series of switches to realize the functions of two as shown in Fig. 2-1-5(b) and the output will be available between the shared resistor and the switches [117].

Since the switches in N-path filter are non-overlapping, one and only one capacitor is connected to the output node at any moment. Assuming that $RC >> T_s/N$, during each time interval T_s/N, the output voltage V_{out} will be the average of the input voltage V_{in}. If the

input frequency is the same as the switching frequency, for a certain branch, the same part of input voltage will be averaged by the same RC circuit for every period. Thus, the output will be stable and is a staircase approximation as shown in Fig. 4(d) (assuming that N=4). In this case, the average voltage across each capacitor for different period keeps the same. Therefore, the capacitors conduct no current. However, if the input frequency f_{in} is not the same as the switching frequency f_s, for a single capacitor, the average voltage across it will change period by period, and its beat frequency is given by $\Delta f = |f_{in} - f_s|$. Thus, the capacitors conduct current while switches are on and the average voltage on the capacitors will tend to zero. Therefore, input signals whose frequency is above or below the switching frequency will be suppressed.

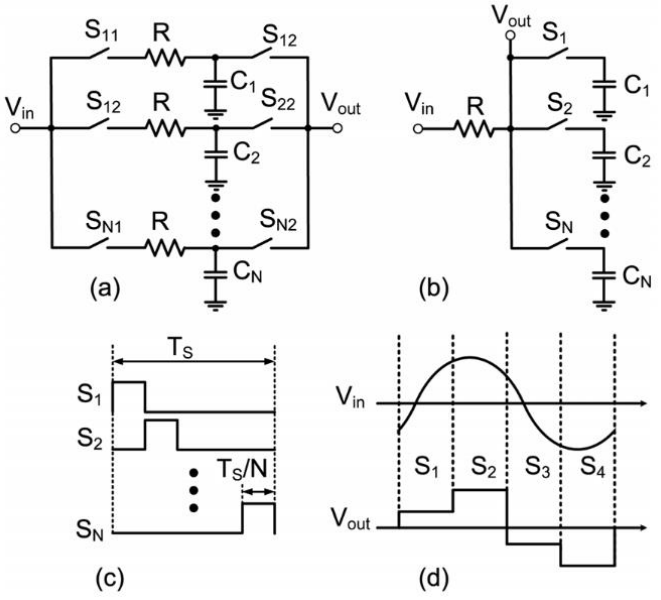


Fig. 2-1-5 (a) Switched-RC N-path filter. (b) Single port, single ended N-path filter. (c) Multiphase clocking. (d) Typical input and output signal [117]

Based on the above analysis, N-path filter has some very attractive features, which make it a good choice in wireless transceivers. It can achieve very good frequency selectivity by simply increasing the sharpness of the low-pass filter. Its center frequency is easy to be tuned by changing the switching frequency and it is easy to be fully integrated as no inductor is needed.

Although most frequencies different from switching frequency can be filtered out by N-path filter, the input signals around the harmonics of switching frequency can't be eliminated by the configuration in Fig. 2-1-5. To cancel the even harmonics, we can apply the differential structure as shown in Fig. 2-1-6(a).

With this architecture, for input signals around the even harmonics of the switching frequency, no net charge is stored on the capacitor in the steady state and no up-converted signal appears at the output node. To investigate other characteristics of the frequency response of the N-path filter in order to guide the design [29, 34-53], the complete output spectrum of differential N-path filter can be given by (2-1-1) to (2-1-4) [117]-[119].

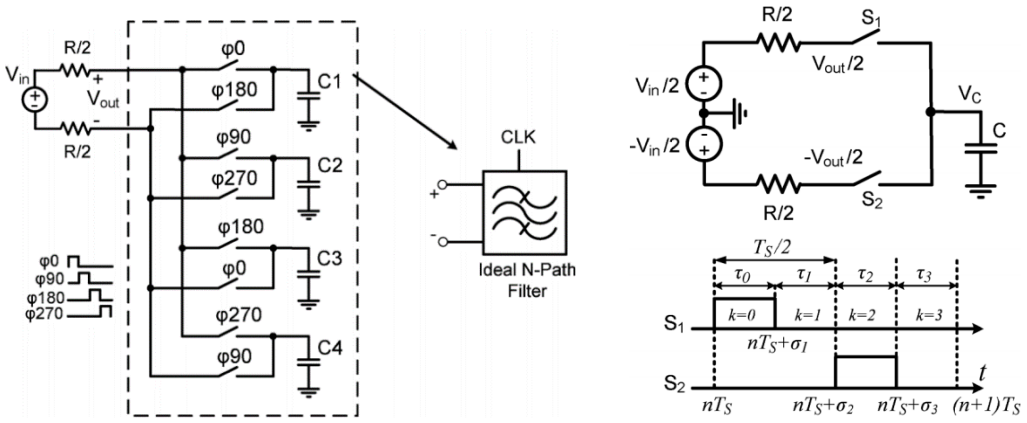
$$V_{out}(f) = \sum_{n=-\infty}^{\infty} H_n(f) V_{in}(f - nf_S), \tag{2-1-1}$$

$$H_n(f) = \sum_{m=0}^{N-1} exp(-j2\pi n\sigma_m f_S) H_{n,m}(f), \tag{2-1-2}$$

$$H_{n,m}(f) = \frac{1}{1+\frac{jf}{f_{rc}}}\left(\left(\frac{1-exp(-j2\pi n\tau_m f_S)}{j2\pi n}\right) + \frac{1+exp(-j2\pi\tau_{m+1}(f-nf_S)-j2\pi n\tau_m f_S)}{\frac{2\pi f_{rc}}{f_S}} G_{0,m}(f)\right), \tag{2-1-3}$$

$$G_{0,m}(f) = -\frac{exp(j2\pi\tau_m(f-nf_S))-exp(-2\pi\tau_m f_{rc})}{exp(\frac{j\pi(f-nf_S)}{f_S})+exp(-2\pi\tau_m f_{rc})}\frac{1}{1+\frac{j(f-nf_S)}{f_{rc}}}, \quad (2\text{-}1\text{-}4)$$

where $f_{rc} = (\pi RC)^{-1}$, which is the 3-dB bandwidth of a single low-pass filter composed of resistor *R*/2 and capacitor *C* (as shown in Fig. 2-1-6(b)). Also, according to Fig. 2-1-6(b), $\tau_{m+1} = T_s/2 - \tau_m$ for each path and $\sigma_m = \sum_{n=0}^{m-1}\tau_n$.



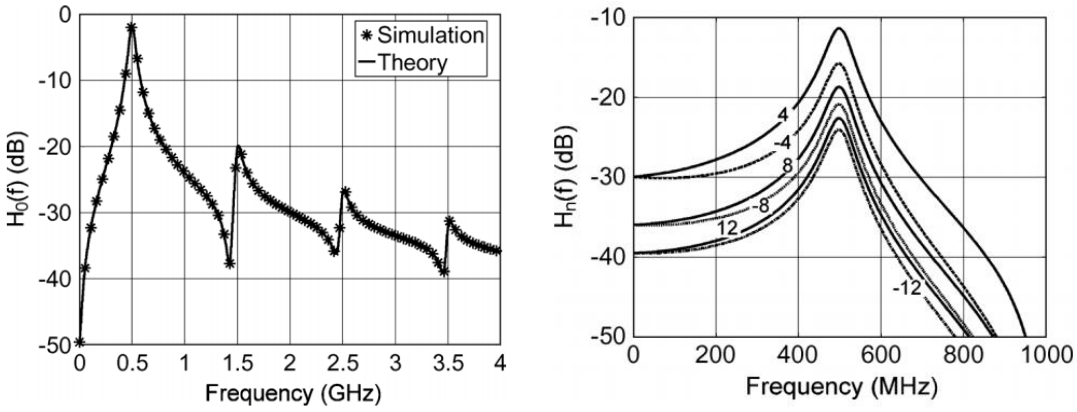
(a) (b)

Fig. 2-1-6 (a) Single port differential 4-path filter (b) Kernel model for (a)

$H_0(f)$ is the desired filtering characteristic without any translation. However, according to (2-1-3), it's not defined, and we can only derive its expression by taking the limit of $H_n(f)$ when *n* approaches continuously to zero. Moreover, in (2-1-3), we assume that the switches for different branches are on continuously, i.e. $\tau_0 = \tau_1 = \cdots = \tau_{n-1} = DT_s$.

Fig. 2-1-7(a) shows the theoretical and simulated curves of $H_0(f)$ in the case where $N = 4$, $D = 1/4$, $R = 100\Omega$, $C = 50$pF and $f_s = 500$MHz and it's clear that the expression can

reflect its characteristic very well. Thanks to the differential architecture, peaking around even harmonics does not occur, however, there are still response peaks around odd harmonics of the switching frequency.



(a) (b)

Fig. 2-1-7 (a) Theoretical and simulated curve for $H_0(f)$ (b) $H_n(f)$ around the switching frequency for a 4-path filter

Now we consider $H_n(f)$ for $n \neq 0$, according to (2-1-2), $H_n(f)$ equals to 0 except the cases when $n = 0, \pm 1, \pm 2, \cdots$ Fig. 2-1-7(b) shows the curves for $H_n(f)$ around the switching frequency with different values of n.

As can be seen from Fig. 2-1-7(b) and taking (2-1-1) into consideration, input frequencies around $k(N\pm1)f_s$ will "fold back" to the desired band around f_s. In general, increasing the number of paths will increase the distance between f_s and the first folded component around $(N\text{-}1)f_s$.

For N-path filter, at any moment there are two switches in the on-state and their noise contributions are not correlated. Thus, we can use the model in Fig. 2-1-8 to analysis the noise voltage.

For Fig. 2-1-8(a), we can find the expression of the thermal noise due to *R*:

$$N_{out,R}(f) = \left|\frac{2R_{SW}+RH_0(f)}{R+2R_{SW}}\right|^2 N_R(f) + \sum_{n=-\infty,n\neq 0}^{\infty} \left|\frac{R}{R+2R_{SW}} H_n(f)\right|^2 N_R(f-nf_S). \quad (2\text{-}1\text{-}5)$$

The first term accounts for the noise power, which appears at the output without any frequency translation, and the second part accounts for noise folding, where $N_R(f-nf_s)$ is the frequency-shifted version of the noise power generated by *R*.

For the circuit in Fig. 2-1-8(b), we can similarly derive the output noise power due to switch resistance:

$$N_{out,SW}(f) = \left(\frac{R}{R+2R_{SW}}\right)^2 \left(|H_0(f)-1|^2 N_{SW}(f) + \sum_{n=-\infty,n\neq 0}^{\infty} |H_n(f)|^2 N_{SW}(f-nf_S)\right). \quad (2\text{-}1\text{-}6)$$

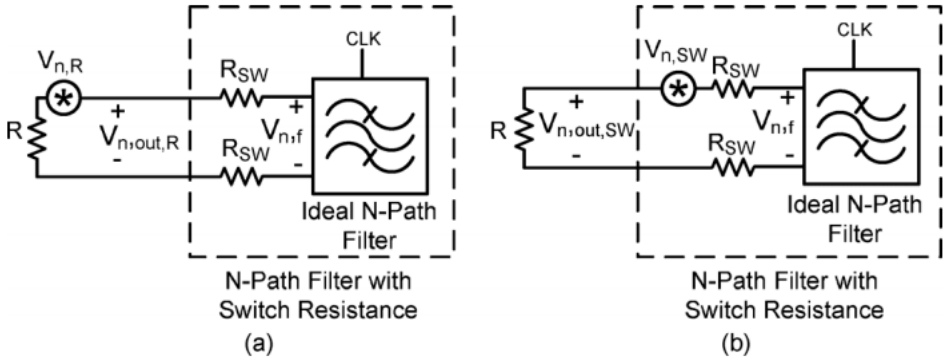


Fig. 2-1-8 The model for noise calculation. (a) Source noise (b) Switch resistance noise

Again, the first part of (2-1-6) corresponds to the noise power without frequency translation. Since $H_0(f)$ is close to 1 around the switching frequency for an N-path filter, the contribution of the first part is very small. The second part is the noise folding term and turns out to be almost negligible. Finally, the noise factor can be calculated by $F = N_{out}/(A_v^2 N_{in})$ and is mainly determined by the noise coming from the source resistance R.

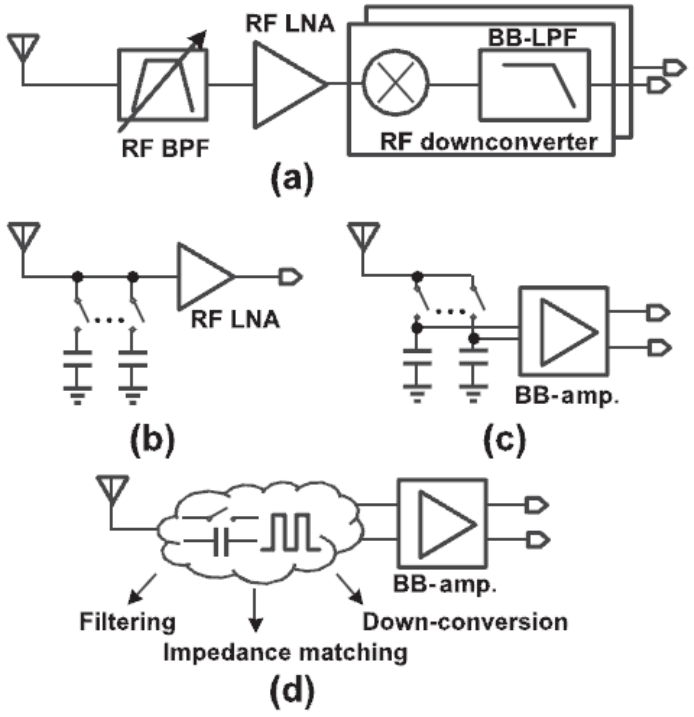


Fig. 2-1-9 (a) Wideband RX with an off-chip RF bandpass filter (b) Wideband RX front end with an N-path filter at the RF input (c) mixer-first RX front end (d) Switched capacitor RX front end

Fig. 2-1-9 gives several different ways to apply N-path filter in the wireless receiver design. In Fig. 2-1-9 (b), an N-path filter is located before the LNA, which can attenuate

RF input blockers, but the stop-band rejection is limited by the switch-on resistance due to the single-port architecture of the filter [120][121]. In mixer-first RXs as shown in Fig. 2-1-9 (c), the stop-band rejection is no longer an issue because the active amplifiers are attached to capacitors. But the bandwidth of the baseband (BB) amplifier may need to be large, which leads to high power consumption [122]-[126]. In Fig. 2-1-9 (d), the authors in [127] proposed a switch capacitor front end where the high-order filtering is achieved by linear passive switch capacitor (SC) circuits.

Another example of the N-path filter based receiver is [128]. The overall structure is depicted in Fig. 2-1-10(a), noting that this is a single-ended version. The front end is composed of eight RF SC branches, baseband G_m cells and trans-impedance amplifiers. All the switches are driven by an eight-phase, non-overlapping clock signal $p<i>$ as shown in Fig. 2-1-10(b), noting that i is an integer from 0 to 7. The clock frequency is f_s, and because there are eight non-overlapping phases, the equivalent local oscillator (LO) frequency is $f_{lo}=f_s/8$. At the RF input, an 8-path band-pass filter is realized by the capacitors $C_{h0}<i>$ and the switches $s_0<i>$ in all the eight branches. The N-path first structure can attenuate the out-of-band blockers effectively. After that, impedance matching is realized by capacitors $C_s<i>$, switches $s_1<i>$ and switches $s_6<i>$. Also in this stage, the RF signal is sampled on $C_s<i>$, and a discrete-time signal is obtained. After sampling, history capacitors $C_{h1}<i>$-$C_{h3}<i>$ and the switches attached to those capacitors ($s_2<i>$-$s_4<i>$) together with $C_s<i>$ and $s_6<i>$ form another high-order discrete-time infinite-impulse-response filter and

the output of this filter is provided to the baseband G_m cells. The G_m cells down-converters the filtered signal and the TIA outputs the signal after proper amplification.

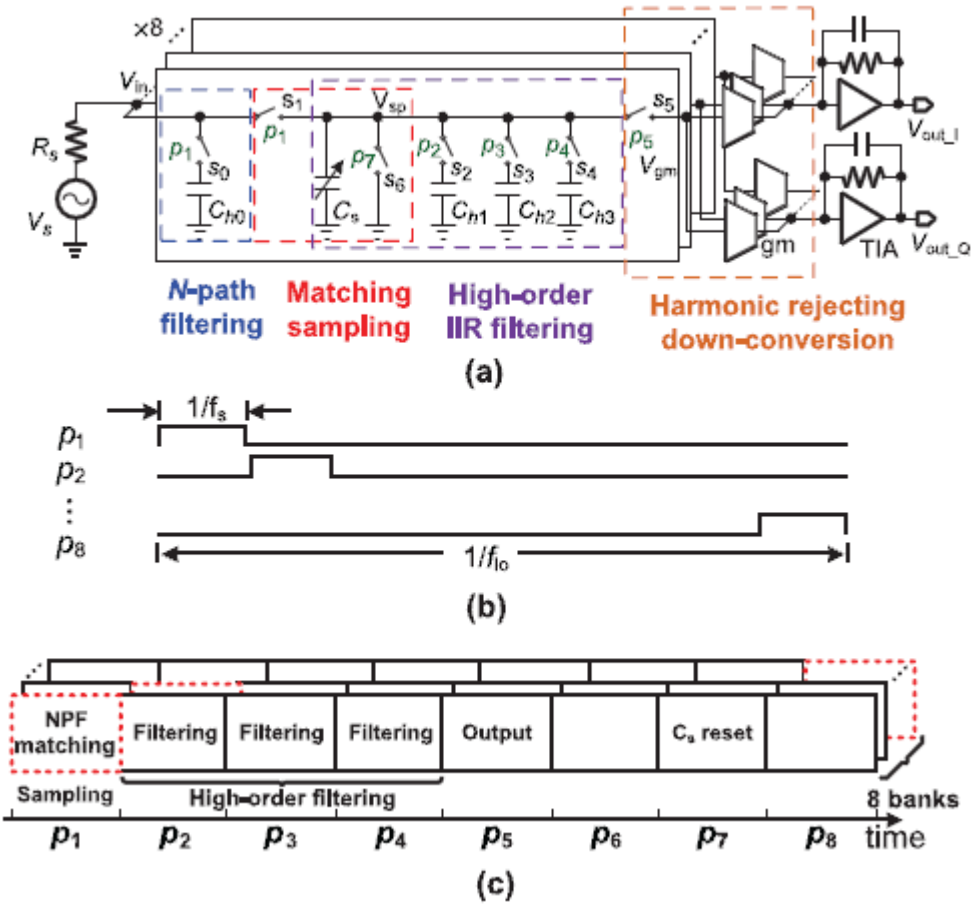


Fig. 2-1-10 (a) Simplified architecture of a single-ended SC RF front end (b) Clock waveform (c) Operation of the SC RF front end [128]

As discussed before, such SC front end achieves different circuit functions according to the on-off status of the switches, and Fig. 2-1-10 (c) shows the function sequences. Taking the first branch as an example, the RF signal is sampled on C_s in sampling phase p_1, propagated to the G_m input node in p_5, and zeroed to ground in p_7. From

p_2 to p_4, the signal is filtered with increasing order. The blank time intervals relax the timing constraints, and the eight banks operate in a time-interleaved manner.

The authors in [128] successfully prove that SC circuits can be applied in the generic RF receiver structure. And this further motivates us to apply the N-path filter in FSK demodulator for IoT wireless sensors to achieve a low power frequency tunable receiver as given in Chapter 3. Table 2-1-1 summarizes the performance for state-of-the-art low power FSK receiver publications, and we can see that the tunability is a common issue. Other than that, our design also aims to maintain a good sensitivity and energy per bit.

Table 2-1-1 Performance summary of state-of-the-art FSK receiver

Reference	[93]	[96]	[97]	[98]	[101]	[102]
Technology(μm)	0.13	0.18	0.18	0.065	0.04	0.18
Supply(V)	1.2	1	0.45	0.75	0.95	0.7
Modulation	FSK	FSK	FSK	GFSK	FSK	FSK
Sensitivity(dBm)	-78	-78	-69	-58	-90	-62
Frequency(MHz)	902-908	433	402-405	2400	5800	72-80
Tunability	No	No	No	No	No	No
Data Rate(Mbps)	8	0.2	0.12	1	0.0625	0.312
Power Consumption(μW)	639	54	352	164	490	45
Energy per bit(nJ/bit)	0.08	0.055	1	0.164	7.8	0.14

2.1.2 Low-Power Frequency Synthesizers

A frequency synthesizer can generate a range of accurate frequencies from a single reference frequency, and the ratio between them can be either integer or fractional number. There are several different techniques for the design of frequency synthesizer, such as

direct digital synthesis, frequency multiplication, frequency division, frequency mixing and PLL. Currently, the PLL-based frequency synthesizer is the most commonly used structure and there are many researchers focusing on this area. Fig. 2-1-11 shows the basic structure of the PLL-based frequency synthesizer [129].

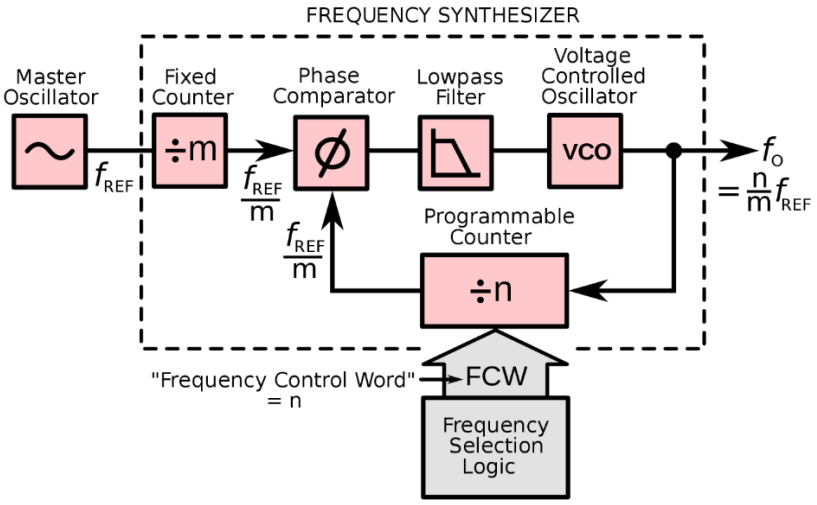


Fig. 2-1-11 Structure of a PLL-based frequency synthesizer

The core of the frequency synthesizer shown in Fig. 2-1-11 is the phase comparator. It compares the phases of two input signals and produces an error signal that is proportional to the difference between their phases. The error signal is then low pass filtered and used to drive a voltage-controlled oscillator (VCO) which creates an output frequency. The output frequency is fed through a frequency divider back to the input of the system, producing a negative feedback loop. If the output frequency drifts, the phase error signal will increase, driving the frequency in the opposite direction in order to reduce the error.

Thus, the output is locked to the frequency at the other input. This other input is called the reference and is usually derived from a crystal oscillator, which is very stable in frequency.

In practice this type of frequency synthesizer cannot operate over a very wide range of frequencies, because the comparator will have a limited bandwidth and may suffer from aliasing problems. This would lead to false locking situations, or an inability to lock at all. In addition to the locking range problem, power consumption is another major concern for the design of frequency synthesizer. There are many attempts trying to solve these issues [130]-[134].

In [131], the authors proposed a 0.5 V, 440 μW frequency synthesizer and its architecture is shown in Fig. 2-1-12.

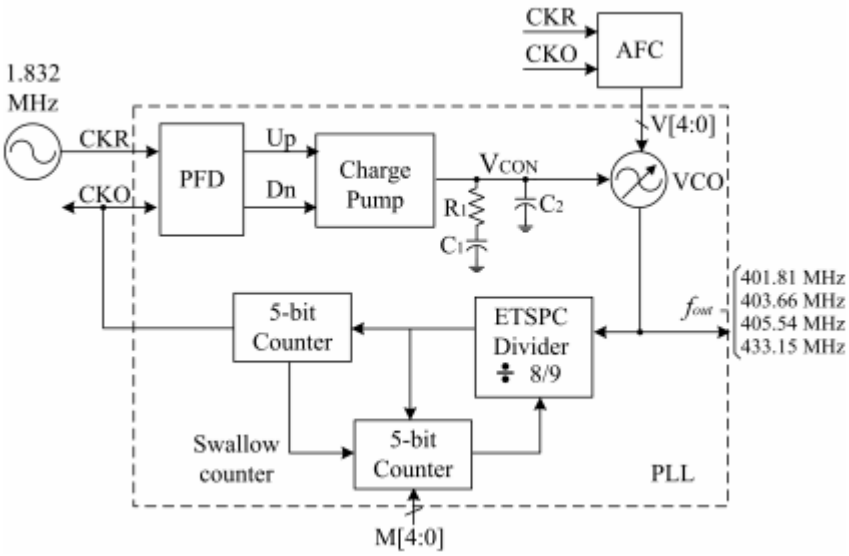


Fig. 2-1-12 Architecture of a 0.5V, 440μW frequency synthesizer [131]

The frequency synthesizer is composed of a dynamic phase-frequency detector (PFD), a charge pump (CP) with low static power and high output current, a low-power ring-based VCO, a frequency divider, an external second-order low-pass filter (LPF) and an automatic frequency calibration (AFC) circuit which is used to compensate the process, voltage and temperature (PVT) variations of the VCO. Due to the limited voltage headroom with 0.5V voltage supply, the nominal threshold voltage transistors or even the low-V_{th} transistors are hard to apply. Thus, the authors adopt dynamic threshold CMOS (DTCMOS) transistors to reduce the V_{th} while maintaining low leakage current. For such transistors, the gate and the body are connected, so the forward body bias voltage can greatly reduce the threshold voltage when the transistors are on. Once the transistors are off, V_{th} returns to its nominal value and the leakage current is limited.

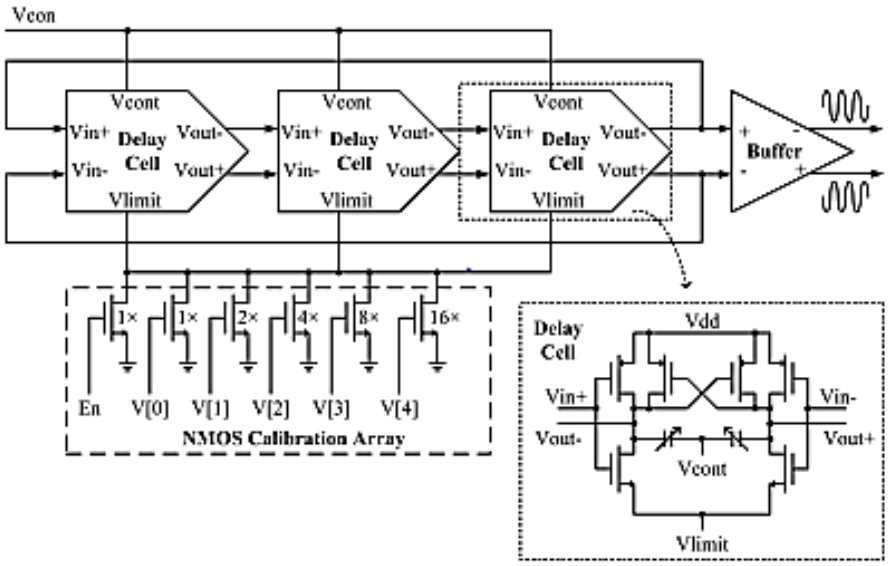


Fig. 2-1-13 Schematic of the VCO in [131]

Fig. 2-1-13 shows the schematic of the VCO, which is a differential ring-based VCO with dual resistor-varactor tuning. The varactors in each delay cell are controlled by the analog signal (V_{CON}) generated from charge pump to fine-tune the frequency generated by the VCO, while an NMOS current biasing array is digitally controlled by 5-bit word to compensate PVT effects.

As the low power design for PLL based frequency synthesizer may require many peripheral and off-chip calibrations, injection locking technique is more and more popular now for frequency synthesizer design. The phenomenon of injection locking happens when a free running harmonic oscillator is disturbed by another oscillator with a close enough frequency. If the coupling from the second oscillator is strong enough, the first oscillator will be forced to operate in the same frequency as the second one [135][136]. Based on this principle, injection-locked oscillator (ILO) can be used to obtain a desired frequency and it is also called injection-locked clock multiplier (ILCM) [137]-[141].

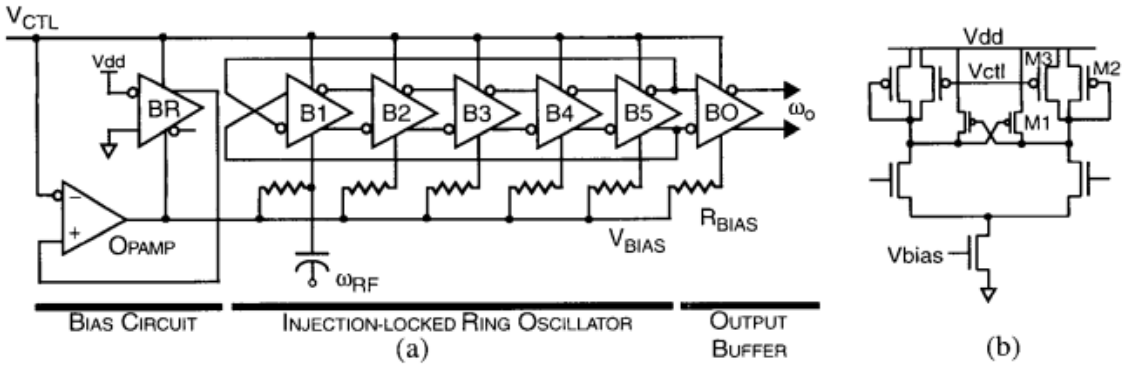


Fig. 2-1-14 Schematic of the (a) 5-stage ring oscillator and (b) differential delay buffer in [139]

In [139], the authors exploited injection-locking in different CMOS ring oscillators as shown in Fig. 2-1-14. The center frequency can be tuned by changing the biasing of the buffers so as the delay through each cell. The delay buffer has a structure of cross-coupled symmetric load as shown in Fig. 2-1-14(b), which has good supply noise rejection and low 1/*f* noise up-conversion characteristics. The RF signal is injected at the tail current source of the first buffer, and the rest of the buffer stages behave as filters to contribute the gain and phase shift required to sustain the oscillation.

Although single-injection oscillator has been proved to be able to provide accurate oscillation frequency, its locking range (LR) is limited. To widen the LR, the idea of multiple injections comes up by injecting multiple properly phase shifted signals into the multiple nodes of the ring oscillator [142]-[147]. It's shown in [xx] that the LR can be widened by a sequence of injection phases which progress with the intrinsic phase delay of a single stage of the oscillator.

Fig. 2-1-15 shows the equivalent model for a three-stage ring oscillator as a 2:1 frequency divider with multiple-input injection, in which the phase difference between the injected signals of the adjacent stages is specified as φ_{inj}. Here, the frequency division is achieved by the multiplication operation provided by the mixer. In [142], the measurement results show that the locking range is increased by a factor of 2.02 and 3.01 for two and three injections, respectively, compared with the single-injection case.

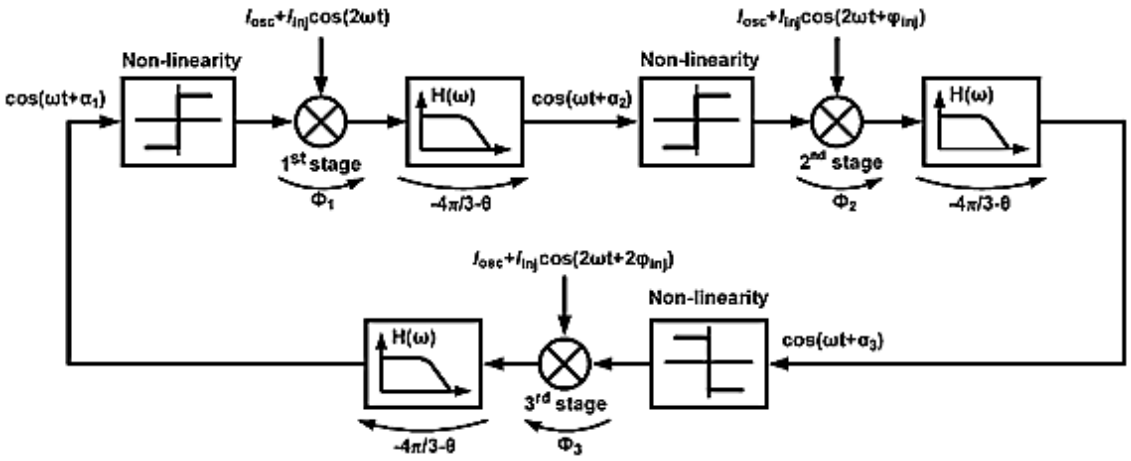


Fig. 2-1-15 Equivalent circuit model for a three-stage ring oscillator with multiple-input injection [142]

Other than the multi-input injection, another way to improve the locking range for ILO is N-path mixer as it has great frequency selectivity, i.e., high-*Q*, as reviewed in Section 2.2.1. Such property can help us to convert the frequency difference to amplitude difference precisely and the complicated frequency tuning can then be done by voltage tuning or digital tuning. Table 2-1-2 summarizes the performance for state-of-the-art ILCM, we can see that the locking range can be enlarged by either applying a larger range of reference frequency [148][149] or different supply voltage [150]. Otherwise, the ILO itself can only provide a very limited locking range as in [151]. In this research, we will keep the reference frequency and supply voltage to be fixed and try to apply N-path technique together with ILO to achieve a wide locking range.

Table 2-1-2 Performance summary for state-of-the-art ILCM

	[148]	[151]	[150]	[149]
Process	90nm	180nm	65nm	65nm
f_{ref}	291MHz~ 336MHz	31MHz	100MHz	105MHz~129MHz
Multiplication Factor	3	13	24	64
Locking Range	873MHz~ 1.008GHz	399.6MHz~ 406.5MHz	2.2GHz~2.5GHz **	6.75GHz~8.25GHz
Power	720μW	107μW	11mW	2.25mW
Integrated RMS Jitter	N/A	N/A	140fs	190fs
Phase noise @ 100kHz	-101 dBc/Hz*	-103 dBc/Hz	-120 dBc/Hz*	-119.2dBc/Hz

* Estimated from the figure

** Achieved by changing the supply voltage

2.2 Reviews for Power Management Unit for Energy Harvester

As discussed in Chapter 1, each kind of energy source has its own limitations and researchers usually optimize the PMU design for a single energy source. In this research, we focus on thermoelectric energy as it is considered as the best candidate to power wearable/portable devices, which is a typical IoT application in people's daily life.

The photovoltaic energy harvester needs to be directly exposed to the light source, which can't be guaranteed in people's daily use. The vibration energy harvester requires constant mechanical movement, and the vibration frequency may change dramatically, which makes it hard to be handled by the harvester circuits. To harvest the RF energy, it

requires that an RF source and antenna/coil are placed near the harvester, which limits people's range of activity.

Comparing to the limits of the energy sources described above, thermoelectric energy is more desired since it can be generated as long as there is temperature difference between the cold and hot junctions of the TEG thanks to the Seeback effect [152]. Fig 2-2-1(a) gives the picture of a real TEG's composition and Fig 2-2-1(b) shows the equivalent circuit model. When it is applied on the human body, one side of the harvester can be placed either on the skin, and the other side is exposed to the cooler ambient air. Then, a continuous input power supply can be obtained [153]-[154]. Thus, it is very suitable for portable/wearable applications. A TEG can be modeled as simple as a voltage source and an internal resistance. The generated voltage is,

$$V_{TEG} = \alpha(T_2 - T_1), \tag{2-2-1}$$

where α is the Seeback coefficient, T_2 and T_1 are the hot side temperature and cold side temperature, respectively. It is worth noting that the internal resistance of a TEG is fixed, meaning that it has the same value no matter what the temperature difference between hot and cold side is.

However, harvesting thermo-electric energy to power electronic devices is facing with challenges. Generally, a TEG working with the temperature difference between human body and ambience may only be able to generate a DC voltage as low as tens of millivolts, which is much lower than the threshold-voltage of the MOSFETs in normal CMOS process. Meanwhile, the output power of TEG is usually hundreds of microwatts

or even lower in portable/wearable applications. To achieve a high efficiency in such a low input voltage and low input power, the startup mechanism [155]-[161] and control strategy [162]-[167] shall be investigated. In addition, the maximum power point tracking (MPPT) technique is a necessity in energy harvesters [168]-[175], which ensures that the harvester can obtain as much power as possible from the energy source.

Fig. 2-2-1 (a) Composition of a TEG. (b) Circuit model of a TEG

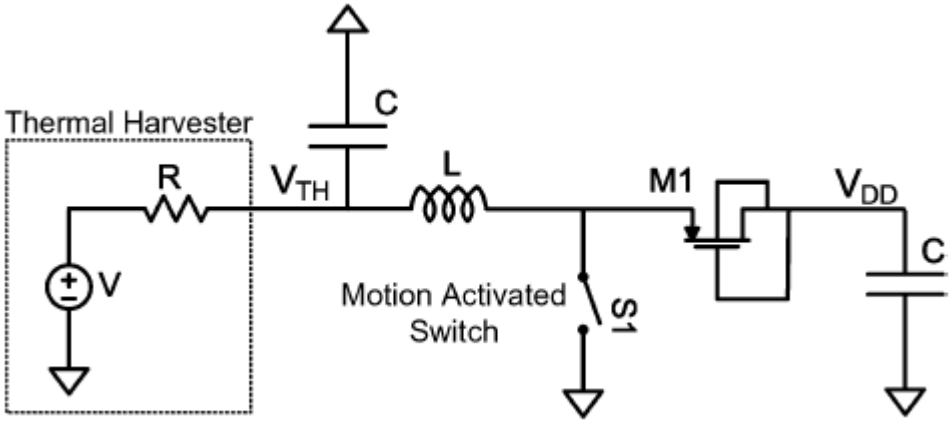


Fig. 2-2-2 The proposed startup circuit in [156]

In [156], a mechanically assisted startup circuit to kick start electrical energy extraction from the TEG is proposed. As shown in Fig.2-2-2, the mechanical switch S1 is turned on and off by the vibrations occurred on the arm or on the body of a person. When S1 is on, a current will flow from the harvester through the inductor to the ground. And after S1 turns off, the stored current in the inductor will force the diode-connected transistor M1 to be on. Thus, energy will eventually be stored in the capacitor C and a high value V_{DD} can be obtained, which can be used to power the control units.

In [160], a transformer-reuse self-startup boost converter is proposed, and its overall architecture is shown in Fig. 2-2-3. Comparing with other commonly used boost converter structure, the proposed converter used a transformer rather a single inductor as the energy transfer device.

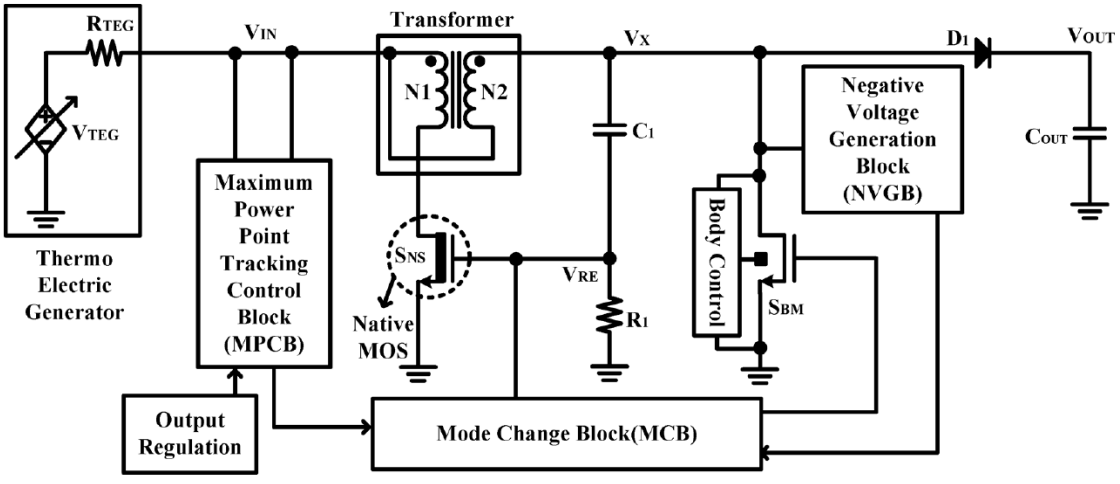


Fig. 2-2-3 Proposed DC-DC converter architecture in [160]

To start up, the authors make use of the noise from the converter. The polarity of the transformer is designed so that the transformer and the native MOS S_{NS} who has a zero-threshold voltage can form a positive feedback loop. The noise of the converter can trigger a small current flowing through S_{NS}, which will generate a small voltage difference across N_1. Then, at node V_X, the voltage is increased by a factor of the turn ratio between N_1 and N_2. Across C_1, this increased voltage will apply back to the gate of S_{NS} and the positive feedback structure makes the oscillation possible. It's shown by the authors that a minimum noise current of 0.3μA is required for the positive feedback loop to have a gain larger than 1.

When V_{IN} is large enough and the Mode Change Block (MCB) determines to change the system operating mode, the gate of S_{NS} will be re-connected to the ground. Then, the system works as a normal boost converter where L_2 works alone as an inductor. In this way, the authors realize the transformer-reuse technique.

In [161], the authors adopted a hybrid-type topology and a boost converter with three stepping-up stages, whose architecture is shown in Fig. 2-2-4. It's composed of a low-voltage starter, an auxiliary step-up converter, a zero-current-switching (ZCS) controlled boost converter and several peripheral controllers.

The low-voltage starter is realized by an LC-tank oscillator followed by a voltage multiplier. The oscillator first converts the input DC voltage into AC form and then the voltage multiplier is used to boost the V_{DDi} to a high level. After V_{DDi} is high enough, the

peripheral controllers start to work and a clock signal CK_S is generated to activate the auxiliary step-up converter.

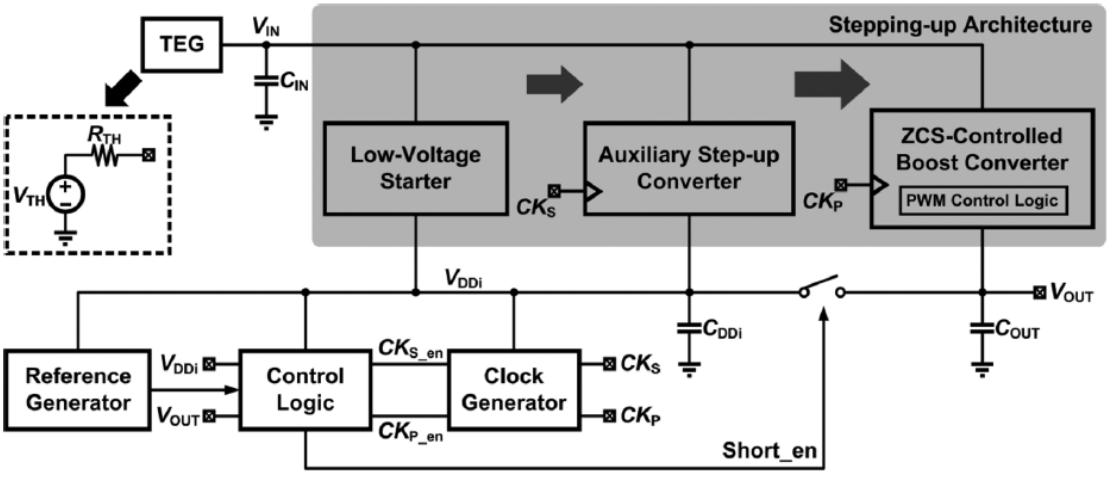


Fig. 2-2-4 3-stage stepping-up architecture proposed in [161]

The auxiliary step-up converter is applied to prevent undesirable loading effects on the low-voltage starter and to further boost the V_{DDi} for the use of the high-efficiency ZCS boost converter. When V_{DDi} reaches a high enough value, it will be used to power the last stage and a regulated voltage at V_{out} is obtained.

Although the systems proposed in [156], [160] and [161] can achieve a low startup voltage as 35mV, 40mV, 50mV and relatively high efficiency as 58%, 61%, 73%, respectively, they all require additional external components for the startup phase, such as mechanical switch, transformer and more than one inductors. In [167], a capacitor pass-on scheme is proposed as shown in Fig. 2-2-5, which only requires a single inductor while keeps the startup voltage low enough.

In startup mode as shown in Fig. 2-2-5(a), the output capacitor is charged by the charge pump, which is driven by the low-voltage oscillator. The oscillator can work with a supply voltage as low as 95mV, while the charge pump is an on-chip 20-stage Dickson structure. At the moment when the output capacitor has a high enough voltage, it will be "passed on" to be part of the boost converter and start to provide supply voltage to the control unit.

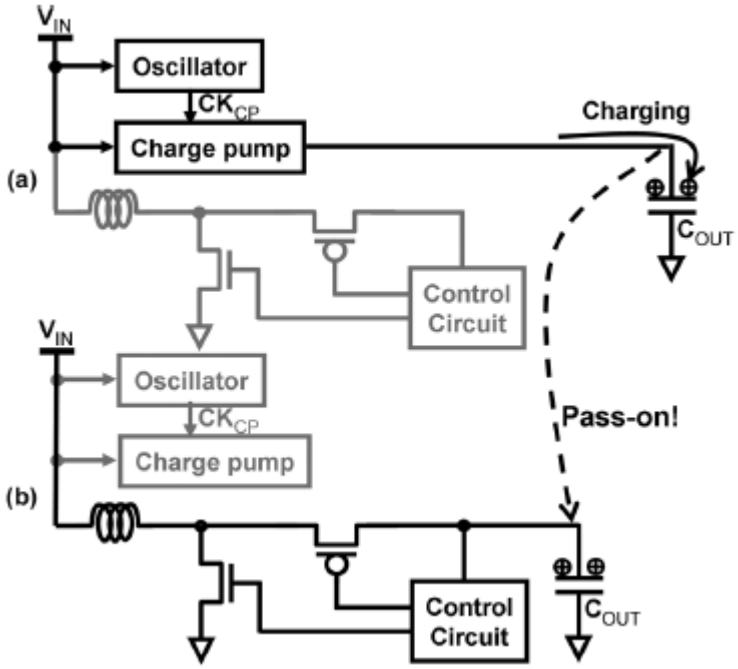


Fig. 2-2-5 Capacitor pass-on scheme to kick-start the system proposed in [167] (a) Startup mode (b) Operation mode

Table 2-2-1 summarizes the performance for state-of-the-art PMUs. In conclusion, for the PMU in IoT wireless sensors, we would like to reduce the external components as much as possible. Thus, a startup structure of oscillator with charge pump is desired as no additional inductor is needed. Also, to maintain a high overall conversion efficiency, we

should de-activate the functional blocks when output power is enough for the load. Thus, the pulse skipping modulation (PSM) is attractive as such control strategy regularly force the converter to be idling and much power can be saved [176][177].

Table 2-2-1 Performance summary for state-of-the-art PMU

	[156]	[160]	[165]	[169]	[173]
Process	350nm	130nm	180nm	180nm	65nm
Startup Integrated?	No	No	Yes	No	No
Startup voltage (mV)	35	40	190	260	40
Output voltage (V)	1.8	2	1-1.6	1.05-1.4	1.1
Pcontrol (μW)	N/A	N/A	10.8	2.4	77
Maximum efficiency	58%	61%	60%	90.8%	75%
MPPT	Yes	Yes	Yes	Yes	No

2.3 Summary

In this chapter, state-of-the-art research publications on wireless communication circuits and thermoelectric energy harvesting systems are reviewed. In Section 2.1.1, the FSK receiver design in IoT application is firstly reviewed. Ideally, the receiver should be able to handle a wide range of frequency bands and consume less power. However, limited by the frequency-to-amplitude converter, it's not easy to cover different frequency bands in a single chip without calibration. Then the concept and characteristics of N-path filter are introduced, and recent research proves that N-path filter is a potential solution. Section 2.1.2 reviews the frequency synthesizer design, where we focus on the injection-locked ring oscillator (ILRO). The ILRO is proved to be suitable for IoT applications because it

consumes less power and is easy to be integrated. However, it suffers from limited locking range. Again, the N-path switching network would help improve the locking range thanks to its high-*Q* property. Section 2.2 first illustrates the reason why we take thermoelectric energy harvester as the example of the PMU design in IoT wireless sensors in this research and then we review the different architectures for thermoelectric energy harvesting systems. Most of the designs follow a "startup - main converter – control unit" topology; however, the detail circuit implementation can differ. For the sake of integration and low power consumption, a startup topology composed of ring oscillator plus charge pump is desired and the PSM is a potential choice for the control unit.

Chapter 3
A Low Power Frequency Tunable FSK Receiver Based on the 4-Path Filter

As discussed in Chapter 2, for short range IoT applications, FSK is preferred compared to another commonly used modulation scheme, i.e., OOK. In the modulation prospective, FSK has constant envelop so that a more power-efficient non-linear power amplifier (PA) can be used. In the transmission channel, FSK modulated signal shows better spectral efficiency than OOK and it also has better noise or interference immunity.

The commonly used FSK modulator is shown in Fig.3-1(a), where the data signal is used to control the analog switch to choose frequencies according to binary input. An internal clock may also be applied to avoid the abrupt phase discontinuities at the output signal. It is worth noting that usually the tones f_1 and f_2 are close to each other in order to save spectrum resources and the data rate f_{data} is much lower than the tones to ensure enough settling time. Conventionally, the FSK modulated signal sets to a high frequency tone for a binary high input and is low for a binary low input. The binary ones and binary zeros are called Mark and Space frequencies, respectively.

Although the structure for FSK modulation is simple, the reception and demodulation of the FSK signal is more complex and can cost much power. A typical FSK demodulator is shown in Fig.3-1(b) and it consists of two band-pass filters, two envelop detectors and a decision circuit. Since the mark frequency and space frequency are close to each other, the band-pass filters should have very good selectivity (or high filter order) to

distinguish two tones. This leads to high power consumption and large area if using conventional filters.

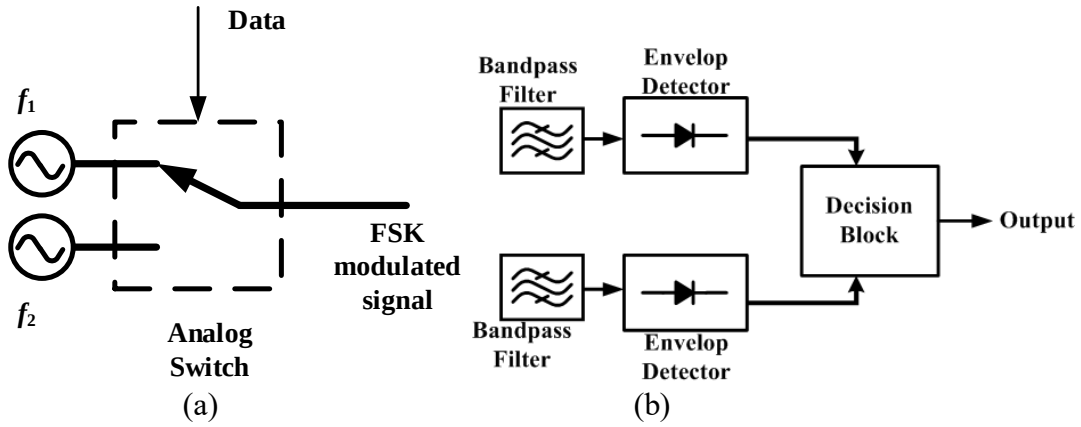
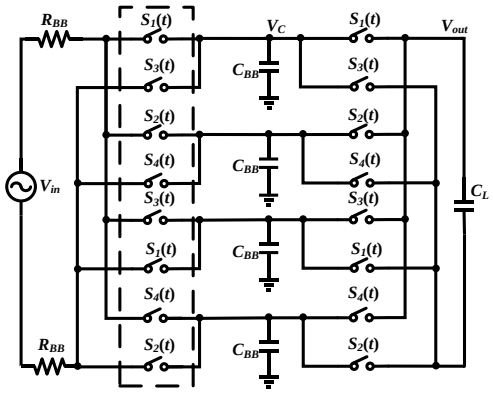


Fig. 3-1 Conventional structure of FSK (a) modulator and (b) demodulator

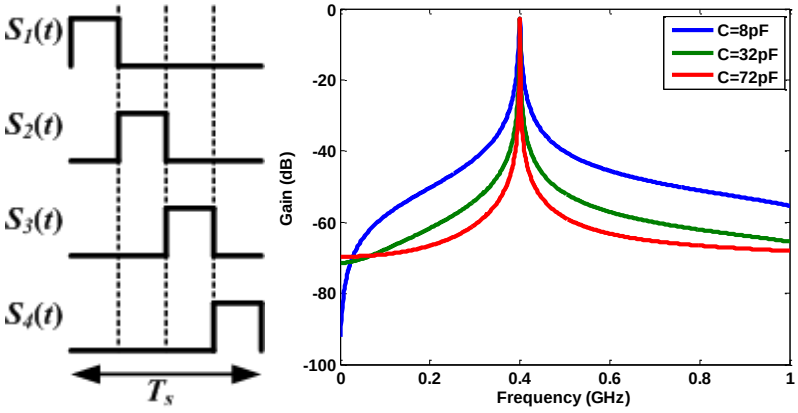
As discussed in Chapter 2, N-path filter has many attractive features such as good frequency selectivity, center frequency tunability and easy on-chip integration. This motivates us to apply N-path filter in FSK receiver, which has not been reported to the best of our knowledge. Rather than one-port N-path filter reviewed in Chapter 2, we adopt two-port structure for the N-path filter as the non-ideal switching resistance has less effect.

A basic topology of two-port differential 4-path filter is shown in Fig. 3-2(a). Here we choose 4-path because the 2-path structure suffers a more severe harmonic folding back effect, which causes higher input referred noise, while the 8-path structure will take double the area. The 4-path filter consists of two sets of switches driven by 4 non-overlapping clock signals, S_1-S_4, as shown in Fig. 3-2(b) and 4 low-pass baseband filters formed by the shared R_{BB} in the main path and C_{BB} in each branch. The first set of switches in dashed box

acts as a down-conversion mixer and shifts the input RF signal to baseband. After filtering by the low-pass filter, the second set of switches up-converts the signal to the RF domain. As a result, the overall frequency response is a band-pass filter whose center frequency is located at the clock frequency, f_S. Fig. 3-2(c) shows the typical gain plots with different baseband filtering capacitance, i.e. larger capacitor will result in high Q for better out-of-band (OOB) attenuation



(a)



(b) (c)

Fig. 3-2 (a) Differential two-port 4-path filter (b) Clocking scheme for 4-path filter (c) Frequency response for 4-path filter with different baseband filtering capacitor

The rest of this chapter is organized as follows: the proposed 4-path filter based FSK receiver is described in Section 3.1. The transient analysis of two-port 4-path filter is presented in Section 3.2. Section 3.3 gives the design considerations of FSK receiver and its measurement results. The conclusion is drawn in Section 3.4.

3.1 4-Path Filter based FSK Receiver

The structure of the proposed 4-path filter based FSK receiver is shown in Fig. 3-1-1. The receiver is composed of a two-port differential 4-path bandpass filter, a Differential-to-Single-Ended (D2S) amplifier, a baseband amplifier, a comparator and an output buffer. The 4-path filter converts the frequency difference of the received signal to amplitude difference, i.e., the input signal is converted from FSK signal to an ASK signal. Thus, the stages following the 4-path filter is basically an ASK demodulator, where the D2S amplifier is used to change the differential signal to single ended and baseband amplifier serves as an envelope detector and an amplifier simultaneously. And the digital output is obtained from the comparator.

Conventionally, the FSK receiver is composed of two bandpass filters to deal with the mark and space frequencies separately to increase the sensitivity by exploiting the input power as much as possible. However, for the 4-path filter based FSK receiver, the area almost doubles if two filters are used due to the relatively large capacitance. Another issue for the use of two bandpass filters is the need of two reference clocks, whose frequencies are close to each other. These clocks may cause severe interference, which could deviate the center frequency of bandpass filter from desired value and the demodulation can’t

function properly. To solve this issue, additional circuitry and power are needed but such solution is not suitable for low-power IoT applications. Therefore, the single 4-path filter topology is adopted. LNA is not used due to the filter-first topology and the low-power requirement. Also, thanks to the center frequency tunability of the 4-path filter, this structure can be applied to different applications where the carrier frequencies are different by simply tuning the reference clock frequency.

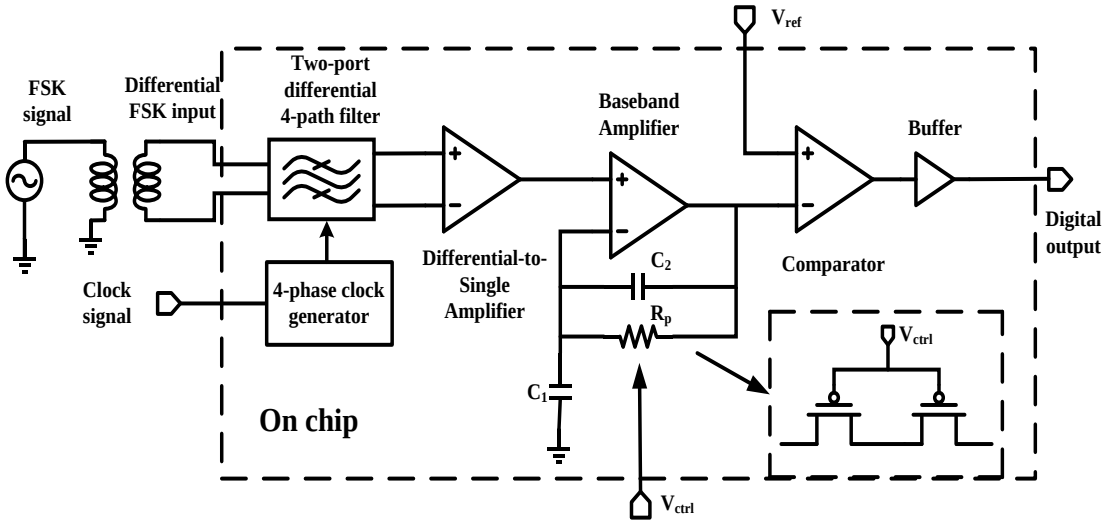


Fig. 3-1-1 Structure for the proposed 4-path filter based FSK receiver

The highest data rate is mainly determined by the 4-path filter in the proposed receiver. Thus, it is important to analyze the 4-path filter in order to determine the data rate. The frequency selectivity is an important consideration. As shown in Fig. 1(c), the increase of filtering capacitance improves the frequency resolution. However, a large capacitor not only takes large chip area, but also prolongs the settling time. The longer settling time will reduce data rate for a given resolution of comparator. This is because the voltage

differences of two adjacent tones from 4path filter outputs would be very close to each other if long settling time is needed. To maintain high data rate in such case, the resolution of the comparator must be increased at the cost of power. To trade-off between power and data rate, it is important to find the transient time of a 4-path filter when frequency changes. To the best of our knowledge, the existing studies mostly focused on the steady-state analysis of 4-path filter and no transient response analysis has been reported.

3.2 Transient Analysis of Two-Port 4-Path Filter

It is challenging to analyze the behaviour of 4-path filter loaded by a capacitor as the capacitor is a storage component. We can't apply kernel independently as in [117]. Fortunately, we observed the following effect of the capacitor value to the output voltage V_{out} and baseband filtering capacitor voltage V_C:

(1) The load capacitor C_L mainly affects the output peak-to-peak voltage. As C_L goes larger, the peak-to-peak value of V_{out} will drop. This increases the power budget of the baseband amplifier and comparator as it requires better resolution to distinguish the voltage level;

(2) The baseband filtering capacitor C_{BB} has obvious influence on data rate. The larger C_{BB} is, the longer settling time will be. Thus, the data rate will be reduced;

(3) In the case when C_L is small enough (the equivalent RC time constant is still much smaller than the clocking period), V_{out} is a stepwise waveform and its envelope is equivalent to V_C;

(4) Oppositely, when the load capacitor is large, the output voltage is sinusoidal like waveform because the capacitor can't be charged or discharged completely. And the filtering capacitor voltage isn't equivalent to the output envelop anymore in this case.

Based on above observations, we can find that large output capacitor should be avoided. This is indeed the case in FSK receiver as the 4-path filter is loaded by a baseband amplifier, thus the load capacitor is the gate oxide parasitic capacitance of a MOS transistor, which is small. For example, in 0.13μm CMOS technology, it is only 12fF/μm^2. Fig. 3-2-1 shows the filtering capacitor voltage and the output voltage. The simulation is performed in the condition of R_{BB} = 2KΩ, W/L = 500nm/130nm, C_{BB} = 40pF and C_L = 80fF (Fig. 3-2-1(a)) and C_L = 20pF (Fig. 3-2-1(b)). The FSK signal is modulated by two frequencies f_1 and f_2 and the clock frequency is equal to f_1. The time interval "1"s indicate when the input FSK signal frequency is equal to the clock frequency while time interval "0"s indicate that the two frequencies are different. For Fig. 3-2-1(b), where C_L has a large value, V_C can't reflect the envelop of V_{out} during time interval "1"s and it's impossible for us to extract the data information from V_C by simply using a comparator. In the case of Fig. 3-2-1(a) where the value of C_L is small, it's interesting to observe that at time interval "1"s, the output envelop looks like a conventional RC charging waveform and the input tone is passed through the 4-path filter. We also notice that in these intervals, V_C is equivalent to the envelope of V_{out}. While during time interval "0"s, V_C will change to a periodic signal with a beat frequency equal to $|f_2-f_1|$ and V_{out} is attenuated by the 4-path filter. Although the baseband filtering capacitor doesn't exactly reflect the output voltage at time interval "0"s,

we notice that the limit values are the same, i.e., the highest and lowest voltages of V_C and V_{out} are the same. Thus, we can still use the transient response to calculate the data rate in extreme conditions.

Thanks to the envelope feature, we can derive the transient time between two frequencies by investigating the baseband filtering capacitor voltage. Also, as we are performing analysis for small load capacitor, we can ignore it firstly and add an empirical factor later as long as the output voltage keeps the same shape, i.e., the clocking period is long enough. Thus, we can still apply the kernel method.

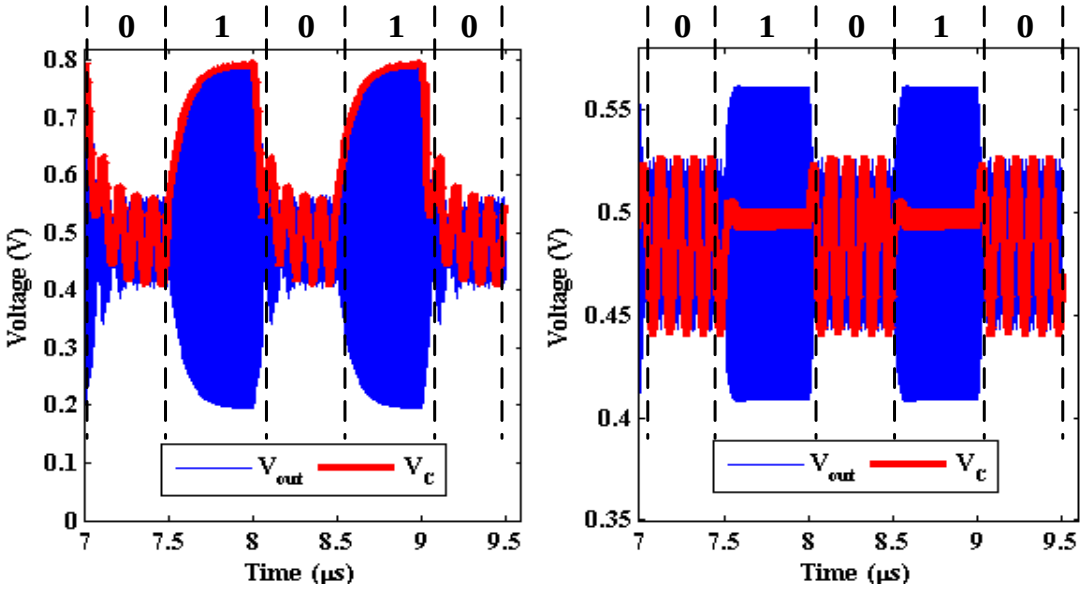


Fig. 3-2-1 Waveforms of the output voltage and baseband filtering capacitor voltage (a) with C_L=80fF (b) with C_L=20pF

3.2.1 Differential Two-Port 4-Path Filter

For differential two-port 4-path filter as shown in Fig. 3-2(a), one branch is connected to the input voltage source during two time-intervals within a switching period. Fig. 3-2-3(a) depicts the corresponding kernel for the first branch. As discussed earlier, C_L is much smaller than C, so we can ignore C_L and simplify the first branch to that in Fig. 3-2-3(b) and Fig. 3-2-3(c), which are the equivalent circuits in S_1 time interval and S_3 time interval, respectively. V_1 and V_2 are the equivalent voltage sources of V_{in} at S_1 and S_3 time intervals, respectively. Our goal is to derive the time-domain expression for the capacitor voltage V_C. Note that the following analysis is performed for the first branch in the time intervals [nT_s, $(n+D)T_s$] and [$(n+1/2)T_s$, $(n+1/2+D)T_s$] , i.e. S_1 and S_3 time interval, respectively. Here, n is the index of switching period and it's an integer greater or equal to 0; T_s is the switching period and D is the duty-cycle for each switch, which is 25% in 4-path filter. Other branches can be analyzed in the same manner.

As V_1 and V_2 are differential, they can be expressed as:

$$V_1(t) = Ae^{j(\omega t+\varphi)}, \tag{3-2-1}$$

$$V_2(t) = Ae^{j(\omega t+\varphi+\pi)}. \tag{3-2-2}$$

Solving the first order RC network in Fig. 3-2-2(b) and Fig. 3-2-2(c), we can find the expression for baseband filtering capacitor voltage in different time intervals. Let f=1/($R_{BB}C_{BB}$), for S_1 time interval [nT_s, $(n+D)T_s$], we have

$$V_C(t) = A'e^{j\omega nT_s}\left(e^{j\omega(t-nT_s)} - e^{-f(t-nT_s)}\right) + V_C(nT_s)e^{-f(t-nT_s)}, \tag{3-2-3}$$

$$A' = \frac{A}{1+jR_{BB}C_{BB}\omega}e^{j\varphi}. \tag{3-2-4}$$

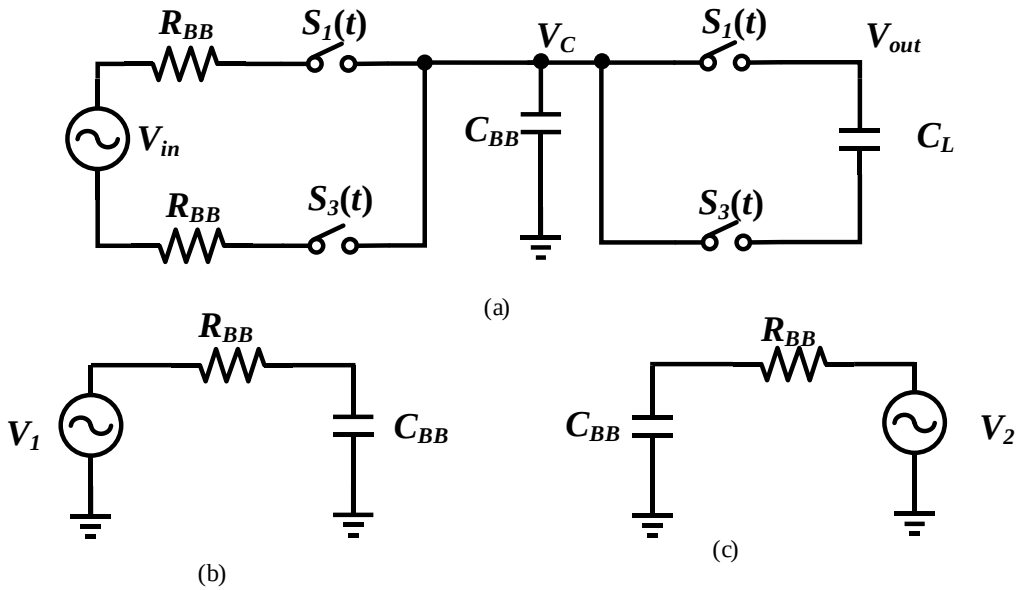


Fig. 3-2-2 (a) Kernel for differential two-port 4-path filter (b) Simplified circuit when S_1 connects and (c) Simplified circuit when S_3 connects

For S_3 time interval $[(n+1/2)T_s,\ (n+1/2+D)T_s]$, we have

$$V_C(t) = A' e^{j\pi} e^{j\omega\left(n+\frac{1}{2}\right)T_s}\left(e^{j\omega\left(t-\left(n+\frac{1}{2}\right)T_s\right)} - e^{-f\left(t-\left(n+\frac{1}{2}\right)T_s\right)}\right)$$

$$+ V_C\left(\left(n+\frac{1}{2}\right)T_s\right) e^{-f\left(t-\left(n+\frac{1}{2}\right)T_s\right)}.$$

(3-2-5)

To find the initial values $v_c(nT_s)$ and $v_c\left(\left(n+\frac{1}{2}\right)T_s\right)$ in (3-2-3) and (3-2-5), respectively, we can write the expression for $v_c((n+D)T_s)$and $v_c\left(\left(n+\frac{1}{2}+D\right)T_s\right)$first. As the capacitor voltage keeps the same anytime outside the two intervals, we can relate the two intervals by the following equations

$$v_c\big((n+D)T_s\big) = v_c\left(\left(n+\frac{1}{2}\right)T_s\right), \qquad (3\text{-}2\text{-}6)$$

$$v_c\left(\left(n+\frac{1}{2}+D\right)T_s\right)=v_c\big((n+1)T_s\big). \tag{3-2-7}$$

By substituting (3-2-6), (3-2-7) with (3-2-3) and (3-2-5) and re-arranging the expression, we can have a discrete time difference equation for $v_c(nT_s)$

$$v_c\big((n+1)T_s\big)=\alpha' v_c(nT_s)+\beta' e^{j\omega nT_s}, \tag{3-2-8}$$

$$\alpha'=e^{-2fDT_s}, \tag{3-2-9}$$

$$\beta'=A'\big(e^{j\omega DT_s}-e^{-fDT_s}\big)\left(e^{j\pi}e^{j\omega\frac{1}{2}T_s}+e^{-fDT_s}\right). \tag{3-2-10}$$

Again, if we assume that $v_c(0)=0$, we can have the expression of $v_c(nT_s)$ as

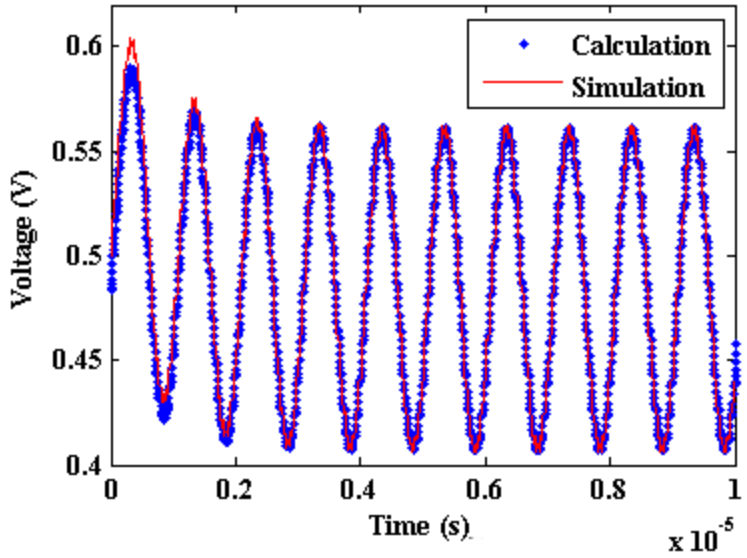
$$v_c(nT_s)=\beta'\frac{e^{j\omega nT_s}-(\alpha')^n}{e^{j\omega T_s}-\alpha'}. \tag{3-2-11}$$

Finally, we can substitute (3-2-11) into (3-2-7) to get the expression of $v_c\left(\left(n+\frac{1}{2}\right)T_s\right)$

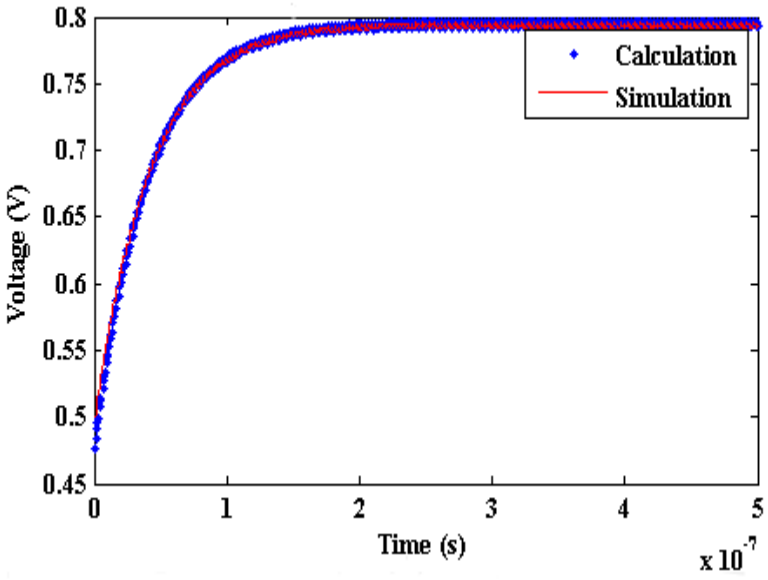
$$v_c\left(\left(n+\frac{1}{2}\right)T_s\right)=A'\big(e^{j\omega DT_s}-$$

$$e^{-fDT_s}\big)\frac{e^{jwnT_s}\left(e^{j\omega T_s}+e^{j\pi}e^{j\omega\frac{1}{2}T_s}e^{-fDT_s}\right)-e^{-(2n+1)fDT_s}\left(e^{j\pi}e^{j\omega\frac{1}{2}T_s}+e^{-fDT_s}\right)}{e^{j\omega T_s}-e^{-2fDT_s}}. \tag{3-2-12}$$

Fig. 3-2-3 plots the calculated waveforms based on (3-2-3), (3-2-5), (3-2-11) and (3-2-12) together with the simulation results for following two cases. Case A: input frequency equals to the switching frequency and Case B: input frequency is different from the switching frequency by 1MHz. It is obvious that the theoretical analysis matches well with the simulation results.



(a)



(b)

Fig. 3-2-3 Comparison between the calculation and simulation results for baseband filtering capacitor voltage (a) the input frequency is different from the clock frequency by 1MHz (b) the input frequency is equal to the clock frequency

3.2.2 Determine the Data Rate based on the Transient Response

Based on the above analysis, we can now calculate the data rate for FSK receiver. The worst case for transient time between two frequencies happens in the case when the filtering capacitor voltage increases from common-mode voltage to the steady-state voltage. To calculate how long it takes, we can let the input frequency equal to the switching frequency, i.e., $\omega=2\pi/T_s$ and substitute it into (3-2-20) to take the limit value after infinitely long time, i.e.

$$\lim_{n\to\infty} V_C(nT_s) = \frac{\beta'}{1-\alpha'}. \tag{3-2-13}$$

Let (3-2-11) equal to 90% of its limit value given by (3-2-13), we obtain the number of n_d, i.e. after n_d clock cycles the output voltage attains a close enough level to the steady-state voltage.

$$n_d = -\left(\frac{ln(0.1)}{2}\right) \times N \times R_{BB}C_{BB} \times f_s, \tag{3-2-14}$$

where N is the number of paths and f_s is the switching frequency.

Above equation can be understood intuitively. As time constant $R_{BB}C_{BB}$ increases, the charging time will increase accordingly, and more clock cycles are required to achieve the same level. When the path number N or switching frequency f_s increases, the effective charging time in one single clock cycle will decrease, thus the required number of clock cycles will also increase accordingly.

Note that (3-2-14) is derived with the initial capacitor voltage equal to the common mode voltage. However, in the real application, the initial value is usually other than the common mode voltage when input frequency is switching to f_1 which equals to clock

frequency as shown in Fig. 3-2-1. This initial value is dependent on the frequency difference between two input tones. To understand the effect of frequency difference on the data rate, we can think about the two extreme cases. When there is no frequency difference (f_2 equals to f_1), no data can be transmitted as the receiver only receives a single tone signal. So, the data rate is 0. On the other hand, in the case when the frequency difference is quite big, according to Fig. 3-2(c), f_2 is almost totally rejected, which means that only common mode voltage appears, and the signal will look like an OOK waveform. Then the maximum data rate can be achieved.

Thus, we need to introduce another factor to find the maximum achievable data rate f_{dr} with a certain frequency difference:

$$f_{dr} = \frac{1-\gamma}{-\left(\frac{ln(0.1)}{2}\right)\times N\times R_{BB}C_{BB}}, \tag{3-2-15}$$

where γ is the gain of 4-path filter at f_2 and its ideal value range is (0,1].

According to Fig. 3-2(c), when f_1 and f_2 are close to each other, γ is large. Thus, the data rate will be low based on (3-2-15). The maximum data rate in the worst case for FSK receiver is 2.3Mbps with N=4, C_{BB}=40pF, R_{BB}=2kΩ and γ=0.18 (f_1 equals to 401MHz and f_2 equals to 406MHz).

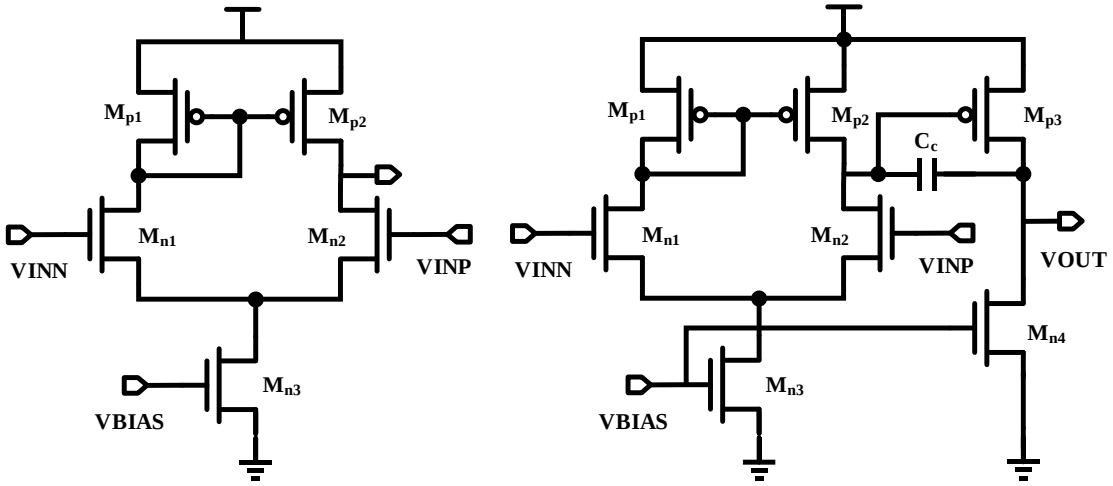
3.3 Circuit Design Considerations and Measurement Results for Proposed FSK Receiver

Based on the analysis in above section, we set the data rate as 2.5Mbps, a value slightly better than the worst case. The two-tone frequencies are 401MHz and 406MHz, respectively.

3.3.1 Circuit Design Considerations

Since the 4-path filter doesn't provide any gain, we need to carefully design both the 4-path filter and the D2S amplifier to attain reasonable noise performance. For the 4-path filter, most of the noise is contributed by the thermal noise of MOS switch and the R_{BB}. A small R_{BB} reduces the noise but it increases the size of C_{BB} resulting large area. So, there is a trade-off between noise and area. For the D2S amplifier, whose structure is given in Fig. 3-3-1(a), the way to improve its noise performance is to increase the size of the input and load transistors as well as the bias current. However, a large transistor may deteriorate the loading effect of the 4-path filter and the increased bias current means more power. For the given values of R_{BB}=2kΩ, input and load transistors are at W/L=500μm/1μm, and bias current sets to 78μA. Simulations show that 4-path filter has a noise figure of 1.6dB and the total in-band input referred noise of the D2S amplifier is 6μV. The spectrum of input referred noise of 4-path filter and D2S amplifier in 300MHz-500MHz band is given in Fig. 3-3-2, and we can see that the noise around switching frequency is low because the 4-path filter has minimum attenuation at that frequency.

The baseband amplifier is a classical two-stage CMOS op-amp with Miller compensation as shown in Fig. 3-3-1(b). As it is used in a feedback structure, the main design consideration is stability. A small Miller capacitor is applied in order to have a high cutoff frequency as well as good phase margin. As shown in Fig. 3-1-1, the feedback capacitor pair C_1 and C_2 set the close-loop gain.



(a) (b)

Fig. 3-3-1 Structure of (a) D2S amplifier and (b) baseband amplifier

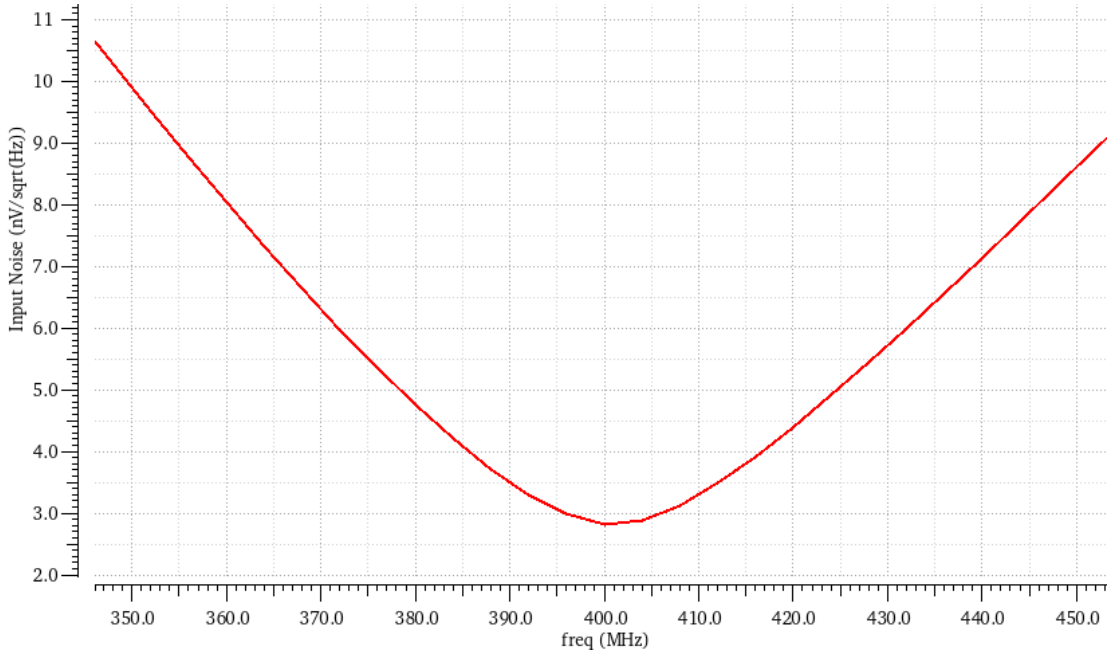


Fig. 3-3-2 Input noise spectrum of 4-path filter and D2S amplifier

As the baseband amplifier serves as the envelop detector, we want it to amplify the signal within the data rate frequency while attenuating the carrier frequency. Thus, the -3dB bandwidth of the close-loop structure should be around 3MHz to have enough margin for 2.5MHz data rate. To achieve this, a large feedback resistor with the value of at least hundreds of Mega ohms is needed. An on-chip pseudo resistor composed of two PMOS transistors is used, which can provide Giga ohms resistance. The resistance of the pseudo-resistor can be easily tuned by a programmable voltage source. As we aim to demonstrate the feasibility of 4-path filter for FSK receiver, an off-chip control voltage V_{ctrl} is used to adjust the equivalent resistance of pseudo-resistor. In addition to the bandwidth setup, the input data should be properly randomized so that the baseband amplifier can also function as an envelope detector properly. Otherwise, if there is a long sequence with only "1"s or "0"s, the output of the amplifier will end up with the common mode voltage and no data can be recovered. Thus, the proposed structure requires a scrambler (or randomizer) at the modulation end, which can avoid the appearance of the long sequence with same value. This phenomenon is depicted in Fig. 3-3-3. The top is the output of the D2S amplifier which is fed to the baseband amplifier and the bottom is the output of the baseband amplifier. As can been seen, when the data bit is changing frequently, the output can reflect the change around the common mode voltage, however, at the end, when the data is kept to 0, the output is stabilized to the common mode voltage.

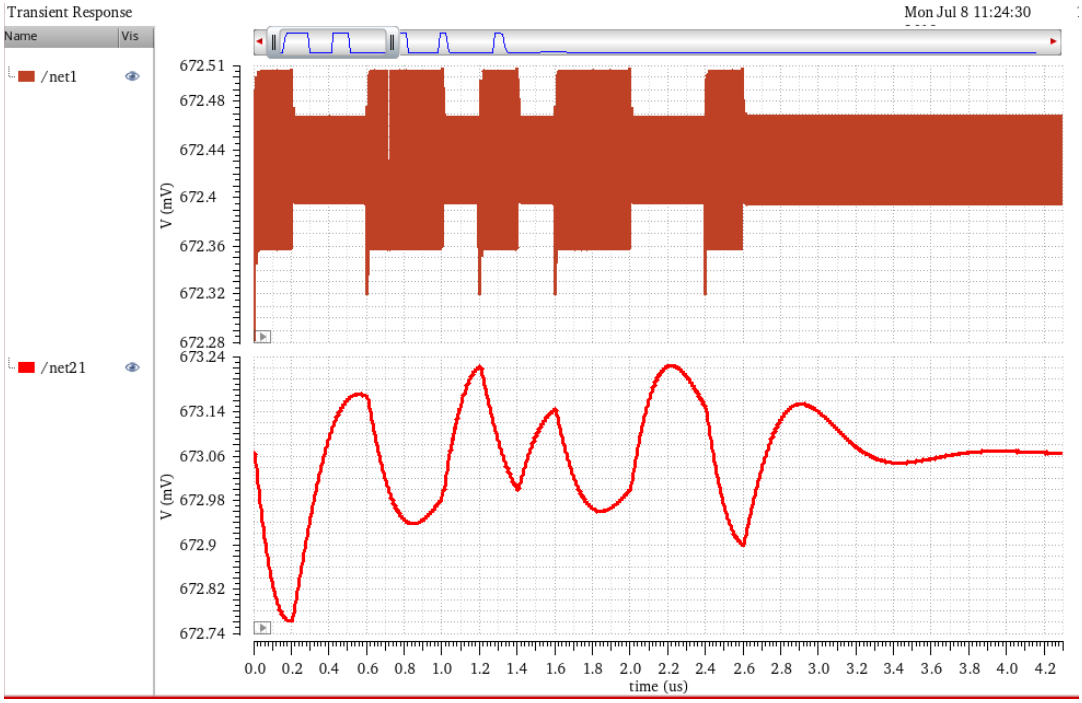


Fig. 3-3-3 Simulation waveforms for difference frequencies of “01” sequences

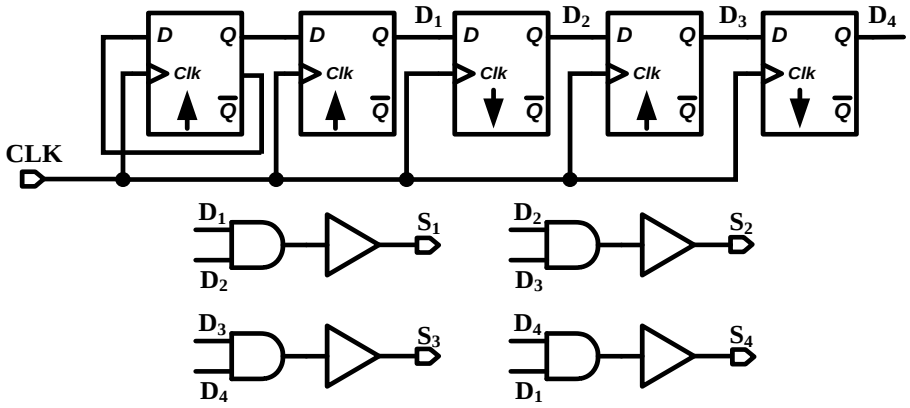


Fig. 3-3-4 Four-phase non-overlapping clock generator

The circuit of 4-phase clock generator is given in Fig. 3-3-4. Its input is a 50% duty-cycle square wave signal of 802MHz. It generates four 25% duty-cycle non-overlapping

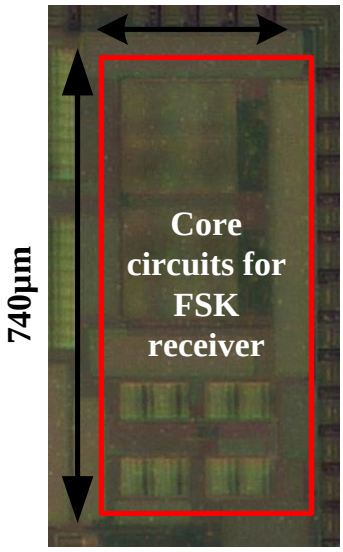
square wave signals as the outputs. The first flip-flop performs as a frequency divider. The following four DFFs generate four 50% duty cycle square waves D_1, D_2, D_3 and D_4 with a delay of 0%, 25%, 50% and 75% of the clock period, respectively. Let D_1-D_4 pass through an AND gate and a buffer pair by pair, we can obtain four 25% duty-cycle non-overlapping pulse wave S_1, S_2, S_3 and S_4.

3.3.2 Measurement Results

The proposed 4-path filter based FSK receiver has been implemented in 130nm CMOS process. A die photo of the chip and the power consumption summary are shown in Fig. 3-3-5. The core area is 300 x 700μm^2.

To measure the chip performance, an RF signal generator (ROHDE & SCHWARZ SMB100A), an RF pulse/pattern generator (KEYSIGHT 81134A) and a mixed-signal oscilloscope (TEKTRONIX MDO3024) are used. The input FSK signal is converted to differential form by an off-chip balun (TDK Corporation HHM1589D1) with bandwidth of 350MHz - 950MHz. The differential FSK signals are fed into the first stage of the receiver.

To illustrate the frequency tunability, we measure the chip in two MedRadio sub-bands, i.e. 401-406MHz and 438-444MHz. The outputs of the baseband amplifier and the digital output of the system are shown in Fig. 3-3-6 (a) for two frequency bands: Case A where the input data is pseudo-random and the chip operates in 401-406MHz band, and Case B where the input data is “0101” sequence and the chip operates in 438-444MHz band.



Power Consumption Summary

D2S amplifier	94μW
Baseband amplifier	42μW
Comparator	33μW
Others	15μW
Total	**184μW**

Fig. 3-3-5 Chip micrograph and power consumption summary

It can be seen from Fig.3-3-6 that the baseband amplifier removes the carrier frequency and amplify the data signal simultaneously. Note that the input of the baseband amplifier is at very low power level and the oscilloscope can't detect it. The system output is a digital signal whose data rate is 2.5Mbps, which is close to the previously given theoretical result. The reason that measured data rate is better than theoretical value is that (3-2-15) is derived in the worst case where the voltage level of baseband filtering capacitor reaches to the highest when the input frequency is equal to the clock frequency. However, the practical data rate can be higher because the comparator has a high enough resolution so that the two voltages can be separated without the higher one goes to the highest. Furthermore, by tuning the input clock frequency, the center frequency of 4-path filter is changed, and the receiver can adapt to different carrier frequencies.

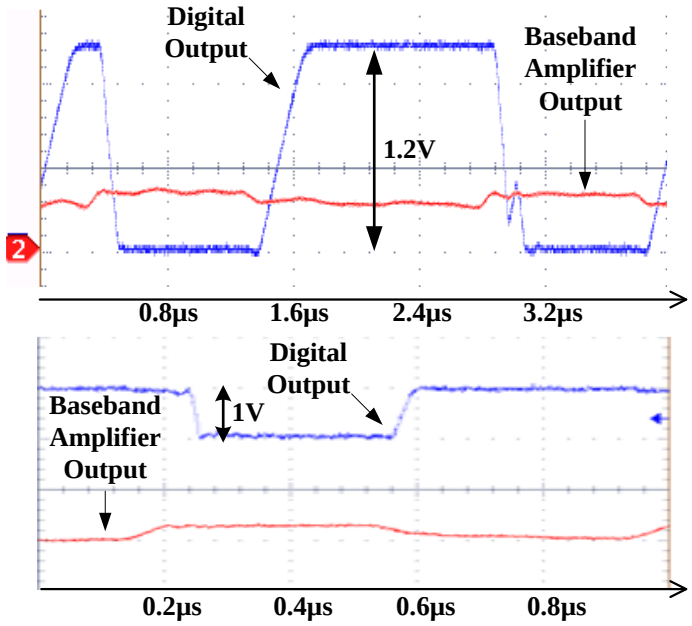


Fig. 3-3-6 Measured waveform for baseband amplifier output and the system digital output for Case A(top) and Case B(bottom)

We did the post-layout simulation for bit error rate (BER)/ signal noise ratio (SNR) plot in the extreme conditions by considering both the external noise and the input referred noise from the components, and the simulation result is given in Fig.3-3-7 with an input power level of -65dBm. As can be observed, the noise level can't exceed -70.5dBm. Otherwise, the bit error rate will be too high.

Table 3-3-1 summarizes the measured performance of the proposed FSK receiver comparing with existing designs. The proposed receiver is competitive in both power consumption and data rate. And it achieves a best energy per bit, which means the proposed structure can have a high data rate with less power consumption.

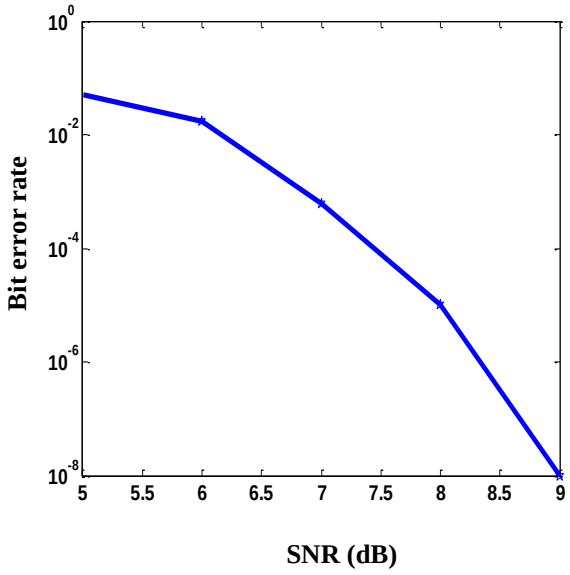


Fig. 3-3-7 Simulated BER vs SNR plot

Table 3-3-1 FSK receiver performance comparison

Reference	[93]	[97]	[102]	This work [85]
Technology(μm)	0.13	0.18	0.18	0.13
Supply(V)	1.2	0.45	0.7	1
Modulation	FSK	FSK	FSK	FSK
Sensitivity(dBm)	-78	-69	-62	-65
Carrier Frequency(MHz)	902-908	402-405	72-80	401-406
Tunability	No	No	No	Yes
Data Rate(Mbps)	8	0.12	0.312	**2.5**
Power Consumption(μW)	639	352	45	**184**
Energy per bit(nJ/bit)	0.08	1	0.14	**0.074**

3.4 Conclusion

This chapter presents a low power frequency tunable FSK receiver based on 4-path filter. The 4-path filter serves as the first stage of the receiver and converts the frequency difference

between two tones to amplitude difference. To evaluate the maximum achievable data rate of the proposed receiver, we studied the behavior of 4-path filter under two-tone input condition. With linear periodically time-variant theory, the equations for transient response between two tones are derived for differential two-port 4-path filters and verified by the simulation. Based on the analysis, an optimum data rate is obtained for the proposed 4-path filter based FSK receiver. Implemented in 0.13µm CMOS process, the chip occupies 300 x 700µm^2, achieves data rate of 2.5Mbps, and 74 pJ/bit Energy per Bit at -65 dBm sensitivity. Frequency tuning is also demonstrated.

Chapter 4
A Low-Power Wide-Locking-Range 4-Path Mixer Based Injection Locking Frequency Synthesizer

In chapter 2, we reviewed the most commonly used structures for the frequency synthesizer and the injection-locking frequency synthesizer, or ILCM, shows good performance in terms of power consumption with simple hardware implementation, which is critical in IoT applications. Therefore, based on the injection locking oscillator, we proposed a two-step calibration frequency synthesizer where the first step is accomplished by the 4-path mixer and the second step is done by injection locking. By introducing the coarse calibration by the 4-path mixer, the overall locking range can be increased while the power consumption is kept in low level.

4.1 4-Path Mixer Based Injection Locking Frequency Synthesizer

In IoT wireless sensors, a frequency synthesizer is commonly used as it can provide a wide range of accurate clock signals to the receiver. However, conventional PLL based frequency synthesizer usually costs much power as discussed in Chapter 2. Thus, reducing its power consumption is of vital importance in reducing the total required power from wireless transceiver or prolonging the battery life to avoid the frequently battery replacement. Several PLLs with low supply voltage (0.5V to 0.6V) have been presented in various publications, but their power consumption remains in the range of milliwatts, mainly because of the design challenges posed by the low supply voltage. The reason is

that with low overdrive voltage, the performance of ultra-low voltage designs is extremely sensitive to PVT variations, especially for analog designs. Fighting against these variations not only require complex circuits that are hard to implement, but also would demand extra power.

In this research, we proposed an alternative way to design frequency synthesizer based on 4-path switching network. The motivation of applying 4-path switching network in frequency synthesizer design comes from the fact that the baseband filtering capacitor can reflect the envelop changing of the output waveform as discussed in Chapter 3. Moreover, as shown in Fig. 3-2-1, when the input frequency is equal to the clock frequency, the envelop of one branch is a high-level stable voltage, and when the input frequency is not equal to the clock frequency, we will have a sinusoidal envelop with low enough peak to peak value for the comparator to distinguish them. Different from the 4-path filter, we can get rid of the second set of switches in Fig. 3-2(a) as we only care about the envelop in this case. And the 4-path filter comes to be a 4-path mixer now.

However, due to the asynchronization between the input signal and clock signal, it's hard to say which branch will output the high-level voltage. Thus, a comparator will be required for each branch to detect the high-level voltage which indicates that the input frequency is equal to the clock frequency. Due to the output of comparator is digital one or zero, we can apply a digital controlled oscillator (DCO) rather than conventional VCO. However, the 4-path switching network and the comparator can only tell us that the output frequency is very close to the reference frequency but it's hard for them to adjust the output

frequency to be exactly equal to the reference because of the limited resolution of the comparator.

Fortunately, as discussed in Chapter 2, injection-locking technique can be used to force the free-running oscillator to output a signal with accurate frequency as long as the free-running frequency and the injected frequency are close enough. Thus, a two-step architecture is applied in our proposed design for an accurate output frequency. The first step is done by the 4-path mixer for a coarse tune of the output frequency which makes the output frequency is close enough to the reference frequency. The second step is done by injection-locking to obtain a stable and accurate output.

4.1.1 Overall Architecture

Fig. 4-1-1 gives the architecture for the proposed frequency synthesizer, and it's composed of a 4-path mixer, a multi-input comparator, a 5-bit calibration block, a DCO and a frequency divider. The accurate clock signal is obtained at V_{out}.

At the beginning, the oscillator is free-running and the 4-path mixer accepts both the divided oscillator output signal and the divided reference clock signal. The structure of the 4-path mixer is given in Fig. 4-1-2(a) and it has four outputs O_1-O_4. The four outputs are compared with a pre-set reference voltage to determine how close the oscillator output frequency and the reference clock frequency are. If no high-level voltage is detected by the comparators, meaning that the two input frequencies of the 4-path mixer are not close enough, the 5-bit Calibration circuit will generate a control bit to adjust the current source and further change the oscillating frequency of the oscillator. Once a high-level voltage is

detected, it means that the oscillator frequency is calibrated to be close enough with the reference frequency. Then the 5-bit Calibration circuit will lock the digital-controlled-current-source and enable the switch for injection locking. And finally, the oscillator will be locked at the injection locking frequency.

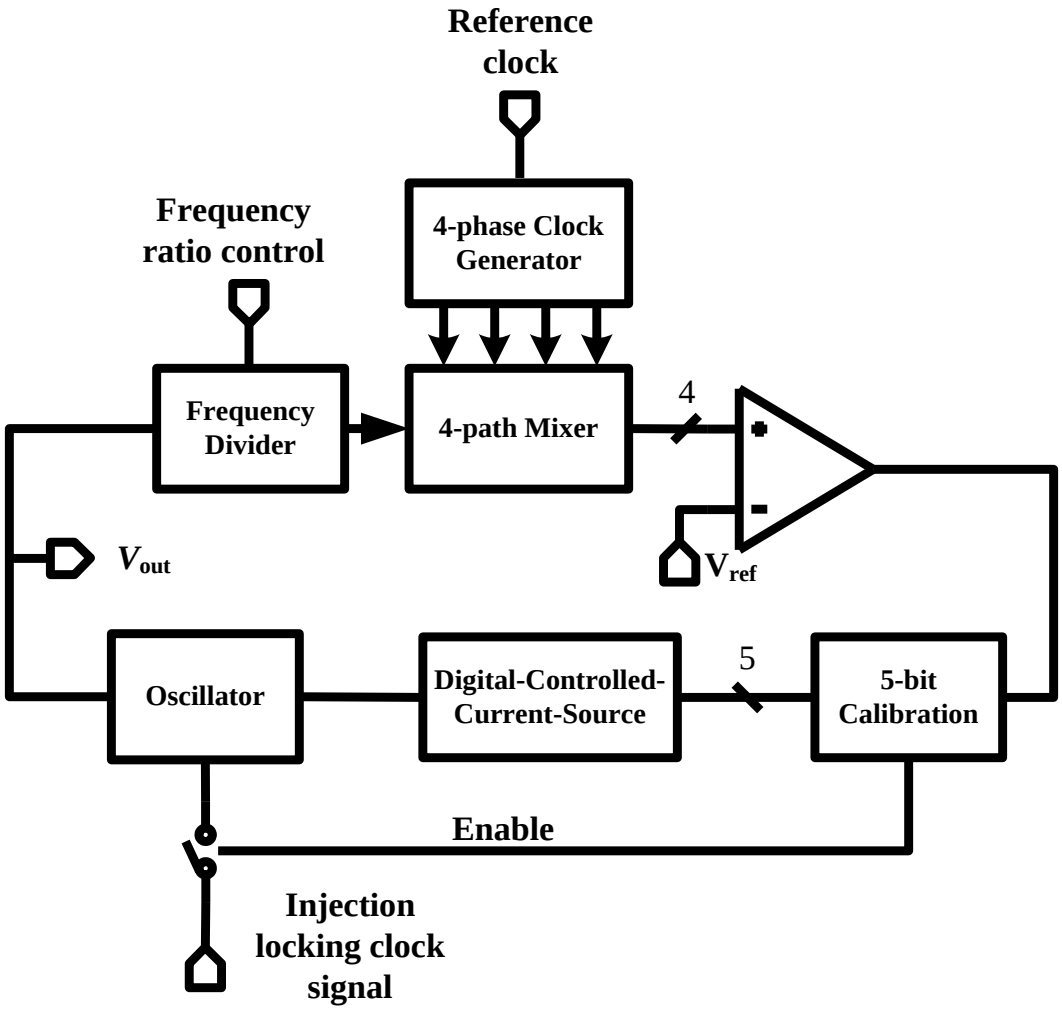


Fig. 4-1-1 Overall Architecture of the proposed frequency synthesizer

Fig. 4-1-2(b) illustrates intuitively how the 4-path mixer works to detect the frequency difference. For 4-path mixer, even though in the worst case for asynchronization, which means that there are two branches whose average outputs are zero, at least one of the branches has a high-level output. Thus, no matter how the phase of input signal is deviated from that of the clock signal, there is always at least one branch who can output a high-level voltage. That's because the input signal has a 50% duty cycle while the clock's duty cycle is 25%. Thus, we can stay assured that the comparators can successfully detect it as soon as the oscillator frequency and the clock frequency are close to each other. However, for 2-path mixer, the worst case happens when the two branches both output zero and it's impossible for the comparators to detect. Even though 8-path mixer can also guarantee the frequency detection, it requires a higher reference frequency for the 8-phase non-overlapping clock signal.

To obtain a wide range of output frequency, the division ratio of the frequency divider can be adjusted by the external frequency ratio control signal. Supposing that the reference frequency is f_{ref} and the oscillator output frequency is f_{vco}, the two-step frequency locking architecture will force the following equation to hold

$$\frac{f_{ref}}{2} = \frac{f_{vco}}{n} \Rightarrow f_{vco} = \frac{n}{2} f_{ref}, \tag{4-1-1}$$

where n is the division ratio provided by the frequency divider. And note that the factor 2 comes from the fact that the output of the 4-phase clock generator for the 4-path mixer will divide the reference frequency by 2 as shown in Chapter 3.

From (4-1-1), we can see that the oscillator output frequency can be changed by adjusting *n* and eventually a wide range of output frequencies can be covered.

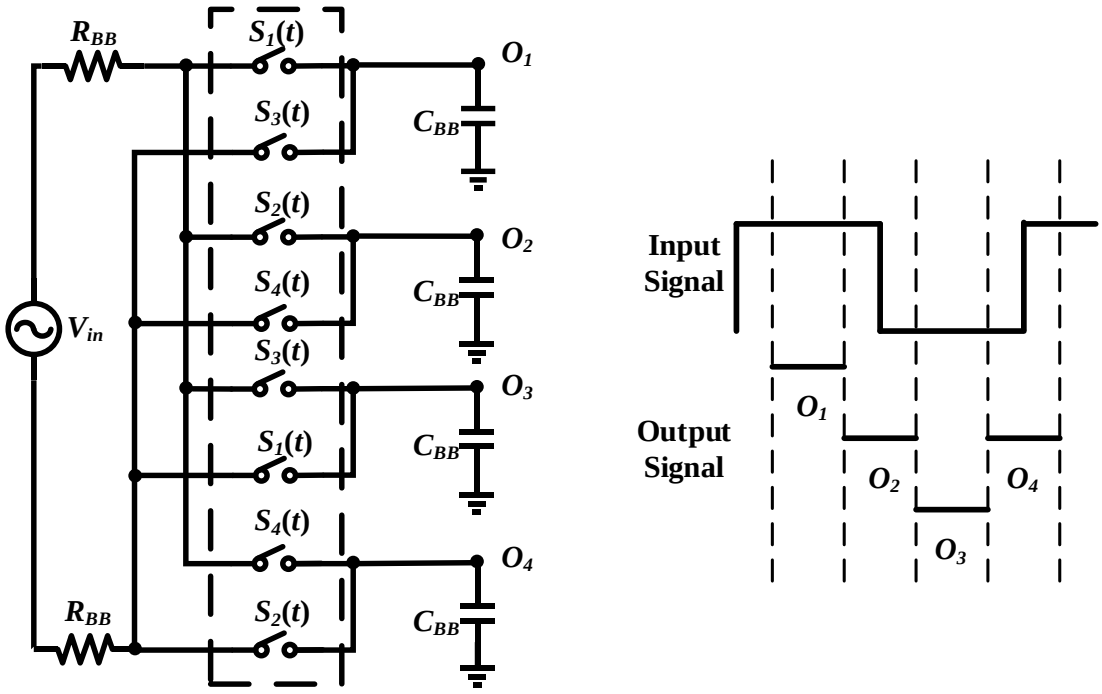


Fig. 4-1-2 (a) Structure of the 4-path mixer (b) Worst case scenario between the input and output of the 4-path mixer

4.1.2 Locking Range Analysis

To make sure that the output signal can be successfully injection locked rather than being injection pulled, it's necessary to analyze the locking range of the two frequency tuning steps separately and to make sure that the locking ranges for the two steps have some overlapping. Supposing that the locking range for the second step, i.e., the injection locking, is $f_{ref} \pm \Delta f$, then the first step, i.e., the 4-path mixer based frequency tuning, should

guarantee its output frequency falls in the range of injection locking. Otherwise, injection pulling will happen and the output frequency will be alleviated from the desired value.

Thus, we will perform the theoretical analysis for the injection locking first and then the 4-path mixer based frequency tuning can be designed accordingly to make sure that injection locking can be achieved.

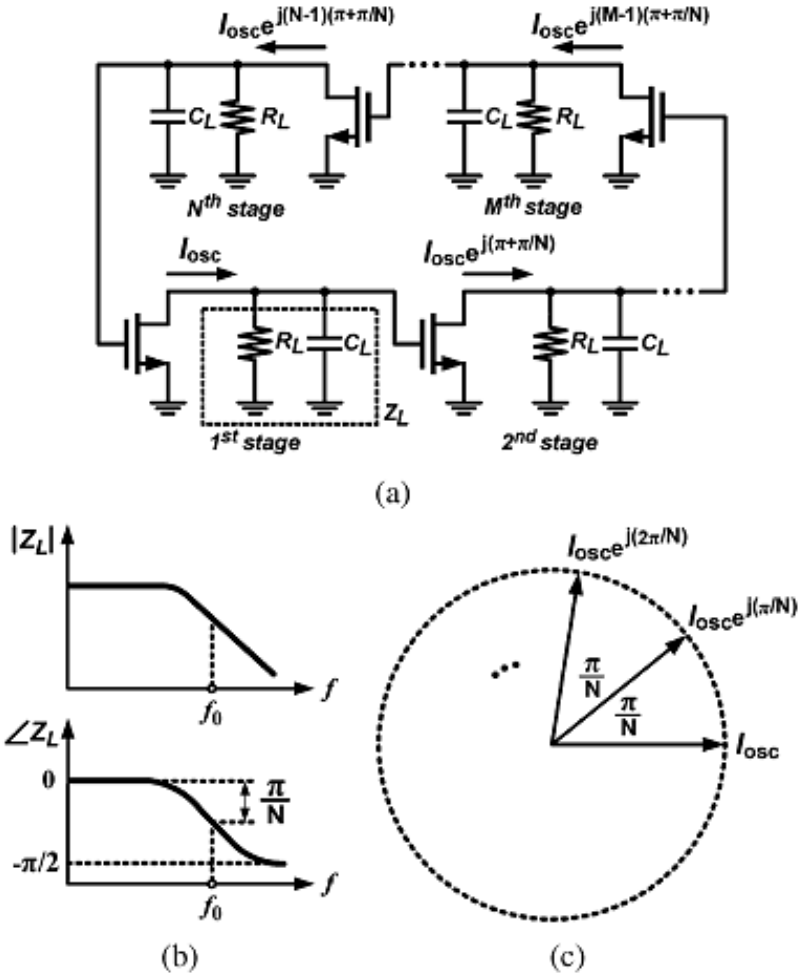


Fig. 4-1-3 (a) Simplified model for *N*-stage ring oscillator without injection (b) Bode diagram for the *RC* load (c) Current phasor diagram [62]

Fig. 4-1-3(a) depicts the simplified model for an *N*-stage single-ended ring oscillator, where *N* must be an odd integer. Every stage of the oscillator can be modeled as a current source loaded by a resistor R_L and a capacitor C_L. Because each current source will change the polarity of the signal, in total, all the current sources generate a phase shift of $N\pi$. Also, the Barkhausen criteria must be satisfied by the loop so that the oscillator can function properly, which means that the total phase shift of the loop must be multiple of 2π. As the load of every stage is identical, each of them must provide a phase shift valued as $(-\pi/N)$. Thus, the oscillator will free-run at a center frequency as f_0 where the load network provides such phase shift as shown in Fig. 4-1-3(b). It is worth noting that we assume the total amplitude gain is greater than 1 in this case. In Fig. 4-1-3(c), the current phasor diagram for the free-running oscillator is shown.

As discussed in Chapter 2, if a signal with a certain frequency near to the free-running frequency of the oscillator is injected into the loop, the oscillator will operate at the injected frequency rather than its free-running frequency. And in this way, an accurate output frequency can be obtained. Fig. 4-1-4(a) depicts the simplified model for the *N*-stage ring oscillator with single injection at the first stage and the injection signal is I_{inj}.

Supposing that the injected signal can successfully lock the oscillator and the oscillation frequency is $f_0+\Delta f$ now. As shown in Fig. 4-1-4(b), at the new oscillation frequency, an additional phase shift valued as θ is added on the phase at f_0. In addition to the phase change due to the new oscillation frequency, the injection signal provides another

phase shift ϕ as shown in Fig. 4-1-4(c). Taking all these phase changes into consideration, the following equation must hold to satisfy the Barkhausen criteria

$$\left(\pi + \frac{\pi}{N} + \theta\right) \bullet N + \phi = 2k\pi, \tag{4-1-2}$$

where *k* is an integer number.

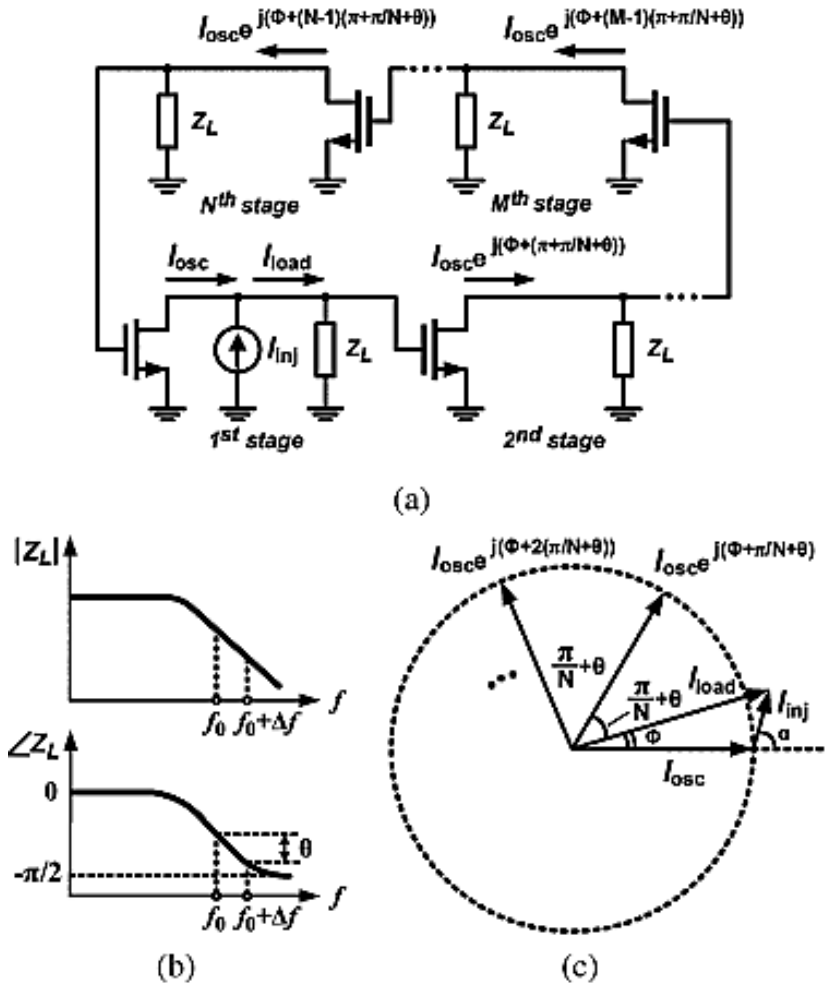


Fig. 4-1-4 (a) Simplified model for *N*-stage ring oscillator with single injection (b) Bode diagram for the *RC* load (c) Current phasor diagram [62]

As N is an odd integer, if θN and ϕ can cancel each other, (4-1-2) will always be true. Thus, the relation between θ and ϕ can be given by follows

$$\theta = -\frac{1}{N}\phi. \tag{4-1-3}$$

Now we can investigate θ and ϕ separately and relate them with (4-1-3) to determine the locking range in the case of single injection. For the following analysis, we assume that the amplitude of the injected signal is pretty small, which is usually the case when we inject a signal to the oscillator.

We can apply the law of sines to the triangle in Fig. 4-1-4(c) and it gives

$$\frac{sin\,\phi}{|I_{inj}|} = \frac{sin(\alpha-\phi)}{|I_{osc}|}. \tag{4-1-4}$$

Due to the small amplitude assumption of I_{inj}, we can also infer that the phase shift ϕ which is caused by the small injection signal is also very small. Thus, we can approximate sin ϕ with ϕ and cos ϕ with 1 and (4-1-4) can be rearranged as follows

$$\phi = \frac{|I_{inj}|\,sin\,\alpha}{|I_{inj}|\,cos\,\alpha+|I_{osc}|}. \tag{4-1-5}$$

For a certain injection amplitude $|I_{\text{inj}}|$, the maximum achievable phase shift ϕ is obtained when the phasor I_{inj} and I_{load} are orthogonal. And in such case, the ϕ_{max} is given by the following equation

$$\phi_{max} = \frac{|I_{inj}|}{\sqrt{I_{osc}^2-I_{inj}^2}}. \tag{4-1-6}$$

From the *RC* Bode diagram in Fig. 4-1-4(b), we can write the relation between the phase and frequency as follows

$$tan^{-1}\left(\frac{f}{f_0}\right) = \frac{\pi}{N} + \theta, \tag{4-1-7}$$

where f_0 is the free-running frequency of the oscillator and f is a frequency close to f_0.

By applying Taylor series to (4-1-7) around f_0 and ignoring the higher order derivatives, we can express θ as follows

$$\theta \approx \frac{tan\frac{\pi}{N}}{1+tan^2\frac{\pi}{N}} \bullet \frac{\Delta f}{f_0}, \tag{4-1-8}$$

where Δf is f-f_0 and it indicates the locking range of the oscillator.

Finally, by substituting (4-1-6) and (4-1-8) to (4-1-3), we can have the locking range being expressed as follows

$$\frac{\Delta f}{f_0} \leq \frac{1}{N} \bullet \frac{1+tan^2\frac{\pi}{N}}{tan\frac{\pi}{N}} \bullet \left|\frac{I_{inj}}{I_{osc}}\right| \bullet \left(1 - \left|\frac{I_{inj}}{I_{osc}}\right|^2\right)^{-\frac{1}{2}}. \tag{4-1-9}$$

As discussed before, now we need to study the behavior of the 4-path mixer and to find out the reference voltage which can tell us if the input frequency is close enough to the reference frequency or not. In Chapter 3, the transient response of the 4-path filter has been studied. Actually, the analysis was done based on the assumption that the load capacitor of the 4-path filter is so small that we can ignore it. Thus, the results obtained for the baseband filtering capacitor voltage are also valid in the 4-path mixer case.

Ideally, the reference voltage can be simply set to the value given by (3-2-22), which indicates the voltage level in the case where the input voltage is exactly equal to the reference voltage. However, in practice, there are always non-idealities such as the limited resolution of the comparator, the energy loss on the parasitic resistance, etc. These factors will affect the eventual voltage level and we must allow some margin during the design.

Thus, we also need to find out the relation between the voltage and frequency when the input frequency is not equal to the reference frequency.

To do that, we can make use of the spectrum of the N-path filter given by (2-1-2). Note that because (2-1-2) is derived for the N-path filter without any load capacitor, we can also apply it in the case of N-path mixer. Also, the envelop of the N-path filter's output is equivalent to one of the baseband filtering capacitors' voltage. Thus, the amplitude of the frequency response in (2-1-2) can give us the information between voltage and frequency for the N-path mixer. From (2-1-2), we can see that $H_0(f)$ is the desired filtering characteristic without any translation. The expression for $H_0(f)$ can be derived as

$$H_0(f) = \frac{N}{1+jf/f_{rc}}\left(D + \frac{1+exp(j\pi(1-2D)f/f_s)}{2\pi f_{rc}/f_s}\right) \times \left(-\frac{exp(j2\pi Df/f_s)-exp(-2\pi Df_{rc}/f_s)}{exp(j\pi f/f_s)+exp(-2\pi Df_{rc}/f_s)}\frac{1}{1+jf/f_{rc}}\right), \quad (4\text{-}1\text{-}10)$$

where N is the number of paths, which equals 4 in our design, $f_{rc} = 1/(\pi RC)$, f_s is the switching frequency and D is the duty cycle of each path.

Now we can give the design procedure for the proposed two-step locking frequency synthesizer. First, we need to determine the locking range of the injection-locking oscillator based on (4-1-9) and find the maximum and minimum frequencies f_{max}/f_{min} for the oscillator to be locked. Then, we can determine a voltage level V_{ref} by substituting f_{max}/f_{min} to (3-2-22) and (4-1-10). Finally, we give a little bit margins to the value of V_{ref} and set it as the reference voltage of the comparator in Fig. 4-1-1. Following these steps, the injection locking can be guaranteed and thanks to the first calibration accomplished by the 4-path

mixer, we can increase the overall locking range as large as we want by increasing the calibration resolution. Here, for the purpose of demonstration, we apply a 5-bit calibration arbitrarily.

The overall locking range for the proposed 2-step locking structure with N-bit calibration is theoretically $(2N+1)$ times of the single injection-locking oscillator as illustrated in Fig. 4-1-5, where $N=3$. Δf is the frequency locking range of the injection locked oscillator calculated from (4-1-9). For current-starved ring oscillator we applied in this design, the oscillation frequency is proportional to the biasing current, so it is easy to set one bit of the digital-controlled-current-source to control $2\Delta f$ oscillation frequency change as shown with the blue range in Fig. 4-1-5. Suppose the initial free-running oscillation frequency is located at the range between $[f_{inj}-7\Delta f, f_{inj}-5\Delta f]$, the 4-path mixer detects that it is outside of the injection locking range and further calibrates the oscillation frequency by changing the control bit one by one. Once (after changing the control bits three times in Fig. 4-1-5) the oscillation frequency is within the range of $[f_{inj}-\Delta f, f_{inj}+\Delta f]$, the first step of calibration is done and injection signal f_{inj} is enabled. And the oscillator can be surely locked as its oscillation frequency is in the locking range. As can be seen, with the 2-step calibration mechanism, the locking range can be enlarged from the yellow range to that of the blue range plus yellow range, which is (2 x 3 + 1) times, noting that a higher initial oscillation frequency can also be calibrated with the same procedure.

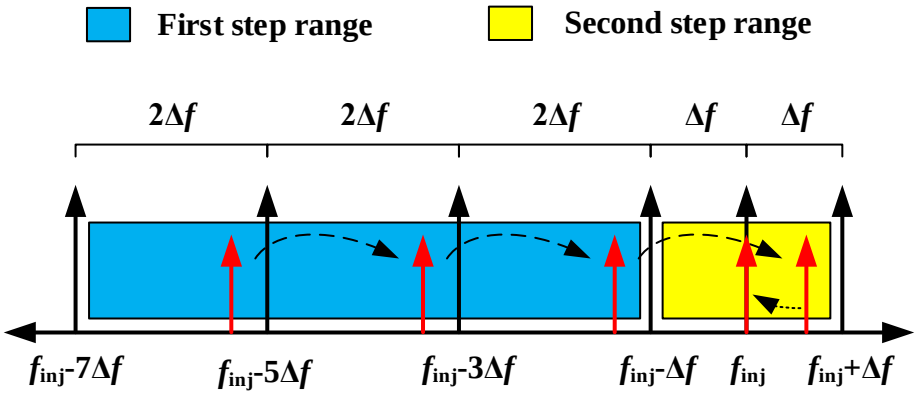


Fig. 4-1-5 The locking mechanism of the proposed 2-step calibration frequency synthesizer

We also want to point out that the $2\Delta f$ frequency step is the ideal choice for the VCO. If the frequency step is smaller, the overall locking range will be smaller. And if the frequency step is larger, it may happen that the 4-path mixer can't calibrate the oscillation frequency to the injection locking range and the desired output frequency can't be reached.

4.2 The Implementation of the Proposed Wide-Locking-Range Frequency Synthesizer

In this design, we would like the final output frequency of the oscillator to be in the range of 401-406MHz or 438-444MHz so that the frequency synthesizer is compatible with the FSK receiver in Chapter 3. And for the sake of simplicity, we choose a division ratio as 64 so the divider circuit is easy to implement. Then we can calculate from (4-1-1) that the f_{ref} should be 13.75MHz, taking the availability of the crystal oscillator into consideration, and this f_{ref} corresponds to an output frequency as 440MHz. In this section, we present the

circuit implementation for the core blocks of the proposed wide-locking-range frequency synthesizer, which are 5-bit calibration circuit, digital-controlled-oscillator and multi-input comparator.

4.2.1 5-bit Calibration Circuit

As discussed in previous section, the calibration circuit is used to generate control bits to adjust the current source and further change the oscillating frequency of the oscillator when the free-running frequency is not close to the reference frequency and to lock the control bits for the current source when the oscillating frequency is close enough to the reference frequency and the injection locking is possible.

In this design, we apply a 5-bit SAR for the calibration function. The calibration circuit accepts the comparison result from the multi-input comparator as input and it outputs 5 control bits to change the bias current of the ring oscillator. Also, the calibration circuit should be able to fix the generated control bits and newly generated bits should not affect the status of the previously generated bits. And the calibration automatically stops once all the 5 control bits are generated and the comparison result can’t change the control bits anymore.

The 5-bit SAR is composed of 6 registers, 5 OR gates and 1 AND gate as shown in Fig. 4-2-1. The composition of a single register is given in Fig. 4-2-2 and the truth table of the MUX in the register is given in Table 4-2-1. Based on these, we can analyze how the control bits are generated properly.

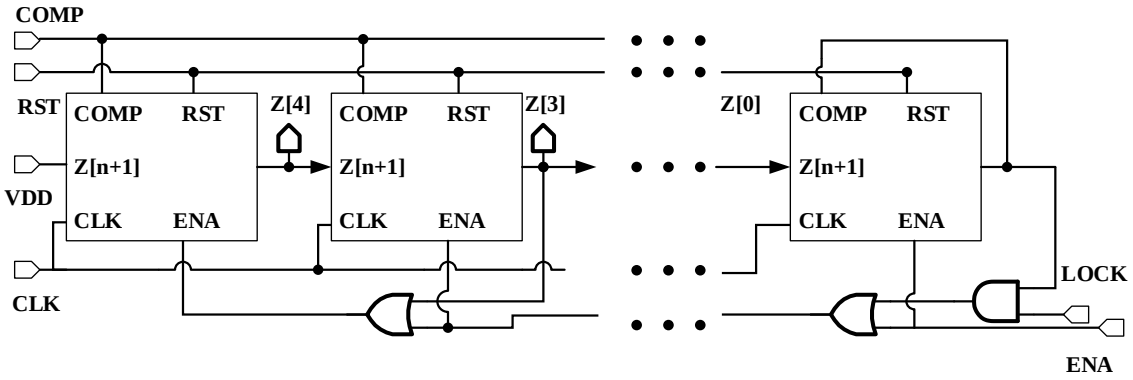


Fig. 4-2-1 Schematic of the 5-bit successive approximate register

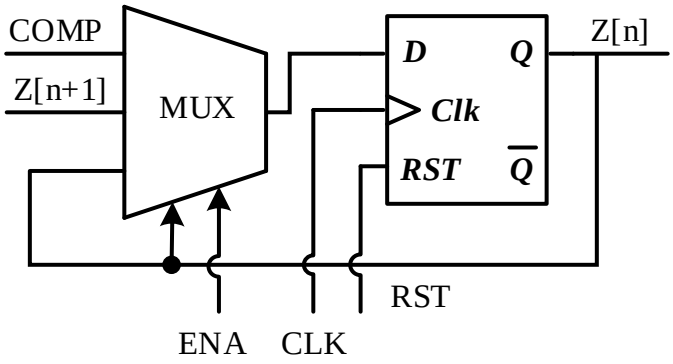


Fig. 4-2-2 Schematic of the register

Table 4-2-1 Truth table of the MUX in the register

ENA	Z[n]	Mux out
1	X	Z[n]
0	1	COMP
0	0	Z[n+1]

At the very beginning, the high-level reset signal RST reset all the control bits Z[4:0] to be 0. When the RST is low, the calibration process will start. Meanwhile, the enable signal ENA and the lock signal LOCK should both be 0. Before the first rising edge, Z[4] is 0 and the ENA signal for the first register is also 0, thus, according to the truth table, Z[4] will switch to 1 at the first rising edge and all the other outputs will be kept at 0. Then, before the second rising edge, Z[4] is 1 and the ENA signal for the first register is still 0. Therefore, Z[4] will change to the value of COMP at the second rising edge, which means that the first control bit has been generated. Meanwhile, for the second register, Z[3] and its ENA are both 0 before the second rising edge and Z[3] will change to 1 at the second rising edge. Before the third rising edge, Z[3] is 1 and thus the ENA signal of the first register also changes to 1 through the OR gate. Thus, the output value of the first register Z[4] keeps to be same. However, as the ENA signal for the second register is 0, Z[3] will change to the value of COMP and the second control bit is generated at the third rising edge. Following the same manner, all the five control bit outputs can be properly generated and locked thanks to the feedback structure in the last register at the sixth rising edge.

We must point out that even the described mechanism can eventually generate and lock the control bits; it will generate an extra positive pulse if the bit value supposes to be 0 as shown in Fig. 4-2-3(d). The solid orange line is the second control bit and its value should follow the value of COMP at the third rising edge, which is 0. However, as can be seen, at the second rising edge, its value changes to 1 and a pulse is generated between the second and third rising edge. As the digital bits are controlling the on/off state of the current

source of the oscillator, an extra pulse of the control bits will disturb the output oscillation frequency, which is undesired during the frequency calibration and may cause wrong judgment of the frequency.

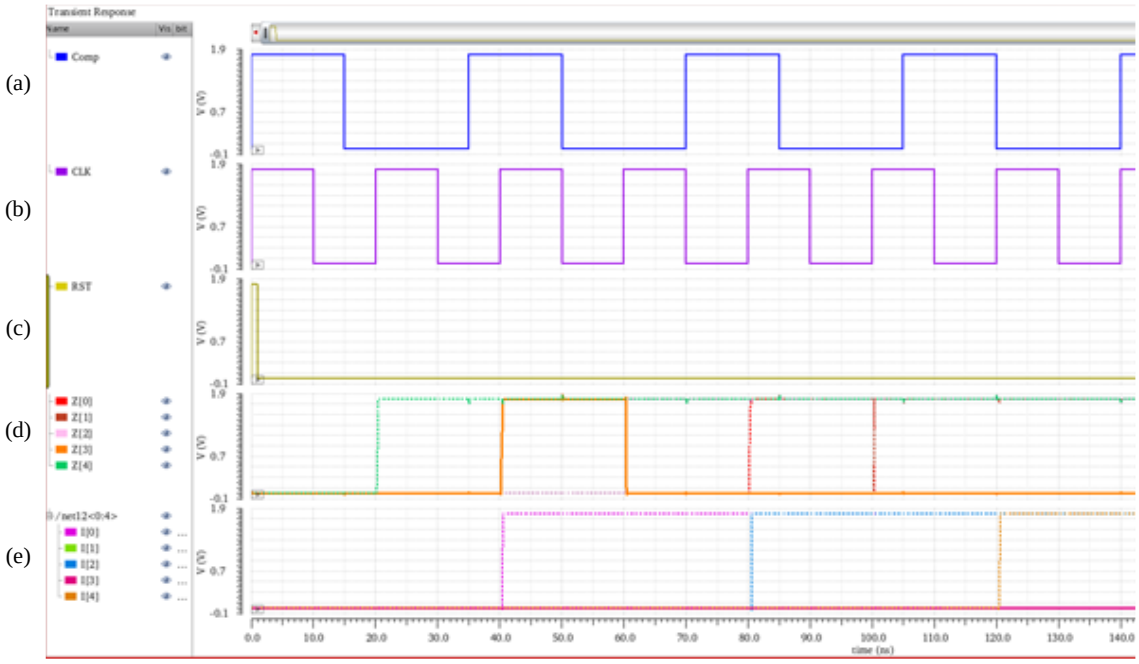


Fig. 4-2-3 Simulated waveforms of control bits generation (a) Comparison input (b) Clock signal (c) Reset signal (d) Control bit signal without pulse elimination (e) Control bit signal with pulse elimination

The extra positive pulse comes from the transfer of VDD, but we can't simply remove it because it is necessary to lock each register. Alternatively, we can eliminate the extra positive pulse by adding a masking circuit at the output. For each control bits, there is a delay of one clock period between the high value caused by VDD and its true value from COMP. Thus, we can apply an additional timing circuit to control the moment when the output bits are available. Ideally, the output moment should be valid only after it copies

the value of COMP. The additional timing circuit is simply composed with a series of flip-flops. At every rising edge of the clock signal, a flip-flop toggles from 0 to 1. Starting from the second rising edge, each toggle of the flip-flop will enable one bit of the output and that bit remains zero before that moment. With such pulse elimination circuit, the extra positive pulse is removed while the other functions of the calibration remain the same as shown in Fig. 4-2-3(e).

4.2.2 Digital Controlled Oscillator

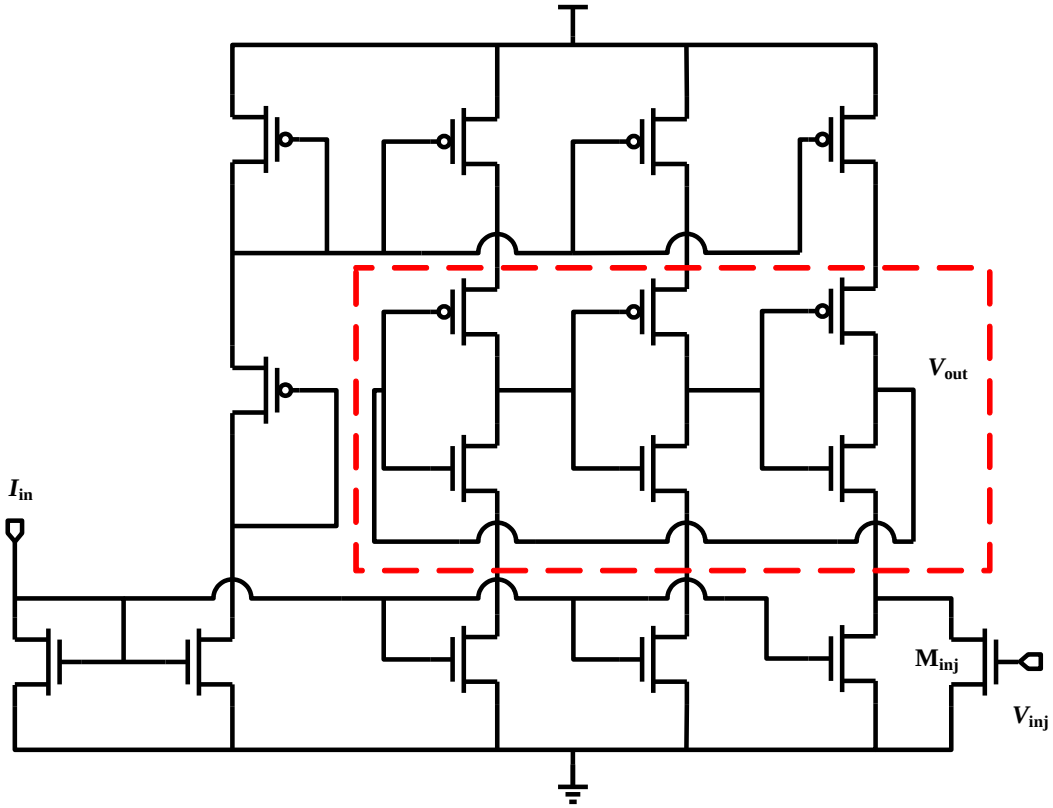


Fig. 4-2-4 3-stage current-starved ring oscillator

For the sake of simplicity and less power consumption, we applied a 3-stage current-starved ring oscillator as shown in Fig. 4-2-4. The core of the oscillator is circled by the red dotted line, while other transistors are providing the bias current from I_{in}. With the biasing circuit, the current flowing through each branch of the transistor can be easily controlled, and so as the output frequency. The injection current is generated by the injection transistor M_{inj} with its gate signal V_{inj}. Note that V_{inj} is only applied to M_{inj} after the first calibration is done.

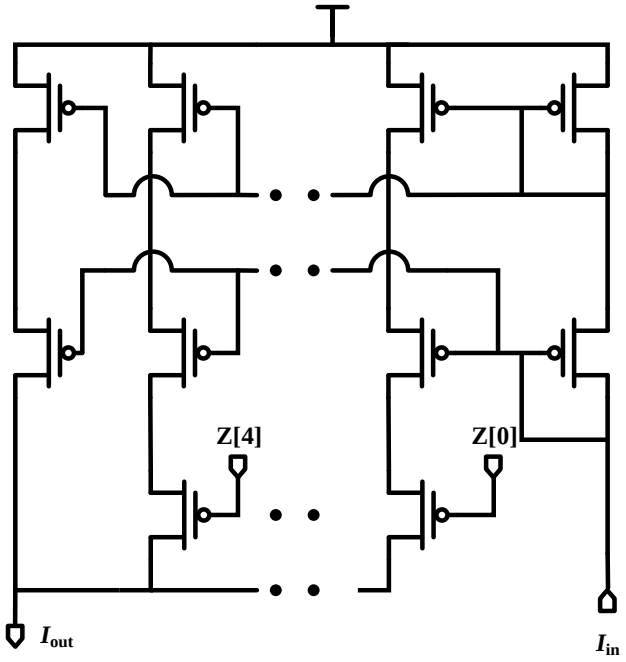


Fig. 4-2-5 Cascaded 5-bit digital-controlled current source

Fig. 4-2-5 depicts the schematic of the cascaded 5-bit digital-controlled current source, which is used to provide bias current to the oscillator according to the control bits generated by the calibration circuit. As can be seen, the current source has in total 7

branches, the right most branch is the reference current, which is provided externally in current design for simplicity. However, the reference current can be generated on the chip. The left most branch is always on and it's necessary for the oscillator to work in the case that all the control bits are 1. In the middle, there are 5 branches which are controlled by the control bits Z[0] to Z[4].

For a 3-stage oscillator and let the injection strength (I_{inj}/I_{osci}) to be 0.02, we can have the value of the locking range based on (4-1-9), which is 0.0154. For a carrier frequency as 440MHz (in the purpose to be adaptive with the FSK receiver in Chapter 3), we need to calibrate the oscillator frequency to the range of 440±6MHz for it to be successfully injection locked. Noting that the oscillator will be divided by 64 before feeding to the 4-path filter as discussed in Section 4.1.1, the locking range for the 4-path mixer shall also be divided by 64.

4.2.3 Multi-Input Comparator

A multi-input comparator is needed because of the fact that the 4-path mixer has four outputs and each of them may have a high voltage level indicating that the input frequency is close enough to the reference frequency.

Fig. 4-2-6 depicts the output waveforms of the 4-path mixer with 13.75MHz reference frequency and 6.96875MHz (obtained from (440+6)/64) input frequency, noting that due to the divide-by-2 property of the 4-path phase generator, the 4-path mixer is distinguishing the input frequency with half of the reference frequency, i.e., 6.875MHz. As can be seen, the achievable maximum voltage level is the same for all the four outputs.

Thus, no matter which output exhibits a voltage higher than reference, we can say that the first step calibration is done. Suppose the reference voltage is 1.1V, which is indicated in each graph by the horizontal line, we can see that there are time windows for each of the output when the voltage is higher than the reference as marked by “1” “2” “3” “4” “5”. If we only apply a single input comparator, saying to only compare O_4 with the reference, the comparator must wait from the end of time window “1” to the beginning of the time window “5” in the worst case, which means a longer delay for the eventual locking of the oscillator. By applying multi-input comparator, on the contrary, there are more effective time windows and the worst-case delay time can be shortened a lot. Thus, a multi-comparator is preferred for the immediate judgment.

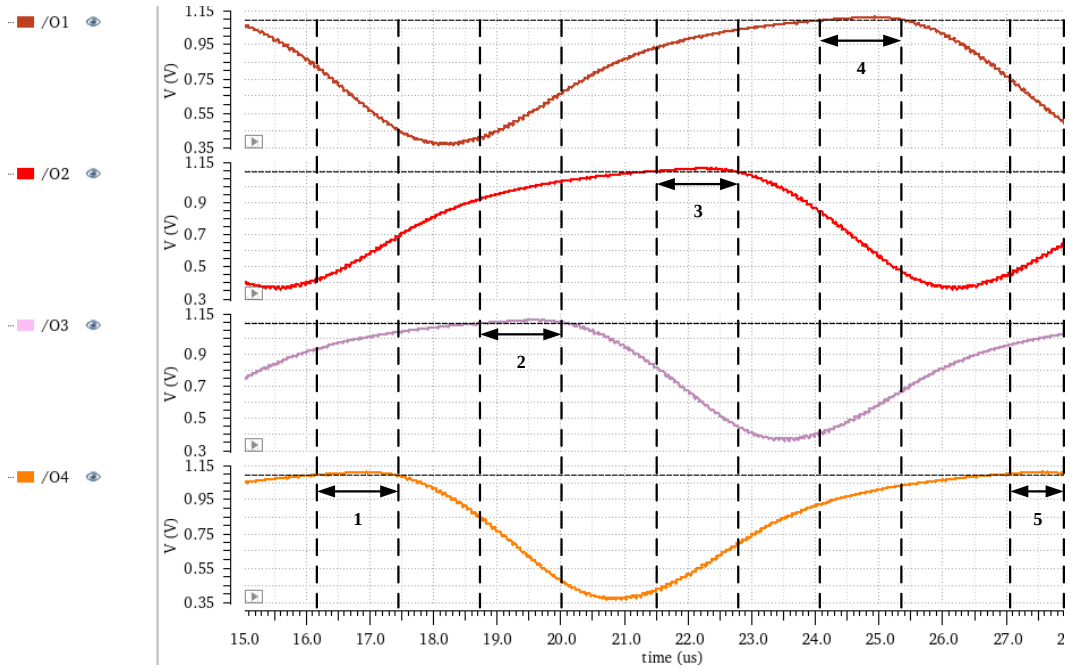


Fig. 4-2-6 Transient waveform of the output of the 4-path mixer

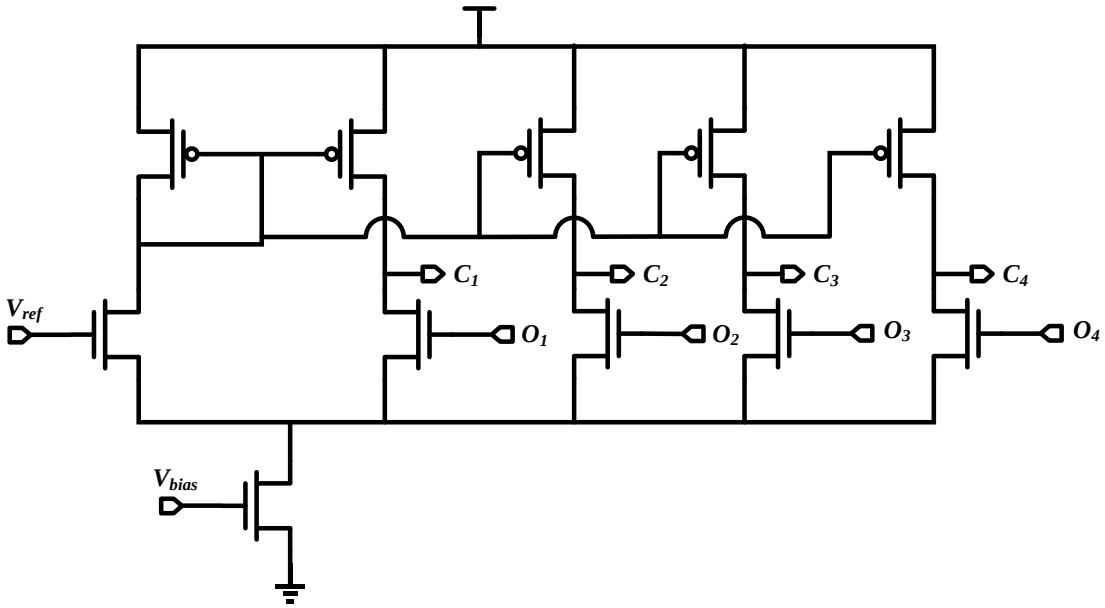


Fig. 4-2-7 Multi-input comparator

Fig. 4-2-7 shows the circuit implementation of the multi-input comparator. It consumes less power than four single comparators because only one tail current is applied. The multi-input comparator is responsible to detect either of the input O_1-O_4 exceeds the reference voltage V_{ref}. Thus, besides the comparator, a 4-input OR gate for C_1-C_4 is needed.

By choosing the reference frequency to be 13.75MHz and the locking range to be 6.875±0.09375MHz, we can determine the value of the reference voltage according to (3-2-22) and (4-1-10), which is 1.1V.

4.3 Simulation Results

The proposed frequency synthesizer has been designed and laid out in 180nm CMOS process and the simulation results are shown and discussed in this section.

The layout of the core circuit of the proposed frequency synthesizer is given in Fig. 4-3-1. It takes an area of 220μm x 190μm.

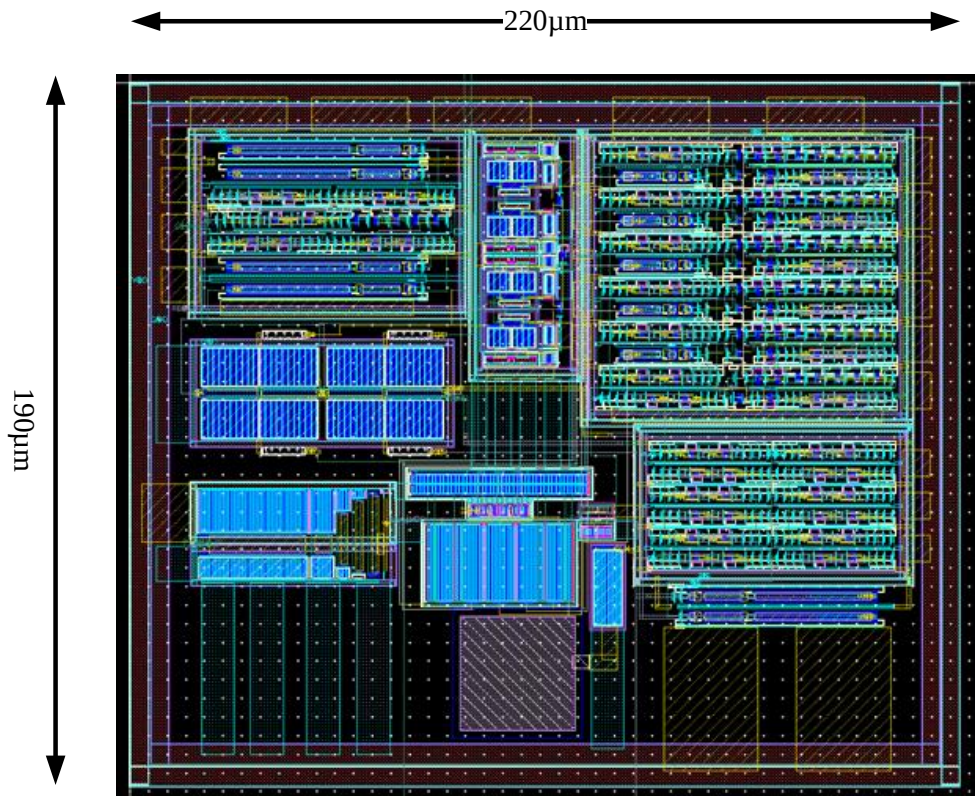


Fig. 4-3-1 Layout for the core circuit of the proposed frequency synthesizer

Fig. 4-3-2 gives the post-layout simulation results for the proposed frequency synthesizer. O_1, O_2, O_3 and O_4 are the output signals of the 4-path mixer. *CLK_HT* is an

internal clock signal for the 5-bit calibration circuit generated by dividing the output frequency of the oscillator, and it has a much larger period comparing to the reference clock because we need to make sure that the 4-path mixer works in steady state between two rising edges of *CLK_HT*. *COMP* is the output of the multi-input comparator and *I*[0:4] are the control bits for the digital-controlled current source. LOCK is the control signal to end the 1st calibration and to start the 2nd calibration.

As can be seen, the frequency synthesizer works in two calibration phases. During the first phase, at each rising edge of the *CLK_HT* signal, a new control bit for the current source is generated according to *COMP*. The change of the control bit will make the output frequency of the oscillator to be closer to the reference frequency, which can be observed through the larger amplitude of the 4-path mixer output O_1-O_4 as indicated in Fig.4-3-2. Once *COMP* goes to 0 from 1 after detecting a voltage higher than the pre-set reference voltage from either one of O_1-O_4 , which indicates that the output frequency of the VCO is close enough to the reference frequency, *LOCK* signal is enabled, and the frequency synthesizer goes to the 2nd calibration phase. The *LOCK* signal has two functions. First, it locks the output bits of the calibration circuit, i.e., *I*[0:4], so that any further comparison results will not affect the control bits. As can be seen from Fig. 4-3-2, the change of the *COMP* signal in the second calibration phase doesn't make any change to *I*[0:4]. Second, it closes the switch between injection signal and VCO so that the injection locking is realized.

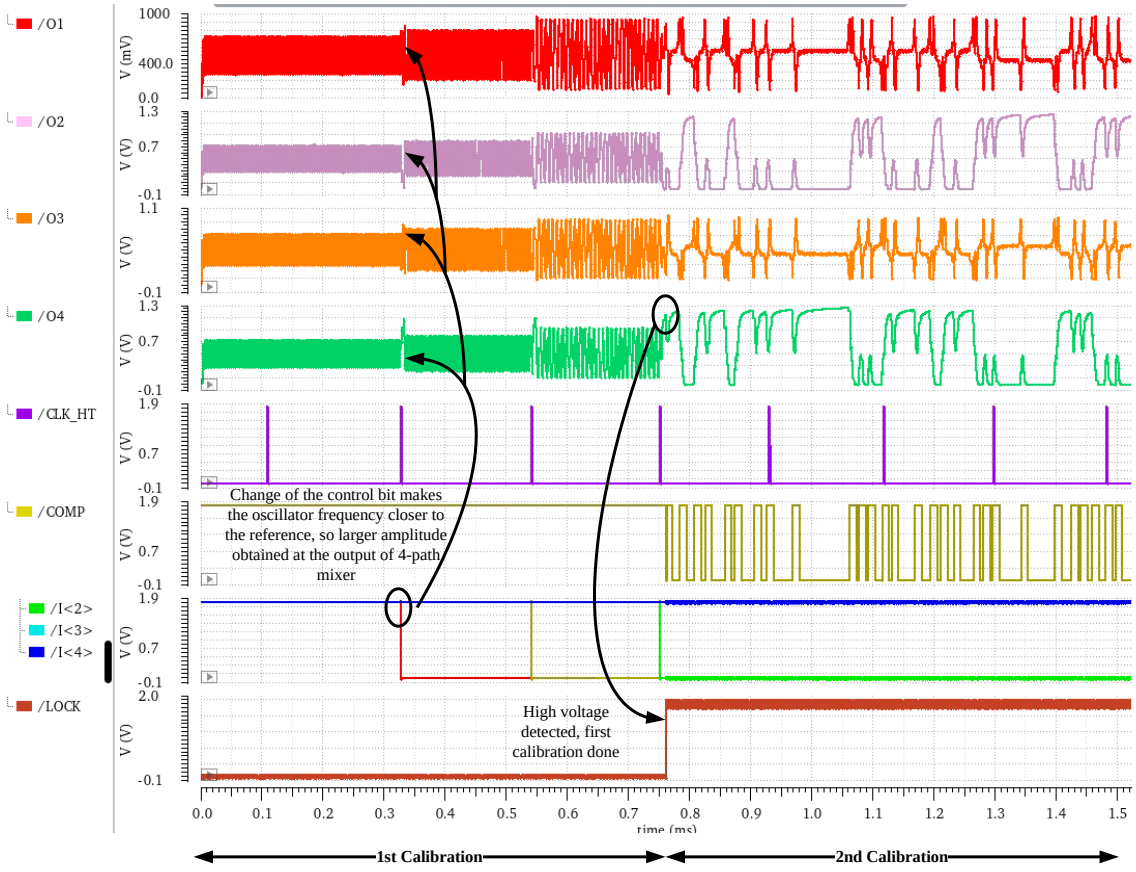


Fig. 4-3-2 Simulation results for proposed frequency synthesizer

Fig. 4-3-3 plots the output spectrum after the second step of calibration, i.e., the injection locking, is stabilized. As can be seen, the output frequency is centered with 440MHz, meaning that the oscillator is successfully injection locked.

Fig. 4-3-4 gives the phase noise plot in the same condition with that of Fig. 4-3-3. The simulated phase noise at 1MHz offset is -124.86dBc/Hz and it is -97.45dBc/Hz at 100kHz offset. And the integrated RMS jitter from 10KHz to 40MHz is 2.5ps.

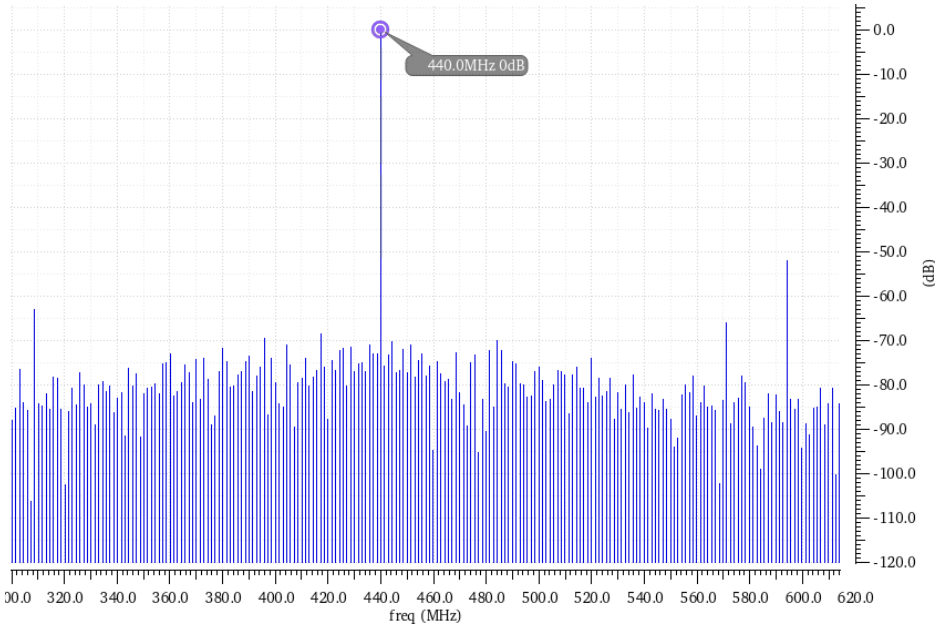


Fig. 4-3-3 Output spectrum when the frequency synthesize is locked

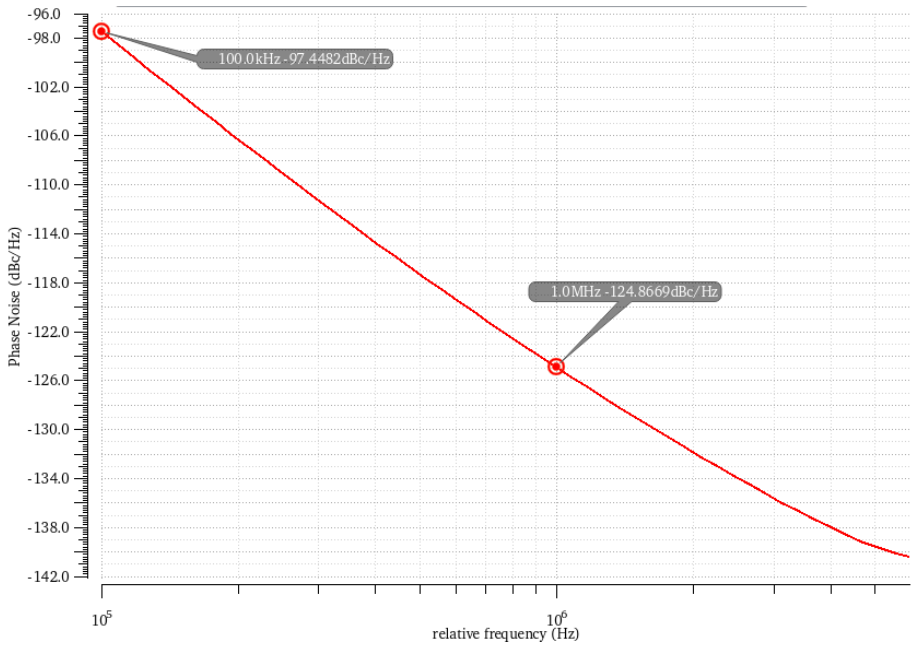


Fig. 4-3-4 Simulated phase noise of output signal

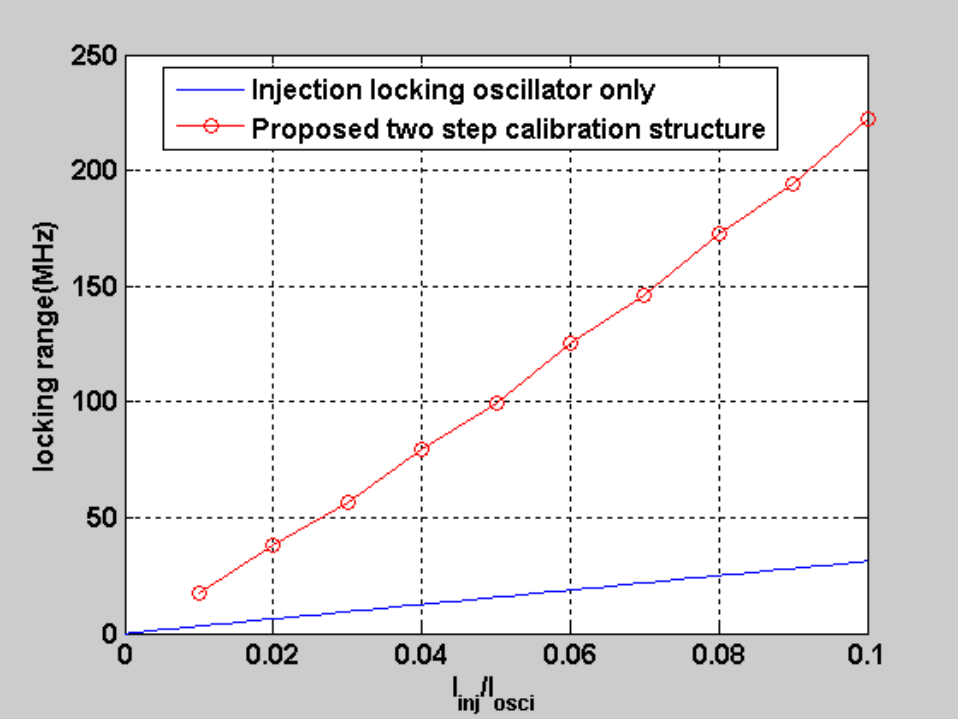


Fig. 4-3-5 Locking range comparison between the proposed structure and conventional injection locking

Fig. 4-3-5 plots the locking range versus different injection strength for the proposed two-step calibration structure and the proposed technique can effectively improve the locking range comparing with the conventional injection locking oscillator. Note that the simulated results show that the effective amplification of the locking range is less than the theoretical value. This is due to the non-idealities introduced by the current mirror and the switches.

The performance comparison with other recent frequency synthesizer publications is given in Table 4-3-1. Noting that even the design example we gave in Section 4.2 is for 12MHz locking range with an injection strength with 0.02, which is an injection power as

low as -35dBm, for the purpose of comparison with other publications, whose minimum injection power is usually -20dBm, i.e., injection strength equal to 0.1, we report the locking range with such injection power in Table 4-3-1. Thus, the locking range is obtained by $f_{center}\pm\Delta f$ with f_{center}=440MHz and $2\Delta f$=220MHz (refer to Fig.4-3-5 for 0.1 injection strength).

Table 4-3-1 Performance comparison

	[148]	[151]	[150]	[149]	This work*
Process	90nm	180nm	65nm	65nm	180nm
f_{ref}	291MHz~ 336MHz	31MHz	100MHz	105MHz~ 129MHz	13.75MHz
Multiplication Factor	3	13	24	64	32
Locking Range	873MHz~ 1.008GHz	399.6MHz~ 406.5MHz	2.2GHz~ 2.5GHz***	6.75GHz~ 8.25GHz	330MHz~ 550MHz
Power	720μW	107μW	11mW	2.25mW	305μW
Integrated RMS Jitter	N/A	N/A	140fs	190fs	2.5ps
Phase noise @ 1MHz	-110 dBc/Hz @600kHz	-110 dBc/Hz**	-129 dBc/Hz	-119.2 dBc/Hz	-124.9 dBc/Hz
FOM (μW/MHz)	5.3	16.7	36.7	1.5	1.4

*Simulated
** Estimated from the figure
*** Achieved by changing the supply voltage

$$FOM = \frac{Power}{locking\ bandwidth}$$

We can see from the comparison table that our design is competitive in the terms of power consumption and locking range. And it has a best overall FOM value, which

means that the proposed frequency synthesizer can achieve a wider locking range with little power consumption. And we also want to point out that the reference frequency and supply voltage in our design are fixed.

4.4 Conclusion

In this chapter, a low power, high locking range frequency synthesizer with two-step calibration is proposed. The first step is accomplished by 4-path mixer and the second step is realized by injection locking and the locking range of each is analyzed separately. Based on the analysis, we can design the circuit parameters to make the two locking ranges for each calibration be compatible and theoretically the frequency synthesizer can achieve a frequency range as large as we desire by increasing the digital control bits. The chip was fabricated with 180nm CMOS process and the core circuit occupies 220μm x 190μm. The simulation results show that it can successfully lock the output frequency at 440MHz of a free running 3 stage ring oscillator with a power consumption as 305μW. The phase noise at 1MHz offset is -124.86dBc/Hz and it is -97.45dBc/Hz at 100kHz offset. And the integrated RMS jitter from 10kHz to 40MHz is 2.5ps.

Chapter 5
An 83.9% Efficiency Thermoelectric Energy Harvesting System with OTC-PSM Control and Low Hardware-Cost MPPT Algorithm

In Chapter 2, we reviewed the state-of-the-art topologies for energy harvester power management units and noted that almost all the papers apply a "startup – main converter – control unit" strategy. Although the basic idea is similar, much effort is required to handle the low input voltage and achieve high conversion efficiency.

To limit the power in the power MOSFETs and the control block, we propose a MOSFET on-time calibration based pulse skipping modulation (OTC-PSM) scheme in a discontinuous conduction mode (DCM) boost converter. The DCM mode ensures low switching loss while the PSM scheme ensures low conduction loss. The control block is optimized with dynamic comparators and a low-power duty-cycle generator for the gate control signals. Since the dynamic comparators only consume current in a very short time during the whole clock period and the bias current of the duty-cycle generator is only several hundreds of nano-amperes, the whole control block is very power-efficient. Moreover, OTC-PSM brings extra advantages to the boost converter in the aspects of transient response and output ripples. ZCS technique is applied to avoid the power dissipated during the non-ideal dead time.

In addition to power efficiency, another important issue of energy harvester is how to extract as much energy as possible from the energy source. Conventionally, to achieve

maximum power point (MPP) of TEG, the root-mean-square (RMS) value of the input voltage of the converter should be regulated to half the open-circuit voltage of TEG. This requires a comparator to be on during the conduction mode of the main converter, which costs much power. To address this issue, a hardware and power efficient MPPT implementation is proposed specifically for TEG and other energy sources with fixed internal resistance.

The rest of this chapter is organized as follows: Section 5.1 introduces the system architecture and the proposed OTC-PSM and MPPT controlling strategy, the overall working flow is also given in this section. Section 5.2 gives the circuit implementation for core blocks. The experimental results are given in Section 5.3. And conclusions are drawn in Section 5.4.

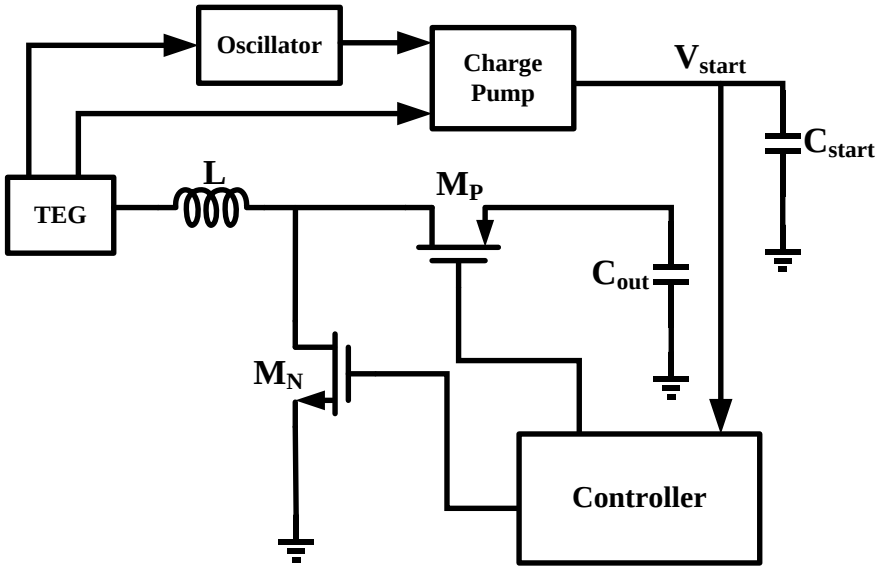


Fig. 5-1-1 Conventional structure of thermoelectric energy harvester

5.1 System Architecture and Control Strategy

A widely used structure of thermoelectric energy harvester is shown in Fig. 5-1-1. The harvester is formed with an oscillator, a charge pump, a controller and a main boost converter. The controller is used to generate the gate signal with proper dead time and enough driving ability to control the power MOSFETs M_N and M_P. The oscillator and charge pump serve as the start-up circuit. The oscillator firstly generates a clock signal whose amplitude could only be 100mV. With this clock signal, the charge pump boosts the low input voltage to about 1V. Then, the startup capacitor C_{start} provides the supply voltage to the controller to activate the boost converter. A large capacitance of C_{start} is needed to continuously provide voltage of 1V or higher, which will take a lot of area or require an extra off-chip component. Another drawback of this structure is that the oscillator and charge pump need to work continuously to power the controller, which limits the power available at the output.

5.1.1 Proposed System Architecture for Thermoelectric Energy Harvester

In this research, a new architecture is proposed as shown in Fig. 5-1-2, which consists of a start-up circuit, controller and main boost converter. The goal of the system is to raise the small input voltage to a regulated output of 1.2V.

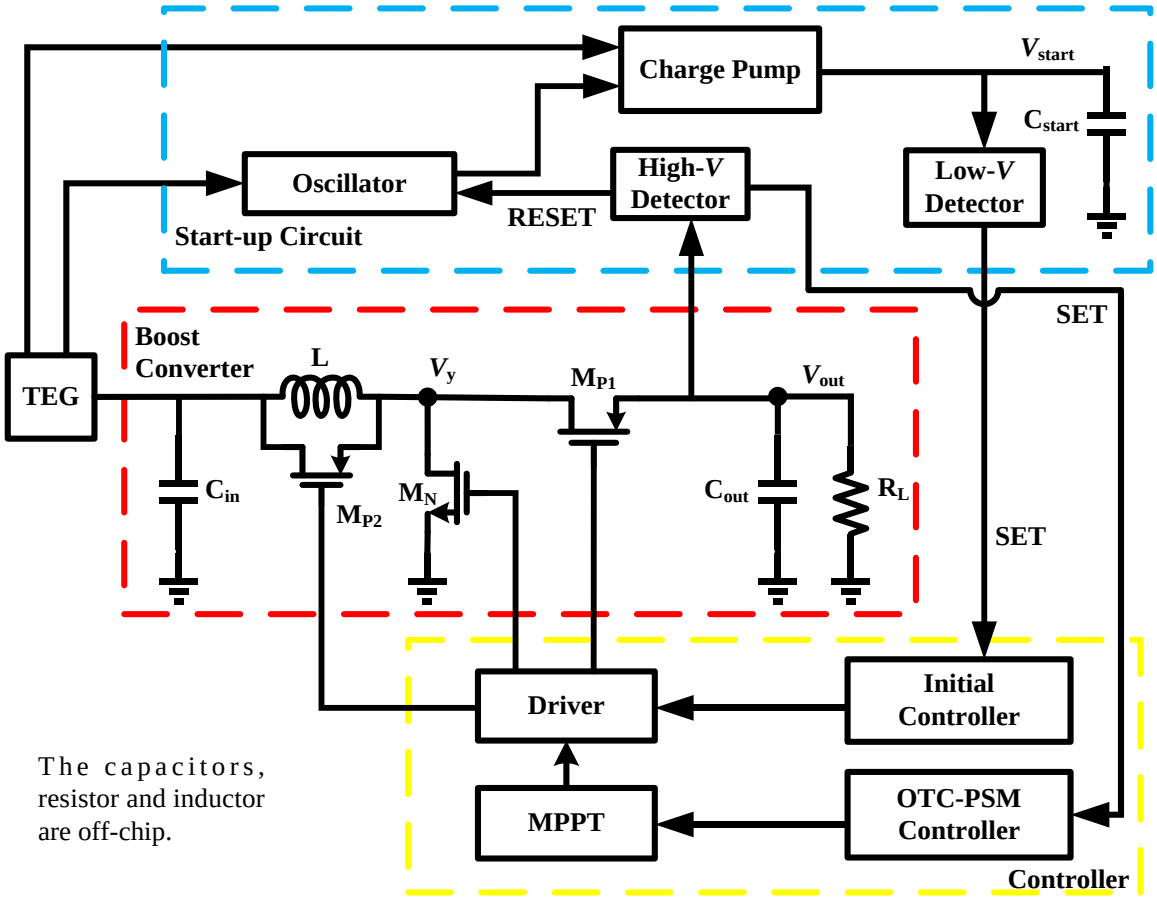


Fig.5-1-2 System architecture of the proposed thermoelectric energy harvester

The operation of system is divided into three phases. First one is the start-up phase, during which only the oscillator and charge pump are activated. What is different from the conventional startup phase is that the charge pump only needs to boost the input voltage to more than 500mV. The voltage detectors (Low-*V* and High-*V* Detectors) act as switches controlled by the level of input voltage. The detector needs no reference voltage and has very low power consumption. Once the voltage V_{start} exceeds 500 mV, the Low-*V* Detector sends a SET signal to Initial Controller and the system shifts to the second phase of pre-

boost. In this phase, C_{start} provides supply voltage V_{start} to the initial controller and the latter one generates a duty-cycle signal to drive M_{P1} and M_N. The generated duty-cycle signal in this phase is to activate the boost converter and get a higher voltage at C_{out}, thus, it's not necessary to regulate the duty-cycle signal very well. As soon as V_{out} gets higher than 1V, the high-V detector resets the oscillator, which means the path from C_{start} to the controller is disabled. Then, the output capacitor C_{out} begins to supply the controller and the system enters the third phase, which is the steady-state phase. In this phase, the gate control signals for the MOSFETs are optimized for MPPT and better conversion efficiency.

5.1.2 OTC-PSM Control Strategy

Due to the input power from the TEG is very little and the load current is light, the boost converter works in DCM for a higher conversion efficiency. In DCM, there are three different operation stages according to the situation of inductor current.

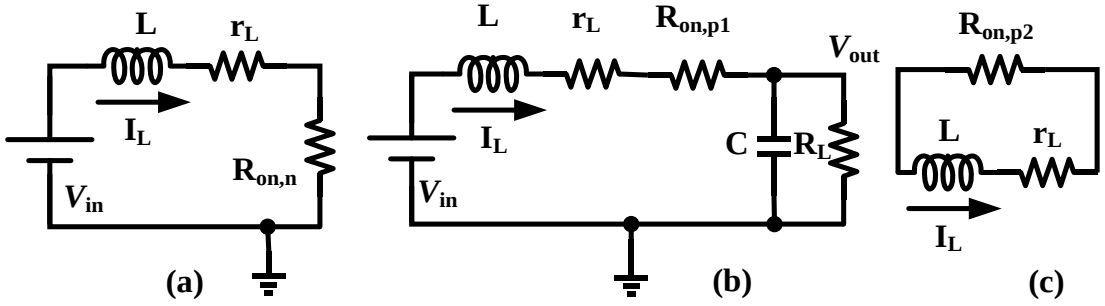


Fig.5-1-3 Equivalent circuits in different phases of boost converter in DCM (a) on-time of M_N (b) on-time of M_{P1} (c) on-time of M_{P2}

First, during the on-time of M_N, it can be modeled as shown in Fig. 5-1-3 (a). In this case, the inductor current increases. Then, M_N turns off and M_{P1} turns on as shown in

Fig. 5-1-3(b), and the inductor current decreases. Fig. 5-1-3(c) shows the last phase, when M_{P1} and M_N are both off and M_{P2} is on to cancel any residue current in the inductor and the inductor current keeps being zero. Otherwise, the residue current in the inductor after M_{P1} turning off will result in oscillation at V_y, which will introduce more power consumption and may cause error for the on-time calibration.

Actually, the best moment for M_{P1} to turn off is when the inductor current reaches zero from a positive value. If M_{P1} doesn't turn off properly, the boost converter will suffer serious power loss. Assuming M_{P1} turns off too early, the discharging period of inductor doesn't finish at the off-moment. Then, the inductor current forces the parasitic diode of M_{P1} to turn on, so V_y becomes even higher than output voltage in the short while after M_{P1} is off. If the off-moment of M_{P1} is late, the inductor current will firstly become zero and then the output capacitor will begin charging the inductor reversely because the output voltage is higher than input voltage. After M_{P1} turns off, the negative inductor current forces the parasitic diode of M_N to turn on and produces a voltage drop on V_y. Both wrong off-time conditions bring the extra energy consumption. The different off-time scenarios are shown in Fig. 5-1-4.

To ensure that M_{P1} turns off at correct moment, one approach is to compare V_y and V_{out} at the off-moment of M_{P1}. According to the comparing result, t_2 (the on-time of M_{P1}) will be increased or decreased in next period to achieve ZCS.

If the off-moment of M_{P1} could be optimally adjusted, the following equation will hold

$$\frac{t_1}{V_{out}-V_{in}} = \frac{t_2}{V_{in}}, \tag{5-1-1}$$

where t_1 is the on-time of M_N and V_{in} is the input voltage of the boost converter.

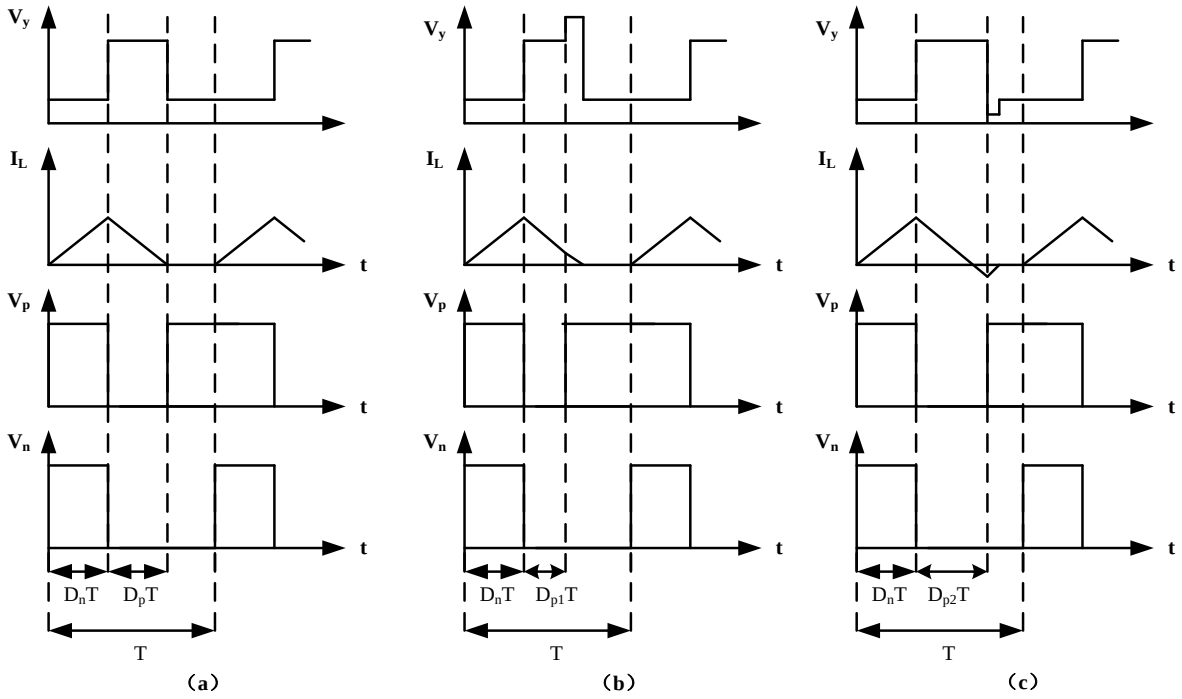


Fig. 5-1-4 PMOS turns off (a) at right moment (b) too early and (c) too late

Different from pulse width modulation (PWM) and pulse frequency modulation (PFM), pulse skipping modulation (PSM) can adapt to the load through skipping clock periods and it shows better conversion efficiency with low input power. In the condition of heavy load or small input, the controller works normally in every clock period. While with light load or large input, the controller will work normally for *m* clock periods and then stop working for *n* clock periods. And the value of *m* and *n* changes according to the load

and input condition. For a traditional PSM controller as shown in Fig. 5-1-5, the on-time of the NMOS and PMOS is set up to be fixed value and output voltage is regulated by tuning the ratio between *m* and *n*. In steady state, *m* and *n* are fixed and the converter works periodically with a period as (*mT*+*nT*), with *T* as the clock period.

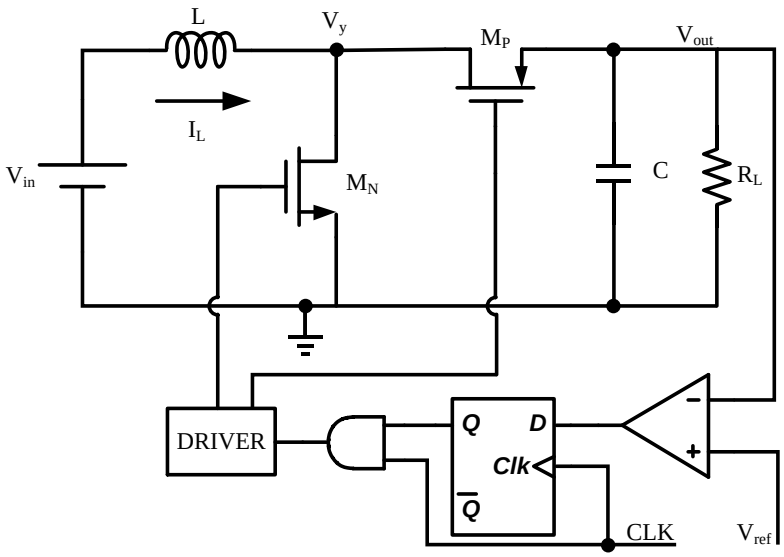


Fig. 5-1-5 Conventional topology for PSM controlled boost converter

To analyze the PSM controlled boost converter in steady-state, we need to take both the working period and sleeping period into consideration. Ideally, according to the energy conservation law, the ratio between the average inductor current and the average output current shall be equal to the ratio between the output voltage and the input voltage in the steady state. Thus, we have the following equation

$$\frac{I_L}{I_{out}} = \frac{V_{out}}{V_{in}}. \tag{5-1-2}$$

In steady state, the average output current is given by

$$I_{out} = \frac{V_{out}}{R_L}. \tag{5-1-3}$$

In a period of (mT+nT), the average inductor current is

$$I_L = \frac{1}{(m+n)T}\left(\frac{1}{2}\left(\frac{V_{in}D_nT}{L} \times \left(D_n + D_p\right)T\right) \times mT\right), \tag{5-1-4}$$

where T is the clock period, D_n and D_p are the duty-cycle for M_N and M_{P1}, respectively. By substituting (5-1-3) and (5-1-4) into (5-1-2), we can have the equation for the boosting factor of PSM controlled boost converter as follows

$$\frac{V_{out}}{V_{in}} = \sqrt{\frac{(D_n+D_p)D_nTR_L}{2L} \times \frac{m}{m+n}}. \tag{5-1-5}$$

Intuitively, by skipping some clock periods, the dissipated power by the power MOSFETs and controller can be decreased. Thus, the general efficiency can be increased. To further increase the conversion efficiency, ZCS requirement given in (5-1-1) shall also be satisfied in the normally working periods. Combining (5-1-1) and (5-1-5), the following equation is found

$$\frac{V_{out}}{V_{in}} = \frac{1}{2} + \sqrt{D_n^2 \times \frac{TR_L}{2L} \times \frac{m}{m+n} + \frac{1}{4}}. \tag{5-1-6}$$

According to (5-1-6), the output voltage could be regulated by calibrating both duty cycle D_n, or the on-time of MOSFET M_N, and the ratio between m and n of PSM. This leads to the proposed OTC-PSM controller, which provides several advantages over the traditional PSM controlling method.

One advantage of OTC-PSM is that the output voltage can recover from a low or high value to the reference voltage more quickly. Fig. 5-1-6 depicts the scenario for the recovering from a low output voltage.

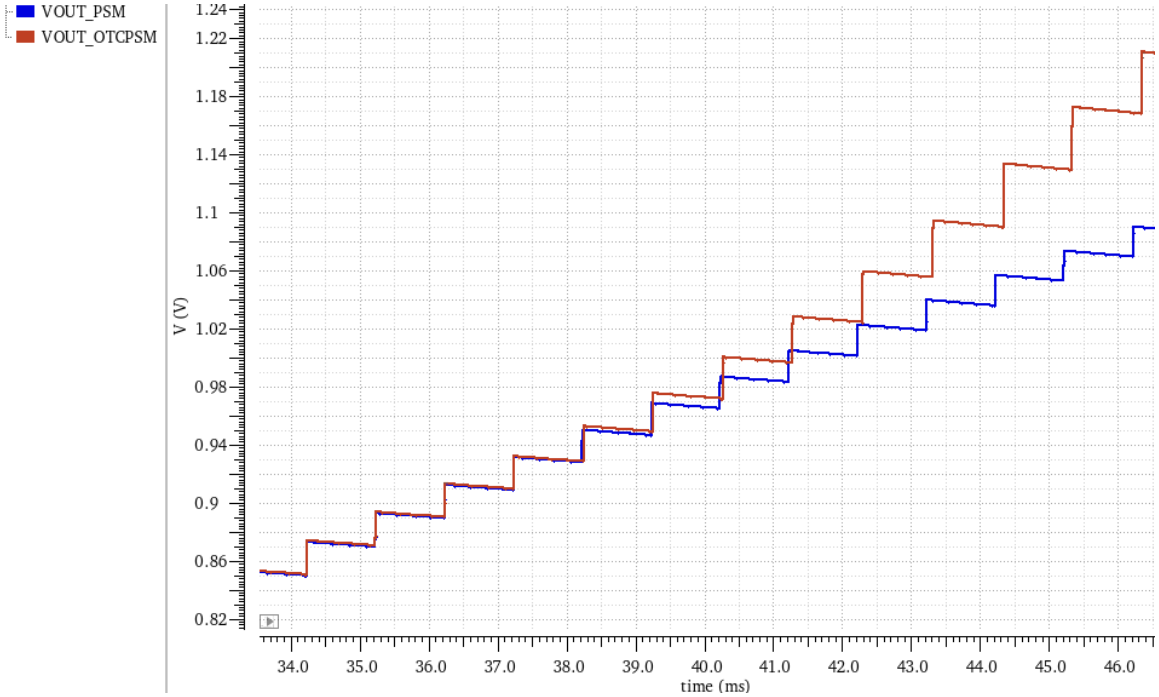


Fig. 5-1-6 Comparison of the output voltage recovering time between OTC-PSM (VOUT_OTCPSM) and traditional PSM (VOUT_PSM)

In the case when the output voltage drops below the reference due to either the decrease of input energy or the increase of load, the on-time of M_N will increase during each period in order to transfer more energy to the output. As a result, the load acquires more energy from each period, i.e., the output voltage can reach the desired value more quickly. On the contrary, the traditional PSM needs more clock periods to regulate the output voltage as the energy transferred to the load is the same within each period due to the fixed on-time. Thus, OTC-PSM control can accelerate the recovering speed of the converter through adjusting the on-time of MOSFETs as shown in Fig. 5-1-6.

Another advantage of OTC-PSM is for the output ripple. For a boost converter operating in PSM, the expression of output ripple is:

$$\Delta V = \frac{\left((1+n)-D_p\right)}{C} \times TI_{out}, \tag{5-1-7}$$

where I_{out} is the load current, D_p is the duty cycle for M_{P1}, which is proportional to D_n because of ZCS requirement, and C is the output capacitance.

If the load current becomes high, the calibration circuit for OTC-PSM would simultaneously increase D_p and reduce n. Comparing to the simple reduction of n in traditional PSM, these two adjustments will compensate the increasing trend of output ripple better and smaller output ripple could be obtained.

5.1.3 The MPPT Strategy

In order to extract as much energy as possible from the energy source in the steady-state, the load of the source, i.e., the input impedance of the main boost converter should be equivalent to the internal resistance of the source. In TEG harvesting systems, the internal resistance of TEG R_T is fixed. And the input impedance R_{IN} of the main boost converter is given by Fig. 5-1-7 as follows

$$R_{IN} = \frac{2L}{t_1^2 f_s}, \tag{5-1-8}$$

where f_s is the switching frequency.

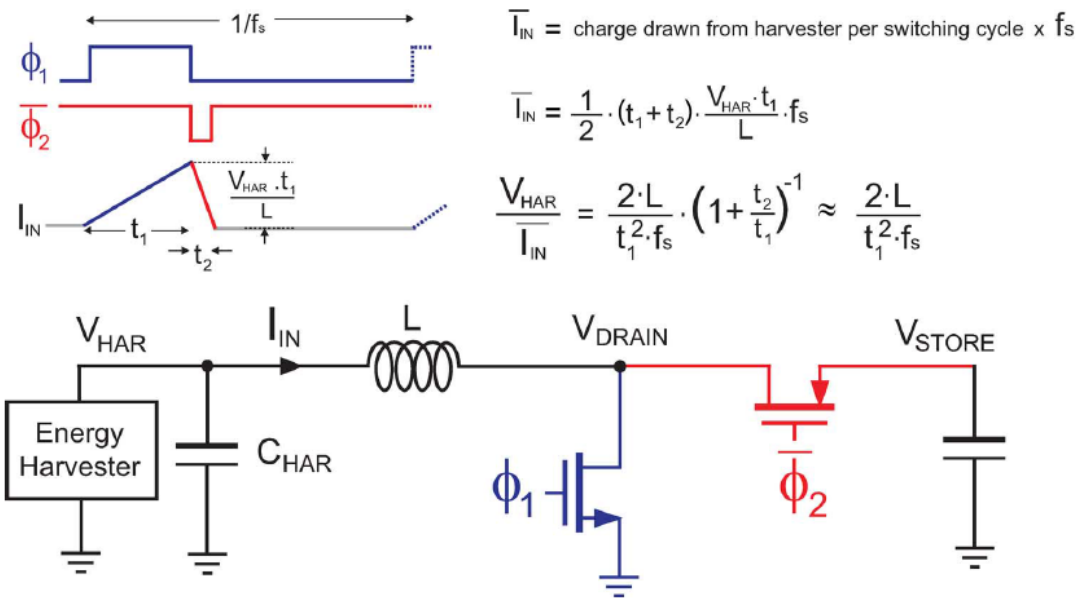


Fig. 5-1-7 Analysis of the input impedance for a boost converter [74]

However, we must point out that (5-1-8) is an approximation in the condition of DCM for the boost converter and the fact that t_1 is much larger than t_2. Fortunately, this situation is satisfied as V_{in} is much smaller than V_{out} in thermoelectric energy harvesting and according to (5-1-1), t_1 will be much larger than t_2. Also, our proposed OTC-PSM control strategy is under DCM.

The most of existing MPPTs use a static comparator to continuously compare the input voltage and the half of the open-circuit voltage of TEG, V_{TEG}. Thus, at least 3 capacitors are needed, two for half of the open-circuit voltage and one for the average input voltage across the transmission cycle. The comparison result is used to tune the duty-cycle or the switching frequency of the transistors to make them equal. In the proposed MPPT strategy, a dynamic comparator is adopted that only works for a short period of time when

M_N is turned off. This saves power as M_N is off for most of the time. In addition, only 2 capacitors are needed instead of 3 because the comparison is made instantaneously at the time when M_N is off. To apply this strategy, we must find out the desired instantaneous value of V_{in}.

The first step is to find out the value of f_s. In addition to (5-1-1) and (5-1-8), another timing constraint condition shall also be satisfied: $t_1+t_2<1/f_s$. Combining these conditions together, we can find the requirement for switching frequency as follows

$$f_s < \frac{R_T}{2L}\left(\frac{V_{out}-V_{in}}{V_{out}}\right)^2. \quad (5\text{-}1\text{-}9)$$

Here, we need a relatively large inductor to limit the input current for a better efficiency. Thus, a 680μH inductance is arbitrarily picked up. Suppose R_T equals to 5Ω and the harvester can provide a regulated 1.2V output with the maximum input voltage as 200mV. The calculated maximum switching frequency is 2.5kHz.

Then we can calculate the instantaneous value of V_{in} when M_N is turned off. Fig. 5-1-8 depicts the equivalent circuit when M_N is on. The initial voltage for C_{in} is V_{TEG} and the initial current for L is zero as the converter works in DCM. During the on-time of M_N, Fig. 5-1-8 can be approximated to be a first-order circuit by ignoring the large capacitor C_{in}. This is due to the fact that C_{in} is set to be large enough to be regarded as an independent voltage source during the M_N on-time. Solving the simplified first-order circuit and we can have the relation between the instantaneous value of V_{in} and the constant voltage V_{TEG} as below

$$\frac{V_{in}(t)}{V_{TEG}} = e^{-\frac{R}{L}t}, \quad (5\text{-}1\text{-}10)$$

where $R=R_{TEG}+r_L+R_{on,N}\approx R_{TEG}$.

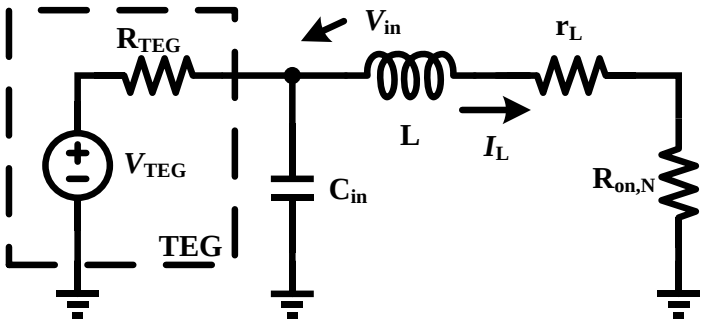


Fig. 5-1-8 Equivalent circuit of the harvester when M_N is on

Combining (5-1-8) and (5-1-10), we can have the ratio between V_{in} and V_{TEG} at the off-moment of M_N as follows

$$V_{MPP}=\frac{V_{in}(t)}{V_{TEG}}=e^{-\sqrt{\frac{2R}{Lf_s}}}=0.18. \quad (5\text{-}1\text{-}11)$$

Thus, the instantaneous voltage of V_{in} at the off-moment of M_N shall be equal to 18% of V_{TEG}, i.e., V_{MPP}, for the purpose of MPPT.

5.1.4 Working Flow of Proposed Converter

Based on the previous analysis, the main converter could be working in two different modes during steady-state phase, i.e. sleeping mode (S-mode) and transmitting mode (T-mode). In S-mode, no duty-cycle signal is generated while in T-mode duty-cycle signals are generated for power MOSFETs. The flowchart for the proposed harvester is given in Fig. 5-1-9 and the topology of the controller is shown in Fig. 5-1-10.

For proper operation, five comparisons are needed. The first two are made by the

Low-V and High-V Detectors, respectively. And they are used to determine which phase the PMU should be in, as described in Section 5.1.1. The rest three are made by dynamic comparators, which only work during a short pulse. The third comparison is between V_{out} and V_{ref} to determine which mode the main converter should be in. For the last two comparisons, i.e., $V_{in} = V_{MPP}$ (for MPPT) and $V_y = V_{out}$ (for ZCS), it's hard to make the two values exactly the same, thus we force the comparison to stop after 8 loops. After the system starts up and all the calibrations are done, the harvester will work in steady state.

The low voltage band gap reference (BGR) provides the reference voltage, and the CLK generator produces the clock signal triggering Comp1. Comp2 and Comp3 are responsible for calibrating the on-time of MOSFETs M_N and M_{P1}, respectively. The register array and timing circuit are used to store the control bits generated by the comparator in a proper sequence. The duty cycle generator accepts the stored control bits and generates the corresponding duty cycle, and the gate driver provides these signals to the power MOSFETs with enough drivability and proper dead time. Fig. 5-1-11(a) is the ideal timing diagram for the comparator clock signals and Fig. 5-1-11(b) is the circuit for V_{TEG} sampler.

Comp1 is responsible to determine which mode the main converter shall work in. The reference voltage is generated by BGR. The two voltages are compared at the rising edge of CLK (t_1 moment in Fig. 5-1-11(a)). If the output voltage is high, which means that the load is not heavy, Comp1 will send a reset signal to the duty cycle generator and the

converter will be in sleeping mode for this clock period. Otherwise, the duty-cycle signals V_N, V_{P1} and V_{P2} will be generated and the converter will be in transmitting mode.

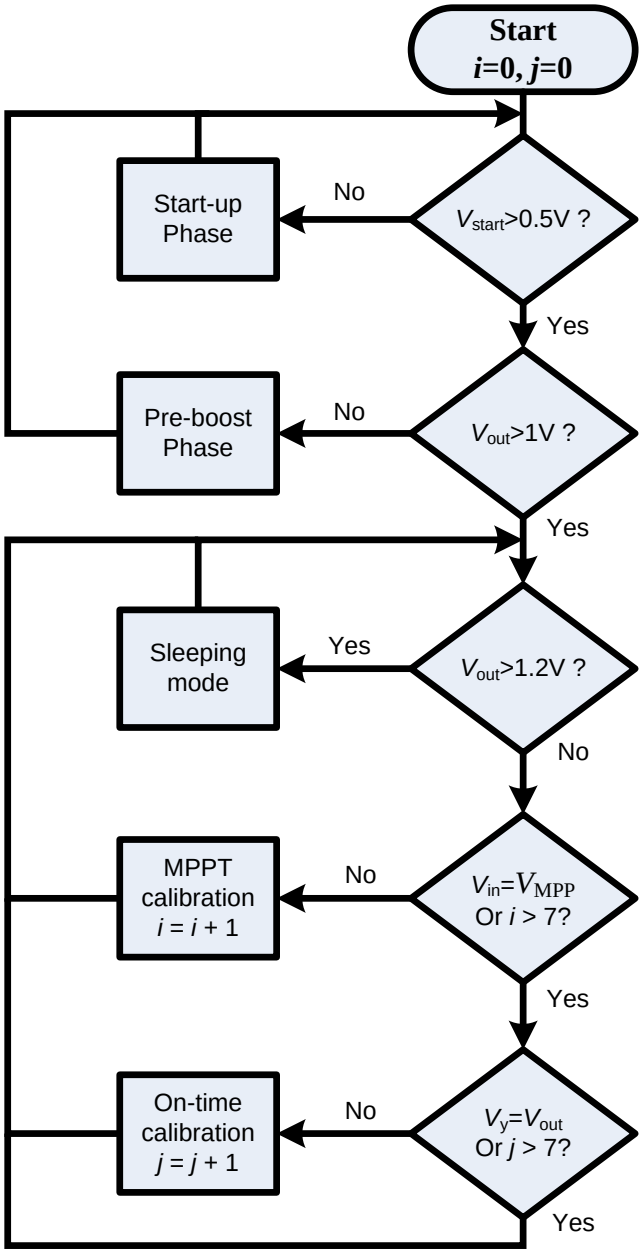


Fig. 5-1-9 Working flow of the proposed harvester

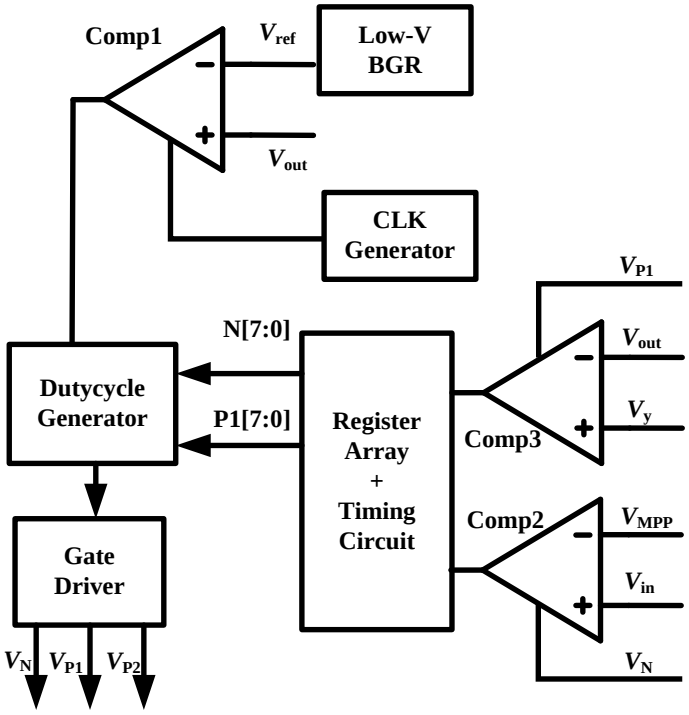


Fig. 5-1-10 Structure of the proposed controller

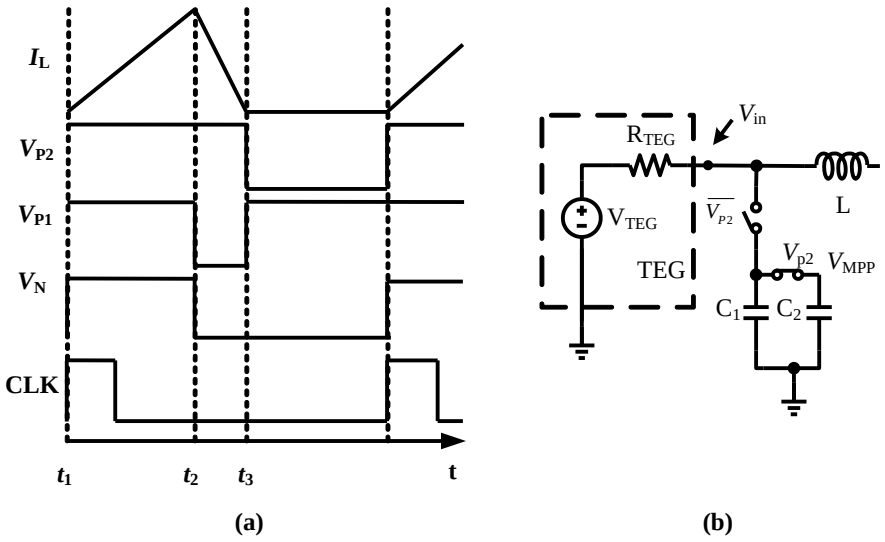


Fig. 5-1-11 (a) Ideal timing diagram for the gate signals and inductor current (b) V_{TEG} sampler

At t_2, the falling edge of V_N triggers the dynamic comparator Comp2. V_{in} and V_{MMP} are compared to determine the optimum on-time for M_N to extract as much energy as possible from the TEG. V_{MMP} is obtained by the sampler circuit in Fig. 5-1-11(b). V_{TEG} is sampled on C_1 when M_N and M_{P1} are both off and V_{MPP} is generated on the shared top plate of C_1 and C_2. The comparison result of Comp2 will be sent to the register array and to control the duty cycle generator to change the on-time of M_N in next clock period. To avoid infinite comparison, we make the register array to be 8 bits. After 8 comparison cycles, this calibration phase for M_N is forced to end. Thus, the tuning range needs to be set up carefully together with the post-layout simulation in order to achieve a desired result.

Next, the rising edge of V_{P1} triggers the dynamic comparator Comp3 at t_3. V_y and V_{out} are compared to determine if M_{P1} turns off exactly at the time when inductor current becomes zero. And the on-time of M_{p1} is adjusted according to the output of Comp3. Similarly, we also set the register array for M_{P1} control signal to be 8 bits, i.e., P1[7:0]. As the on-time of M_{P1} is dependent on that of M_N, thus, we need a timing circuit to control the sequence of N[7:0] and P1[7:0]. The M_{P1} control bits P1[7:0] can only be generated after the control bits for M_N are all properly generated.

After a while when M_{P1} turns off, M_{P2} will turn on to zero the residue current on the inductor. Otherwise, a severe oscillation at V_y may occur. And M_{P2} will turn off if a new transmitting mode comes.

Dynamic comparators Comp1, Comp2 and Comp3 are used rather than static comparators in this design. Therefore, the comparators don't consume static current in most

of the time. In this way, the power consumption of the controller is reduced, and the efficiency is improved. In addition, this structure only makes use of 2 capacitors and 2 switches to implement MPPT. Comparing to the traditional method which uses integrator or current detector, this approach is much simpler and more efficient.

5.2 Circuit Implementation

In this section, the circuit design details for the core blocks in the proposed thermoelectric energy harvester are given.

5.2.1 Start-Up Circuit

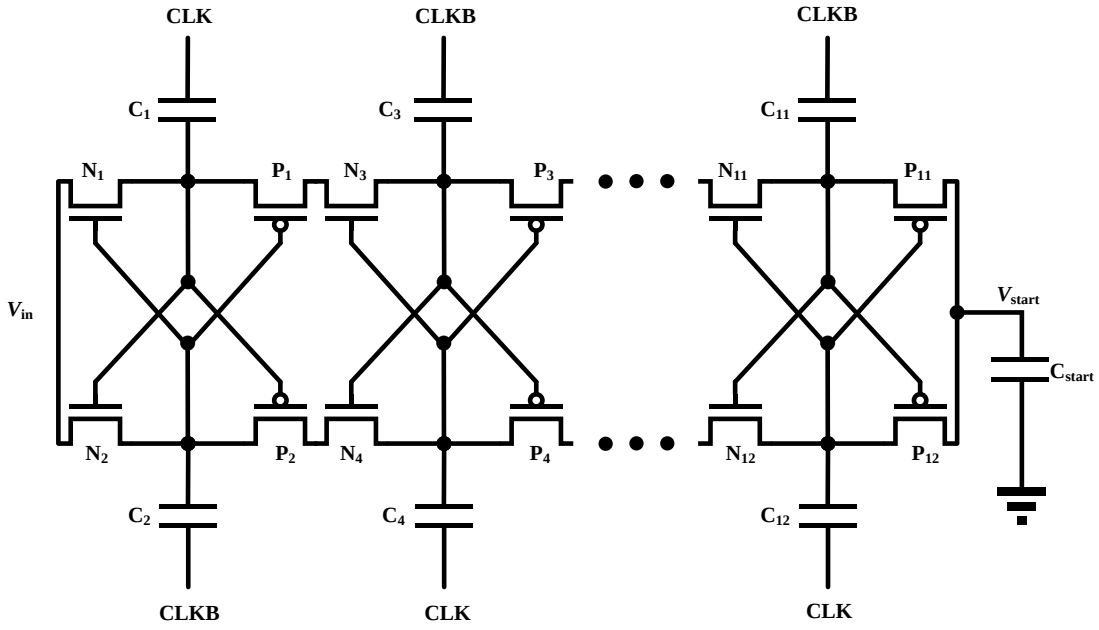
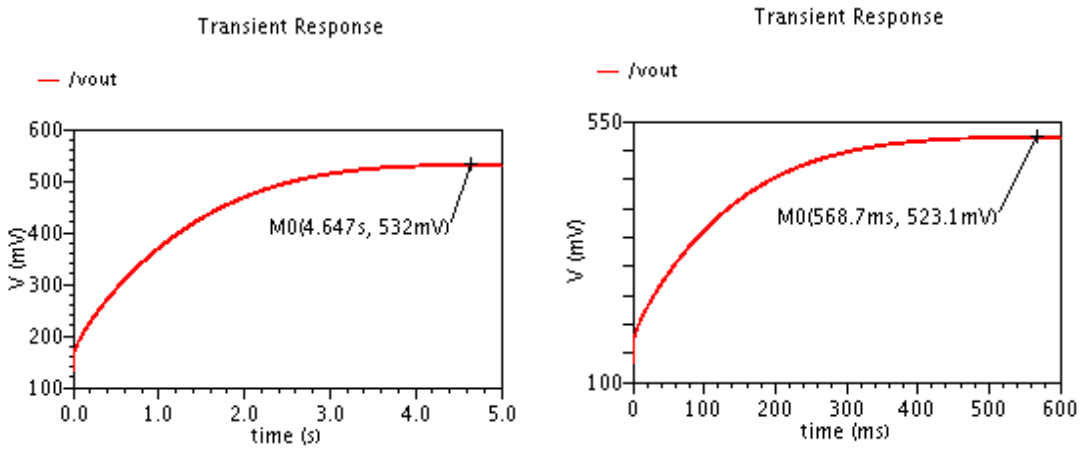


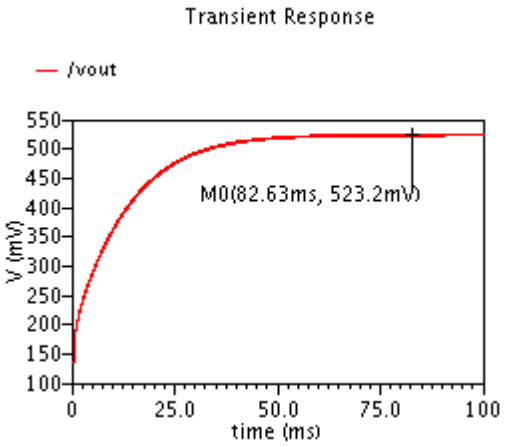
Fig. 5-2-1 Cross-coupled charge pump

As shown in Fig. 5-1-2, the start-up circuit consists of an oscillator and a charge pump. The oscillator is used to generate a non-overlapping clock signal to drive the charge pump. And the charge pump is responsible to boost the input voltage to a value higher than 500mV. Here, we apply ring oscillator and cross-coupled charge pump to form the start-up circuit.



(a)

(b)



(c)

Fig. 5-2-2 Simulation results for the startup process with 80mV input voltage in (a) slow corner (b) typical corner and (c) fast corner

Fig. 5-2-1 shows the structure of the cross-coupled charge pump. Totally it has 6 stages, so ideally, it's a 7x voltage booster. Taking the first two stages as example, when CLK is low, P_2 and N_4 will be on and the charge is transferred from C_2 to C_4. While at the same time, P_1 and N_3 are off and the reverse transfer from C_3 to C_1 is prevented. The charges are accumulated stage by stage and a boosted voltage is obtained at V_{start}. Fig. 5-2-2(a), (b) and (c) give the simulation waveforms for V_{start} with an 80mV input voltage at slow, typical and fast corners, respectively. As can be seen, the voltage can be successfully boosted to a value larger than 500mV in different corners. However, the boosting time varies a lot, which is not a big issue as long as the desired voltage can be obtained

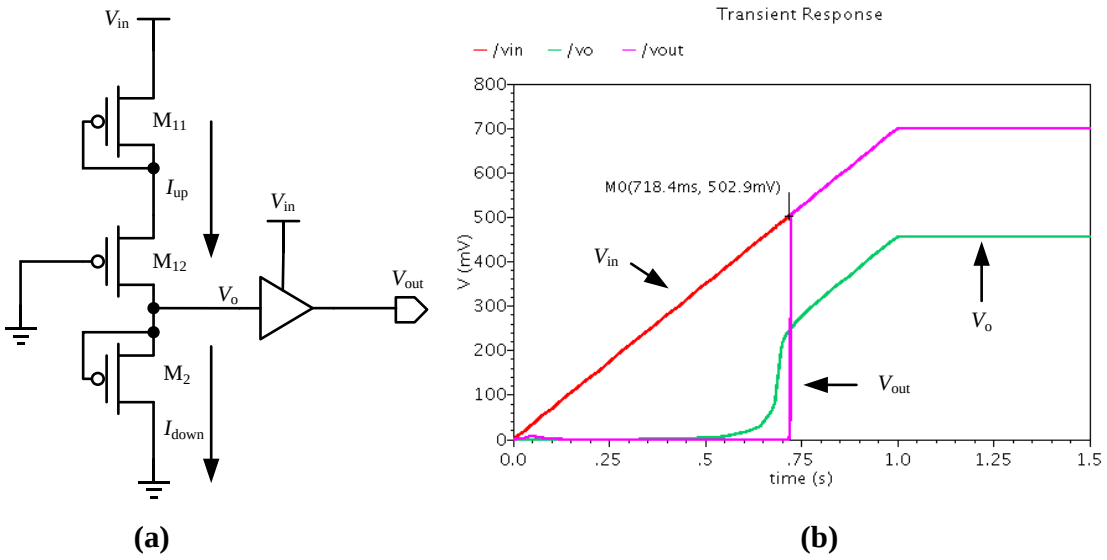
5.2.2 Voltage Detector

Voltage detector plays an important role in the proposed harvester. It determines the working phase until the converter works in steady-state. However, the BGR can only work with a stable power supply. Thus, a voltage detector without reference voltage is needed. In addition, the voltage detector should consume little power so that it doesn't deteriorate the loading condition for the charge pump.

Fig. 5-2-3(a) depicts the circuit for voltage detector, the transistor sizes are determined by the following equation [167]

$$(\frac{W_2}{L_2})/(\frac{W_1}{L_1}) = e^{q\frac{V_{in,d}}{2mkT}}, \quad (5\text{-}2\text{-}1)$$

where (W_1/L_1) and (W_2/L_2) are the width and length ratio of M_{11}/M_{12} and M_2, respectively. kt/q is the thermo voltage, m is the sub-threshold swing coefficient and $V_{in,d}$ is the threshold voltage which wants to be detected.



(a) **(b)**

Fig. 5-2-3 (a) Low-power reference-less voltage detector (b) Simulated performance for the voltage detector

Fig. 5-2-3(b) is the simulation results for the voltage detector. As can be seen, the threshold voltage is 502mV. When the input voltage is lower than this value, the output is 0, and once the input voltage exceeds this value, the output will follow the input voltage. The high-voltage detector which has a threshold voltage around 1V can be designed in the same manner.

5.2.3 Duty Cycle Generator

Fig. 5-2-4 is the schematic of the proposed low-power duty cycle generator and Fig. 5-2-5 is the simulated waveforms for the critical points in the duty cycle generator. The duty cycle signal is controlled by the charging time of the capacitor C_1 and C_2.

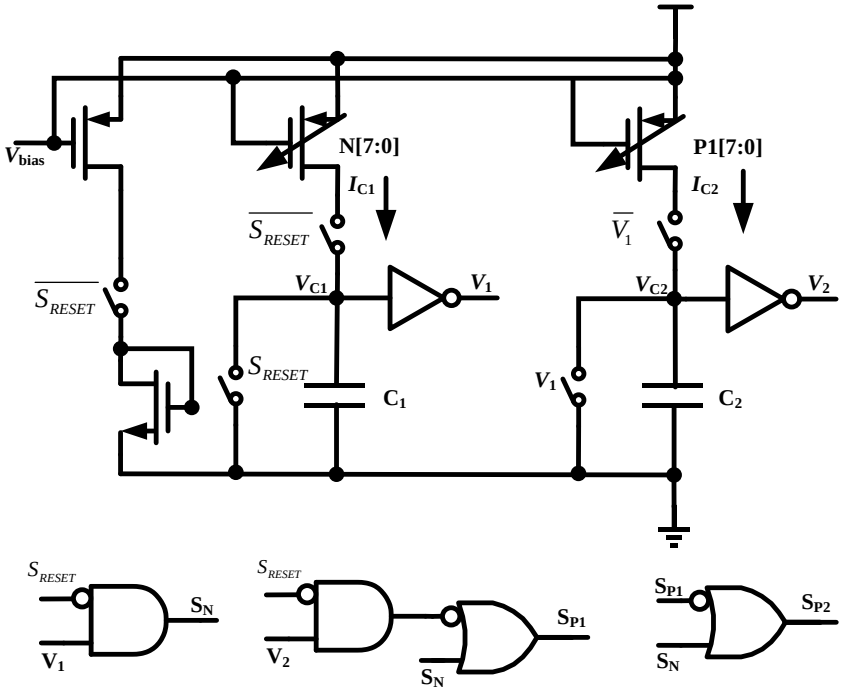


Fig. 5-2-4 Low power duty cycle generator

When the converter works in sleeping mode, Comp1 in Fig. 5-1-10 will set S_{RESET} to be 1. Thus, S_N and S_{P1} will be 0 and 1, respectively, to turn off M_N and M_{P1}. And S_{P2} will be 0 to turn on M_{P2}. Meanwhile, capacitor C_1 and C_2 are shorted to ground so that there is no charge stored in them.

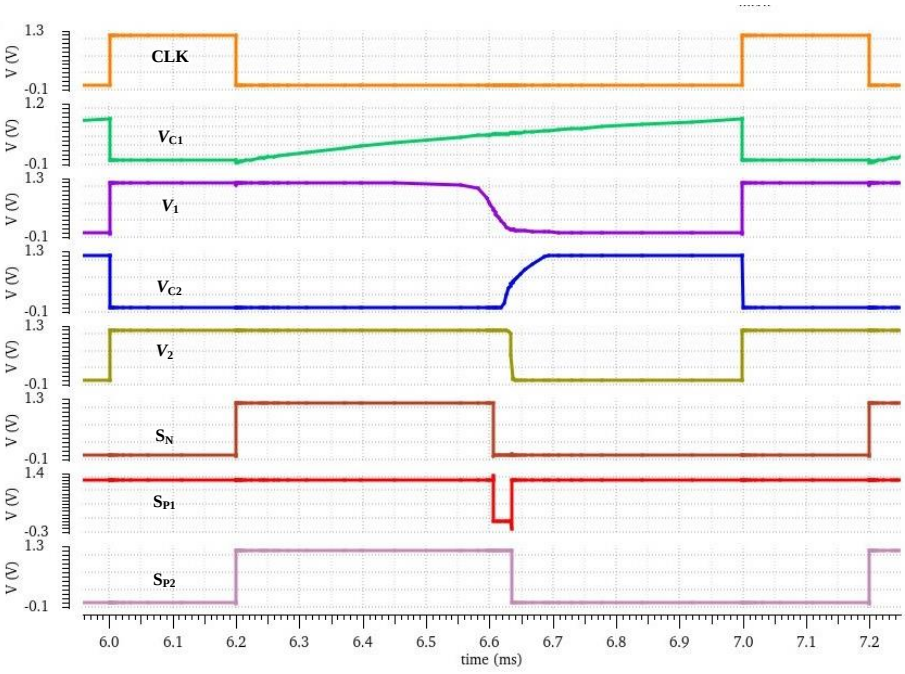


Fig. 5-2-5 Simulated performance for the duty cycle generator

In transmitting mode, S_{RESET} will be set to 0. The current I_{C1} starts to charge C_1. Once the capacitor voltage V_{C1} exceeds the flipping level of the inverter, V_1 will become 0 from 1. And then S_N will change to 0 from 1, meaning that the on-time of M_N ends. So, the on-time of M_N can be determined by following equation

$$t_1 = \frac{V_{flip} C_1}{I_{C1}}, \tag{5-2-2}$$

where V_{flip} is the flipping level of the inverter and I_{C1} is the charging current determined by N[7:0].

A similar mechanism will determine the on-time of M_{P1} and it can be expressed as follows

$$t_2 = \frac{V_{flip} C_2}{I_{C2}}. \tag{5-2-3}$$

From (5-2-2) and (5-2-3), we can see that the on-time can be controlled by changing the charging current I_{C1} and I_{C2}. The control bits are generated by Comp2 and Comp3 in Fig. 5-1-10 For either I_{C1} or I_{C2}, we apply 9 current sources in parallel. Each one is controlled by 1 bit except there is one current source which is always on. As the tuning range of the current is limited by the number of bits, we need to carefully set up the size of the current sources to make sure that the desired on-time can be covered by the tuning range. Also, all current sources are biased in sub-threshold region to reduce power consumption. Fig. 5-2-5 shows the simulated waveforms for the critical signals in Fig. 5-2-4.

5.2.4 Register Array and Timing Circuit

The register array is used to accept and store the results from the dynamic comparators and further control the current sources by changing the bits N[7:0] and P1[7:0] in Fig. 5-1-10. The calibration mechanism is similar to that described in Chapter 4.1.3, so we don't repeat it here. Since two calibration circuits are needed and the second calibration can only be done once the first calibration is finished as discussed in Section 5.1, a timing circuit to control the calibration sequence is necessary.

Fig. 5-2-6(a) gives the implementation of the timing circuit. As the control bits for M_N and M_{P1} are both 8 bits, the working periods are counted by 16 and 32 times first. The combinational logics are used to generate the lock signal TN_LCK and TP1_LCK for N[7:0] and P1[7:0], respectively. For the register array, when the lock signal is high, it will keep current states and ignore the new coming comparison results. The TN_LCK and

TP1_LCK are both designed to be low for 8 periods so that the 8 control bits can be stored in the register array. Note that the low level of TN_LCK and TP1_LCK are non-overlapping to guarantee the correct timing sequence. After the register arrays are locked, only the RESET signal can start a new calibration process.

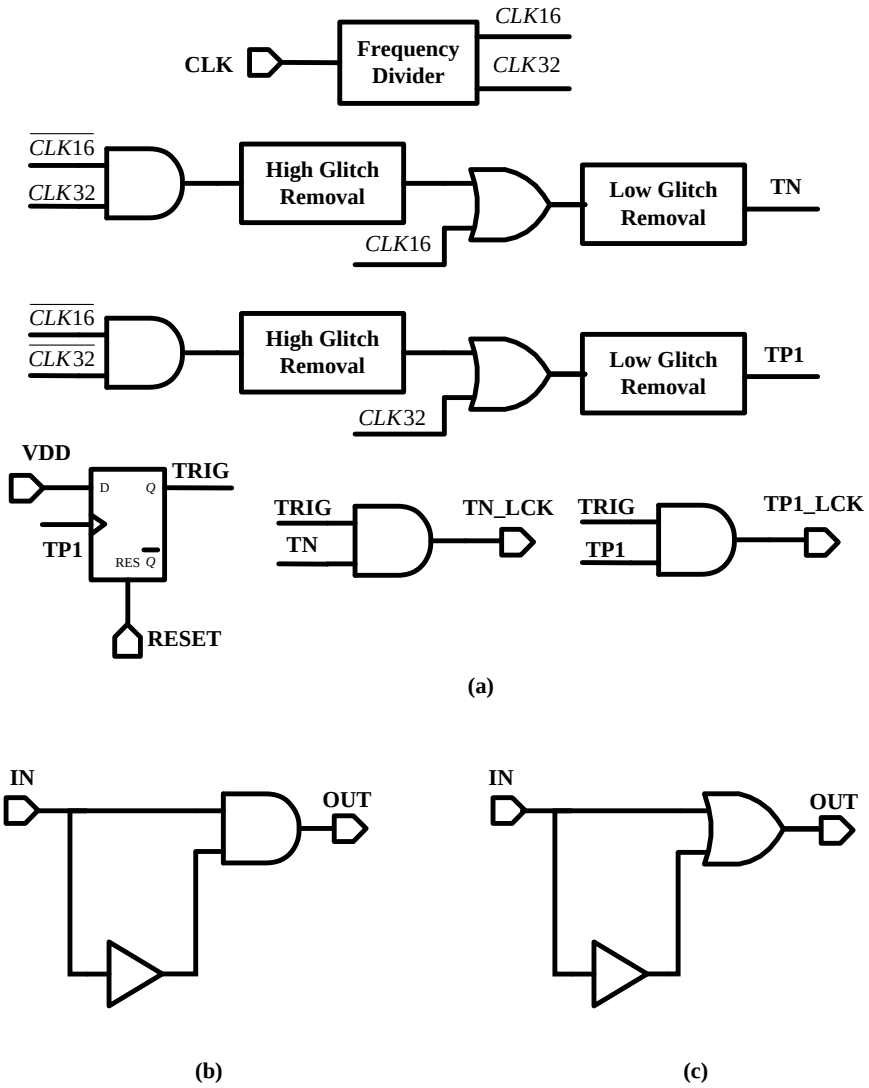


Fig. 5-2-6 (a) Timing circuits (b) High glitch removal circuit (c) Low glitch removal circuit

Due to the existing of race and competition in the combinational logic, there will be both high-level and low-level glitch at the output which will may cause the signal to be wrong. We apply glitch removal circuit to overcome this issue. Fig. 5-2-6(b) and Fig.5-2-6(c) depict the high glitch removal circuit and low glitch removal circuit, respectively.

5.3 Experimental Results

The system is designed in a standard 180 nm CMOS process. Fig. 5-3-1 shows the die photo and the core of the chip takes 1090 μm x 860 μm area.

To measure the chip performance, a power supply, a function generator and an oscilloscope are used. The power supply together with a 5 Ω resistance mimics the TEG. For this design, the clock signal is fed from external so that we can easily change the operation frequency during the steady-state, however, it can be embedded into the chip as well. Note that before reaching the steady-state, the external clock is not in use.

Fig. 5-3-2 gives the startup waveform of V_{out}, and the startup process takes about 420ms and the output voltage is stabilized at 1.2V after startup.

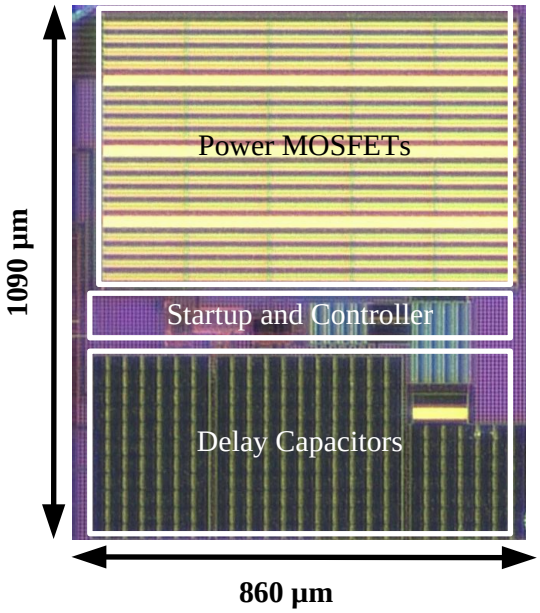


Fig. 5-3-1 Chip micrograph for the proposed harvester

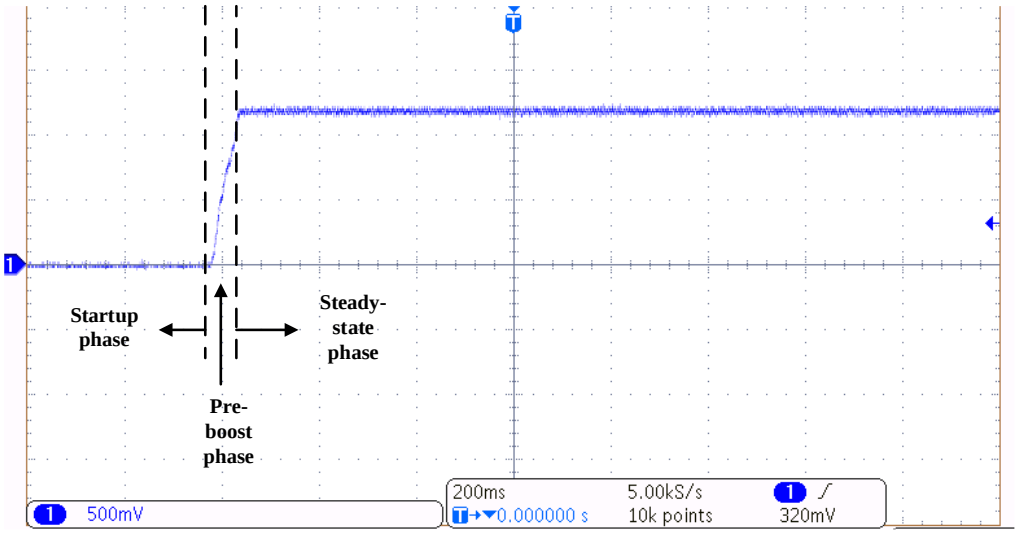
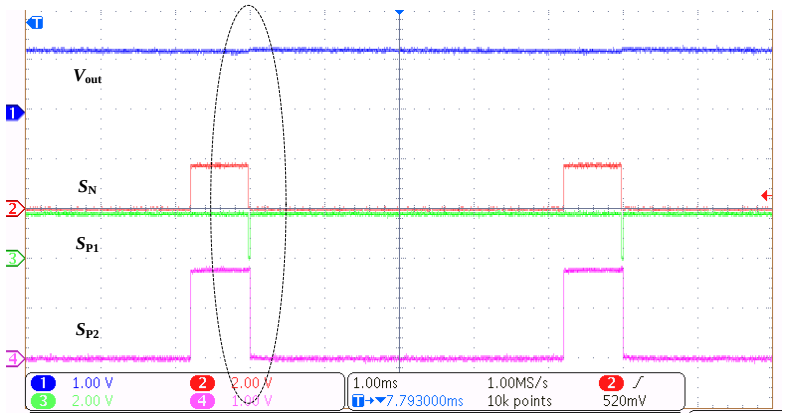
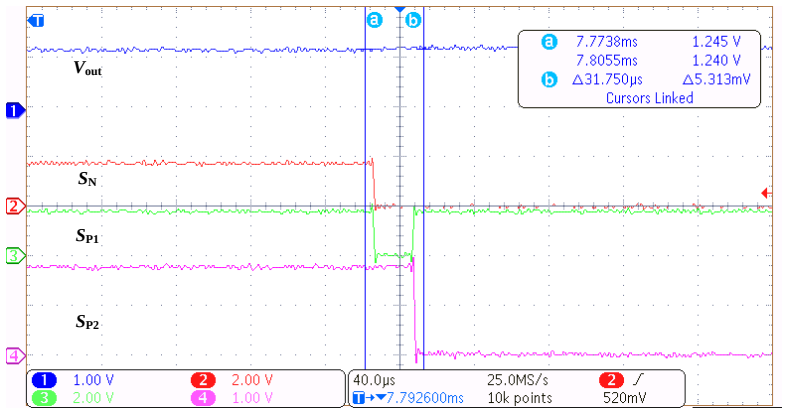


Fig. 5-3-2 Startup waveform of V_{out}



(a)



(b)

Fig. 5-3-3 (a) Steady-state waveform of V_{out} and gate signals (b) Zoom in graph centered with S_{P1}

Fig. 5-3-3(a) shows the waveforms for steady-state output voltage V_{out}, gate control signals S_N, S_{P1} and S_{P2}, respectively. As can be seen, with the clock frequency equal to 1kHz, the converter works for a clock period and then sleeps for 3 clock periods. Fig. 5-3-3(b) is the zoom-in of (a) centered with S_{P1}. And it shows that there is proper dead time between S_N/S_{P1} and S_{P1}/S_{P2}, also we can see that the ripple is only 5mV.

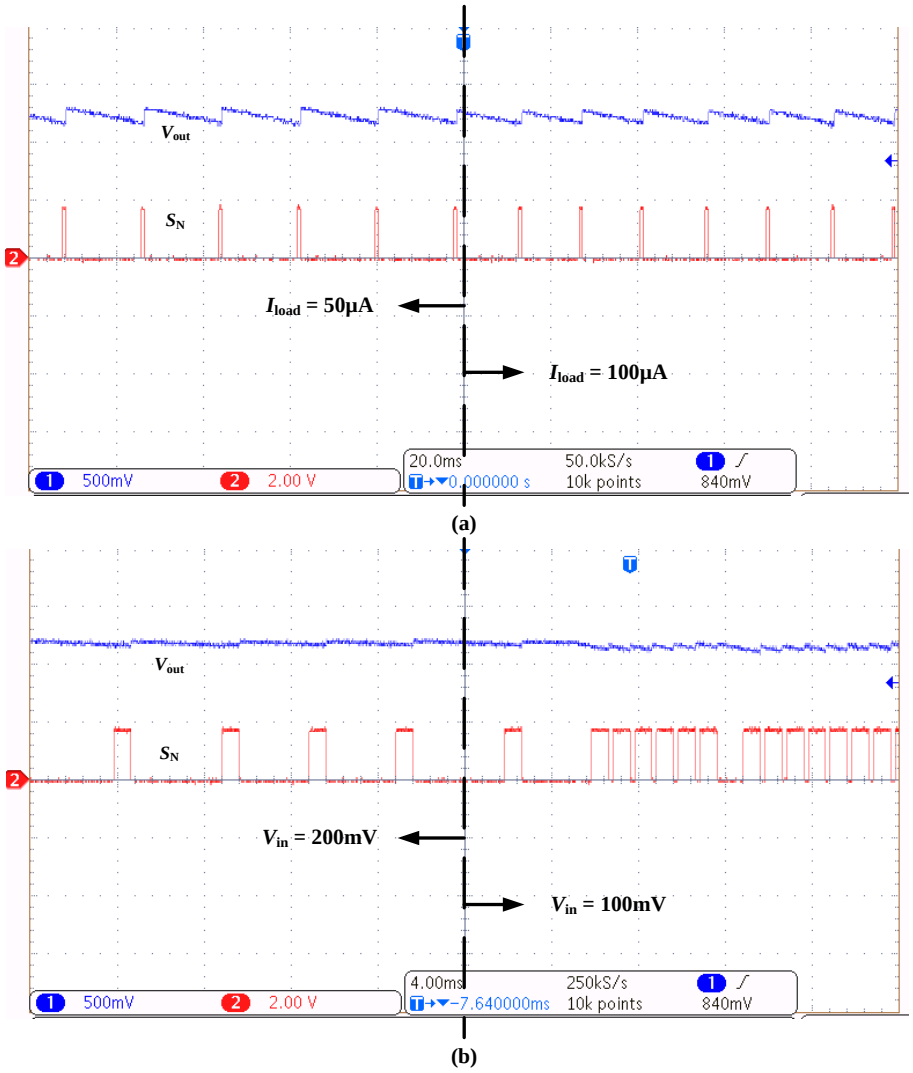


Fig. 5-3-4 (a) Transient waveform of V_{out} and S_N when load changes (b) Transient waveform of V_{out} and S_N when input changes

Fig. 5-3-4(a) and (b) show the waveforms when the load and input condition of the converter are changed, respectively. When the load changes from 50µA to 100µA, there are more working periods within a given time frame, and the same phenomenon is observed when the input voltage changes from 200mV to 100mV. These observations are in

consistency with the theory because when the output power is increased or the input power is reduced, the converter needs to work more frequently in the transmitting mode to ensure that the required power can be obtained in the output. Also, it's observed that there is no overshooting or undershooting when the load and input are changed thanks to the OTC-PSM.

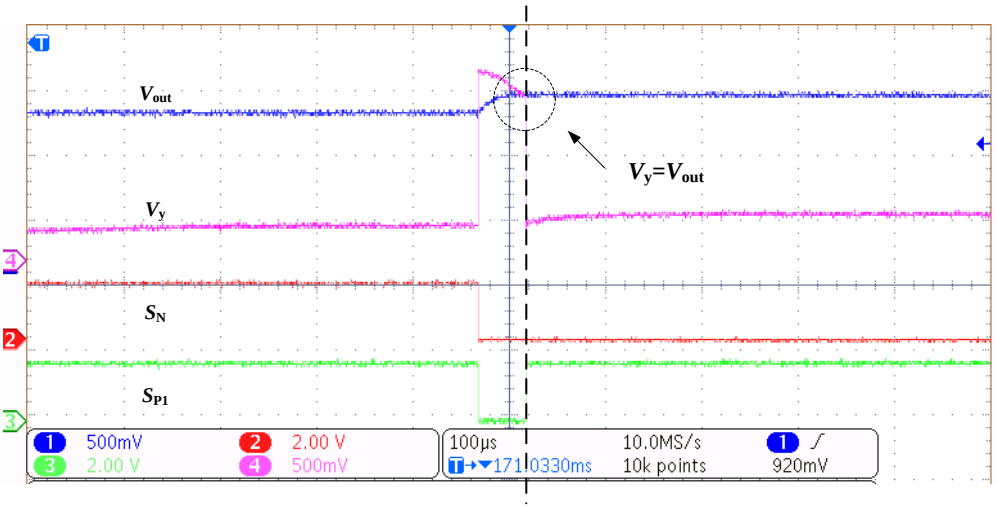


Fig. 5-3-5 ZCS waveform of V_{out} and V_y

Fig. 5-3-5 shows the waveform of V_y and V_{out} when the calibration is finished. As can be seen, at the turn-off moment of S_{P1}, the instantaneous value of V_y and V_{out} are almost the same, which is desired for the ZCS operation.

Fig. 5-3-6 shows the measured curve of efficiency and output power versus input voltage V_{TEG}. When V_{TEG} is within the range of 80mV to 200mV, the system has a high efficiency and the highest efficiency occurs at 120mV V_{TEG} and 600µW output power.

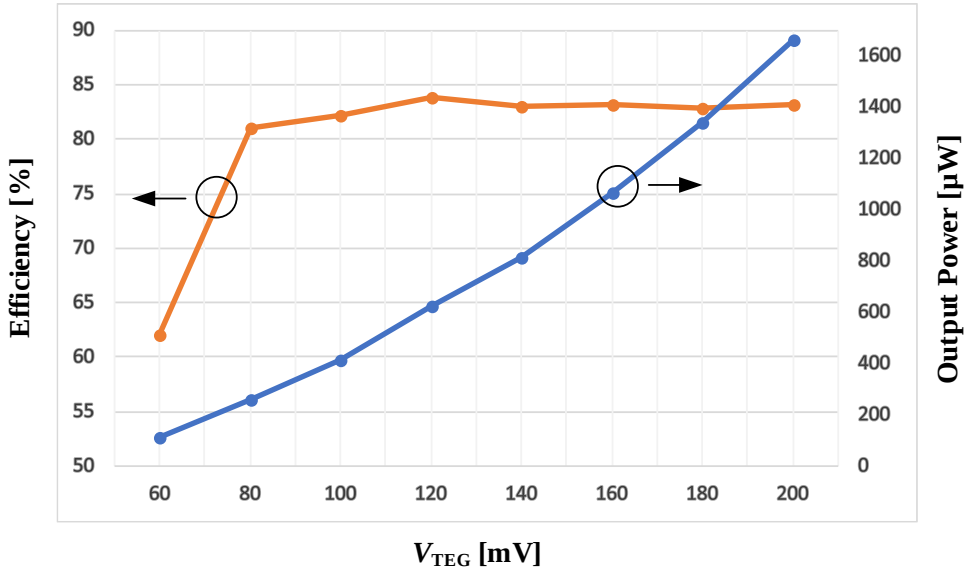


Fig. 5-3-6 Efficiency and output power curve versus input voltage

Table 5-3-1 Performance comparison

	[165]	[169]	[173]	This work [86]
Process	180nm	180nm	65nm	180nm
Startup Integrated?	Yes	No	No	Yes
Startup voltage (mV)	190	260	40	100
Output voltage (V)	1-1.6	1.05-1.4	1.1	1.2
$P_{control}$ (µW)	10.8	2.4	77	3.6*
Maximum efficiency	60%	90.8%	75%	83.9%
MPPT	Yes	Yes	No	Yes

*Simulated

Table 1 gives the comparison among this work and other state-of-the-art papers. The proposed boost converter achieves high efficiency of 83.9% at 120mV input voltage

and relatively light load of 600 μW with integrated energy-efficient MPPT and startup circuits. It has several advantages. First, it applies oscillator and charge pump as the start-up circuit, which can be easily integrated on the chip. Second, the OTC-PSM scheme saves considerable power to achieve a high efficiency as well as low output ripple. Third, the proposed MPPT structure is simple and easy to implement, thus it lowers hardware cost and boosts energy efficiency.

5.4 Conclusions

A boost converter for thermoelectrical energy generator is presented with 83.9% peak efficiency and simplified MPPT implementation. The proposed OTC-PSM control mechanism reduces the power dissipation by turning off the converter periodically with the help of dynamic comparators. A simple MPPT algorithm specifically designed for the TEG energy sources with fixed internal resistance is also proposed, costing nearly no power.

Chapter 6
Conclusions and Future Works

6.1 Fulfilled Objectives and Contributions

The research objectives of this research have been set in Section 1.2 and now let's check them one by one. In general, this research focuses on ultra-low power wireless sensor circuits design for IoT applications. According to the circuit functions, there are two main parts in the dissertation. One part is the data communication circuits, which includes receiver and frequency synthesizer. And they are illustrated in Chapter 3 and Chapter 4. Another part is the autonomous power management unit design for the energy harvester, whose design detail is given in Chapter 5. And the literature reviews for these blocks are given in Chapter 2, which concludes the conventional means of implementation and state-of-the-art publications.

For short range communication in IoT applications, FSK is preferred in both the prospective of modulation and transmission channel. However, the demodulation of FSK signal may be challenging because the design of high-*Q* on-chip filter is usually not easy. In this research, motivated by the features such as good frequency selectivity, center frequency tunability and easy on-chip integration, we proposed a new topology of the FSK receiver using 4-path filter in Chapter 3.

The proposed 4-path filter based FSK receiver has two main features. First, the 4-path filter serves as the first stage of the receiver and it converts the frequency difference of the input signal to amplitude difference. This facilitates the further demodulation to

easily implemented ASK demodulation and the removal of the LNA reduces the overall power consumption of the receiver. Second, a baseband amplifier is used to detect the envelop and amplify the signal simultaneously, which is possible by making the data bits random. In order to set up the desired bandwidth of the amplifier, a tunable pseudo resistor is applied. Moreover, mathematical analysis of the 4-path filter transient behavior has been done and the maximum achievable data rate was derived to guide the circuit design.

The design was implemented with 0.13μm CMOS process and the chip occupies an area as 300 x 700 μm^2. The receiver has been tested with 2 set of carrier frequencies for different MedRadio sub-bands. The first set of carrier frequencies are 401MHz and 406MHz while the second set is 438MHz and 444MHz. The frequency tunability is achieved thanks to the center frequency tunability of the 4-path filter. Meanwhile, the data rate of the proposed receiver is 2.5Mbps with 184μW power consumption at -65dBm input condition, which returns the value of energy per bit as 74pJ/bit. Such performance is very competitive among the state-of-the-art publications and the objectives of low power and high data rate set in Section 1.2 for receiver have been met.

Frequency synthesizer is another important block in wireless data communication system. The main requirement in IoT applications is low power. In this research, having observed the fact that the baseband filtering capacitor in the 4-path filter can reflect the envelop changing of the output waveform, we proposed a two-step calibration frequency synthesizer in Chapter 4.

The first calibration is coarse tracking, and it is accomplished by the 4-path mixer, which can be easily implemented from the 4-path filter. By comparing the output voltages of the four branches with the pre-set reference voltage. We can determine whether the input frequency is close enough to the reference frequency. Once they are close enough, the frequency synthesizer moves to the second step. The fine tracking in the second step of calibration is done with the conventional injection-locking technique. And eventually the frequency of the output signal is equal to a fixed ratio of the reference frequency.

We analyzed the locking range of the ring oscillator and the frequency response of the 4-path mixer. Such analysis can guide the circuit design to guarantee that the ring oscillator can be successfully injection locked. The core circuit blocks for the proposed frequency synthesizer include 4-path mixer, 5-bit calibration circuit, digital-controlled-oscillator and multi-input comparator. Their implementation details are given in Chapter 4 and the overall frequency synthesizer has been implemented with 0.18µm CMOS technology.

The core circuit occupies 220µm x 190µm. The simulation results show that it can successfully lock the output frequency at 440MHz of a free-running 3 stage ring oscillator with a power consumption as 305µW. The phase noise at 1MHz offset is -124.86dBc/Hz and it is -97.45dBc/Hz at 100kHz offset. And the integrated RMS jitter from 10KHz to 40MHz is 2.5ps.

To avoid changing or charging the batteries regularly, autonomous powering for the wireless sensor is highly desired in IoT applications. And thermoelectric energy

harvesting attracts much attention because it's the most widely available energy source in IoT applications, especially in the wearable/portable applications scenarios and such energy harvesting almost doesn't impose any limitations to human's daily activity. In this research, we proposed a power management unit for thermoelectric energy harvesting, which aims to adapt the low power and low input voltage situation.

The proposed PMU can be started up with an input voltage as low as 100mV thanks to the cross-coupled charge pump and oscillator. After successfully start up, the mode switching circuit will disable the startup circuit and activate the main boost converter. The OTC-PSM is proposed to limit the power consumed both in the power MOSFETs and the control block for a high conversion efficiency. Meanwhile, OTC-PSM strategy also has advantage in terms of response speed and output ripple. In addition, a hardware and power efficient MPPT method is proposed specifically for TEG and other energy sources with fixed internal resistance.

Dynamic comparators which only consume power in a short time interval together with well-designed timing circuits are used to save the power consumption in control blocks. In addition, an ultra-low power duty cycle generator is proposed, which only consumes hundreds of nano-watts. To reduce the power consumption in the MOSFETs, ZCS technique is applied, which can let the switches turn on and off at the best moment.

The proposed PMU has been implemented with 180nm CMOS process and the chip occupies 1090 μm x 860 μm area. Power MOSFETs and delay capacitors take most of the area. The chip can provide 1.2V stable output voltage with minimum input as 100mV. It

can achieve a maximum efficiency as 83.9% at 200mV input. The maximum output power of the chip is 600 μW. Moreover, it has no overshoot or undershoot in the case of line change or load change thanks to the OTC-PSM strategy. Meanwhile, the output ripple is only 5mV.

6.2 Considerations for Future Work

This research may be continued in the following aspects pertaining to the data communication and self-powering circuits design for IoT applications.

For the receiver, the current design and measurement have been performed under ideal transmission channel. In other words, the negative effects coming from external interferences are not taken into consideration. However, such phenomenon may be very common in reality because the electronic devices may be exposed in an environment with many active frequency channels. Even though the 4-path filter has a high-*Q* property and can remove most of the out-of-band interferences, the undesired folding back effect may transfer the odd harmonics of the center frequency to the band of interest. Thus, to make the receiver more robust, the future optimization will focus on the improvement of the interference rejection, especially the rejection of the odd harmonics.

For the self-powering circuit, we consider taking use of other means of energy source in addition to TEG, like vibration or photovoltaic. We want to store the additional energy and only use it when the power provided by TEG is not enough. Thus, a more complicated PMU with multi energy sources (vibration power/photovoltaic power and

thermoelectric power) and two loads (regular load and storage load) is needed for future work.

The last consideration is to integrate all these blocks into one chip as currently they have been tested/simulated separately as the receiver, frequency synthesizer and PMU. Some other issues may occur when all the things are assembled together, and more effort may be required to make the overall self-powered wireless data communication chip function properly.

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