A MULTI-MODE STACKED-SWITCH INVERTER/RECTIFIER LEG FOR BIDIRECTIONAL POWER CONVERTERS

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Abstract

The development of renewable energy systems (e.g. wind and solar) is significant to cope with an energy crisis yet, at the same time, it presents challenges to the grid for their MW-scale integration due to their volatile characteristics. Battery energy storage systems are essential in providing sustainable power and improving the overall system reliability effectively with the large deployments of renewable energy conversion systems. Bidirectional power converters are responsible for transferring power between the battery energy storage system and the grid. Selecting an efficient and cost-effective power topology along with a reliable control system is critical to ensure that the energy storage system operates safely with prolonged service life and minimized maintenance cost.

In this dissertation, a multi-mode stacked-switch leg with soft-switching capability for use in bidirectional DC/DC converters is proposed for battery energy storage applications. This dissertation consists of three parts. The first part focuses on the development of a bidirectional soft-switched converter utilizing a *CLLC* resonant circuit and the proposed multi-mode switching legs. The presented leg is able to facilitate multiple operating modes to enable high voltage gain under different operating conditions and allow the converter to operate with a much lower output voltage ripple (50%) compared with the conventional stacked-switches-based converter topology. In the second part of this thesis, a fault-tolerant control scheme is proposed which enables seamless post fault operation of the presented multi-mode DC/DC converter if any switches in the presented leg experience an open-circuit fault. In the third part of this thesis, a comprehensive hybrid control system is proposed so that the overall voltage gain range of the converter is widely extended with a narrow switching frequency range (less than 10% of the base frequency), while at the same time, the efficiency of the converter is improved over the whole gain range (more than 1%). The operating principles and characteristics of the proposed converter and the proposed control schemes are explained in detail in this thesis. The performance of each of the presented circuit and control concepts is verified through simulation as well as experimental results on silicon-carbide (SiC)-based proof-of-concept hardware prototypes.

to my parents,

and my sisters

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List of Abbreviations

AC	Alternating Current
APWM	Asymmetrical Pulse-Width Modulation
ADC	Analog To Digital
BD	Bidirectional
BESS	Battery Energy Storage System
BMS	Battery Management Systems
CAES	Compressed Air Energy Storage
CC	Constant Current
CTE	Coefficients Of Thermal Expansion
CV	Constant Voltage
DAB	Dual Active Bridge
DC	Direct Current
DSP	Digital-Signal Processor
EMI	Low Electromagnetic Interference
ESS	Energy Storage System
EV	Electric Vehicle
FB	Full-Bridge

FT	Fault-Tolerant
FW	Full-Wave
GaN	Gallium Nitride
HB	Half-Bridge
HEMT	High-Electron-Mobility Transistor
HEV	Hybrid Electric Vehicle
HF	High Frequency
HFET	Hetero-Structure Field-Effect Transistor
HVDC	High-Voltage Direct Current
HW	Half-Wave
IGBT	Insulated-Gate Bipolar Transistor
JBS	Junction Barrier Schottky
JFET	Junction-Gate Field-Effect Transistor
LF	Low Frequency
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NiCd	Nickel–Cadmium
NiMh	Nickel–Metal Hydride
NPC	Neutral Point Clamp
OCF	Open-Circuit Fault
PbA	Lead-Acid
PF	Power Factor

PFC	Power Factor Correction
PHM	Prognostics And Health Management
PI	Proportional Integral
PSM	Phase-Shift Modulation
PV	Photovoltaic
PWM	Pulse-Width Modulation
RE	Renewable Energy
RES	Renewable Energy Source
RF	Radio Frequency
RMS	Root Mean Square
SCF	Short Circuit Fault
Si	Silicon
SiC	Silicon Carbide
SMES	Superconducting Magnetic Energy Storage
SOC	State Of Charge
SOH	State Of Health
SR	Synchronous Rectification
TL	Three-Level
UPS	Uninterruptible Power Supplies
VCO	Voltage Controlled Oscillator
VD	Voltage-Doubler

VFM	Variable-Frequency Modulation
WBG	Wide Band-Gap
WT	Wind Turbine
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Chapter 1. Introduction

Climate change due to the production of carbon dioxide from burning fossil fuels is one of the most threatening problems facing modern society. As a result, renewable energy sources (RESs) (e.g. wind and solar) are becoming attractive replacements [1]–[3]. Furthermore, traditional power plants with fossil fuel suffer a very low efficiency from sources to end-users, approaching an overall efficiency of about 30% (thermodynamic cycles have limited efficiency and there are several other losses, including the transmission and distribution losses), while the

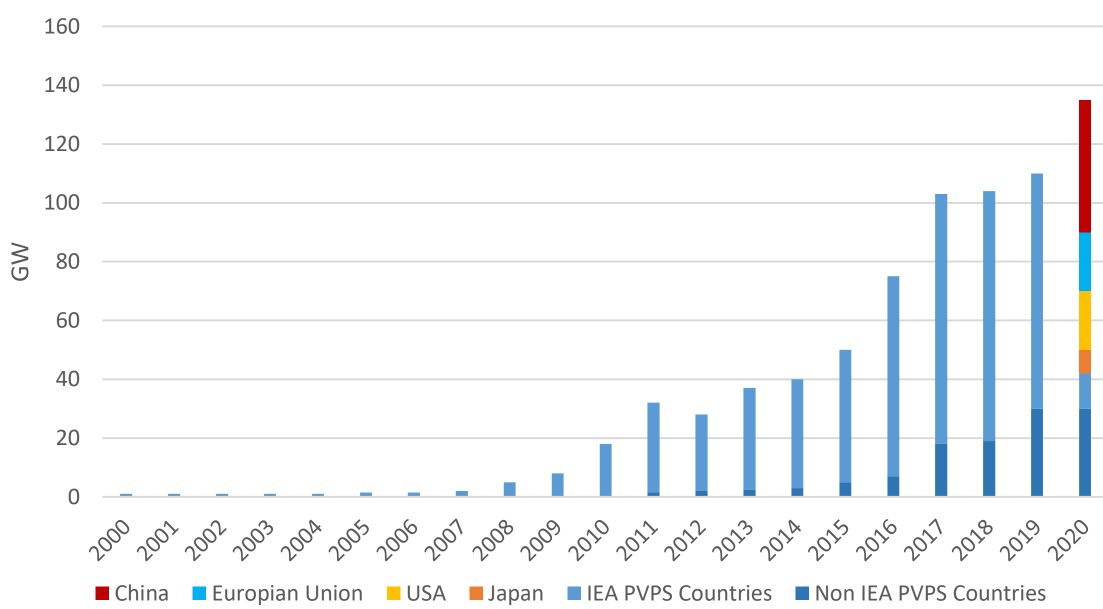


Figure 1.1- Evolution of annual PV installation [5]

efficiency of the local generation from RESs reaches an overall value of about 70% [4]. As a result, RESs have been installed at a fast pace globally in recent years. Currently, wind energy and solar energy are the most promising sources of future large scale carbon-free energy. Ideally, 100% of our energy should come from carbon-free sources such as wind and solar. Reported market data shows that the global PV market again grew significantly in 2020. At least 135 GW of PV systems have been installed and commissioned in the world last year. Figure 1.1 shows the evolution of annual PV installation between 2000 and 2020. The total cumulative installed capacity for PV at the end of 2020 reached at least 760.4 GW [5].

In the wind industry, the 93 GW of new installations in 2020 brings global cumulative wind power capacity up to 743 GW (Figure 1.2). In the onshore market, 86.9 GW was installed, an increase of 59% compared to 2019 [6]. Viewed over a slightly longer period, wind and solar capacity more than doubled between 2015 and 2020, increasing by around 800 GW, which equates to an average annual increase of 18%.

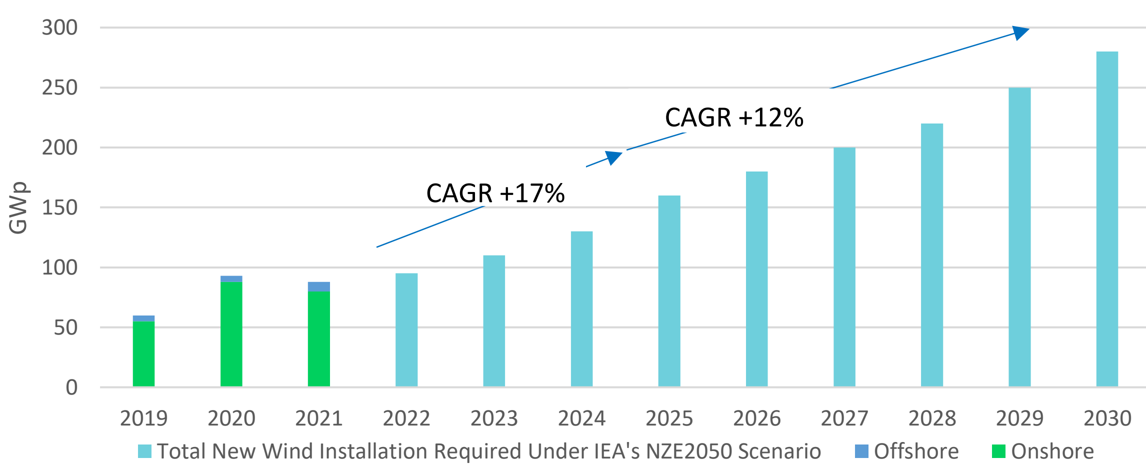


Figure 1.2- Annual wind installations (GW) [6]

Although among the current available renewable energy technologies, wind and solar energy sources are the most promising options, as they are omnipresent, freely available, and environment friendly and are improving in various aspects, their intermittent nature remains the main obstacle to their utilization and becomes a serious concern for the stability of the grid, particularly with increased RES penetration and at times when a high percentage of instantaneous demand is supplied by RES [7], [8]. Consequently, only 11.7% of the total global electricity is generated by RES, of which wind energy contributes to almost 50% and solar energy represents around 27% [9]. In the case that a huge portion of the instantaneous demand (50%+) is supplied by RES, significant operating reserves are required to meet the demand in the case of a sudden decrease in the output of RES, leading an increase in the operational cost of the electricity network. Utility-scale energy storage system (ESS) with fast response characteristics is a promising option to provide alternatives to provide operating reserves for RES and is one of a suite of options to provide energy system flexibility, and it can generally be deployed quickly and modularly when and where flexibility is needed [10]. Furthermore, there is virtually no cost to the system when energy storage systems are not providing power.

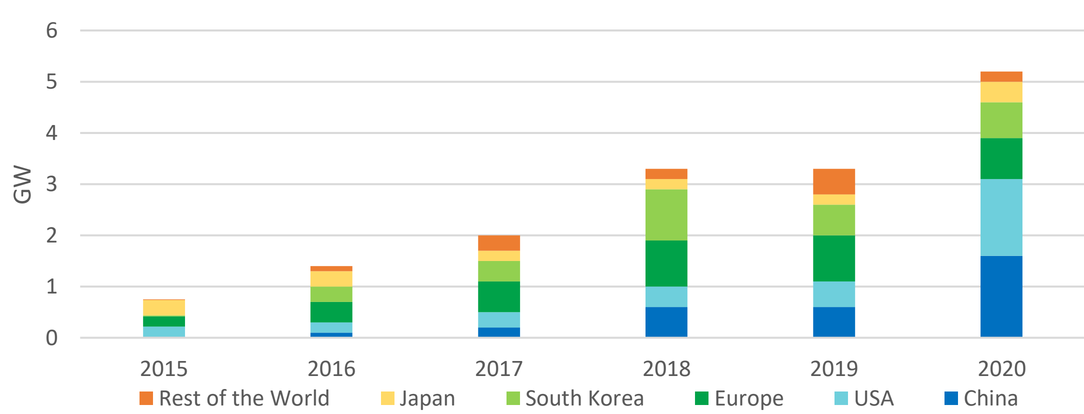


Figure 1.3- Energy storage deployment by country [10]

In terms of grid support, fast response ESS can provide stability to the power system. In addition, ESS can help to black-start networks while providing voltage support for the transmission and/or distribution lines [11]. Numerous utility-scale ESS (i.e. > 10 MW) have been commissioned or announced in the world. As shown in Figure 1.3, the capacity of ESS has increased rapidly over the recent years as their deployment reached a record level in 2020, more than doubling from 2017. The leading country was Korea, followed by China, the United States, and Germany.

In addition, with the increasing concerns on environmental issues, electric vehicle (EV) is also popularly regarded as one of the most effective strategies to reduce oil dependence and gas emission, and increase the efficiency of energy conversion [11], [12]. Electric car registrations increased by 41% in 2020 and at the end of the same year, there were 10 million electric cars on the world's roads, following a decade of rapid growth illustrating the trend towards the utilization of EVs as a promising solution for transportation as well as global warming [13].

1.1. Battery Energy Storage Systems (BESSs)

Energy storage technologies are critical in order to improve the quality of the power that is injected into the grid and provide voltage support, peak shaving, black start, etc. Many energy storage technologies have been reviewed and investigated in the literature [14]–[17] including supercapacitor energy storage (supercapacitors, ultra-capacitor, etc.), superconducting magnetic energy storage, flywheels, and batteries (Lead-Acid, Nickel Cadmium, Sodium Sulphur, Li-Ion, etc.) The ideal storage technology would provide fast access to power, offer high energy capacity with low cost and long life expectancy. However, no energy storage technology can meet all the features at the same time. Each one of the above-mentioned technologies has different characteristics.

Some energy storage technologies which are called access-oriented energy storage systems have a fast response time and can provide high power to the load or inject several MW of power into the grid for a short period of time. Flywheels, supercapacitors, and superconducting magnetic energy storage (SMES) are among access-oriented energy storage technologies and are used for responding to short-time disturbances, such as fast load transients and for power quality issues. They have a very high life cycle and efficiency of around 95%, yet their cost per unit of stored energy is also very high. Other energy storage technologies which are called capacity-oriented energy storage systems do not have fast response time and can provide lower powers for longer periods of time and are used for addressing slow load variations. Capacity-oriented storage systems include pumped hydroelectric systems, compressed air energy storage (CAES), and hydrogen storage.

Depending on the design, batteries can also be classified as access oriented or capacity oriented however, their life cycle is shorter than other fast-access storage technologies [14], [18]. Significant research is focused on the grid integration of access-oriented storage technologies including supercapacitors, SMES, flywheels, and batteries to provide high power for a short period of time. Therefore in this thesis, only fast-access technologies are reviewed and investigated.

Battery energy storage systems are known as "BESSs" and are composed of one or more electrochemical cells. BESSs store energy in the form of chemical energy [19]. During off-peak/low-cost the battery is charged and the electrical energy is converted to chemical energy and when discharged this energy is converted into electrical energy again [20].

BESSs offer the flexibility in capacity and rapid response required to meet application demands over a much wider range of functions than many other types of storage. Depending on the cycled time and the type of electrochemistry, batteries are available in various capacities from less than 100W to several MW with efficiency to be in the 60% to 90% range.

While BESS currently account for only a small portion of energy storage technologies integrated within the grid and despite the fact that the BESSs represent the first electrical energy storage system introduced, compared to the other technologies, they are still the most cost-efficient technology on the market [21]. BESSs have seen great growth recently due to their

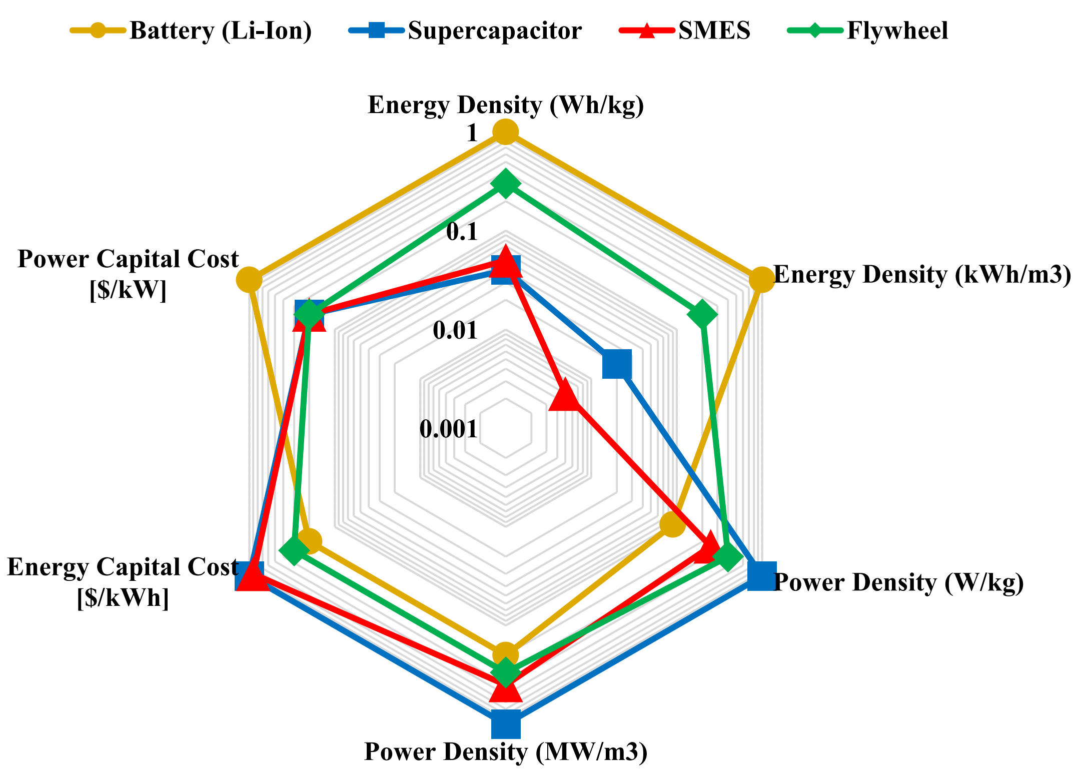


Figure 1.4- Comparison of power, energy, and cost of energy storage technologies

versatility, high energy density, and efficiency. More grid applications have become suitable for BESS as battery costs have decreased while its performance and life have continued to increase. Batteries have been used for lighting, automotive applications and can be the major source of power supplies and compensators in future grids. Today, energy storage systems using batteries have a capacity of up to 40 MWh with an efficiency of up to 90% [22].

The main advantages of battery energy storage technology over other technologies are very quick response time (about 20 milliseconds), the availability of factory-built modules which reduces construction lead time, their simple-efficient way of storing energy, and their less complexity in interfacing with the common RESs, mostly solar and wind energy [23]. However, their main disadvantage is the limited life span. Recently, modern battery technologies such as Li-Ion, Sodium-Sulphur, and Flow batteries are being utilized more frequently in electric applications than other ESS technologies. It can be expected that considering the popularity of BESS, within the upcoming future, improved and more efficient batteries will be realized at a reasonable cost [23]. Figure 1.4 presents the power, energy, and cost characteristics of various high-power storage technologies.

1.2. Major Components of a Battery Energy Storage Systems

As discussed in the previous section, in order to address the issue of sporadic availability of renewable resources and improve the quality of the power system, energy storage systems can be introduced to the system. Depending on the application, power and energy rating, response time, operating temperature, etc., the choice of the ESS will be different [24]. Due to several advantages of BESS mentioned in [11] including fast response, wide power rating range, etc., it is one the most popular energy storage technologies. BESS is used for various purposes in all sectors (generation, transmission, and distribution) of electrical power systems and thus provides benefits to consumers [15]. BESS is a combination of different subsystems. Each subsystem operates along with others to make the total system work. Batteries, battery management systems, and power electronic converters are the major components of a BESS [24].

1.2.1. **Batteries**

A battery is a pack of one or more cells with a positive electrode (cathode), a negative electrode (anode), a separator, and an electrolyte and works by directly converting chemical energy into electrical energy by employing various chemical reactions. Depending on the chemicals and materials used in batteries, the properties (e.g. power rating and energy density, life cycle, etc.) will be different. Consequently, battery companies are constantly investigating to find chemistries that offer better performance.

Due to the advantages including low cost, low self-discharge rates, long life cycle (5-15 years) [25], and despite being the oldest battery energy storage technology, lead-acid (PbA) battery is the most popular and widely used rechargeable storage technology in different applications especially where the low energy density is not an issue [15], [24]. Among the electrolyte batteries, the PbA battery demonstrates a high efficiency (70%-80%) [15], yet, factors such as high toxicity and increased weight, resulted that for certain applications such as energy management, the use of lead-acid batteries has been hindered [26].

Li-Ion is a popular technology for use in BESS. The main advantages of lithium-ion batteries are high efficiency (>90%), high energy density, the rapid response time (in milliseconds), no memory effect, and a low self-discharge rate (5% per mount) [15], [24], [27].

The aforementioned benefits of Li-Ion batteries, make this battery technology attractive. Currently, lithium-ion technology took over 50% of the small portable application market including laptops, cameras, mobile telephones, and has also led to its application as a power source within medical devices [24], [28]. The high energy density of the Li-Ion batteries proves it to be a promising technology for plug-in hybrid and electric vehicle (EV) applications [24]. Yet, the price is still high for many applications and due to the ongoing debate regarding the available worldwide lithium reserves, the price may become more contentious given the limited lithium resources. Another challenge for large-scale utilization of lithium-ion batteries is the requirements of special packaging and internal overcharge protection circuits as the internal resistance can produce internal heat-up and failure [28]. As a result, battery management systems have to be used to ensure the safe operation of the batteries which leads to higher costs [24].

NiCd and NiMh batteries are other technologies used in BESS. NiCd batteries are superior to lead-acid batteries in terms of energy density and cycle life. Due to their lower cost relative to other batteries, and low self-discharge rate, the NiCd battery was preferred for medium-term energy management for a while and was used for applications varying from 1 kW to 0.5 MW [26]. However, due to their lower energy density compared to chemistries such as Li-Ion and NiMH, the toxicity of Cd and presenting some environmental hazards that require complex recycling procedures, they have rapidly lost their market share in the 1990s to NiMH and Li-Ion batteries and their market share dropped significantly [21], [24].

NiMH batteries have gained prominence over NiCd batteries in recent years. Because of their relatively higher power density compared to that of NiCd and PbA batteries, low maintenance, proven safety, and very long life cycle, NiMH batteries have been a popular choice for EV and hybrid electric vehicle (HEV) applications in the 1990s and 2000s, respectively [24]. One of the problems of NiMH chemistry is their relatively high self-discharge rate, therefore, their usages in power system applications are very limited [24], [26].

A comparative analysis of the popular battery technologies for use in BESSs is provided in Table 1.1 and Table 1.2.

Table 1.1- Battery technologies in BESSs [24]

Type	Energy Efficiency (%)	Energy Density (Wh/kg)	Power Density (W/kg)	Cycle Life (cycles)	Self-discharge
Pb-Acid	70-80	20-35	25	200-2000	Low
Ni-Cd	60-90	40-60	140-180	500-2000	Low
Ni-MH	50-80	60-80	220	<3000	High
Li-Ion	>90%	100-200	360	500-2000	Low

Table 1.2- Basic comparison and characteristics of rechargeable batteries [23]

Type	Advantages and Disadvantages	Applications
Pb-Acid	Low cost, high reliability, high efficiency, relatively bulky, cannot be left in the discharged state for long without damage	Photovoltaic systems, automotive applications, emergency power supply system, uninterruptible power supplies (UPS) system
Ni-Cd	long service life, more expensive than lead acid batteries, having “Memory effect”	Stand by and emergency power system such as in photovoltaic applications
Ni-MH	high self-discharge rate, low maintenance, higher power density, cell rupture in high charge rate	electric vehicle and hybrid electric vehicle applications
Li-Ion	High Efficiency (over 90%), long life, high cycle life, high energy density, high cost (above $1200/kWh) and requires safety circuitry	Renewable energy applications, hybrid and electric vehicles, portable electronics such as laptop computers and power tools

1.2.2. **Battery Management Systems**

Batteries are different in terms of chemical and constructing material and are dynamic in nature, operating outside of the equilibrium state. As a result, battery-powered energy storage systems require a battery management system (BMS) to protect the batteries and ensure optimum operation of the overall system, especially in Li-Ion battery technologies where internal heat-up and failures are an issue [29]. Overcharging and deep discharging of Li-Ion chemistry may damage the battery, shortening its lifetime, and even causing hazardous situations [30], [31]. Furthermore, since the system operates in a closed structure with only a few measurable state variables, evaluating the state of the battery is a challenge.

In addition, in most of the applications especially high-power BESS, the batteries are connected in series and parallel to satisfy the specified voltage level due to their low terminal voltage [32]. Yet, fabricating two cells with the same characteristics is highly unlikely. Therefore, due to the difference in performance and characteristics of the series batteries (e.g. different capacities, self-discharge, internal resistances), charge imbalance between the individual cells is a common problem. In addition, non-optimum and extreme charging patterns, high temperatures, overcharging, and undercharging can have severe impacts on the normal operation of the BESS and can degrade the batteries [29].

The simplest BMSs are only responsible for meeting the power demand. However, in order to ensure battery safety and improve the performance of the overall system in sensitive applications such as EVs and grid integration of RES and ESS, smart BMS with modern control techniques (e.g. predictive and adaptive based algorithm) have to be employed.

Figure 1.5 describes the general structure of a BMS. The complete BESS in Figure 1.5 can be used for many different objectives, including peak power demand matching, improving grid stability and power quality, and reducing renewable energy sources’ intermittency.

As mentioned before, due to the closed structure of the battery packs, all the internal states of the cells are not accessible to the BMS. Among all, the only measurable parameters of the system are voltage, current, and temperature. In addition, the only controllable parameters by BMS are current and the ambient temperature (Only if cooling and heating are available). Yet, through an appropriate model of the battery, BMS can accurately estimate the state of the battery including battery state of charge (SOC) and state of health (SOH).

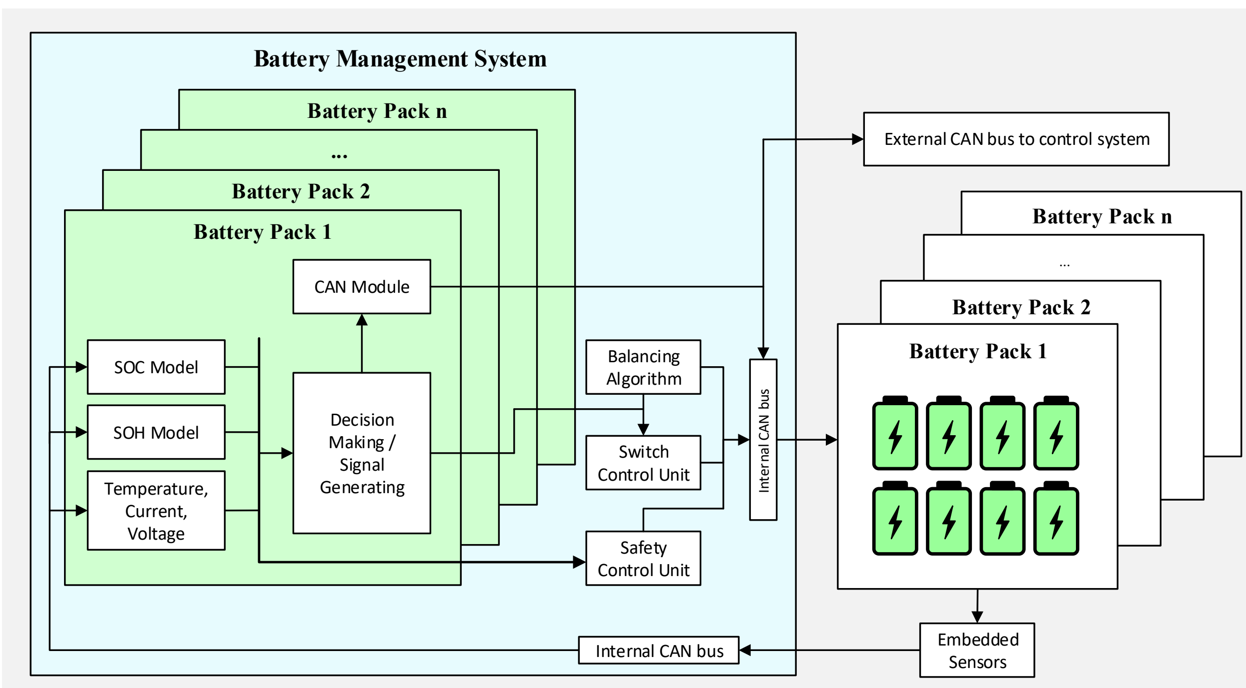


Figure 1.5- Internal structure of a BMS

1.2.3. Power Electronics

Power electronics is the key to integrating the BESS into the electricity grid and ensuring system stability and safe and optimal energy management [33]. The power electronic unit is responsible for bidirectional power flow between the ESS and the grid [29]. Simultaneously, it controls and regulates the operating points of the batteries and functions to meet the grid codes and standards when absorbing/injecting power from/into the grid. The most important requirements for the power electronics unit are summarized below [34].

1. High energy efficiency
2. Low Electromagnetic Interference (EMI)
3. Low cost
4. Proper voltage ratio (i.e. low, medium, high)
5. Low current ripple
6. Availability and reliability in case of electrical failures

Depending on the system configuration, many different converters may be needed for the integration of the BESS. The way these individual converters are structured creating a hierarchical system architecture impacts the system efficiency and operation of the entire system. For instance, in EV, the main bus is DC and due to the existence of high power AC and high power DC charging plugs, a set of AC/DC and DC/DC converters are required. Table 1.3 provides the information on various converters employed in a typical EV. The internal electrical structure of an EV is illustrated in Figure 1.6.

The performance of the bidirectional DC/DC battery charger is linked to the parameters of the battery including the charging time and the battery life. By controlling the charge and discharge operation of the battery, the bidirectional DC/DC battery charger regulates the bus voltage and battery current, prolonging its service life and minimizing the maintenance cost of the entire BESS. Further, the operation of the battery charger depends on the components, control, and switching strategies and must be efficient, reliable with high power density, etc. [40].

The bidirectional AC/DC converter operates as a rectifier at times the power is transferred from the grid to the BESS charging the battery. Alternately, it works as an inverter when the power is injected into the grid in the opposite direction.

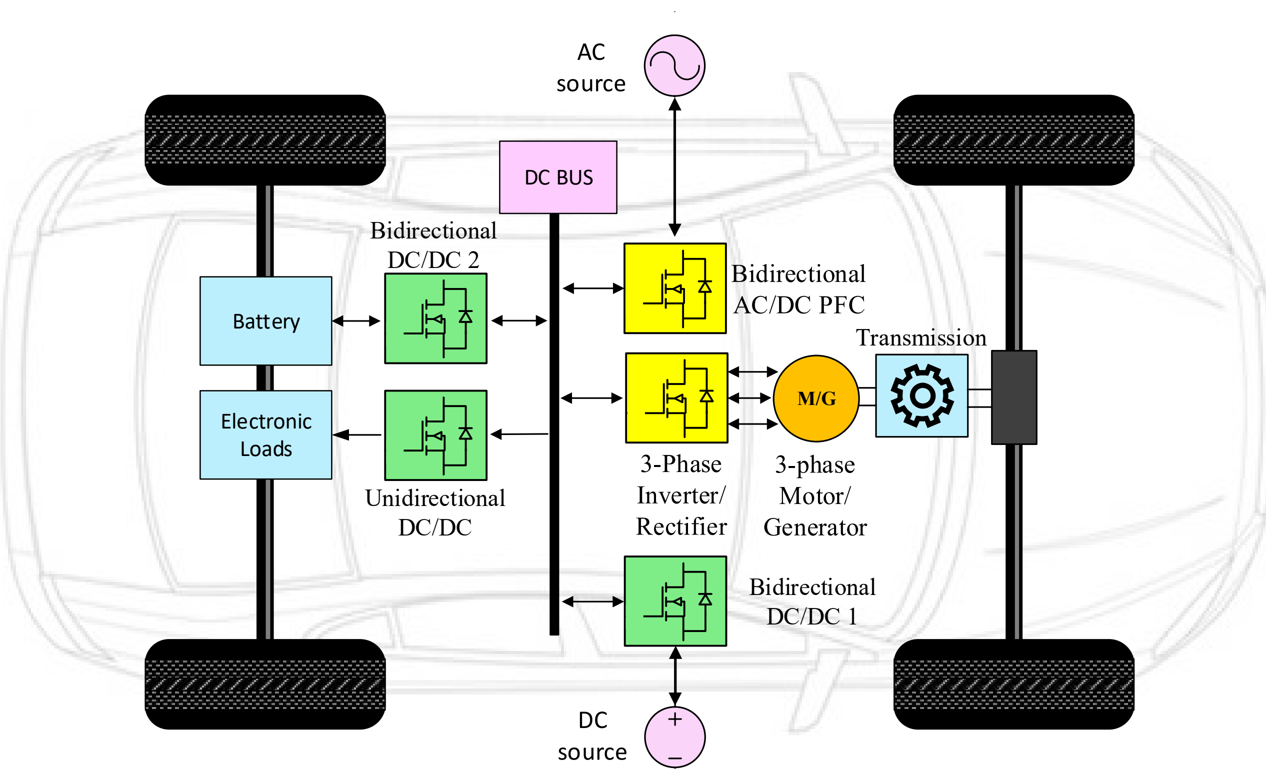


Figure 1.6- Internal electrical structure of an EV

Table 1.3- Power electronic components of a bidirectional dc-coupled electric storage system

Converter	Description
Bidirectional AC/DC Power Factor Correction Converter	Absorbs/Injects the power from/into the grid based on the direction of power flow and improves the power factor simultaneously
Bidirectional DC/DC Converter 1	Absorbs/Injects the power from/into the dc source based on the direction of power flow
Bidirectional DC/DC Converter 2	Controls the charge of the battery by charging and discharging it according the control system
Bidirectional 3-phase inverter/rectifier Traction Drive	Controls the speed of the traction motor and injects the power to in regenerative mode
Unidirectional DC/DC Converter	Adjusts the voltage level and provide power to the dc loads

The bidirectional AC/DC circuit, also called power factor correction (PFC) unit, ensures that the AC current is drawn and injected with a close-to-unity power factor and low distortion to minimize the power quality issues. Also, the PFC circuit must be able to transfer reactive power into the grid when needed to provide stability.

1.2.3.1. Power Losses

Power losses in a power electronic converter mainly consist of steady-state conduction loss and switching loss [36]–[38].

I. Switching Losses

When the switch is turned ON or OFF, the transition time needed to achieve the next state is very short, but it is not instantaneous. The time which the switch needs to fully transition between ON and OFF states produces wasted energy, known as a switching loss. Switching losses occur at the intersection of the voltage and current waveforms and are generated in the form of heat negatively affecting the switch performance.

a) Hard Switching

Hard switching occurs when there is an overlap between the voltage and current when turning the power switch ON and OFF. The overlap between the current and voltage causes

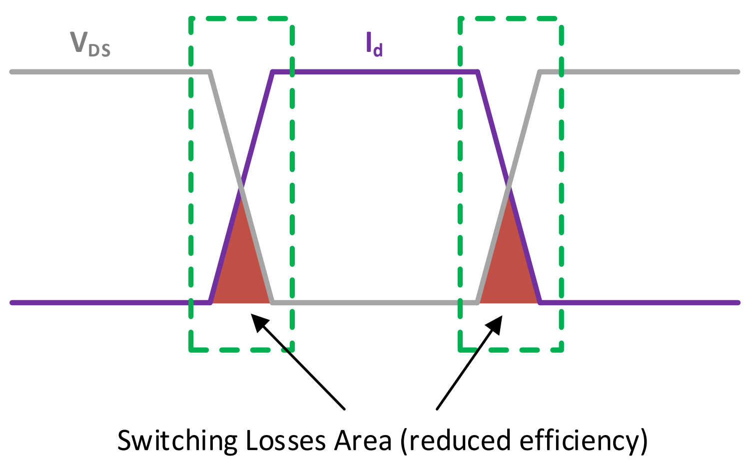


Figure 1.7- Hard switching MOSFET current and voltage waveform

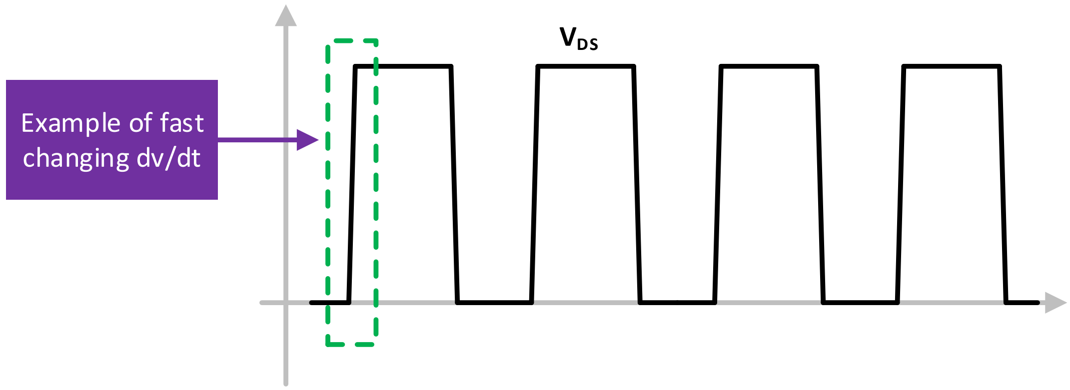


Figure 1.8- Fast changing dv/dt waveform (V_{DS})

energy losses. The overlap and consequently the dissipated power can be minimized by increasing the *di*/*dt* and *dv*/*dt*. Yet, there is a tradeoff between the switching losses and the rate of *di*/*dt* or *dv*/*dt*. High *di*/*dt* or *dv*/*dt* leads to the appearance of electromagnetic interference (EMI) and noises in the converter distorting the normal operation of the circuit. As a result, the *di*/*dt* and *dv*/*dt* should be optimized to avoid EMI issues.

To achieve high efficiencies, power converters with hard switching need to operate with relatively lower switching frequencies. Consequently, the size of the circuit components must be increased to hold the power for a longer period due to lower switching frequencies. In addition, by reducing the switching frequency, harmonic distortion and output ripple increase. As a result, to improve the quality of the power, larger output filters are needed which in turn, contributes to a higher cost, size, and weight of the converter.

b) Soft Switching

In soft switching, the idea is to prevent the overlap of the voltage and current waveforms during switch commutation by using external circuits [39]. Soft switching happens when the

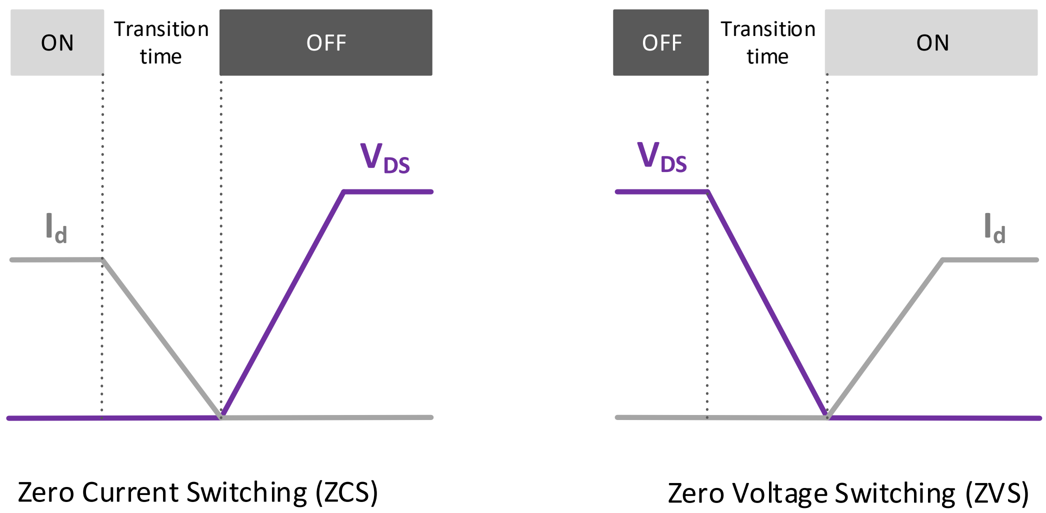


Figure 1.9- Soft switching MOSFET current and voltage waveform

voltage across the switch becomes zero before the switch is turned ON (zero voltage switching) and the current of the switch becomes zero before the switch is turned OFF (zero current switching). By adding a resonant circuit, the commutation time can be accurately adjusted in a way to introduce an offset between the current and voltage waveforms preventing the overlap between them. The benefits of resonant soft-switching are the elimination of the switching losses, an increase in efficiency, and a reduction in EMI.

II. Conduction Losses

The conduction losses are the losses that occur while the switch or the freewheeling diode is ON and conducting current. The total power that is dissipated during the ON-state is obtained by multiplying switch voltage and the current. The conduction losses are independent of the switching frequency but dependent on the duty cycle, therefore in the PWM (pulse-width modulation) applications, the total dissipated power is obtained by multiplying the calculated conduction loss by the duty ratio. Switching losses on the other hand are dependent on and are directly proportional to the switching frequency.

III. Reverse Recovery Time

During the diode transition from the ON-state to the blocking state, the energy that is stored in the diode must be discharged. The discharge process takes a finite amount of time known as the reverse recovery time (t_{rr}) [40]. During the reverse recovery time, the diode current may flow in the reverse direction to discharge the stored energy.

As the operating power and switching frequency increase, the reverse recovery time becomes more critical. The higher the switching frequency, the higher the power dissipated in the reverse direction. As a result, in high power high voltage applications, t_{rr} becomes a limiting factor on the rating and selection of the diodes.

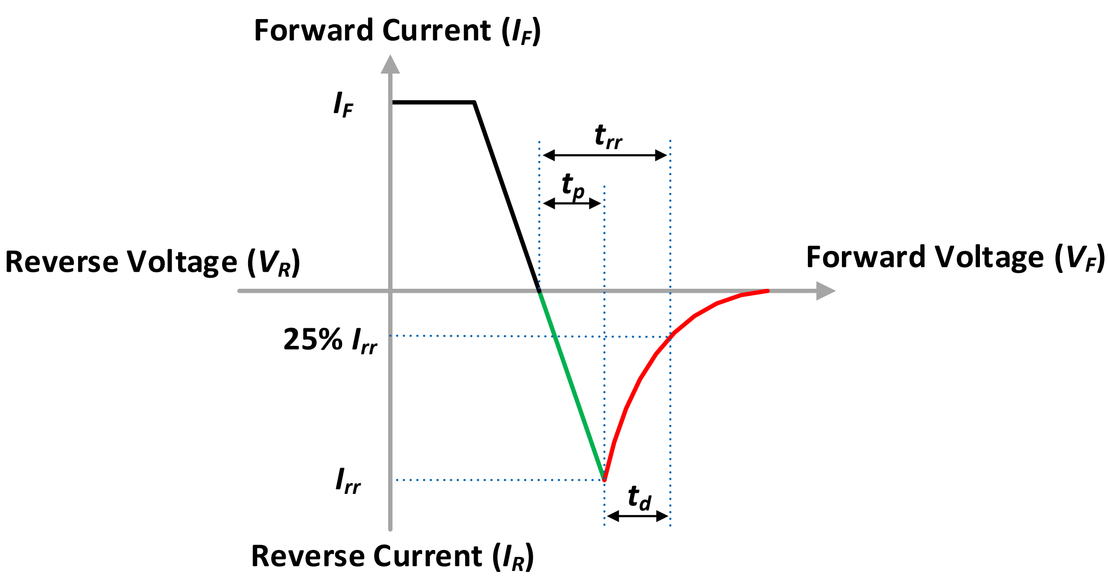


Figure 1.10- Reverse recovery characteristic of a diode

1.2.3.2. Wide Band-Gap Devices

The key to the next generation of energy-efficient converters lies in the use of new materials and technologies in switch manufacturing such as wide band-gap semiconductors (WBG) [41], [42]. Significant research has been done for the development and application of WBG semiconductor devices in power electronics.

The main advantages of the WBG switches over the conventional silicon (Si) switches are their low losses, high switching frequency, and high-temperature operation capability which helps increase the efficiency, low levels of electromagnetic interference (EMI), reducing the size and weight, lowering the overall cost or all of them together. Silicon carbide (SiC) and gallium nitride (GaN) are the two most prominent WBG materials for use in power switches.

I. Silicon Carbide (SiC) Switches

Silicon-made switches have had a major share of the market for high-voltage applications. In recent years, however, Si has been replaced with SiC technology due to the growth in process technology. SiC has a wide band-gap of 3 electronvolts (eV) and a much higher thermal conductivity compared to silicon (slightly better than copper). As a result, SiC switches are most suited for high-power applications with high switching frequency. In addition, SiC has a relatively low thermal coefficient of expansion, which makes the switch parameters such as on-state drain-source resistance ($R_{DS(ON)}$) change less with temperature and prevents the switch from getting damaged in high temperatures and thermal cycling. Currently, SiC switches haven't reached their maximum potential due to the design and manufacturing challenges for very high-voltage modules.

II. Gallium Nitride (GaN) Switches

Compared to silicon, the breakdown field of GaN devices is ten times higher and the electron mobility is double (3.4 electronvolt for GaN and 1.14 electronvolt for Si). GaN also has a higher band-gap and consequently higher electron mobility than that of SiC (2.3 to 3.3 electronvolt). GaN has roughly the same thermal conductivity as Si-based semiconductors. However, the reverse recovery charge of the GaN devices is almost zero which makes it a perfect choice for high-frequency applications. GaN is a promising technology in modern resonant topologies that enables new approaches and applications.

To summarize, SiC is a proper choice and is fast enough for any power conversion applications, and its overall higher ruggedness is a real plus, too. GaN is extremely fast for its own good and is most suitable for applications in which space is at a premium, and where MHz switching speeds are a must (e.g. low-voltage DC/DC converters). The characteristics of Si,

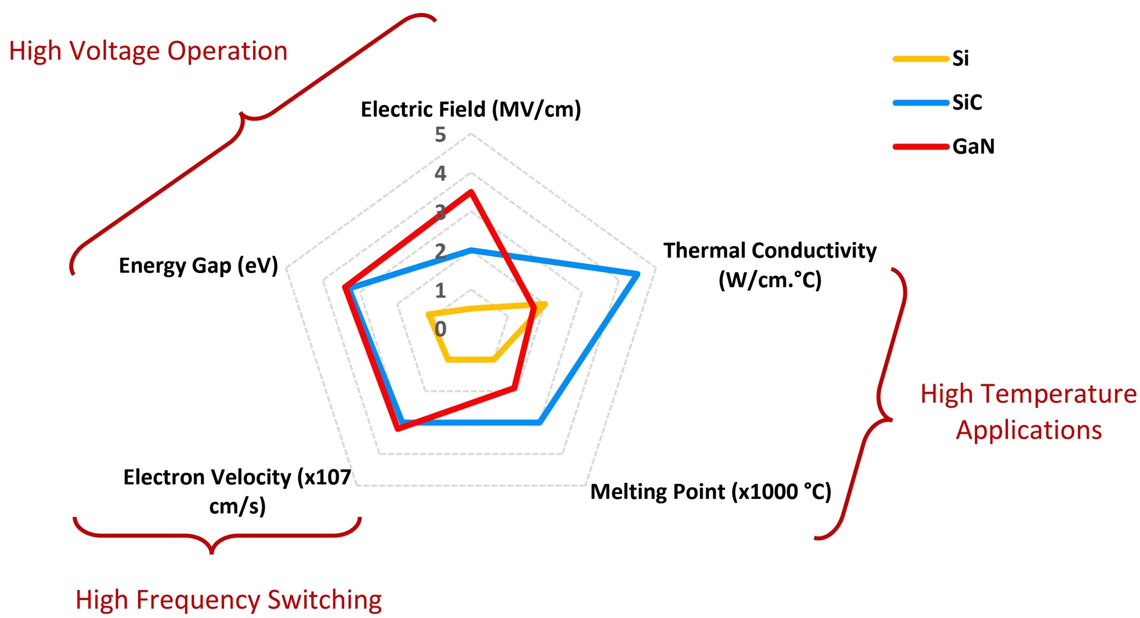


Figure 1.11- Comparison of Si, SiC, GaN switch technologies [28]

SiC, and GaN devices are demonstrated and compared in Figure 1.11. The switching frequency range and power rating of WBG technologies and their applications are given in Figure 1.12.

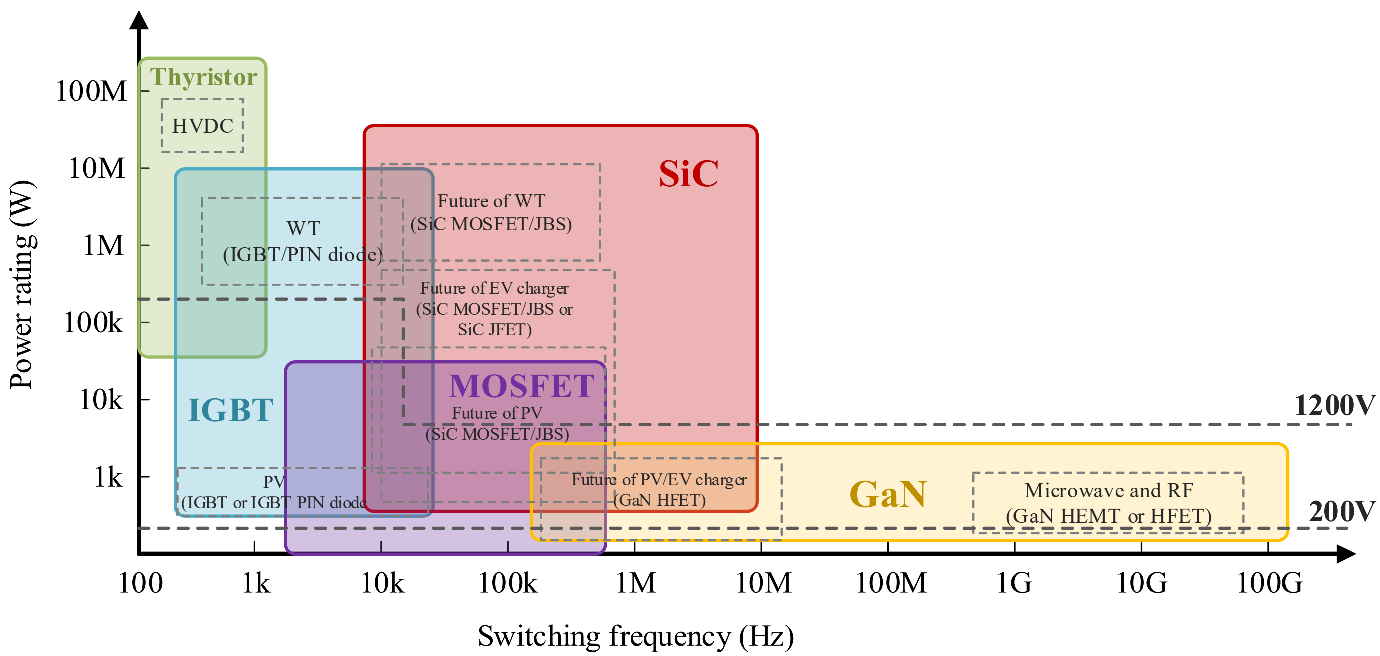


Figure 1.12- Si, SiC, and GaN-based applications

1.3. Power Converters for Energy Storage Applications

Bidirectional power converters are the key in enabling bidirectional power exchange between the grid and the RES or ESS. Generally for this purpose, a two-stage bidirectional AC/DC converter including an AC/DC PFC converter and a bidirectional DC/DC converter is used for BESS [43].

Bidirectional AC/DC converters for ESS are developed to provide controlled and uncontrolled unidirectional and bidirectional power conversion. They may suffer from low power quality, high current harmonics, low power factor at the AC input, low efficiency and high ripple output DC voltage. Consequently, various filter topologies have been developed to improve the quality of the power. Yet, these filters are costly, bulky and reduces the overall efficiency of the circuit.

Based on the grid requirements, a bidirectional converter needs to function smoothly in both directions. In charging mode, the converter has to absorb a clean sinusoidal current with close to unity power factor. In the discharge mode, the converter has to inject a similar sinusoidal current in phase with the voltage with low harmonics to comply with the grid code. This can be done by many different converter topologies, yet all of them must follow the basic diagram depicted in Figure 1.13.

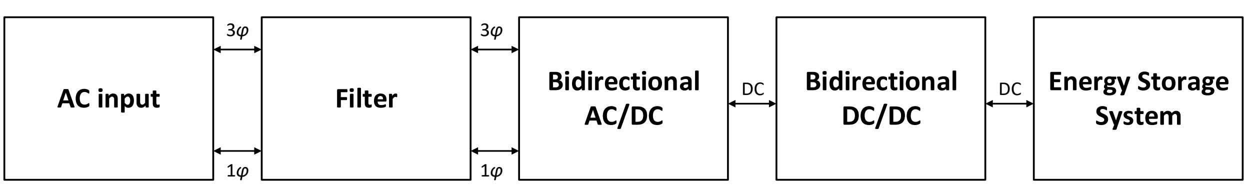


Figure 1.13- General topology of a bidirectional charger for energy storage systems

In the charging mode, the filter first eliminates the unwanted harmonics of the input current. The filtered AC current then is rectified into a DC current and is fed to the bidirectional DC/DC converter. The bidirectional DC/DC converter adjusts the voltage to match the voltage of the ESS.

In the discharging mode, this process is reversed. The DC current leaves the energy storage unit and goes through the bidirectional DC/DC converter. The DC/DC converter then adjusts the voltage to match the DC-link voltage on the grid side. The DC voltage and current then pass through the AC/DC PFC converter being inverted into AC voltage and current. The filter and the AC/DC PFC ensure the AC voltage is in phase with the AC current and the injected current complies with the grid requirements.

1.3.1. **Bidirectional DC/DC Converters**

The bidirectional DC/DC converter is responsible for converting the DC output of the AC/DC PFC circuit to the battery voltage level to transfer power to the battery pack in the charging mode and discharge the battery when needed, coupling the AC/DC converter to the energy storage unit. Several bidirectional DC/DC converters are presented in the literature [44]–[49] which can accomplish the tasks outlined by the general topology.

In low-voltage low-power applications, a non-isolated buck/boost bidirectional converter has been preferred in many studies due to its simple structure, low cost, and high efficiency. However, in medium to high voltage high power applications such as the DC/DC bidirectional converter in EVs, the two-switch structure exhibits several shortcomings, including low efficiency at light load [49]. In [50], a bidirectional fly-back converter is presented. It is simple and is capable of achieving soft-switching operation, but its efficiency suffers at high-power applications.

According to [51], the DC/DC converters are classified into four main general groups of configurations, namely transformer-based converters, coupled-inductor-based converters, switched capacitor converter with resonant inductors, and switched capacitor converters with coupled inductor topologies.

In the transformer-based DC/DC topologies, the high-frequency transformer provides galvanic isolation and large voltage/current gain while reducing the voltage stress over the switches. In this category, LLC and DAB (Dual Active Bridge) converters are among the popular topologies.

In the coupled-inductor-based converters, with a similar structure as the transformer, coupled inductors based on different windings with electrical connections are used to improve the voltage gain. The main advantages of the coupled-inductor-based converters are the wide input voltage range and reduced input current ripples. Basic and interleaved coupled inductors are taken as typical examples of converters in this category.

Switched-capacitor circuits and their derivative topologies are gradually adopted in high voltage conversion ratio applications. Switch-capacitor-based topologies with a resonant inductor can provide soft-switching and soft-charging and have good scalability. For high voltage conversion ratio and high-frequency operations, many topologies are proposed based on the two basic architectures to solve the above issues, which can be classified into two distinct categories of the ladder and Dickson topologies.

The last category of the DC/DC converters is the switched-capacitor with coupled inductor-based topologies. The coupled inductors can be adopted to increase the voltage gain of switched-capacitor converters dramatically, which does not depend on the number of capacitors. Table 1.4 provides a summary of the high-frequency high voltage conversion ratio bidirectional DC/DC converters discussed in the literature [51]–[53].

Table 1.4- Summary of high-frequency bidirectional DC/DC converter topologies

<table>
<tr><th colspan="2">Topology</th><th>Advantages</th><th>Disadvantages</th></tr>
<tr><td rowspan="3">Transformer-based converters</td><td>LLC</td><td rowspan="3">• Isolation
• Volume reduction by using leakage inductor to resonant
• Lower current stress and current ripple
• Flexible controllability
• High-voltage conversion can be achieved</td><td rowspan="2">• Large number of switches
• DC-link level voltage stress over the switches</td></tr>
<tr><td>DAB</td></tr>
<tr><td>Proposed multi-mode converter</td><td>• Large number of switches</td></tr>
<tr><td rowspan="3">Converters with coupled inductors</td><td>Basic coupled inductor</td><td>• Soft-switching capability</td><td>• Lower operating frequency
• Non-isolated structure
• High inrush current stress</td></tr>
<tr><td>Interleaved coupled-inductor</td><td>• Boosted output voltage
• Low input current ripple
• Increased rating power</td><td>• Large amount of components
• Bulky structure</td></tr>
<tr><td>Topologies with basic modules</td><td>• Reduced leakage energy
• Lower high voltage spikes</td><td>• Non-isolated structure</td></tr>
<tr><td rowspan="2">Switched-Capacitor Converters</td><td>Ladder-based</td><td>• High power density
• Fast dynamic response</td><td rowspan="2">• High inrush current stress
• Discrete output voltage
• Large amount of capacitors
• Large voltage stress on capacitors</td></tr>
<tr><td>Dickson-based</td><td>• Soft charging and switching to improve efficiency</td></tr>
<tr><td rowspan="3">Switched-capacitor with coupled inductor</td><td>Ladder-based</td><td>• High design freedom
• PWM controllability</td><td>• Voltage spikes caused by leakage inductance
• Complex magnetic design</td></tr>
<tr><td>2 windings</td><td rowspan="2">• High boost ability
• Reduced switch voltage stress and conduction loss</td><td rowspan="2">• Voltage spikes caused by leakage inductance
• Diode recovery problems</td></tr>
<tr><td>3 windings</td></tr>
</table>

Dual active bridge (DAB), Three-level (TL) bidirectional converters, and the 4-switch string inverter/rectifier-based bidirectional converters are among the popular topologies used to provide bidirectional energy flow between the energy storage element and the DC input source [54]–[56].

1.3.1.1. Dual Active Bridge DC/DC Converter

Dual active bridge (DAB) based DC/DC converters are the most popular topology and are widely used for providing bidirectional power flow between the DC sources while realizing soft switching for the switches [54], [57]. It is composed of two active bridges with a passive element bank in between (mostly inductors and/or a transformer for galvanic isolation). The diagram of a bidirectional DAB demonstrated in Figure 1.14 consists of two full-bridges with 8 switches and their free-wheeling diodes, two inductors, and one transformer.

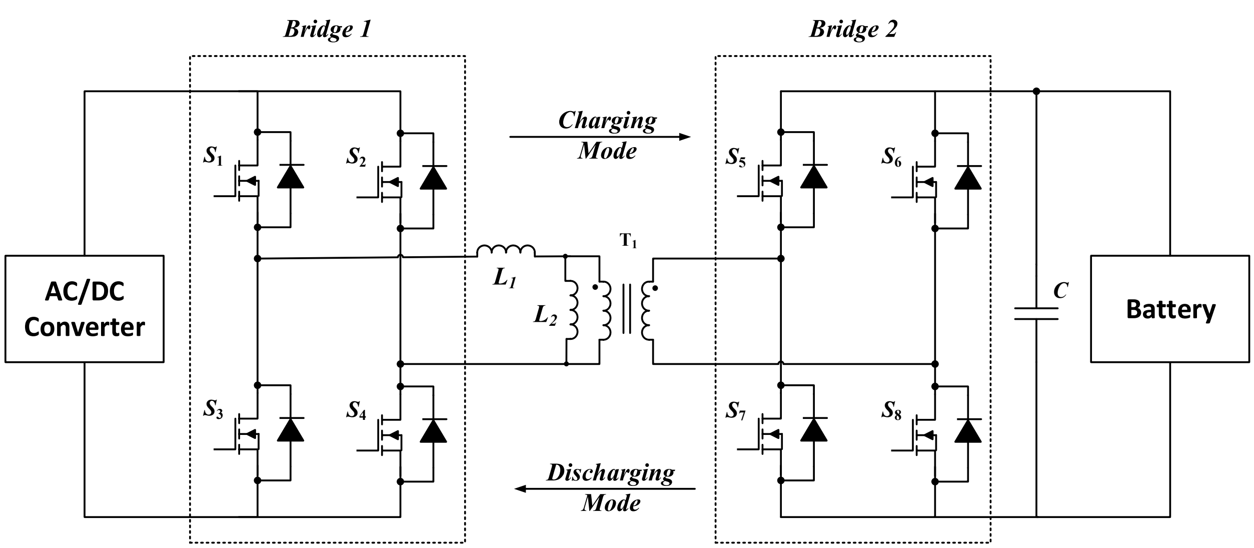


Figure 1.14- Topology of the Dual Active Bridge (DAB) DC/DC converter

In the charging mode, the first bridge operates as an inverter generating a high-frequency AC voltage at the primary side of the middle tank, while the second bridge acts as a full-wave rectifier and through the body diodes of switch S_6-S_8, the current is rectified to DC and is delivered to the battery. The second bridge also allows active switching in the rectifying mode. When the converter operates in the opposite direction discharging the battery, the second bridge acts as an inverter generating a high-frequency AC waveform at the secondary of the transformer. The first bridge then acts as a rectifier converting the high-frequency AC voltage to a DC voltage. Similarly, bridge 1 can also be actively switched if needed.

The higher the frequency of the waveform generated by the inverter, the smaller transformer can be used for galvanic isolation. It should be noted that due to the high number of switches contained in this circuit, ZVS and ZCS techniques has to be implemented to reduce the switching losses. While the DAB converter provides a high power density and fast control, the soft-switching region of a conventional DAB converter is only limited to a narrow output voltage range and the voltage stress across each power switch is equal to the DC-link voltage [43].

1.3.1.2. Three-level (TL) Bidirectional DC/DC Converter

Three-level (TL) based bidirectional converters shown in Figure 1.15 have been reported in the literature [58]–[63]. They are popular as they are able to reduce the voltage stress across the switches while doubling the frequency of the output voltage ripple when the circuit operates in rectifying mode, hence reducing the output voltage ripple. Due to the asymmetric loss distribution between the inner and outer switches in the TL circuit, as well as the DC-link capacitor unbalance voltage distribution, an active TL circuit has been reported [60] by replacing the two diodes with switches. In [61], a comparative study on various TL-based resonant and soft-switching converters has been reported. A drawback with the TL circuit when it is used in conjunction with resonant circuits is that as the duration of the zero voltage level increases at the output of the inverter, the maximum achievable gain of the resonant converter decreases. It also loses soft-switching operation as the converter operates away from full load conditions [61].

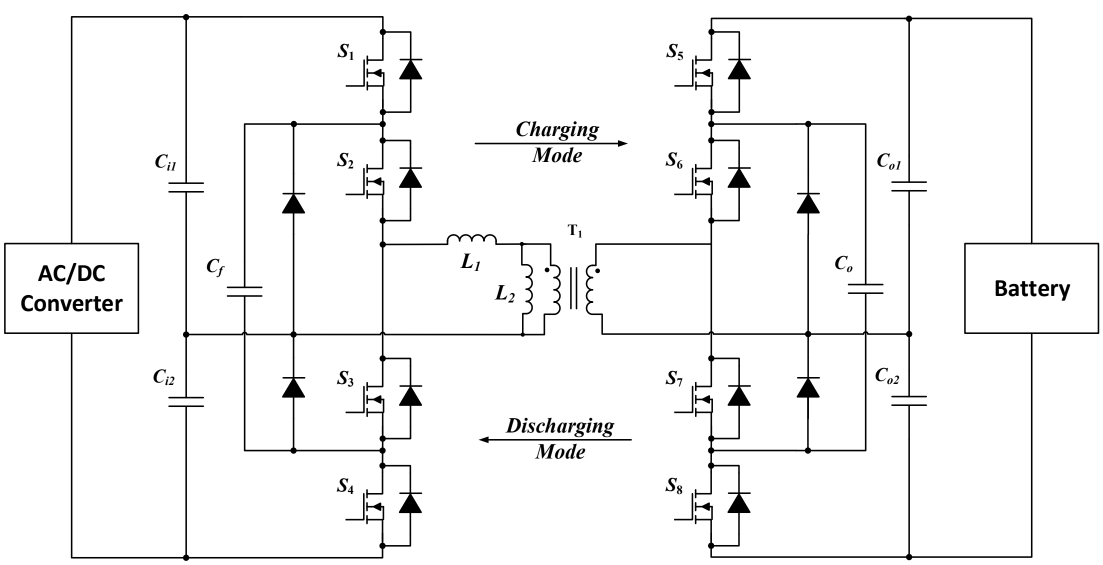


Figure 1.15- Topology of the TL bidirectional DC/DC converter

Different additional passive or active auxiliary circuits have been reported to aid the TL converter to extend soft-switching operation [58], [61], [62].

1.3.1.3. 4-Switch String Structure Bidirectional DC/DC Converter

Another type of bidirectional converter for the use in energy storage applications is the 4-switch string structured rectifier/inverter circuit (see Figure 1.16) in which the voltage stress is equally distributed among the switches and is reduced by half compared to that of the conventional full-bridge inverters, making it a suitable choice for medium and high voltage applications [55]. However, in this topology, when the circuit operates in the rectifying mode, the circuit operates as a half-wave rectifier and only the positive current flows through the output capacitor while the negative current circulates in the resonant circuit, leading to higher

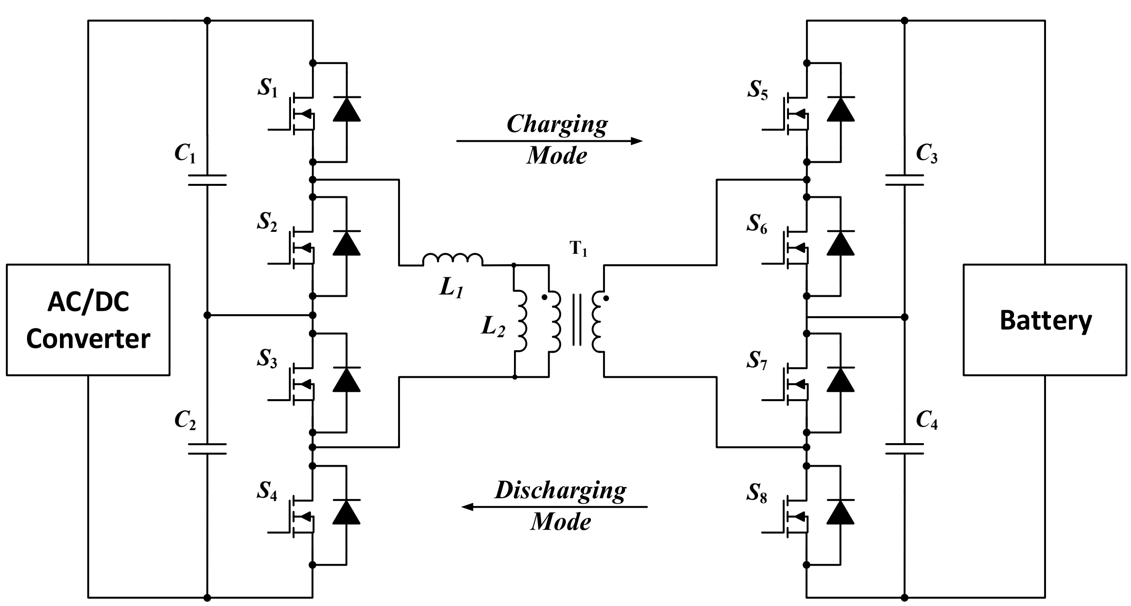


Figure 1.16- Topology of the 4-switch string DC/DC converter

voltage ripple in the load with the frequency of the output current ripple equals to the switching frequency (Figure 1.17) [56].

1.3.2. **Bidirectional AC/DC Power Factor Correction Converters**

The AC/DC power factor correction converter is added at the utility interface in order to make the AC current in phase with the voltage and increase the power factor and as a result, improve the quality of the power drawn/injected from/to the grid [43]. In addition, the PFC circuit converts the AC current into a DC current in the charging mode and the DC current to an AC current in the opposite direction. Different PFC topologies have been developed based on the application and the associated requirements in the AC side as well as the DC load, yet

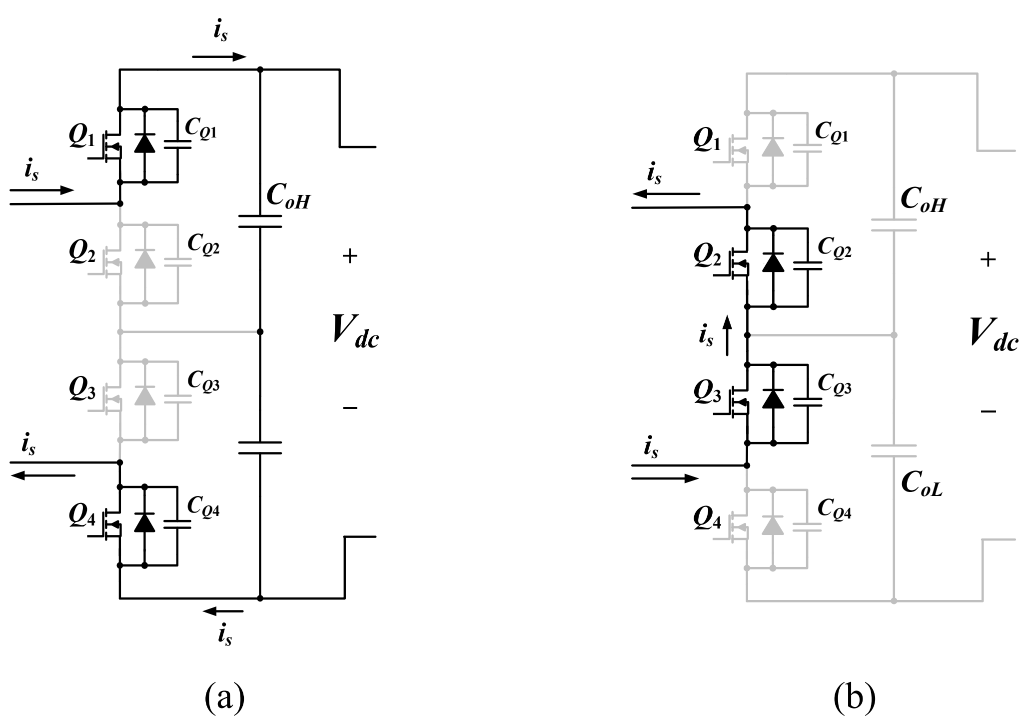


Figure 1.17- Topology of the 4-switch string converter in the rectifier block including the current path for: a) positive i_s, b) negative i_s

this thesis focuses on the development and control of bidirectional DC/DC converters and the bidirectional AC/DC power converters are out of the scope of this thesis.

1.3.3. Resonant Converters

In light of their soft-switching ability, resonant converters are appealing in high-power applications. A typical structure of the resonant circuit is shown in Figure 1.18. The inverter generates a high-frequency pulsating voltage at the input terminal of the resonant tank consisting of passive elements. Depending on the switching frequency, the resonant converter increases or reduces the voltage level at the output terminal. The high-frequency voltage generated at the output terminals of the resonant tank is then rectified by means of the rectifier circuit and the DC voltage/current is delivered to the load. The gain of the resonant circuit can be modified by changing the switching frequency of the pulsating voltage at its input terminal.

The main disadvantages of the *LC* series/parallel resonant converters are the voltage regulation and efficiency at light loads along with the high circulating current. In order to address the abovementioned shortcomings of the *LC* resonant circuits, other elements can be

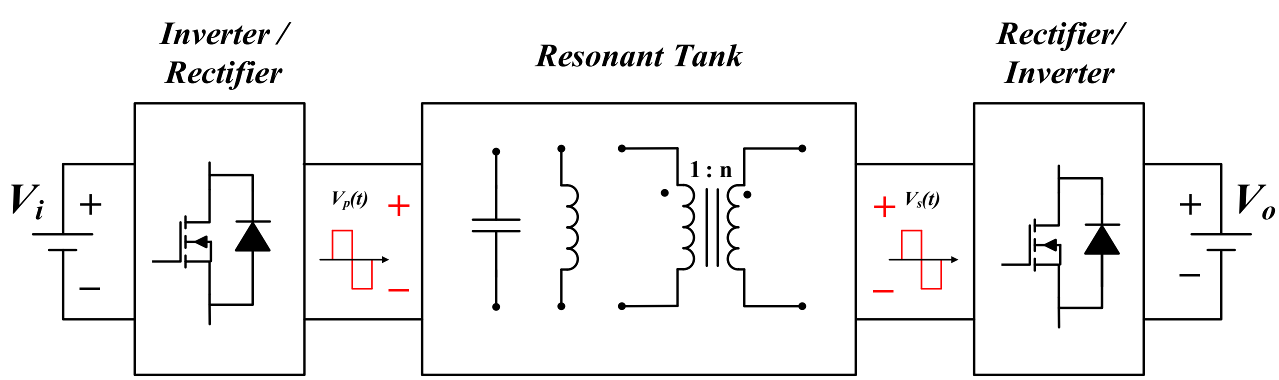


Figure 1.18- General structure of a soft-switched DC/DC resonant converter

introduced to the existing *LC* topology [64], [65]. Among the presented topologies in [59], *LLC*, *LCC* are the most popular ones. While the *LLC* and *LCC* converters combine the properties of both series and parallel resonant converters by retaining their benefits and relieving their disadvantages, the *LCC* resonant converter is dominated by parallel resonant frequency and as a result, exhibits the same deficiencies. High circulating current in *LCC* resonant converters may lead to lower converter efficiency and increase the current stress. In addition, *LCC* resonant converters cannot achieve zero current switching (ZCS) on the rectifier side.

1.4. Reliability of Power Electronic Systems for Energy Storage Applications

Renewable energy generation, energy storage, smart and micro-grid technologies are underpinned by power electronics as the core of their energy conversion process. Yet, power electronics is a frequent source of failure and may cause downtime and high costs in different applications [66]. As the promising wide band-gap devices are not fully developed and power electronics for energy storage applications is not fully mature yet, modern reliability engineering methods are steadily being developed and applied to the energy storage sector, and research is being done on the reliability and fault diagnosis of power electronic converters to prevent converter damage, loss of production to end-users, and to reduce their high maintenance costs.

As illustrated in Figure 1.11, the WBG technologies demonstrated different characteristics including switching frequency, high voltage, high-temperature operation, etc. As a result, each

WBG device technology may exhibit different behavior under transients and unexpected circumstances. Surveys and field experiences have shown that due to high power and thermal stress, power semiconductor devices (MOSFETs, IGBTs, etc.) account for over 30–35% of all converter faults [67].

The switch faults in power converters can be categorized as open circuit fault (OCF) and short circuit fault (SCF) [68]. The SCF is the most severe type of switch-fault and gives rise to a high current that exceeds the rated current of the circuit components. Failing to detect and address this fault and to protect the converter fast enough can cause the entire power converter to fail. However, due to the severity of the SCFs, switch drive circuits have integrated monitoring and protection to prevent it. Although the OCF is not as severe as the SCF, failing to diagnose it fast enough can cause components' overstress and lead to secondary failures of other components due to voltage/current distortion. Therefore, proper fault-detection and diagnostic methods along with device-fault-tolerant systems must be included in the converter design and the development of the control system to avoid system failure and a power interruption.

1.5. Voltage Regulation and Control Principles in Power Converters

Renewable energy sources, e.g., PV and fuel cell, feature a wide range of output voltage [69]. In addition, in energy storage applications, to increase the battery life-cycle and efficiently charge the battery, the normal charging is divided into two zones namely the constant current (CC) zone where the battery is charged with its maximum allowed current and constant voltage zone (CV) in which the voltage across the battery pack is maintained to be constant to its maximum allowed voltage [70], [71]. The two zones are demonstrated in Figure 1.19 where V_B is the battery pack voltage, V_{BM} is the maximum battery voltage, I_B is the battery current, I_{BM} is the maximum allowed battery current, and P_B is the power going through the battery pack. As can be seen in Figure 1.19, in the CC zone, while the charging current is kept constant, the voltage varies to efficiently charge the battery while increasing the battery life cycle. Hence, the converter must be able to achieve a wide output voltage range to provide the voltage/current profile illustrated in Figure 1.19.

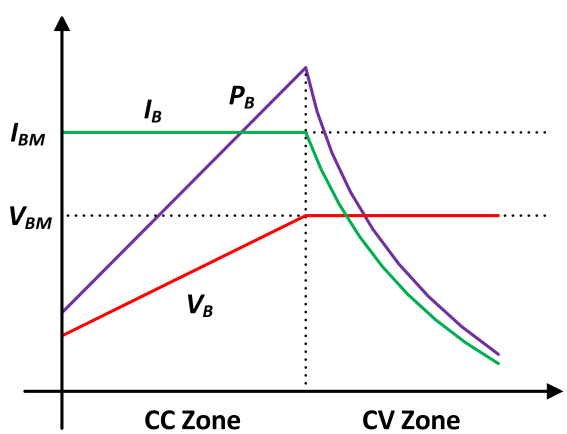


Figure 1.19- Battery's voltage, current, and power profile during the CC/CV charging process

Consequently, the DC/DC converter integrating the RES and BESS should be capable of maintaining high efficiency over a wide input/output voltage range. The resonant converters have been widely adopted by industries due to their soft-switching capability and their excellent performance in efficiency and power density. Nevertheless, in the case of using a variable frequency modulation control and a significant change in the input voltage, the switching frequency variation is considerably large and the resonant circuit operates far away from its optimized point which leads to a limited soft-switching area and a limited light-load regulation ability.

In order to provide output voltage regulation for a wide gain range, and achieve a flat efficiency curve, many approaches have been presented in the literature including reconfiguration of the resonant tank, restructuring the primary-side or the secondary-side switch network, and modification in control strategies [69], [72]–[79]; however, each of the aforementioned approaches suffers from one or several issues including the complicated design of the resonant components, complicated design of the controller with high-frequency oscillation in the output and inability of the converter to maintain high efficiencies when dealing with both wide-input and wide-output voltages.

In addition to the wide gain range issue, many bidirectional DC/DC topologies including the 4-switch string converter suffer from a voltage imbalance between the upper and lower capacitors of the DC-link [80]. This voltage imbalance is considered a system imperfection, which is caused by the difference in hardware components or switching operations of the converter. The unbalanced voltage across the input/output capacitors would result in unsafe operation of the devices and capacitors and even damage the converter. Many strategies have been proposed to solve the input/output capacitor voltage imbalance problem including introducing additional balancing circuits or employing modulation techniques to address this issue.

As a result, a proper comprehensive control system needs to be developed to ensure voltage regulation for a wide input wide output voltage, maintain a flat efficiency curve for different loading conditions, and achieve ZVS turn ON and ZCS turn OFF for all of the semiconductor devices, balance the voltage distribution across the input/output capacitors and provide fault-tolerant operation in the converter experiences a fault incident.

1.6. Technical Challenges and Possible Solutions

Traditionally, to integrate a high power energy storage system into the grid, a power transformer operating at 50/60 Hz frequency is utilized which is large and inefficient. In addition, in high power applications, the power loss associated with the hard-switching leads to a dramatic increase in the operating temperature which may damage the components. In the case of hard-switching along with the use of traditional semiconductor devices, the converter is unable to operate at high frequencies which imposes stress exceeding than the rated values over the components, and the overall converter including the transformer becomes bulky and big.

In addition to the aforementioned challenges, the use of improper converter topologies in the bidirectional power conversion and imposing voltage and current stress over the circuit components may lead to failures in the converter or the energy storage system and the power transfer may be interrupted. As a result, selecting a proper topology is key in the development of a reliable power converter. Finally, developing a comprehensive control system with a fault-tolerant operation while achieving high efficiencies in different loading conditions for a wide gain range is critical to ensure that the energy storage operates safely and the quality of the power injected from the storage into the grid and vice versa is guaranteed.

1.7. Research Objectives

Various types of power converter topologies along with different resonant circuits have been introduced and investigated for bidirectional energy storage applications. Yet, the existing converter topologies for high-power applications face one or more of the following challenges.

- Limited soft-switching condition or hard-switching (i.e. low efficiency)
- High voltage stress over the semiconductor devices
- Lack of voltage balancing technique and asymmetrical loss distribution over the switches
- Low to medium switching frequency operation
- Lack of fault-tolerant operation control
- Low efficiency at light loads
- Narrow voltage gain region

The proposed research is aimed at developing a novel converter topology along with a comprehensive control system to provide bidirectional power conversion for energy storage applications while addressing the aforementioned challenges. In particular, the objectives of this thesis are to:

- develop a new multi-mode inverter/rectifier leg for use in bidirectional converter to facilitate various operating modes depends on the voltage gain and load conditions.
- develop a fault-tolerant control scheme with the proposed multi-mode inverter/rectifier leg to enable seamless post-fault converter operation.
- develop a comprehensive control system that features a multi-mode operating strategy to achieve high efficiency for different loading conditions with wide voltage gain range capability.

In the proposed bidirectional multi-mode stacked-switch converter, by employing a CLLC resonant tank and achieving soft-switching as well as utilizing SiC switches, the switching has been increased significantly to above 100 kHz which resulted in reduced switching losses and converter size.

The proposed multi-mode topology also reduces the voltage stress over the switches by half compared to that of the DAB converter.

The multi-mode operation of the proposed topology enables the converter to continue to deliver power to the load in the case of an open-circuit fault in any of the switches and ensures a safe and reliable operation and avoids the O&M costs in the case of the converter failure.

The developed hybrid comprehensive control system extends the gain range of the converter while ensuring a narrow switching frequency spectrum. By doing so, the efficiency of the converter has been improved and a flat efficiency curve has been achieved in light loads. Also, the voltages across the switches and the capacitors have been balanced by the proposed comprehensive control system.

As a result, the proposed bidirectional topology and the developed comprehensive control system contributes to the development of high efficiency, reliable and low-cost power converters for energy storage applications, and provides incentives to install and make use of renewable energy sources.

1.8. Dissertation Outline

In Chapter 1, different types of energy storage technologies have been introduced and battery energy storage systems were investigated as the main technology for realizing bidirectional power conversion in this thesis. Major components of a BESS were presented. Modern wide band-gap semiconductor devices were introduced and their applications were discussed. Then, several existing power converters for battery energy storage systems along with their advantages and shortcomings were reviewed. Towards the end, the research motivations of this thesis, as well as its organization are highlighted.

In Chapter 2, a novel multi-mode stacked-switch inverter/rectifier leg for the use in bidirectional DC/DC power conversion is proposed. The overall bidirectional converter utilizes the proposed leg in both the inverter as well as the rectifier blocks. In addition, a *CLLC* resonant circuit is utilized to provide soft-switching for all of the semiconductor devices and to boost the voltage level at the output of the converter. The analysis and the design process of the overall converter along with the component selection of the resonant tank are provided in this chapter. In order to regulate the output voltage in the proposed converter, a variable frequency modulation control is developed and implemented. The feasibility of the proposed converter is then verified through the simulation results and experimental works on the proof-of-concept prototypes.

In Chapter 3, fault incidents in power electronic converters are investigated and a novel open-circuit fault-tolerant control technique is proposed through the built-in circuit redundancy operation of the presented multi-mode stacked-switch rectifier leg. The proposed fault-tolerant technique enables post-fault operation of the converter to continue to deliver the demanded load power with soft-switching operation in case any switch in the rectifying side experiences an open-circuit fault. Then, an open-circuit fault is investigated in the inverter side and consequently, in order to address it, a modified topology of the multi-mode stacked-switch leg is presented. The added switching redundancy provides an open-circuit fault-tolerant operation for both the inverter and rectifier blocks while improving the efficiency through synchronous rectification. To highlight the merits of the proposed fault-tolerant control in the multi-mode stacked-switch leg, simulation and experimental results are provided.

In Chapter 4, the voltage distribution over the input/output capacitors, the performance of the converter for a wide gain range along the efficiency in different loading conditions in the proposed multi-mode stacked-switch converter are discussed and a comprehensive control system is proposed to address all of the above-mentioned challenges. The presented control enables the converter to regulate the output voltage for a wide gain range for various loading conditions within a narrow switching frequency range by utilizing the built-in circuit redundancy of the converter. In addition, it allows the voltage stress over the DC-link capacitors to be equally distributed. The proposed converter is capable of achieving soft-switching operation for all semiconductor devices. Simulation and experimental results are given to highlight the merits of the proposed comprehensive control system.

In Chapter 5, the contributions of this thesis are summarized and some future works are suggested to improve the performance of the proposed converter with the developed comprehensive control system.

Chapter 2. Proposed Multi-Mode Stacked-Switch Inverter/Rectifier Leg for Bidirectional DC/DC Power Conversion

This chapter focuses on the development of a new bidirectional DC/DC converter topology that addresses the drawbacks of the conventional converters discussed in Chapter 1, which include: limited soft-switching operation, high voltage stress over the semiconductor devices, unbalanced voltage distribution over capacitors, loss distribution over the switches, etc.

In the first part of this chapter, a novel multi-mode stacked-switch inverter/rectifier leg is proposed that is capable of operating in rectifying mode with a much lower voltage ripple compared to the standard 4-switch string rectifier circuit with the same capacitive ;filter. Then, a new bidirectional DC/DC converter topology employing a *CLLC* resonant tank and the multi-mode stacked-switch leg in both inverter and rectifier block is presented and investigated.

In the second part of this chapter, the design equations, loss analysis of the circuit, and operation of the overall converter along with the analysis on achieving soft-switching conditions of the circuit are provided. In the final section, the simulation and experimental results are provided to highlight the merits of the proposed converter.

2.1. The Proposed Multi-Mode Stacked-Switch Inverter/Rectifier Leg

As discussed in Chapter 1, the 4-switch string-structured bidirectional converter shown in Figure 2.1 is among the popular topologies for the use in energy storage application as the voltage stress across each switch is reduced to half of the DC source voltage, making it a suitable choice for medium and high voltage applications [81], [82]; yet, in the case of being used in conjunction with a resonant circuit, the equivalent inductance at the output terminal of the resonant tank acts similar to a current source as demonstrated in Figure 2.2 [83]. As a result, in the rectifying mode, the circuit operates as a half-wave rectifier and only the positive current flows through the output capacitor while the negative current circulates in the resonant circuit, leading to a higher voltage ripple at the load where the frequency of the output current ripple equals the switching frequency. Figure 2.3 presents a multi-mode stacked-switch leg combining the features of a full-bridge and that of a 4-switch string-structured converter.

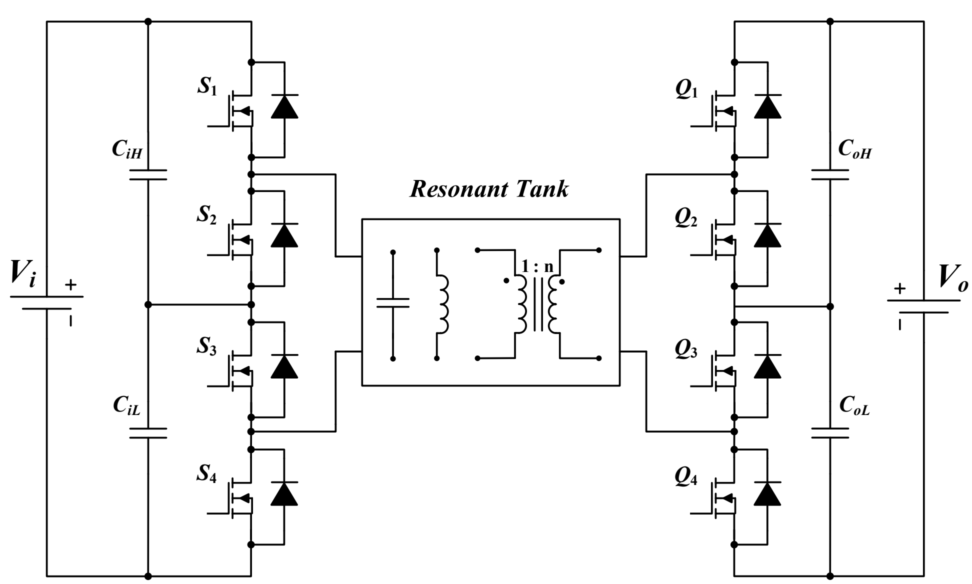


Figure 2.1- Topology of the 4-switch string-based bidirectional converter with a resonant circuit

The two middle switches in the proposed multi-mode stacked-switch leg are low frequency (negligible compared to the switching frequency) and the two extra diodes have been added to

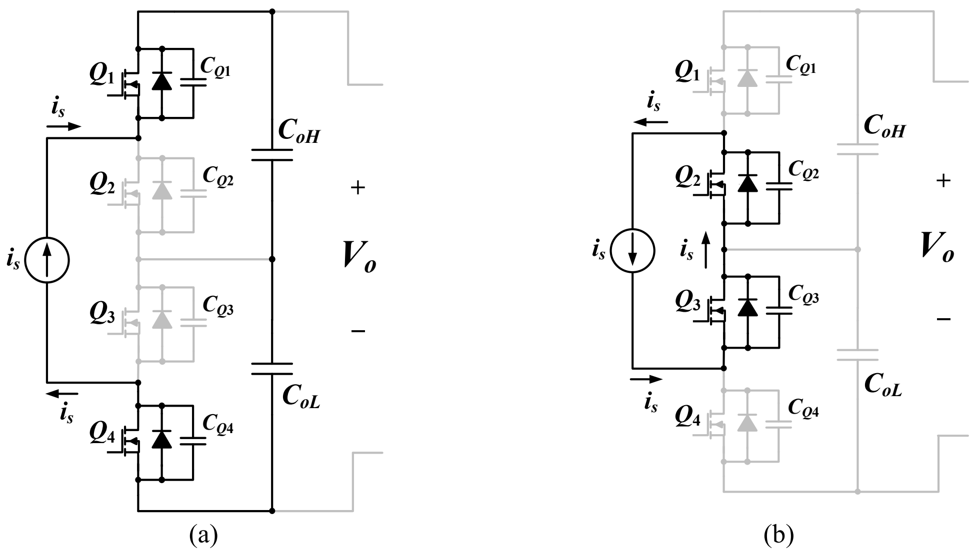


Figure 2.2- The current path in a 4-switch string rectifier a) positive i_s b) negative i_s

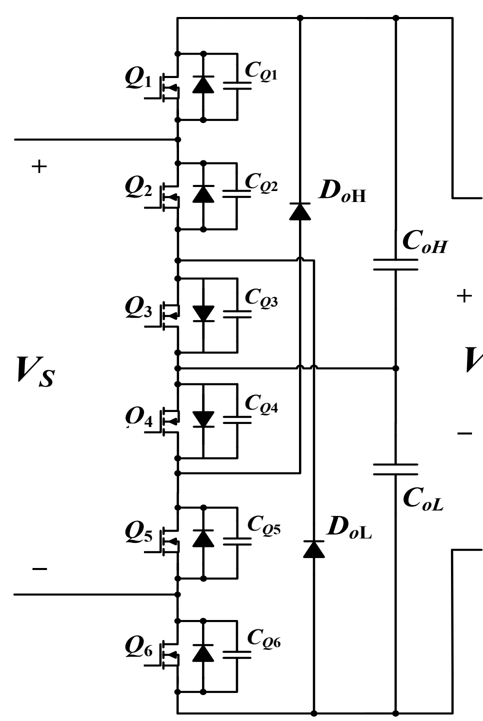


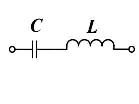
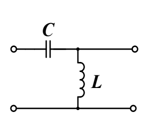
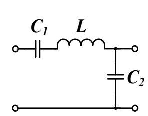
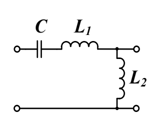
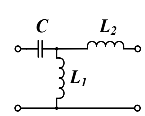
Figure 2.3- The topology of the proposed multi-mode stacked-switch

enable the leg to operate as a full-wave rectifier hence reducing the output ripples. The middle switches are turned ON in the inverting block and the generated voltage is unipolar.

2.2. Resonant Converters

In high power applications in particular, to improve the efficiency, reduce the converter size, and provide galvanic isolation, resonant tanks are often used to allow the converter to operate in higher frequencies while minimizing the switching losses. Also, resonant converters are utilized in order to achieve high voltage gain without using a high turns-ratio transformer. Many topologies have been presented in the literature. Table 2.1 summarizes the features of the most popular resonant topologies [6]. *LLC* and *LCC* are the most promising candidates in DC/DC applications. Yet, since the proposed multi-mode stacked-switch leg in Figure 2.3 generates a unipolar voltage at the terminals of the resonant tank, for bidirectional power

Table 2.1- Comparison of different resonant circuit topologies

	***LC* Series**	***LC* Parallel**	***LCC***	***LLC***	***CLL***
					
Frequency Variation	Wide	Wide	Narrow	Moderate	Moderate
Voltage/Current Stress	Lowest	High	Highest	Low	High
ZVS (on switch network)	✓	✓	✓	✓	✓
ZCS (on rectifier network)	✗	✗	✗	✓	✓

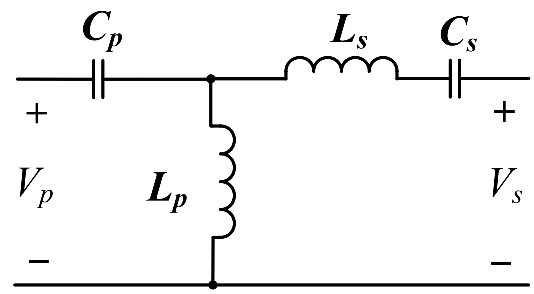


Figure 2.4- The topology of the *CLLC* resonant circuit

transfer, a capacitor is required in series at each terminal to block the *DC* component of the generated voltage. As a result, a *CLLC* resonant tank shown in Figure 2.4 is proposed and employed to allow bidirectional power transfer while providing soft-switching and stepping up/down the voltage level.

2.3. The Proposed Multi-Mode Stacked-Switch Bidirectional Converter Employing a *CLLC* Resonant Tank

Figure 2.5 shows the proposed bidirectional converter that employs a *CLLC* resonant tank and the multi-mode stacked-switch leg in both the inverting and rectifying blocks to reduce the voltage stress across the switches. In the proposed circuit, each inverter or rectifier leg consists of 4 high frequency (HF) switches and 2 low frequency (LF) switches. The two legs as shown in Figure 2.5 are then connected via an isolated *CLLC* resonant circuit. The proposed converter can operate in boost conversion mode (i.e. charging mode with V_i representing the DC-bus voltage, and V_o representing the battery voltage) or buck conversion mode (i.e. discharging mode). When leg 1 operates as an inverter, by turning ON the middle switches, the inverter generates a unipolar square wave voltage across the resonant tank. As mentioned earlier, in order to step up/down the voltage level and to provide zero voltage switching (ZVS) for the switches during turn-ON and turn-OFF, a *CLLC* resonant circuit is employed in the proposed converter. An integrated high-frequency transformer is utilized in the resonant circuit for offering galvanic isolation between the primary and secondary sides. Therefore, all the semiconductor devices in the proposed circuit achieve either ZVS or zero current switching (ZCS) operation.

The proposed converter shown in Figure 2.5 can also be used in a modular structure. In the modular converter, based on the application, each module can be connected in either

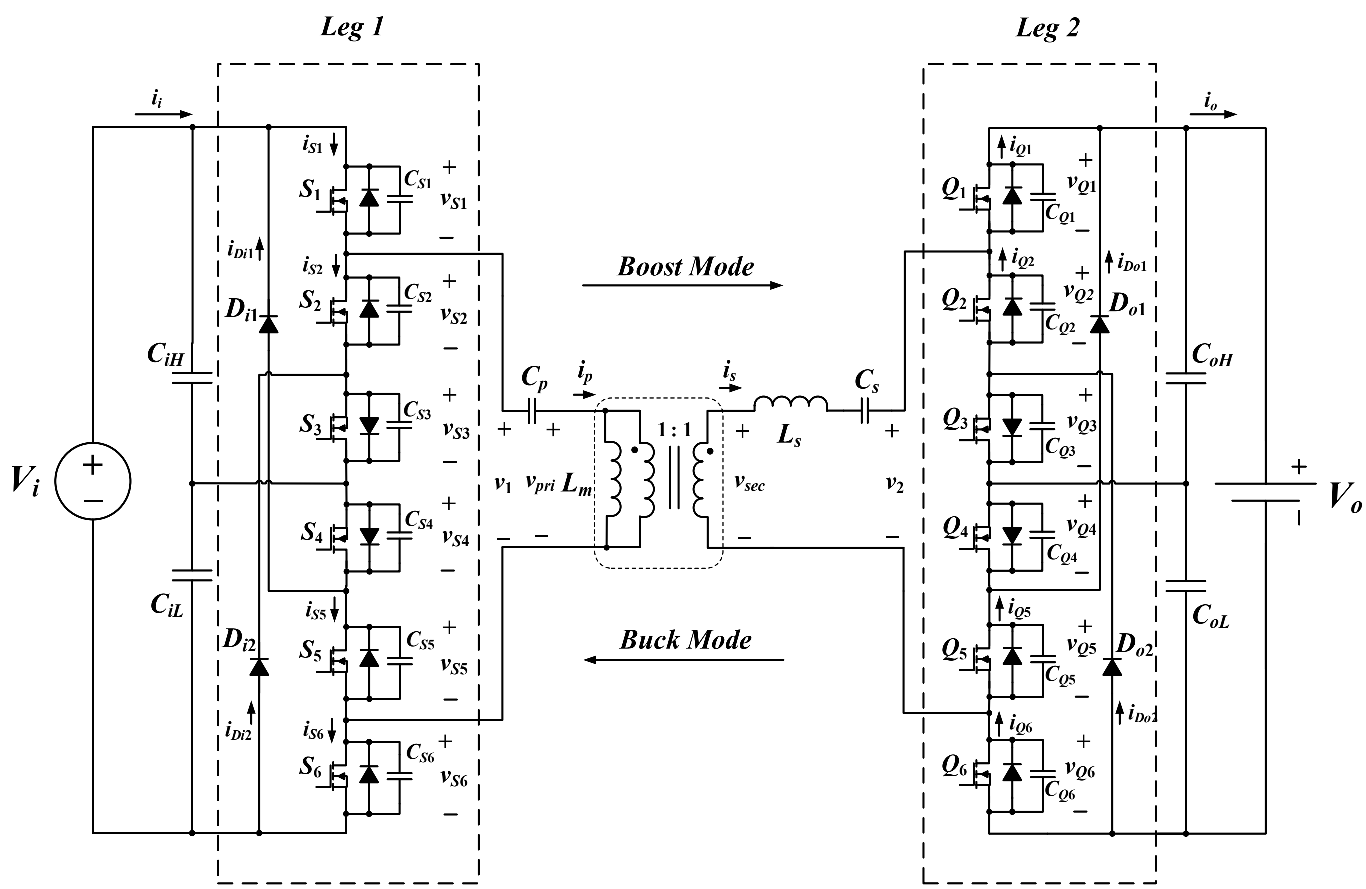


Figure 2.5- Topology of the bidirectional *CLLC* resonant converter employing the stacked-switch inverter/rectifier legs

parallel/cascaded inputs or parallel/cascaded outputs. A modular converter structure with the proposed circuit modules in parallel is shown in Figure 2.6. The proposed bidirectional multi-mode soft-switched converter with a *CLLC* resonant tank has the following features:

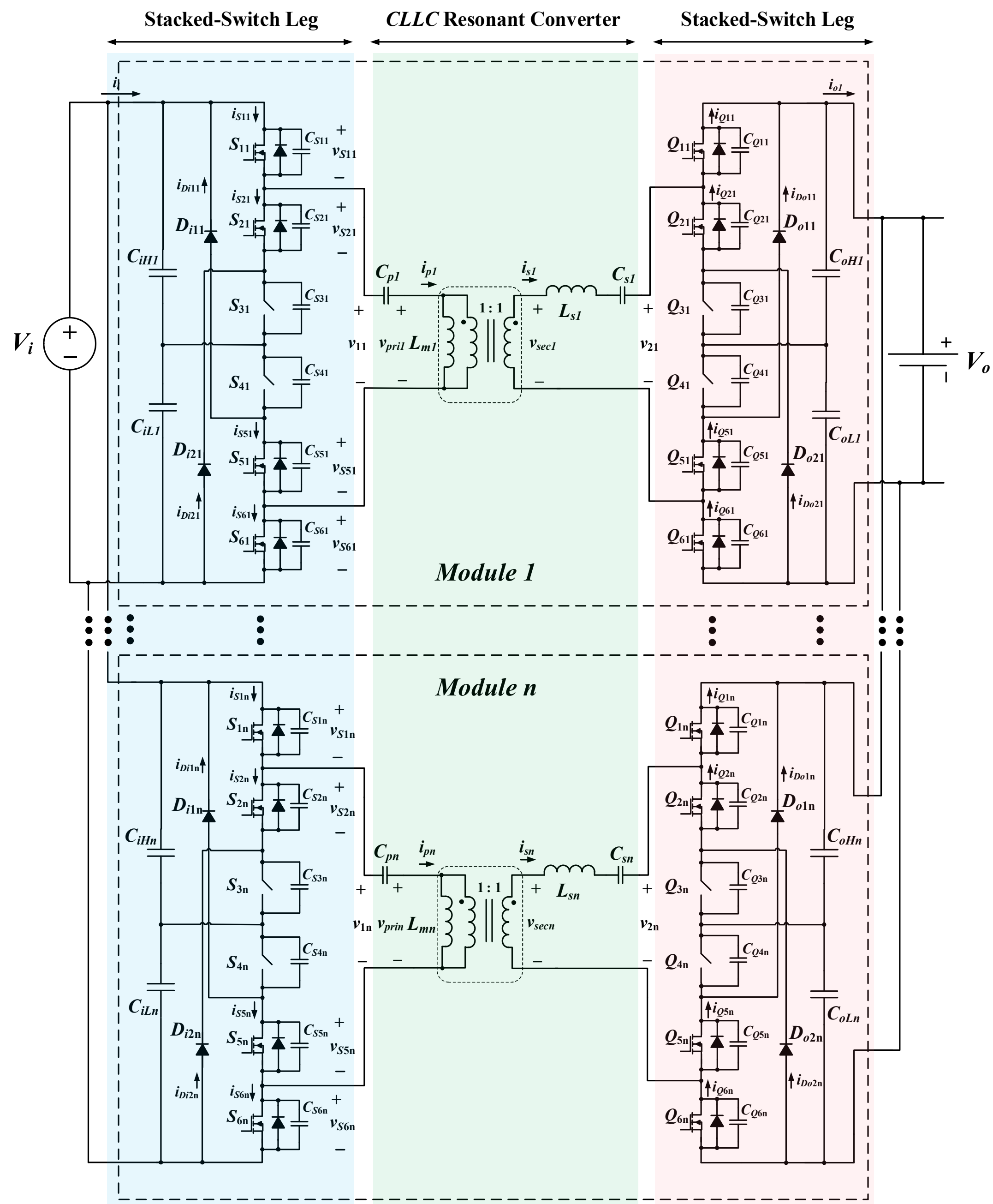
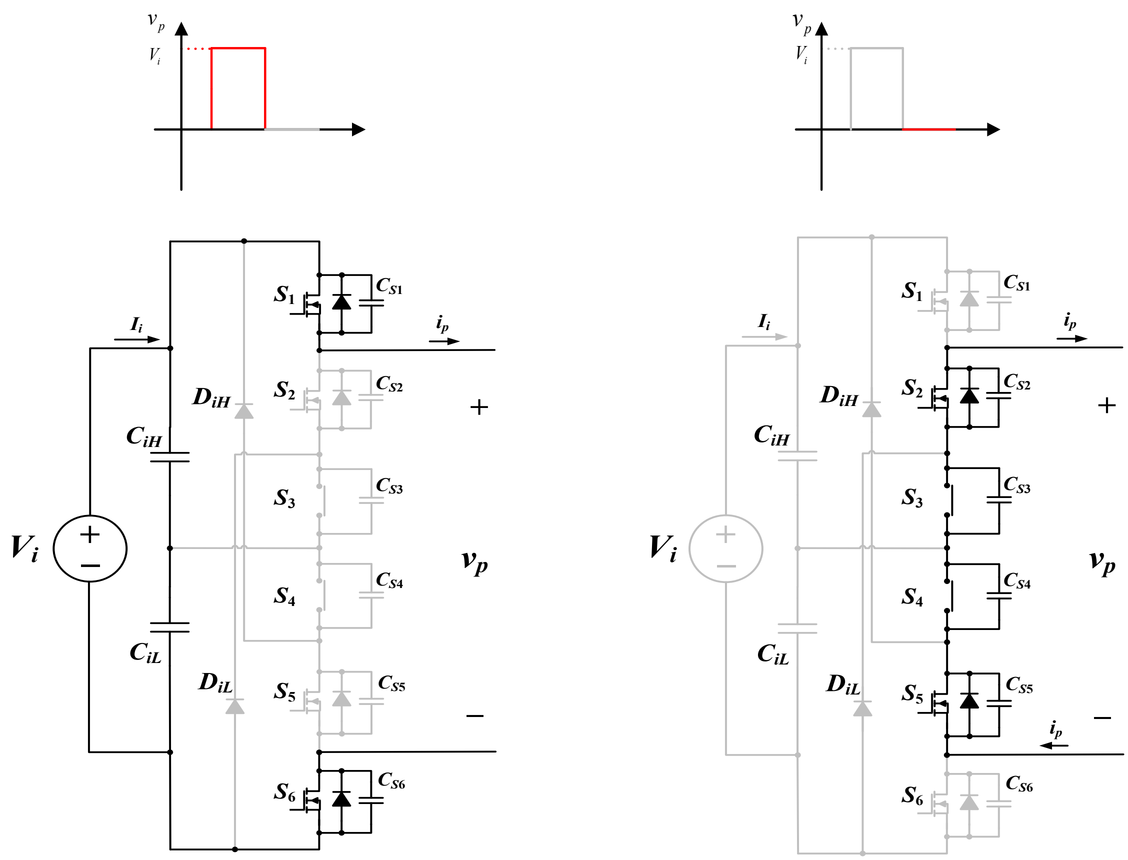


Figure 2.6- Modular converter structure with the proposed multi-mode stacked-switch converter module

1) The voltage across each switch in the inverting block equals half of the DC link
2) ZVS turn-ON and ZCS turn-OFF are achieved for all of the semiconductor switches.
3) The converter is able to step up/down the voltage level, without the need of using a high turn-ratio transformer.
4) The output voltage is regulated through the variable frequency control

2.3.1. Operation of the Proposed Multi-Mode Stacked-Switch Leg

The topology of the proposed multi-mode stacked-switch leg shown in Figure 2.3 consists of 6 switches (S_1 to S_6) where S_3 and S_4 are low-frequency switches, and S_1 and S_6 operate in a



State I: DT_S State II: $(1\text{-}D)T_S$

Figure 2.7- Operating states of the proposed multi-mode stacked-switch leg in inverting mode

complementary fashion with S_2 and S_5. As demonstrated in Figure 2.7, when S_3 and S_4 are ON, the proposed leg operates as a conventional 4-switch string structured inverter and a unipolar square wave voltage is generated across the resonant tank, resulting in voltage stress of half of the input voltage across each switch. In state I, S_1 and S_6 turn ON during the interval DT_S, while in state II switches S_2 and S_5 turn ON during the interval $(1\text{-}D)T_S$.

In the rectifier block, however, depending on the operating modes, Q_3 and Q_4 are either ON or OFF. The various operating modes of the stacked-switch rectifier leg are shown in Figure 2.8 to Figure 2.10. To simplify the analytical operation of the circuit, the resonant tank is replaced with a current source. The added semiconductor devices to the circuit, provide multiple options for i_s to circulate through the converter depending on the switching pattern.

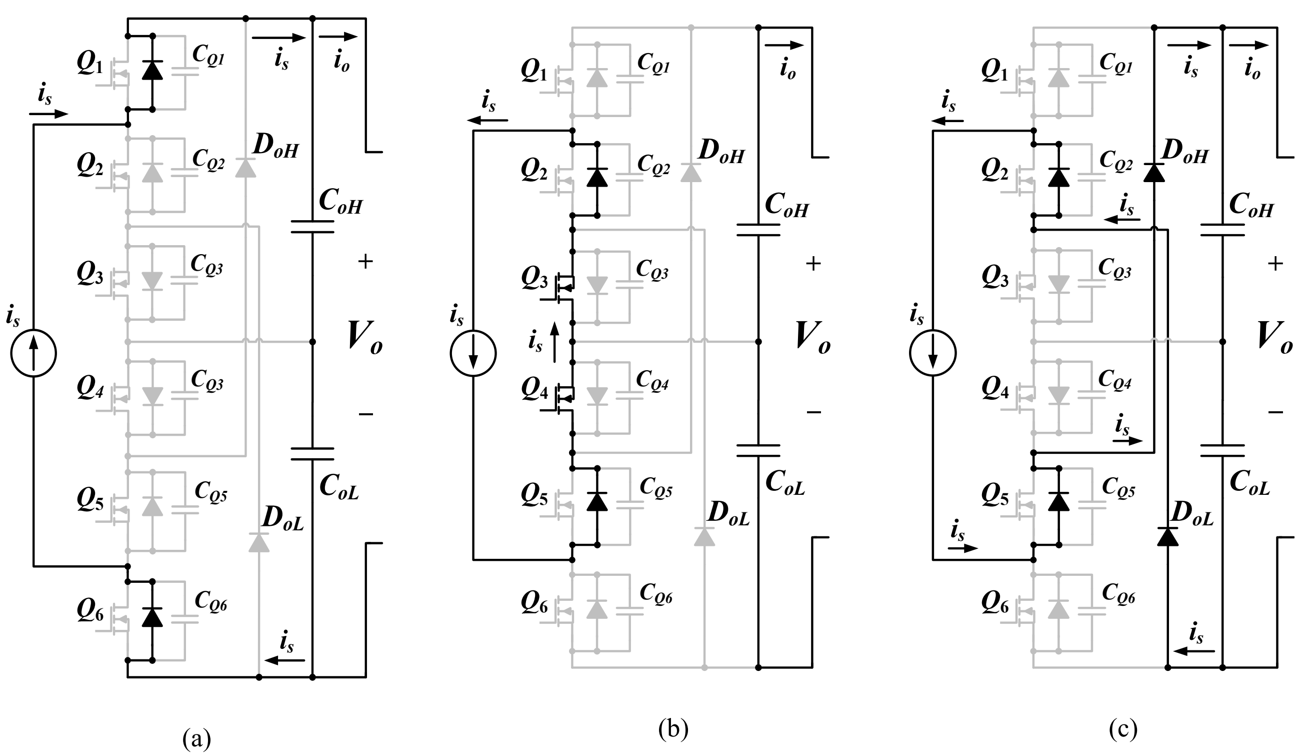
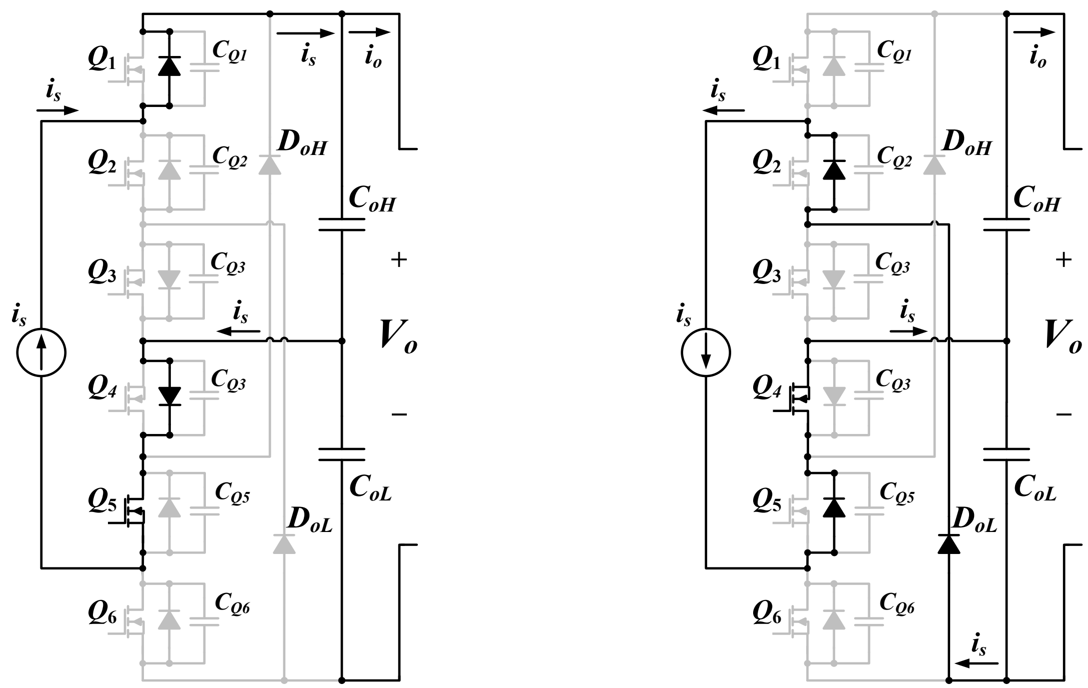
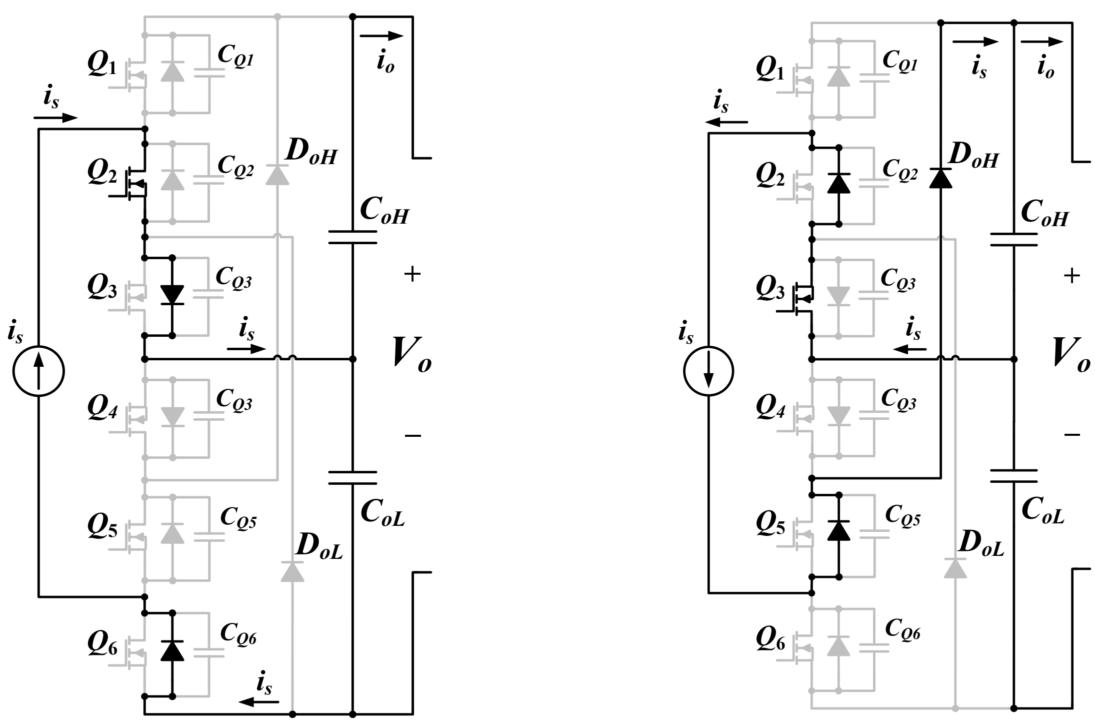


Figure 2.8- Operating modes of the multi-mode stacked-switch rectifier leg with: a) positive i_s, b) negative i_s (HW rectification), c) negative is (FW rectification)



(a) (b)

Figure 2.9- VD operation of the stacked-switch rectifier leg: a) positive i_s charging C_{oH}, b) negative i_s charging C_{oL}



(a) (b)

Figure 2.10- VD operation of the stacked-switch rectifier leg: a) positive i_s charging C_{oL}, b) negative i_s charging C_{oH}

By turning Q_3 and Q_4 ON at the same time shown in Figure 2.8 (a) and Figure 2.8 (b), the proposed circuit operates as a conventional 4-switch rectifier. In this case, the positive i_s passes through Q_1 and Q_6 charging both capacitors and the negative i_s closes its path through Q_3 and Q_4 shorting the secondary side acting as a half-wave rectifier (HW).

By switching Q_3 and Q_4 OFF simultaneously, while the path for the positive i_s remains the same, the negative i_s passes through Q_2, Q_5, D_{oH}, and D_{oL} and charges the output capacitors circulating through the load shown in Figure 2.8 (c) enabling the circuit to act as a full-wave (FW) rectifier leading to a reduced output voltage ripple.

In addition to the above switching patterns where the middle switches have the same state, Q_3 and Q_4 can be switched in a complementary fashion as well. By switching OFF Q_3 and turning Q_4 and Q_5 ON at the same time as shown in Figure 2.9, positive i_s closes its path through Q_1, Q_4, and Q_5 charging the top capacitor (C_{oH}) while the negative i_s circulates through the bottom capacitor (C_{oL}) by means of Q_2, Q_4, and Q_5. As a result, the positive and negative i_s charge C_{oH} and C_{oL} respectively allowing the circuit to operate as a voltage-doubler (VD).

Also, by switching OFF Q_4 and turning ON Q_2 and Q_3 instead, as demonstrated in Figure 2.10, the positive i_s passes through Q_2, Q_3, and Q_6 charging C_{oL}, while the negative i_s goes

Table 2.2- Switching patterns of the multi-mode stacked-switch rectifier leg during normal operation

Switching Pattern	**Switching patterns**						**Mode**
	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	
1	OFF	OFF	OFF	OFF	OFF	OFF	FW
2	OFF	OFF	ON	ON	OFF	OFF	HW
3	OFF	ON	ON	OFF	OFF	OFF	VD
4	OFF	OFF	OFF	ON	ON	OFF	VD

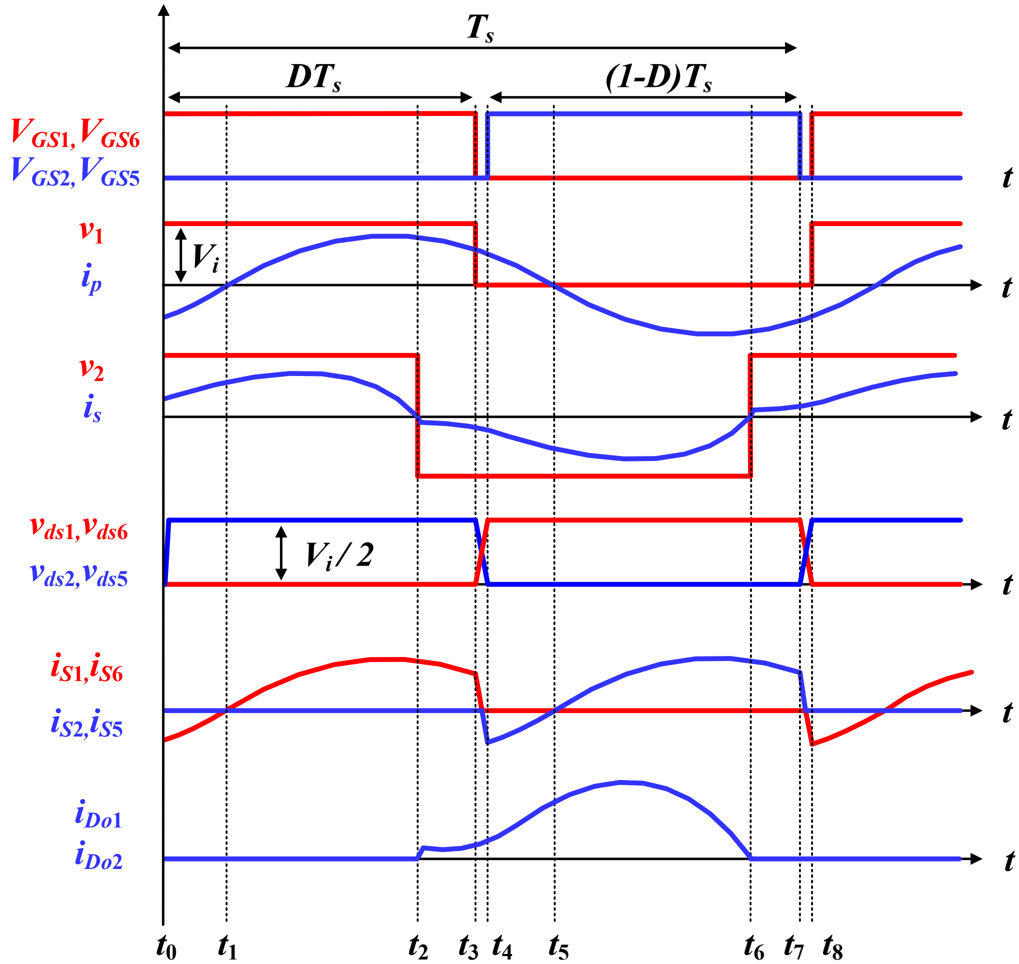


Figure 2.11- Key waveforms of the DC/DC portion in the proposed converter

through Q_2, Q_3, Q_5, and D_{oH} charging C_{oH}. In this mode, the positive and negative i_s charge C_{oL} and C_{oH} respectively. Table 2.2 summarizes different operating modes of the multi-mode stacked-switch rectifier leg during the normal operation of the circuit.

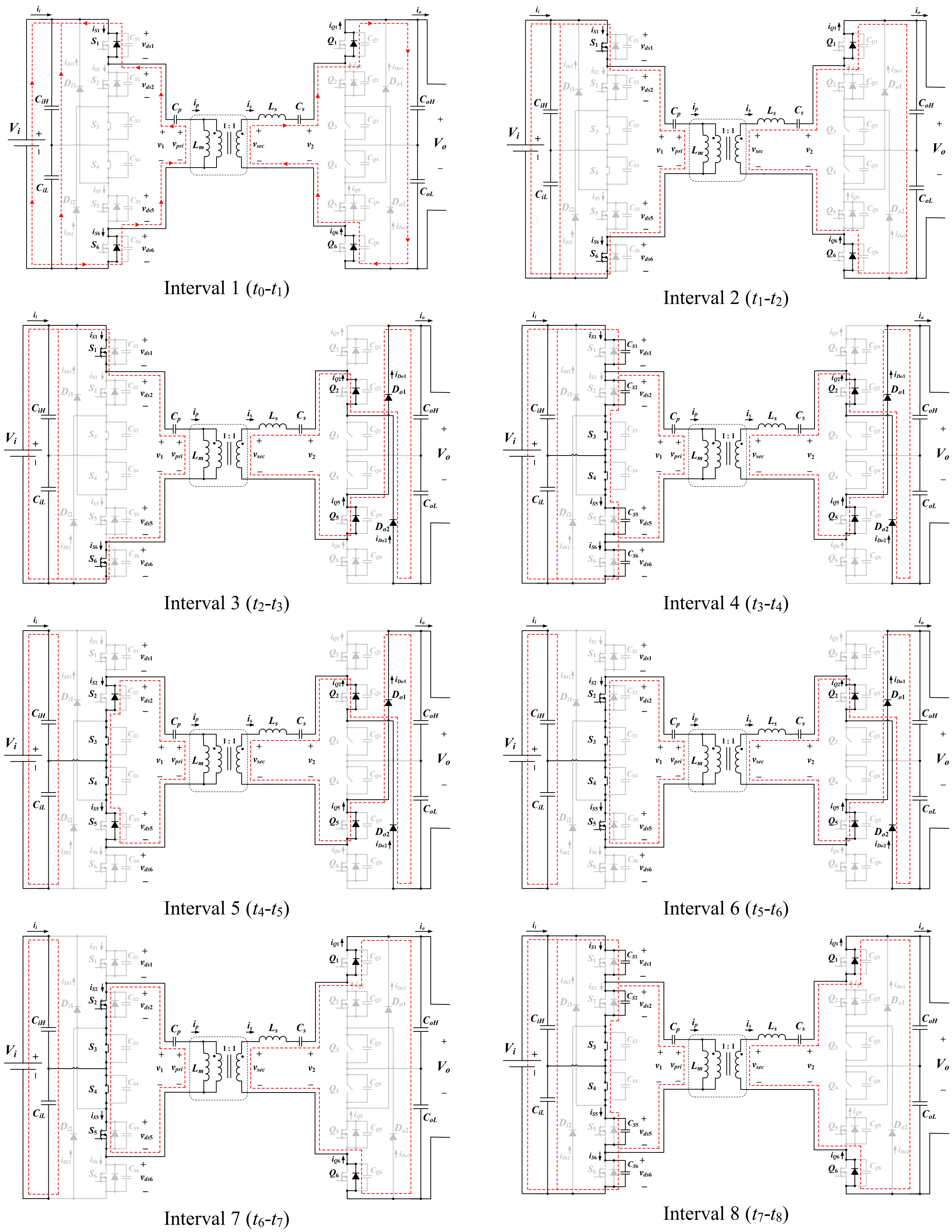


Figure 2.12- Operating stages of the proposed the proposed bidirectional multi-mode stacked-switch converter in full-wave mode

2.3.2. Converter Operating Principles

The key operating waveforms of the proposed bidirectional multi-mode stacked-switch converter in full-wave mode are demonstrated in Figure 2.11. Since the proposed circuit is bidirectional, only the operating principles of the boost operating mode are discussed below. The detailed operating states of the converter in each time interval along with the corresponding equivalent circuit have been provided in Figure 2.12.

As mentioned before, S_1 and S_6 are turned ON during the interval DT_S while S_2 and S_5 are turned ON during the interval $(1\text{-}D)T_S$. In the following analysis, the switches and diodes are assumed to be ideal components.

Interval 1 [$t_0<t<t_1$]:

At $t=t_0$, the gate signals are applied to S_1 and S_6 while S_2, S_5, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 are OFF and S_3 and S_4 are ON. The primary side resonant current (i_p) is negative and the current passes through the body diodes of S_1 and S_6 until it reaches zero. Meanwhile, the secondary side resonant current (i_s) is positive and the anti-parallel diodes of Q_1 and Q_6 conduct the current.

Interval 2 [$t_1\leq t<t_2$]:

In this interval, S_1, S_3, S_4, and S_6 are still ON while the rest of the switches are OFF. At $t=t_1$, i_p becomes positive and passes through S_1 and S_6. Hence, S_1 and S_6 turn ON under ZVS. At the same time, i_s is still positive passing through the body diodes of Q_1 and Q_6.

Interval 3 [$t_2 \leq t < t_3$]:

The gate signals remain unchanged in this interval, yet i_s becomes negative at $t=t_2$. At this point, Q_3 and Q_4 prevent v_2 from being short and allow the negative current to flow through D_{o1} and D_{o2} and the anti-parallel diodes of Q_2 and Q_5 charging C_{oH} and C_{oL}.

Interval 4 [$t_3 \leq t < t_4$]:

At $t=t_3$, the gate signals of S_1 and S_6 are removed. i_p is positive and flows through C_{S2} and C_{S5} discharging them while charging C_{S1} and C_{S6}. As a result, v_{ds1} and v_{ds6} rise slowly from zero, providing ZCS for S_1 and S_6. The flowing path for i_s remains unchanged.

Interval 5 [$t_4 \leq t < t_5$]:

At $t=t_4$, the gate signals of S_2 and S_5 are applied while S_1, S_6, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 are OFF and S_3 and S_4 are ON. i_p is positive and the current passes through the body diodes of S_2 and S_5 until it reaches zero. i_s is negative and passes through D_{o1} and D_{o2} and the anti-parallel diodes of Q_2 and Q_5.

Interval 6 [$t_5 \leq t < t_6$]:

In this interval, the gate signals remain unchanged. At $t=t_5$, i_p becomes negative and passes through S_2 and S_5 providing ZVS turn on. The current path for i_s remains unchanged.

Interval 7 [$t_6 \leq t < t_7$]:

S_2 and S_5 are still ON while S_1, S_6, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 are turned OFF. i_s becomes positive at $t=t_6$ and passes through the anti-parallel diodes of Q_1 and Q_6 charging C_{oH} and C_{oL}.

Interval 8 [$t_7 \leq t < t_8$]:

At $t=t_7$, the gate signals of S_2 and S_5 are removed. i_p is negative and flows through C_{S1} and C_{S6} discharging them while charging C_{S2} and C_{S5} making v_{ds2} and v_{ds5} rise slowly from zero, providing ZCS for S_2 and S_5.

2.3.3. Analysis of the Proposed Converter with *CLLC* Resonant Circuit

This section analyzes the characteristics of the employed *CLLC* resonant circuit and the converter's soft-switching operating condition. Fundamental harmonic analysis is used to analyze the circuit voltage gain in both boost mode and buck mode. In boost operating mode, as mentioned in the previous section, S_1 and S_6 turn ON during DT_s and operate in a complementary fashion with S_2 and S_5 turn ON in interval $(1-D)T_s$, where D is the duty ratio and T_s is the switching period. Unipolar square wave voltage v_I given by (2.1) is generated by the inverter and is applied to the primary of the resonant circuit, where θ_h is given by (2.2).

$$v_1 = V_i D + \sum_{h=1}^{\infty} \frac{\sqrt{2}V_i}{h\pi} \sqrt{(1-\cos 2h\pi D)} \sin(h\omega_{sw} t + \theta_h) \tag{2.1}$$

$$\theta_h = \tan^{-1}\left(\frac{\sin 2h\pi D}{1-\cos 2h\pi D}\right) \tag{2.2}$$

In the above equations, h is the harmonic order, ω_{sw} is the angular switching frequency and V_i is the input voltage. Since the capacitors in the resonant tank block the DC component, the voltage at the primary side of the resonant circuit (v_I) can be written as given by (2.3).

$$v_1 = \sum_{h=1}^{\infty} \frac{\sqrt{2}V_i}{h\pi} \sqrt{(1-\cos 2h\pi D)} \sin(h\omega_{sw} t + \theta_h) \tag{2.3}$$

2.3.3.1. Voltage Gain

Since the output voltage of the converter is regulated by varying the switching frequency, in order to maximize the voltage at the primary side of the resonant circuit, D is set to 50%. v_1 can then be expressed as given by (2.4). By ignoring the higher-order harmonics and only considering the fundamental frequency of the voltage at the primary of the resonant circuit, the RMS (Root Mean Square) value of v_1 ($V_{1(rms)}$) is given by (2.5):

$$v_1 = \sum_{h=odd}^{\infty} \frac{2V_i}{h\pi} \sin(h\omega_{sw} t) \tag{2.4}$$

$$V_{1(rms)} = \frac{\sqrt{2}V_i}{\pi} \tag{2.5}$$

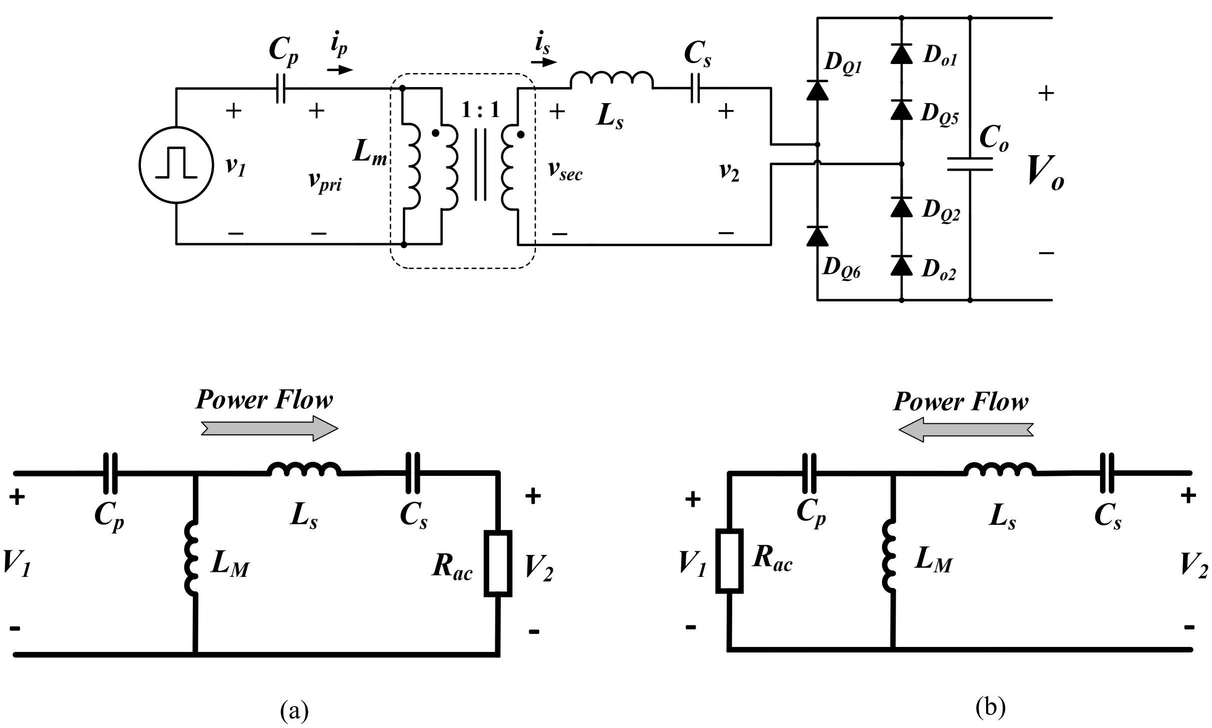


Figure 2.13- Fundamental equivalent circuit in a) boost mode b) buck mode

Figure 2.13 shows the fundamental harmonic equivalent resonant circuit. The *CLLC* resonant tank consists of L_M, L_s, C_p, and C_s where L_M represents the magnetizing inductance of the high-frequency transformer, C_p and C_s stand for the primary and secondary side capacitors respectively and L_s represents the secondary side inductance. In addition, $k=L_s/L_M$ is defined as the ratio between the secondary side and the magnetizing inductances and $m=C_s/C_p$ is the ratio between the secondary side and the primary side capacitances. The equivalent resistance R_{ac} (given in (2.6)) and the angular resonant frequency ω_0 (rad/s) of the resonant components (given in (2.8)) are chosen as the base values, where N_p and N_s are the number of turns in the primary and secondary of the high-frequency transformer respectively and R_L is the output equivalent resistance of the resonant circuit.

$$\mathrm{R}_{ac} = \frac{8}{\pi^2} \cdot \left(\frac{N_p}{N_s}\right)^2 \cdot R_L \tag{2.6}$$

Since the turn ratio of the high-frequency transformer is 1, the equivalent AC resistance R_{ac} can be expressed as given by (2.7), where ω_r is the normalized angular switching frequency and is given by (2.10) and Q represents the quality factor and is given by (2.9).

$$\mathrm{R}_{ac} = \frac{8}{\pi^2} \cdot R_L \tag{2.7}$$

$$\omega_0 = \frac{1}{\sqrt{L_M C_p}} \tag{2.8}$$

$$Q = \frac{\mathrm{R}_{ac}}{L_M \cdot \omega_0} = \mathrm{R}_{ac} \cdot C_p \cdot \omega_0 \tag{2.9}$$

$$\omega_r = \frac{\omega_{sw}}{\omega_0} \tag{2.10}$$

Considering the above assumptions and ignoring the higher-order harmonics, the voltage gain in the boost operating mode is given by (2.11).

$$\frac{V_2}{V_1}=\frac{\mathrm{R}_{ac}\cdot jL_M\omega_{sw}\cdot jC_p\omega_{sw}}{(\mathrm{R}_{ac}+jL_M\omega_{sw}+\frac{1}{jmC_p\omega_{sw}})\cdot jL_M\omega_{sw}\cdot jC_p\omega_{sw}+\mathrm{R}_{ac}+j(k+1)L_M\omega_{sw}+\frac{1}{jmC_p\omega_{sw}}} \tag{2.11}$$

Using (2.7) to (2.10), the voltage gain can be further simplified as shown in (2.12).

$$\frac{V_2}{V_1}=\frac{\omega_r^{\,2}}{(\omega_r^{\,2}-1)+j\frac{1}{Q}(k\omega_r^{\,3}-\frac{\omega_r}{m}-k\omega_r+\frac{1}{m\omega_r}-\omega_r)} \tag{2.12}$$

Using the same method, the voltage gain in the buck mode is obtained as given by (2.13).

$$\frac{V_1}{V_2}=\frac{j\omega_r}{\frac{1}{Q}(1+\frac{1}{m}-\frac{1}{m\omega_r^{\,2}}+k(1-\omega_r^{\,2}))+j(\omega_r-\frac{1}{m\omega_r}+k\omega_r)} \tag{2.13}$$

As can be seen in Figure 2.12, Q_3 and Q_4 and the diodes in the rectifying side allow the current to flow through the output capacitors for both positive and negative secondary side resonant current (i_s), allowing the rectifying circuit to operate as a full-wave rectifier. The gain of the rectifying stage is given by (2.14). Hence, the total voltage gain of the proposed converter in boost operating mode is given by (2.15).

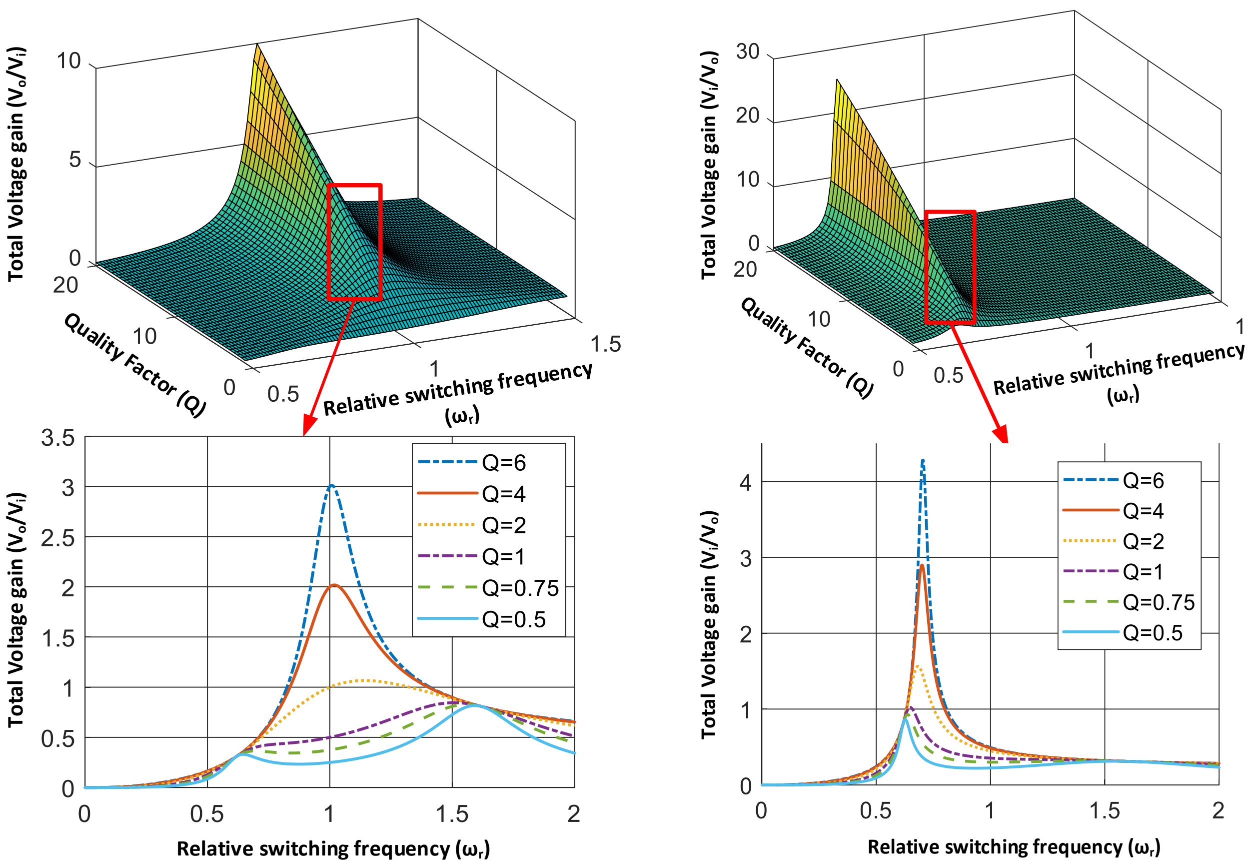
$$\frac{V_o}{V_2}=\frac{\pi}{2\sqrt{2}} \tag{2.14}$$

$$G_{disch}=\left|\frac{V_o}{V_2}\times\frac{V_2}{V_1}\times\frac{V_1}{V_i}\right|=\frac{\omega_r^{\,2}}{\sqrt{(\omega_r^{\,2}-1)^2+\frac{1}{Q^2}\times(k\omega_r^{\,3}-\frac{\omega_r}{m}-k\omega_r+\frac{1}{m\omega_r}-\omega_r)^2}} \tag{2.15}$$

Where V_o is the output voltage of the converter and V_2 is the voltage in the secondary side of the resonant circuit. Similarly, the total voltage gain of the proposed converter in buck operating mode is obtained as given by (2.16).

$$G_{ch} = \frac{1}{2} \times \frac{\omega_r}{\sqrt{\frac{1}{Q^2}(1+\frac{1}{m}-\frac{1}{m\omega_r^{\,2}}+k(1-\omega_r^{\,2}))^2+(\omega_r-\frac{1}{m\omega_r}+k\omega_r)^2}} \tag{2.16}$$

The voltage gain curves of the converter in both boost and buck modes are demonstrated in Figure 2.14 (a) and Figure 2.14 (b) respectively for k=1 and m=1.



(a) (b)

Figure 2.14- Voltage gain plot of the proposed converter for k=1, m=1 in a) boost mode b) buck mode

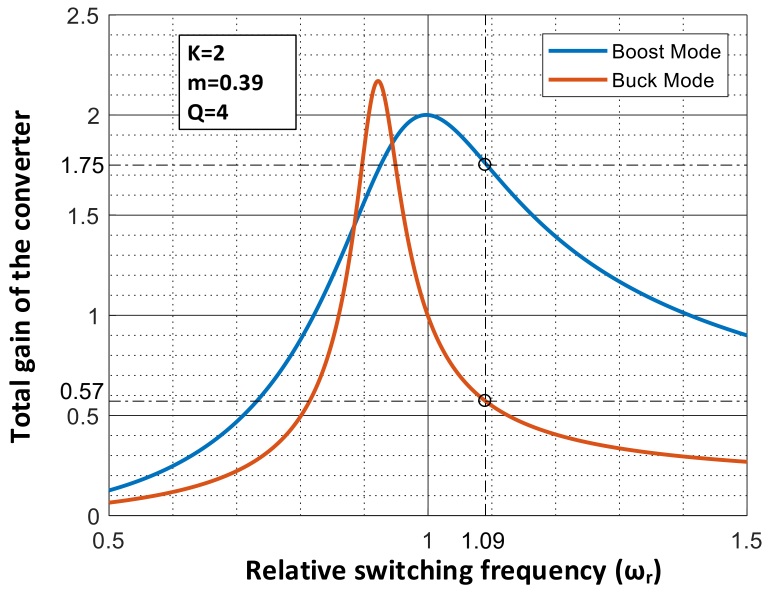


Figure 2.15- The voltage gain curves in the proposed converter

In energy storage applications, typically a two-stage converter is used to integrate the battery into the grid. In a single-phase battery charger, the voltage of the DC link varies from 400V to 1kV, and depending on the technology of the battery pack, the nominal voltage goes from 400V to 700V. In the case of using a Li-Ion battery technology, the voltage across a 400V battery pack goes from around 250V in fully discharged to 450V in fully charged. In a single-phase two-stage AC/DC converter, the DC-bus voltage V_{DC} must be higher than the peak magnitude of the line-to-line grid voltage $V_{gg,p}$ of a confidence factor C_f that accounts for the voltage drops across AC filter and the power switches inside the AC/DC block [71].

$$V_{DC} = C_f \cdot V_{gg,p} \tag{2.17}$$

By selecting a convenient confidence factor, generally, a DC-bus voltage of 700 V can be considered in the design of a single-phase battery charger. Consequently, in order to allow the converter to achieve the required specifications, a quality factor of 4 is selected in the design of the resonant circuit. Further, for a given quality factor, k and m can be adjusted to make the voltage gain of 700 V to 400 V happen for the same switching frequency in both buck and boost modes. Figure 2.15 demonstrates the voltage gain curve of the proposed DC/DC multi-mode stacked-switch converter for Q=4, k=2, and m=0.35.

2.3.3.2. Resonant Current Analysis

From (2.3), the primary side resonant current of the converter (i_p) is then obtained as given by (2.18), where $|Z_{i,h}|$ is the amplitude of the equivalent impedance of the hth harmonic and is given by (2.19), and $\varphi_{\mathrm{Zi,h}}$ represents the phase angle given by (2.20).

$$i_p = \sum_{h=1}^{\infty} \frac{\sqrt{2}V_i}{h\pi |Z_{i,h}|} \sqrt{(1-\cos 2h\pi D)} \sin(h\omega_{sw}t + \theta_h - \varphi_{Z_{i,h}}) \tag{2.18}$$

$$|Z_{i,h}| = R_{ac} \cdot \sqrt{\frac{(k+1+\frac{1}{m}(1-\frac{1}{h^2\omega_r^2}) - k\omega_r^2)^2 + (hQ\omega_r \cdot (1-\frac{1}{h\omega_r^2}))^2}{Q^4 + (hQ\omega_r \cdot (k+1-\frac{1}{mh\omega_r^2}))^2}} \tag{2.19}$$

$$\varphi_{Z_{i,h}} = \tan^{-1}\left(\frac{hQ\omega_r \cdot (1-\frac{1}{h\omega_r^2})}{k+1+\frac{1}{m}\cdot(1-\frac{1}{h^2\omega_r^2}) - k\omega_r^2}\right) - \tan^{-1}\left(\frac{h\omega_r \cdot (k+1-\frac{1}{mh\omega_r^2})}{Q}\right) \tag{2.20}$$

The peak value of the primary resonant current ($I_{p(max)}$) and the RMS value of the fundamental component of the primary resonant current ($I_{p(rms)}$) are then obtained as shown in (2.21) and (2.22) respectively.

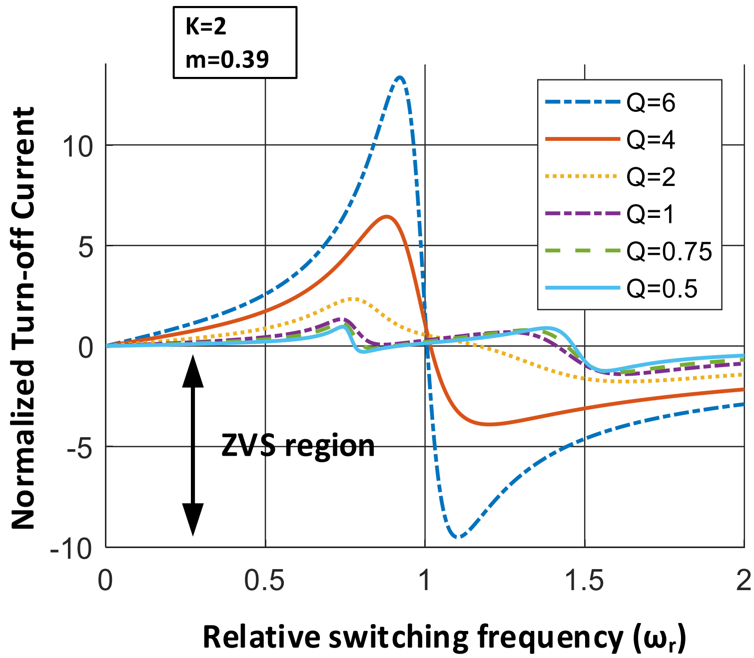


Figure 2.16- Normalized RMS value of the primary side resonant current at $t=t_0$ and D=0.5

$$I_{p(\max)}=\sum_{h=1}^{\infty}\frac{\sqrt{2}V_i}{h\pi\left|Z_{i,h}\right|}\sqrt{(1-\cos 2h\pi D)} \tag{2.21}$$

$$I_{p(rms)}=\frac{V_i}{\pi}\cdot\sum_{h=1}^{\infty}\sqrt{\frac{1-\cos 2h\pi D}{(h\left|Z_{i,h}\right|)^2}} \tag{2.22}$$

Further from (2.18), the per-unit fundamental component of the current in the primary of the resonant circuit for $t=t_0$ and $t=t_4$ is obtained in (2.23) and (2.24) respectively.

$$i_p(t_0)=\frac{\sqrt{2}}{\pi}\sqrt{(1-\cos 2h\pi D)}\sin(\theta_h-\varphi_{Zi,h}) \tag{2.23}$$

$$i_p(t_4)=\frac{\sqrt{2}}{\pi}\sqrt{(1-\cos 2h\pi D)}\sin(2\pi hD+\theta_h-\varphi_{Zi,h}) \tag{2.24}$$

As can be observed from Figure 2.11, in order to provide soft-switching for S_1 and S_6, i_p has to be negative at $t=t_0$. The curve of i_p for D=0.5 and different values for ω_r and Q are shown in Figure 2.16 along with the soft-switching area. Similarly, for S_2 and S_5 to turn on under ZVS, i_p has to be positive at $t=t_4$. With D=0.5, the soft-switching curve for S_2 and S_5 is the same and the current is mirrored with a negative sign. Considering the above assumptions and the specified operating point shown in Figure 2.15, soft-switching is realized for all of the switches in boost and buck operating mode.

2.3.3.3. Power Loss Analysis

The total power loss of the proposed DC/DC converter can be divided into SiC switch losses, diode losses, and losses in the resonant circuit.

I. Power Loss Analysis of the SiC MOSFETs

Power losses of a SiC switch mainly consist of steady-state conduction loss, switching loss and gate charge loss which are explained as follows:

a) Conduction Loss

The conduction loss of the switches in the proposed converter can be obtained by (2.25), where $R_{on(Si)}$ is the switch ON-resistance and the RMS current in the switches can be obtained from the resonant current i_p in (2.18).

$$P_{cond\_loss} = \sum_{n=1}^{6} I_{Si(rms)}^{2} R_{on(S_i)} \tag{2.25}$$

Since the harmonic components of the resonant current are negligible in loss calculations, i_p can be written as below.

$$i_p = \frac{\sqrt{2}V_i}{\pi|Z_i|}\sqrt{(1-\cos 2\pi D)}\,\sin(\omega_{sw}t + \theta - \varphi_{Z_i}) \tag{2.26}$$

Consequently, the RMS current passing through the SiC switches can be obtained as follows:

$$\begin{aligned} I_{S1} = I_{S6} &= \sqrt{\frac{1}{T_s}\int_{t_1}^{t_3}[i_p]^2\,dt} = \frac{V_i}{\pi|Z_i|}\sqrt{1-\cos(2\pi D)} \\ &\times\sqrt{D - \frac{t_1}{T_s} + \frac{\sin(2\omega_{sw}t_1 + 2\theta - 2\varphi_{Zi}) - \sin(4\pi D + 2\theta - 2\varphi_{Zi})}{4\pi}} \end{aligned} \tag{2.27}$$

The maximum RMS current passing through the switches can be calculated when t_1 approaches zero ($t_1 \rightarrow 0$) and consequently $\varphi_{Zin} \rightarrow 0$.

$$I_{S1(\max)} = I_{S6(\max)} = \frac{V_i}{\pi|Z_i|}\sqrt{(1-\cos(2\pi D))(D + \frac{\sin(2\theta) - \sin(4\pi D + 2\theta)}{4\pi})} \tag{2.28}$$

Similarly, the RMS current passing through S_2 and S_5 can be obtained by (2.29).

$$\begin{aligned} I_{S2} = I_{S5} &= \sqrt{\frac{1}{T_s}\int_{t_5}^{t_7}[i_p]^2\,dt} = \frac{V_i}{\pi|Z_i|}\sqrt{1-\cos(2\pi D)} \\ &\times\sqrt{1 - \frac{t_5}{T_s} + \frac{\sin(2\omega_{sw}t_5 + 2\theta - 2\varphi_{Zi}) - \sin(2\omega_{sw}T_s + 2\theta - 2\varphi_{Zi})}{4\pi}} \end{aligned} \tag{2.29}$$

The maximum current of S_2 and S_5 is given by (2.30).

$$I_{S2(\max)} = I_{S5(\max)} = \frac{V_i}{\pi |Z_i|}\sqrt{(1-\cos(2\pi D))(1-D+\frac{\sin(4\pi D+2\theta)-\sin(2\theta)}{4\pi})} \qquad (2.30)$$

b) Switching Loss

According to the waveforms shown in Figure 2.11, the switching losses of the SiC switches can be expressed by (2.31), where t_r is the switch rise time, t_f represents the switch fall time, t_{d_on} is the turn-on delay time, t_{d_off} represents the turn-off delay time and f_s is the switching frequency.

$$P_{sw\_loss} = \sum_{i=1}^{6}\left[\frac{1}{2}V_S(t_{on})\cdot I_S(t_{on})\cdot(t_r+t_{d\_on})\cdot f_s+\frac{1}{2}V_S(t_{off})\cdot I_S(t_{off})\cdot(t_f+t_{d\_off})\cdot f_s\right] \qquad (2.31)$$

Yet, considering the ZVS turn-ON and the ZCS turn-OFF and the fact that *CLLC* resonant converter is utilized to provide soft-switching, the switching losses are negligible.

c) Gate Charge Loss

Gate charge loss is the power that dissipates charging the switch gate and can be calculated by (2.32), where Q_g represents the gate electric charge, C_g is the gate capacitance and V_g is the gate-source voltage.

$$P_{G\_loss} = \sum_{i=1}^{6} Q_G \cdot V_G \cdot f_{sw} = \sum_{i=1}^{6} C_G \cdot V_G^2 \cdot f_{sw} \qquad (2.32)$$

II. Power Loss Analysis of the Diodes

Conduction Loss of the diodes is divided into conduction loss and switching loss. Due to the near-zero ZCS turn-ON and turn-OFF of the body diodes of the switches and the added diodes, the switching loss of the diodes can be ignored. As a result, only conduction loss is contributed to the diode loss as follows.

$$P_{G\_loss} = \sum_{i=1}^{4} R_{Di} \cdot I_{Di\_ave}^{2} \tag{2.33}$$

In (2.33), R_{Di} represents the on-state resistance of the diodes.

III. Power Loss Analysis of the High-Frequency Transformer and Inductor

The loss associated with the high-frequency transformer and inductor is divided into conduction loss and core loss. The inductor conduction loss in the secondary side of the resonant circuit can be expressed by (2.34), where R_{LDC} is the DC resistance of the inductor winding and $I_{s(rms)}$ represents the RMS value of the current in the secondary side of the resonant tank.

$$P_{ind\_cond} = R_{LDC} \cdot I_{s(rms)}^{2} \tag{2.34}$$

The conduction loss associated with the high-frequency transformer is calculated by (2.35), where R_{PDC} and R_{SDC} represent the DC resistance of the primary and secondary windings of the high-frequency transformer respectively.

$$P_{TR\_cond} = R_{PDC} \cdot I_{p(rms)}^{2} + R_{SDC} \cdot I_{s(rms)}^{2} \tag{2.35}$$

The core losses of the transformer and the inductor can be obtained by (2.36), where k, α, and β are constants and ΔB is the peak AC flux density expressed by (2.37), where N is the number of turns and A_e is the core window area.

$$P_{core} = k \cdot \Delta B^{\alpha} \cdot f_{sw}^{\beta} \tag{2.36}$$

$$\Delta B = \frac{V_{in} DT}{4NA_e} \tag{2.37}$$

2.3.3.4. Control Principles and Voltage Balancing Technique

The block diagram of the control system is demonstrated in Figure 2.17. The output voltage of the converter can be controlled through the variable frequency method or the duty ratio control using the pulse-width modulation technique (PWM). In this chapter, the variable frequency control technique has been utilized to regulate the output voltage. Considering the voltage gain curve of the resonant converter in terms of normalized angular switching frequency (ω_r) shown in Figure 2.14, in order to make sure that the converter operates within the ZVS region, the switching frequency has to be kept above the resonant frequency. Furthermore, as can be seen in Figure 2.15, considering the relationship between the overall gain of the converter and ω_r, for the frequencies greater than the resonant frequency, as the switching frequency increases, the gain decreases, and vice versa. Therefore, in the control system, first, the output voltage of the converter is sensed and is compared with the desired value. Then, the difference

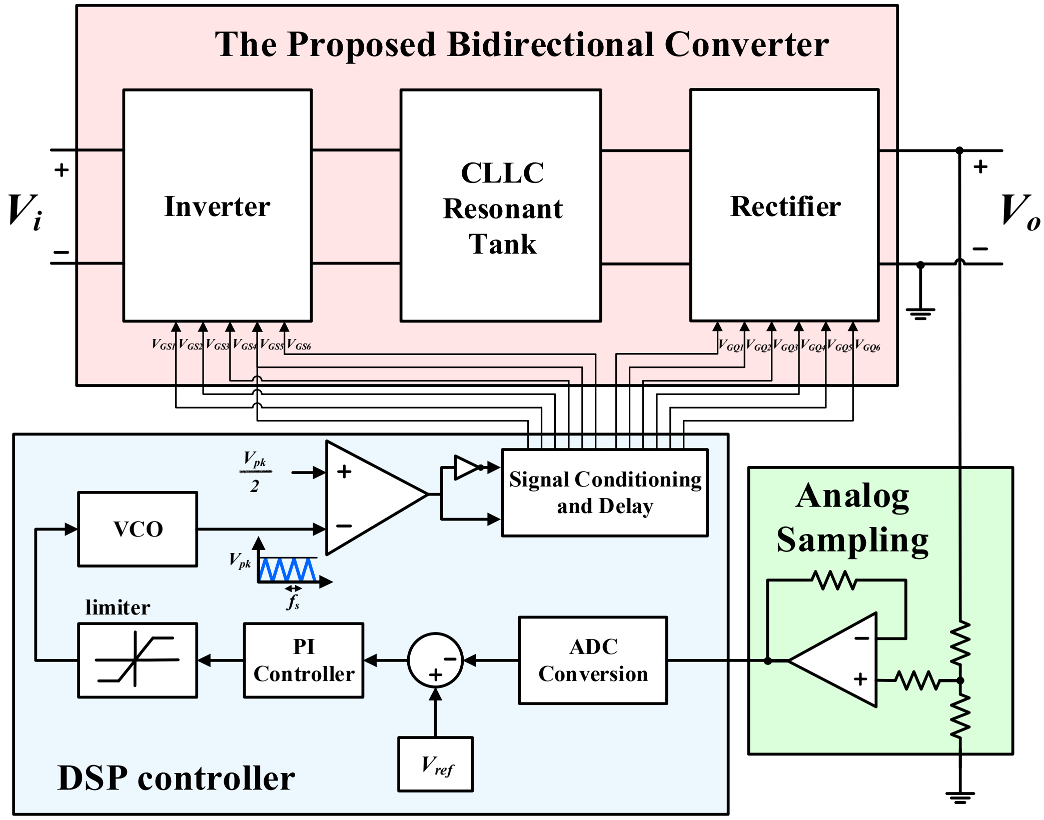


Figure 2.17- Block diagram of the variable frequency closed-loop system

(error) is fed into a PI controller. The output of the PI controller determines whether the switching frequency has to be increased or reduced to regulate the output voltage. In addition, in order to avoid operating at frequencies below resonance, a limiter is added to the control system to set a lower limit to the operating frequency and to ensure that the converter operates within the ZVS region.

2.4. Simulation Results

To demonstrate the performance of the proposed converter, a 400VDC to 700VDC 1 kW bidirectional multi-mode stacked-switch converter with a *CLLC* resonant tank is simulated in PSIM. PSIM is an electronic circuit simulation software, designed specifically for use in power electronics simulations which uses nodal analysis and the trapezoidal rule integration as the basis of its simulation algorithm. The proposed converter has been designed in PSIM's schematic capture interface and the simulation results were captured through Simview waveform viewer. In the analysis of the proposed converter in PSIM, no calibration, uncertainty or sensitivity analysis is required. The base switching frequency of the converter is selected to be 100 kHz to minimize the size of the converter and the components. Considering the aforementioned assumptions, the resonant circuit components are obtained as shown by (2.38) to (2.43).

$$R_L = \frac{V_o^2}{P_o} = \frac{700^2}{1000} = 490\Omega \tag{2.38}$$

$$R_{ac} = \frac{8}{\pi^2} \cdot R_L = 397.18\Omega \tag{2.39}$$

$$L_M = \frac{\mathrm{R}_{ac}}{Q \cdot 2\pi f_0} = 158\mu H \tag{2.40}$$

$$L_s = k \cdot L_M = 316.07\mu H \tag{2.41}$$

$$C_p = \frac{1}{L_M \omega_0^2} = 16.03nF \tag{2.42}$$

$$C_s = mC_p = 6.25nF \tag{2.43}$$

The simulation waveforms in boost mode are demonstrated in Figure 2.18 for D=0.5. L_M, L_s, C_p, and C_s are 158µH, 316.07µH, 16.03nF, and 6.25nF respectively. Figure 2.19 compares the output voltage ripple in the conventional 4-switch converter and the proposed multi-mode stacked-switch converter in boost and buck operating modes respectively. The switching frequency of the converter is 107 kHz in boost mode. In this mode, S_3 and S_4 are turned ON and Q_3 and Q_4 are turned OFF. As a result, the power is delivered to the load for both negative and

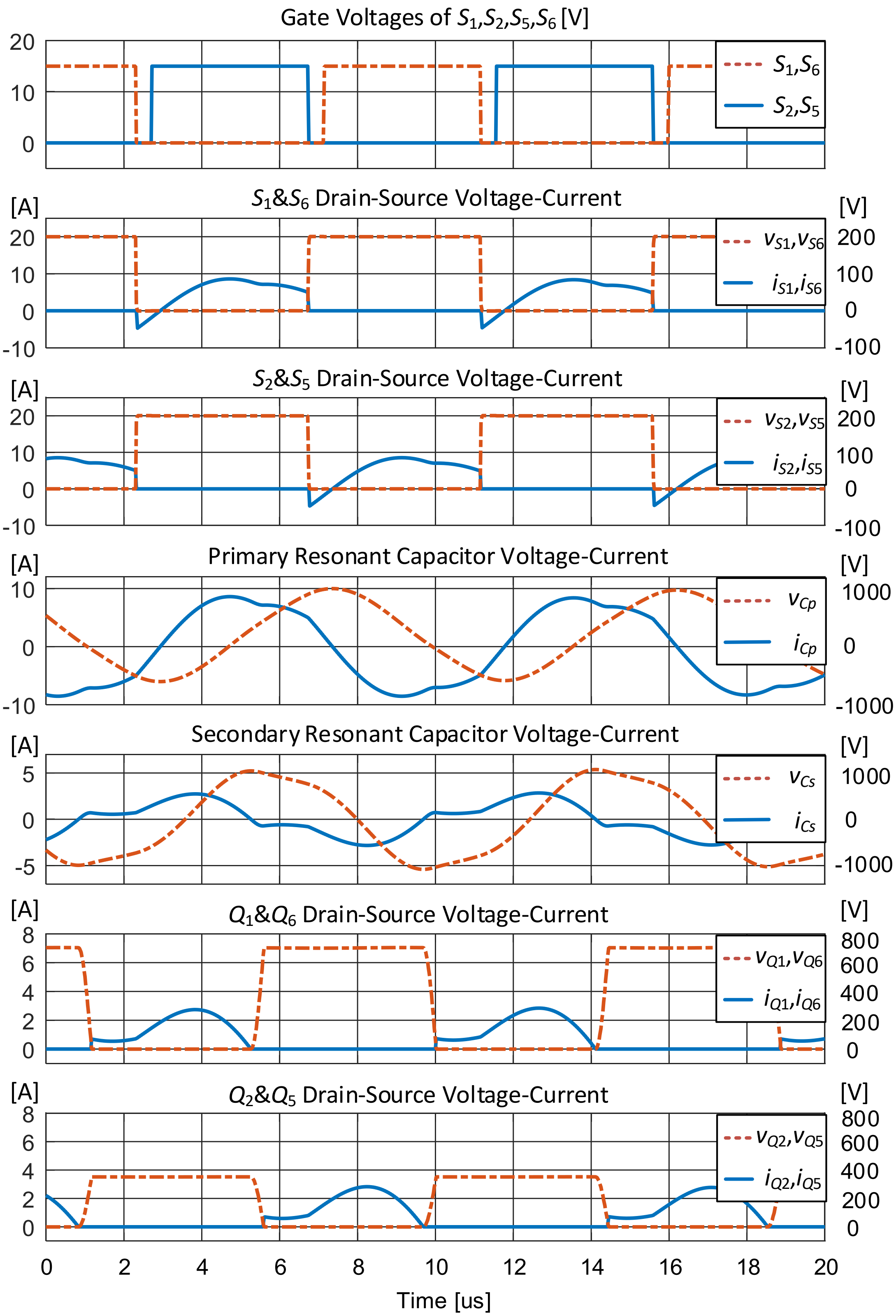


Figure 2.18- Simulation waveforms of the bidirectional multi-mode stacked-switch converter in boost operating mode

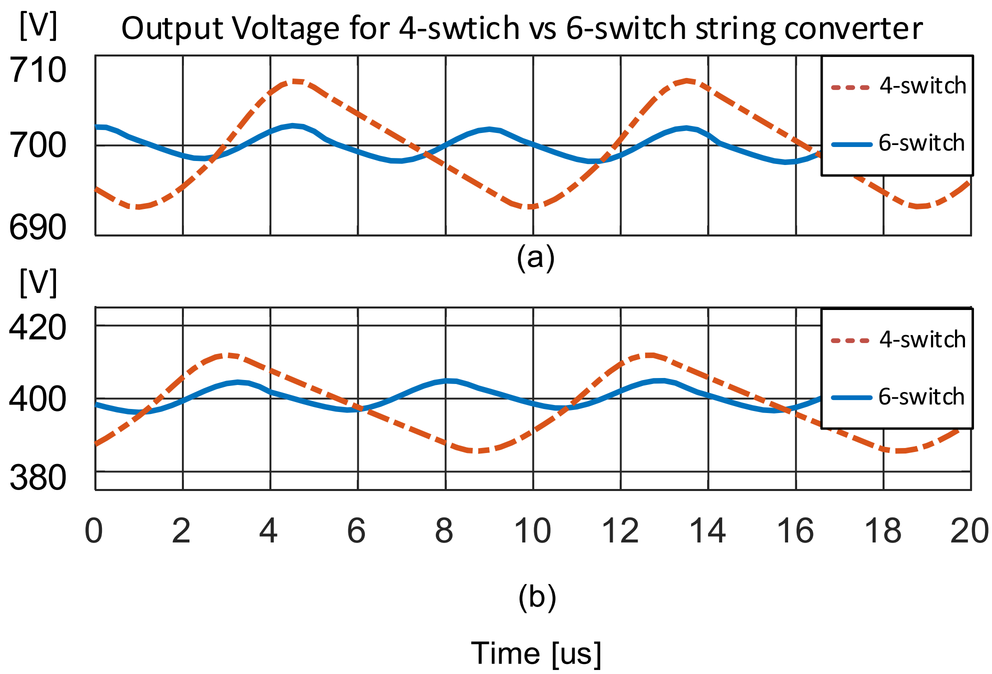


Figure 2.19- Output Voltage for 4-swtich vs multi-mode stacked-switch converter in a) boost operating mode, (b) buck operating mode

positive secondary-side resonant current and hence, the output ripple frequency is increased from 100 kHz to 200 kHz. The simulation results agree with the theoretical analysis. As expected and described in Figure 2.8, by switching from HW to FW mode, the frequency of the output ripple has been increased and the oscillations have been reduced by more than 50%.

2.5. Experimental Results

To further verify the performance of the proposed multi-mode stacked-switch converter, a 1 kW proof-of-concept prototype shown in Figure 2.20 and Figure 2.21 is designed to verify the operation of the proposed circuit. The component parameters used in the experiments are given in Table 2.3. InfiniiVision MSOX6004A oscilloscope by Keysight Technologies was used to capture the experimental waveforms and measure the efficiencies.

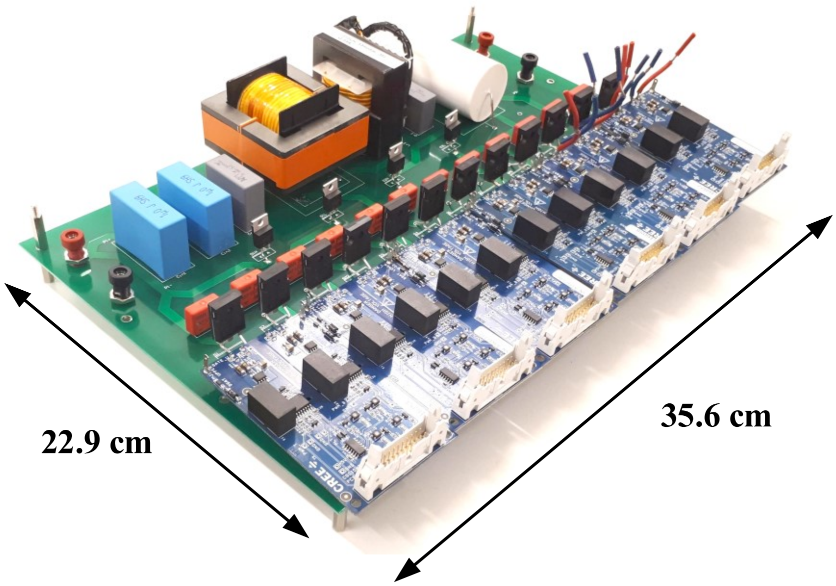


Figure 2.20- The proof-of-concept prototype in laboratory

Figure 2.21- The proof-of-concept prototype hardware set-up in laboratory

Table 2.3- Design Specifications & Circuit Parameters

Output Power (P_o)	1 kW
Output Voltage (V_o)	700 V
Input Voltage (V_i)	400 V
Magnetizing inductance (L_M)	160 µH
Secondary side resonant inductance (L_s)	320 µH
Primary side resonant capacitance (C_p)	15 nF
Secondary side resonant capacitance (C_s)	5.8 nF
Switching Frequency (f_s)	>100 kHz
Switches	SiC SCT3080KL
Added Diodes	U1560 Ultrafast Diode
Primary side snubber caps	330 pF
Secondary side snubber caps	150 pF

Figure 2.22 demonstrates the voltage and current of the primary and secondary sides of the resonant circuit in boost operating mode. Figure 2.23 shows the drain-source voltage and current of the inverting side switches. As can be seen, the voltage stress over the switches is half of the DC-link voltage. ZVS turn-on is provided for all the switches in the inverting block.

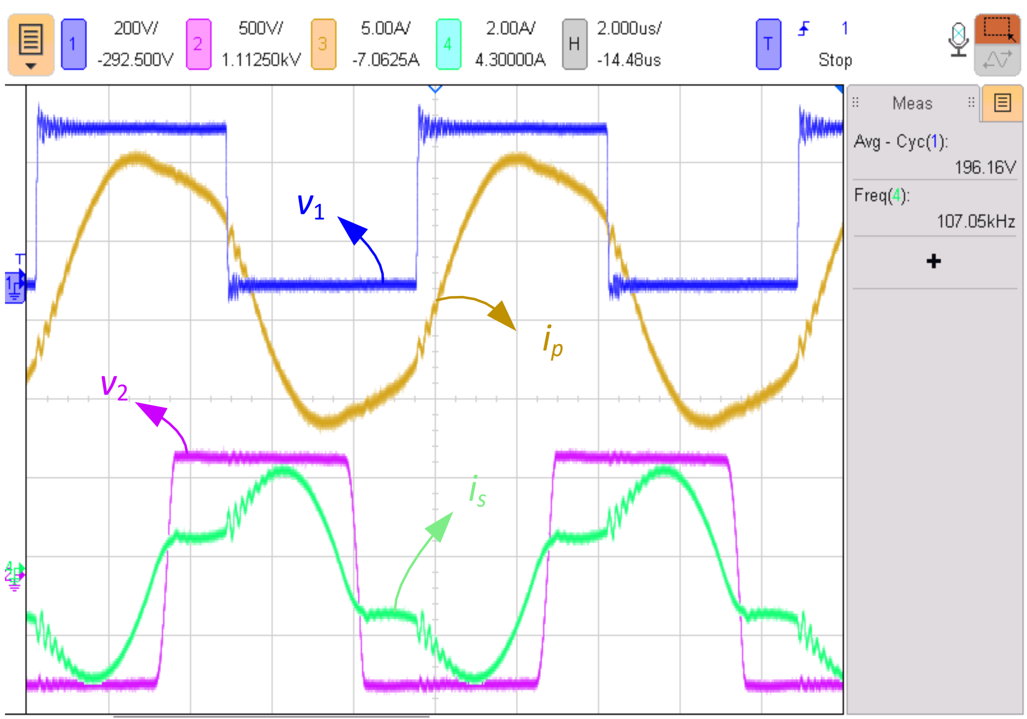
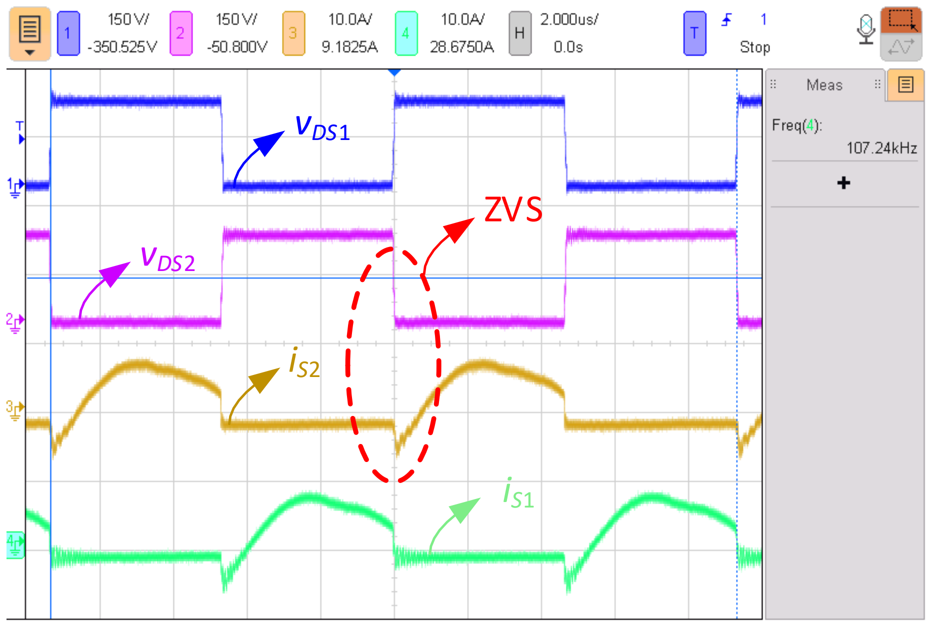


Figure 2.22- Experimental waveforms of the converter in boost mode. Voltage and current at the primary and secondary side of the resonant converter

In the experiment prototype, a snubber capacitor of 330pF is added across each switch to provide ZCS turn-off for the primary side switches. The output voltage along the secondary-side resonant current is demonstrated in Figure 2.24. The positive current passing through the



(a)

(b)

Figure 2.23- Experimental waveforms of the converter in boost mode (a) Drain–source voltage and current of S_1 and S_2 for two switching periods (b) Zoomed-in snapshot.

body diodes of Q_1 and Q_6 is identical to the negative current passing through D_{o1} and D_{o2} and the anti-parallel diodes of Q_2 and Q_5. The voltage stress and the current passing through Q_1 and Q_2 are shown in Figure 2.25. Since no gate signals are applied to the rectifying block switches, no switching losses in rectifying block are associated with the total converter loss in boost operating mode.

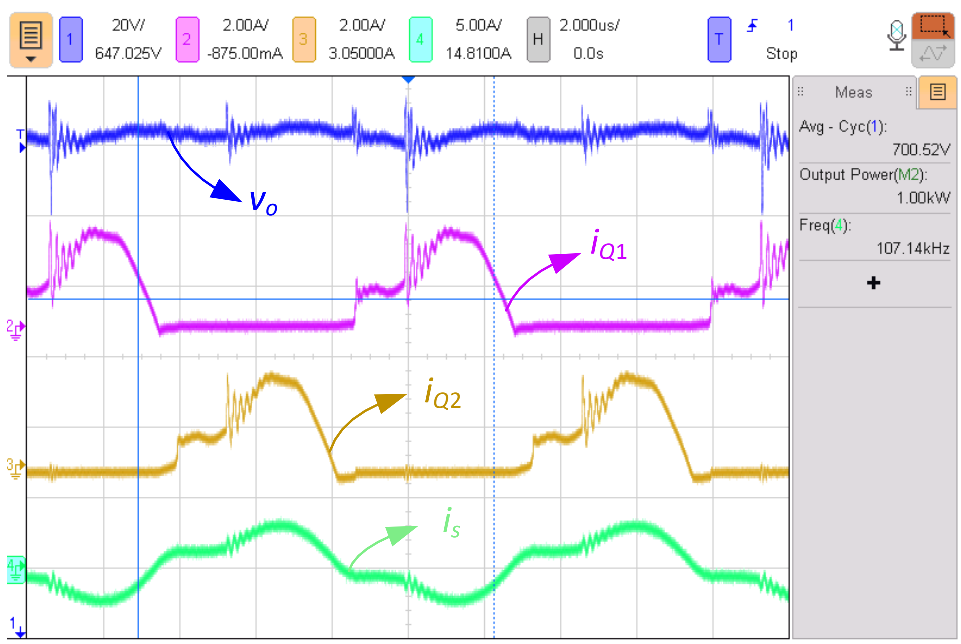
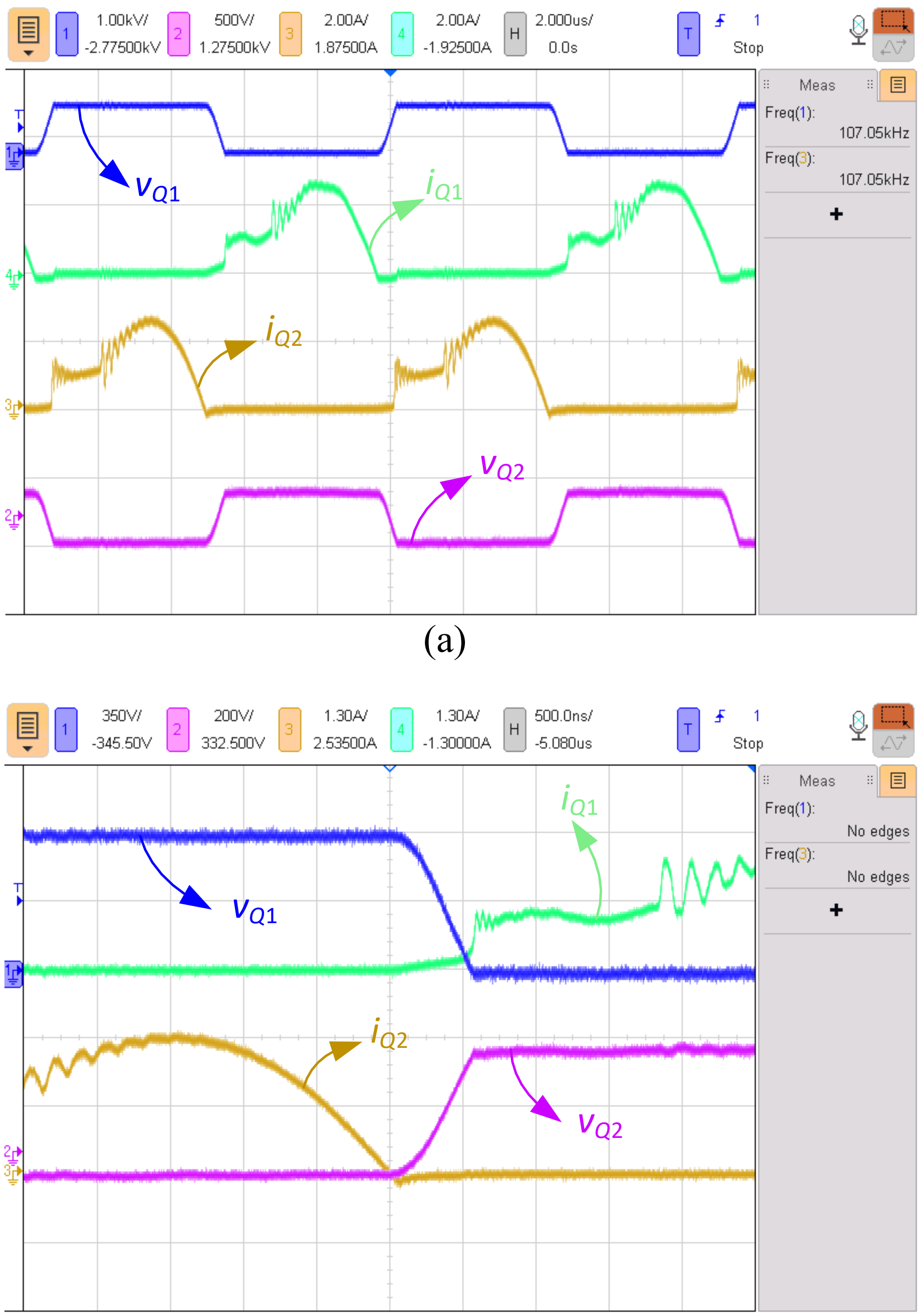


Figure 2.24- Experimental waveforms of the converter in boost mode. Converter's output voltage, current of Q_1 and Q_2 in the rectifying block and the current in secondary side of the resonant circuit



(a)

(b)

Figure 2.25- Experimental waveforms of the converter in boost mode. (a) Drain-source voltage and current of Q_1 and Q_2 in the rectifying block for two switching periods. (b) Zoomed-in snapshot.

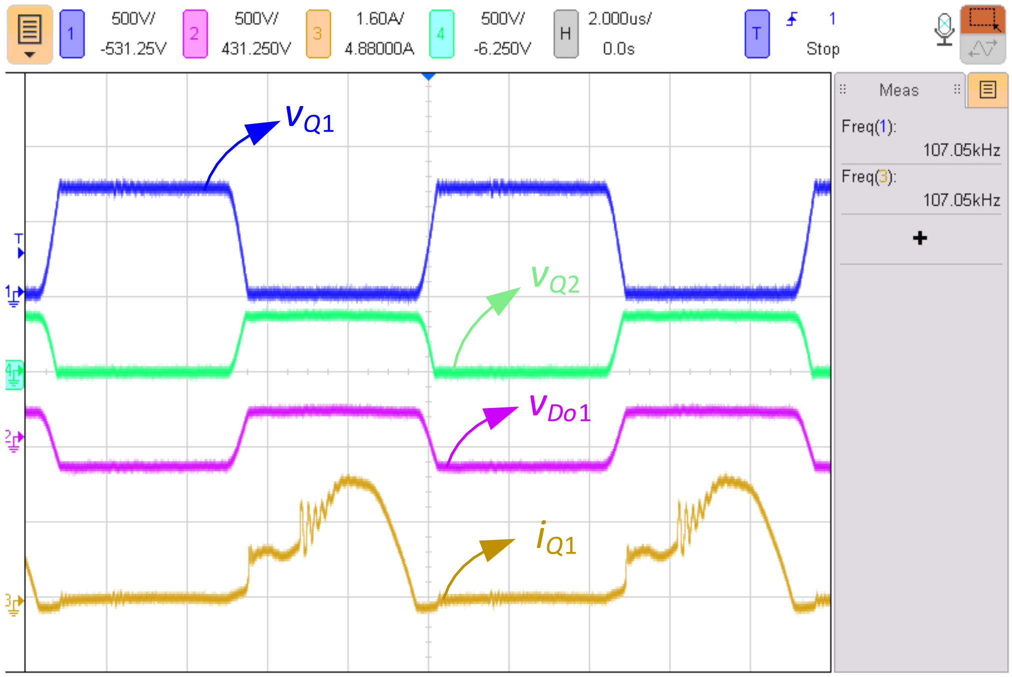


Figure 2.26- Voltage stress over Q_1, Q_2 and D_{o1} in the rectifying block and current of Q_1.

Figure 2.26 shows the voltage stress across the switches and the diodes in the rectifying circuit. Snubber capacitors of 150 pF are utilized in the secondary side to provide ZCS in this mode and to balance the voltage stress over Q_2, Q_5, D_{o1}, and D_{o2}.

In order to evaluate the performance of the control system, two scenarios have been investigated. In the first scenario, the input voltage has been reduced from 400V to 250V in boost mode and it has been investigated whether the converter can regulate the output voltage on 700V for a reduced loading condition (60%). The dynamic response of the proposed converter for a step input voltage change is provided in Figure 2.27. As can be seen, the control system has successfully regulated the output voltage to the desired value while providing ZVS for the switches. (Figure 2.28 and Figure 2.29).

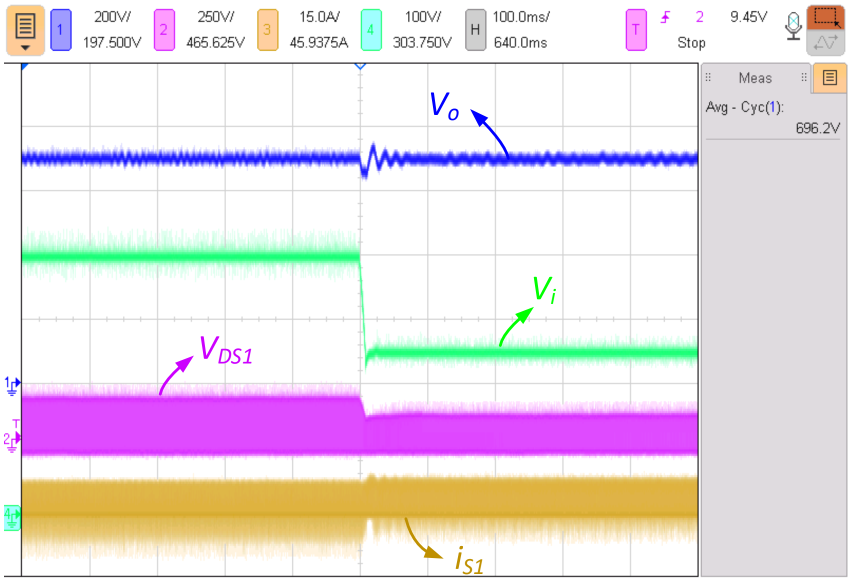


Figure 2.27- Dynamic response of the proposed converter for a step input voltage change (400V to 250V) with variable frequency control technique in boost mode for reduced loading condition (60%)

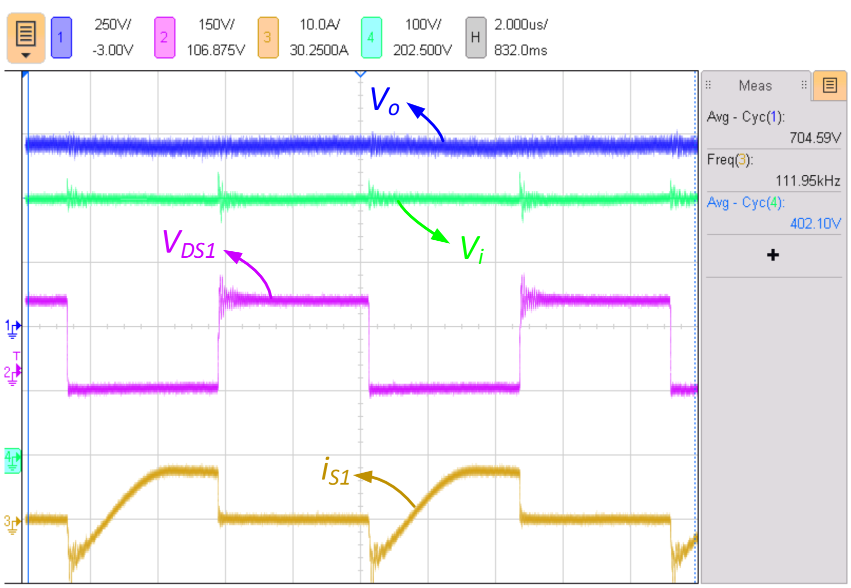


Figure 2.28- Experimental waveforms of the converter before the input step change (V_i =400V) for reduced loading condition (60%)

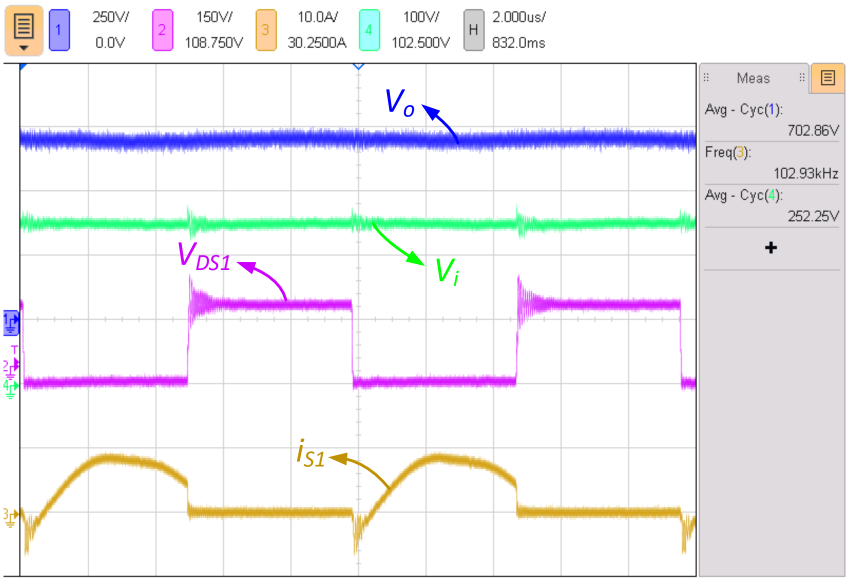


Figure 2.29- Experimental waveforms of the converter after the input step change (V_i =250V) for reduced loading condition (60%)

The zoomed-in snapshot of the experimental waveforms is demonstrated in Figure 2.30 and Figure 2.31. As can be seen, at the time the gate signal is applied to the S_1, the current is passing through its body diode in the opposite direction providing ZVS for S_1.

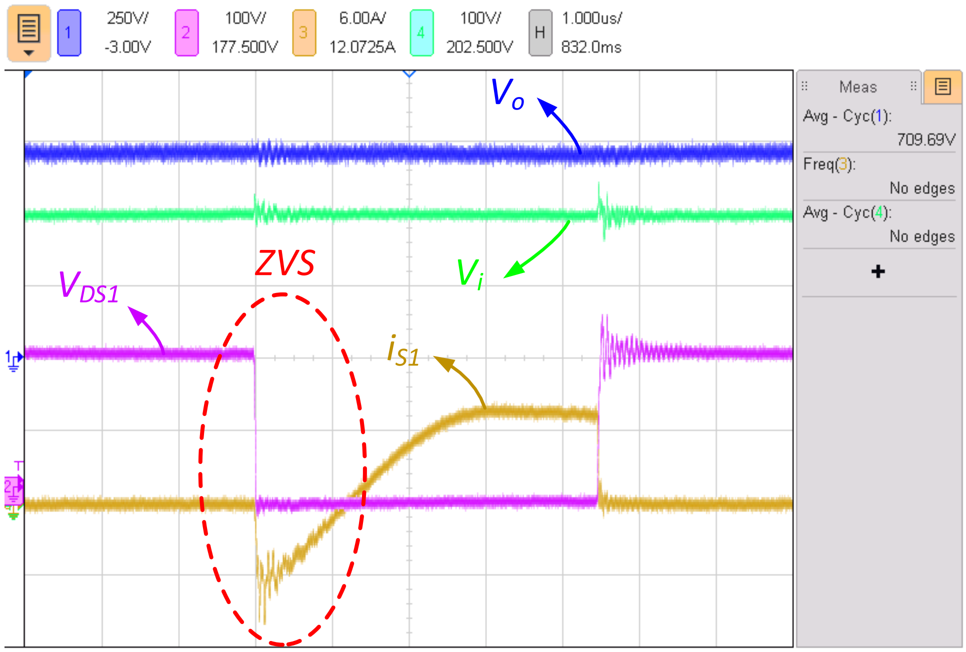


Figure 2.30- Zoomed-in snapshot of the experimental waveforms of the converter in boost mode (a) before the input step change (V_i=400V) at reduced loading condition (60%)

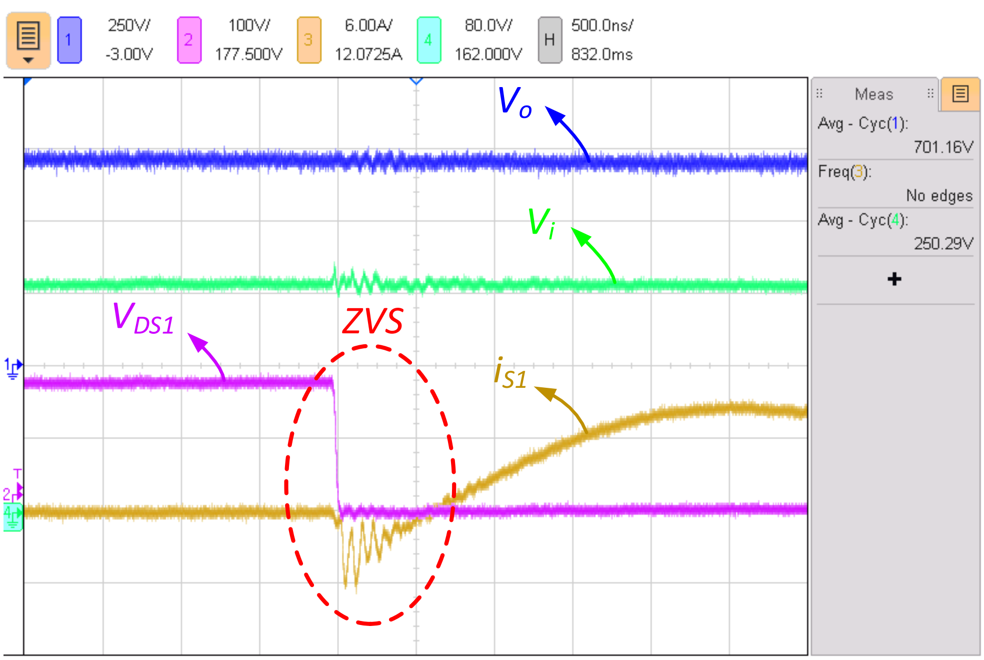


Figure 2.31- Zoomed-in snapshot of the experimental waveforms of the converter in boost mode (a) after the input step change (V_i=250) reduced loading condition (60%)

In the second scenario, the performance of the control system has been investigated in buck mode. In this mode, the load has been increased from 60% to 100% of the rated power and the performance of the converter in regulating the output voltage has been investigated. As can be seen in Figure 2.32, after the load has been increased, the converter has successfully regulated the output voltage in buck mode through the variable frequency control while providing ZVS for all of the switches (Figure 2.33 and Figure 2.34). The zoomed-in snapshots of the experimental waveforms are demonstrated in Figure 2.35 and Figure 2.36.

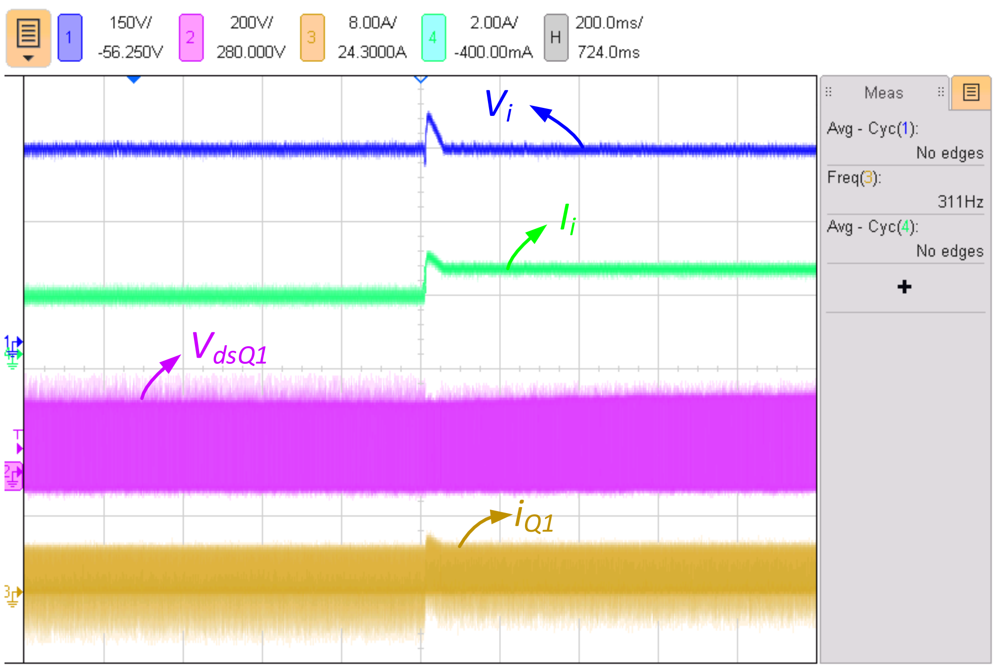


Figure 2.32- Dynamic response of the proposed converter for a 60% to 100% load change with variable frequency control in buck mode

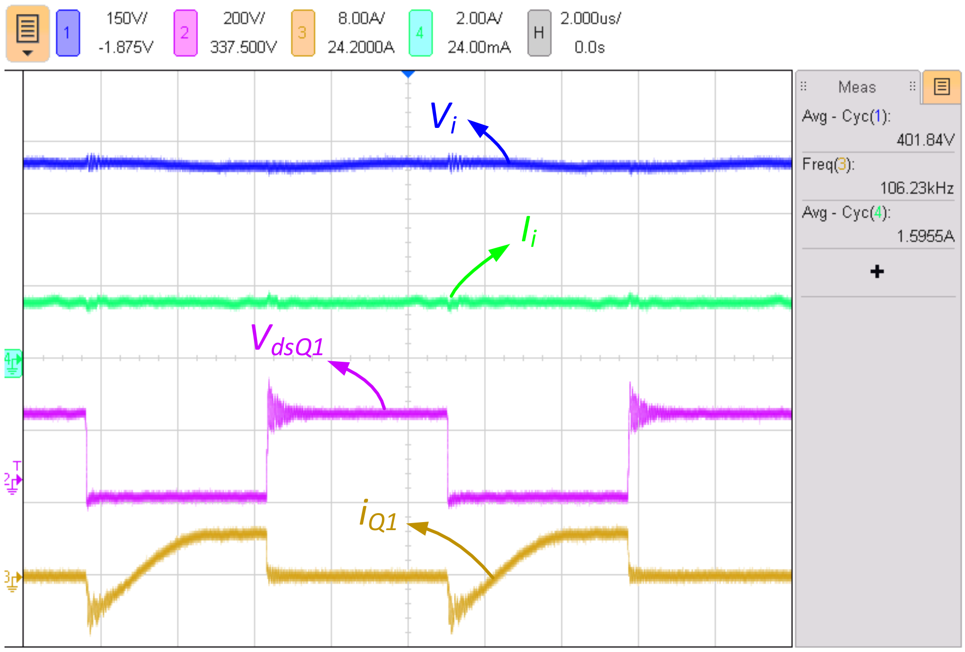


Figure 2.33- Experimental waveforms of the converter before the load step change

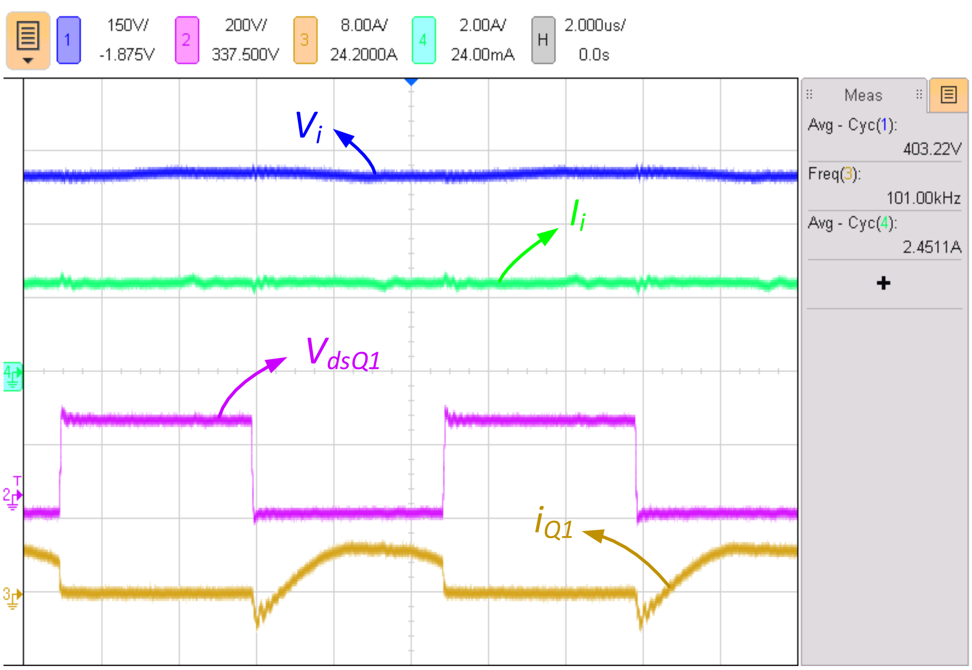


Figure 2.34- Experimental waveforms of the converter after the load step change

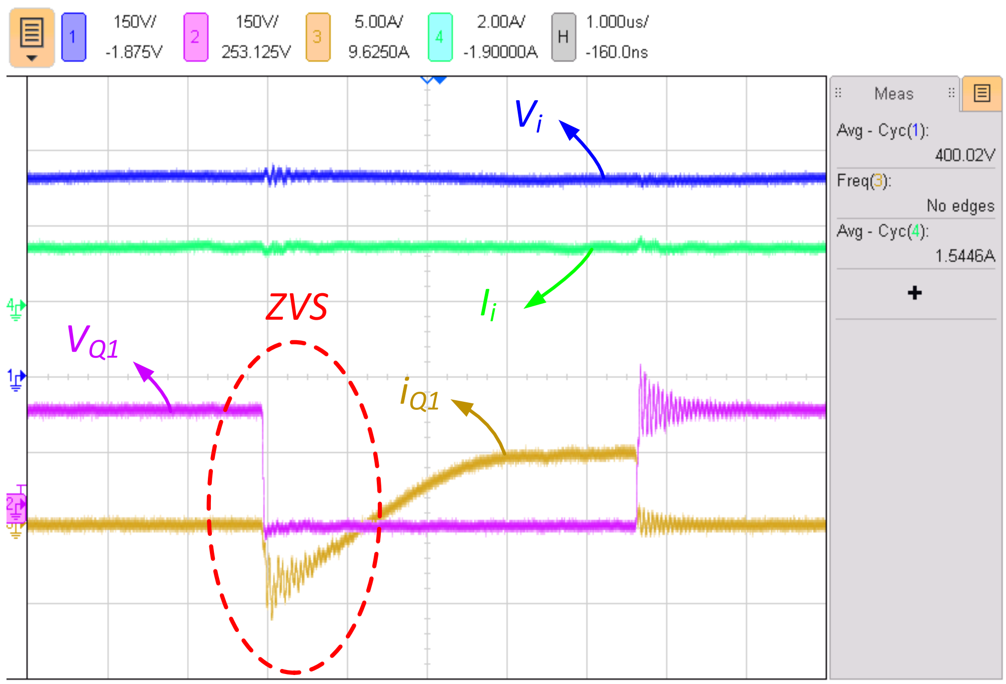


Figure 2.35- Zoomed-in snapshot of the experimental waveforms of the converter in buck mode before the load step change

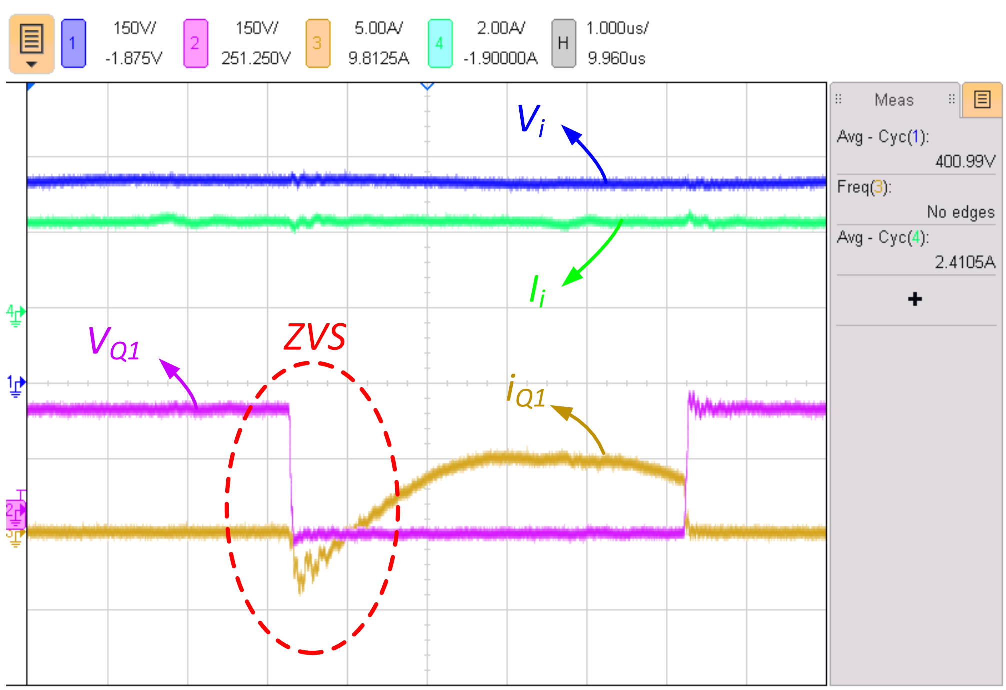


Figure 2.36- Zoomed-in snapshot of the experimental waveforms of the converter in buck mode after the load step change

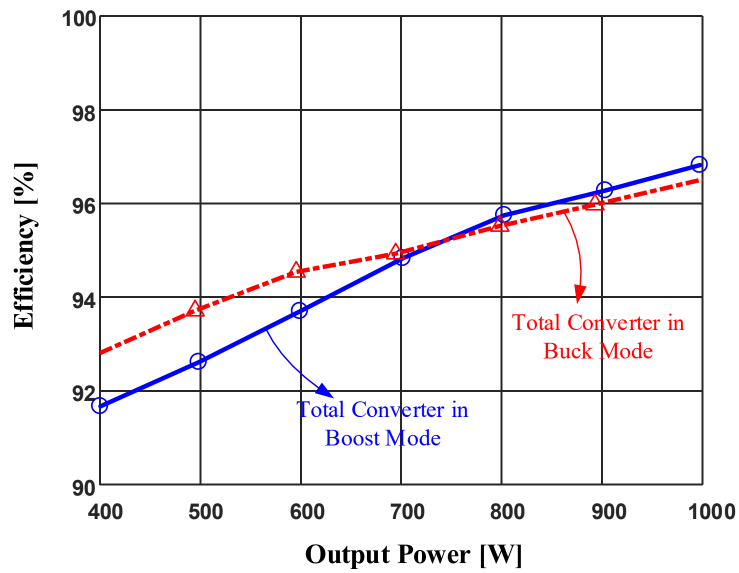


Figure 2.37- Efficiency curve of the proposed topology in both boost and buck modes

The efficiency curves of the proposed converter in boost and buck operating modes are presented in Figure 2.37. At 1 kW output power, the designed prototype shows a maximum efficiency of 96.8% in boost mode (Figure 2.38) and 96.5% in buck mode for a switching frequency of 107 kHz (Figure 2.39). The loss breakdown of the key components in the prototype is shown in Figure 2.40. Compared to the conventional DAB bidirectional converters, the proposed multi-mode stacked-switch converter reduces the voltage stress of half of the required switches to one-half of either the DC-link voltage or the battery voltage. In addition, the peak-to-peak output voltage ripple in the proposed topology is less than one-half of that in the conventional 4-switch string structured rectifier circuit, allowing lower output filter capacitance to be used. The thermal distribution of the primary and secondary side switches are shown in Figure 2.41. As can be seen, the loss is distributed equally over the switches and diodes.

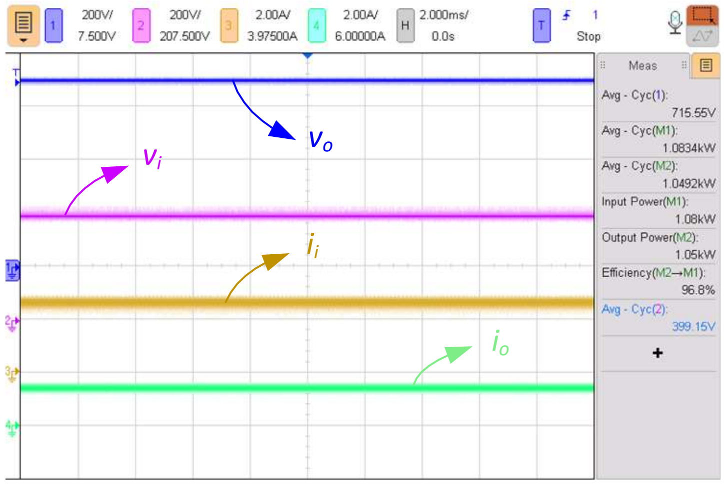


Figure 2.38- Experimental waveforms of the converter in boost mode for a 400V input, 700V output and a 487Ω resistive load. Input and output voltage and current waveforms along with the measured efficiency.

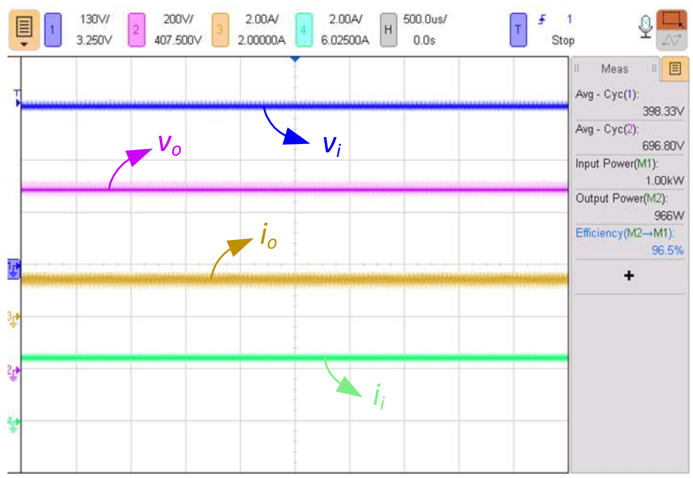


Figure 2.39- Experimental waveforms of the converter in buck mode for a 700V input, 400V output and a 160Ω resistive load. Input and output voltage and current waveforms along with the measured efficiency.

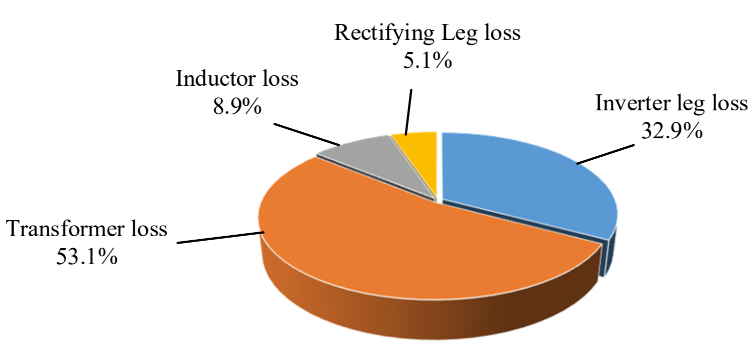
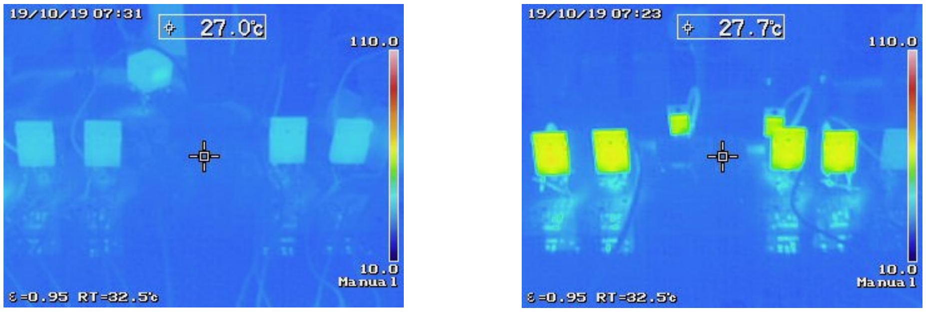


Figure 2.40- Loss breakdown of the key components in the prototype



(a) (b)

Figure 2.41- The thermal test results of the prototype operating at 1 kW output power in buck mode in a) inverting block b) rectifying block

2.6. Chapter Summary

In this chapter, a new multi-mode stacked-switch leg is proposed and analyzed for use in bidirectional power conversion for energy storage applications. The presented leg enables the converter to operate in rectifying mode with a much lower voltage ripple compared to the conventional 4-switch string converter with the same capacitive filter. Also, a bidirectional soft-switched converter utilizing a *CLLC* resonant circuit and the proposed multi-mode leg in both inverter and rectifier blocks is presented. The *CLLC* resonant tank allows the converter to step up/down the voltage levels while providing soft switching for all the switches and diodes. The operating principles and soft-switching conditions of the proposed converter are analyzed in detail. Variable frequency control is used to regulate the output voltage in the proposed converter. Simulation and experimental results on a 1kW, 100 kHz, 400 V/700 V converter prototype have been provided to further verify the theoretical concept and to highlight the features of the proposed circuit. Experimental results demonstrate that efficiency of close to

97% is achieved in the proposed converter in both boost mode and buck mode at full load condition. The dynamic performance of the converter prototype has also been given.

Chapter 3. Fault-Tolerant Operation of the Multi-Mode Stacked-Switch Leg

As discussed earlier, DC/DC power converters play an essential role in enabling the use of storage technologies and hence, are widely used in many industries like automotive, aerospace, and consumer electronics [85][35][86][54]. In these applications, the converters often experience transients while transferring power from the input to the load which may cause failures and interrupts in the power delivery [87][88][68]. System failures are not desirable especially in military and aerospace applications where they may lead to drastic economic losses. In energy storage applications, reliability is of most importance since any failure in the converters might result in irreparable damage to the storage system and incur additional costs since batteries and other energy storage technologies tend to be the most expensive components of the energy storage systems. Hence, fault-tolerant approaches are mandatory to ensure service continuity.

Early remedial actions using fault-tolerant control increase the reliability of the converter and minimize the damage. Surveys and field experiences have shown that due to high power and thermal stress, power semiconductor devices (MOSFETs, IGBTs, etc.) are the most vulnerable and fragile components in power converters (31%), followed by those of capacitors

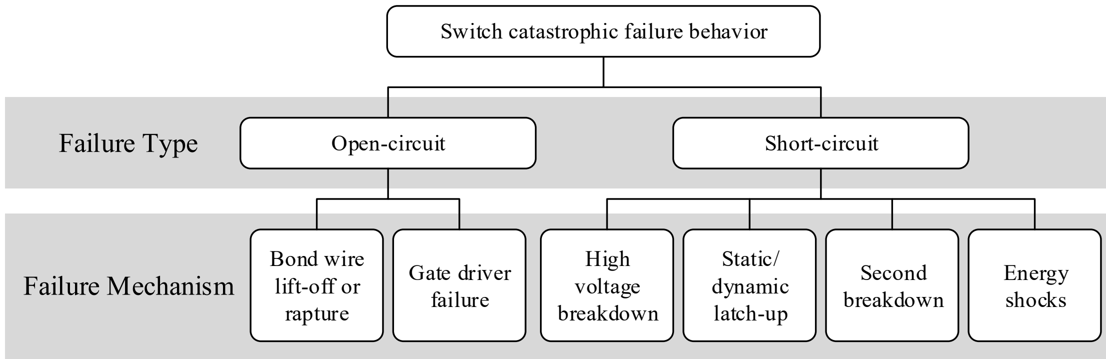


Figure 3.1- Overview of switch catastrophic failure [90]

(17%) and gate driver circuits (15%) [88][89]. Since, most of the power converters don't offer redundancy in operation, in case any fault incurs during the normal operation, the converter cease to operate.

Switch failures can be generally classified as catastrophic failures and wear-out failures. Switch wear-out failure is mainly caused by accumulated degradation with time, while catastrophic failure is triggered by single-event overstress, such as overvoltage, overcurrent, overheating, etc. While the wear out failures can be estimated by Prognostics and Health Management (PHM) methods with monitoring the degradation of switches, PHM is not applicable for catastrophic failure, which is more difficult to be predicted [90].

A significant amount of research has covered switch failure and fault diagnosis and protection methods. Semiconductor catastrophic failure behaviors in power converters are more related to semiconductor physics and overstress working conditions and are broadly classified as short circuit-faults (SCF) and open-circuit faults (OCF) as demonstrated in Figure 3.1[68][91].

As illustrated in Figure 3.2, SCF modes can be classified with respect to time-sequence. Switch short circuit during turn-on can be caused by a high gate voltage and external failure. Failure during ON-state may be caused by static latch-up or the rapid increase of intrinsic temperature caused by energy shocks. Dynamic latch-up and high voltage breakdown may cause failure during turn-off.

OCF can happen as a result of an external disconnection due to vibration, as well as bond wire lift-off or rupture or gate driver failure. Bond wire lift-off failure can happen after short-circuit failure and is generally due to mechanical reasons including the mismatch of coefficients of thermal expansion (CTEs) between Silicon and other ingredients. The thermal cycling causes repeated cooling and heating; thus, allowing the joint materials to expand and shrink at different rates and it applies the stress at the point of contact leading to cracks in the bond area. Another failure mechanism is bond wire rupture, which is slower than lift-off and is usually observed after long power cycling tests.

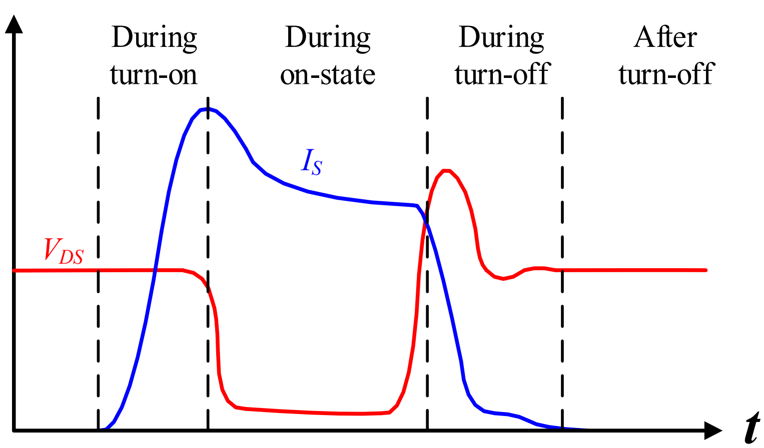


Figure 3.2- Time-sequence classification of the switch short-circuit failure [90]

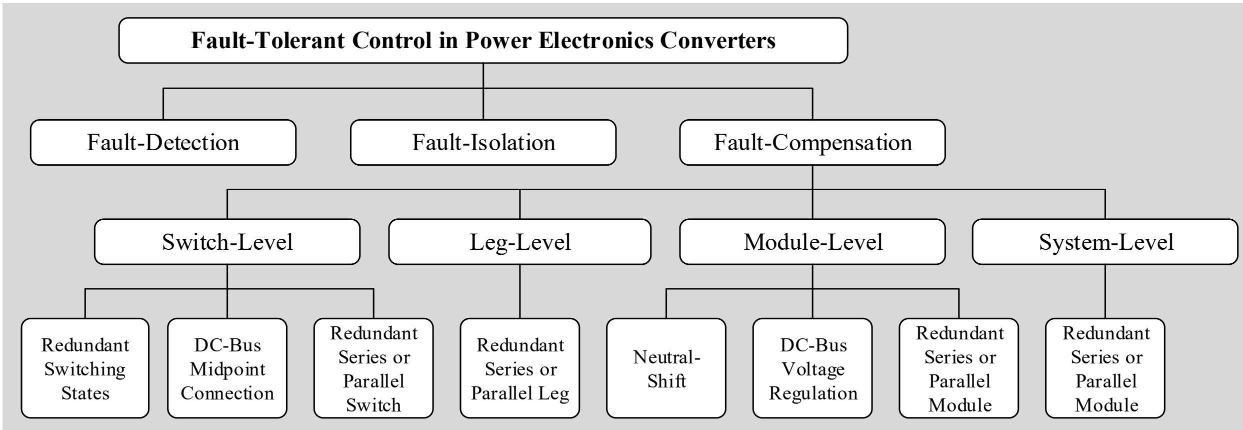


Figure 3.3- State-of-the-art fault-tolerant methodology chart [88]

There are various causes of a gate driver failure, such as abnormal work conditions in power terminals of the switch, damaged power stage devices, and disconnection of wires between drive board and switch. The driver failure may result in switch intermittent misfiring, degraded output voltage, and overstress of other switches and capacitors [92][90].

Considering the severity of the SCFs, standard monitoring and protection measures have already been integrated into the gate drivers to prevent them. Typically, an SCF in the power converter feeding a BESS will stop its operation; in contrast, an OCF will likely keep the BESS working. Compared to an SCF, OCF may not always cause serious damage but the system performance is reduced drastically. In addition, OCFs may cause secondary failures of other components due to voltage/current distortion [90].

The key goal of a fault-tolerant control scheme is to intercept the propagation of the fault to the rest of the converter to prevent cascading failures [93]. Steps involved in any fault-tolerant control scheme are detection, isolation, and fault compensation (Figure 3.3). Due to its benefits, fault-tolerant control schemes are employed at the design stage of the converter to improve its resilience against all types of failures.

Table 3.1- Comparison table for fault-tolerant control schemes in different converter topologies [93]

Topology	Fault Type	FT Scheme	Service Continuity
Cascaded DC/DC Con. [98]	SCF	Extra SM	LVF Partial, HVF No
PV Mod. with Buck-Boost Con. [99]	SCF	Extra SM	Yes
Modular Resonant DC/DC Con. with VSC [100]	SCF	Extra SM	No
CDCDC [101]	SW SCF	Extra SM for each cell	Yes
Interleaved boost Con. [67]	OCF/SCF	Adj. of control scheme	Yes
BD boost Con. with 3φ Inv. [102]	OCF	Extra leg	Yes
DAB with CPS Control [103]	OCF	Control adj. of primary Arm bypass Secondary	Primary side ¾ power Secondary side 7/9 power
6φ IBC [104]	OCF	Bypass of faulty leg	Yes
Reconfigurable boost with NPC Con.[105]	OCF/SCF	Disconnection of faulty leg	Yes
5 Channel 3L-NPC [106]	OCF	Extra shared leg	50% of power
3φ Dual buck VSI [107]	OCF/SCF	Redundant dual buck HB with coupled inductor	Yes
Buck, boost Buck-boost [108], [109]	OCF/SCF	Extra switch	Yes
Modified boost Con. [110]	OCF	Extra switch	80% of power
Two stage buck Buck-boost con. [87]	OCF	Extra Switch	Yes
Single ended DC/DC Con.[111]	OCF/SCF	Extra Switch	Yes
Parallel connected DC/DC Con. [112]	OCF/SCF	Extra Switch	Yes
FB-SMC [113]	OCF/SCF	SW reconfiguration	8% Less efficient
PCSAB [114]	OCF	Phase Adjustment of Healthy Module	Yes
Buck with Multimode single leg Con. [115]	OCF	PWM reconfiguration Relocation of diodes	Yes
M5LT DAB Con. With PDPWM [116]	OCF/SCF	Adj. of control scheme	Reduced voltage quality

Considering the aforementioned arguments, open-circuit fault-compensation has been considered the main focus of this thesis. In both SCF and OCF cases, the remedial actions are generally based on hardware redundancy and redundant switches fault-tolerant control associated with a proper switching strategy [88].

Fault-tolerant operation of several efficient converter topologies has been reviewed in Table 3.1. In some cases, by introducing additional components in the basic converter topology, service continuity is ensured. Whereas, in other cases, the fault-tolerant control is implemented by changing the control sequence without adding any components or reconfiguration of the converter. Yet, the fault-tolerant strategies need to be carried out carefully and cannot be incorporated into any converter blindly. Some of the consequences of implementing a fault-tolerant control in DC/DC converters are higher conduction and switching losses, reduced power output, and high ripples in the output.

This chapter discusses the open-circuit fault in the proposed multi-mode stacked-switch leg and investigates the performance of the converter in the case an OCF incident happens on any of the switches. In the first part, a novel fault-tolerant control is proposed based on the built-in circuit redundancy in the multi-mode stacked-switch converter in the rectifying block. In the second part of this chapter, OCF is investigated in the proposed converter in the inverting block. A modified version of the multi-mode stacked-switch converter is presented to address the shortcomings of the previously proposed converter. In the final section, experimental results are provided to investigate the performance of the proposed fault-tolerant control in the multi-mode stacked-switch converter.

3.1. Open-Circuit Fault in Power Converters

As mentioned in Chapter 2, in the case of using an *LLC* or *CLLC* resonant circuit to provide soft-switching in a bidirectional converter, the series inductance at the input terminal of the rectifier acts as a current source. The operation of the rectifying block in the DAB and the 4-switch string circuits employing a *CLLC* resonant tank are demonstrated in Figure 3.4 and

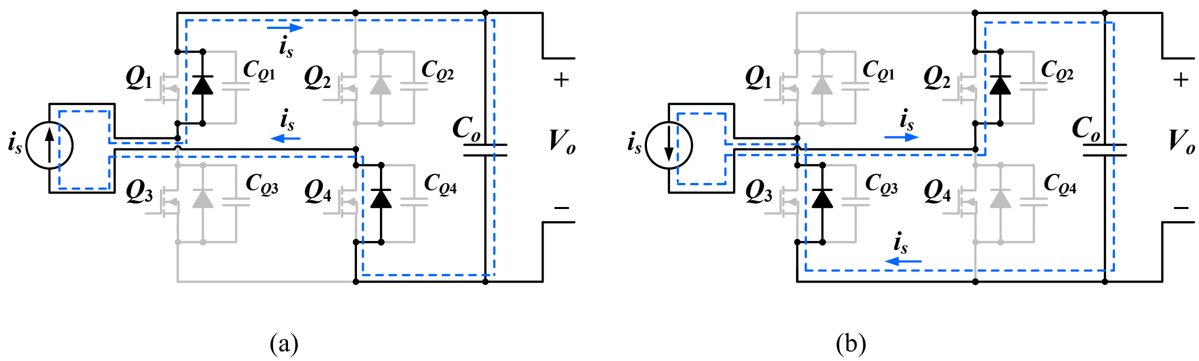


Figure 3.4- Topology of the rectifying stage of a DAB circuit with OCF in Q_1 for: a) positive i_s with alternative current path in blue, b) negative i_s

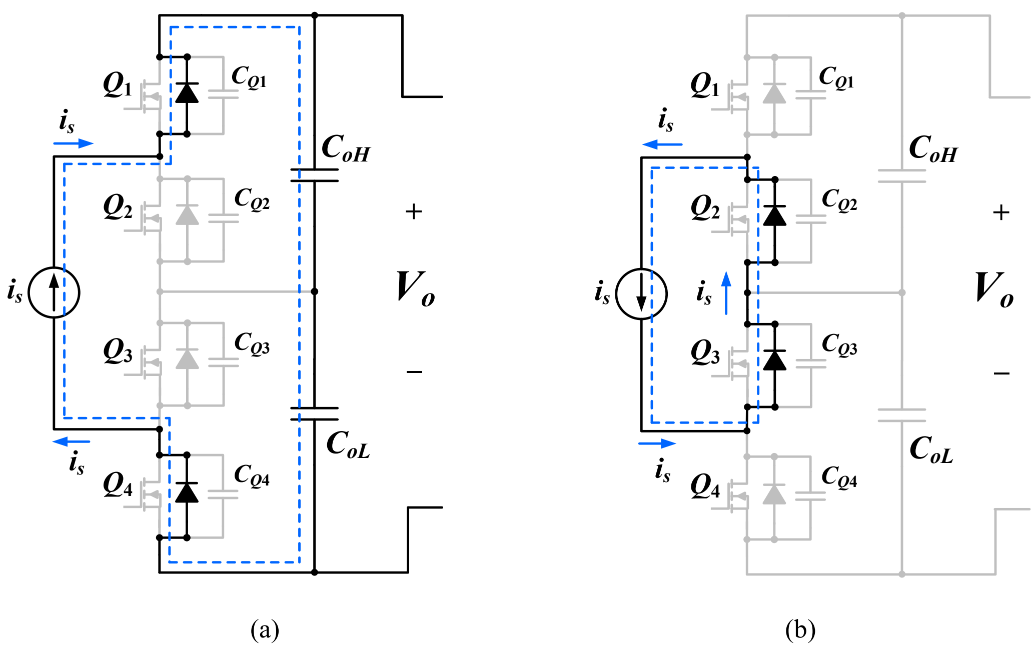


Figure 3.5- Topology of the conventional 4-switch string circuit operating as a rectifier including the current path for: a) positive i_s, b) negative i_s

Figure 3.5 respectively. In these converters, before any OCF incident and during normal operation of the circuit, the positive current at the secondary side of the resonant circuit (i_s) passes through the body diodes of Q_1 and Q_4 (Figure 3.4a and Figure 3.5a) and the negative current circulates through the freewheeling diodes of Q_2 and Q_3 (Figure 3.4b and Figure 3.5b).

However, in the DAB converter, in case of a complete loss of Q_1 and its body diode (Figure 3.6), since the normal current path for the positive i_s to feed the load is open, in order to address the fault and to enable the converter to provide power to the load, right after the fault has been detected, by turning ON Q_3, operating in a complementary fashion to Q_1, the converter is still able to deliver power to the load for the negative i_s while allowing the positive i_s to circulate through the converter (the blue current path), operating as a half-wave rectifier, therefore; the voltage ripple in the output terminal is doubled.

In the 4-switch string converter topology and during normal operation, as it is demonstrated in Figure 3.5, only the positive current passes through the output capacitors and the negative current circulates through Q_2 and Q_3. As a result, in the case of an OCF in Q_1 or Q_4 shown in Figure 3.7, the circuit is not able to deliver power to the load. While with any OCF in Q_2 or Q_3,

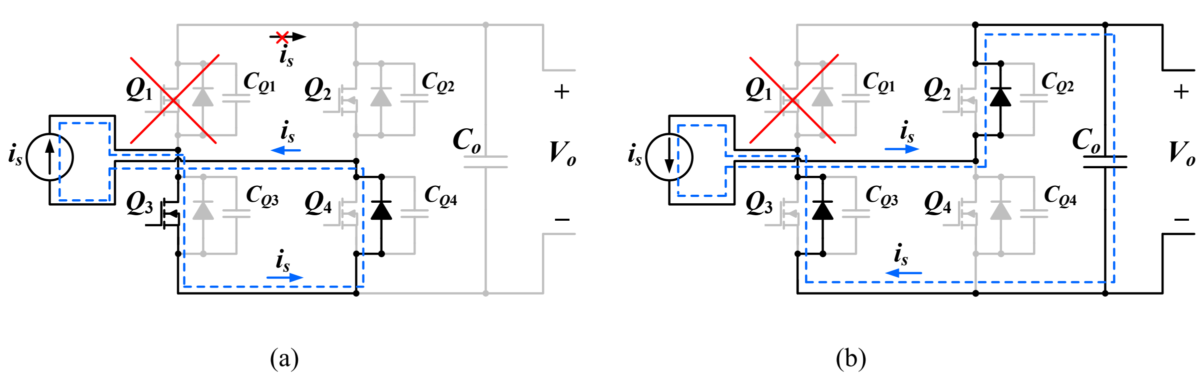


Figure 3.6- Topology of the rectifying stage of a DAB circuit with OCF in Q_1 for: a) positive i_s with alternative current path in blue, b) negative i_s

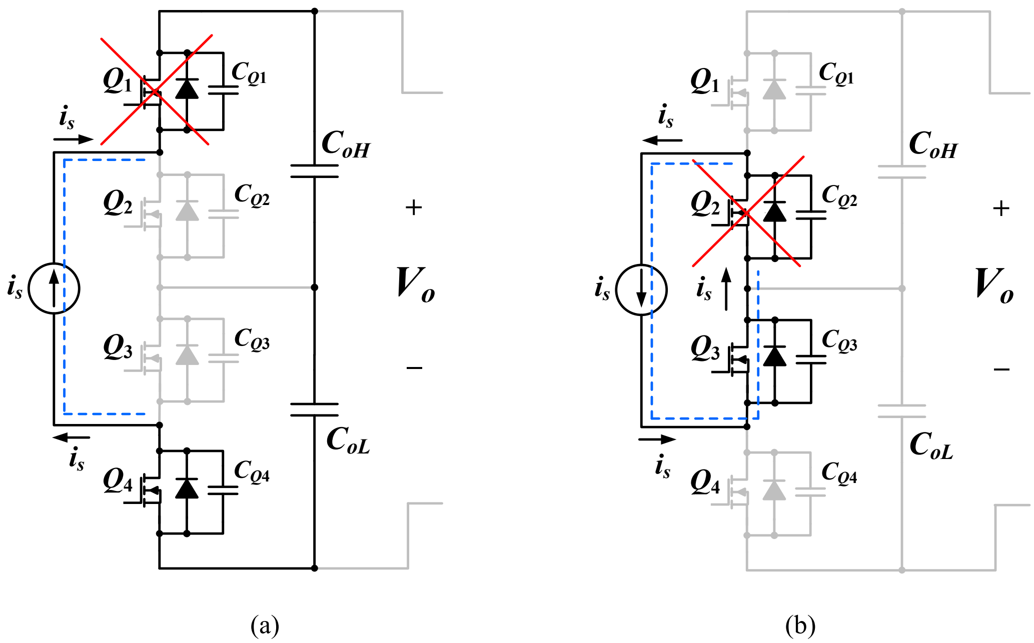


Figure 3.7- Topology of the conventional 4-switch string circuit operating as a rectifier including the current path for: a) positive i_s, b) negative i_s

the circuit is still able to provide power to the load, since there is no path for the secondary side current to circulate, it drastically impacts the operation of the converter and imposes voltage/current stress over the switches and the resonant components.

3.2. Open-Circuit Fault-Tolerant Operation of the Multi-Mode Stacked-Switch Converter

The operating principle of the multi-mode stacked-switch bidirectional converter has been discussed in Chapter 2. The added diodes and low-frequency switches provide a built-in circuit redundancy operation and allow the converter to switch between multiple operating modes namely full-wave (FW), half-wave (HW), voltage-doubler (VD).

To better understand the behavior of the converter during an open-circuit fault, the key waveforms of the converter have been provided in Figure 3.8 in which an OCF happens at t=t_{10} in Q_1. When the converter experiences an OCF the incident needs to be detected as soon as

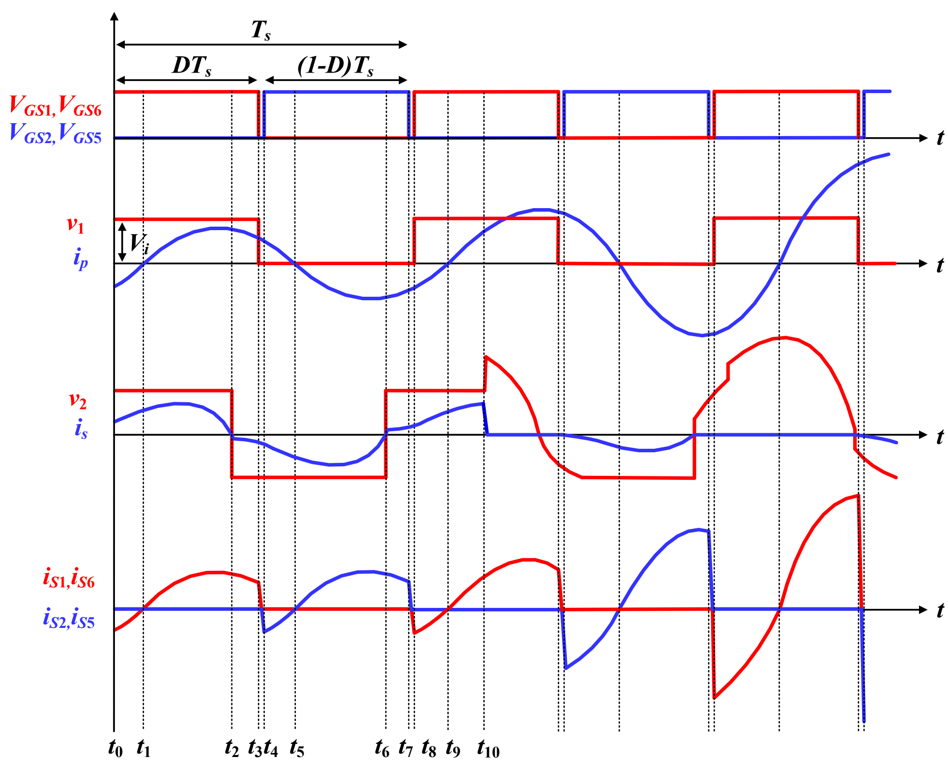


Figure 3.8- The key waveforms of the multi-mode DC/DC converter during an OCF in Q_1

possible and appropriate gate signals need to be applied to the switches on the rectifying side. Fault-tolerant operation of the multi-mode stacked-switch rectifier leg with an OCF in Q_1 has been shown in Figure 3.9 and Figure 3.10. Considering the normal operating modes of the converter described in Table 3.2, by losing Q_1, both VD and HW operating modes can address the fault and enable the converter to operate without any interruption.

Table 3.2- Switching patterns of the multi-mode stacked-switch rectifier leg during normal operation

Switching Pattern	Switching patterns						**Mode**
	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	
1	OFF	OFF	OFF	OFF	OFF	OFF	FW
2	OFF	OFF	ON	ON	OFF	OFF	HW
3	OFF	ON	ON	OFF	OFF	OFF	VD
4	OFF	OFF	OFF	ON	ON	OFF	VD

Figure 3.9 shows the VD operating mode after an OCF in Q_1. After detecting the fault, Q_2 and Q_3 are switched ON and the positive i_s goes through Q_2, Q_3, and Q_6 charging C_L. In the same manner, the negative i_s passes through Q_2, Q_3, Q_5, and D_H charging C_H, hence; the output

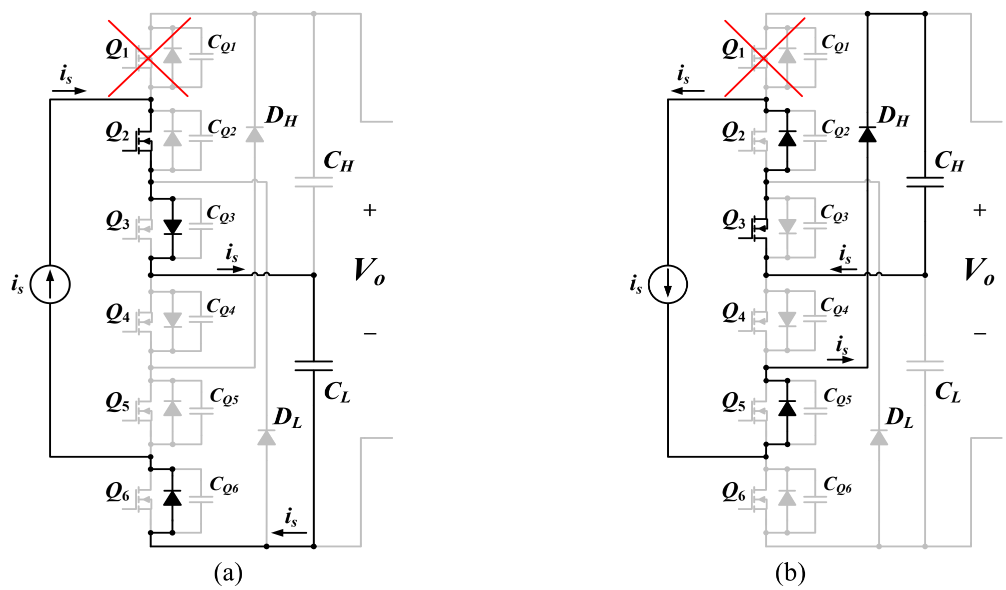


Figure 3.9- VD fault-tolerant operation of the multi-mode stacked-switch rectifier leg with OCF in Q_1. a) positive i_s, b) negative i_s

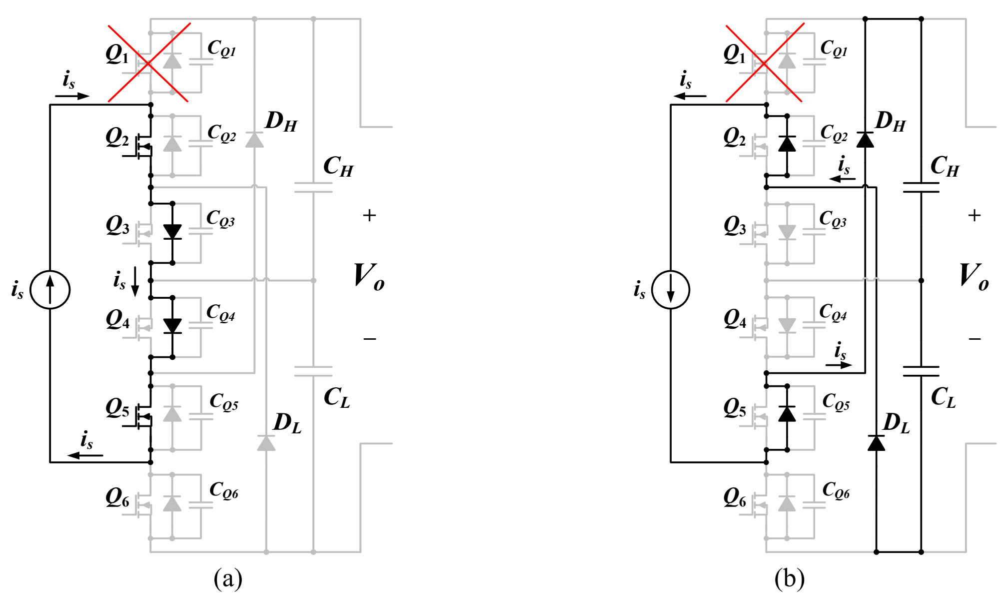


Figure 3.10- HW fault-tolerant operation of the multi-mode stacked-switch rectifier leg with OCF in Q_1. a) positive i_s, b) negative i_s

voltage ripple is minimized. HW operation of the converter after an OCF in Q_1 has been depicted in Figure 3.10. To address the fault, Q_2 and Q_5 are turned ON. As a result, the positive i_s goes through Q_2, Q_3, Q_4, and Q_5 and circulates without passing through the load while the negative i_s closes its path through Q_2, Q_5, D_H, and D_L charging C_H and C_L.

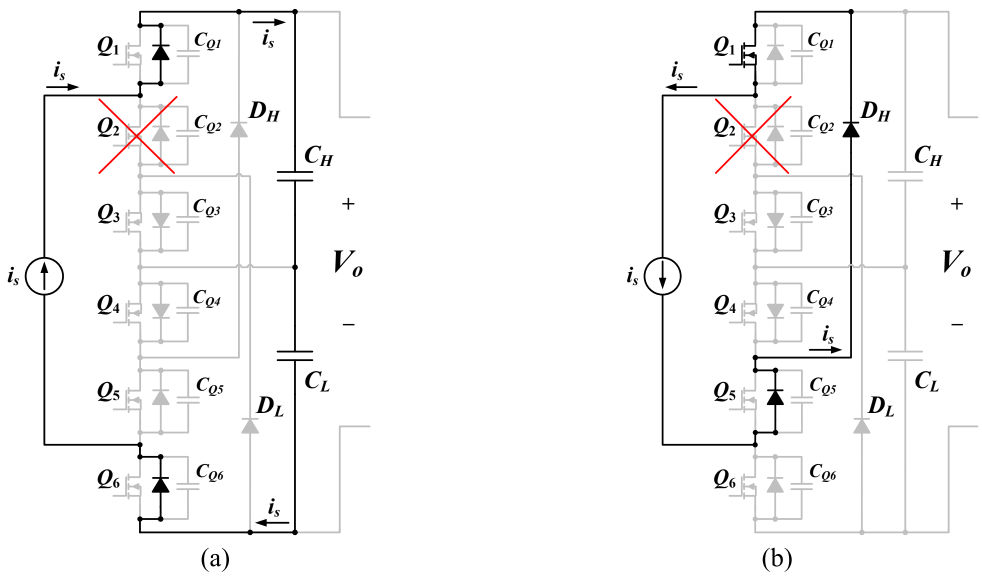


Figure 3.11- HW fault-tolerant operation of the multi-mode stacked-switch rectifier leg with OCF in Q_2. a) positive i_s, b) negative i_s

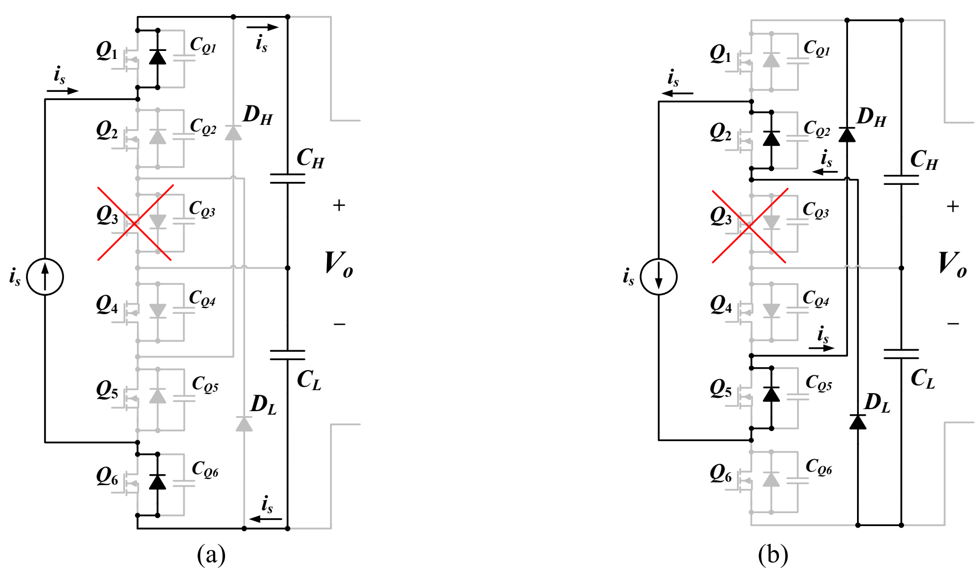
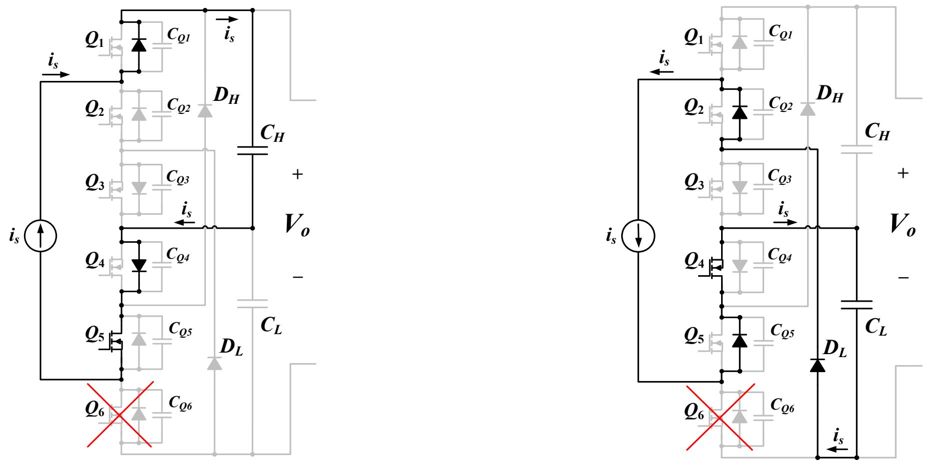
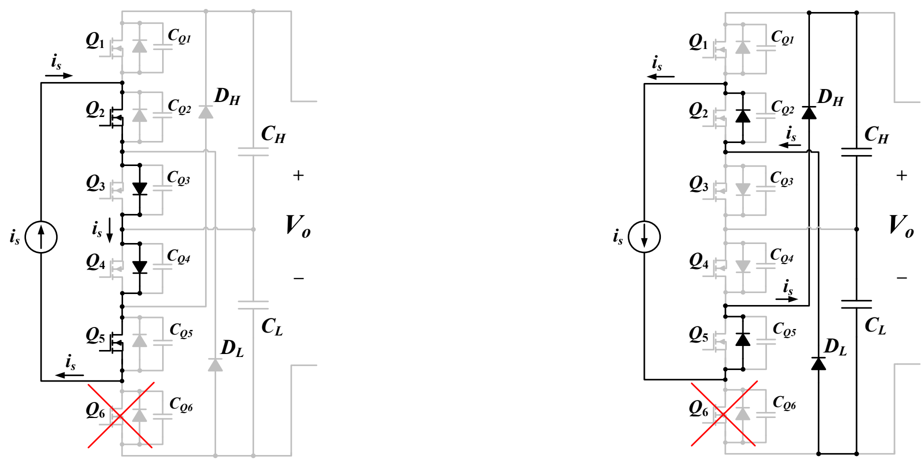


Figure 3.12- FW fault-tolerant operation of the multi-mode stacked-switch rectifier leg with OCF in Q_3. a) positive i_s, b) negative i_s



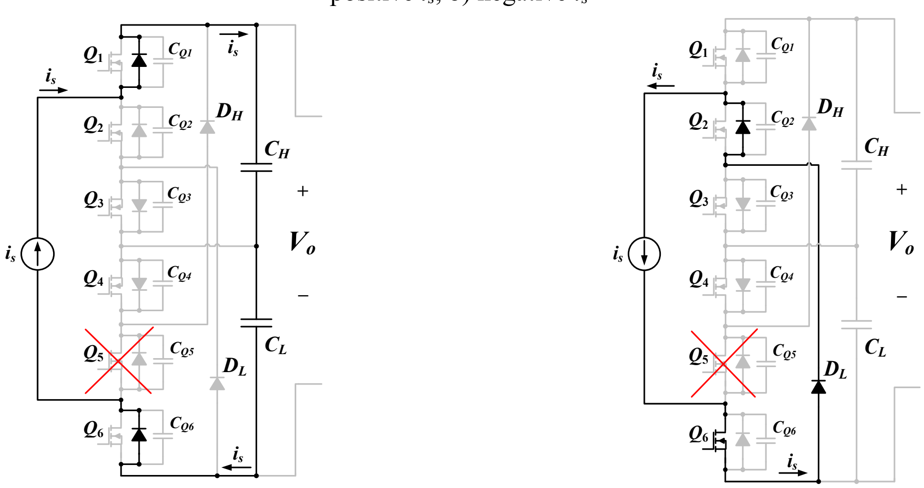
(a) (b)

Figure 3.13- VD fault-tolerant operation of the multi-mode stacked-switch rectifier leg with OCF in Q_6. a) positive i_s, b) negative i_s



(a) (b)

Figure 3.14- HW fault-tolerant operation of the multi-mode stacked-switch rectifier leg with OCF in Q_6. a) positive i_s, b) negative i_s



(a) (b)

Figure 3.15- HW fault-tolerant operation of the multi-mode stacked-switch rectifier leg with OCF in Q_6. a) positive i_s, b) negative i_s

Figure 3.11 shows the HW operating mode after an OCF in Q_2. As can be seen, Q_1 is turned ON right away to overcome the fault. In this case, positive i_s goes through Q_1 and Q_6 charging both capacitors, while the negative i_s passes through Q_1, Q_5, and D_H and circulates without going through the load, therefore; the output voltage ripple is high.

Figure 3.12 demonstrates the FW fault-tolerant operation of the converter in the case of an OCF in Q_3. In the same manner, Figure 3.13 and Figure 3.14 show the alternative switching patterns in the case of an OCF in Q_6 and Figure 3.15 and Figure 3.16 demonstrate the HW and FW fault-tolerant operation in case of a fault in Q_5, and Q_4 respectively. Table 3.3 summarizes the switching patterns for the fault-tolerant operation of the multi-mode stacked-switch rectifier leg.

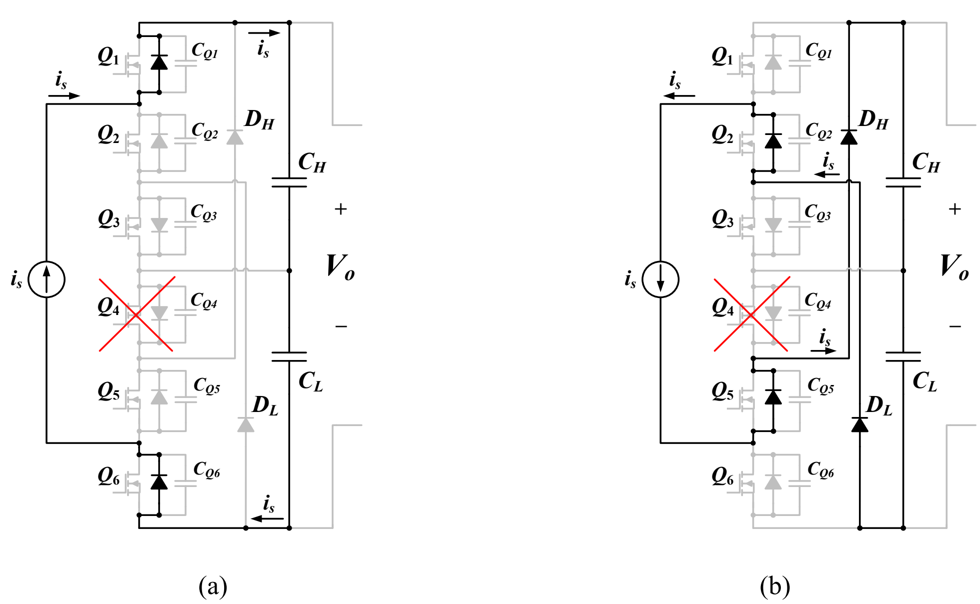


Figure 3.16- FW fault-tolerant operation of the multi-mode stacked-switch rectifier leg with OCF in Q_4. a) positive i_s, b) negative i_s

Table 3.3- Fault-tolerant switching pattern of the multi-mode stacked-switch rectifier leg

OCF	Switching patterns						Mode
	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	
Q_1	-	ON	ON	OFF	OFF	OFF	VD
	-	ON	OFF	OFF	ON	OFF	HW
Q_2	ON	-	OFF	OFF	OFF	OFF	HW
Q_3	OFF	OFF	-	OFF	OFF	OFF	FW
	OFF	OFF	-	ON	ON	OFF	VD
	ON	OFF	-	OFF	OFF	OFF	HW
	OFF	OFF	-	OFF	OFF	ON	HW
Q_4	OFF	OFF	OFF	-	OFF	OFF	FW
	OFF	ON	ON	-	OFF	OFF	VD
	ON	OFF	OFF	-	OFF	OFF	HW
	OFF	OFF	OFF	-	OFF	ON	HW
Q_5	OFF	OFF	OFF	OFF	-	ON	HW
Q_6	OFF	OFF	OFF	ON	ON	-	VD
	OFF	ON	OFF	OFF	ON	-	HW

3.2.1. **Design Consideration for the Multi-Mode Operation**

In Chapter 2, the steady-state analysis of the proposed bidirectional multi-mode stacked-switch converter was presented. The overall gain of the converter was obtained and based on the operating points, the circuit components of the *CLLC* resonant tank were selected. Yet, due to the ability of the converter to switch between different operating modes (HW, VD, and FW), the equivalent AC resistance seen at the secondary of the resonant tank varies depending on the operating mode. While R_{ac} is equal to $8R_L/\pi^2$ for the full-wave rectifier operating mode mentioned in Chapter 2, it is reduced to $2R_L/\pi^2$ for the half-wave and voltage-doubler rectifying modes. The same voltage gain equations given in (3.1) and (3.2) are valid for the overall gain of the converter in both boost and buck modes.

$$\frac{V_2}{V_1}=\frac{\omega_r^{\,2}}{(\omega_r^{\,2}-1)+j\dfrac{1}{Q}(k\omega_r^{\,3}-\dfrac{\omega_r}{m}-k\omega_r+\dfrac{1}{m\omega_r}-\omega_r)} \tag{3.1}$$

$$\frac{V_1}{V_2}=\frac{j\omega_r}{\dfrac{1}{Q}(1+\dfrac{1}{m}-\dfrac{1}{m\omega_r^{\,2}}+k(1-\omega_r^{\,2}))+j(\omega_r-\dfrac{1}{m\omega_r}+k\omega_r)} \tag{3.2}$$

Yet, considering that the quality factor $Q = R_{ac}/L_M\omega_0$ is different due to a change in R_{ac}, the overall gain of the converter differs significantly depending on the operating mode. The total

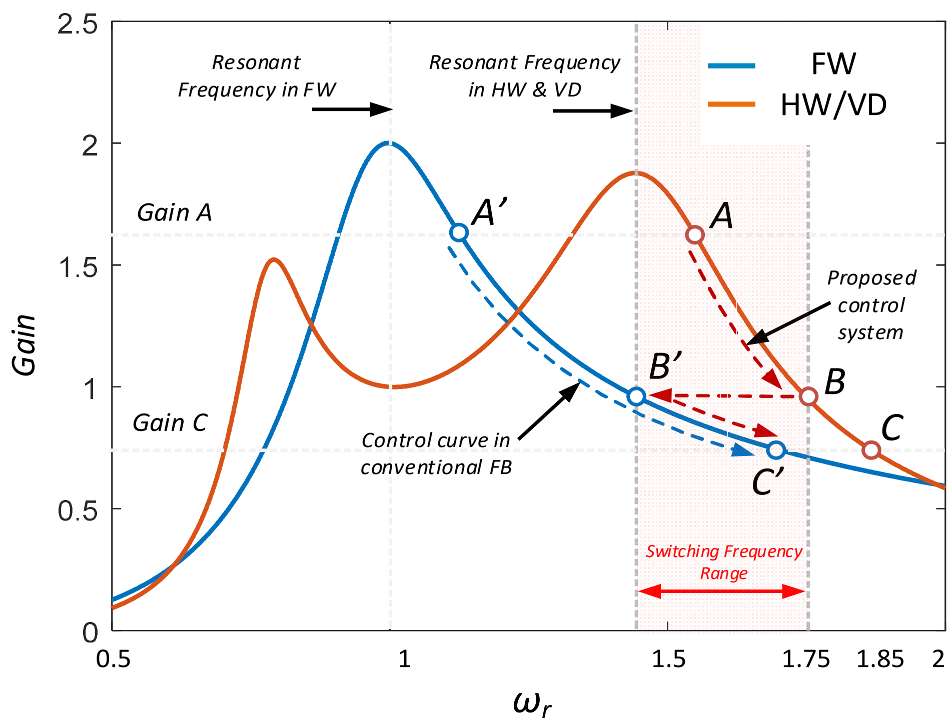


Figure 3.17- Voltage gain plot of the multi-mode stacked-switch converter with a *CLLC* resonant tank in boost mode

gain of the converter in boost mode in terms of the normalized angular switching frequency is obtained in Figure 3.17 for both FW and HW/VD modes with k=2 and m=0.39.

As can be seen by switching from one mode to another, the gain curve undergoes a drastic change and the peak gain moves from ω_r=1 to ω_r=1.5. In addition, achieving a gain of A or B requires further increasing the switching frequency in HW/VD mode compared to that of in FW. As a result, by properly controlling the switching states of Q_3 and Q_4 and by switching from one mode to another, in the case of using the variable frequency control to regulate the output voltage, the switching frequency can be limited while achieving the same gain (Figure 3.17). As an example, to move from a gain of A to a gain of C, instead of setting the normalized angular switching frequency to 1.85 in HW/VD mode, ω_r can be limited to 1.7 by moving from HW/VD mode to FW mode.

3.3. Open-Circuit Fault Detection

As it has been shown in Figure 3.8, in the case of an OCF in the multi-mode stacked-switch converter, if the OCF is not addressed and there is no path for the secondary side current to circulate while delivering power to the load, the converter undergoes a drastic voltage and current pressure. In this case, while the current going through the faulty point goes down to zero, the current in the primary of the resonant tank increases dramatically.

In order to detect an OCF in the rectifier block, the switch current and the primary side current of the resonant tank can be monitored and sampled by means of a high-frequency current transformer with a ferrite core as is shown in Figure 3.18.

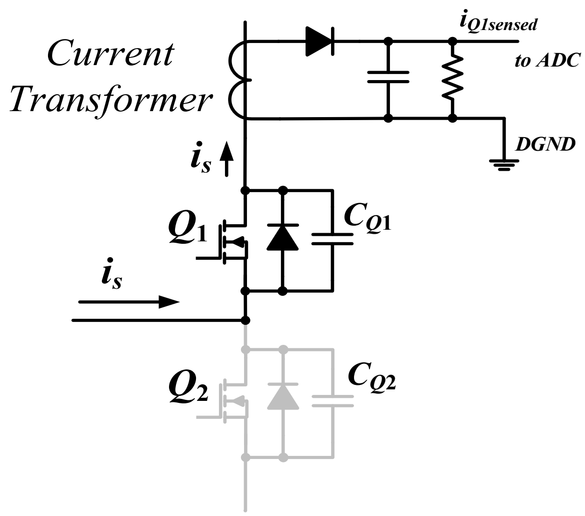


Figure 3.18- Open circuit fault detection current measurement

While the use of a high-frequency current transformer is effective in the detection of a switch OCF, it increases the cost of the overall design considering the number of the switches.

To address this issue, precision current sensing through shunt resistors can be utilized to monitor the switch current. The use of operational amplifiers and shunt resistors instead of high-frequency transformers reduces the cost but the analog circuit parameters have to be designed properly and the analog to digital conversion has to be implemented with maximized resolution. If the switch current decreases while the primary resonant current increases, the micro-controller detects that as an OCF and by taking appropriate measures, switches the operating mode accordingly (FW, HW, VD) and the converter continues to deliver the power to the load.

3.4. A Modified Multi-Mode Stacked-Switch Inverter/Rectifier Leg

In the previous section, an open-circuit fault was investigated on any of the switches in the rectifier block of the multi-mode stacked-switch bidirectional converter. The added middle switches and the extra diodes, enable the converter to continue delivering power to the load if any of the switches experience an OCF.

Yet, as demonstrated in Figure 3.19, the proposed converter resembles a 4-switch string converter in the inverting block and the middle switches are turned ON generating a unipolar

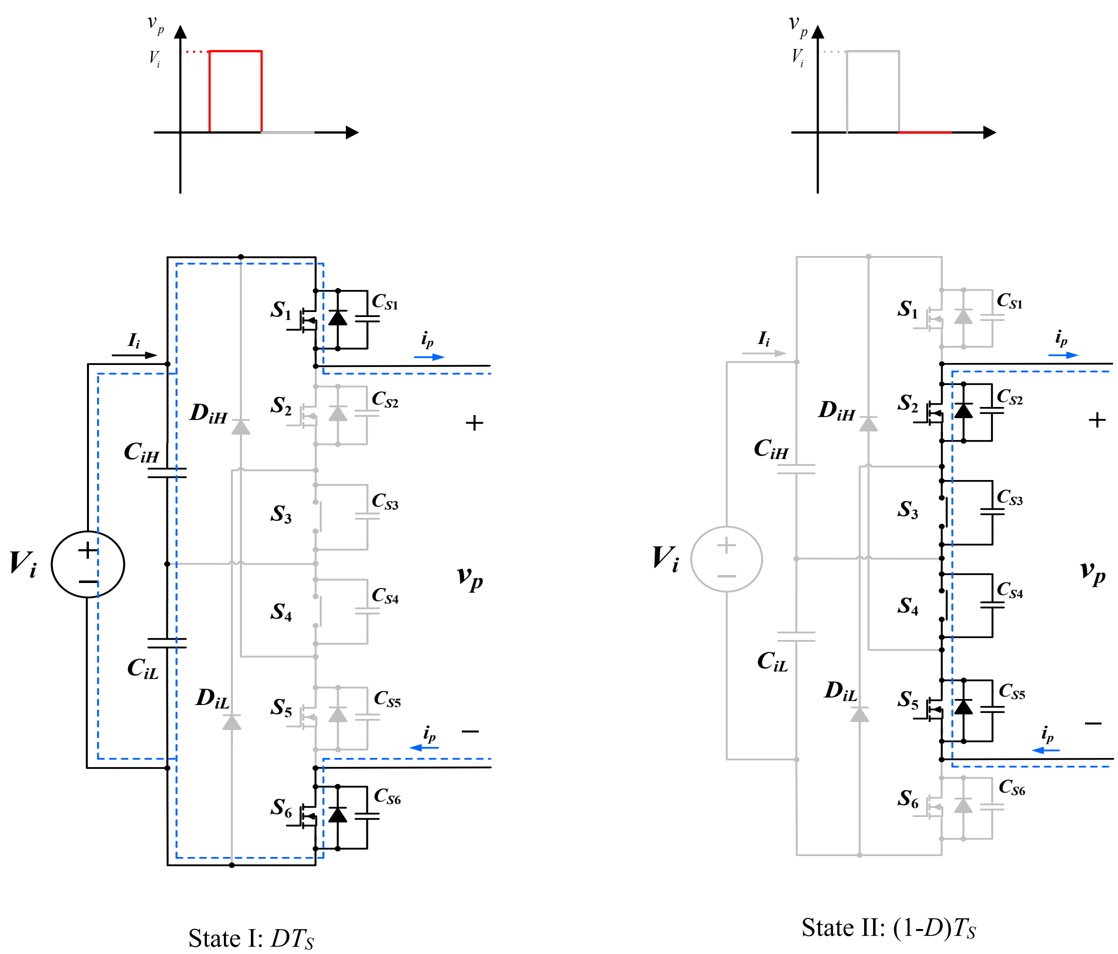


Figure 3.19- Operating states of the proposed multi-mode stacked-switch leg in inverting mode

voltage at the input terminal of the resonant tank. Hence, any OCF incident in S_1 hinders the performance of the converter and no power can be delivered to the output.

Figure 3.20 demonstrates the OCF in S_1 during DT_s time interval in the inverting block of the multi-mode stacked-switch converter. During DT_s time interval and for the positive i_p, since S_1 is open, the current passes through the body diode of S_2 (Figure 3.20a). Yet, considering the loss of S_1, only the voltage across C_L ($V_i/2$) can is applied to the primary of the resonant tank which means the converter can no longer provide full power to the load, and due to the unbalanced operation of the converter, C_H and C_L experience voltage imbalance. During DT_s time interval and for a negative i_p, in case the OCF is caused by the lifting of bond wires or due to the thermal cycling, then the whole switch will be open circuit and there will be no path for

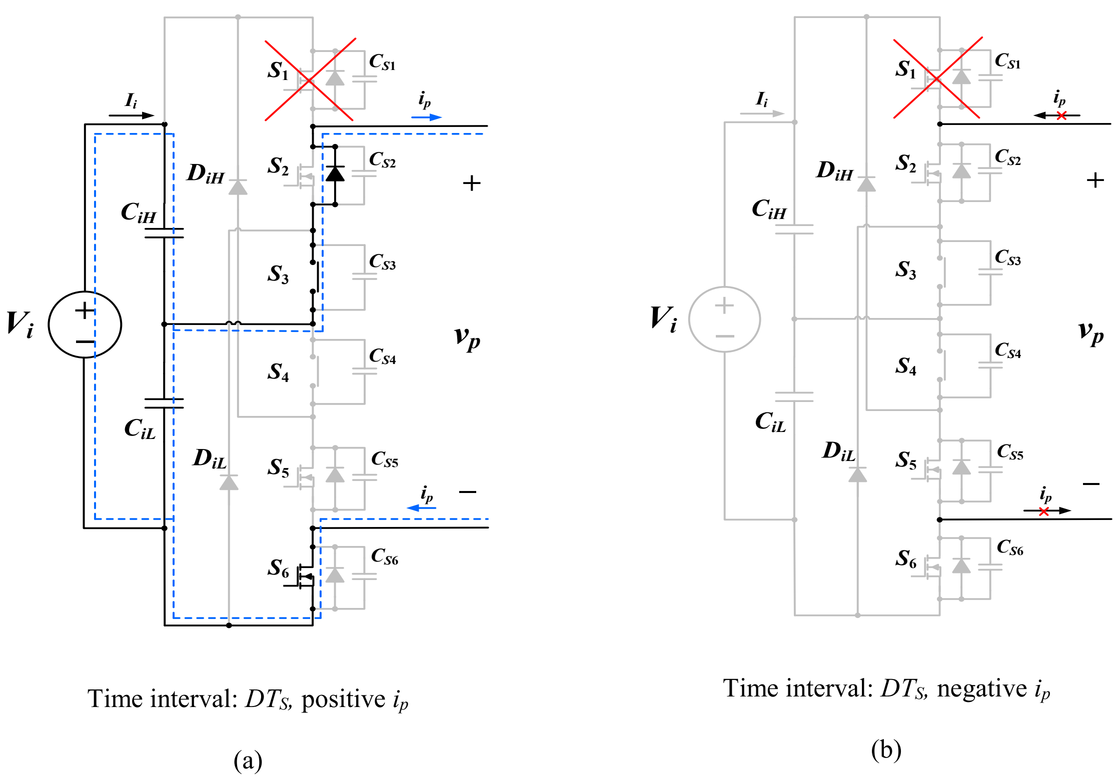
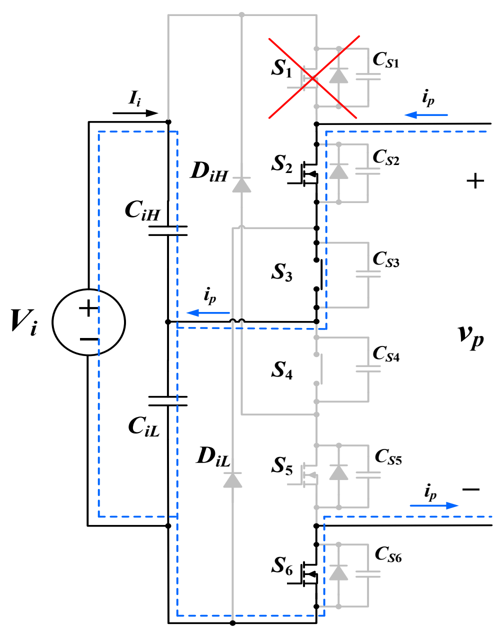


Figure 3.20- Operating states of the proposed multi-mode stacked-switch leg in inverting mode. (a) positive i_p, (b) negative i_p

the negative i_p to circulate and hence, it is forced to zero. This can lead to severe voltage spikes over the switches and may damage and cause secondary failures of other components.

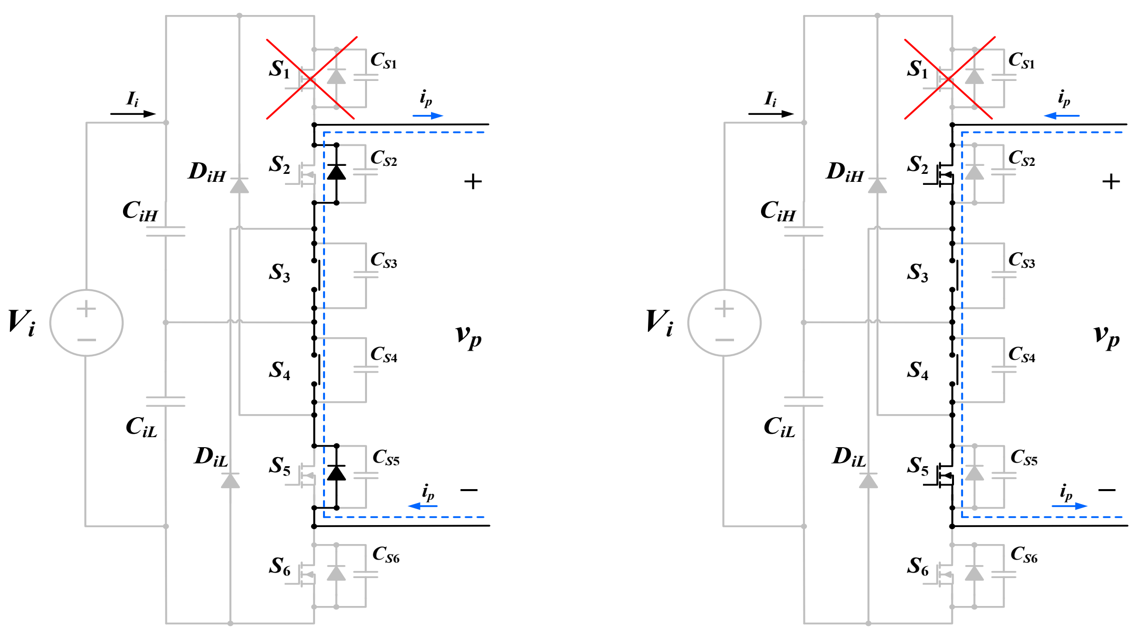
As depicted in Figure 3.21, by developing a proper fault-tolerant control in the inverting leg and turning ON S_2 right after an OCF in S_1 is detected, the unavailability of a current path for the negative i_p during DTs time interval and the consequent voltage/current spikes can be addressed. Yet the power delivery issue still exists and further measures need to be taken. Therefore, the dependency of the power delivery and the circuit transients on the OCF in S_1 has to be addressed.



Time interval: DT_S, negative i_p

Figure 3.21- Operating state of the proposed multi-mode stacked-switch leg in inverting mode for negative i_p after OCF is detected in S_1 and S_2 is turned ON

Figure 3.22 demonstrates the OCF in S_1 during $(1\text{-}D)T_s$ time interval for positive and negative i_p. During this time interval, since S_2 and S_5 are turned ON, both positive and negative i_p can circulate through the resonant tank, yet no power from the input source is delivered into the load. Therefore, the dependency of the power delivery and the circuit transients on the operating status of S_1 and other switches have to be addressed.



Time interval: $(1\text{-}D)T_S$, positive i_p

(a)

Time interval: $(1\text{-}D)T_S$, negative i_p

(b)

Figure 3.22- Operating states of the proposed multi-mode stacked-switch leg in inverting mode. (a) positive i_p, (b) negative ip

3.4.1. **Synchronous Rectification**

Physical limitations prevent the forward voltage drop of diodes from being reduced below approximately 0.3V. In contrast, the on-resistance, R_{DSON}, of MOSFETs can be lowered, either by increasing the size of the die or by paralleling discrete devices. In low voltage high power applications, this voltage drop causes significant power loss. To improve the efficiency and reduce the conduction losses of the diodes, synchronous rectification (SR) becomes necessary by replacing the diodes with actively controlled switches since employing a MOSFET in place of a diode can have a significantly smaller voltage drop at a given current than the diode.

This makes SR attractive, especially in applications sensitive to efficiency, converter size, and thermal performance, such as portable or handheld devices. In addition, semiconductor manufacturers are constantly introducing new MOSFET technologies that have lower R_{DSON} and total gate charge, (Q_G), which makes it easier to implement SR in power converter design.

The advantages of using SR in high-performance, high-power converters include better efficiency, lower power dissipation, better thermal performance, lower profile, increased quality, improved manufacturing yields through automated assembly processes (higher reliability), and inherently optimal current sharing when synchronous FETs are paralleled. Because the effective R_{DSON}, in this case, is inversely proportional to the number of paralleled devices, conduction losses are reduced. Also, the R_{DSON} has a positive temperature coefficient so the FETs will automatically tend to share current equally, facilitating optimal thermal distribution among the SR devices. As a result, to increase the efficiency of the multi-mode stacked-switch leg by means of SR, D_H, and D_L can be replaced by active switches.

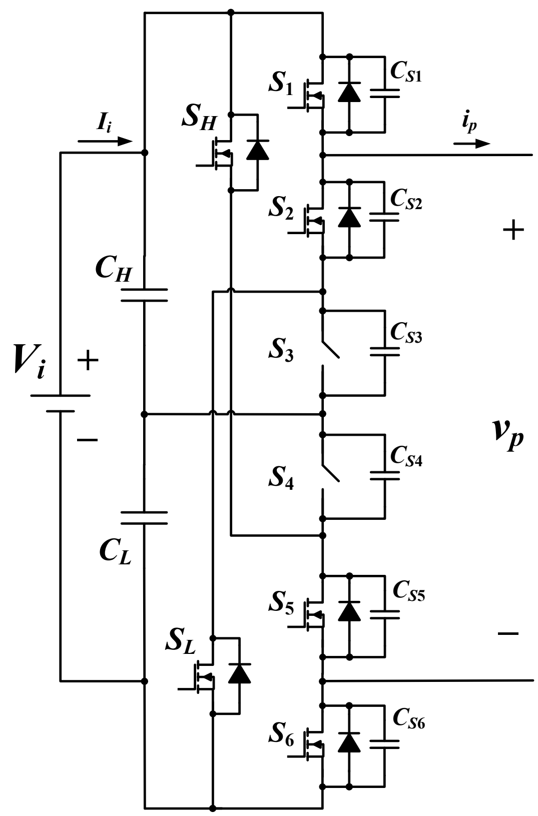


Figure 3.23- Topology of the modified stacked-switch inverter/rectifier leg

3.5. Open-Circuit Fault-Tolerant Operation of the Modified Multi-Mode Stacked-Switch Bidirectional DC/DC Converter

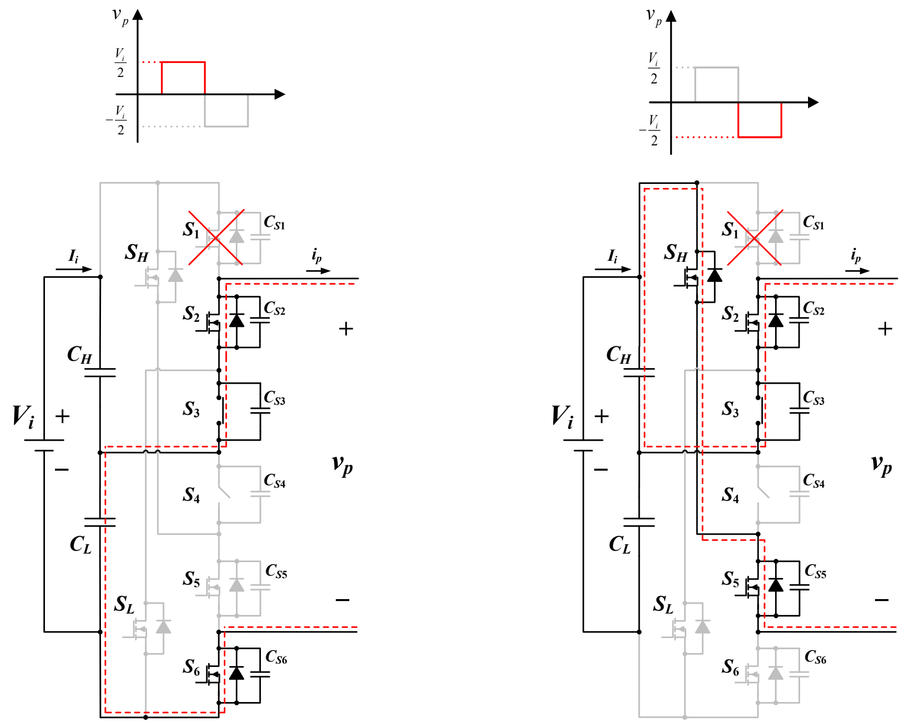
The topology of the modified multi-mode stacked-switch leg is shown in Figure 3.23. By replacing the diodes with the active switches, extra switching redundancy is added to the previously proposed converter. While during the normal operation of the converter, a unipolar voltage is generated at the input of the resonant tank, S_H and S_L enable the converter to generate a bipolar voltage by introducing a proper switching pattern to the gate-source of the switches in the inverting block.

Table 3.4 has summarized the open-circuit faults on S_1 to S_6 along with the associated switching patterns to address the incident. In Table 3.4, G_1 and G_2 indicate the proper gate signals applied to the inverting side switches operating in a complementary fashion. Figure 3.24 exhibits the alternative operating modes and the current paths to address an OCF in S_1 with a complete loss of the switch. As can be seen, after losing S_1, by turning ON S_2, the voltage at the output of the inverter is bipolar where C_L generates the positive edge and C_H delivers the power on the negative edge. As a result, the converter continues to deliver full power to the load without facing any interrupts while avoiding any voltage imbalance over C_H and C_L.

In the same manner, an OCF in S_2 can be addressed by turning ON S_1 while S_3 and S_4 are turned OFF as demonstrated in Figure 3.25. In this case, the converter continues to

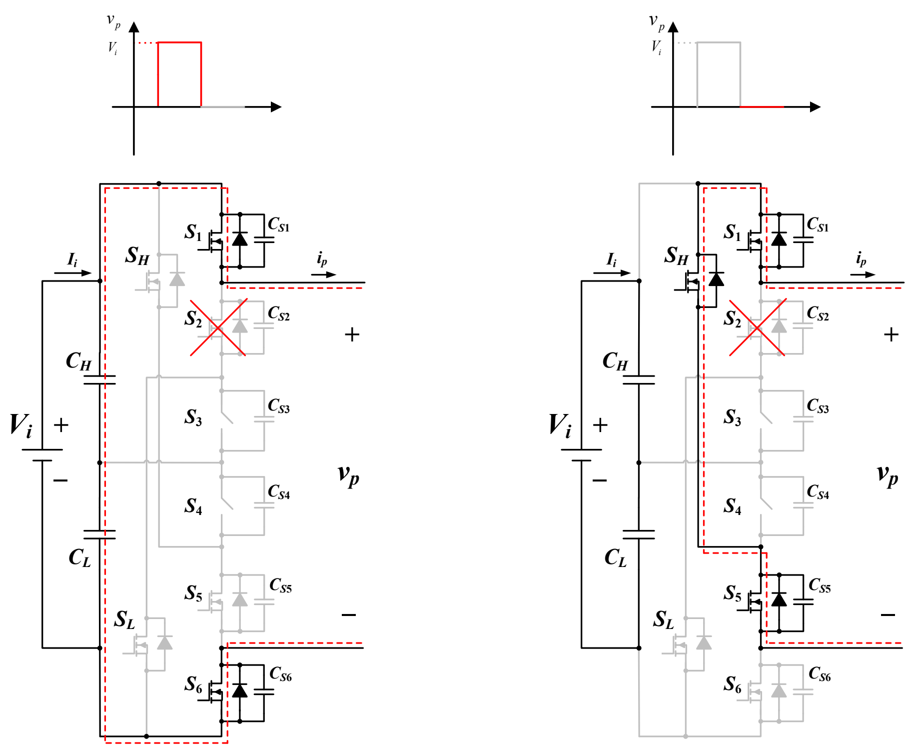
Table 3.4- Fault-tolerant switching pattern of the modified multi-mode stacked-switch inverter leg

OCF	Switching patterns							
	S_1	S_2	S_3	S_4	S_5	S_6	S_H	S_L
S_1	-	ON	ON	OFF	G_2	G_1	G_2	OFF
S_2	ON	-	OFF	OFF	G_2	G_1	G_2	OFF
S_3	ON	OFF	-	OFF	G_2	G_1	G_2	OFF
S_4	G_1	G_2	OFF	-	OFF	ON	OFF	G_2
S_5	G_1	G_2	OFF	ON	-	ON	OFF	G_2
S_6	G_1	G_2	OFF	ON	ON	-	OFF	G_2



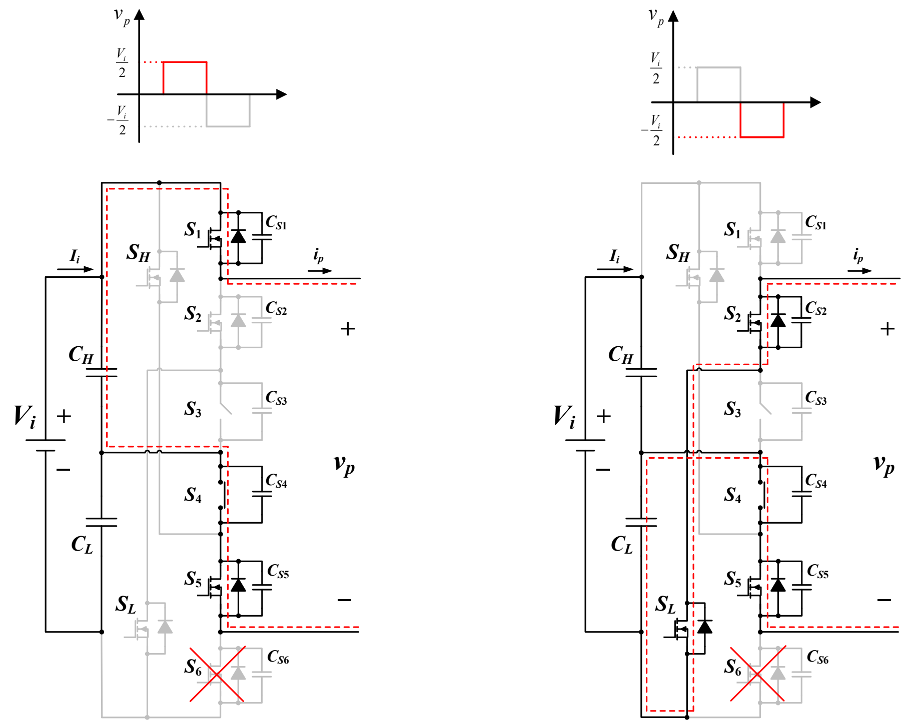
(a) (b)

Figure 3.24- Fault-tolerant operation of the multi-mode stacked-switch leg during an OCF in S_1. a) positive voltage, b) negative voltage at the output



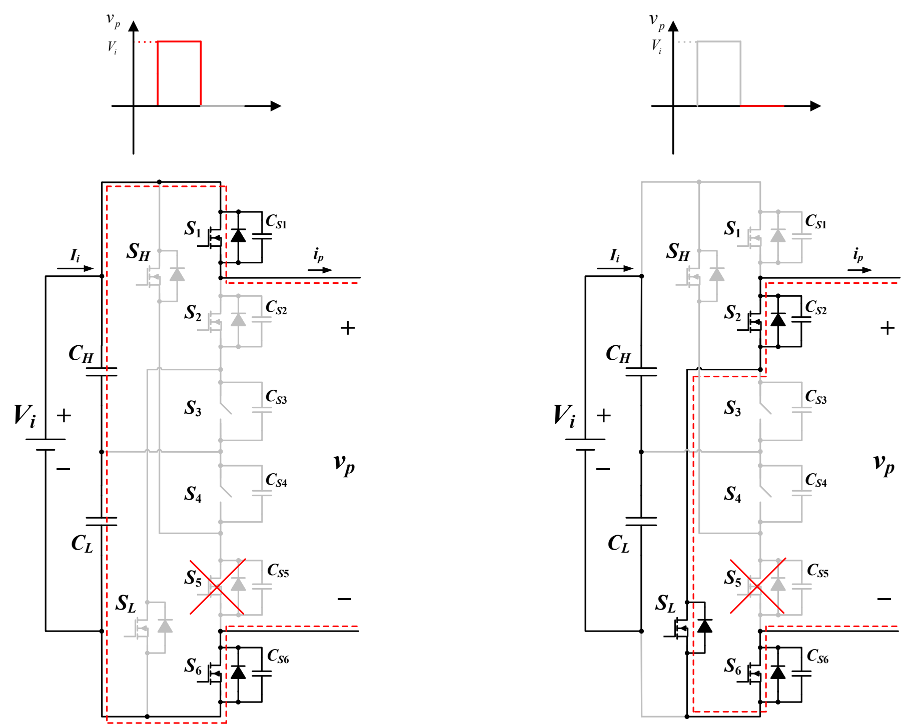
(a) (b)

Figure 3.25- Fault-tolerant operation of the multi-mode stacked-switch leg during an OCF in S_2. a) positive voltage, b) zero voltage at the output



(a) (b)

Figure 3.26- Fault-tolerant operation of the multi-mode stacked-switch leg during an OCF in S_6. a) positive voltage, b) negative voltage at the output



(a) (b)

Figure 3.27- Fault-tolerant operation of the multi-mode stacked-switch leg during an OCF in S_5. a) positive voltage, b) zero voltage at the output

generate a unipolar voltage at the input of the resonant circuit. The current in the zero voltage edge passes through S_5 and S_1 to circulate. In this mode, since C_H and C_L are charged/discharged simultaneously, no voltage imbalance is caused.

Similarly, Figure 3.26 and Figure 3.27 show the open-circuit fault-tolerant operation of the modified multi-mode stacked-switch leg with an OCF incident in S_6 and S_5 respectively.

3.6. Control Principles and Voltage Regulation Technique

The block diagram of the closed-loop control system has been shown in Figure 3.28. According to the voltage gain plot of the multi-mode stacked-switch converter demonstrated in Figure 3.17, the HW/VD curve has two peaks happening at ω_r=0.7 and ω_r =1.4. Same as in

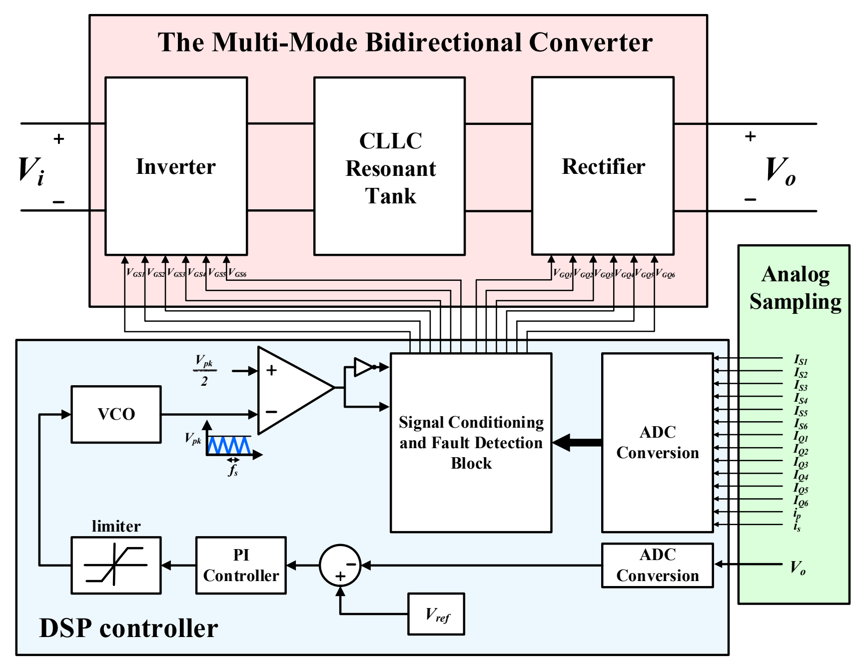


Figure 3.28- Block diagram of the fault-tolerant control system

Chapter 2, the variable frequency control technique has been utilized to regulate the output voltage. In order to make sure that the soft-switching is achieved for all the semiconductor devices, the switching frequency has to be kept above the resonant frequency. As can be seen in the FW curve in Figure 3.17 shown in blue, for the switching frequencies above the resonant frequency, as the switching frequency increases, the gain decreases, and vice versa. Therefore, in the control system, first, the output voltage of the converter is sensed and is compared with the desired value. Then, the difference (error) is fed into a PI controller. The output of the PI controller determines whether the switching frequency has to be increased or reduced to regulate the output voltage.

In the HW/VD curve, however, there is another peak at the right side of the resonant frequency. As a result, to simplify the control system and to utilize the same concept that is used in the FW control, a limiter has been placed in the output of the PI controller in HW/VD mode, preventing the switching frequency to move below the designated limit and hence ensuring soft-switching. The upper boundary of the limiter also determines when to switch from FW to HW/VD. The same limiter ensures soft-switching in both FW and HW/VD operating modes.

In addition, in order to detect and address OCFs, the currents going through each of the switches along with the primary and secondary side resonant currents are sampled and after being filtered are fed to the micro-controller through the analog sampling block. In the rectifier block, in the case, a switch current drops significantly while the primary side resonant current increases dramatically, the micro-controller detects an OCF in the corresponding switch, and the gate signals of the appropriate switching pattern based on Table 3.3 and Table 3.4 are applied to the converter to address the fault.

3.7. Results and Performance

To verify the performance of the fault-tolerant operation of the proposed scheme, experimental results have been provided on a 300 W, 250V/400V bidirectional *CLLC* resonant converter using the multi-mode stacked-switch leg in both inverter and rectifier blocks demonstrated in Figure 3.29. The base switching frequency of the converter is 100 kHz.

InfiniiVision MSOX6004A oscilloscope by Keysight Technologies was used to capture the experimental waveforms and measure the provided efficiencies. In the design of the converter, first considering the output voltage and power, the equivalent load resistance is obtained. After specifying the switching frequency range and selecting a proper quality factor from the gain curves, the values of the resonant components are obtained. The operating frequency is then decided based on the experimental curve of the converter. Considering the aforementioned parameters and assuming k=2 and m=0.39, the values for the resonant circuit components are obtained below:

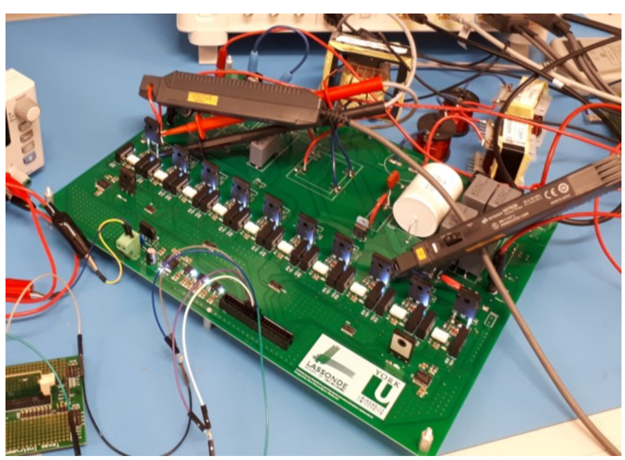


Figure 3.29- The proof-of-concept prototype hardware set-up in laboratory

$$R_L = \frac{V_o^2}{P_o} = \frac{400^2}{300} = 533\Omega \tag{3.3}$$

$$R_{ac-FW} = \frac{8}{\pi^2} \cdot R_L = 432\Omega \tag{3.4}$$

$$L_M = \frac{\mathrm{R}_{ac}}{Q \cdot 2\pi f_0} = 172\mu H \tag{3.5}$$

$$L_s = k \cdot L_M = 344\mu H \tag{3.6}$$

$$C_p = \frac{1}{L_M \omega_0^2} = 14.73nF \tag{3.7}$$

$$C_s = mC_p = 5.74nF \tag{3.8}$$

Table 3.5- Design specifications and circuit parameters

Output Power (P_o)	300 W
Output Voltage (V_o)	400 V
Input Voltage (V_i)	250 V
Magnetizing inductance (L_M)	172 µH
Secondary side resonant inductance (L_s)	344 µH
Primary side resonant capacitance (C_p)	15 nF
Secondary side resonant capacitance (C_s)	5.8 nF
Switching Frequency (f_s)	>100 kHz
Switches	SiC SCT3080KL
Added Diodes	U1560 Ultrafast Diode
Primary side snubber caps	330 pF
Secondary side snubber caps	150 pF

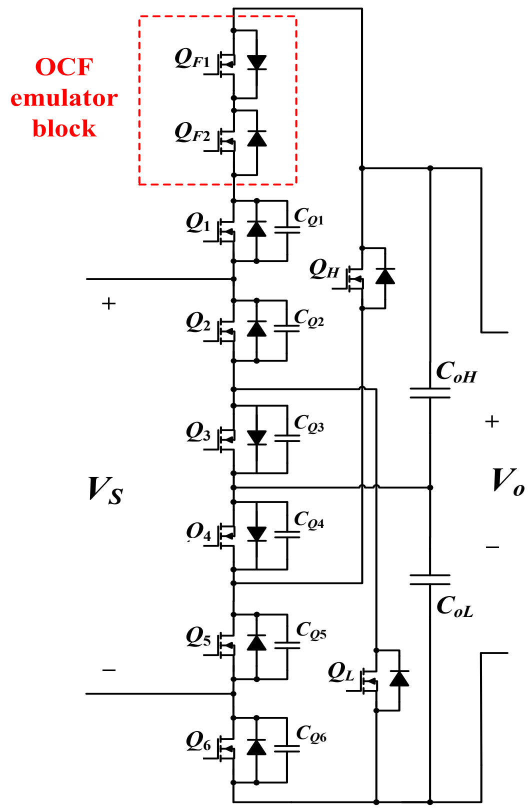


Figure 3.30- The circuit diagram of the added bidirectional MOSFETs to emulate an OCF in Q_1 in the modified multi-mode stacked-switch leg

The summary of the circuit parameters has been provided in Table 3.5. In order to emulate an open-circuit fault in a MOSFET, two back-to-back switches have been placed in series with the target MOSFET. The circuit diagram of the added back-to-back MOSFETs to emulate an OCF in Q_1 in the modified multi-mode stacked-switch leg is shown in Figure 3.30. To emulate an OCF, during normal operation of the circuit, a common active low fault signal is applied to the gates of Q_{F1} and Q_{F2}, hence prior to the OCF, the gates of Q_{F1} and Q_{F2} are high and the back-to-back switches are turned ON acting as a wire. Yet, to emulate the open-circuit fault at a given time, the active-low fault signal is set to low and Q_{F1} and Q_{F2} are turned OFF at the same time. Therefore, the body-diode of back-to-back switches prevents the current to pass through and the block acts as an open circuit.

A number of scenarios have been investigated to fully examine the performance of the fault-tolerant control system. Figure 3.31 shows the current and the drain-source voltage of S_1 in the inverting leg of the bidirectional multi-mode converter along with the output voltage during the normal operation of the converter. As can be seen, zero voltage switching (ZVS) is provided for S_1, and soft-switching is achieved. Also, near-zero current switching (ZCS) has been achieved for the converter.

Figure 3.32 depicts the waveform of the primary and secondary resonant currents along with V_o prior to an OCF. Figure 3.33 shows the waveform of the primary and secondary resonant currents, along with the output voltage during an OCF in the proposed multi-mode string converter without any fault-tolerant operation. As can be seen, i_p increases dramatically by more than 300% when the fault happens, which may severely damage the circuit. i_{S1} and V_{ds1} after the OCF are demonstrated in Figure 3.34. After the fault, V_o drops to zero, and no current is delivered to the output load.

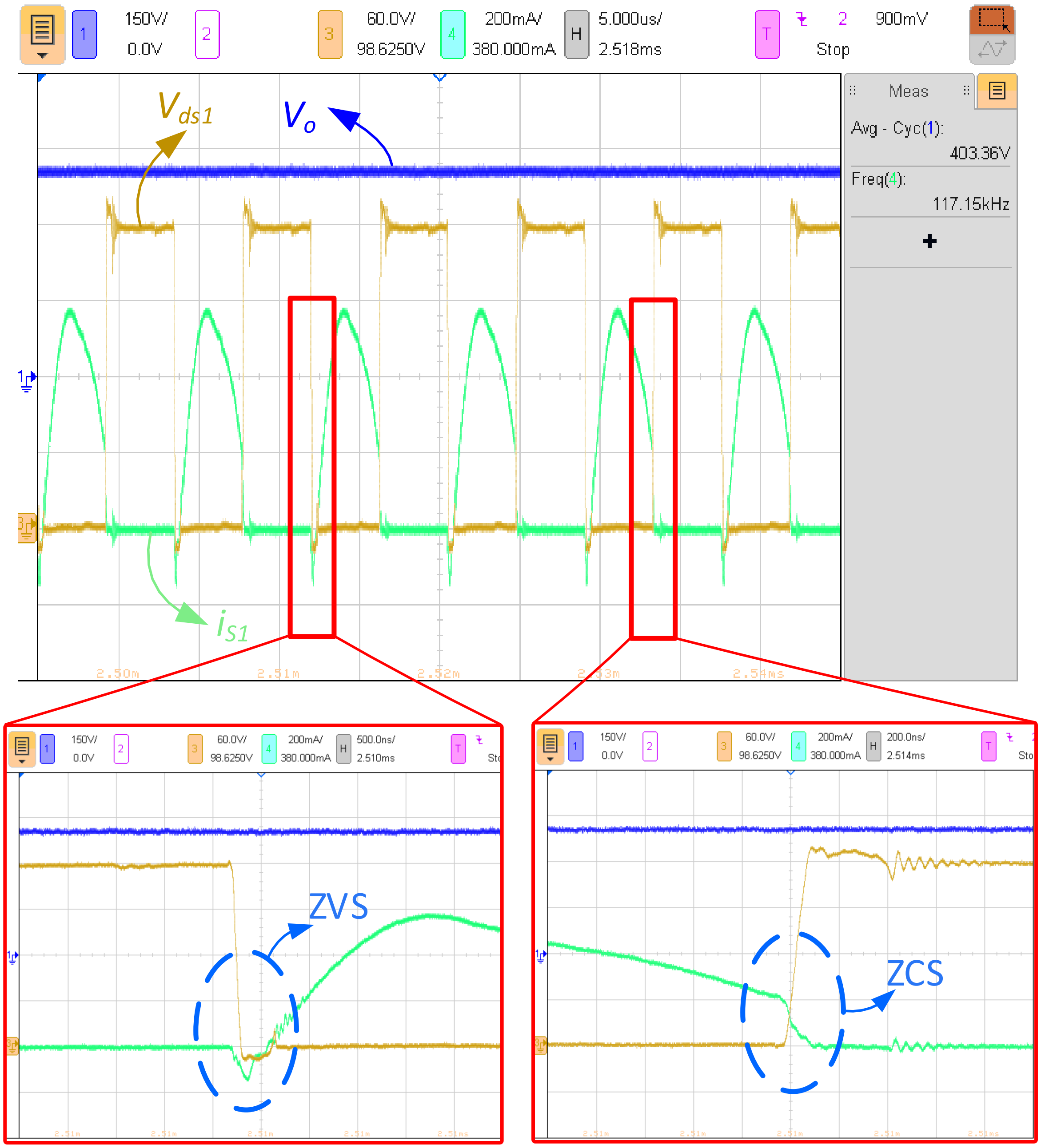


Figure 3.31- Experimental waveforms of the converter in boost mode. Output voltage and voltage and current of S_1 in the inverting block of the converter

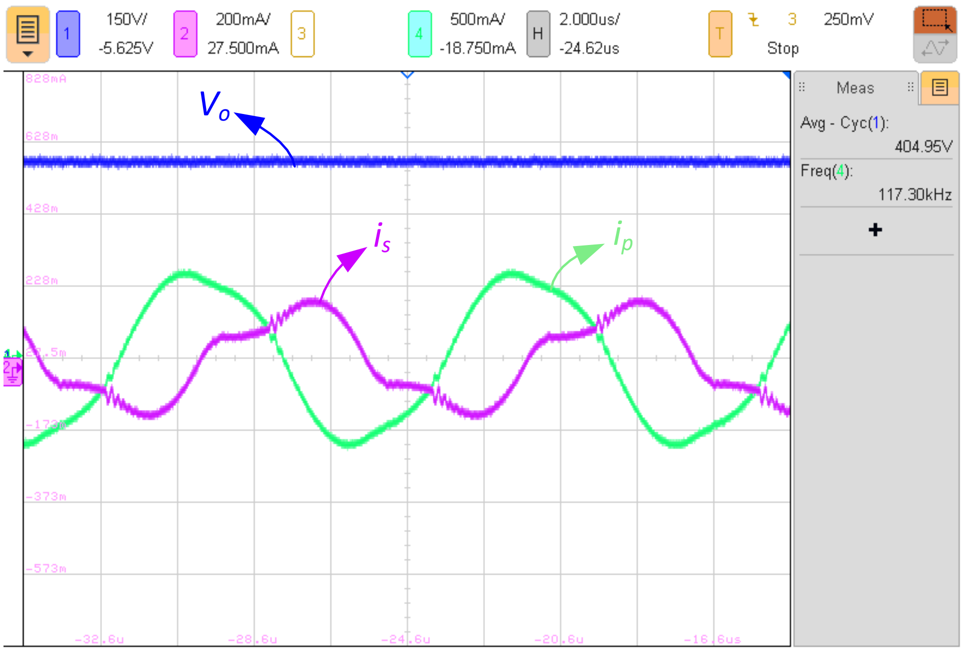


Figure 3.32- Experimental waveforms of the converter in boost mode. The output voltage and the currents in the primary and secondary side of the resonant converter

Figure 3.35 shows the partial fault-tolerant operation of the converter after an OCF in Q_1 going from FW to HW. In partial fault-tolerant control, although the appropriate switching pattern is applied, the switching frequency has not been increased. As a result, based on the voltage-gain curve of the multi-mode stacked-switch converter in boost mode provided in Figure 3.17, by keeping the frequency constant after switching from FW to HW, the operating point moves to a hard-switching area. Also, since the previous frequency on the new curve indicates a different gain, the gain of the overall converter drops. Figure 3.36 shows the zoomed-in dynamic response of the converter with the partial fault-tolerant operation. The orange waveform in Figure 3.36 demonstrates the sensed current of Q_1. As it has been shown, the sensed current drops as the switch experiences an OCF. The purple waveform in Figure 3.36 shows when the OCF has been detected. As it can be seen, the OCF has been detected in three cycles. It is clear that the operating point has moved to the hard-switching area.

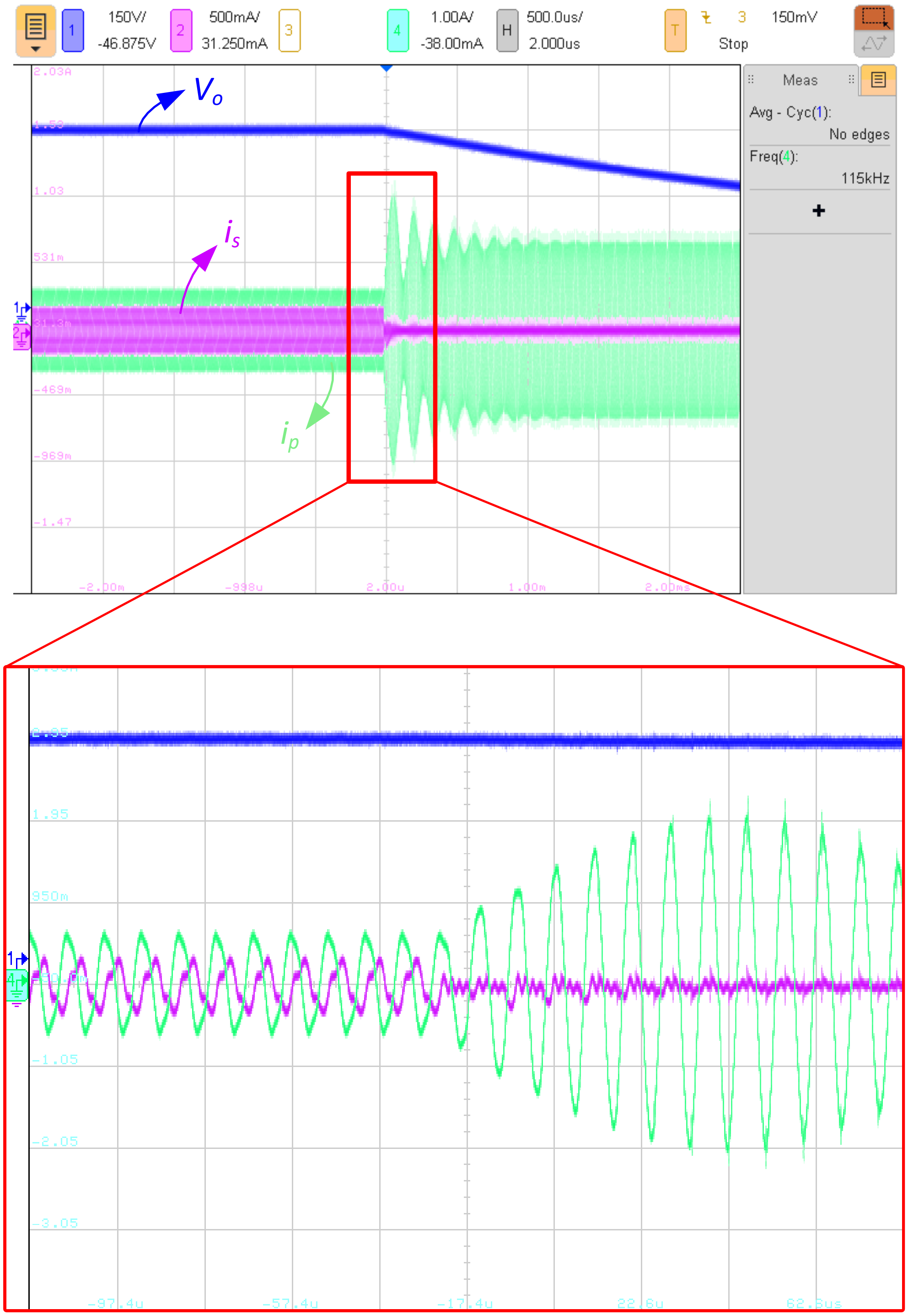


Figure 3.33- Dynamic response of the converter during OCF in boost mode. The output voltage and the currents in the primary and secondary side of the resonant converter

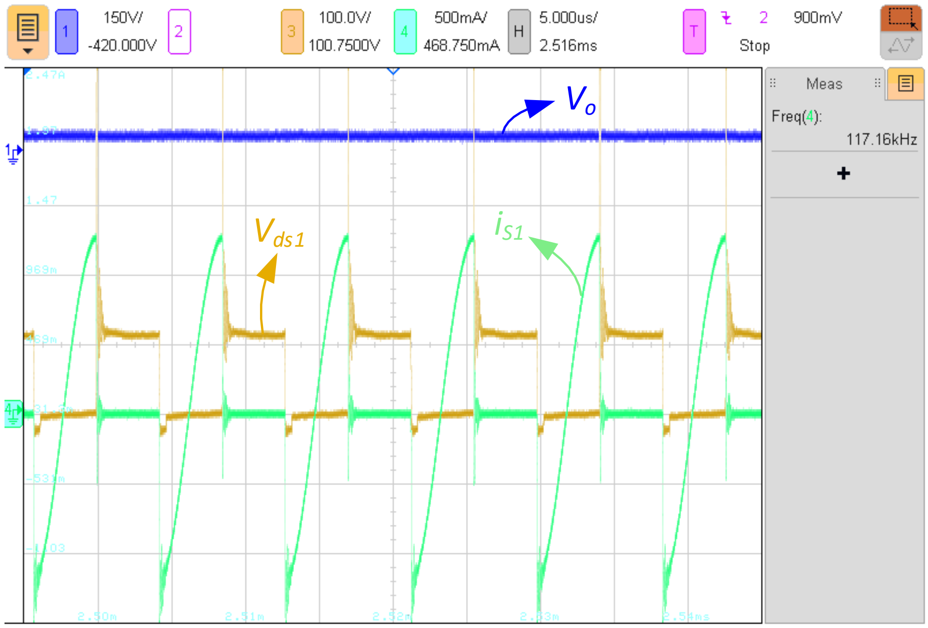


Figure 3.34- Post OCF experimental waveforms of the converter in boost mode. The output voltage and the voltage and current of S_1 without fault-tolerant control

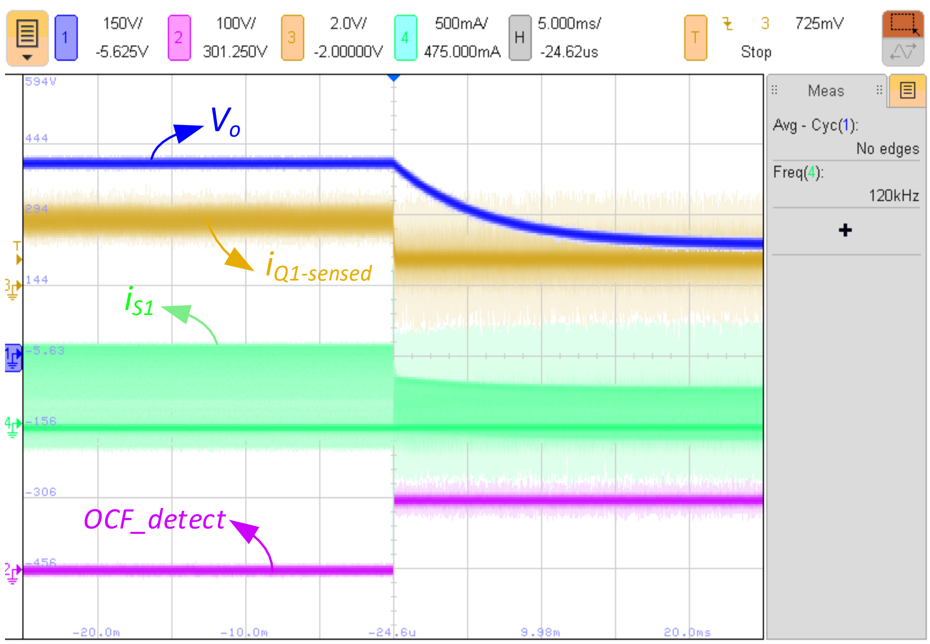


Figure 3.35- Dynamic response of the converter during OCF in boost mode with partial fault-tolerant control

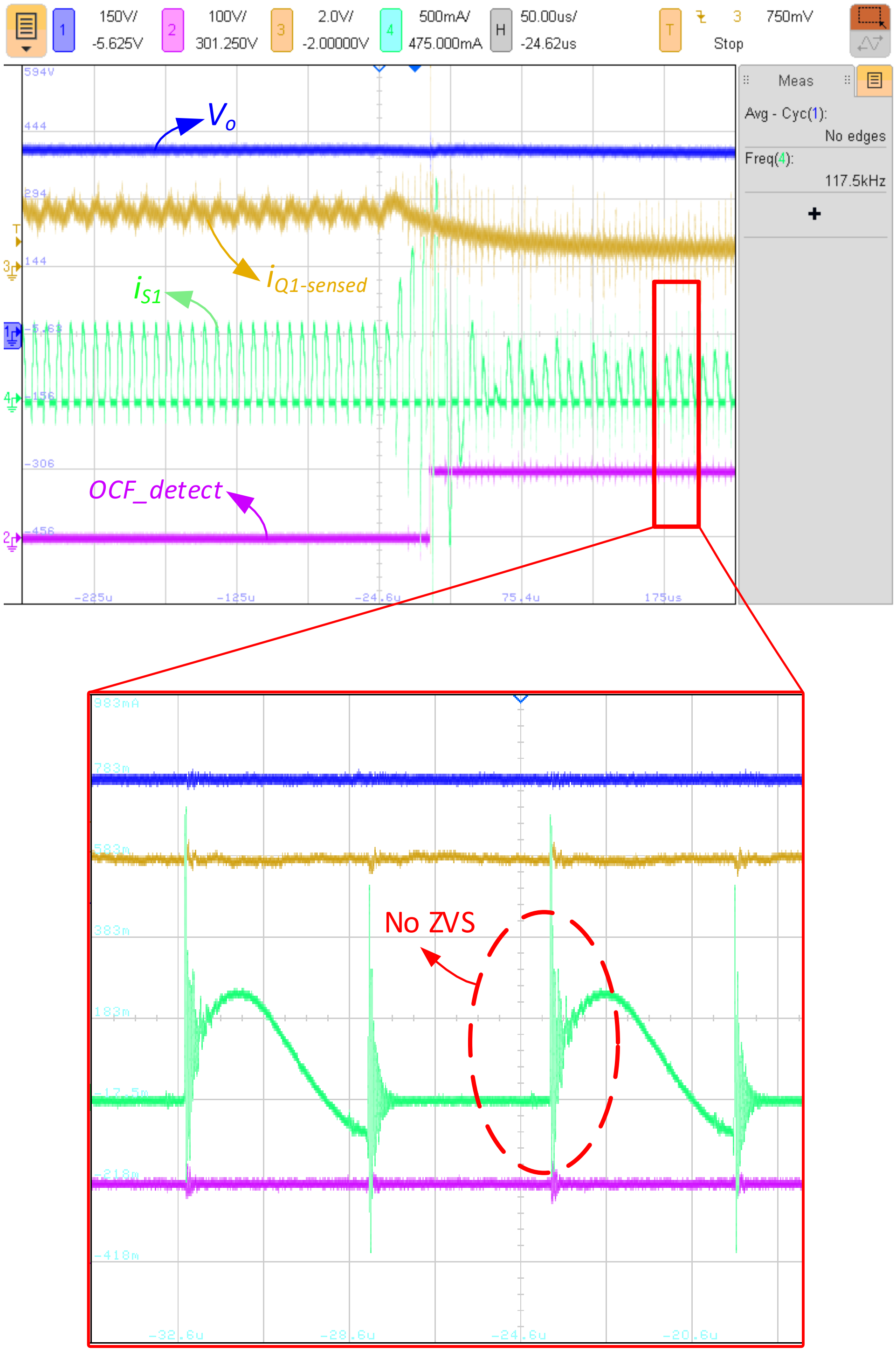


Figure 3.36- Zoomed-in snapshot of the dynamic response of the converter during OCF in boost mode with partial fault-tolerant control

Figure 3.37 shows the dynamic response of the converter with full fault-tolerant control. As can be seen, by proper detection of the OCF, i_{S1} has been limited and was avoided reaching its peak value in Figure 3.33. Also, the closed-loop variable frequency control was capable of regulating the output voltage with OCF occurred. The zoomed-in snapshot of the switching waveforms during an OCF in Q_1 has been shown in Figure 3.38. The OCF has been detected after two cycles. The purple waveform shows when the transition has taken place. As can be seen, the control system increased the switching frequency from 117 kHz to 155 kHz to regulate the output voltage at 400V, with ZVS turn-ON achieved during the entire dynamic change in operation.

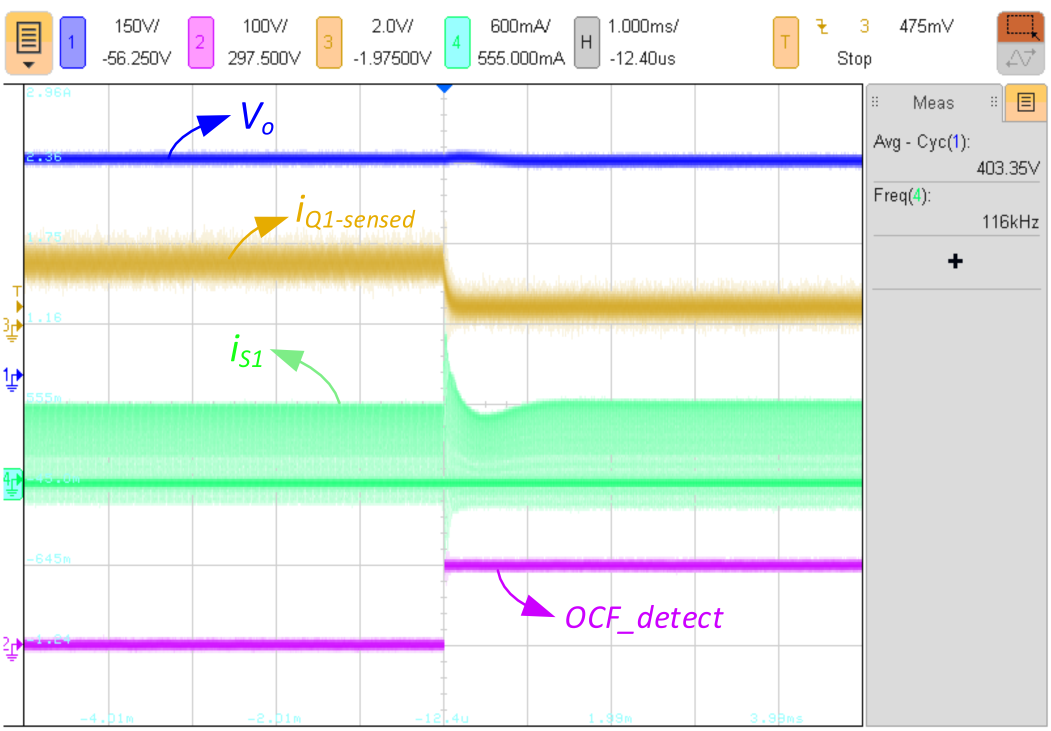


Figure 3.37- Post OCF experimental waveforms of the converter in boost mode. The output voltage and the voltage and current of S1 with fault-tolerant control

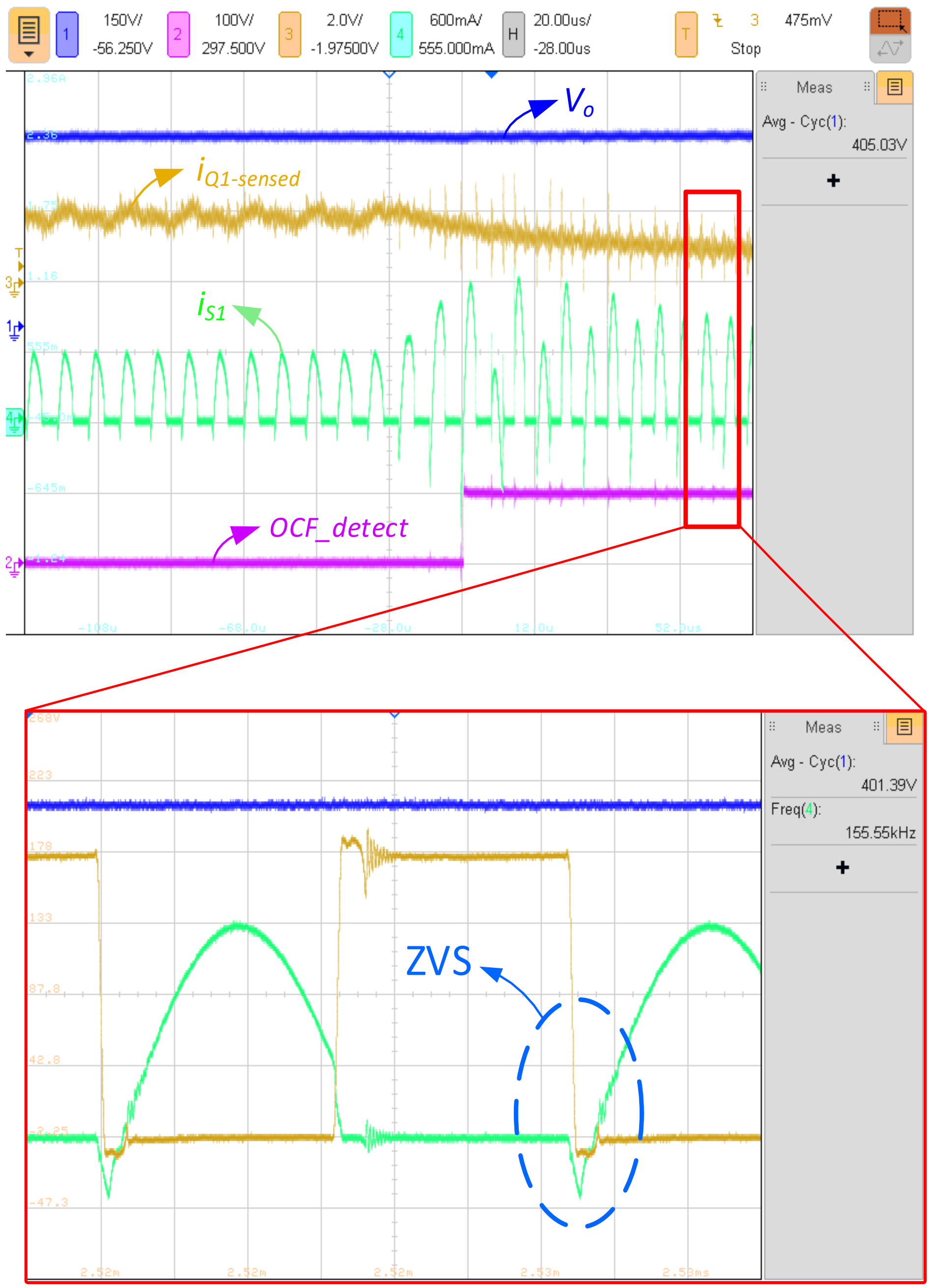


Figure 3.38- Zoomed-in snapshot of the dynamic response of the converter during OCF in boost mode with fault-tolerant control

Figure 3.39 shows the voltage stress and current going through Q_1 prior to and during the OCF with fault-tolerant control. It can be observed that i_{Q1} drops to zero but the output voltage stays constant all the time.

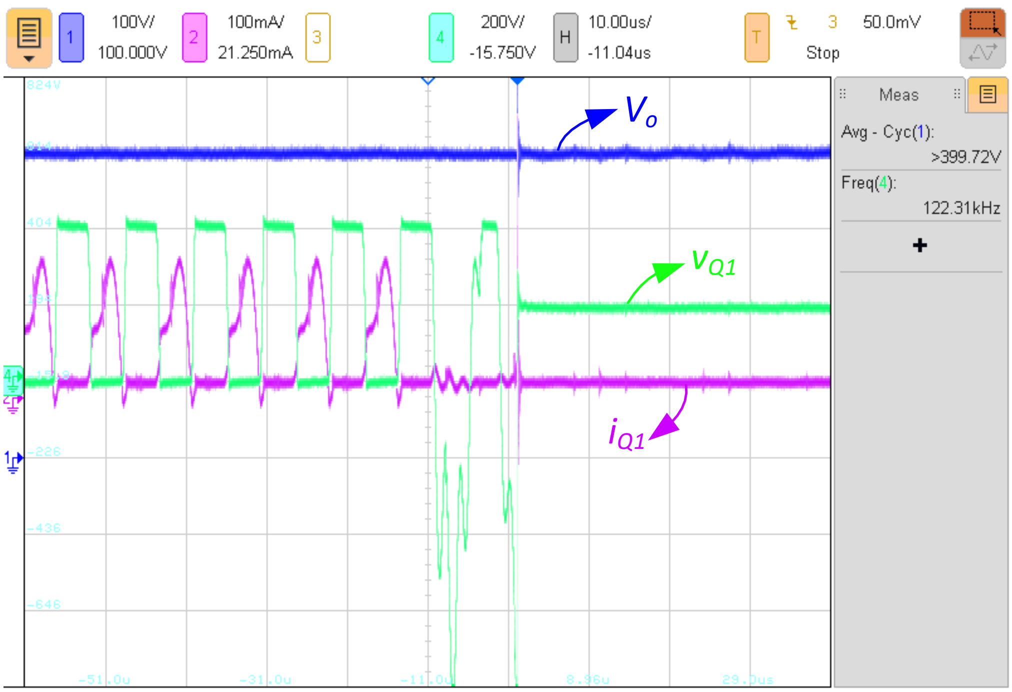


Figure 3.39- The output voltage and the voltage and current of Q_1 prior to and during the OCF with fault-tolerant control

As can be seen, by means of the developed fault-tolerant control, in the case of an open-circuit fault in any of the switches, the fault can be addressed after detection and the converter can continue to deliver power to the load without interruption.

3.8. Chapter Summary

In this chapter, first, the open-circuit fault on any of the switches in the rectifier block of the multi-mode stacked-switch converter is investigated and analyzed in detail. It is demonstrated that in the case of an OCF in any of the switches, the switch current drops while the primary side resonant current increases dramatically which drastically impacts the performance of the converter and imposes voltage and current stress over the semiconductor devices and the circuit components. Yet, it is shown that the proposed novel fault-tolerant control through the built-in circuit redundancy operation of the presented multi-mode stacked-switch rectifier leg, enables post fault operation of the converter and allows it to continue delivering the demanded load power with soft-switching operation in case any switch experiences an open-circuit fault.

In the inverter leg, however, due to the nature of the proposed multi-mode stacked-switch leg, in the case of an OCF in the top or the bottom switch, the converter is not able to continue generating a unipolar voltage at the input of the resonant tank. Consequently, the output voltage drops significantly and the converter fails to deliver continuous power to the load. In order to address the OCF in the inverter block a modified multi-mode stacked-switch leg is presented. In the proposed modified structure, the diodes have been replaced by active switches to introduce additional switching redundancy and to provide open-circuit fault-tolerant control in the inverter leg while improving the efficiency by means of synchronous rectification.

In addition to the fault-tolerant control, the provided built-in circuit redundancy of the leg allows the converter to operate in different operating modes, resulting in an enhanced control in regulating the output voltage while avoiding the switching frequency to diverge far from the resonant frequency, leading to better performance and improved efficiency with the complete soft-switching operation before and after the fault.

In the final section, to verify the performance of the proposed fault-tolerant control, and to highlight the merits of the proposed modified multi-mode stacked-switch leg, a 300W, >100kHz, 250V/400V proof-of-concept prototype is designed and implemented. The provided experimental results demonstrate that the proposed open-circuit fault-tolerant control is able to successfully address the fault while providing zero voltage switching (ZVS) turn-ON and zero current switching (ZCS) turn-OFF for all of the semiconductor devices.

Chapter 4. A Comprehensive Control System in the Multi-Mode Stacked-Switch Bidirectional DC/DC Converter

As mentioned in the previous chapters, resonant converters are widely used in various applications due to their several advantages including their high power density, high efficiency, high operating frequency, and low electromagnetic interference (EMI) [94], [95]. The closer the converter operates in the vicinity of the resonant frequency, the higher efficiency is achieved. Output voltage regulation and achieving a linear efficiency for different loading conditions while simultaneously addressing the unbalanced voltage distribution over the link capacitors stay among the challenges in the design of bidirectional converters.

This chapter focuses on the development of a comprehensive control scheme with different modes of operation to regulate the output voltage in a bidirectional converter that employs a multi-mode stacked-switch inverter/rectifier leg while simultaneously providing voltage balancing across all the DC-link capacitors.

First, a novel comprehensive hybrid control system based on the circuit redundancy in the multi-mode stacked-switch converter is proposed. With the developed built-in circuit redundancy and by using a hybrid control, the gain range is widely extended for various loading conditions with a narrow switching frequency range while the voltage stress over the DC-link capacitors is equally distributed. In the final section, experimental results are provided to investigate the performance of the proposed comprehensive control system.

4.1. Analysis and Modeling of the Proposed Converter with a *CLLC* Resonant Circuit

The general equivalent model structure of a *CLLC* resonant converter is demonstrated in Figure 4.1 [96]. A quasi-square wave voltage v_1 is generated at the input terminal of the resonant circuit. In Figure 4.1, a symmetrical *CLLC* resonant converter is utilized. The rectifier block is represented by switch Q. When $i_s>0$, Q is located at the position of "1" and when $i_s<0$, Q is located at "2". $|i_s|$ represents the rectified current in the rectifying block. The nonlinear state equations can be written as follows.

$$L_p \frac{di_p}{dt} + v_{cp} + L_m \frac{d(i_p - \frac{i_s}{n})}{dt} = v_1 \tag{4.1}$$

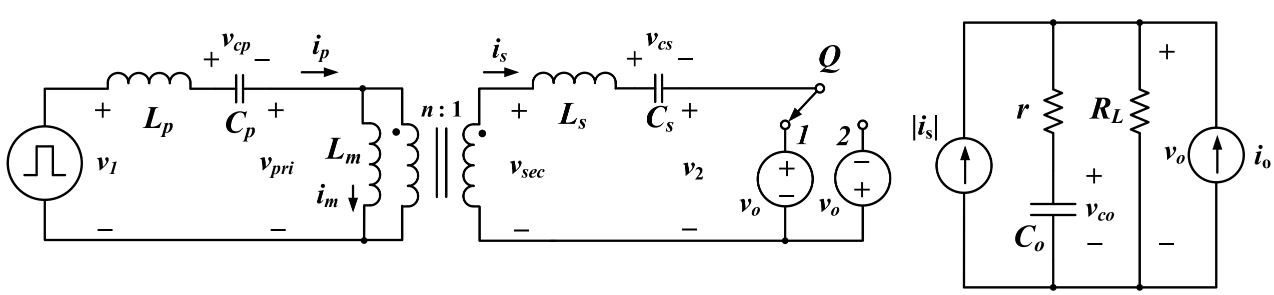


Figure 4.1- General equivalent model structure of a *CLLC* resonant converter

$$L_m \frac{d(i_p - \frac{i_s}{n})}{dt} \cdot \frac{1}{n} = L_s \frac{di_s}{dt} + v_{cs} + \mathrm{sgn}(i_s) \cdot v_o \tag{4.2}$$

$$i_p = C_p \frac{dv_{cp}}{dt} \tag{4.3}$$

$$i_s = C_s \frac{dv_{cs}}{dt} \tag{4.4}$$

In the above equations, i_p, i_s, v_{cp}, v_{cs}, and v_{co} are the state variables and $sgn(i_2)$ is the symbolic function modeling the behavior of the rectifying block at the secondary terminal of the resonant tank. The nonlinear output equation can be written as follows where v_i and i_i is the input voltage and current of the converter, and R_{eq} is the equivalent resistance of the rectifier network.

$$(1 + \frac{r}{R_L})C_o \frac{dv_{co}}{dt} + \frac{v_{co}}{R_L} = |i_s| + i_o \tag{4.5}$$

$$v_o = \mathrm{R}_{eq}(|i_s| + i_o) + \frac{\mathrm{R}_{eq}}{r} v_{co} \tag{4.6}$$

$$i_i = \frac{1}{T_s} \int_0^{T_s} i_p \frac{v_1(t)}{v_i(t)} dt \tag{4.7}$$

a) Large-Signal Model of the *CLLC* Resonant Converter

The state variables in Figure 4.1 can be approximated as a fundamental component as provided in (4.8) to (4.11).

$$i_p = i_{ps}(t)\sin\omega_s t + i_{pc}(t)\cos\omega_s t \tag{4.8}$$

$$i_s = i_{ss}(t)\sin\omega_s t + i_{sc}(t)\cos\omega_s t \tag{4.9}$$

$$v_{cp} = v_{cps}(t)\sin\omega_s t + v_{cpc}(t)\cos\omega_s t \tag{4.10}$$

$$v_{cs} = v_{css}(t)\sin\omega_s t + v_{csc}(t)\cos\omega_s t \tag{4.11}$$

The derivative expressions of (4.8) to (4.11) are obtained in (4.12) to (4.16).

$$\frac{di_p}{dt} = (\frac{di_{ps}}{dt} - i_{pc}\omega_s)\sin\omega_s t + (\frac{di_{pc}}{dt} + i_{ps}\omega_s)\cos\omega_s t \tag{4.12}$$

$$\frac{di_s}{dt} = (\frac{di_{ss}}{dt} - i_{sc}\omega_s)\sin\omega_s t + (\frac{di_{sc}}{dt} + i_{ss}\omega_s)\cos\omega_s t \tag{4.13}$$

$$\frac{dv_{cp}}{dt} = (\frac{dv_{cps}}{dt} - v_{cpc}\omega_s)\sin\omega_s t + (\frac{dv_{cpc}}{dt} + v_{cps}\omega_s)\cos\omega_s t \tag{4.14}$$

$$\frac{dv_{cs}}{dt} = (\frac{dv_{css}}{dt} - v_{csc}\omega_s)\sin\omega_s t + (\frac{dv_{csc}}{dt} + v_{css}\omega_s)\cos\omega_s t \tag{4.15}$$

$$\frac{di_m}{dt} = (\frac{di_{ms}}{dt} - i_{mc}\omega_s)\sin\omega_s t + (\frac{di_{mc}}{dt} + i_{ms}\omega_s)\cos\omega_s t \tag{4.16}$$

In the proposed bidirectional converter, both inverter and rectifier blocks are non-linear. As a result, in order to model the converter, the nonlinear terms can be approximated by the extended description function to linearize the equations. By obtaining the Fourier series of v_1 and considering the fundamental component, v_1 can be written as below.

$$v_1 \approx \frac{2v_i}{\pi}\sin(\frac{\pi}{2}d)\sin\omega_s t \tag{4.17}$$

With the same approach, the *sgn* function can be approximated by (4.18).

$$\operatorname{sgn}(i_s)\cdot v_o \approx \frac{4}{\pi}\cdot\frac{i_{ss}}{i_{sp}}v_o\sin\omega_s t + \frac{4}{\pi}\cdot\frac{i_{sc}}{i_{sp}}v_o\cos\omega_s t \tag{4.18}$$

Where i_{sp} is:

$$i_{sp} = \sqrt{i_{ss}^2 + i_{sc}^2} \tag{4.19}$$

In Figure 4.1, $|i_p\text{-}i_m|$ is the secondary side current of the resonant circuit, and the rectified current going through the load can be approximated as given in (4.20).

$$|i_s| \approx \frac{2}{\pi}\cdot i_p \tag{4.20}$$

Since the input current of the converter is DC, i_i can be approximated by (4.21).

$$i_i \approx \frac{2}{\pi}i_{ps}\sin(\frac{\pi}{2}d) \tag{4.21}$$

Using (4.8) to (4.21) and bringing them into (4.1) to (4.7), the state equations can be written as below.

$$K_2\frac{di_{ps}}{dt} - K_2 i_{pc}\omega_s + v_{cps} + K_4 v_{css} = \frac{2}{\pi}\sin(\frac{\pi}{2}d)\cdot v_i - K_6\frac{i_{ss}}{i_{sp}}\cdot v_o \tag{4.22}$$

$$K_2\frac{di_{pc}}{dt} + K_2 i_{ps}\omega_s + v_{cpc} + K_4 v_{\mathrm{csc}} = -K_6\frac{i_{sc}}{i_{sp}}v_o \tag{4.23}$$

$$K_1\frac{di_{ss}}{dt} - K_1 i_{sc}\omega_s + v_{cps} + K_3 v_{css} = \frac{2}{\pi}\sin(\frac{\pi}{2}d)\cdot v_i - K_5\frac{i_{ss}}{i_{sp}}v_o \tag{4.24}$$

$$K_1 \frac{di_{sc}}{dt} + K_1 i_{ss}\omega_s + v_{cpc} + K_3 v_{\mathrm{csc}} = -K_5 \frac{i_{sc}}{i_{sp}} v_o \tag{4.25}$$

$$C_p \frac{dv_{cps}}{dt} = C_p v_{cpc}\omega_s + i_{ps} \tag{4.26}$$

$$C_p \frac{dv_{cpc}}{dt} = -C_p v_{cps}\omega_s + i_{pc} \tag{4.27}$$

$$C_s \frac{dv_{css}}{dt} = C_s v_{csc}\omega_s + i_{ss} \tag{4.28}$$

$$C_s \frac{dv_{\mathrm{csc}}}{dt} = -C_s v_{css}\omega_s + i_{sc} \tag{4.29}$$

The output equations are obtained by (4.30) to (4.32).

$$C_o \frac{dv_{co}}{dt} \cdot r + v_{co} = v_o \tag{4.30}$$

$$v_o = v_{co} \frac{R_L}{(R_L + r)} + \frac{2R_L r}{\pi(R_L + r)} n i_p + \frac{R_L r}{(R_L + r)} i_o \tag{4.31}$$

$$i_i = \frac{2}{\pi}\sin(\frac{\pi}{2}d) i_{ps} \tag{4.32}$$

After the resonant converter reaches the steady-state, the operating point of the converter can be obtained by circuit parameters (e.g. V_i, I_o, R, D, Ω_s). In the steady-state, the derivative terms become zero, and (4.22) to (4.29) turn into the below equations. (4.33) to (4.45) represent the large-signal model of the *CLLC* resonant converter.

$$-K_1 I_{sc}\Omega_s + V_{cps} + K_3 V_{css} = V_e - \frac{4}{\pi} K_3 K_5 I_{ss} \tag{4.33}$$

$$K_1 I_{ss}\Omega_s + V_{cpc} + K_3 V_{\mathrm{csc}} = -\frac{4}{\pi} K_3 K_5 I_{sc} \tag{4.34}$$

$$-K_2 I_{pc}\Omega_s + V_{cps} + K_4 V_{css} = V_e - \frac{4}{\pi} K_4 K_5 I_{ss} \tag{4.35}$$

$$-K_2 I_{ps}\Omega_s + V_{cpc} + K_4 V_{\mathrm{csc}} = -\frac{4}{\pi} K_4 K_5 I_{sc} \tag{4.36}$$

$$-C_p V_{cpc}\Omega_s = I_{ps} \tag{4.37}$$

$$C_p V_{cps}\Omega_s = I_{pc} \tag{4.38}$$

$$-C_s V_{csc}\Omega_s = I_{ss} \tag{4.39}$$

$$C_s V_{css}\Omega_s = I_{sc} \tag{4.40}$$

$$V_o = \frac{2}{\pi} I_p R_L \tag{4.41}$$

$$I_i = \frac{2}{\pi} I_{ps} \sin(\frac{\pi}{2} D) \tag{4.42}$$

By assuming a duty ratio (D) of 0.5, the gain of the resonant tank as a function of the switching frequency can be obtained by (4.43) to (4.45).

$$M = \frac{V_o}{V_i} = \frac{f_n^3}{\sqrt{A^2 Q^2 + f_n^2 B^2}} \tag{4.43}$$

$$A = -f_n^4\left(2 + \frac{1}{L_n}\right) + 2 f_n^2\left(1 + \frac{1}{L_n}\right) - \frac{1}{L_n} \tag{4.44}$$

$$B = f_n^2\left(1+\frac{1}{L_n}\right)-\frac{1}{L_n} \tag{4.45}$$

The parameters of the large-signal and small-signal model of the *CLLC* resonant converter in (4.33) to (4.42) are provided in (4.46) to (4.66).

$$L_{e1} = L_p + L_m \tag{4.46}$$

$$L_{e2} = \frac{L_m}{n} + n \cdot L_s \tag{4.47}$$

$$R_{eq} = R_L \parallel r \tag{4.48}$$

$$K_1 = \frac{L_{e1}L_{e2}}{L_m} - \frac{L_m}{n} \tag{4.49}$$

$$K_2 = L_{e1} - \frac{L_m^2}{nL_{e2}} \tag{4.50}$$

$$K_3 = \frac{nL_{e1}}{L_m} \tag{4.51}$$

$$K_4 = \frac{L_m}{L_{e2}} \tag{4.52}$$

$$K_5 = \frac{2}{\pi}R_L \tag{4.53}$$

$$K_6 = K_1\Omega_s - \frac{K_3}{C_s\Omega_s} \tag{4.54}$$

$$K_7 = K_2\Omega_s - \frac{1}{C_p\Omega_s} \tag{4.55}$$

$$q_1 = \frac{4V_o}{\pi I_{sp}}\left(1-\frac{I_{ss}^2}{I_{sp}^2}\right) \tag{4.56}$$

$$q_2 = \frac{4V_o I_{ss} I_{sc}}{\pi I_{sp}^3} \tag{4.57}$$

$$q_3 = \frac{4I_{ss}}{\pi I_{sp}} \tag{4.58}$$

$$q_4 = \frac{4V_o}{\pi I_{sp}}\left(1 - \frac{I_{sc}^2}{I_{sp}^2}\right) \tag{4.59}$$

$$q_5 = \frac{4I_{sc}}{\pi I_{sp}} \tag{4.60}$$

$$q_6 = \frac{2I_{ss}}{\pi I_{sp}} \tag{4.61}$$

$$q_7 = \frac{2I_{sc}}{\pi I_{sp}} \tag{4.62}$$

$$E_d = 2V_i \cos\left(\frac{\pi}{2}D\right) \tag{4.63}$$

$$K_v = \frac{4}{\pi}\sin\left(\frac{\pi}{2}D\right) \tag{4.64}$$

$$J_d = I_{ps}\cos\left(\frac{\pi}{2}D\right) \tag{4.65}$$

$$J_i = \frac{2}{\pi}\sin\left(\frac{\pi}{2}D\right) \tag{4.66}$$

b) Small-Signal Model of the *CLLC* Resonant Converter

By applying a small-signal perturbation to the circuit parameters (e.g. $v_i = V_i + \hat{v}_i$, $i_o = I_o + \hat{i}_o$, $d = D + \hat{d}$ and $\omega_s = \Omega_s + \hat{\omega}_s$) and linearizing the equations, the small-signal mathematical state model of the converter can be obtained as below.

$$\frac{d\hat{i}_{ps}}{dt} = \Omega_s \hat{i}_{pc} - \frac{K_4 q_1}{K_2}\hat{i}_{ss} + \frac{K_4 q_2}{K_2}\hat{i}_{sc} - \frac{1}{K2}\hat{v}_{cps} - \frac{K_v}{K_2}\hat{v}_{css} + \frac{K_v}{K_2}\hat{v}_i + I_{pc}\hat{\omega}_s + \frac{E_d}{L_e}\hat{d} - \frac{K_4 q_3}{K_2}\hat{v}_o \quad (4.67)$$

$$\frac{d\hat{i}_{pc}}{dt} = -\Omega_s \hat{i}_{ps} + \frac{K_4 q_2}{K_2}\hat{i}_{ss} - \frac{K_4 q_4}{K_2}\hat{i}_{sc} - \frac{1}{K_2}\hat{v}_{cpc} - \frac{K_4}{K_2}\hat{v}_{\mathrm{csc}} - I_{ps}\hat{\omega}_s - \frac{K_4 q_5}{K_2}\hat{v}_o \quad (4.68)$$

$$\frac{d\hat{i}_{ss}}{dt} = -\frac{K_3 q_1}{K_1}\hat{i}_{ss} + \left(\Omega_s + \frac{K_3 q_2}{K_1}\right)\hat{i}_{sc} - \frac{1}{K_1}\hat{v}_{cps} - \frac{K_3}{K_1}\hat{v}_{css} + \frac{K_v}{K_1}\hat{v}_i + I_{sc}\hat{\omega}_s + \frac{E_d}{K_1}\hat{d} - \frac{K_3 q_3}{K_1}\hat{v}_o \quad (4.69)$$

$$\frac{d\hat{i}_{sc}}{dt} = \left(-\Omega_s + \frac{K_3 q_2}{K_1}\right)\hat{i}_{ss} - \frac{K_3 q_4}{K_1}\hat{i}_{sc} - \frac{1}{K_1}\hat{v}_{cpc} - \frac{K_3}{K_1}\hat{v}_{\mathrm{csc}} - I_{ss}\hat{\omega}_s - \frac{K_3 q_5}{K_1}\hat{v}_o \quad (4.70)$$

$$\frac{d\hat{v}_{cps}}{dt} = \frac{1}{C_p}\hat{i}_{ps} + \Omega_s \hat{v}_{cpc} + V_{cpc}\hat{\omega}_s \quad (4.71)$$

$$\frac{d\hat{v}_{cpc}}{dt} = \frac{1}{C_p}\hat{i}_{pc} - \Omega_s \hat{v}_{cps} - V_{cps}\hat{\omega}_s \quad (4.72)$$

$$\frac{d\hat{v}_{css}}{dt} = \frac{1}{C_s}\hat{i}_{ss} + \Omega_s \hat{v}_{\mathrm{csc}} + V_{\mathrm{csc}}\hat{\omega}_s \quad (4.73)$$

$$\frac{d\hat{v}_{\mathrm{csc}}}{dt} = \frac{1}{C_s}\hat{i}_{sc} - \Omega_s \hat{v}_{css} - V_{\mathrm{csc}}\hat{\omega}_s \quad (4.74)$$

$$\frac{d\hat{v}_{co}}{dt} = \frac{q_6}{C_o}\hat{i}_{ss} + \frac{q_7}{C_o}\hat{i}_{sc} - \frac{1}{C_o(R_L + r)}\hat{v}_{co} + \frac{1}{C_o(R_L + r)}\hat{i}_o \quad (4.75)$$

$$\hat{v}_o = R_{eq} q_6 \hat{i}_{ss} + R_{eq} q_7 \hat{i}_{sc} + \frac{R_{eq}}{r}\hat{v}_{co} + R_{eq}\hat{i}_o \quad (4.76)$$

$$\hat{i}_i = J_d \hat{d} + J_i \hat{i}_{ps} \quad (4.77)$$

The general state-space representation of the linearized system is given in (4.78) and (4.79).

$$\frac{d\hat{x}}{dt} = A\hat{x} + B\hat{u} \tag{4.78}$$

$$\hat{y} = C\hat{x} + D\hat{u} \tag{4.79}$$

Where

$$\hat{x} = (\hat{i}_{ms}, \hat{i}_{mc}, \hat{i}_{ps}, \hat{i}_{pc}, \hat{v}_{cps}, \hat{v}_{cpc}, \hat{v}_{css}, \hat{v}_{csc}, \hat{v}_{co}) \tag{4.80}$$

$$\hat{u} = (\hat{v}_i, \hat{d}, \hat{\omega}_s, \hat{i}_o) \tag{4.81}$$

$$\hat{y} = (\hat{v}_o, \hat{i}_i) \tag{4.82}$$

By transforming (4.67) to (4.77) into the state-space representation given in (4.78) and (4.79), the transfer function of the *CLLC* resonant converter along with a bode plot of the static operating point can be obtained. In the next step, the obtained static operating points can be used to analyze and predict the dynamic characteristics of the converter by the obtained small-signal model.

4.2. Voltage Regulation and Control Methods in Bidirectional DC/DC Converters

One of the challenges in the design of resonant converters is how to control the switching pattern to maintain soft-switching under different input voltages and loading conditions. In general, the efficiency of the resonant converters is decided by the power semiconductor devices and the passive elements of the circuit. The parameters of the converter (component parameters, switching pattern) can only be optimized at a certain operating point (certain input/output voltage and load). In the case the working condition changes, the converter will drift away from its optimal operation point and the soft switching may be lost. Normally the component parameters cannot be changed once the converter was designed, so the only control freedom left is the switching pattern of the converter. The control system and the modulation schemes adopted for resonant converters have a significant impact on the efficiency of these converters.

4.2.1. Modulation Techniques in the Proposed Comprehensive Control System

The modulation schemes used for resonant converters can be classified into variable-frequency modulation (VFM), and fixed-frequency modulation schemes including phase-shift modulation (PSM) and pulse-width modulation (PWM). In this thesis, the proposed comprehensive control system utilizes variable-frequency modulation and asymmetric pulse width modulation (APWM) to regulate the output voltage in different operating modes.

4.2.1.1. Variable-Frequency Modulation (VFM)

The overall gain of the converter in boost mode in terms of the normalized angular switching frequency is obtained in Figure 3.17 for both FW and HW/VD modes. In Figure 3.17, in order to make sure that the soft-switching is achieved for all the semiconductor devices, the switching frequency has to be kept above the resonant frequency. As can be seen in the FW curve in Figure 3.17 shown in blue, for the switching frequencies above the resonant frequency, as the switching frequency increases, the gain decreases, and vice versa. Therefore, in the control system, first, the output voltage of the converter is sensed and is compared with the desired value. Then, the difference (error) is fed into a PI controller. The output of the PI controller determines whether the switching frequency has to be increased or reduced to regulate the output voltage.

In the HW/VD curve, however, there is another peak at the right side of the resonant frequency. As a result, to simplify the control system and to utilize the same concept that is used in the FW control, a limiter has been placed in the output of the PI controller in HW/VD mode, preventing the switching frequency to move below the designated limit and hence ensuring soft-switching. The upper boundary of the limiter also determines when to switch from FW to HW/VD. The same limiter ensures soft-switching in both FW and HW/VD operating modes.

The resonant converter is a nonlinear system and it is extremely difficult to analyze it using an analytical formula. Yet, if the input and output voltages are nearly constant quantities under changing loads, and properties of the system do not change significantly, small-signal analysis and linearization can be performed on the system. Since, a small change in the input voltage, reference, or load only causes a linearly dependent or proportional change in the switching period, mathematically we approximate all nonlinear terms with a 1-term Taylor Series Approximation about an operating point.

In the variable frequency control system, the goal is to generate the correct voltage (V_2) at the output of the resonant converter by varying the switching period (T) of the inverter. For a *CLLC* resonant converter, the relation between V_2 and T is nonlinear, and therefore, the

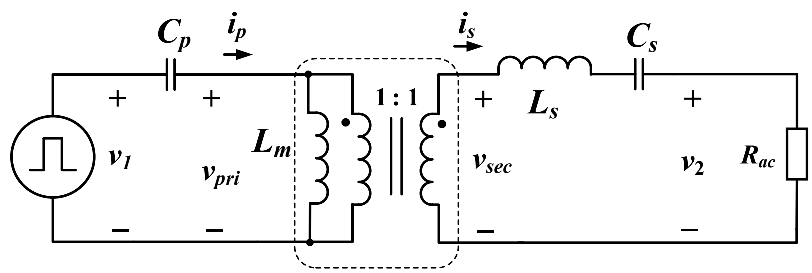


Figure 4.2- Equivalent circuit of the proposed *CLLC* resonant converter

operating point approach is used. The desired voltage V_2 is obtained by varying the impedances of the various elements in the circuit shown in Figure 4.2. The impedances are given by X_{cp}, X_{cs}, X_m and X_{ls} and are functions of the inverter switching frequency.

To simplify the analysis, considering the fact that the equivalent resistance of the rectifying stage (R_{ac}) does not vary with the switching frequency, it can be ignored in the small-signal analysis of the variable frequency control system. Hence, only C_p and L_m are included in the small-signal modeling of the variable frequency control. Consequently, the voltage that gets applied to the magnetizing inductance is given in (4.83).

$$v_{pri} = \frac{X_m}{X_m - X_{Cp}} \cdot v_1 \tag{4.83}$$

$$G_p = \frac{X_m}{X_m - X_{Cp}} \tag{4.84}$$

Where v_1 is the input voltage generated at the input terminal of the resonant tank and the v_{pri} is determined by the gain of the primary circuit. This gain is shown in (4.84) where $X_m = 2\pi f_s L_m$ is the impedance of the magnetizing inductance, $X_{cp} = 1/2\pi f_s C_p$ is the impedance of the primary capacitor. By modifying the switching frequency f_S, the gain of the circuit is changed and therefore the output voltage can be controlled with varying load and input voltage. For modeling the system, a relationship between the gain and the switching frequency needs to be determined.

Due to the nonlinear nature of the gain equation, we perform operating point analysis about the nominal operating point, i.e. the resonant frequency. In order to perform operating point analysis, we define a new variable p at the resonant frequency f_r as shown in (4.85).

$$p = \frac{1}{G_p} = \frac{X_m - X_{Cp}}{X_m} = 1 - \frac{1}{4\pi^2 f_S^2 C_p L_m} \tag{4.85}$$

$$v_{pri} = \frac{v_1}{p} \tag{4.86}$$

Using (4.85) and (4.86), v_{pri} can be expressed by (4.87).

$$v_{pri} = \frac{v_1}{\left(1 - \frac{1}{4\pi^2 f_S^2 C_p L_m}\right)} \tag{4.87}$$

Differentiating both sides with respect to frequency results in (4.88).

$$\delta v_{pri} = -\frac{v_1}{p^2} \cdot \frac{1}{\left(2\pi^2 f_S^3 C_p L_m\right)} \cdot \delta f_S \tag{4.88}$$

δv_{pri} is the change in v_{pri} for a small change in the switching frequency. The switching frequency can be represented as a function of the switching period, as shown in (4.89).

$$f_S = \frac{1}{T_S} \tag{4.89}$$

$$\delta f_S = \frac{-1}{T_S^2} \cdot \delta T_S = -f_S^2 \delta T_S \tag{4.90}$$

Substituting (4.90) in (4.88) gives:

$$\delta v_{pri} = \left(\frac{v_1}{2p^2\pi^2 f_S C_p L_m} \right) \cdot \delta T_S \tag{4.91}$$

Since the change in frequency is assumed to be small, f_S can be replaced by the nominal operating frequency (i.e., the resonant frequency f_r). Hence (4.91) changes to (4.92).

$$\delta v_{pri} = \left(\frac{v_1}{2p_0^2\pi^2 f_r C_p L_m} \right) \cdot \delta T_S \tag{4.92}$$

Where p_0 is the inverse gain calculated at the resonant frequency. The final period output is defined in (4.93).

$$T_S = T_{nom} + \delta T_S = T_{nom} + \left(\frac{\delta v_{pri}}{v1} \right) \cdot \left(2p_0^2\pi^2 f_r C_p L_m \right) \tag{4.93}$$

In (4.93), the term $2p_0^2\pi^2 f_r C_p L_m$ is constant, since the change in period is assumed to be small. Hence, this term can be replaced by the constant T_{Vf} which is defined in (4.94).

$$T_{Vf} = 2p_0^2\pi^2 f_r C_p L_m \tag{4.94}$$

The term δv_{pri} is also the change in the v_{pri} for a corresponding change in the period (δT_s) given in (4.95).

$$\delta v_{pri} = v_{pri} - v_{pri\_nom} \tag{4.95}$$

Substituting (4.94) and (4.95) in (4.93), the final expression for the desired switching period is obtained as shown in (4.96).

$$T_S = T_{nom} + T_{Vf} \cdot \left(v_{pri} - v_{pri\_nom}\right) \cdot \left(\frac{1}{v_1}\right) \tag{4.96}$$

T_{nom} is known from the converter design, and T_{Vf} is a constant defined previously. v_{pri} is the voltage at the primary of the high-frequency transformer that is needed to produce the desired output voltage. In (4.96), v_{pri} can be replaced by the output voltage (v_o) with a convenient approximation.

$$T_S = T_{nom} + T_{Vf} \cdot \left(v_o - v_{ref}\right) \cdot \left(\frac{1}{v_1}\right) \tag{4.97}$$

Based on the relationship between the switching period and the output voltage given in (4.97), a transfer function of the controller given in (4.98) is used to regulate the output voltage.

$$s^2 LC + sRC + K_p + \frac{K_i}{s} = 0 \tag{4.98}$$

Where L is the output inductor, C is the output capacitor, R is the equivalent parasitic series resistance of the circuit (R_p and R_s), K_p and K_i are the proportional and the integral gain of the compensator. Yet, a proportional + integral (PI) compensator can be used to regulate the output voltage. The use of a Derivative term is ruled out because the series parasitic resistance of the system acts as a natural damping factor, and swamps any effect of the derivative term. Hence, substituting (4.98) in (4.97), the relationship between the period and the output voltage can be written by (4.99).

$$T_S = T_{nom} + \left[K_p \left(v_o - v_{ref} \right) + K_i \int_0^t \left(v_o - v_{ref} \right) dt \right] \cdot \left(\frac{1}{v_1} \right) \tag{4.99}$$

In the proposed comprehensive control system used in this thesis to regulate the output of the multi-mode stacked-switch converter, (4.99) is used to regulate the output voltage.

4.2.1.2. Asymmetric Pulse-Width Modulation (APWM)

As discussed in Chapter 2. and section 2.3.3, the unipolar square wave voltage v_1 generated by the inverter at the primary of the resonant circuit is given by (4.100).

$$v_1 = V_i D + \sum_{h=1}^{\infty} \frac{\sqrt{2} V_i}{h\pi} \sqrt{(1 - \cos 2h\pi D)} \sin(h\omega_{sw} t + \theta_h) \tag{4.100}$$

$$\theta_h = \tan^{-1}\left(\frac{\sin 2h\pi D}{1 - \cos 2h\pi D}\right) \tag{4.101}$$

Where D is the duty ratio in v_1 and T_s is the switching period.

In APWM control of the resonant converter, the frequency is kept constant. In this control, the compensated voltage error is compared to a saw-tooth waveform to generate a pulse train with duty cycle D. The duty cycle variation of the main switch varies the shape of the AC waveform incident on the tank thus regulating the output voltage. The total gain of the converter in terms of the normalized angular switching frequency is obtained in Figure 4.3 and Figure 4.4

for both FW and HW/VD modes respectively for different duty cycles. As can be seen, as the duty cycle decreases, the peak of the overall gain curve drops.

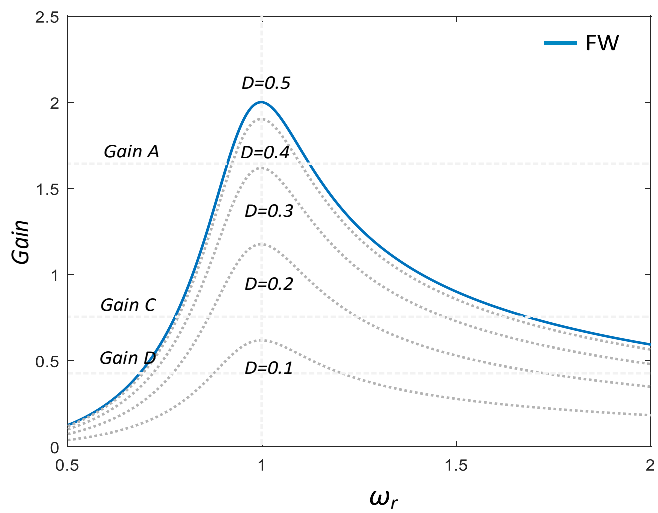


Figure 4.3- Voltage gain plot of the bidirectional DC/DC converter based on the multi-mode stacked-switch leg in FW mode

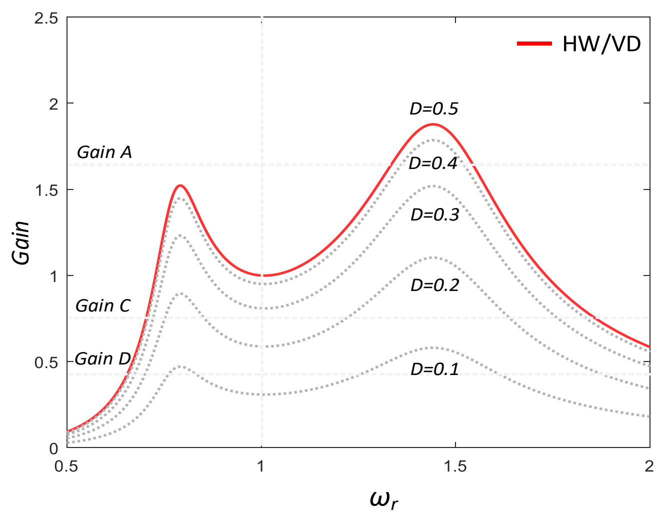


Figure 4.4- Voltage gain plot of the bidirectional DC/DC converter based on the multi-mode stacked-switch leg in HW mode

4.2.1.3. Voltage Balancing in Multi-Mode Stacked-Switch DC/DC Converters

Another drawback of the conventional 4-switch string converter is the unbalanced voltage stress across the input/output capacitors. Any mismatch in the capacitance values leads to unbalanced voltage stress over the capacitors which may damage the capacitors in the long term and causes unbalanced voltage stress over the switches.

In [97], the middle switches operate in a way that are either completely turned ON or OFF. As discussed in Chapter 2, according to Table 2.2, the added semiconductor devices in the proposed multi-mode stacked-switch leg, introduce additional switching patterns for the converter and provide multiple current paths for the secondary side current to circulate through the circuit. As an example, as demonstrated in Figure 2.9 and Figure 2.10, by applying different switching signals, a similar voltage-doubler operation can be achieved. Yet, in Figure 2.9 the positive i_s charges C_{oH} and the negative i_s feeds C_{oL} while in Figure 2.10, it is the opposite. Therefore, by carefully switching between different operating modes and applying appropriate switching signals with calculated time intervals, the unbalanced voltage distribution over the DC-link capacitors can be addressed.

Although in the proposed multi-mode stacked-switch leg presented in Figure 2.3, the middle switches are assumed to operate in a low-frequency range, they can be replaced by high-frequency switches and high-frequency gate signals can be applied to provide additional control in the voltage regulation and voltage balancing strategies.

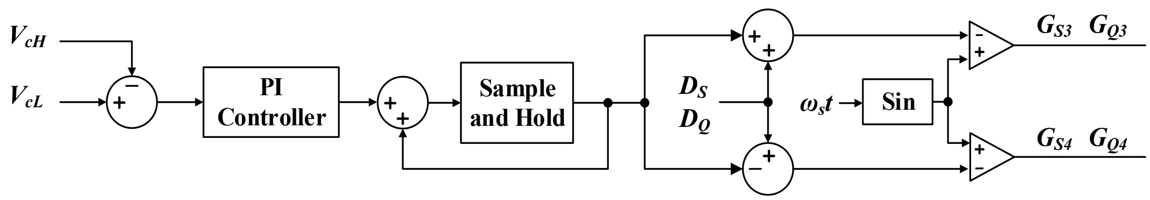


Figure 4.5- Block diagram of the voltage balancing system

The block diagram of the voltage balancing system is demonstrated in Figure 4.5. To address the voltage unbalancing issue across the DC-link capacitors, the voltage across the input and output capacitors are sampled and fed to the controller. The voltage difference goes through a PI controller and its output translates into an offset to the current duty ratio of the middle switches (such as Q_3 and Q_4 in the rectifying leg) while operating with the same switching frequency. The duty ratio difference balances the voltage stress over the input/output capacitors.

4.2.2. A Novel Comprehensive Control System Based on Circuit Redundancy

In applications where the voltage gain is wide, in the case of using a variable frequency control in order to regulate the output voltage, the converter is bound to operate in a wide switching frequency range. However, drifting away from the resonant frequency leads to a restricted soft-switching range, increased core size in the design process, and limited light-load regulation ability [75]. To address the abovementioned issues and to improve the efficiency of the resonant converter in applications with a wide input/output range, many modification methods have been presented. [72], [73] focus on reconfiguration of the resonant tank, but this

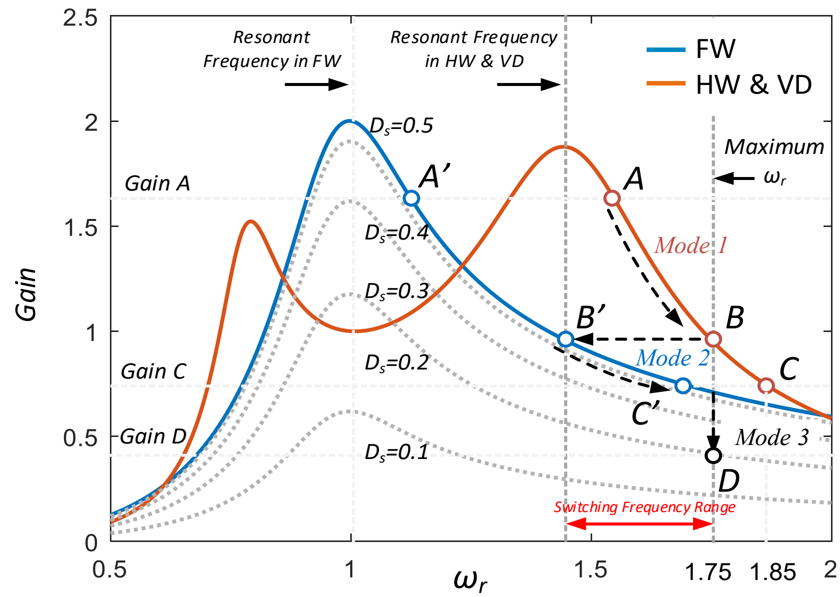


Figure 4.6- Voltage gain plot of the bidirectional DC/DC converter based on the multi-mode stacked-switch leg

approach requires a complicated design of the resonant components. Frequent reconfigurations also damage the overall efficiency and slow down the transient response. [69], [74] suggest addressing the issue by modifying the primary-side switch network which is most suitable for wide input voltage range applications. [75], [76] present methods based on modifications in the secondary side rectifier where it usually restructures among full-bridge, voltage-doubler, and voltage-quadrupler. As a result, the output voltage range is extended. [77]–[79] propose modification in control strategies where it can improve the light load regulation capacity and efficiency of the converter, but the controller design is complicated with high-frequency oscillations in the output.

To regulate the output voltage for a wide range of gains, a comprehensive control system is proposed with 3 modes of operation employing the restructuring capability of the converter in the rectifying block and modification in control strategies as demonstrated in Figure 4.6.

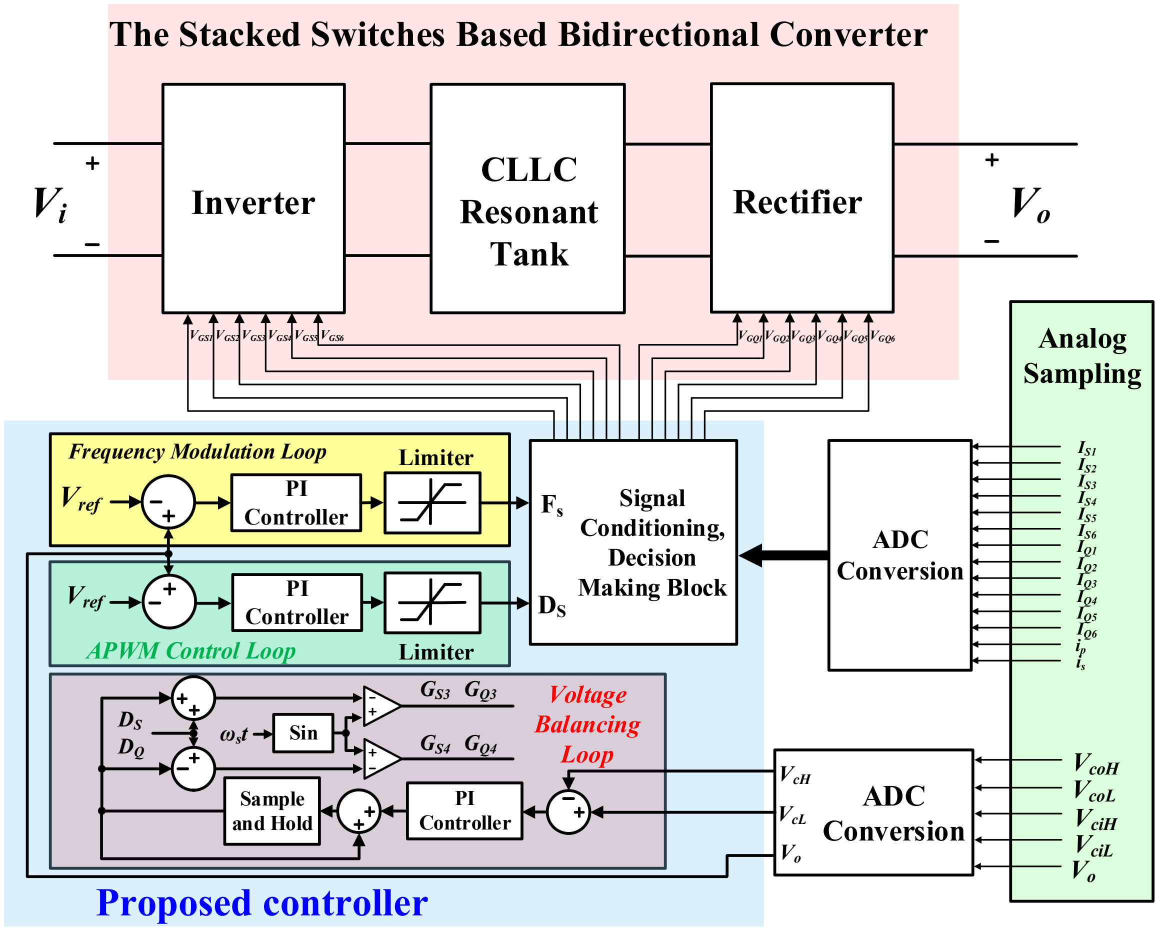


Figure 4.7- Block diagram of the proposed closed-loop control system

In mode 1, the converter operates in the half-wave rectifier mode, and the output voltage is regulated through variable frequency modulation control. In order to achieve high efficiency for various loading conditions, the frequency range has been limited as narrow as possible. Once the switching frequency reaches the upper limit, the structure of the rectifying block switches to the full-wave rectifier, and the switching frequency is set to the bottom limit going from mode 1 to mode 2. In this case, the gain curve switches from HW/VD to FW. In mode 2, the output voltage is again regulated by the variable frequency modulation control. In mode 2, by reaching the upper-frequency limit, the control moves to mode 3 whereas, once the operating

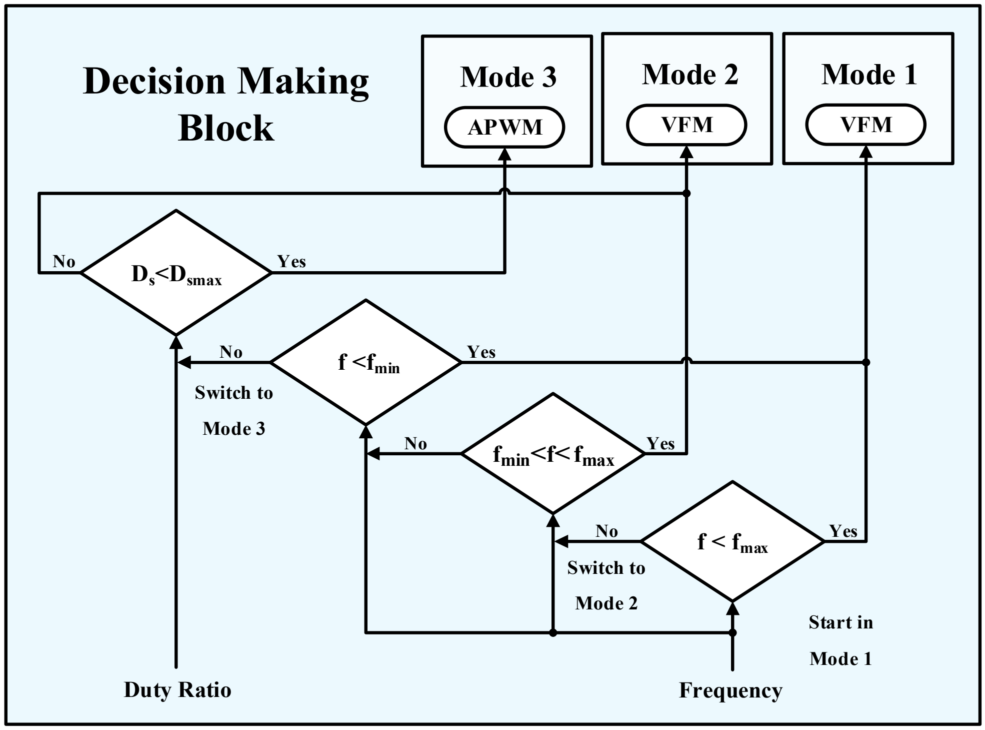


Figure 4.8- Decision-making block of the proposed closed-loop control system in bidirectional DC/DC conversion

switching frequency reaches the bottom limit in this mode, the control goes back to mode 1. In mode 3, while the switching frequency stays constant at the maximum limit, the output voltage is regulated by varying the duty ratio of the unipolar voltage generated by the inverting block at the primary of the resonant tank. The block diagram of the control system and the flowchart of the decision-making block are shown in Figure 4.7 and Figure 4.8 respectively.

As discussed earlier, the problem of the variable frequency modulation used as a sole modulation method is the wide frequency variation to maintain soft-switching operation. Specifically in some cases, to achieve ZVS, the switching frequency could vary from one to more than twice the resonant frequency [98]. A higher switching frequency for a given load leads to higher current peaks and therefore, higher conduction losses and a de-rating of the converter. In addition, a wide range of switching frequency results in poor utilization of the magnetic components and introduces a wide noise spectrum and EMI into the system.

The developed comprehensive control system enables the converter to regulate the output voltage within a narrow switching range demonstrated in Figure 4.6. As an example, moving from a gain of A to a gain of D requires a dramatic increase in the switching frequency in either FW or HW/VD modes while in the proposed control system, a gain of D can be achieved at a significantly lower switching frequency. As a result, by properly controlling the switching states of Q_3 and Q_4 and switching between different operating modes, the switching frequency can be limited while achieving the same gain.

4.2.3. A Modified Comprehensive Control System in a Multi-Mode Stacked-Switch Bidirectional DC/DC Converter

In the presented control system demonstrated in Figure 4.6, in mode 1, Q_3 and Q_4 are turned ON and the rectifier block operates in HW/VD mode. In this mode, when the frequency modulation control increases the switching frequency and it hits the upper limit, by switching Q_3 and Q_4 OFF, the control moves to mode 2, and the rectifier block moves to the FW mode. However, in transitioning from mode 1 to mode 2 as demonstrated in Figure 4.6, the switching frequency is set to the lower limit from the upper limit. Restructuring the rectifier block and at the same time the significant change in the switching frequency may impose a drastic transient on the waveform and the circuit components.

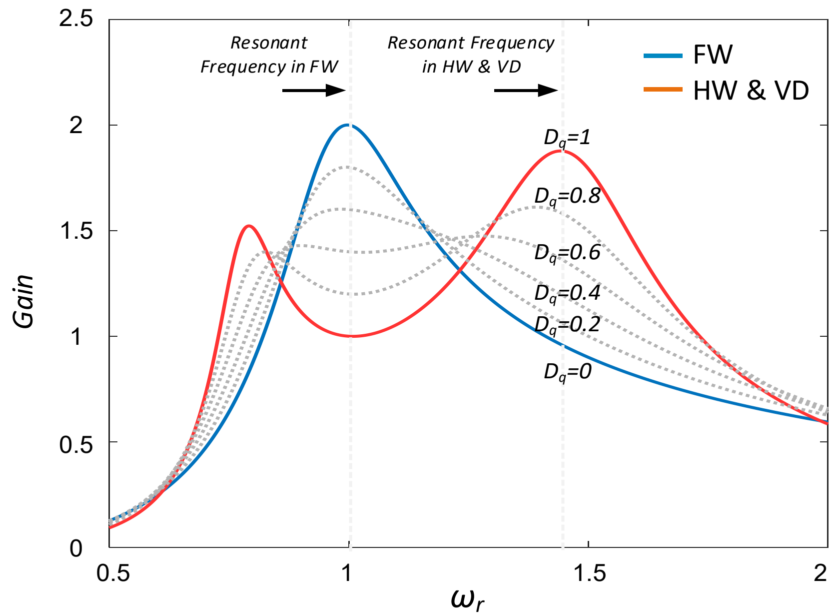


Figure 4.9- Voltage gain plot of the bidirectional DC/DC multi-mode stacked-switch converter with a pulse-width modulated rectifier block

Yet, by adopting a proper approach, the transition from mode 1 to mode 2 in Figure 4.6 can take place smoothly. As mentioned earlier, the middle low-frequency switches can be replaced by high-frequency MOSFETs. As a result, instead of switching Q_3 and Q_4 either ON or OFF, high-frequency pulse-width-modulated gate signals can be applied to the gates of Q_3 and Q_4.

Figure 4.9 demonstrates the voltage gain curve of the bidirectional DC/DC multi-mode stacked-switch converter with a pulse-width modulated rectifier block. As can be seen, by applying high-frequency gate signals with various duty ratios, (2.7) in Chapter 2 changes to (4.102).

$$\mathrm{R}_{ac} = \frac{2}{\pi^2}\cdot(2-D_q)^2\cdot R_L \tag{4.102}$$

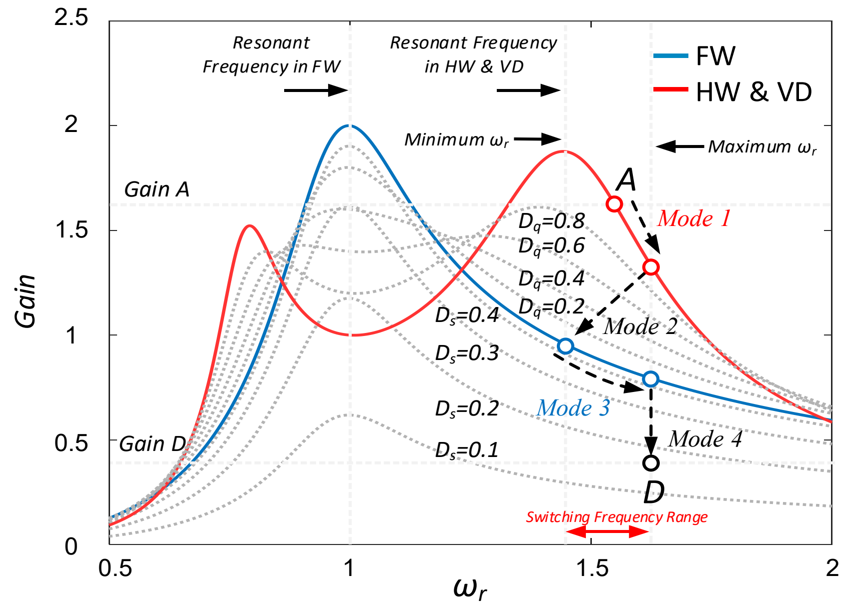


Figure 4.10- Voltage gain plot of the bidirectional DC/DC converter based on the multi-mode stacked-switch leg

In addition, the gain of the rectifier block in terms of the duty ratio (D_q) is updated from (2.14) to (4.103).

$$\frac{V_o}{V_2} = \frac{\pi}{\sqrt{2\cdot(2-D_q)}} \tag{4.103}$$

From (4.102) and (4.103), multiple gain curves can be obtained between the FW and HW/VD curves. In Figure 4.9, the frequency of the PWM signals in the rectifier block is the same as that of in the inverter block. Also, as can be seen in Figure 4.9, on the right side of the peak in HW/VD curve, as the duty ratio in the rectifier block (D_q) decreases, the gain of the converter drops. Hence, an additional PWM control can be added to the previously proposed closed-loop control system.

The overall gain curve of the multi-mode stacked-switch bidirectional DC/DC converter with the proposed modified comprehensive control system is demonstrated in Figure 4.10. As

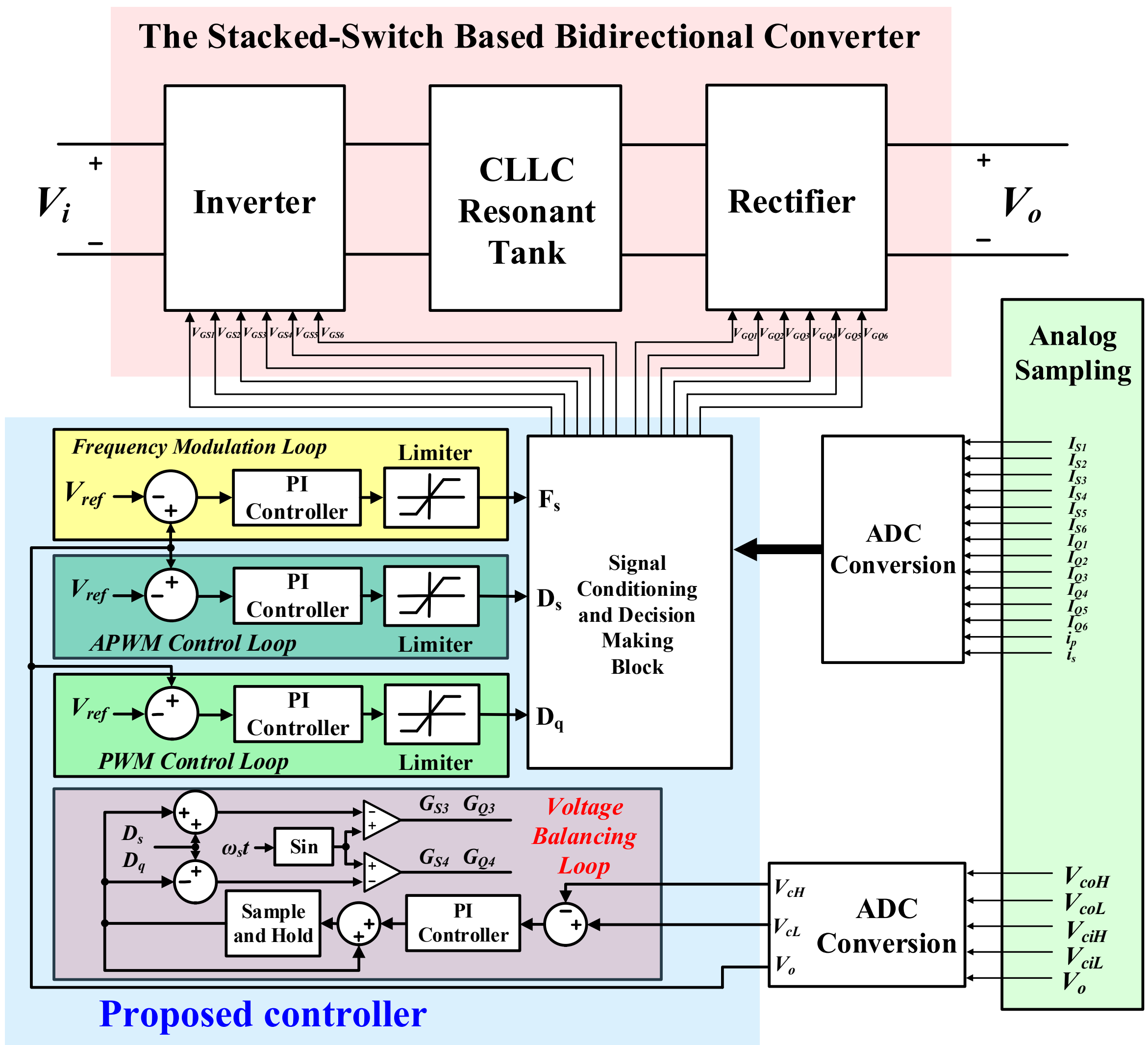


Figure 4.11- Block diagram of the proposed modified comprehensive control system

discussed earlier, the transition between mode 1 and mode 2 in Figure 4.6 imposes transients on the converter. In the modified comprehensive control system, the number of control modes is increased from 3 to 4. In the added PWM control in the rectifier block (mode 2 in Figure 4.10), by simultaneously changing the duty ratio and updating the switching frequency, the converter switches from VF in FW (mode 1) to VF in HW (mode 3) smoothly. In addition, by comparing Figure 4.10 and Figure 4.6, it can be seen that in the modified comprehensive control system, the switching frequency range is further reduced. The wide gain and narrow operating

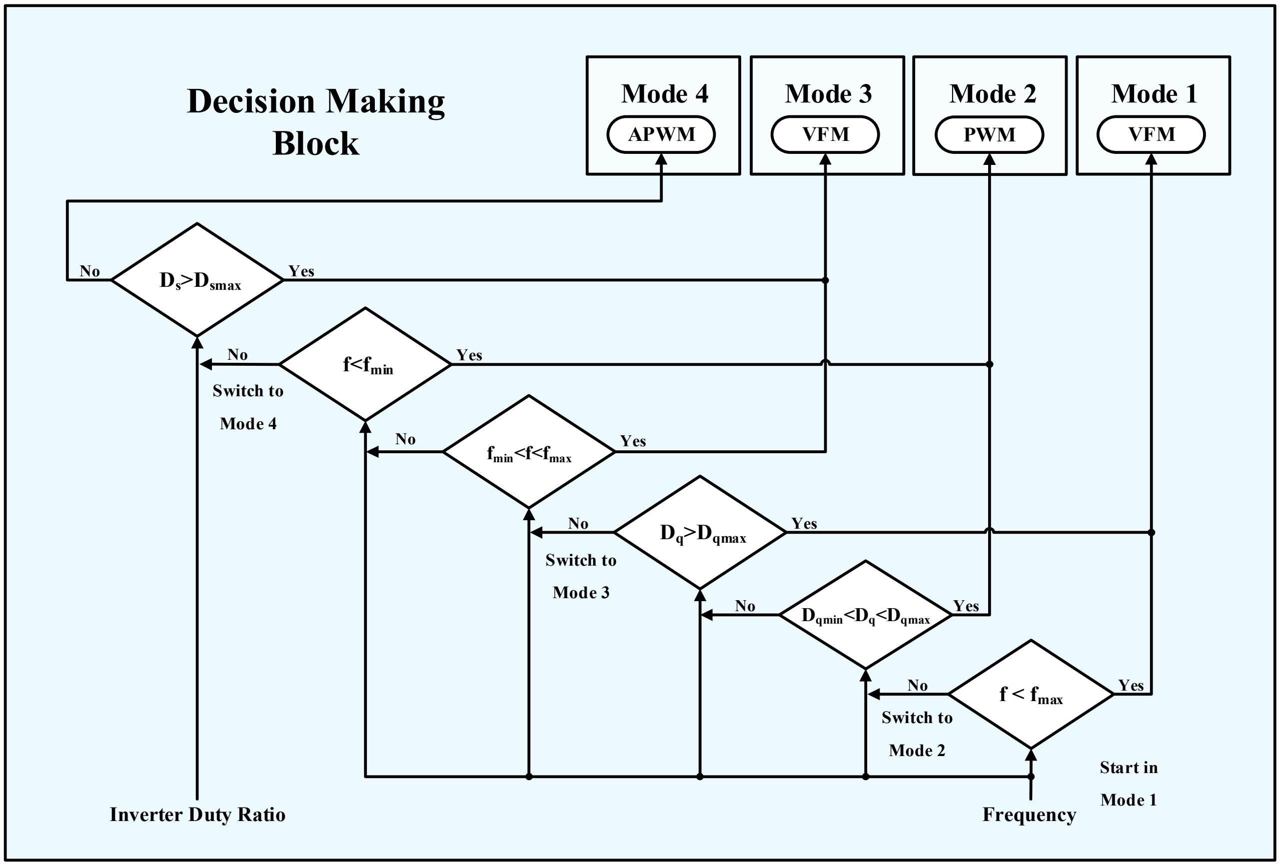


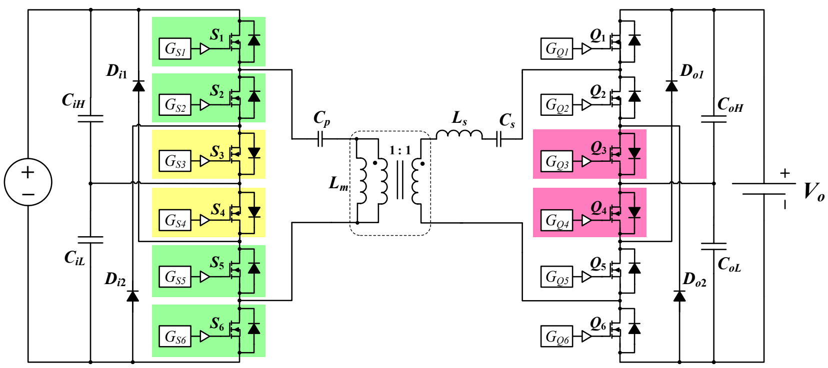
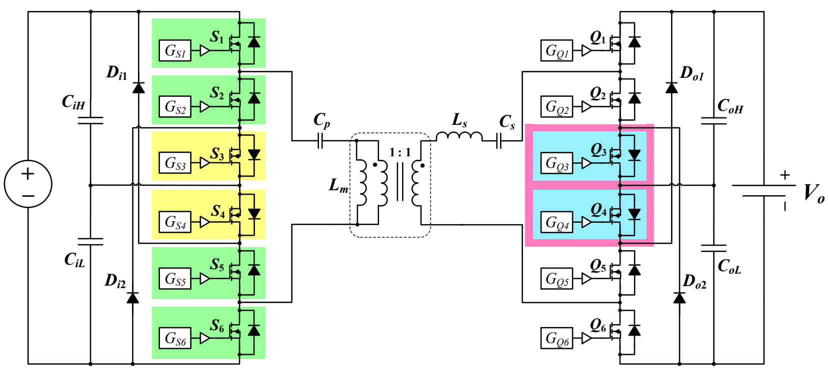
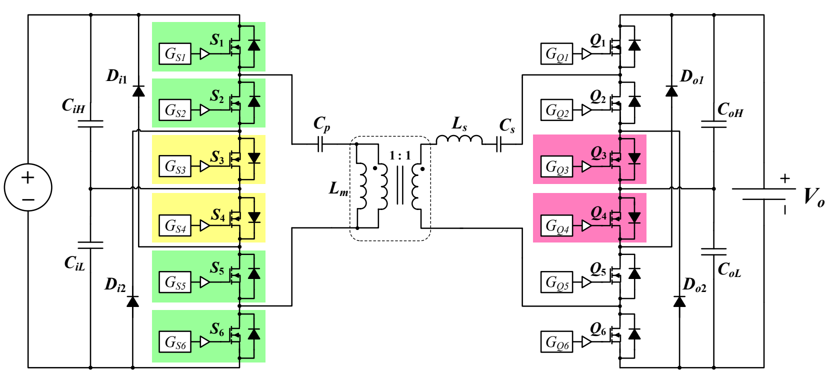
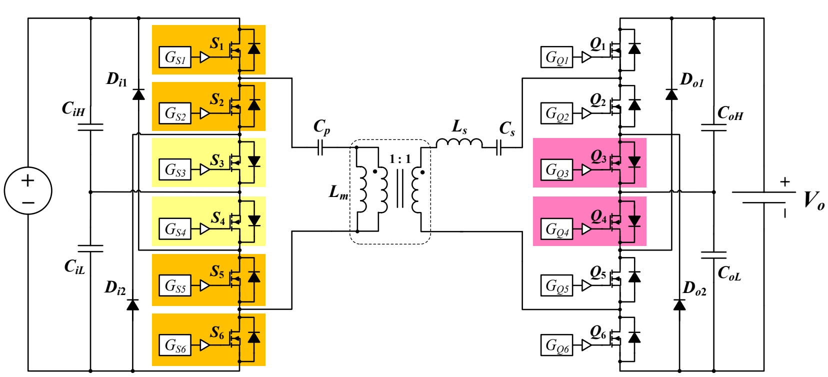
Figure 4.12- Decision-making block of the proposed closed-loop control system in bidirectional DC/DC conversion

frequency range in the proposed control system results in the optimum utilization of the magnetic components, reduced EMI, and a flat efficiency curve in different loading conditions.

The block diagram of the modified comprehensive control system is depicted in Figure 4.11. The developed control system utilizes a VFM, an APWM, and a PWM control loop to regulate the output voltage. The two voltage balancing loops are developed to balance the voltage across the DC capacitors. The flowchart of the decision-making block in Figure 4.11 is given in Figure 4.12. The control system starts from VFM in HW/VD mode (mode 1) initially. As the input voltage increases or the load decreases, the switching frequency is increased to compensate for the changes and regulate the output voltage. Once the operating frequency exceeds the upper limit, the control moves from mode 1 to mode 2 and a high-frequency PWM signal is applied to the middle switches (Q_3 and Q_4). By defining a linear relationship between the duty ratio (D_q) and the switching frequency, as D_q is reduced, the switching frequency goes down as depicted in Figure 4.10. By simultaneous variation of the duty ratio and the operating frequency, the output voltage is regulated in this mode. In mode 2, when D_q or switching frequency hits the bottom limit, the control system moves from mode 2 to mode 3 (VFM in FW) while by exceeding the upper-frequency limit, the control moves back from mode 2 to mode 1. In mode 3, the output voltage is regulated by varying the switching frequency. In the same manner, by hitting the upper-frequency limit, the control goes from mode 3 to mode 4 (APWM) and by hitting the bottom limit, the control moves back to mode 2. In mode 4, by keeping the switching frequency constant at the upper limit and changing the duty ratio of the switch signals in the inverting block (D_s), the output voltage is regulated. In this mode, once D_s reaches the bottom limit, the control moves from mode 4 to mode 3.

Table 4.1 provides the switch signals associated with each control mode. As can be seen, in mode 1, VFM control regulates the output voltage and the output gate signals are applied to S_1, S_2, S_3, and S_4 marked in green while at the same time the primary side voltage balancing loop generates gate signals to S_3 and S_4 marked in yellow and the output of the secondary side voltage balancing loop is applied to Q_3 and Q_4 shown in pink. In mode 2, as illustrated in Figure 4.10, PWM control regulates the output voltage while adjusting the switching frequency accordingly. The PWM signals are applied to Q_3 and Q_4 marked in blue. In mode 3, the operation is similar to mode 1. In mode 4, the switching frequency is kept constant and the gate signals generated by the APWM control are applied to S_1, S_2, S_5, and S_6 marked in orange.

Table 4.1- Switch signals associated with each control mode (green: VFM, blue: PWM, orange: APWM, yellow: primary side voltage balancing, pink: secondary side voltage balancing)

	Control	Associated Switches
Mode 1	VFM	
Mode 2	PWM/VFM	
Mode 3	VFM	
Mode 4	APWM	

4.3. Results and Performance

The 1kW, 400VDC/700VDC, >100kHz bidirectional converter employing the multi-mode stacked-switch legs demonstrated in Figure 4.13 has been designed and used in order to verify the performance of the modified comprehensive control system. According to Figure 4.10, the bottom limit for the switching frequency happens around ω_r=1.45. Therefore, to design the converter to operate at >100 kHz switching frequency, the based frequency of the resonant circuit is set to 75 kHz (f_0). Consequently, the resonant circuit components are obtained as shown by (4.104) to (4.111).

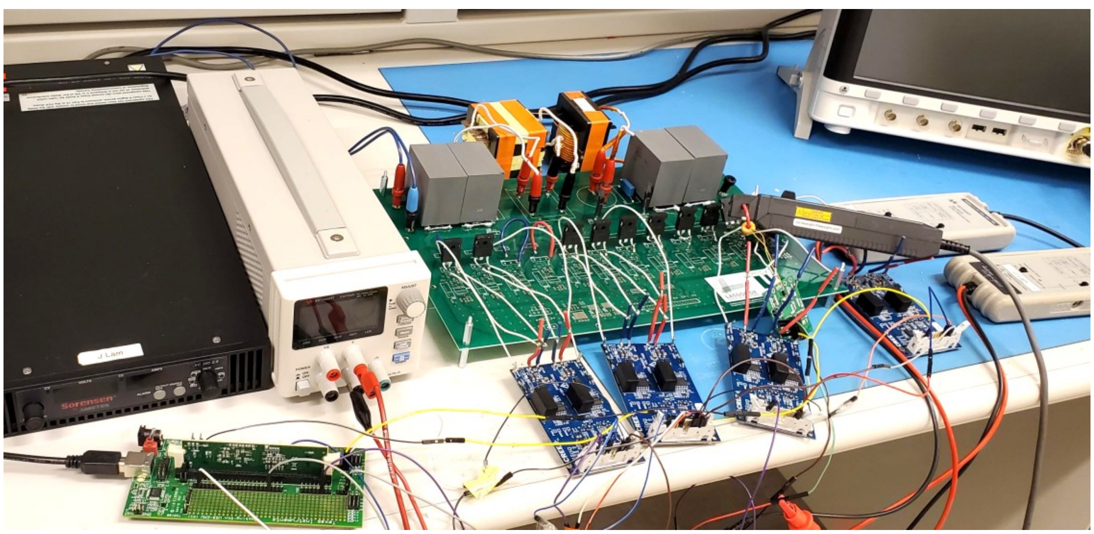


Figure 4.13- Hardware experimental set-up in laboratory

$$R_L = \frac{V_o^{\,2}}{P_o} = \frac{700^2}{1000} = 490\Omega \tag{4.104}$$

$$R_{ac} = \frac{8}{\pi^2} \cdot R_L = 397.18\Omega \tag{4.105}$$

$$L_M = \frac{\mathrm{R}_{ac}}{Q \cdot 2\pi f_0} = 210\mu H \tag{4.106}$$

Table 4.2- Design specifications and circuit parameters

Output Power (P_o)	1 kW
Output Voltage (V_o)	700 V
Input Voltage (V_i)	400 V
Magnetizing inductance (L_M)	210 µH
Secondary side resonant inductance (L_s)	420 µH
Primary side resonant capacitance (C_p)	21 nF
Secondary side resonant capacitance (C_s)	8.3 nF
Minimum Switching Frequency (f_{smin})	108.75 kHz
Maximum Switching Frequency (f_{smax})	121.5 kHz
Switches	SiC SCT3080KL
Added Diodes	U1560 Ultrafast Diode
Primary side snubber caps	330 pF
Secondary side snubber caps	150 pF

$$L_s = k \cdot L_M = 420\mu H \tag{4.107}$$

$$C_p = \frac{1}{L_M \omega_0^2} = 21nF \tag{4.108}$$

$$C_s = mC_p = 8.3nF \tag{4.109}$$

$$f_{s\min} = 1.45 \times f_0 = 108.75kHz \tag{4.110}$$

$$f_{s\max} = 1.62 \times f_0 = 121.5kHz \tag{4.111}$$

The circuit parameters are given in Table 4.2.

As demonstrated in Figure 4.10 and Figure 4.12, initially the control system starts in mode 1. Figure 4.14 shows the input and output voltage of the converter along with the current passing through S_1 and Q_3. In Figure 4.14, the input voltage is 400VDC and the developed comprehensive control system regulates the output voltage at 700VDC through the variable frequency modulation.

The primary resonant current passing through S_1 and S_2 is demonstrated in Figure 4.15. As can be seen, i_{S1} and i_{S2} are identical and the primary side resonant current passing through S_1 and S_2 is evenly balanced.

Figure 4.16 depicts the primary and secondary current in the *CLLC* resonant tank. The drain-source voltage across S_1 (v_{S1}) along with the current passing through S_1 (i_{S1}) is demonstrated in Figure 4.17. As it is shown, by maintaining the switching frequency within the

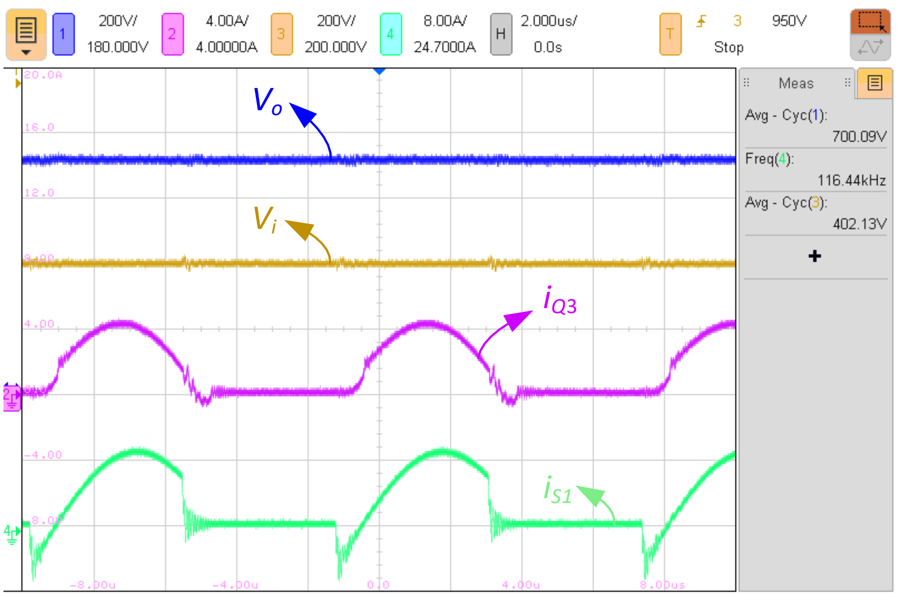


Figure 4.14- Experimental waveforms of the converter in boost mode in mode 1. Input and output voltage and the current passing through S_1 and Q_3

specified frequency boundaries, the control system provides ZVS and ZCS for all of the inverting switches.

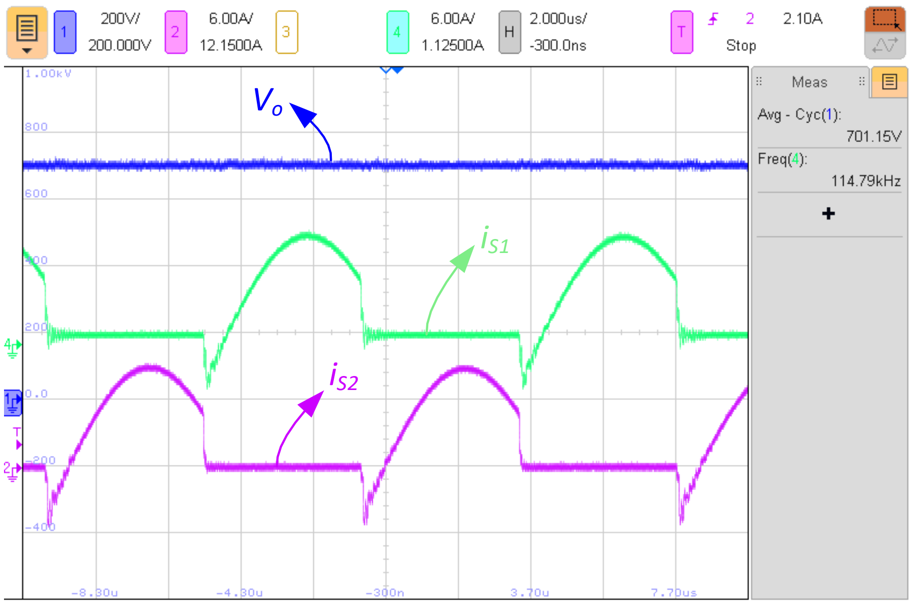


Figure 4.15- Experimental waveforms of the converter in boost mode. Output voltage and the current passing through S_1 and S_2

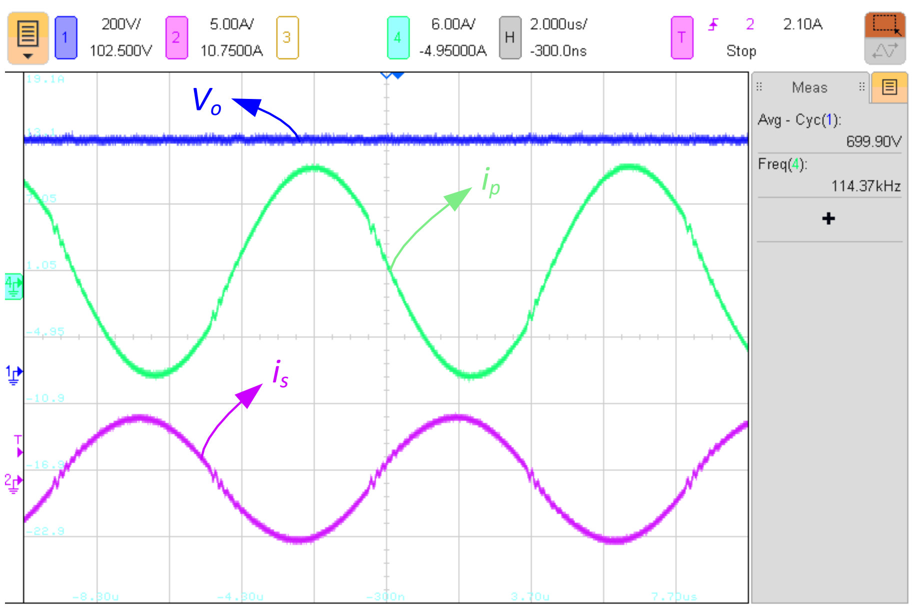


Figure 4.16- Experimental waveforms of the converter in boost mode. Output voltage and the current at the primary and secondary side of the resonant converter

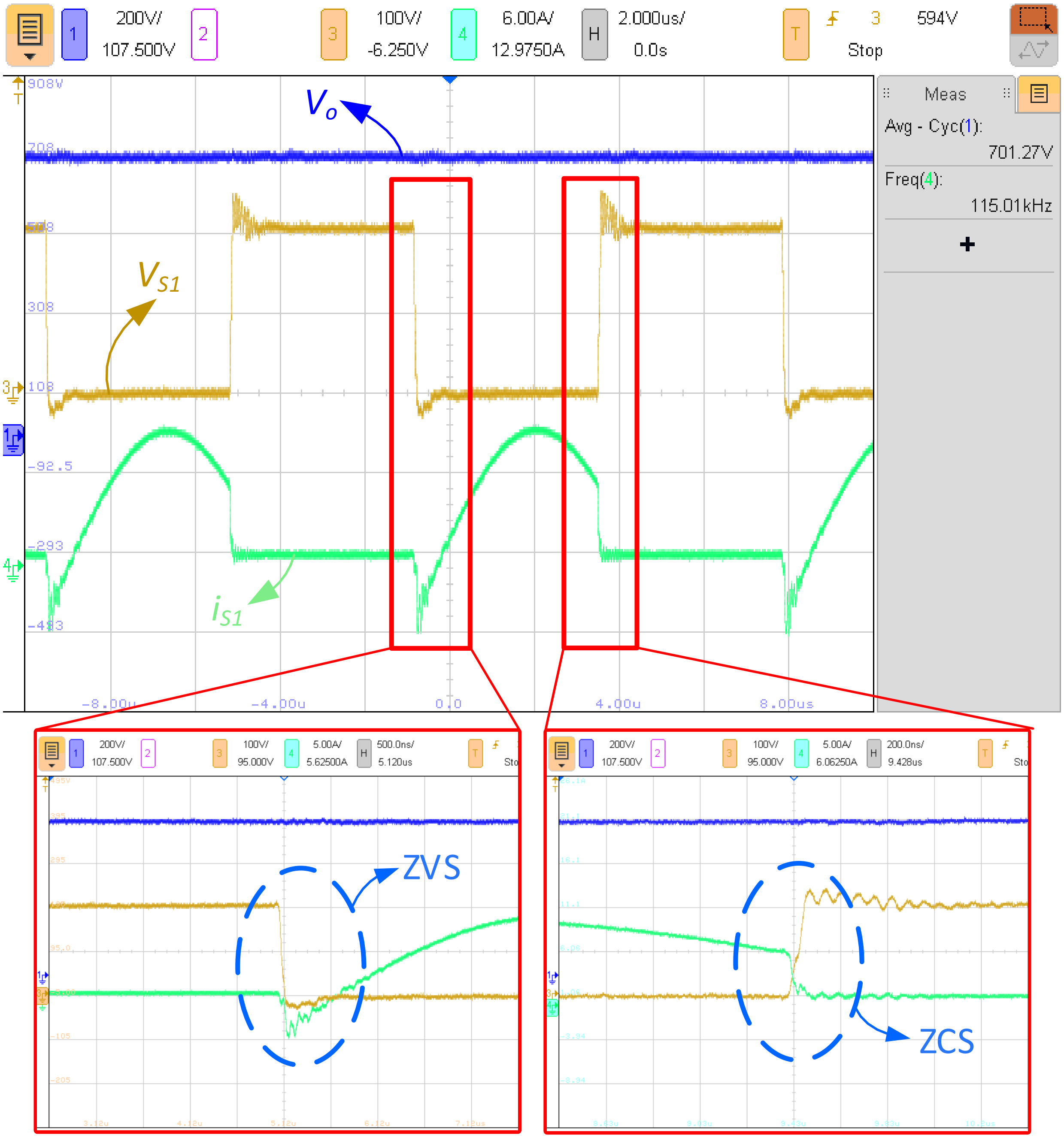


Figure 4.17- Experimental waveforms of the converter in boost mode. Output voltage and voltage and current of S_1 in the inverting block of the converter

The drain-source voltage across Q_1 (v_{Q1}) and the current passing through Q_1 (i_{Q1}) are given in Figure 4.18. As can be seen, ZVS and ZCS is also realized for all the semiconductor devices in the rectifier block.

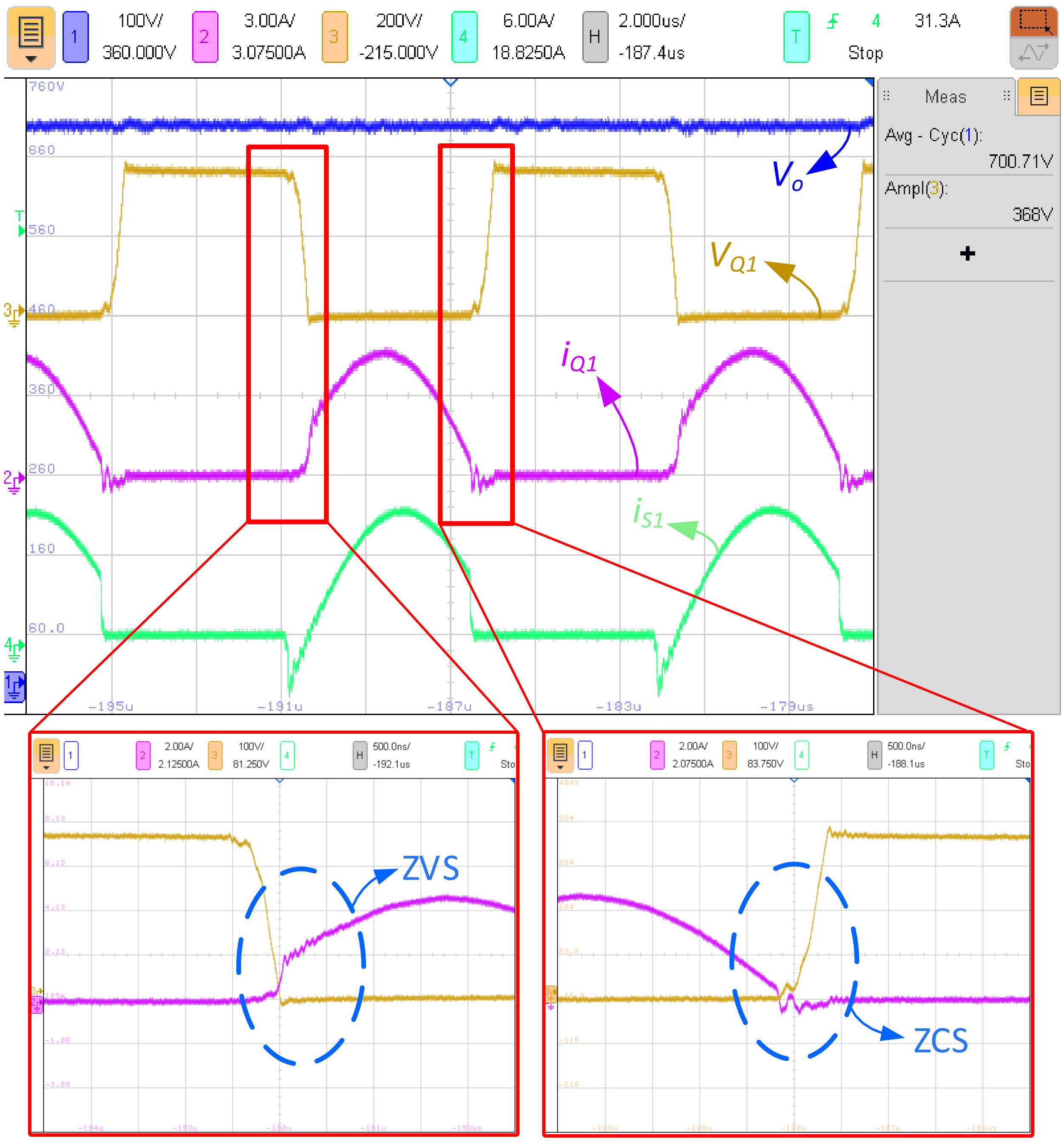


Figure 4.18- Experimental waveforms of the converter in boost mode. Output voltage, the voltage and current of Q_3 in the rectifying block of the converter, and the current passing through S_1

In order to verify the functionality of the developed comprehensive control system, a number of scenarios are considered to investigate the performance of the converter in each mode. In the first scenario, in mode 1 where a variable frequency modulation is used in HW/VD mode to regulate the output voltage, the input voltage is increased from 400VDC to 450VDC.

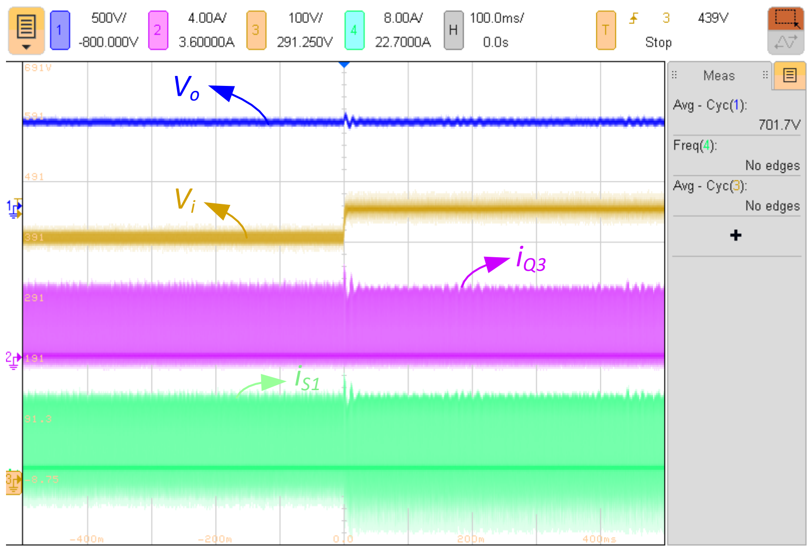


Figure 4.19- Dynamic response of the converter in boost mode in mode 1 for a step change in V_i (400V to 450V). The input and output voltage, and the current passing through S_1 and Q_3.

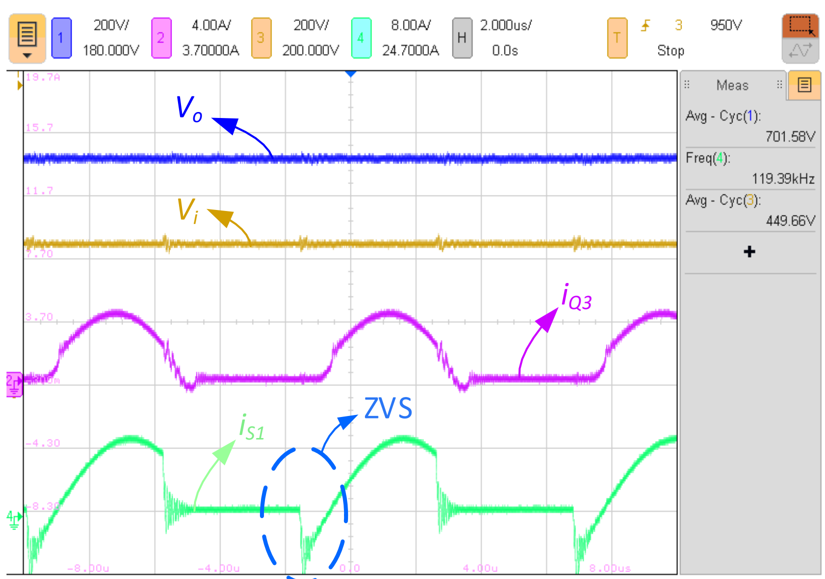


Figure 4.20- Experimental waveforms of the converter in boost mode in mode 1 for a V_i = 450V. The input and output voltage, and the current passing through S_1 and Q_3.

The performance of the VFM control loop in mode 1 is demonstrated in Figure 4.19 and Figure 4.20. As can be seen, by changing the switching frequency from 115 kHz to 119 kHz, the control system regulates the output voltage while providing ZVS for the switches.

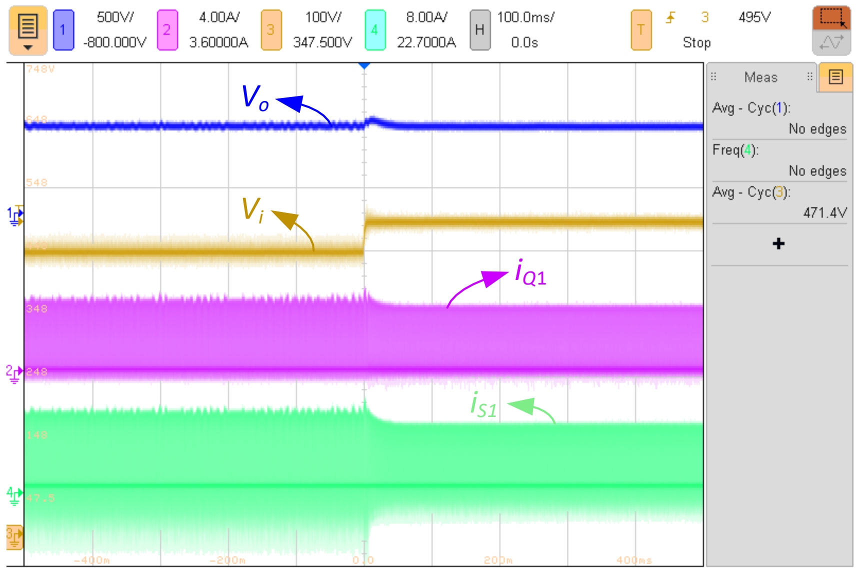


Figure 4.21- Dynamic response of the converter in boost mode transitioning from mode 1 to mode 2 for a step change in V_i (450V to 500V). The input and output voltage, and the current passing through S_1 and Q_3.

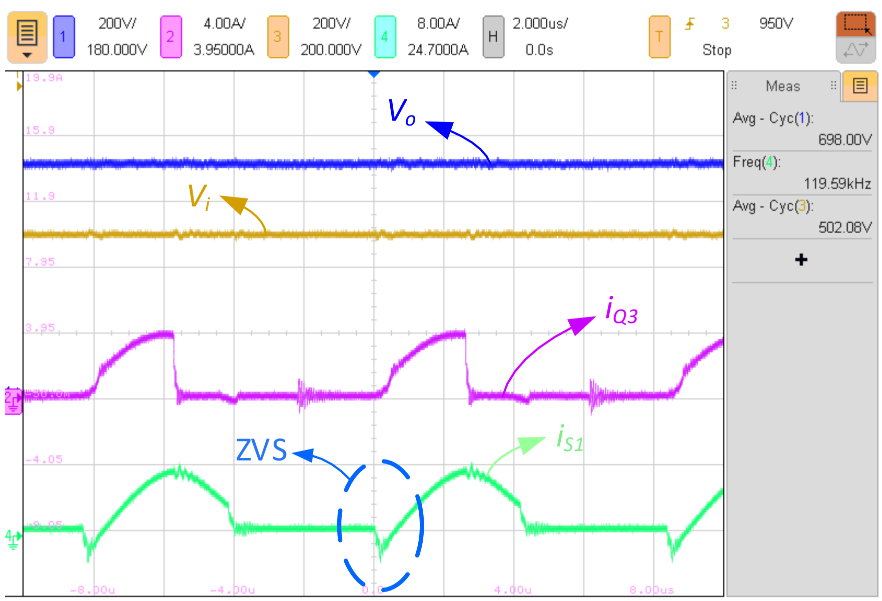


Figure 4.22- Experimental waveforms of the converter in boost mode in mode 2 for a V_i = 500V. The input and output voltage, and the current passing through S_1 and Q_3.

In the 2nd scenario, the input voltage is increased from 450VDC to 500VDC. In this case, the switching frequency exceeds the upper limit and the comprehensive control system moves the control from mode 1 (VFM in HW/VD) to mode 2 (PWM). As can be seen in Figure 4.21, the comprehensive control system regulates the output voltage at 700VDC by switching from

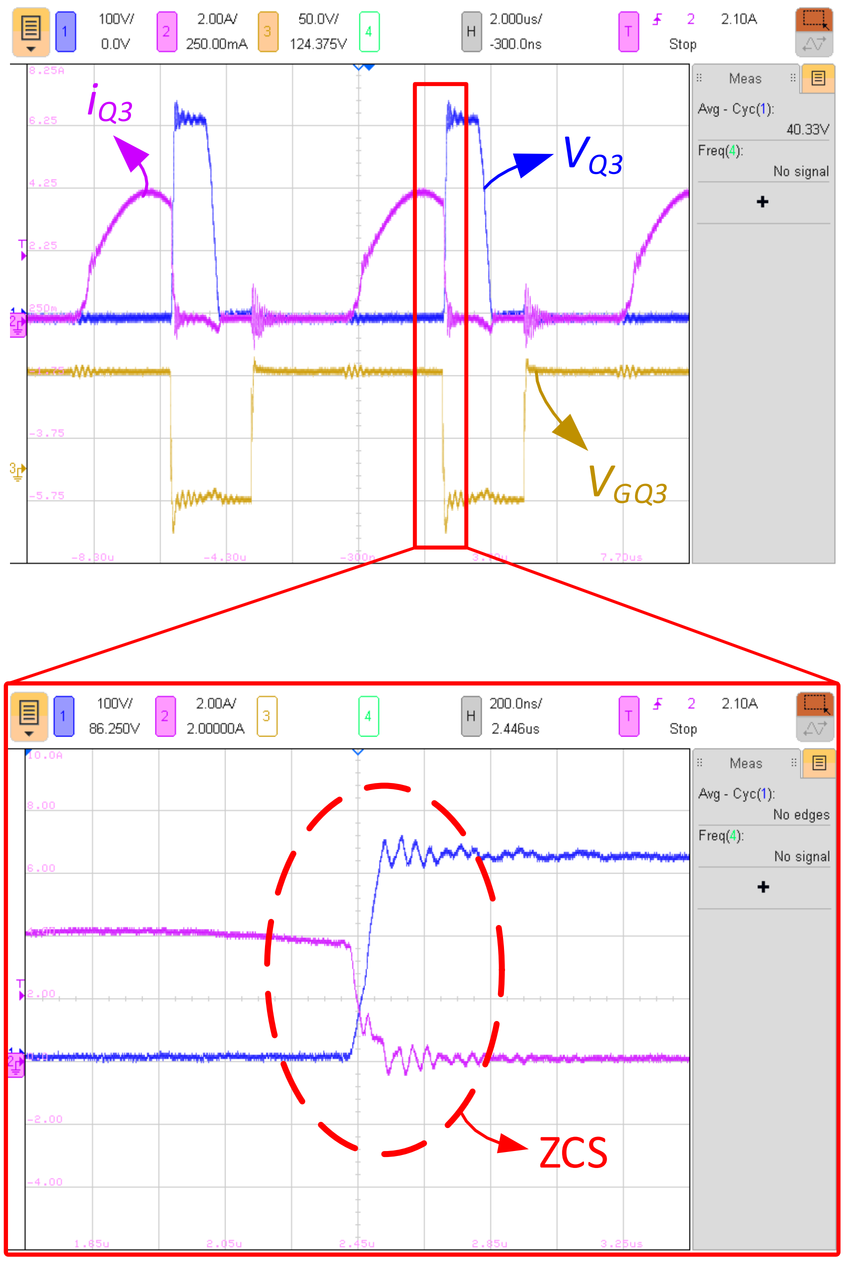


Figure 4.23- Experimental waveforms of the converter in boost mode in mode 2 for a V_i = 500V. The drain-source voltage across Q_3, the current passing through Q_3 and the gate signal applied to Q_3

mode 1 to mode 2 and at the same time, applying a high-frequency PWM signal to the middle switches (Q_3 and Q_4). Figure 4.22 demonstrates the input voltage, output voltage, the current going through the middle switch (i_{Q3}), and the current through S_1. Figure 4.23 shows the PWM signals applied to the middle switches to regulate the output voltage. The drain-source voltage of Q_3 along with its current and the gate signals are given in Figure 4.23. As can be seen, ZVS and ZCS are realized.

In the next scenario, the dynamic response of the proposed comprehensive control system in mode 2 is investigated by applying a step input voltage and increasing the input voltage from 500VDC to 700VDC in Figure 4.24. The input and output voltage of the converter along with the current passing through the middle switches in the rectifier block and the current going through S_1 are demonstrated in Figure 4.25. In Figure 4.25, it is clear that the comprehensive control system is able to provide ZVS for the switches in the inverting block.

In order to examine the performance of the control system when transitioning from mode 2 (PWM) to mode 3 (VFM in FW), the input voltage is increased from 700VDC to 775VDC while the control regulates the output voltage at 700VDC. In doing so, the switching frequency hits the bottom limit, therefore the control moves from mode 2 to mode 3. In mode 3, the PWM signals applied to the middle switches in the rectifier block are removed, and Q_3 and Q_4 are turned OFF and the control system regulates the output voltage by varying the operating frequency. The dynamic response of the converter transitioning from mode 2 to mode 3 is shown in Figure 4.26. As can be seen in Figure 4.27, same as the previous scenarios, in this case, all of the semiconductor devices experience ZVS and ZCS.

In mode 3, same as mode 1, in order to investigate the functionality of the VFM, a step-change in the input voltage is made and the performance of the comprehensive control system is monitored. The input voltage is increased from 775VDC to 825VDC. The VFM control in

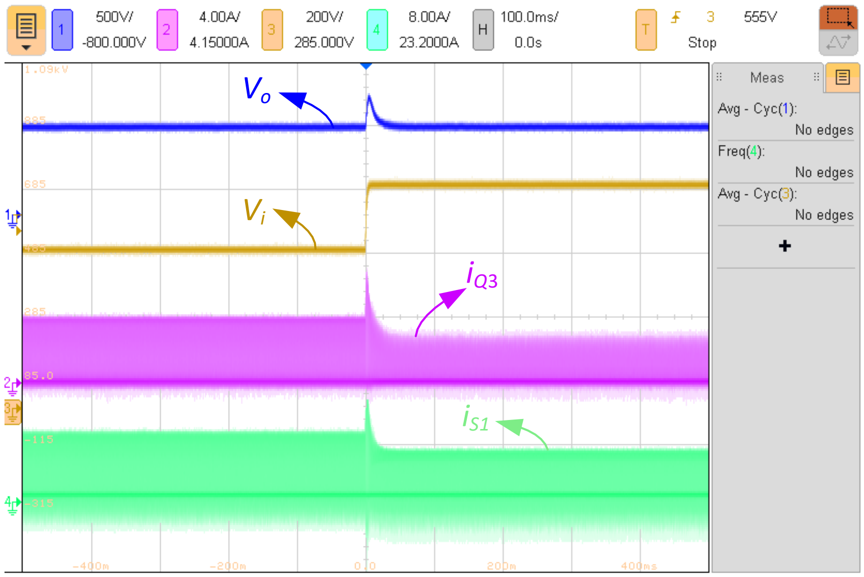


Figure 4.24- Dynamic response of the converter in boost mode in mode 2 for a step change in V_i (500V to 700V). The input and output voltage, and the current passing through S_1 and Q_3.

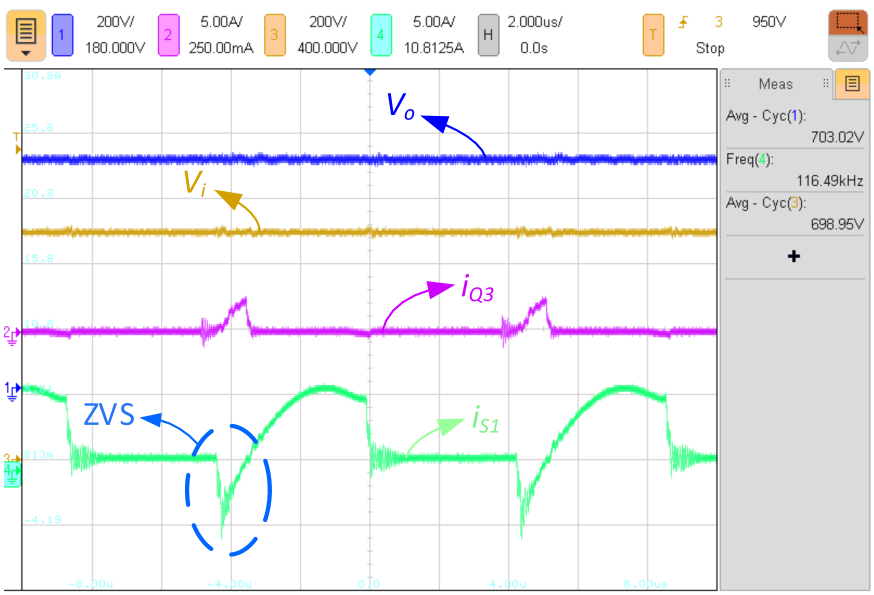


Figure 4.25- Experimental waveforms of the converter in boost mode in mode 2 for a V_i = 700V. The input and output voltage, and the current passing through S_1 and Q_3.

mode 3 regulates the voltage at 700VDC while providing ZVS for all of the switches. Figure 4.28 and Figure 4.29 demonstrate the dynamic response of the VFM control in mode 3.

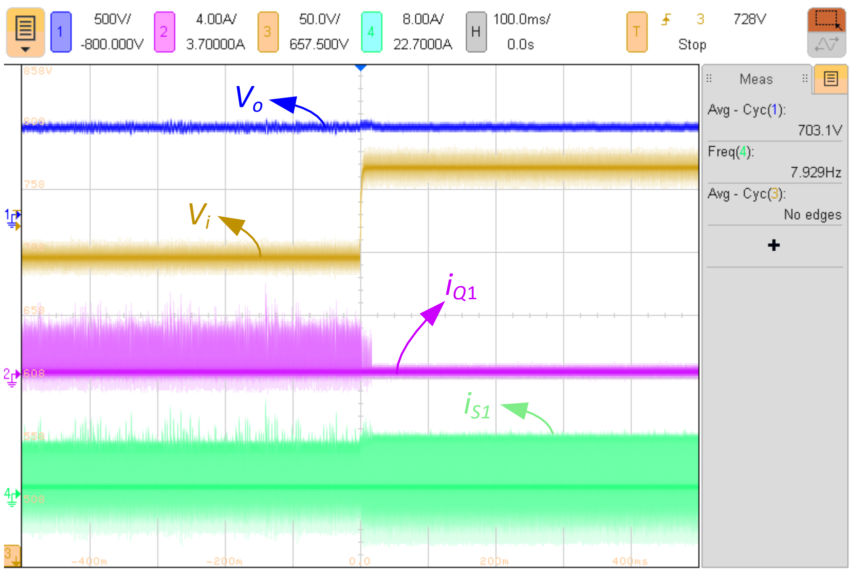


Figure 4.26- Dynamic response of the converter in boost mode transitioning from mode 2 to mode 3 for a step change in V_i (700V to 775V). The input and output voltage, and the current passing through S_1 and Q_3.

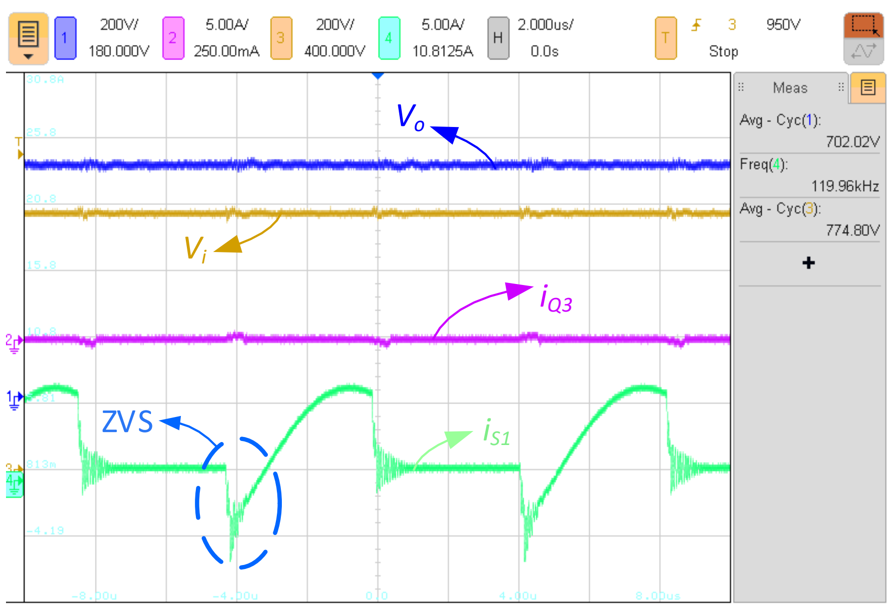


Figure 4.27- Experimental waveforms of the converter in boost mode in mode 3 for a V_i = 775V. The input and output voltage, and the current passing through S_1 and Q_3.

By increasing the input voltage from 825VDC to 875VDC, as the comprehensive control system tries to regulate the output voltage, the operating frequency exceeds the upper limit. Hence, the control moves from mode 3 (VFM in FW) to mode 4 (APWM).

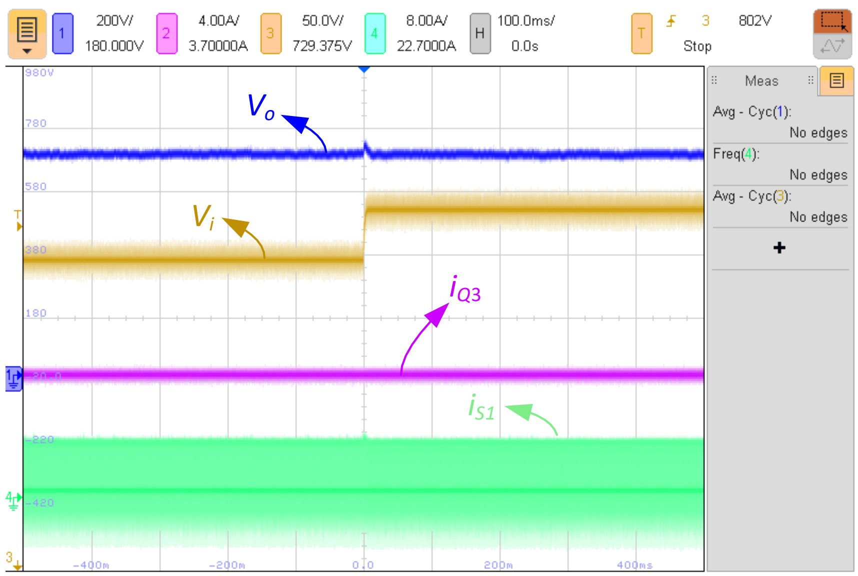


Figure 4.28- Dynamic response of the converter in boost mode in mode 3 for a step change in V_i (775V to 825V). The input and output voltage, and the current passing through S_1 and Q_3.

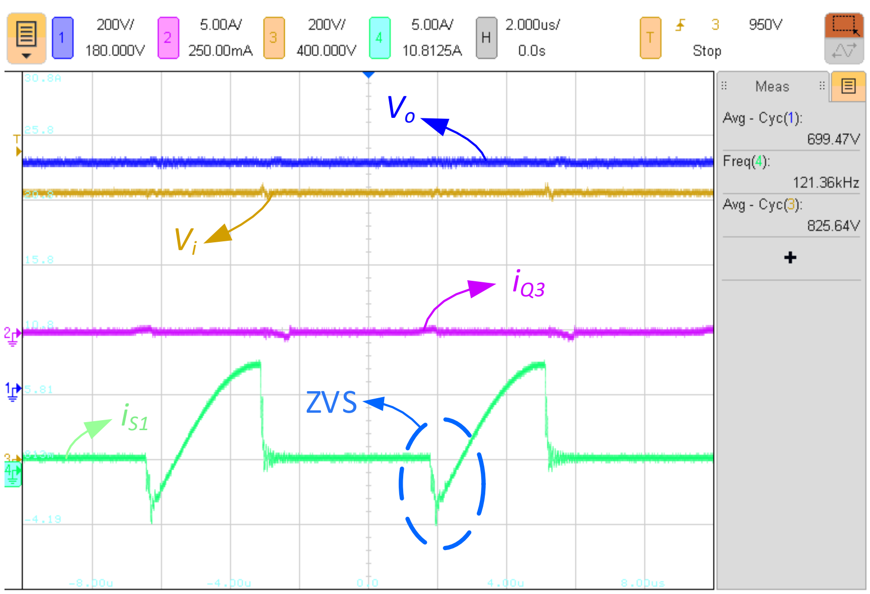


Figure 4.29- Experimental waveforms of the converter in boost mode in mode 3 for a V_i = 825V. The input and output voltage, and the current passing through S_1 and Q_3.

The dynamic performance of the comprehensive control transitioning from mode 3 to mode 4 is depicted in Figure 4.30 and Figure 4.31. In mode 4, by keeping the operating frequency at its upper limit and changing the duty ratio of the inverting side switches (S_1, S_2, S_5, and S_6), the output voltage is regulated at 700VDC.

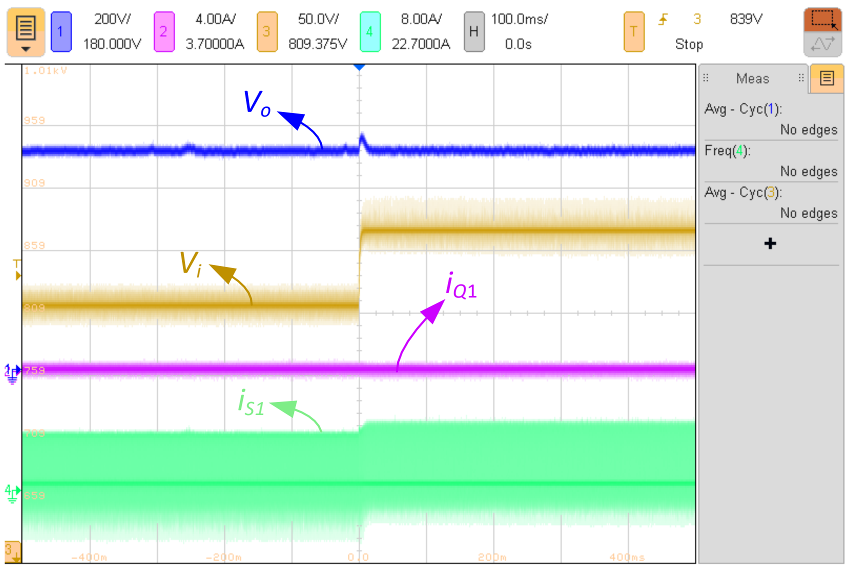


Figure 4.30- Dynamic response of the converter in boost mode transitioning from mode 3 to mode 4 for a step change in V_i (825V to 875V). The input and output voltage, and the current passing through S_1 and Q_3.

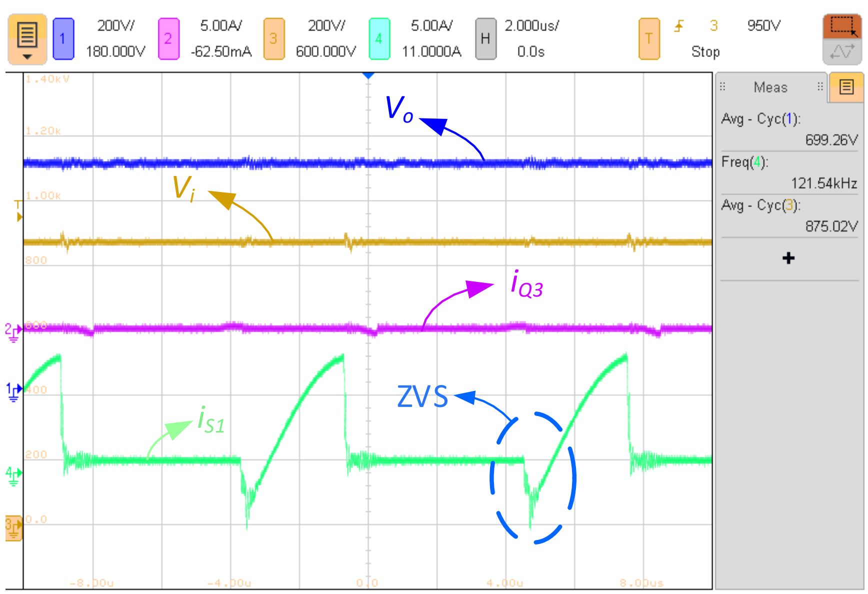


Figure 4.31- Experimental waveforms of the converter in boost mode in mode 4 for a V_i = 875V. The input and output voltage, and the current passing through S_1 and Q_3.

In the final scenario, the performance of the APWM loop in mode 4 is examined by applying a step-change in the input voltage increasing from 875VDC to 950VDC. As can be seen in Figure 4.32 and Figure 4.33, the comprehensive control system successfully regulates the output voltage on 700VDC while providing ZVS and ZCS for all of the semiconductor switches.

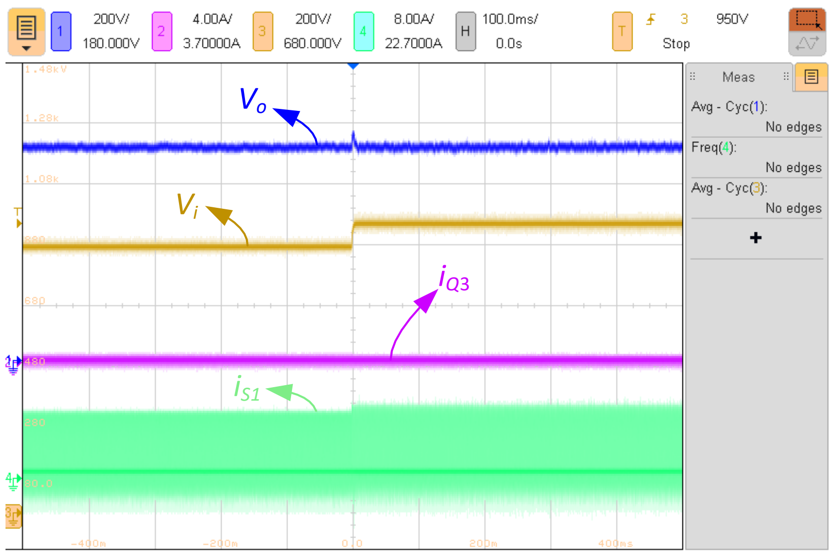


Figure 4.32- Dynamic response of the converter in boost mode in mode 4 for a step change in V_i (875V to 950V). The input and output voltage, and the current passing through S_1 and Q_3.

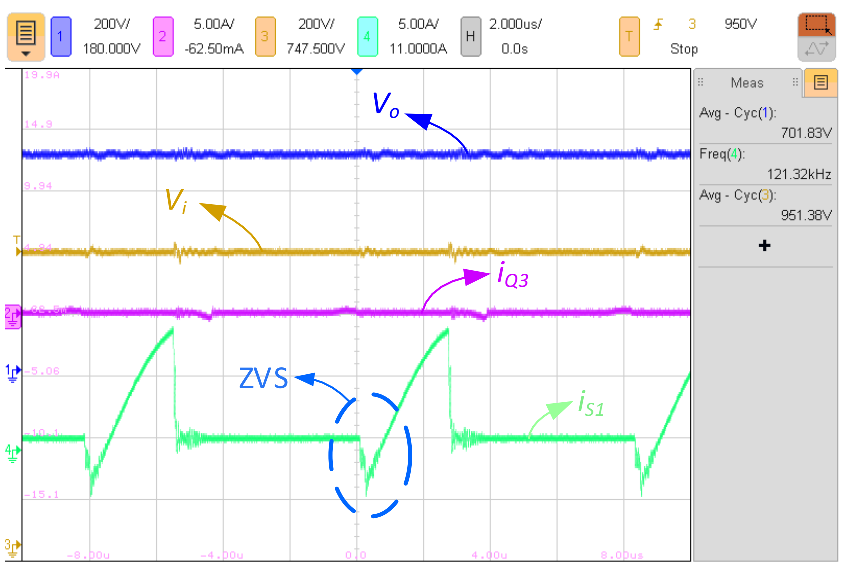


Figure 4.33- Experimental waveforms of the converter in boost mode in mode 4 for a V_i = 950V. The input and output voltage, and the current passing through S_1 and Q_3

In the proposed comprehensive control system, in order to examine the functionality of the voltage balancing loop, a small offset in the value of the capacitance is introduced in the DC link capacitors. Therefore, without the use of the voltage balancing control, as shown in Figure 4.34, the rectifier block experiences unbalanced voltage distribution over the DC link

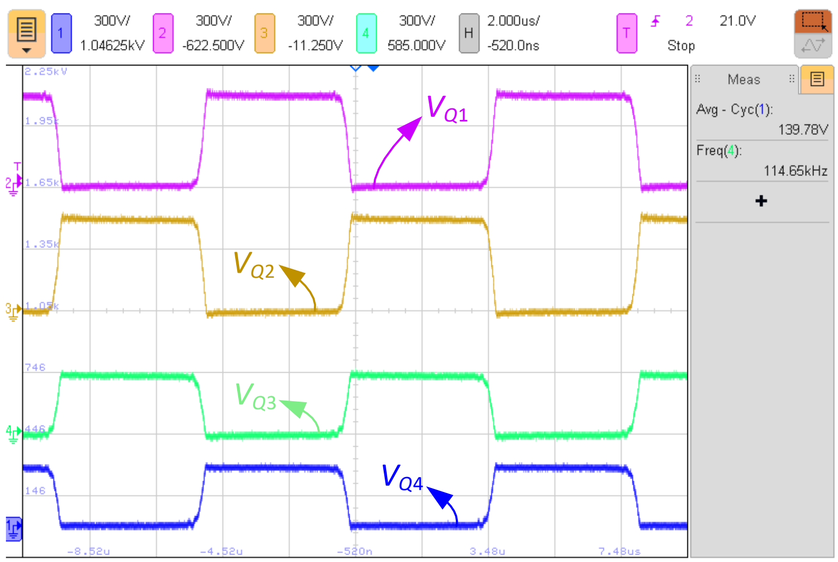


Figure 4.34- Experimental waveforms of the converter in boost mode in mode 1. Voltage stress over the switches in the rectifier block without the voltage balancing control

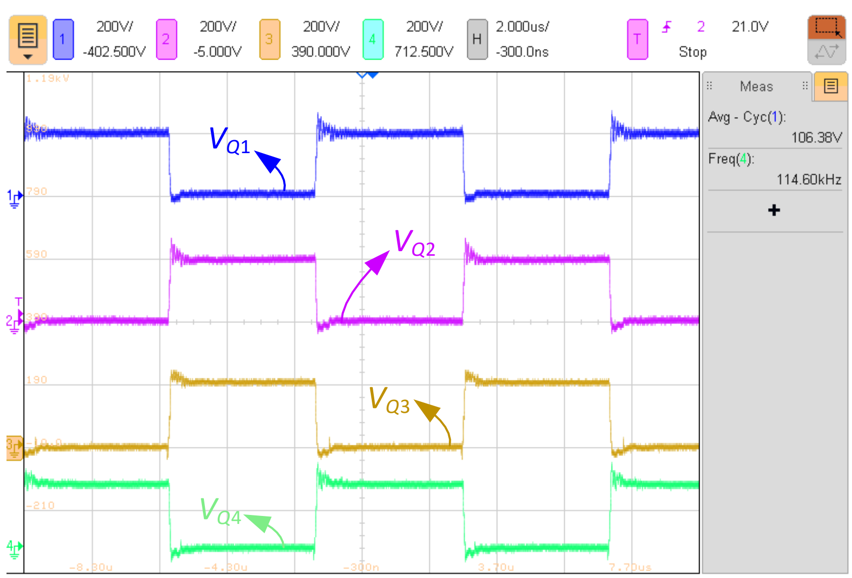


Figure 4.35- Experimental waveforms of the converter in boost mode in mode 1. Voltage stress over the switches in the rectifier block with the voltage balancing control

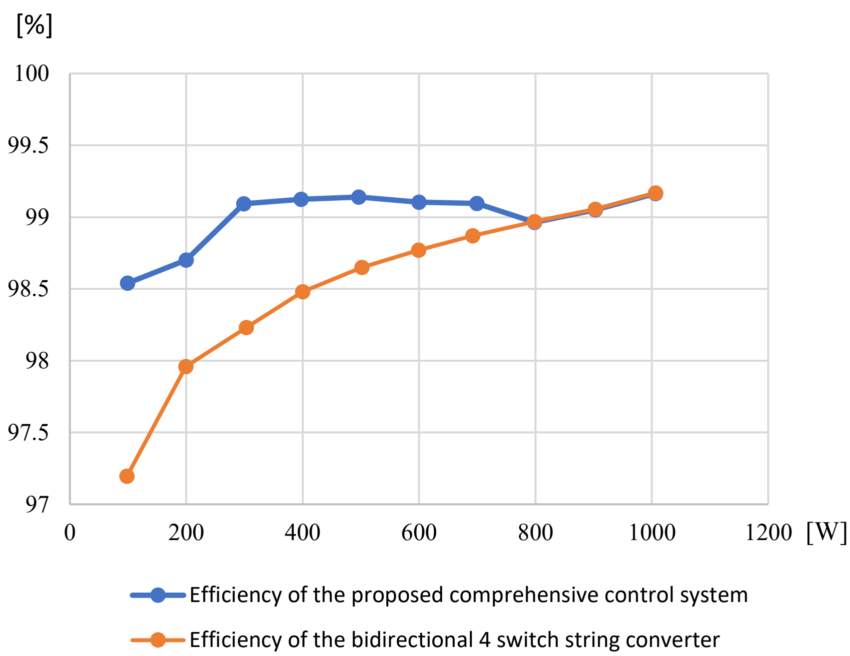


Figure 4.36- Efficiency curve of the proposed topology compared with that of the conventional 4-switch string converter

capacitors. However, in the proposed control system, by applying appropriate gate signals to the middle switches (Q_3 and Q_4) the voltage over the capacitors is balanced as demonstrated in Figure 4.35.

The comparison between the efficiency of the proposed multi-mode stacked-switch converter with the proposed comprehensive control system and the conventional 4-switch string converter with a variable frequency control in boost operating mode is provided in Figure 4.36. As can be seen, the proposed comprehensive control system in the multi-mode stacked-switch converter results in an almost flat efficiency curve for different loading conditions.

Table 4.3 compares the performances of the control systems in various converters moving from a gain of A to a gain of D in Figure 4.10. As can be seen, by means of the proposed hybrid comprehensive control system, the output voltage has been regulated within by increasing the switching frequency within a narrow range.

Table 4.3- Comparison between the performances of different converter topologies

Topology	f_s (kHz) to achieve a gain of		Δf_s (kHz)
	A	D	
4-switch string converter with FM	115.5	168.75	53
The proposed converter in FW with FM	86.25	225	138
The proposed converter with 3-mode control	115.5	131.25	15.75
The proposed converter with 4-mode control	115.5	121.5	6

4.4. Chapter Summary

In this chapter, a wide-gain comprehensive control system is proposed in the multi-mode stacked-switch converters. The proposed control system includes 4 modes of operation including 3 closed-loops (VFM, PWM, APWM). By utilizing the multi-mode operation of the proposed leg to switch between HW/VD and FW and by replacing the low-frequency middle switches with high-frequency MOSFETs and applying high-frequency gate signals in PWM control in the rectifier block, the proposed control system enables the converter to regulate the output voltage for a wide gain range for various loading conditions with a narrow switching frequency range while providing soft-switching for all of the semiconductor devices.

In addition to the voltage regulation loops, due to the non-self-voltage balancing operation of the 4-switch string converter over the input and output capacitors, two voltage balancing loops are developed in the proposed comprehensive control system. By introducing an offset between the duty ratios of the middle switches resulting from the voltage balancing loops, the voltages across the input and output capacitors are balanced.

In the final section of this chapter, a 1kW, >100kHz, 400VDC/700VDC proof-of-concept prototype is designed to investigate the functionality of the proposed comprehensive control system. By introducing various voltage steps at the input of the converter, the performance of the control system is monitored. By switching between different modes of operation, the converter is able to regulate the output voltage for a wide input voltage range (400VDC to 950VDC) within a narrow switching frequency range while providing ZVS and ZCS for all of the semiconductor devices. In addition, the proposed control is able to successfully balance the voltage across the input/output capacitors.

Chapter 5. Conclusions and Future Work

5.1. Conclusions

In the past few decades, due to an increase in earth pollution, the rapid growth of energy consumption, and the serious energy crisis, the promotion and use of clean energy and deployment of renewable electricity technologies continue to grow. While the advancement in renewable energies is exciting and promising, their non-dispatchable and intermittent nature creates significant technical challenges to the power industry and as the penetration level of renewable generation increases over time, such high fluctuations in generation create critical power quality concerns. Energy storage systems assist renewable energy integration in many ways and enable a decent power balance during a power crisis.

Bidirectional power converters are key in the integration of the RES and ESS into the grid. In general, the converter utilized for this purpose consists of a bidirectional AC/DC converter followed by a bidirectional DC/DC converter. The bidirectional DC/DC converter controls the battery charge and discharge, and prolongs its service life, and reduces the operation and maintenance costs of the entire power generation system. Hence, developing a reliable and effective power converter with proper topology to ensure optimum operation of the ESS is essential.

In conventional ESS in EV or net-zero houses, a bulky, heavy, and relatively low-frequency transformer is used to provide galvanic isolation and enable bidirectional power transfer. In addition, traditional hard-switching power converters with Silicon made switches had the major share of the market for high power applications where the associated power loss leads to a dramatic increase in the operating temperature and complicated cooling systems including large heat-sinks and fans are needed to address the temperature issue and prevent the components from being damaged. Furthermore, the conventional topologies of power converters have a limited gain and the efficiency suffers in low load conditions.

In general, the traditional power converters in EVs, net-zero houses and power system level energy storage systems face at least one of the following challenges including: (1) hard-switching/limited soft-switching condition; (2) high voltage stress over the switches ;(3) lack of voltage balancing technique and asymmetrical loss distribution over the switches; (4) relatively low switching frequency range; (5) lack of fault-tolerant operation control; (6) low efficiency at light loads, and (7) narrow voltage gain region. The above challenges inspired the research for developing a novel topology and control system.

The contributions of this thesis are summarized and are highlighted in the next section.

5.2. Contributions

High penetration of wind and solar into the power grid is problematic due to their intermittency and unpredictability. This problem can be solved, at least in principle, with sufficient energy storage, but large scale energy storage is currently quite expensive, and in any case including storage represents an addition cost to the price of renewable electricity beyond the costs of generation. Increasing the number of reduced-sized energy storage units in a 100% carbon-free electricity portfolio is therefore a high priority.

The bidirectional power converter protects the battery by controlling the discharge current of the battery, prolongs its service life, and reduces the operation and maintenance costs of the entire power generation system. Power conversion systems mainly employ line-frequency transformers to achieve galvanic isolation and voltage matching. Rapid development of distributed generation and energy storage has led to the increasing popularity of power conversion systems as an ever-lasting key interface. However, bulky, heavy, lossy, and noisy line-frequency transformers hinder the efficiency and power density of power conversion systems.

The use of high-frequency power converters is considered to be the developing trend of next-generation power conversion. The advantages of high-frequency power converters are low volume, light weight, and low cost. High frequency power conversion systems based on high-frequency transformers can also avoid voltage and current waveform distortion. In addition, when the switching frequency is above 20 kHz, the power converter noise can be greatly reduced.

The contributions of this thesis are summarized below:

1. A novel multi-mode stacked-switch inverter/rectifier leg is proposed and analyzed for use in bidirectional power conversion for energy storage applications. The presented leg provides multiple operating modes and enables the converter to operate in rectifying mode with a much lower output voltage ripple compared to that of the conventional 4-switch string converter with the same capacitive filter.
2. A bidirectional soft-switched converter utilizing a *CLLC* resonant circuit along with the proposed multi-mode stacked-switch legs in both inverter and rectifier blocks has been presented and analyzed in which Zero voltage switching (ZVS) turn-ON and close-to-zero current switching (ZCS) turn-OFF for all semiconductor switches are realized. By employing a high-frequency modulation technique in the proposed control system, a high gain can be achieved and the need for high turns-ratio step-up transformers has been eliminated. The proposed converter is able to transfer power in both directions and charge/discharge the ESS as needed.
3. Open-circuit fault (OCF) incidents in the rectifier block of the multi-mode stacked-switch converter are investigated and analyzed in detail. A fault-tolerant control through the built-in circuit redundancy operation of the presented leg has been developed which enables post fault operation of the converter and allows the power to be transferred continuously with soft-switching operation in the case of any of the switches experiencing an OCF.
4. A novel comprehensive hybrid control system based on circuit redundancy is proposed in the multi-mode stacked-switch converter. By means of the developed control system, the voltage gain range is widely extended within a narrow switching range. In addition,

the efficiency of the converter is improved significantly especially for light loads, and an almost flat efficiency curve is achieved within different loading conditions.

5. By replacing the low-frequency middle switches with high-frequency switches, applying high-frequency pulse-width modulated signals and introducing an offset between the duty ratios of the middle switches resulting from the voltage balancing loops, the non-self-voltage balancing operation of the converter over the input and output capacitors is compensated and the voltage across the capacitors are balanced.
6. The performance of the proposed bidirectional DC/DC converter in this thesis has been verified through simulation as well as experimental results on a laboratory-scale proof-of-concept prototype. The thorough design procedure of the converter presented in this thesis along with the analysis of the closed-loop control system has also been provided. In addition, the performance of the developed fault-tolerant control and the comprehensive hybrid control system have been investigated in detail.

5.3. Future Work

With regards to the research conducted in this thesis, some future works related to this thesis are summarized below:

1. While open-circuit faults have been considered to be the main focus of the developed fault-tolerant control system, the impact of short-circuit faults (SCF) in the proposed converter can be investigated in detail and proper short-circuit fault-tolerant control can be integrated into the existing comprehensive control system. In addition, state-of-the-art fault detection approaches can be examined to reduce the detection time and improve the performance of the fault-tolerant control.
2. In the presented comprehensive hybrid control system, 4 modes of operation have been developed to regulate the output voltage (mode 1: VFM in HW, mode 2: PWM, mode 3: VFM in FW, and mode 4: APWM in FW) and 3 control variables have been used to regulate the output voltage namely, switching frequency (f_s), the duty ratio of the inverting side switches (D_s) and the duty ratio of the middle switches in the rectifying block (D_q).

   In mode2, the PWM signals applied to the middle switches have the same switching frequency as the inverting side switches. In addition, the impact of the phase-shift modulation between the inverter and the rectifier blocks has not been considered. By introducing an additional control variable into the control system, the performance of the comprehensive control system can be enhanced and the voltage gain range of the converter can be further extended with an improved efficiency curve.

3. While the proposed multi-mode stacked-switch converter has proven to be a perfect candidate to be used in bidirectional DC/DC power conversion, a single-stage bidirectional AC/DC converter can be developed based on the modified multi-mode stacked-switch leg along with a proper control technique to integrate the energy storage system into the grid.

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Appendix A List of Publications

The following is a list of publications by the author during doctoral studies.

A.1 Refereed Journal Papers

[1] R. Emamalipour and J. Lam, "Fault-Tolerant Operation of a Multi-Mode Stacked-Switch Rectifier Leg through Built-In Circuit Redundancy," *Accepted for publication in the IEEE Transactions on Industry Applications (accepted in February 2022)*.

[2] Abbasi, M., Emamalipour, R., Cheema, M. A. M., and Lam, J., "A step-up reconfigurable multi-mode LLC converter module with extended high efficiency range for wide voltage gain application in medium voltage DC grid systems". *Accepted for publication in the IEEE Transactions on Power Electronics. (accepted in January 2022)*

[3] R. Emamalipour and J. Lam, "A Hybrid String-Inverter/Rectifier Soft-Switched Bidirectional DC/DC Converter," *IEEE Transactions on Power Electronics, vol. 35, no. 8, pp. 8200-8214, Aug. 2020*.

A.2 Refereed Conference Papers

[1] R. Emamalipour and J. Lam, "Voltage Balancing Feature and Output Regulation in a Multi-Mode Inverter/Rectifier Leg," *to appear in Proc. of the 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), 2022. (accepted in October 2021).*

[2] R. Emamalipour and J. Lam, "Open Circuit Fault-tolerant Operation of a Modified Hybrid String Inverter/Rectifier Leg," IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society, 2021, pp. 1-5.

[3] R. Emamalipour and J. Lam, "Built-in Circuit Redundancy and Fault-tolerant Operation of a New Multi-Mode Hybrid String Inverter/Rectifier Leg," 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), 2021, pp. 626-631.

[4] R. Emamalipour and J. Lam, "A New AC/DC Half-Bridge/String-Inverter Hybrid-Structured Isolated Bi-directional Converter," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), 2019, pp. 2713-2718.

[5] R. Emamalipour and J. Lam, "A new non-multi-level structured, H-bridgeless DC/DC bidirectional converter with low voltage stress and complete soft-switching operation," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2019, pp. 2322-2328.